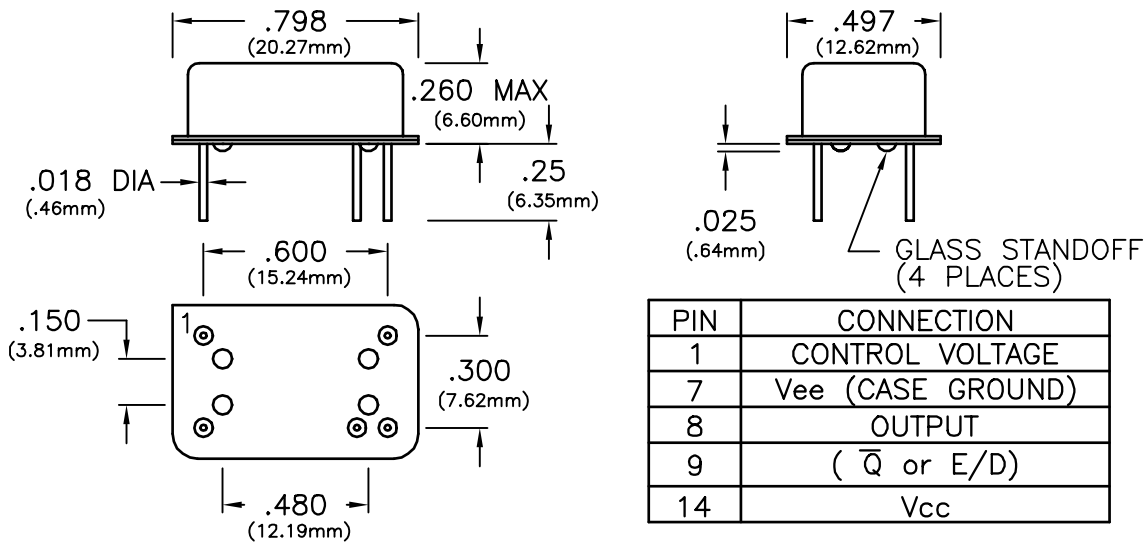
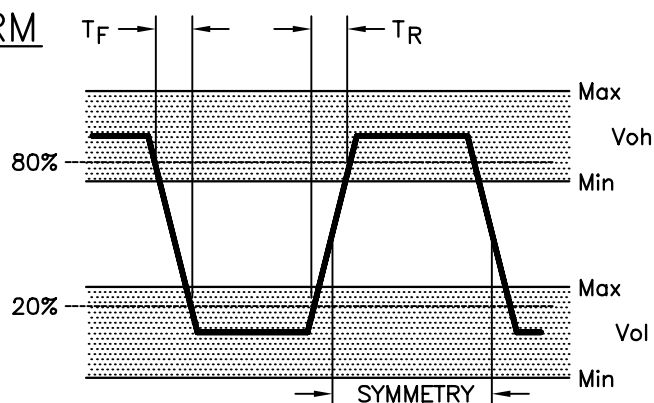


14 PIN DIP PLL-BASED PECL VCXO

SPECIFICATIONS	GV23-52*	GV23-53*	GV23-54*	GV23-62*	GV23-63*	GV23-64*	
Available Frequency Ranges	120 to 135 MHz 144 to 168 MHz 174 to 205 MHz 232 to 270 MHz 288 to 336 MHz 348 to 410 MHz 464 to 540 MHz 576 to 672 MHz			144 to 168 MHz 174 to 205 MHz 288 to 336 MHz 348 to 410 MHz 576 to 672 MHz			
Frequency Stability	±50ppm	±100ppm	±20ppm	±50ppm	±100ppm	±20ppm	
Operating Temp Range	0°C to +70°C			-40°C to +85°C			
Storage Temp Range	-55°C to +125°C						
Output	Waveform	PECL Squarewave , 100K Compatible					
	Load	Output must be terminated into 50 Ohms to 3Vdc.					
	Voltage	Voh	4.0V Minimum , 4.5V Maximum				
		Vol	2.9V Minimum , 3.4V Maximum				
	Symmetry	45/55 Maximum measured at 50% level					
	Rise/Fall Time	750pS Maximum					
	Jitter	10pS rms Maximum					
	SSB Phase Noise	-100dBc/Hz typical @ 10KHz offset					
Frequency Control	Positive Transfer Characteristic						
Control Voltage	0 to 5Vdc						
Deviation @25°C	±75ppm Minimum , ±140ppm Maximum						
Center Frequency @25°C	Control Voltage 2.5Vdc ±0.5Vdc						
Linearity	< ±10%						
Input Impedance	> 50K ohms at < 10KHz						
Enable/ Disable Option (Pin 9):	Enable (Vil)	0.5Vdc Maximum					
	Disable (Vih)	1.5Vdc Minimum					
	Q (Pin 8) disables to low state. When Pin 9 is floating, output is in disabled state.						
Supply Voltage	+5Vdc ±5%						
Supply Current	100mA Maximum						
Package	All metal, hermetically sealed, welded package						
Options * - add suffix to model number	1	Pin 9: Complementary Output					
	2	Pin 9: Enable/Disable					



OUTPUT WAVEFORM



TEST CIRCUIT

