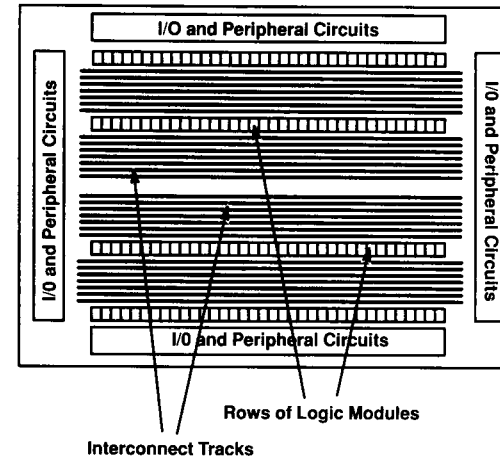
SRFS001F – D3864, DECEMBER 1989 – REVISED FEBRUARY 1993

- **Four Arrays With up to 2000 Usable Equivalent Gates**
- **TI Action Logic™ System (TI-ALS) Software for:**
  - **View*Logic*™**
  - **Mentor™**
  - **OrCAD/SDT III™**
  - **Cadence™/Valid™**
- **Reliable Antifuse Interconnect**
- **Built-In Clock Distribution Network**
- **Silicon-Gate CMOS Technology**
- **Desktop TI-ALS Creates Design Files for:**
  - **I/O Pin Assignment**
  - **Design Validation**
  - **Place and Route**
  - **Circuit Timing Analysis**
  - **Array Antifuse Programming**
  - **Test and Debug**



TPC10 Series FPGA Die Architecture

description

The Texas Instruments (TI) TPC10 Series comprises four field-programmable gate arrays (FPGAs). The TPC1010A, TPC1010B, TPC1020A, and TPC1020B FPGAs are fabricated using the TI silicon-gate CMOS process. The process features polysilicon gate, source, drain elements, and two levels of copper-doped-aluminum metallization to reduce internal resistance and enhance performance. Typical die architecture is illustrated above.

These field-programmable devices combine gate-array flexibility with desktop programmability. This combination allows the designer to avoid fabrication cycle times and nonrecurring engineering charges associated with conventional mask-programmed gate arrays. The FPGAs are unique in that the arrays are fabricated, tested, and shipped to the user for programming. The FPGA contains user-configurable inputs, outputs, logic modules, and minimum-skew clock driver with hardwired distribution network. The FPGA also includes on-chip diagnostic probe capabilities and security fuses to protect the proprietary design.

Table 1. Product Family Profile

DEVICE	TPC1010A	TPC1020A	TPC1010B	TPC1020B
Capacity				
Gate array equivalent gates	1200	2000	1200	2000
TTL equivalent packages	34	53	34	53
CMOS Process	1.2 µm	1.2 µm	1.0 µm	1.0 µm
Logic Modules	295	547	295	547
Flip-Flops (maximum)	130	273	130	273
Antifuses	112,000	186,000	112,000	186,000
Horizontal Tracks	22	22	22	22
Vertical Tracks	13	13	13	13

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OrCAD/SDT III is a trademark of OrCad Systems Corporation.
View*Logic* is a trademark of Viewlogic System, Incorporated.

Action Logic System (ALS) and Activator

TPC10 Series FPGAs are supported by the ALS software and Activator™ programming hardware. The combination facilitates logic design and FPGA programming on popular CAE workstations with minimum effort. ALS interfaces to the resident CAE system providing a complete library of TPC10 Series functions. The ALS includes automatic place and route, timing verification, and FPGA device programming. The ALS and Activator are available for View*Logic* or OrCAD (SDT III) 386/486 based PC systems, Mentor-equipped Apollo workstations, and View*Logic*- or Valid/Cadence-equipped Sun-4 workstations.

library functions

The TPC10 Series FPGA library contains over 250 logic building blocks of hardwired and soft macros. The hardwired macros provide a wide selection of predesigned, fully characterized functions. The soft macros provide popular MSI functions that can be called into the design. Additional user-defined soft macros can be created using the TPC10 library macros. The library contains the following classes of macros:

- Primitive Gates, Booleans, and Buffers
- CMOS, TTL, and Clock Buffer Inputs and Totem-Pole, 3-State, and I/O Output Buffers
- Adders and Multiplexers
- D-Type Flip-Flops
- J-$\overline{K}$ Flip-Flops
- Latches
- MSI Complexity Soft Macros

design flow

Custom logic functions, designed in conjunction with the TPC10 Series FPGA library, can be simulated and verified prior to creating the ALS design data base and programming files. Figure 1 provides an overview of the design flow.

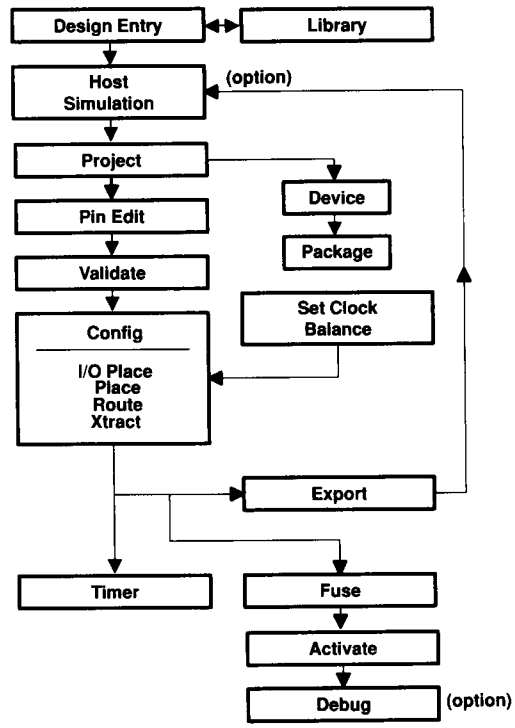


Figure 1. Design Flow

Table 2. TI-ALS Design Configurations (see Note 1)

HARDWARE PLATFORM	LIBRARY/CAE HOST ENVIRONMENT	DESIGN SUPPORT (gates)		TI SUSTEM PART NUMBER
		UP TO 2500	UP TO 10000	
386/486-based PC	View*Logic*	X		TPC-ALS-DS–PC-VL
	View*Logic*		X	TPC-ALS-DA–PC-VL
	OrCAD	X		TPC-ALS-DS–PC-OR
	OrCAD		X	TPC-ALS-DA–PC-OR
Sun	Cadence		X	TPC-ALS-DA–SN-CD
	Mentor		X	TPC-ALS-DA–SN-MG
	Valid		X	TPC-ALS-245†
	View*Logic*		X	TPC-ALS-DA–SN-VL
HP700	Mentor		X	TPC-ALS-DA-HP7-MG
DN4000/ HP400				TPC-ALS-235†

NOTE 1: Authorization codes for design systems are supplied upon request, after receipt of the system.

† The TPC-ALS-235 and TPC-ALS-245 systems only provide support for the TPC10 and TPC12 series, and will not be supported in Revision 3.0 scheduled for release in the fourth quarter of 1993. These systems are being replaced by TPC-ALS-DA-HP7-MG and TPC-ALS-DA-SN-CD, respectively.

Table 3. TI-ALS Programming Configurations (see Note 2)

HARDWARE PLATFORM	CAE HOST ENVIRONMENT	DESIGN SUPPORT		TI SUSTEM PART NUMBER
		ONE DEVICE	FOUR DEVICES	
386/486-based PC	View*Logic* /OrCAD	X		TPC-ALS-DS–P2S-PC
			X	TPC-ALS-219
Sun	Cadence/Mentor/ Valid/View*Logic*	X		TPC-ALS-DS–P2S-SN
			X	TPC-ALS-249
HP700	Mentor	X		TPC-ALS-DS–P2S-HP7
			X	TPC-ALS-DS–P2-HP7
HP400	Mentor	X		TPC-ALS-DS–P2S-HP4
			X	TPC-ALS-DS–P2-HP4
DN Series	Mentor		X	TPC-ALS-239

NOTE 2: Programming units are compatible with both high (10000 gates) and low (2500 gates) density systems.

architecture

device organization

Each FPGA consists of a matrix of logic modules arranged in rows separated by channels containing interconnect tracks. The matrix is surrounded with peripheral inputs, outputs, I/Os, and diagnostic circuits. A partial view of the TPC10 Series logic modules with examples of interconnections is illustrated in Figure 2.

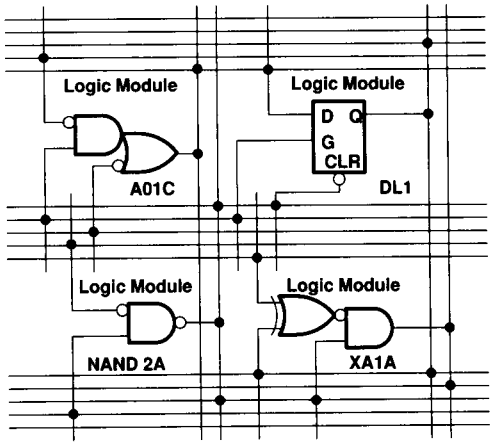


Figure 2. Partial View of TPC10 Series Interconnection Capability

logic module

Each core logic module has the equivalent complexity of four 2-input NAND gates. The module shown in Figure 3, is an 8-input, 1-output gate cluster that can implement hardwired primitive gates, Booleans, latches, flip-flops, multiplexers, half or full adder slices, or multiplexed-input flip-flops. The TI-ALS library contains a full spectrum of 2-, 3-, and 4-input AND, NAND, OR, and NOR gate macros covering all derivatives of true and/or complement input combinations. Similar modular implementations, covering the spectrum of true and/or complement input combinations, are included for each functional category of macros in the library. Latches and flip-flops are created by connecting two or more logic modules in the appropriate circuit configuration. The macros are captured, simulated, placed, analyzed, and programmed using the TPC10 design library.

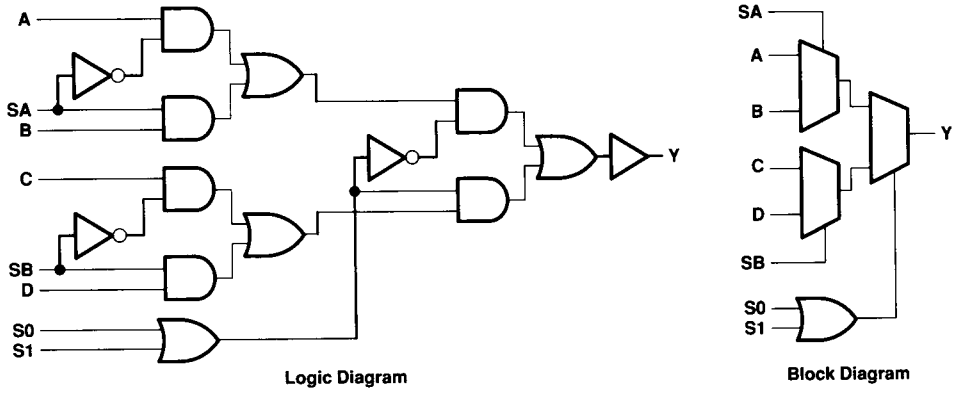


Figure 3. TPC10 Series Logic Module

interconnect tracks

The channeled interconnect tracks consist of isolated metal segments that can be connected by addressing and programming antifuses. Each channel has 25 horizontal routing tracks, 22 are for logic, one is for clock, one is for power, and one is for ground. In addition, there are 13 vertical routing tracks per logic module column. Both horizontal and vertical tracks, in combination with the approximately 340 antifuses per logic module, produce a network that is capable of interconnecting up to 90 percent of the equivalent gates. Based on the placement of macros, the programming process selects and activates antifuses that both create the logic module macros and I/Os, and interconnect the entire array.

I/O buffers

Each I/O pin is configurable as an input or an output. In addition, I/O pins configured as outputs can be defined as totem-pole, 3-state, or bidirectional. Inputs can be driven by CMOS or TTL levels and output levels are compatible with standard CMOS and TTL specifications. Outputs sink or source a current of 4 mA at TTL output levels. See the dc characteristics for additional I/O buffer specifications. The I/Os can be manually assigned to any available package pin, or the ALS software can automatically place the I/Os in the optimum configuration.

diagnostic probe pins

TPC10 Series devices have two independent diagnostic probe pins, PRA and PRB. The pins allow the user to observe any internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on an oscilloscope, logic analyzer, or with the workstation diagnostics using the Actionprobe diagnostic tools. The probe pins can also be used as user-defined I/Os, depending on the level of the mode control pin. When configured as user-defined I/Os, the pins have the same characteristics as other I/O pins.

security fuses

The TPC10 Series security fuses can be used to permanently disable further diagnostics and testing. After the security fuses are programmed, access to the architecture is not available. This makes the FPGA design difficult to copy.

FPGA array performance

logic module size

A mask-programmed gate array cell with four transistors usually implements only one logic level. The TPC10 Series array logic module is more complex and typically implements multiple logic levels within a single module. This reduces intermodule wiring and associated RC delays. In effect, the TPC10 logic module implements the equivalent of a net compression that enhances performance.

TERMINAL FUNCTIONS

PIN NAME	I/O	DESCRIPTION
CLK	I	Clock. TTL clock input for global clock distribution network. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.
DCLK	I	Diagnostic clock. TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
GND	I	Ground. Input low supply voltage.
I/O	I/O	Input/output. I/O pin functions as an input, output, 3-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically set low by the ALS software.
MODE	I	Mode. The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is high, the special functions are active. When the MODE pin is low, the pins function as I/Os.
NC		No connection. This pin is not connected to circuitry within the device.
PRA	O	Probe A. The probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe B pin to allow real-time diagnostic output of any signal path within the device. The probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRA is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
PRB	O	Probe B. The probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe A pin to allow real-time diagnostic output of any signal path within the device. The probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
SDI	I	Serial data input. Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
V_{CC}	I	Supply voltage. Input high supply voltage.
V_{PP}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range , V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I ..... – 0.5 to V_{CC} + 0.5 V
Output voltage range, V_O ..... – 0.5 to V_{CC} + 0.5 V
Input clamp current‡ , I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current§, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current§, (V_O = 0 to V_{CC}) ..... ± 25 mA
Operating free-air temperature range, T_A: Commercial ..... 0°C to 70°C
Industrial ..... – 40°C to 85°C
Operating case temperature range, T_C: Military ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Applies for input and bidirectional buffers
§ Applies for bidirectional and output buffers

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Commercial	4.75	5	5.25	V
		Industrial	4.5	5	5.5	
		Military	4.5	5	5.5	
V_{PP}	Program pin voltage (while not programming)		V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage		2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
T_A	Operating free-air temperature	Commercial	0	25	70	°C
		Industrial	−40	25	85	
T_C	Operating case temperature	Military	−55	25	125	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (see Note 3)	I_{OH} = −4 mA	3.84									V
		I_{OH} = −3.2 mA				3.7			3.7			
V_{OL}	Low-level output voltage (see Note 3)	I_{OL} = 4 mA			0.33			0.4			0.4	V
I_I	Input current	$V_I = V_{CC}$ or 0			±10			±10			±10	µA
I_{OZ}	Off-state output current	$V_O = V_{CC}$ or 0			±10			±10			±10	µA
I_{OS}	Short-circuit output current (see Note 4)	$V_O = V_{CC}$	20		140	20		140	20		140	mA
		V_O = 0	−10		−100	−10		−100	−10		−100	
I_{CC}	Standby supply current	$V_I = V_{CC}$ or 0, Outputs open		3	10		3	20		3	25	mA
C_{io}	Input/output capacitance (see Note 5)	V_O = 0, f = 1 MHz		7			7			7		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. These limits apply when all other outputs are open.
4. When testing TPC1010A and TPC1020A, not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second. The I_{OS} parameter does not apply to TPC1010B or TPC1020B.
5. These limits apply for each user I/O pin.

switching characteristics

The following tables summarize switching characteristics of various classes of TPC10 Series logic module hardwired macros. An unloaded logic module propagation delay time is 4 ns. All other delays shown include the module delay time and statistical estimates for wiring delays based on 85% to 95% FPGA logic module utilization. Module utilization above 95% can result in performance degradation. Actual delay values are determined after place and route is accomplished using the ALS. ALS provides for assigning criticality to nets, automatic balancing of clock buffer loads, and utilizing long horizontal or vertical nets for connecting noncritical functions. For specific timing parameters pertaining to a hardwired logic module, refer to the individual macro library specification.

The ALS provides a capability to assign one of four levels of criticality to logic module output nets. The switching characteristics reflect the delay time differences for nets with criticality and without criticality assigned. Nets assigned as critical will be limited to a fan-out of 6 loads by the ALS. Clock load balancing, selectable by the designer, can be specified as moderate, strong, or very strong to control clock skew.

timing requirements over recommended operating conditions, no further derating required

				MIN	MAX	UNIT
f_{clock}	Clock frequency				100	MHz
t_w	Pulse duration	CLK, PRE, or CLR	FO = 1	7.7		ns
			FO = 2	8.5		
			FO = 3	9.2		
			FO = 4	10		
			FO = 8	14		
t_{su}	Setup time, flip-flop	All synchronous inputs before clock transition		3.9		ns
t_{su}	Setup time, latch	All synchronous inputs before clock transition	FO = 1	3.5		ns
			FO = 2	3.9		
			FO = 3	4.2		
			FO = 4	4.5		
			FO = 8	4.8		
t_h	Hold time, flip-flop or latch	All synchronous inputs after clock transition		0		ns

typical switching characteristics

single-level logic module hardwired macro (module count = 1), V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME (see Note 6)					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	5.4	5.8	6.2	8.5	See Note 7	ns
t_{pd}	Not critical	6.3	6.7	7.7	8.6	10.8	ns

double-level logic module hardwired macro (module count = 2), V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME (see Note 6)					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	9.2	9.6	10	12.3	See Note 7	ns
t_{pd}	Not critical	10.2	10.6	11.6	12.5	14.6	ns

flip-flop and latch hardwired macro, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	OUTPUT-NET CRITICALITY	DELAY TIME (see Note 6)					UNIT
		FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{pd}	Critical	5.4	5.8	6.2	8.5	See Note 7	ns
t_{pd}	Not critical	6.3	6.7	7.7	8.6	10.8	ns

NOTES: 6. An unloaded logic module propagation delay time is 4 ns. All delays shown include the module delay time and statistical estimates for wiring delays based on 85% to 95% FPGA logic module utilization.
7. Critical nets are limited to a fan-out of 6 loads.

long net, V_{CC} = 5 V, T_J = 25°C, typical process

Long nets include long horizontal and vertical routing resources used for noncritical signals and interconnecting logic macros separated by large distances. Long nets are used by the autorouter when no other means exist to complete the interconnection. Delays due to the use of long nets range from 15 ns to 35 ns. Typically less than one percent of all nets in a design require the use of a long net.

typical switching characteristics

input buffer and bidirectional-input buffer, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	FROM (INPUT)	TO (OUTPUT)	DELAY TIME					UNIT
			FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	
t_{PHL}	Pad	Y	6.9	7.6	8.9	10.7	14.3	ns
t_{PLH}			5.9	6.5	7.7	8.4	12.4	

output buffer, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PHL}	D	Pad	C_L = 50 pF	3.9	4.9	ns
t_{PLH}				7.2	5.7	
Δt_{PHL}	D	Pad		0.03	0.046	ns/pF
Δt_{PLH}				0.07	0.039	

The BIBUF macro's output section exhibits the same delays as the OUTBUF macro. The delta numbers can be extrapolated down to 15 pF minimum.

Example: Delay for an OUTBUF output buffer driving a 100-pF TTL load

t_{PHL} = 4.9 + [(0.046 x (100 – 50)] = 4.9 + 2.3 = 7.2 ns

t_{PLH} = 5.7 + [(0.039 x (100 – 50)] = 5.7 + 2.0 = 7.7 ns

3-state and bidirectional output buffer, V_{CC} = 5 V, T_J = 25°C, typical process

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PHL}	D	Pad	C_L = 50 pF	3.9	4.9	ns
t_{PLH}				7.2	5.7	
t_{PHZ}	E	Pad	See test loads in Figure 8	5.2	3.4	ns
t_{PZH}				6.5	4.9	
t_{PLZ}	E	Pad		6.9	5.2	ns
t_{PZL}				4.9	5.9	
Δt_{PHL}	D	Pad		0.03	0.046	ns/pF
Δt_{PLH}				0.07	0.039	
Δt_{PHZ}	E	Pad		0.08	0.046	ns/pF
Δt_{PZH}				0.07	0.039	
Δt_{PLZ}	E	Pad		0.07	0.039	ns/pF
Δt_{PZL}				0.03	0.039	

clock buffer, V_{CC} = 5 V, T_J = 25°C, typical process (see Note 8)

PARAMETER	FROM	TO	DELAY TIME			UNIT
			FO = 40	FO = 160	FO = 320	
t_{PHL}	Pad	Y	9	12	15	ns
t_{PLH}			9	12	15	

NOTE 8: The ALS software provides user-selectable options for choosing four levels of automatic clock load balancing. There is no limit to the number of loads that may be connected to the clock buffer (CLKBUF) macro.

extended output current operation

The TPC10 Series devices are capable of driving larger sink current loads by derating the low-level output voltage to 0.5 V and high-level output voltage to 2.4 V. The derating factors for commercial and military devices are illustrated in Figure 4 and Figure 5. The commercial devices are derated up to 8 mA and military devices are derated for up to 6 mA.

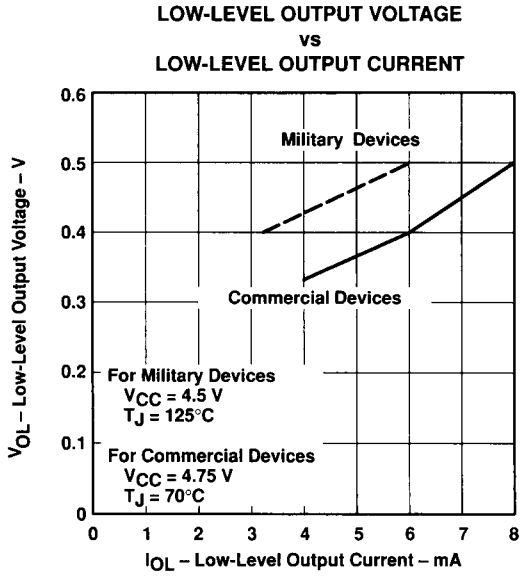


Figure 4

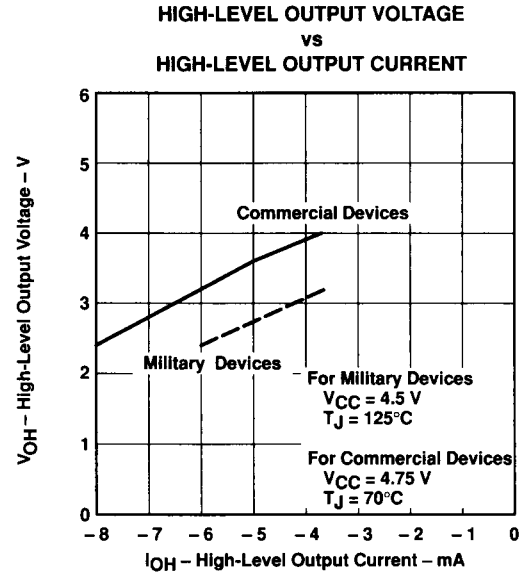


Figure 5

slow input transition (rise and fall) times

Slow signal transition is a condition that commonly occurs even in today's high-performance systems. A typical example is the signal degradation encountered with signals coming off of a highly capacitive bus. These slow signal transitions can cause undesirable results when traveling through the threshold region of a CMOS input. Texas Instruments recommends that input signal transitions be limited to 500 ns or less to ensure device integrity.

worst-case delay time

Unlike mask-programmed gate arrays, performance variations of TPC10 Series arrays caused by voltage and temperature changes are due primarily to the changes in the active elements. Voltage and temperature delay time factors are shown in Figure 6 and Figure 7.

timing derating

Operating temperature, operating voltage, and device processing conditions, along with product revision and speed grade, account for variations in array timing characteristics. These variations are summarized in derating factors for TPC10 array typical timing specifications. The derating factors as shown in Table 4 are based on the recommended operating conditions for TPC10 commercial, industrial, and military applications.

For estimating performance, the delay factors may be used in conjunction with the delay values shown in the typical switching characteristics tables. Temperature and voltage variations are measured according to the curves in the graphs shown in Figure 6 and Figure 7. The ALS timing analyzer can be used to provide actual postlayout timing specifications for each circuit implementation.

Table 4. Timing Derating Factor (x typical) (see Note 9)

TPC1010A, TPC1020A TPC1010B, TPC1020B	C SUFFIX		I SUFFIX		M SUFFIX	
	BEST CASE	WORST CASE	BEST CASE	WORST CASE	BEST CASE	WORST CASE
Standard speed	0.45	1.54	0.40	1.65	0.37	1.79
–1 Speed grade	0.45	1.28	0.40	1.37	0.37	1.49
–2 Speed grade†	0.45	1.13	0.40	1.20	0.37	1.32

† Applies to TPC1010B and TPC1020B only

NOTE 9: Best case reflects maximum operating voltage, minimum operating temperature, and best case processing. Worst case reflects minimum operating voltage, maximum operating temperature, and worst case processing. Best case derating is based on sample data only and is not guaranteed.

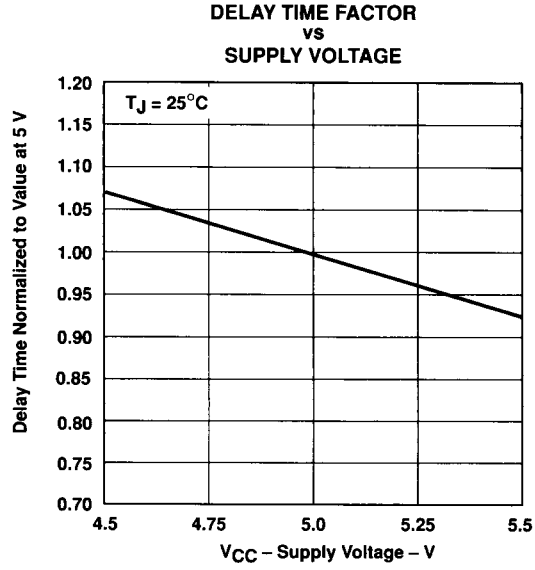


Figure 6

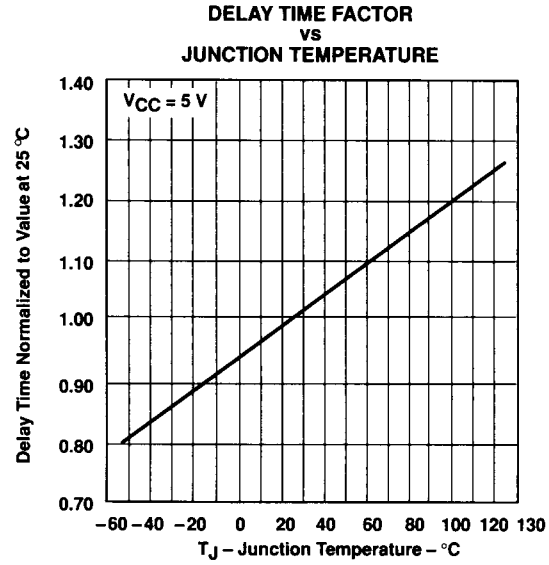
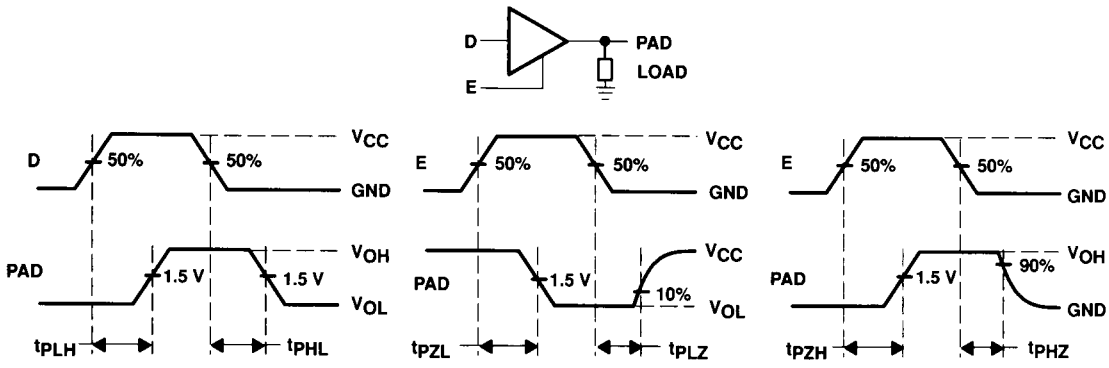
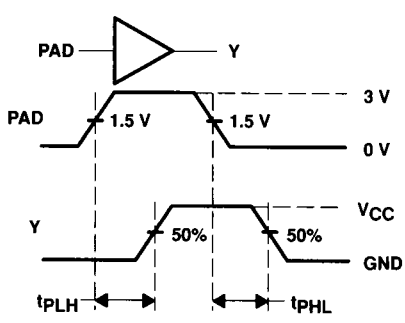


Figure 7

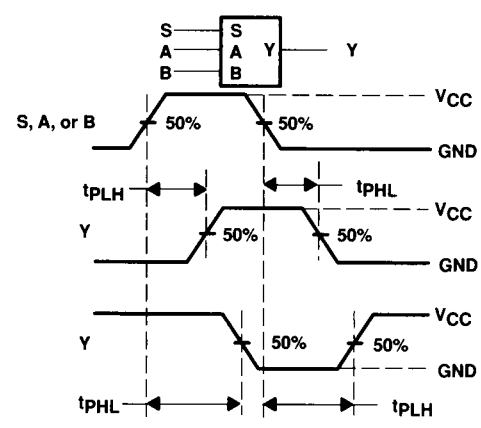
PARAMETER MEASUREMENT INFORMATION



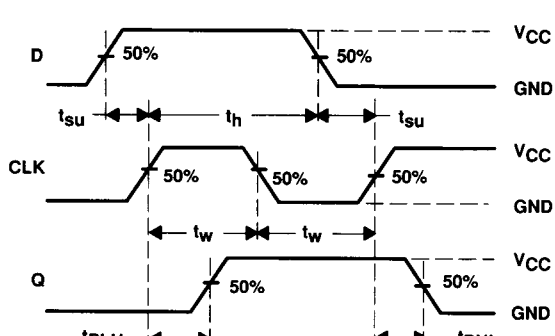
OUTPUT BUFFER DELAYS

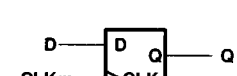


INPUT BUFFER DELAYS



MODULE DELAYS

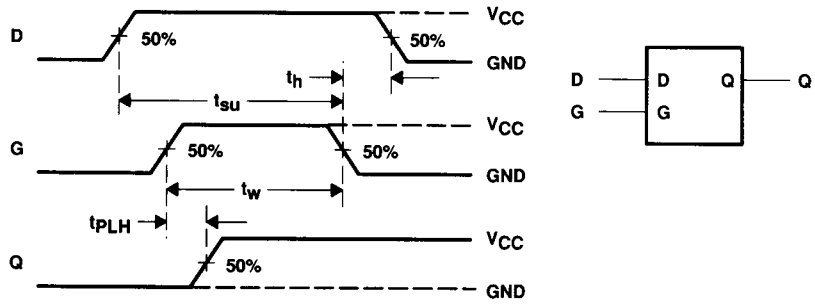




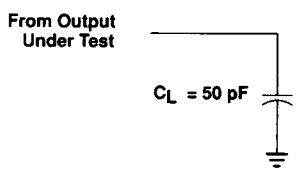
D FLIP-FLOP SHOWING POSITIVE-EDGE TRIGGERED CLOCK

Figure 8. Symbols, Test Loads, and Voltage Waveforms

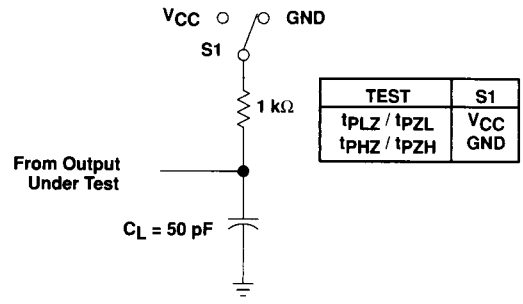
PARAMETER MEASUREMENT INFORMATION



DATA LATCH DELAYS



LOAD CIRCUIT FOR PROPAGATION DELAY TIMES



LOAD CIRCUIT FOR ENABLE AND DISABLE TIMES

Figure 8. Symbols, Test Loads, and Voltage Waveforms (Continued)

dynamic power calculations

The formula for calculating typical dynamic die power consumption in mW is:

$$\text{Total die power} = (0.20N \times f1) + (0.085M \times f2) + (0.80P \times f3)$$

where:

f1 = Average logic module switching rate in MHz
f2 = Average clock pin switching rate in MHz (see Note 10)
f3 = Average I/O switching rate in MHz
M = Number of logic modules connected to the clock pin (see Note 10)
N = Number of logic modules used on the chip (including M)
P = Number of I/Os used with 50-pF load

NOTE 10: The F2 and M factors can be ignored if the CLKBUF macro is not used.

For example, if a TPC1010A design has 200 logic modules used, 40 of which are connected to the high-fan-out clock buffer running at 20 MHz and the rest running at 4 MHz, plus 50 I/Os (25 outputs, 25 inputs) running at an average of 4 MHz, it will dissipate the following amount of power:

$$\begin{aligned}\text{Total die power} &= (0.20N \times f1) + (0.085M \times f2) + (0.80P \times f3)\\ &= 0.20\ (200 \times 4) + 0.085\ (40 \times 20) + 0.80\ (25 \times 4)\\ &= 308\ \text{mW}\end{aligned}$$

ESD rating

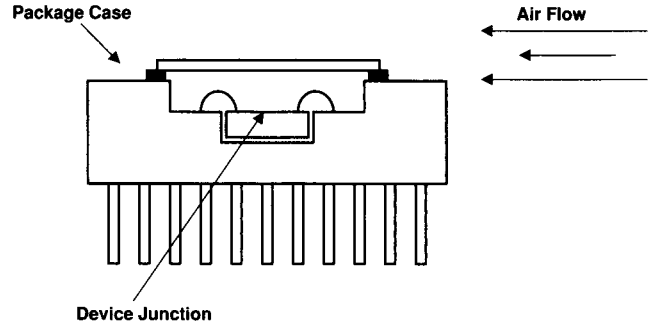
ESD characterization of Texas Instruments FPGAs is performed in accordance with Method 3015 of MIL-STD-883. This calls out the human body model which included discharging a 10-pF capacitor through a 1.5-kΩ resistor. Three positive and three negative pulses are discharged into each pin at each voltage level. After pulsing, the units are tested on a VLSI tester. Testing is performed for initial device qualification and product redesign only. All devices have been designed for ESD protection.

package thermal characteristics

The device junction to case thermal characteristic is $R_{\theta JC}$, and the junction to ambient air characteristic is $R_{\theta JA}$. The thermal characteristics for $R_{\theta JA}$ are shown with two different air-flow rates. Maximum junction temperature is 150°C for short durations. However, a maximum junction temperature of 140°C is recommended for continuing operation. A sample calculation of the maximum power dissipation for a PLCC 84-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp. (°C)}}{R_{\theta JA}\ (°C/W)} = \frac{150°C - 70°C}{40°C/W} = 2\ W$$

PACKAGE TYPE	PIN COUNT	$R_{\theta JC}$	$R_{\theta JA}$ STILL AIR	$R_{\theta JA}$ 300 FT/MIN	UNIT
Ceramic Pin Grid Array (CPGA)	84	3.5	48	NA	°C/W
Ceramic Quad Flat Package (CQFP)	84	3.5	75	NA	°C/W
Plastic Leaded Chip Carrier PLCC	44 68 84	13 13 10	65 50 40	41 32 27	°C/W
Plastic Quad Flat Package (PQFP)	100	10	60	38	°C/W



TPC1010A device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	295	1200	34	R	R
68-pin PLCC			57	R	R
100-pin PQFP			57	R	R

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	295	1200	34	R	R
68-pin PLCC			57	R	R
100-pin PQFP			57	R	R

Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
84-pin CPGA	295	1200	57	R	R
84-pin CQFP			57	R	R

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1020A device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	547	2000	34	R	R
68-pin PLCC			57	R	R
84-pin PLCC			69	R	R
100-pin PQFP			69	R	R

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
44-pin PLCC	547	2000	34	R	R
68-pin PLCC			57	R	R
84-pin PLCC			69	R	R
100-pin PQFP			69	R	R

Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
84-pin CPGA	547	2000	69	R	R
84-pin CQFP			69	R	R

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1010B device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	295	1200	34	R	R	P
68-pin PLCC			57	R	R	P
100-pin PQFP			57	P	P	P

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	295	1200	34	R	R	P
68-pin PLCC			57	R	R	P
100-pin PQFP			57	P	P	P

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1020B device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	547	2000	34	P	P	P
68-pin PLCC			57	P	P	P
84-pin PLCC			69	P	P	P
100-pin PQFP			69	P	P	P

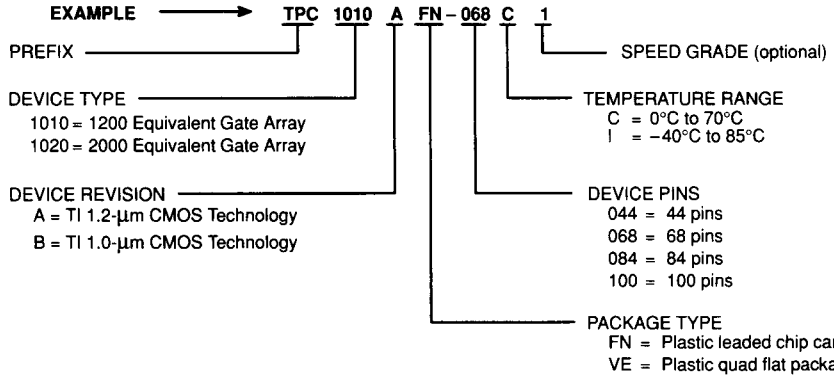
Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE		
				STD	–1	–2
44-pin PLCC	547	2000	34	P	P	P
68-pin PLCC			57	P	P	P
84-pin PLCC			69	P	P	P
100-pin PQFP			69	P	P	P

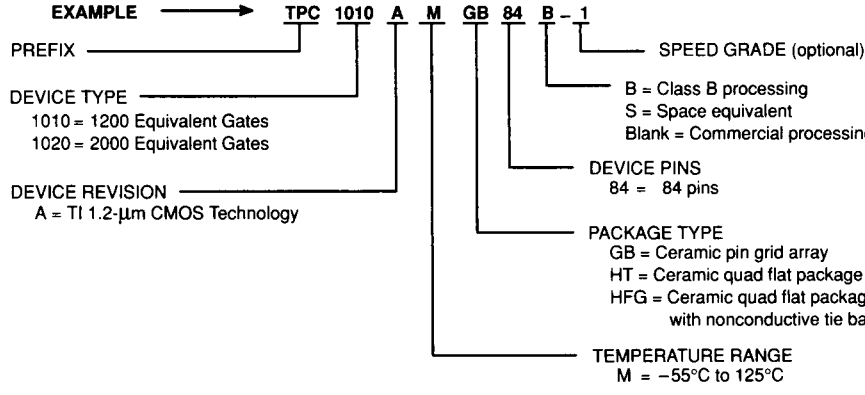
R = released
P = planned, consult your local TI sales representative for current availability.

ordering information

Configurations of the TPC10 Series devices can be ordered using the part numbers in the examples below. Commercial and industrial versions can be ordered as follows:



Military versions can be ordered as follows:



DEFENSE ELECTRONIC SYSTEM CENTER (DESC) NUMBER

DEVICE NAME	AVAILABLE PROCESSING	DESC NUMBER
TPC1010AM	Class B	5962-9096401M
TPC1020AM	Class B Space Equivalent	5962-9096501M

macro library

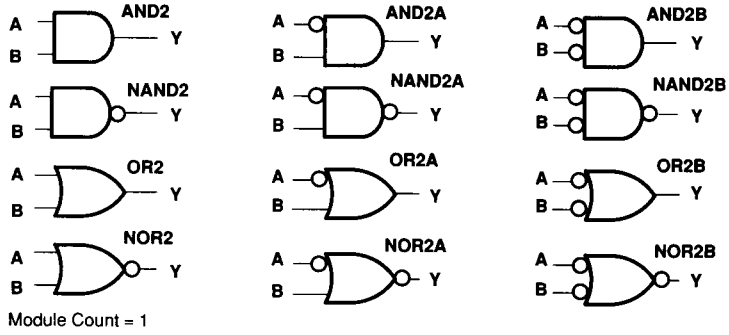
The TPC10 Series is supported by a macro library of more than 250 hardwired and soft macro functions. The macros range from primitive logic gates to MSI-level complex functions such as counters, decoders, and comparators. The hardwired macro characteristics are provided in the electrical and switching characteristics. The software macros have characteristics similar to the components of the macro but need the place and route data back annotated into the design to establish actual performance.

The FPGA logic module implements logic functions with inverted inputs as efficiently as noninverted inputs, without an increase in propagation delay. By taking advantage of the various combinations of input polarity, the use of separate inverters can be virtually eliminated.

TPC10 SERIES SOFTWARE MACROS

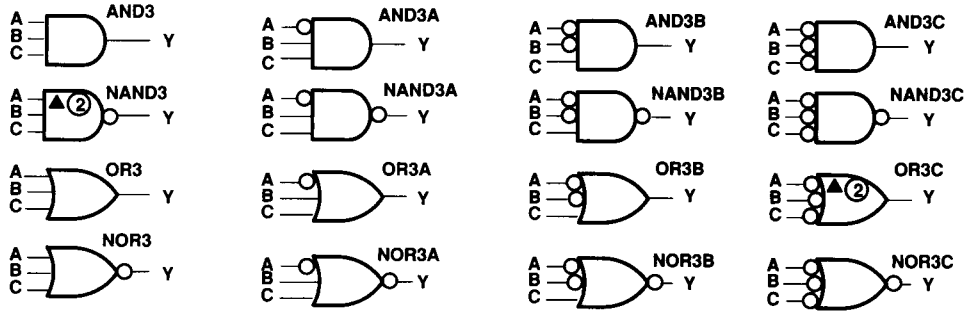
MACRO NAME	DESCRIPTION	MODULE COUNT	LOGIC LEVELS
CNT4A	4-Bit Binary Counter With Load and Clear	18	4
CNT4B	4-Bit Presettable Binary Counter With Load and Clear	15	4
DEC2X4	2-Line to 4-Line Decoder	4	1
DEC2X4A	2-Line to 4-Line Inverting Decoder	4	1
DECE2X4	2-Line to 4-Line Decoder With Enable	4	1
DECE2X4A	2-Line to 4-Line Inverting Decoder With Enable	5	1
DEC3X8	3-Line to 8-Line Decoder	8	1
DEC3X8A	3-Line to 8-Line Inverting Decoder	9	1
DECE3X8	3-Line to 8-Line Decoder With Enable	11	2
DECE3X8A	3-Line to 8-Line Inverting Decoder With Enable	11	2
DEC4X16A	4-Line to 16-Line Inverting Decoder	20	2
DLC8A	Octal D-Type Latch With Clear	8	1
DLE8	Octal D-Type Latch With Enable	8	1
DLM8	Octal D-Type Latch With Multiplexed Inputs	8	1
FA1	1-Bit Full Adder	3	3
FADD8	8-Bit Fast Adder	37	4
FADD12	12-Bit Fast Adder	58	5
FADD16	16-Bit Fast Adder	79	5
FADD24	24-Bit Fast Adder	120	6
FADD32	32-Bit Fast Adder	160	7
ICMP4	4-Bit Identity Comparator	5	2
ICMP8	8-Bit Identity Comparator	9	3
MCMPC2	2-Bit Magnitude Comparator With Enable	9	3
MCMPC4	4-Bit Magnitude Comparator With Enable	18	4
MCMPC8	8-Bit Magnitude Comparator With Enable	36	6
MCMP16	16-Bit Magnitude Comparator	93	5
MX8	8-Line to 1-Line Multiplexer	3	2
MX8A	8-Line to 1-Line Inverting Multiplexer	3	2
MX16	16-Line to 1-Line Multiplexer	5	2
REGE8A	Octal Register With Preset and Clear	20	1
REGE8B	Octal Register With Preset and Clear	20	1
SMULT8	8 x 8 Twos Complement Multiplier	241	–
SREG4A	4-Bit Shift Register With Clear	8	1
SREG8A	8-Bit Shift Register With Clear	18	1
TA138	3-Line to 8-Line Decoder/Demultiplexer	12	2
TA139	2-Line to 4-Line Decoder/Demultiplexer	4	1
TA151	8-Line to 1-Line Multiplexer	5	3
TA153†	4-Line to 1-Line Multiplexer	2	2
TA157†	2-Line to 1-Line Multiplexer	1	1
TA161	Synchronous 4-Bit Counter With Direct Clear	22	3
TA164	8-Bit Parallel-Out Shift Register	18	1
TA169	4-Bit Up/Down Counter	25	6
TA194	4-Bit Bidirectional Universal Shift Register	14	1
TA195	4-Bit Parallel-Access Shift Register	11	1
TA269	8-Bit Up/Down Counter	50	8
TA273	Octal D-Type Flip-Flop With Clear	18	1
TA280	9-Bit Odd/Even Parity Generator/Checker	9	4
TA377	Octal D-Type Flip-Flop With Clock Enable	16	1
UDCNT4A	4-Bit Up/Down Counter With Sync Load and Carry	24	6

† These MSI functions are hardwired.



Module Count = 1

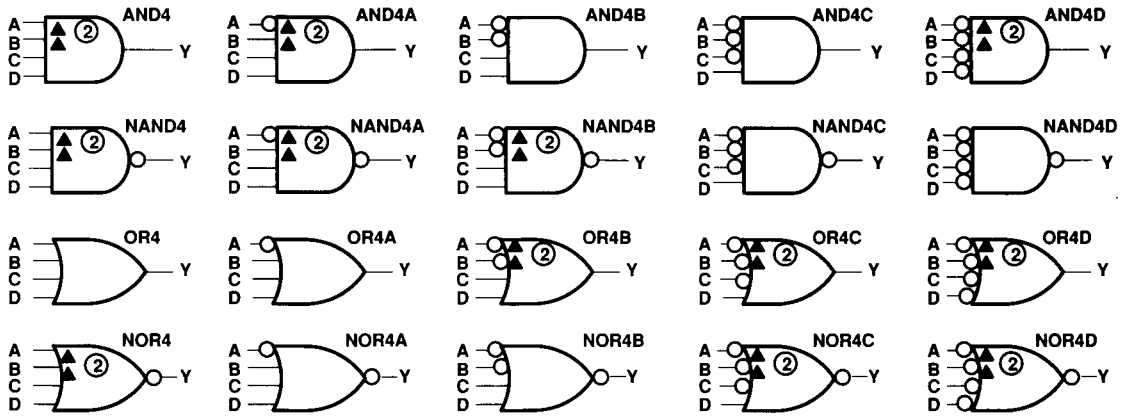
Figure 9. 2-Input Gates



Module Count = 1 (unless otherwise noted)

(2) Indicates Module Count = 2 ▲ Indicates extra delay input

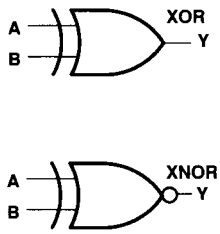
Figure 10. 3-Input Gates



Module Count = 1 (unless otherwise noted)

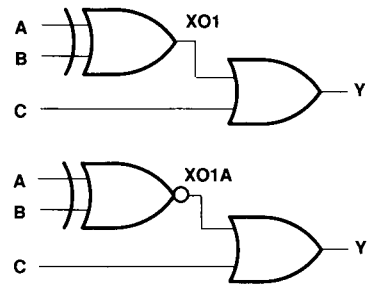
② Indicates Module Count = 2 ▲ Indicates extra delay input

Figure 11. 4-Input Gates



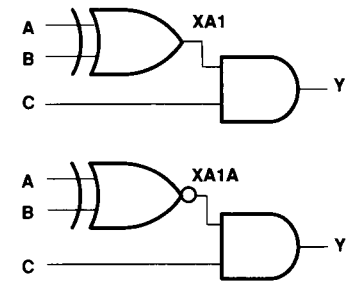
Module Count = 1

Figure 12. XOR/XNOR Gates



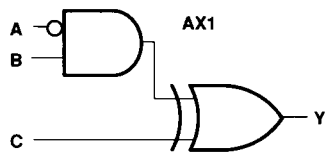
Module Count = 1

Figure 13. XOR-OR/XNOR-OR Gates

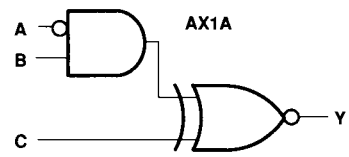


Module Count = 1

Figure 14. XOR-AND/ XNOR-AND Gates



Module Count = 1



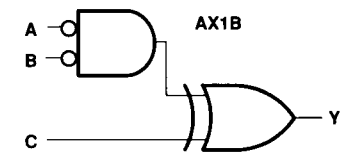
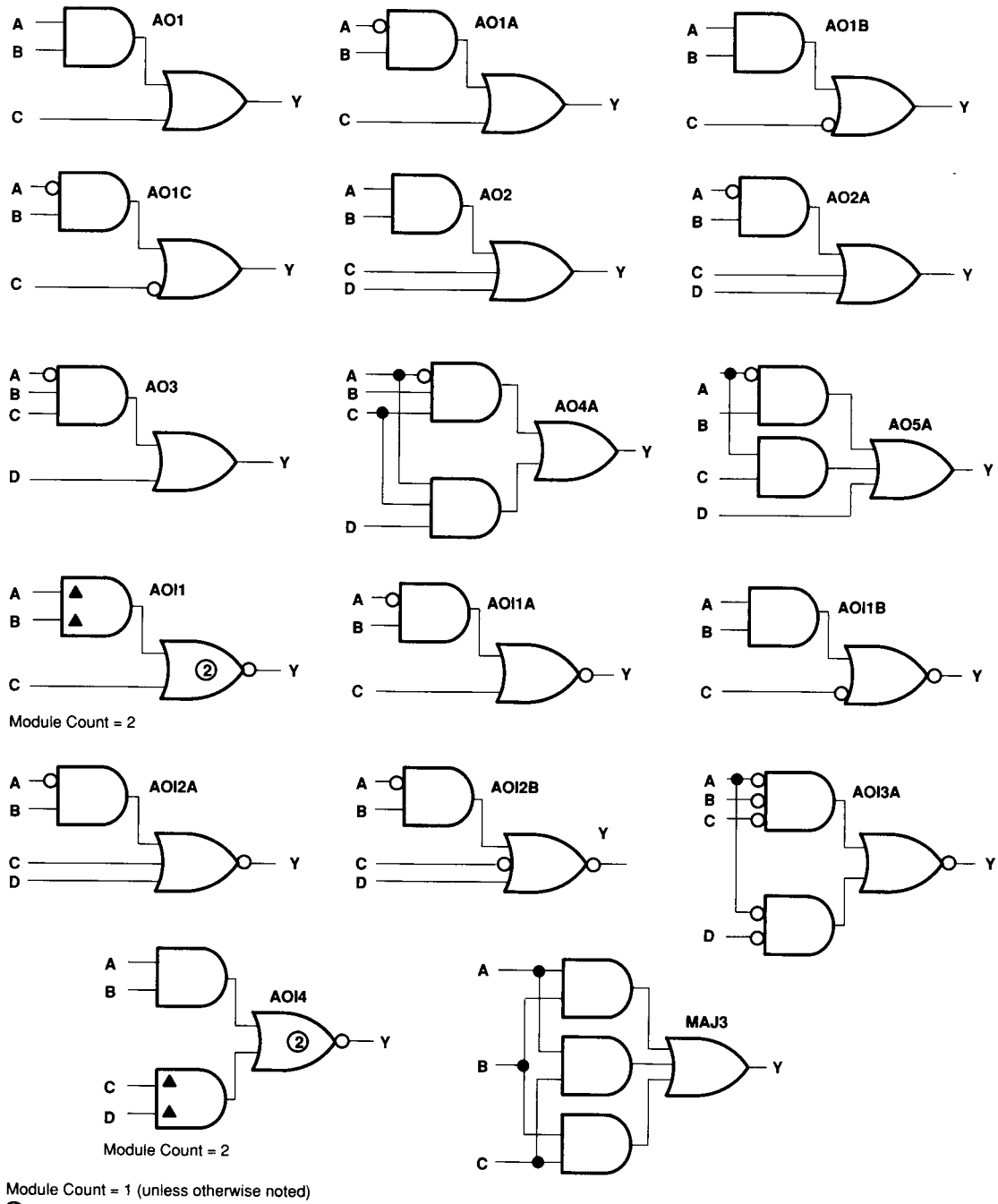


Figure 15. AND-XOR/AND-XNOR Gates

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

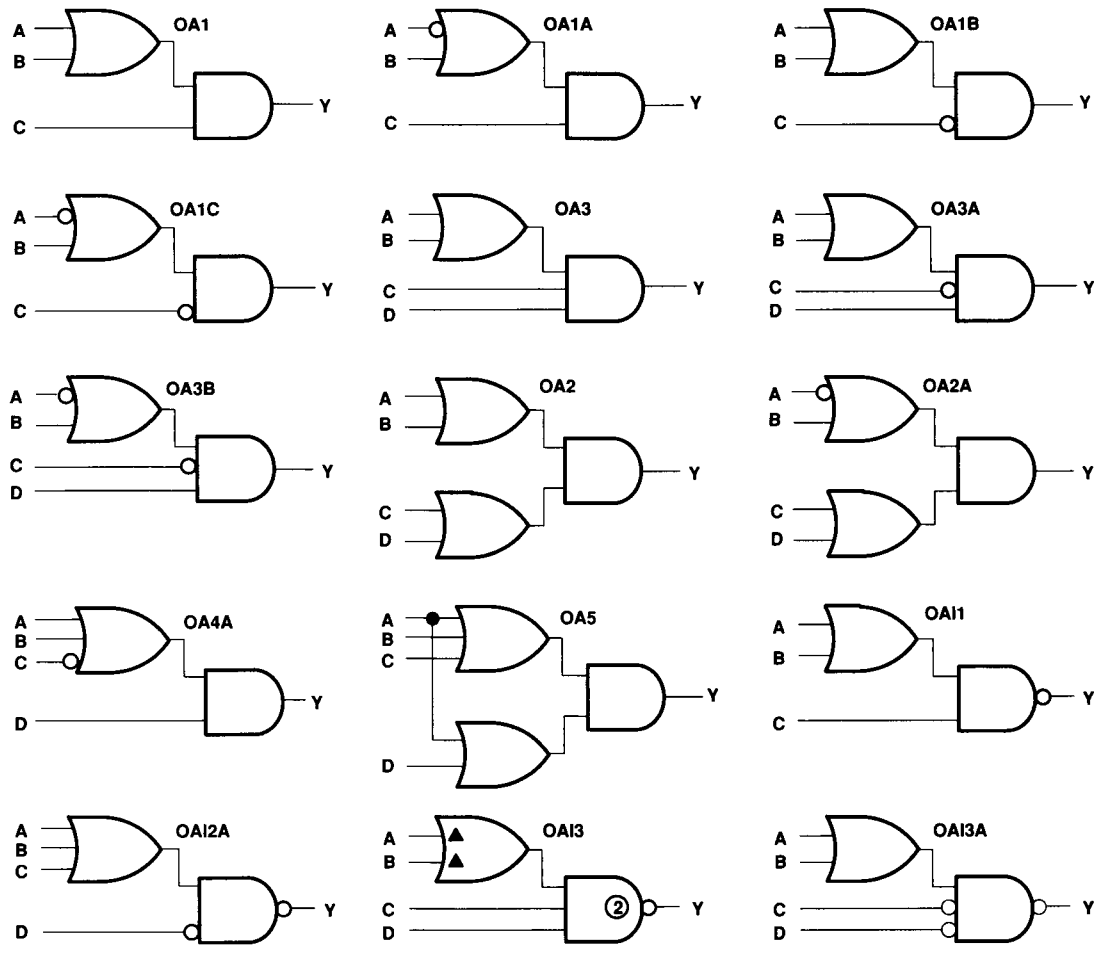


Module Count = 2

Module Count = 2

Module Count = 1 (unless otherwise noted)
② Indicates Module Count = 2
▲ Indicates extra delay input

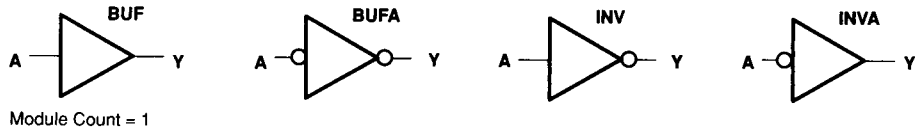
Figure 16. AND-OR/AND-NOR Gates



Module Count = 1 (unless otherwise noted)
▲ Indicates extra delay input
② Module Count = 2

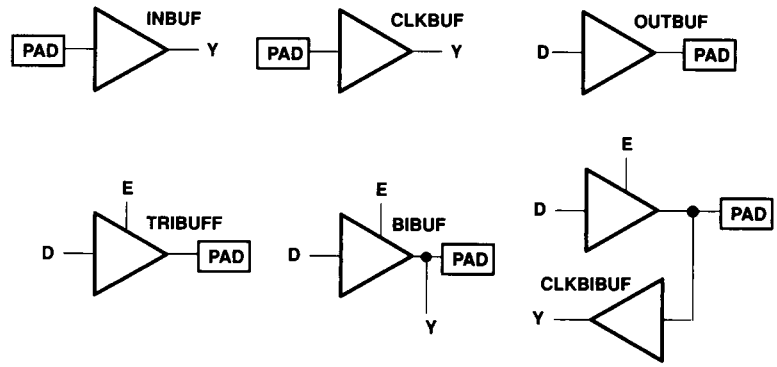
Figure 17. OR-AND/OR-NAND Gates

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



Module Count = 1

Figure 18. Buffers



I/O Module Count = 1

Figure 19. I/O Buffers

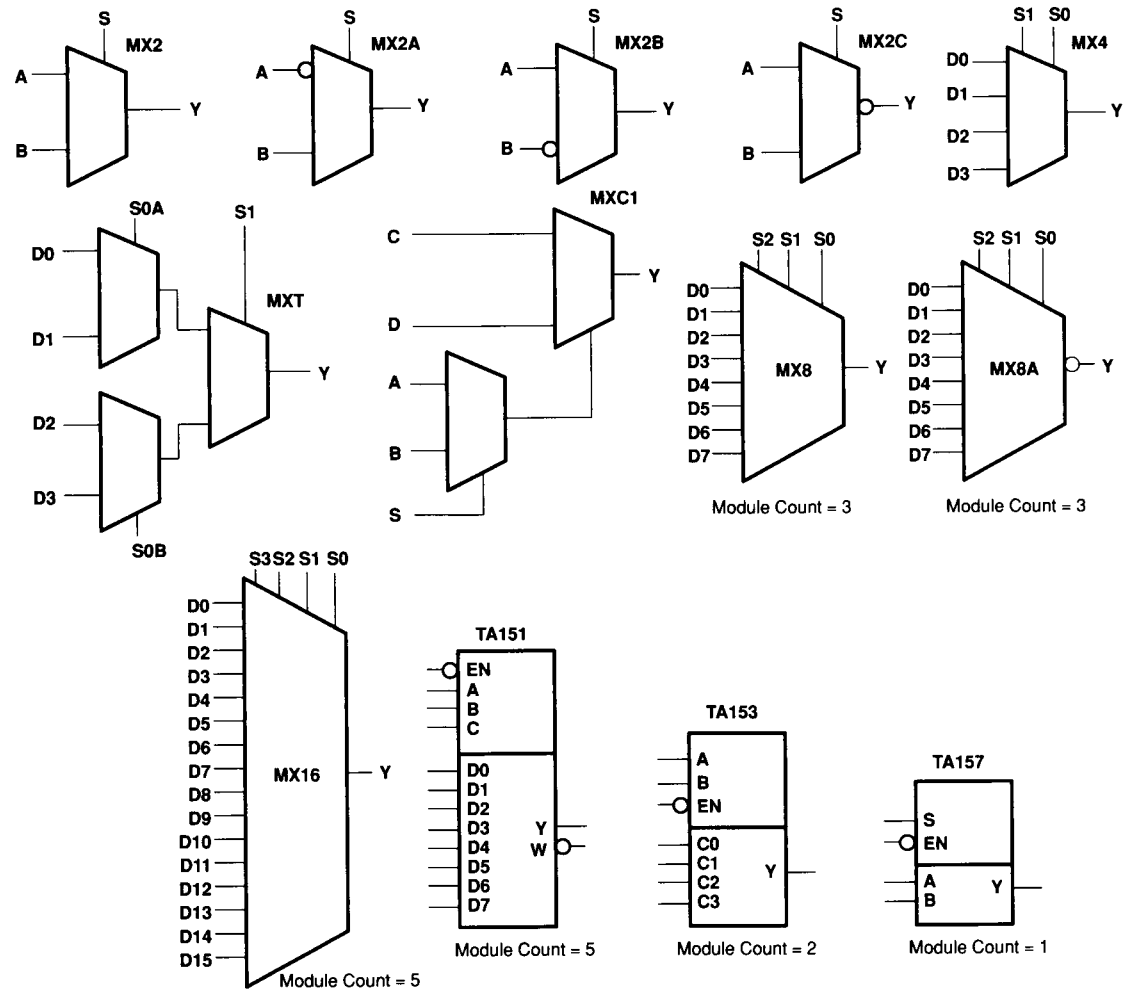
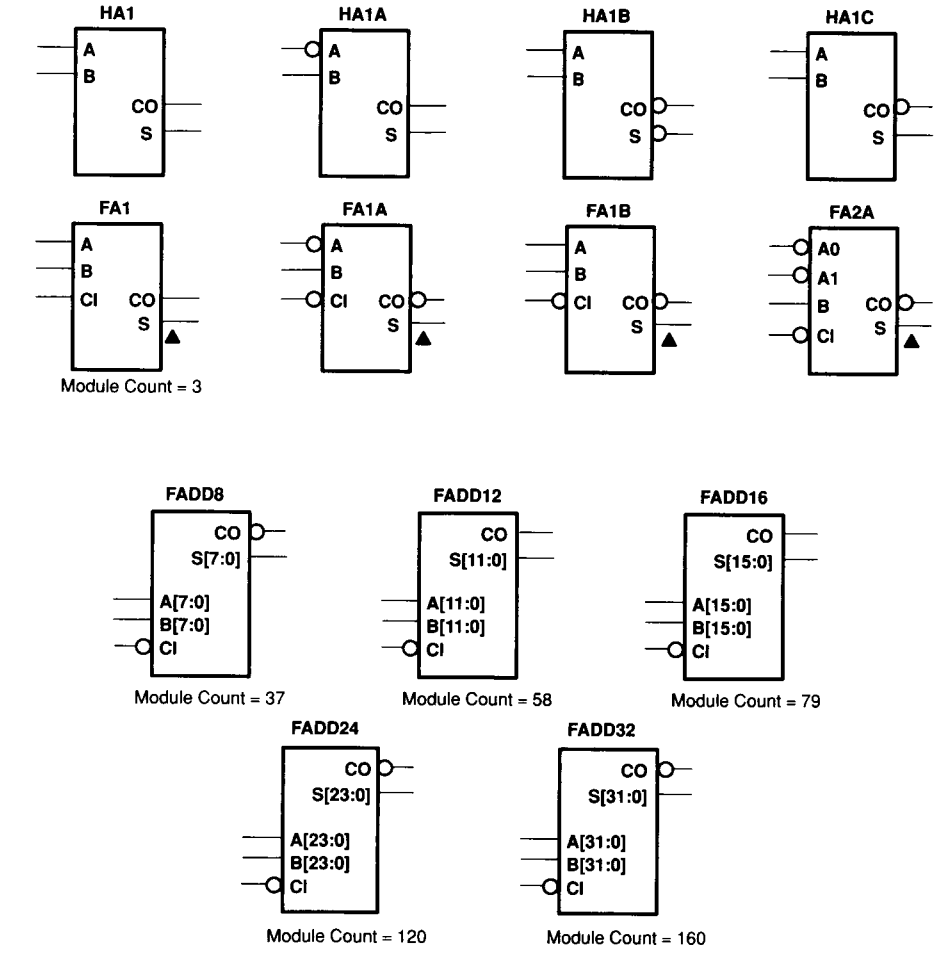


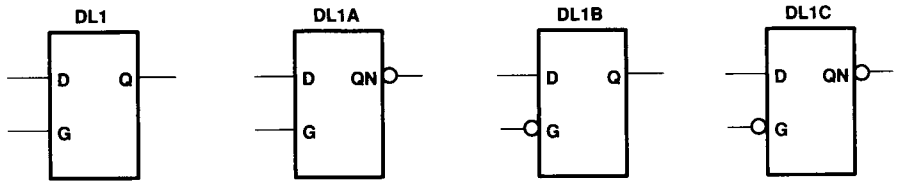
Figure 20. Multiplexers



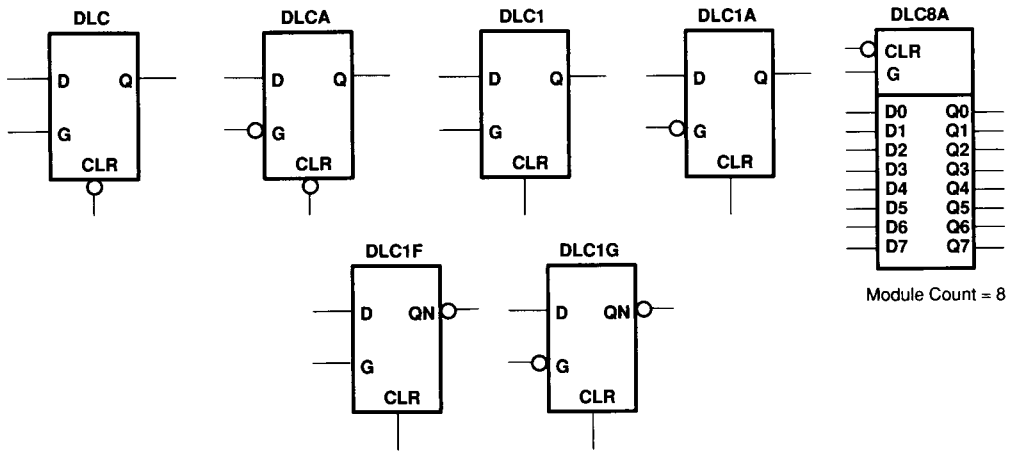
Module Count = 2 (unless otherwise noted)
▲ Indicates two logic module delay path

Figure 21. Adders

D-TYPE LATCHES

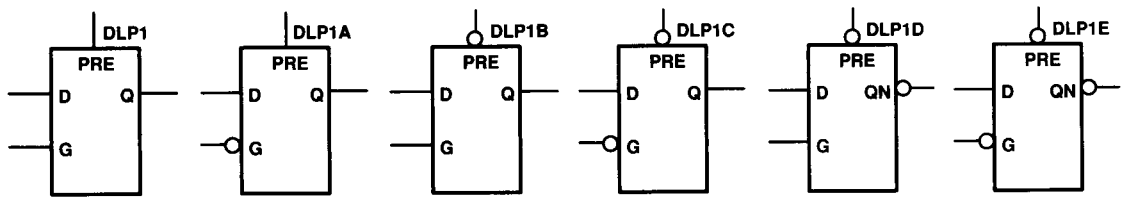


D-TYPE LATCHES WITH CLEAR

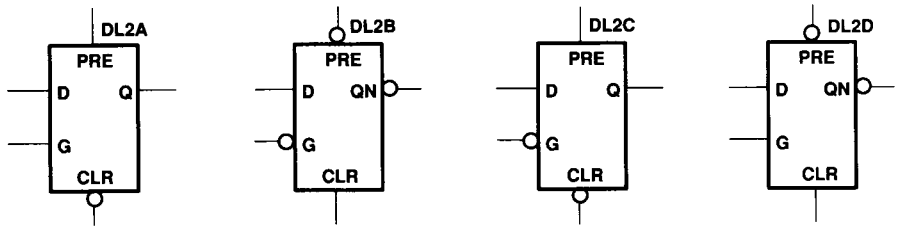


Module Count = 8

D-TYPE LATCHES WITH PRESET



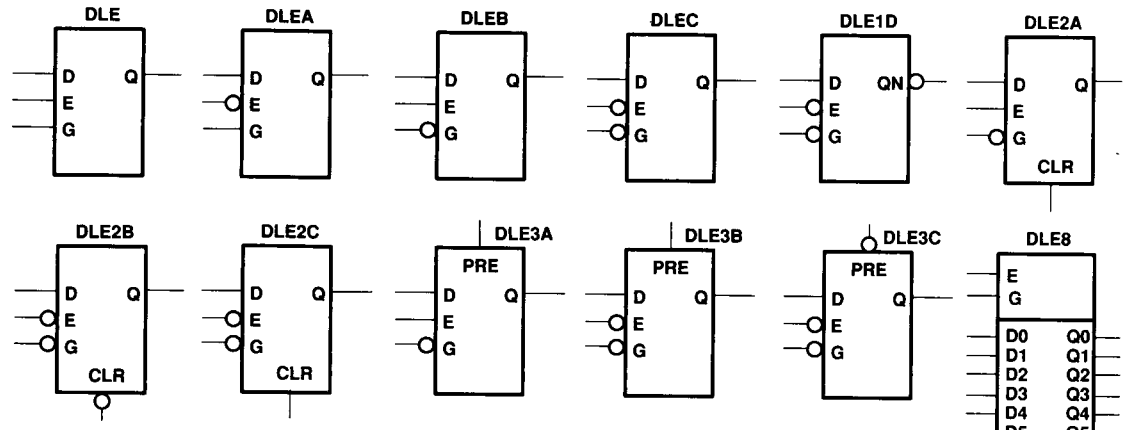
D-TYPE LATCHES WITH CLEAR AND PRESET



Module Count = 1 (unless otherwise noted)

Figure 22. D-Type Latches

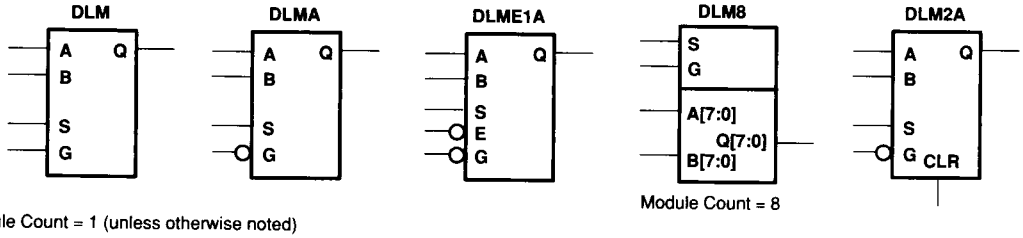
D-TYPE LATCHES WITH ENABLE



Module Count = 1 (unless otherwise noted)

Module Count = 8

D-TYPE LATCHES WITH MULTIPLEXED INPUTS

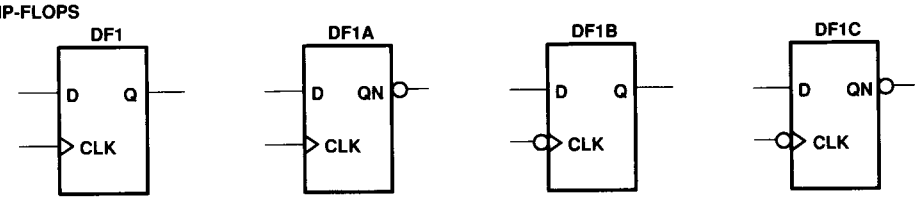


Module Count = 1 (unless otherwise noted)

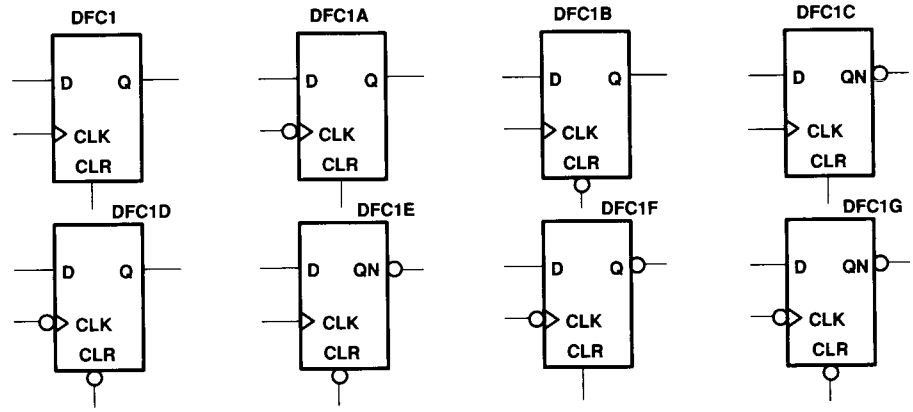
Module Count = 8

Figure 22. D-Types Latches (Continued)

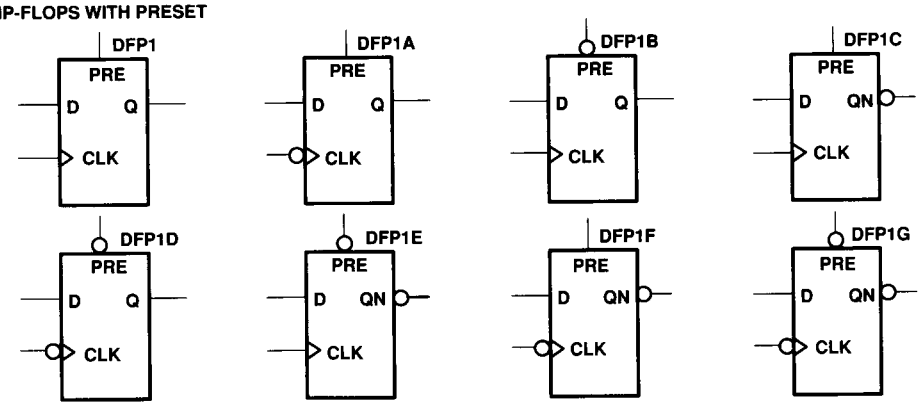
D-TYPE FLIP-FLOPS



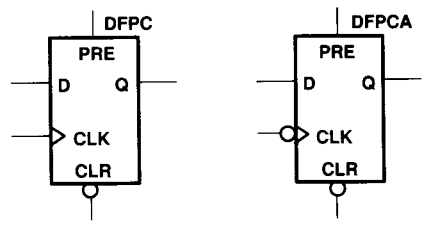
D-TYPE FLIP-FLOPS WITH CLEAR



D-TYPE FLIP-FLOPS WITH PRESET

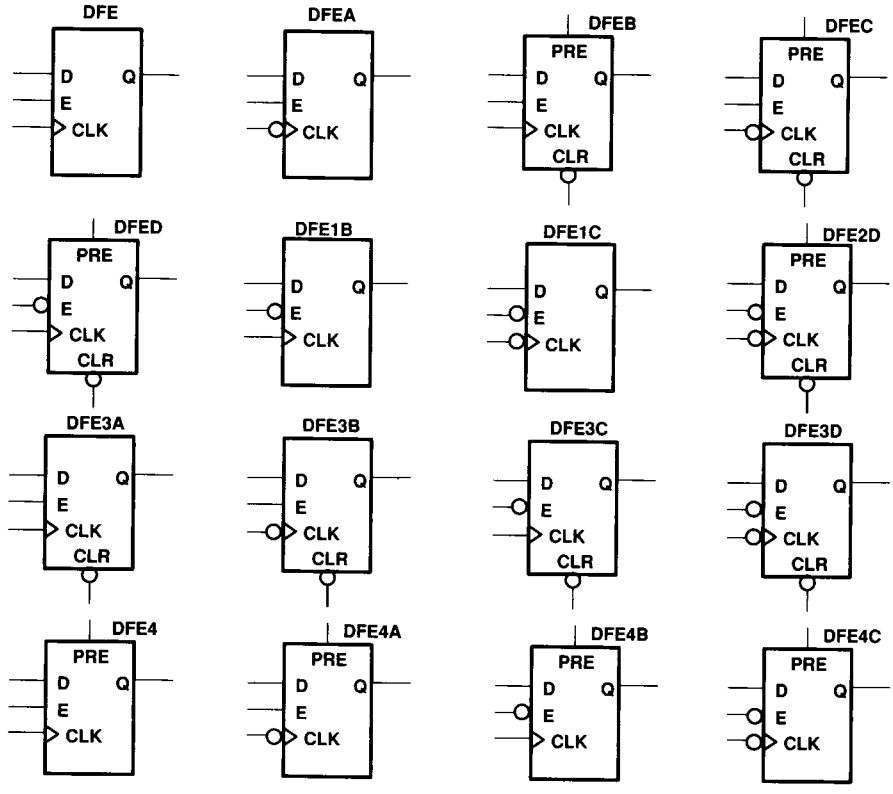


D-TYPE FLIP-FLOPS WITH PRESET AND CLEAR



Module Count = 2

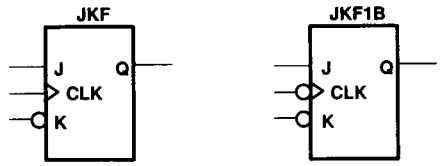
Figure 23. D-Type Flip-Flops



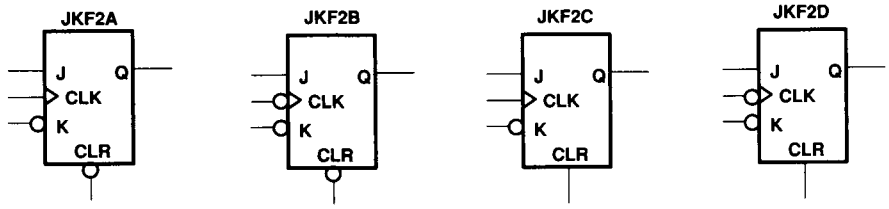
Module Count = 2

Figure 24. D-Type Flip-Flops With Enable

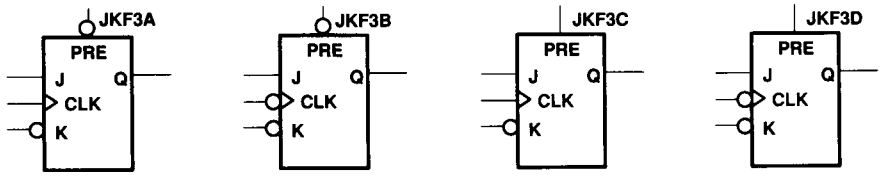
J-$\overline{K}$ FLIP-FLOPS



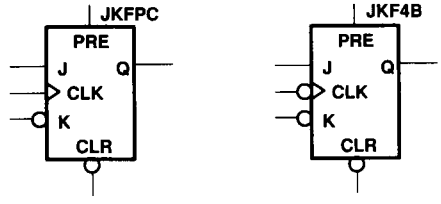
J-$\overline{K}$ FLIP-FLOPS WITH CLEAR



J-$\overline{K}$ FLIP-FLOPS WITH PRESET



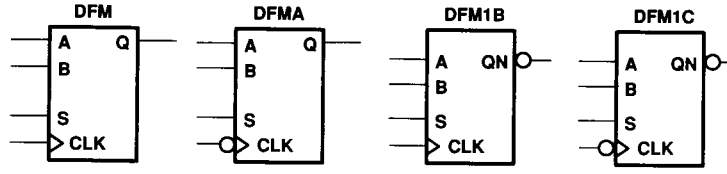
J-$\overline{K}$ FLIP-FLOPS WITH PRESET AND CLEAR



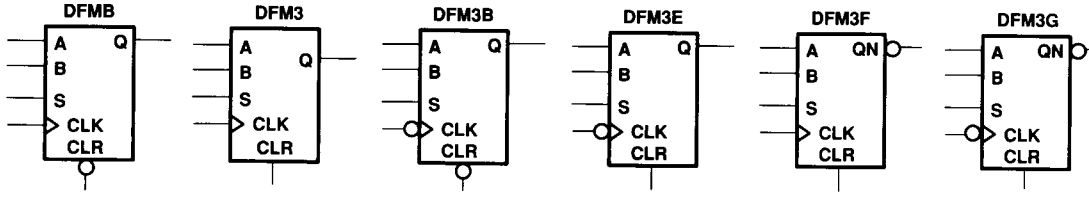
Module Count = 2

Figure 25. J-$\overline{K}$ Flip-Flops

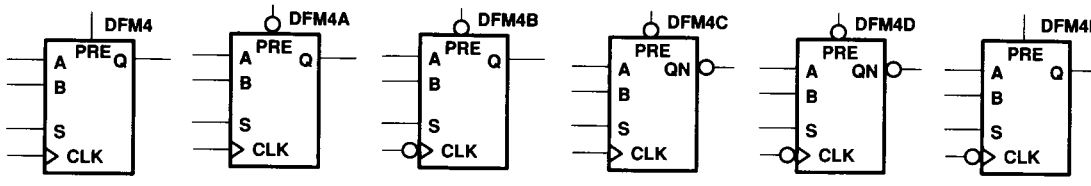
MULTIPLEXED-INPUT FLIP-FLOPS



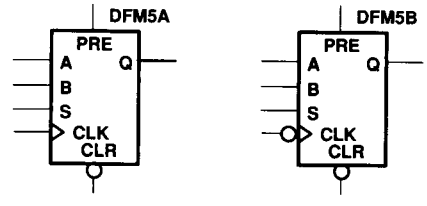
MULTIPLEXED-INPUT FLIP-FLOPS WITH CLEAR



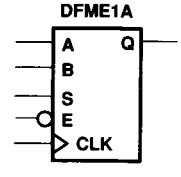
MULTIPLEXED-INPUT FLIP-FLOPS WITH PRESET



MULTIPLEXED-INPUT FLIP-FLOPS WITH PRESET AND CLEAR



MULTIPLEXED-INPUT FLIP-FLOPS WITH ENABLE



Module Count = 2

Figure 26. Multiplexed-Input Flip-Flops

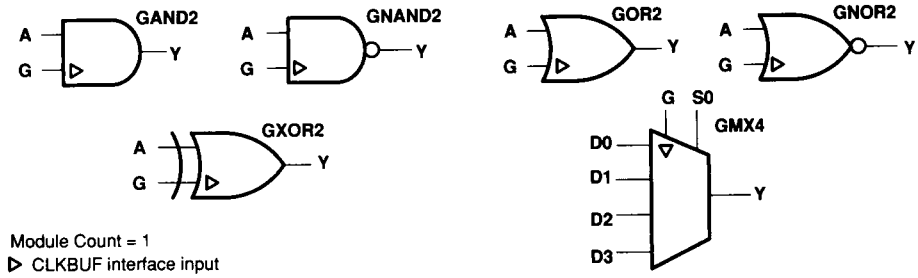


Figure 27. Clock Buffer (CLKBUF) Interface

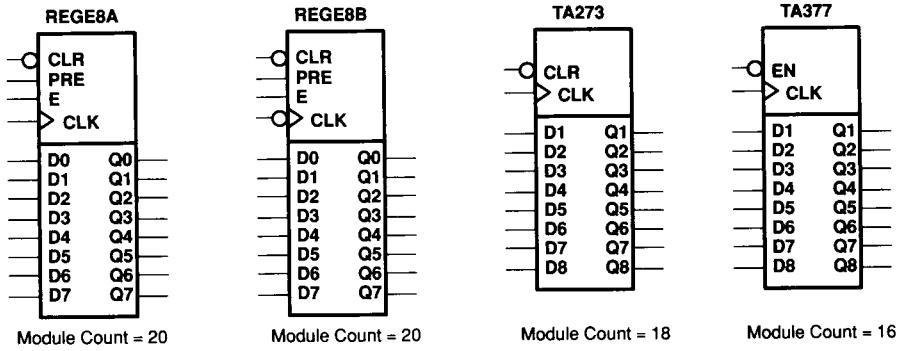


Figure 28. Octal D-Type Flip-Flops and Registers

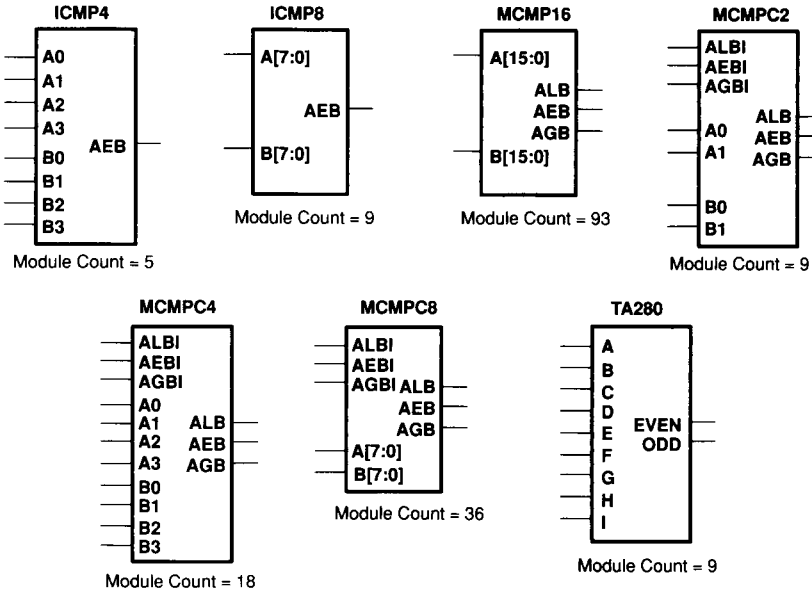


Figure 29. Comparators/Parity Checker

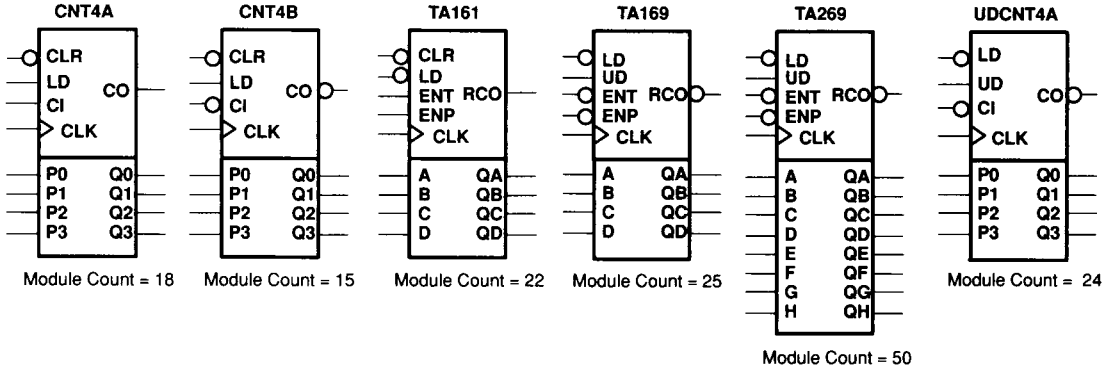


Figure 30. Counters

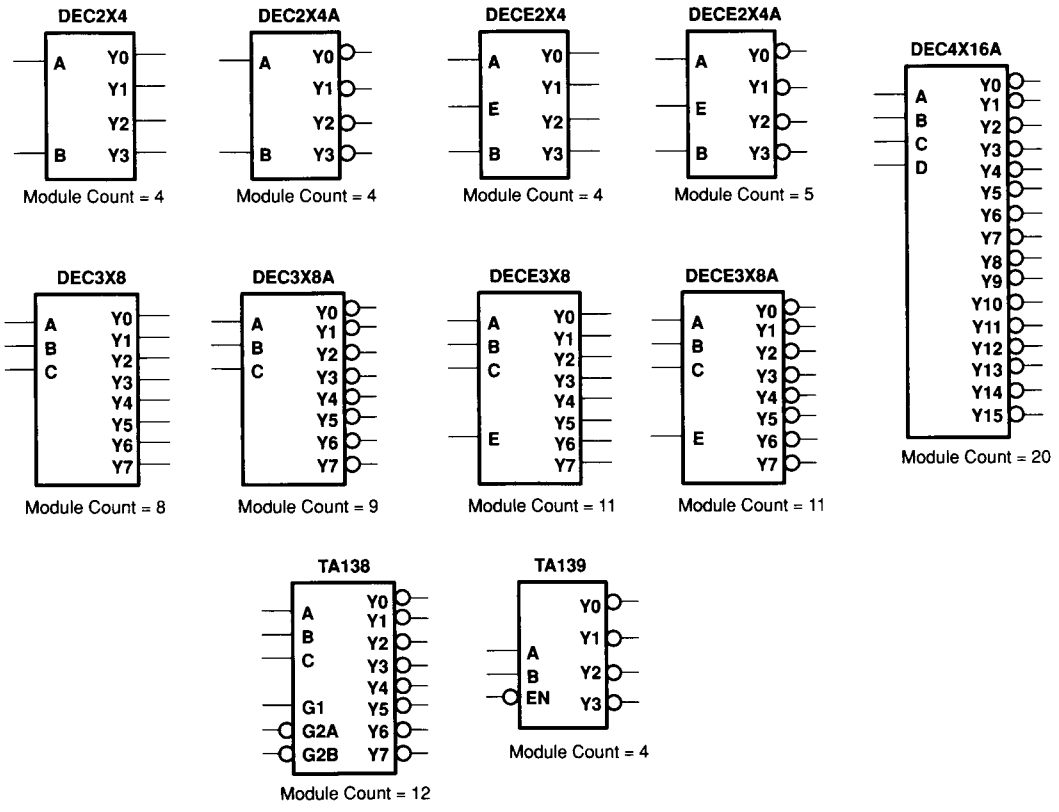


Figure 31. Decoders

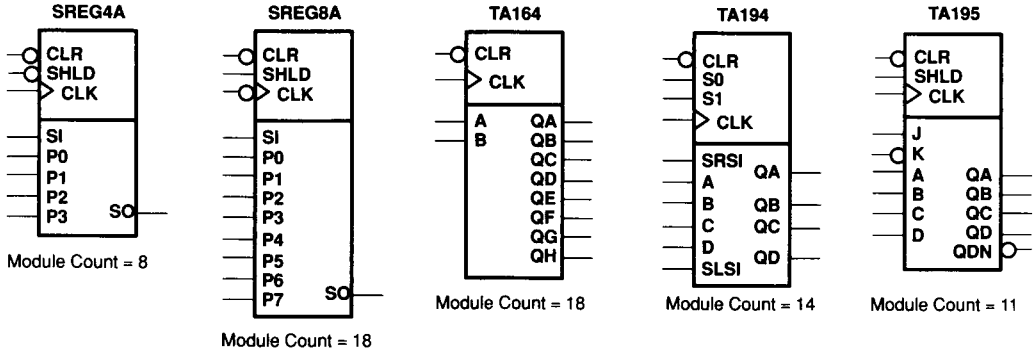


Figure 32. Shift Registers

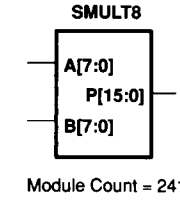


Figure 33. 8-Bit Multiplier

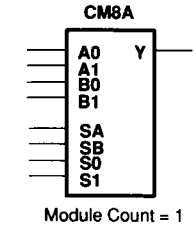
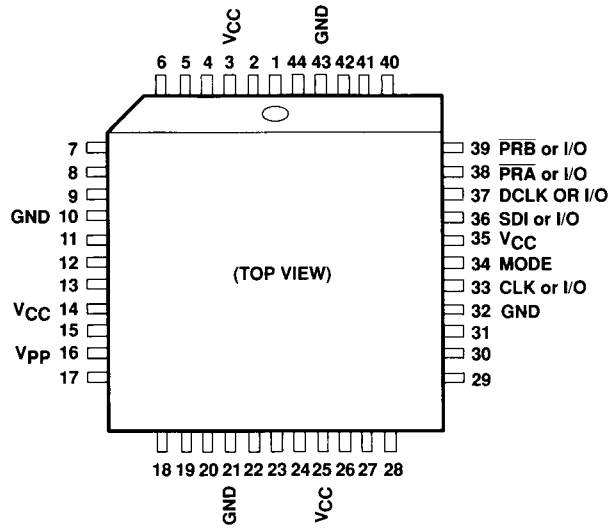


Figure 34. Logic Module

package pin assignments

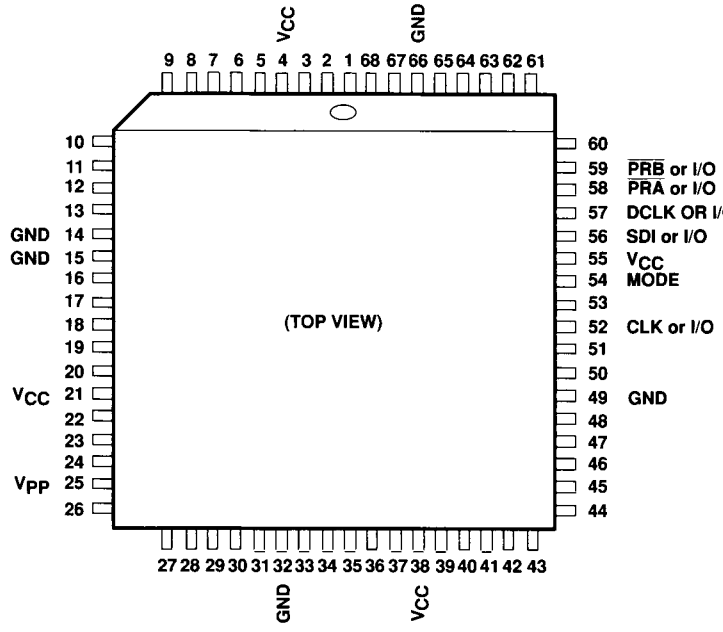


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 35. 44-Pin PLCC Pin Assignment

package pin assignments (continued)

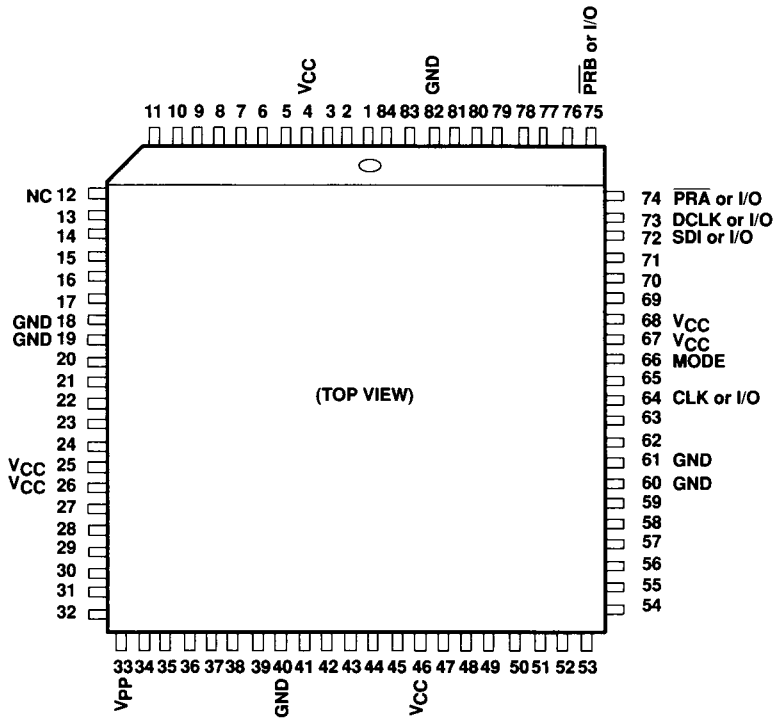


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 36. 68-Pin PLCC Pin Assignment

package pin assignments (continued)

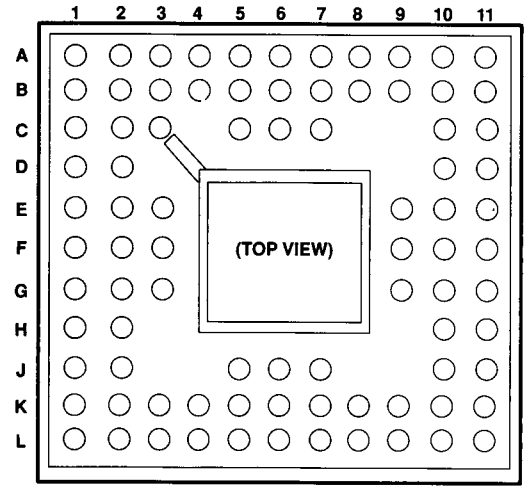


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 37. 84-Pin PLCC Pin Assignment

package pin assignments (continued)



I/O Pin Assignments for the 84-Pin Ceramic Pin Grid Array Package

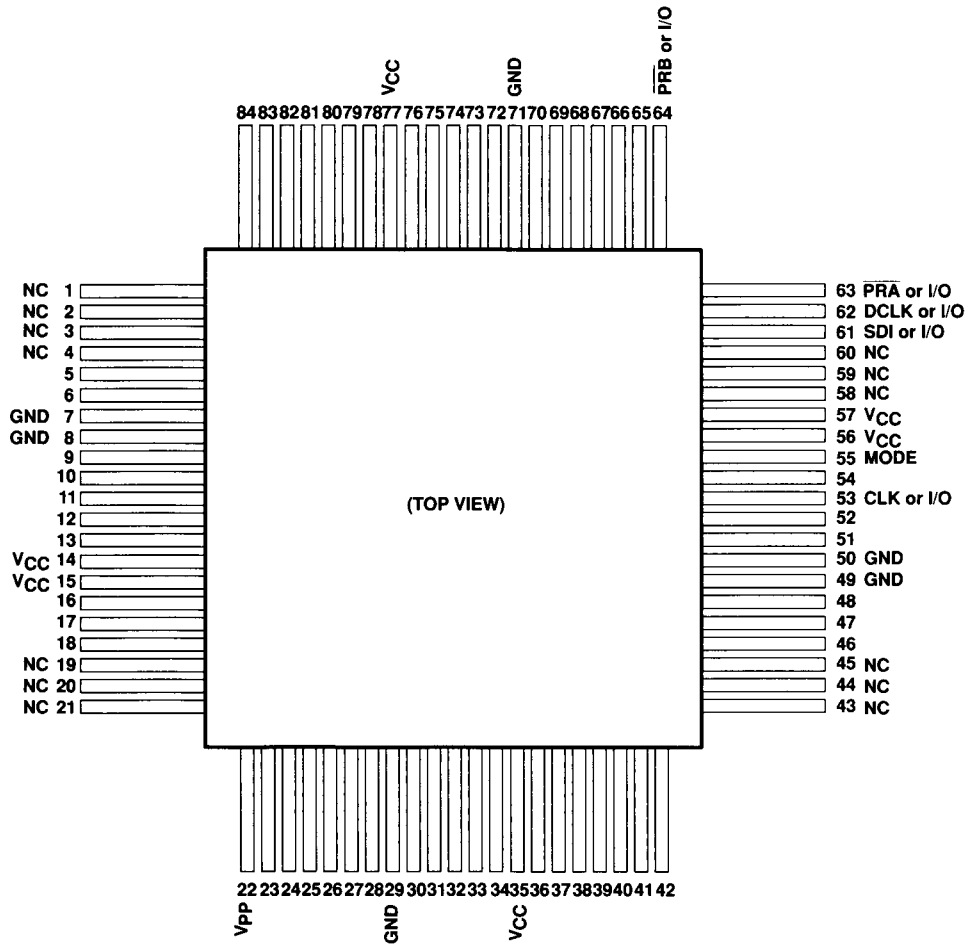
SIGNAL	TPC1010A	TPC1020A
$\overline{PRA}$	A11	A11
$\overline{PRB}$	B10	B10
MODE	E11	E11
SDI	B11	B11
DCLK	C10	C10
V_{PP}	K2	K2
CLK or I/O	F9	F9
GND	B7, E2, E3, K5, F10, G10	B7, E2, E3, K5, F10, G10
V_{CC}	B5, F1, G2, K7, E9, E10	B5, F1, G2, K7, E9, E10
NC (No internal connection)	B1, B2, C1, C2, K1, J2, L1, J10, K10, K11, C11, D10, D11	B2

NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. Orientation pin C3 is connected internally to pin C2.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 38. 84-Pin CPGA Pin Assignment

package pin assignments (continued)

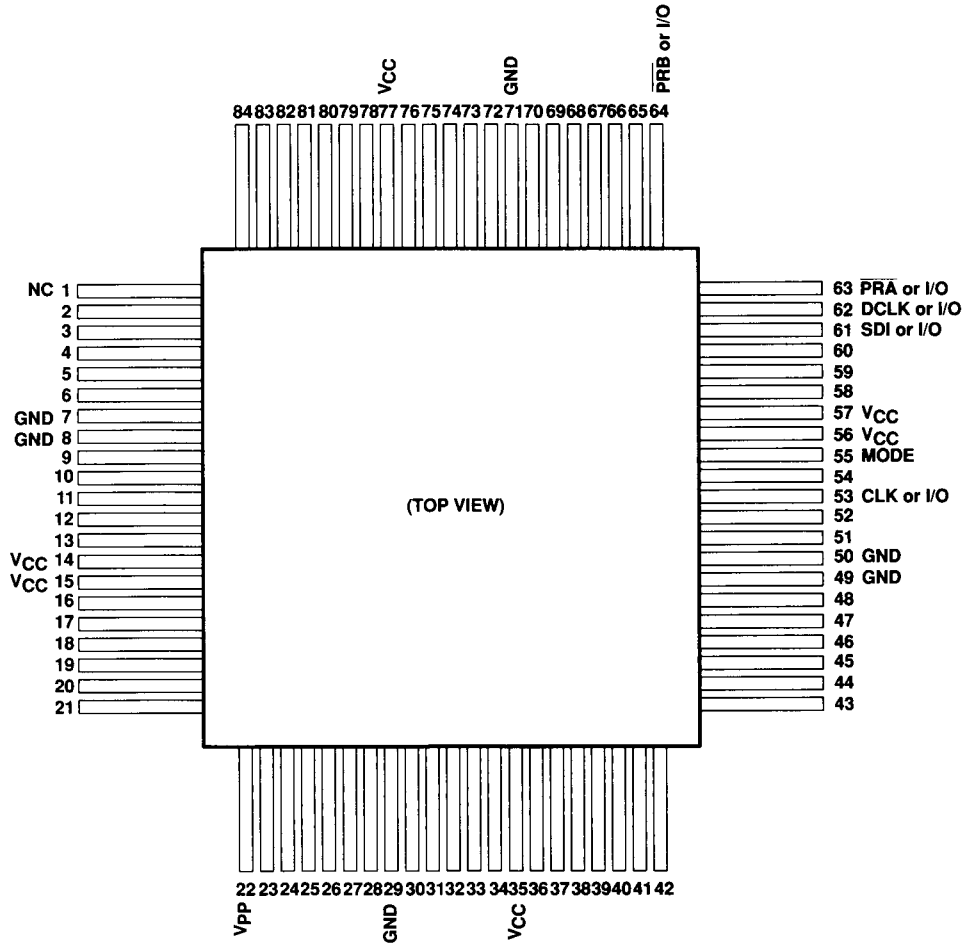


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 39. TPC1010A 84-Pin CQFP Pin Assignment

package pin assignments (continued)

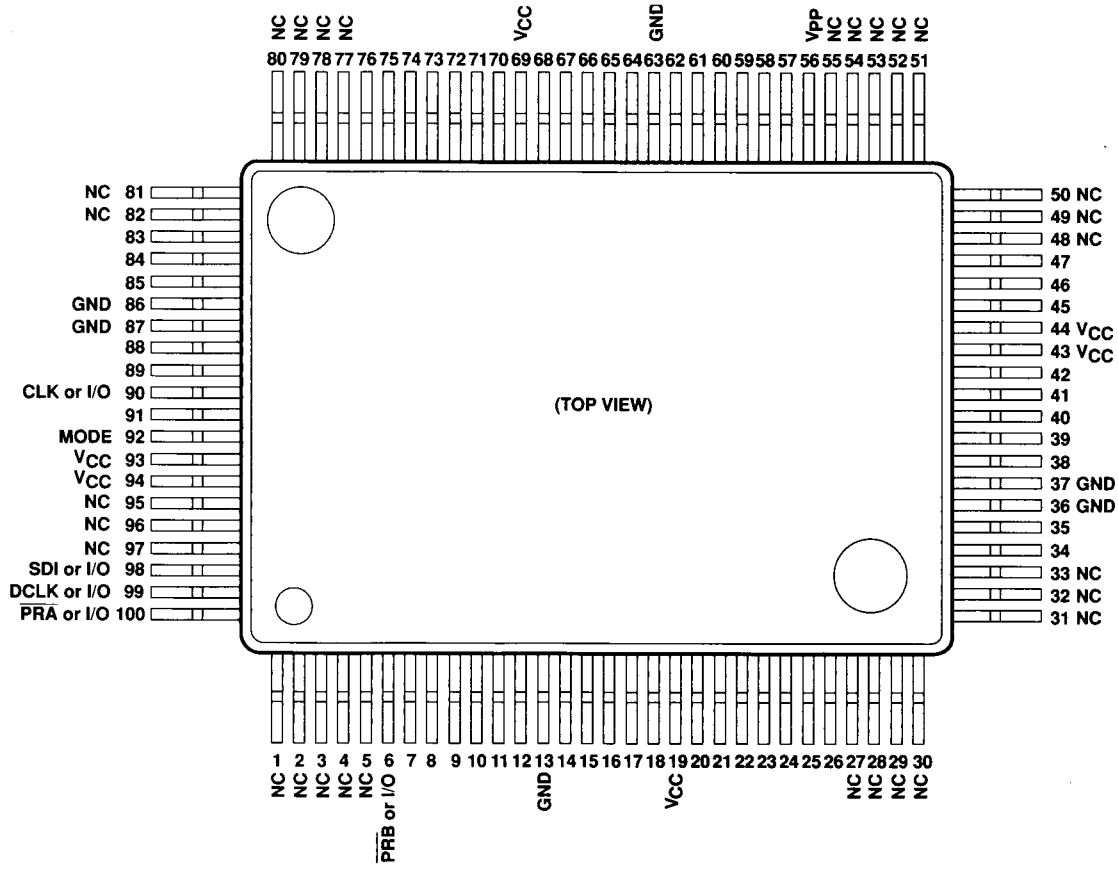


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 40. TPC1020A 84-Pin CQFP Pin Assignment

package pin assignments (continued)

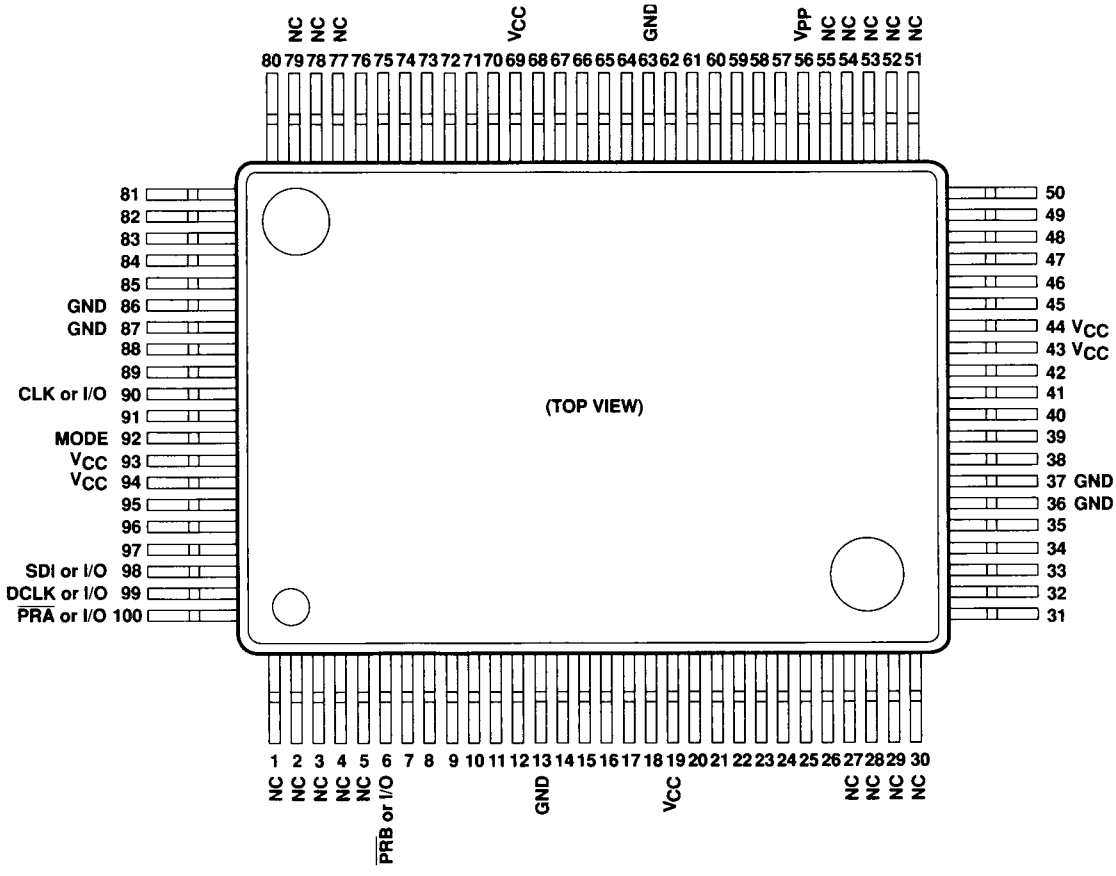


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 41. TPC1010A 100-Pin PQFP Pin Assignment

package pin assignments (continued)



NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. $\overline{PRA}$ and $\overline{PRB}$, the diagnostic probe outputs, should remain open if not used as I/Os.
D. MODE must be terminated to circuit ground except during programming.†
E. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
F. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
G. All unidentified pins on the pin assignment drawings are standard I/Os.
H. NC = No internal connection

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 42. TPC1020A 100-Pin PQFP Pin Assignment

actionprobe pin assignments

There are four types of Actionprobes available: 44-, 68-, and 84-pin PLCC, and 84-pin PGA. At the time your order is placed, please specify which Actionprobe you need.

The Actionprobes are detailed in Figure 43 through Figure 46.

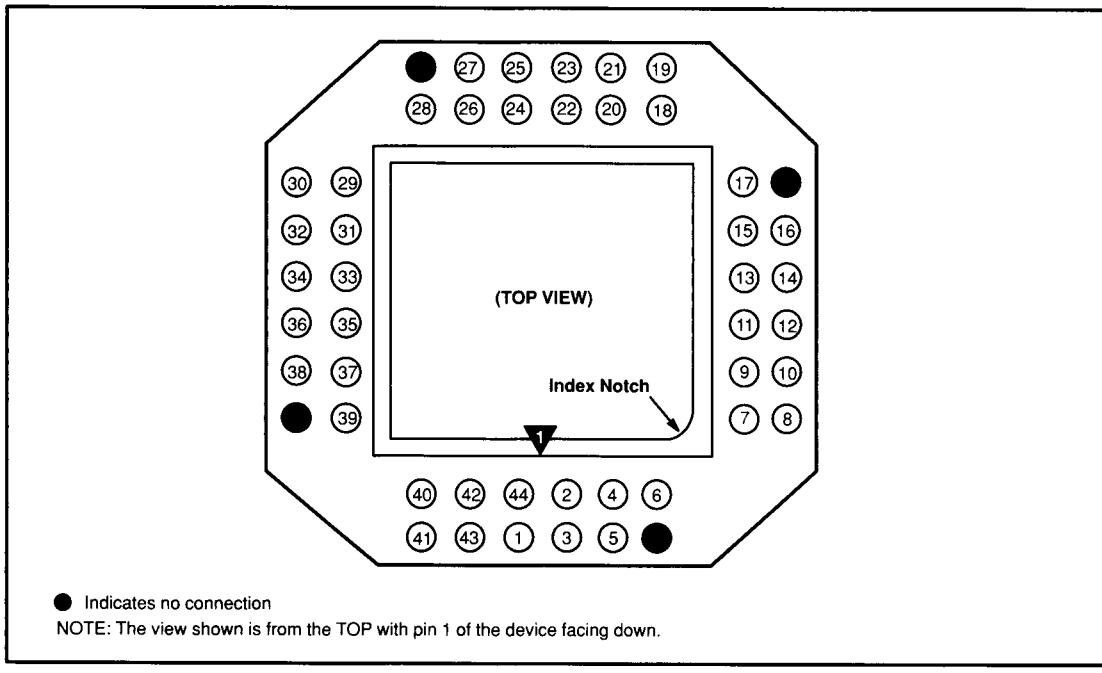


Figure 43. 44-Pin PLCC Actionprobe

TEXAS INSTRUMENTS
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actionprobe pin assignments (continued)

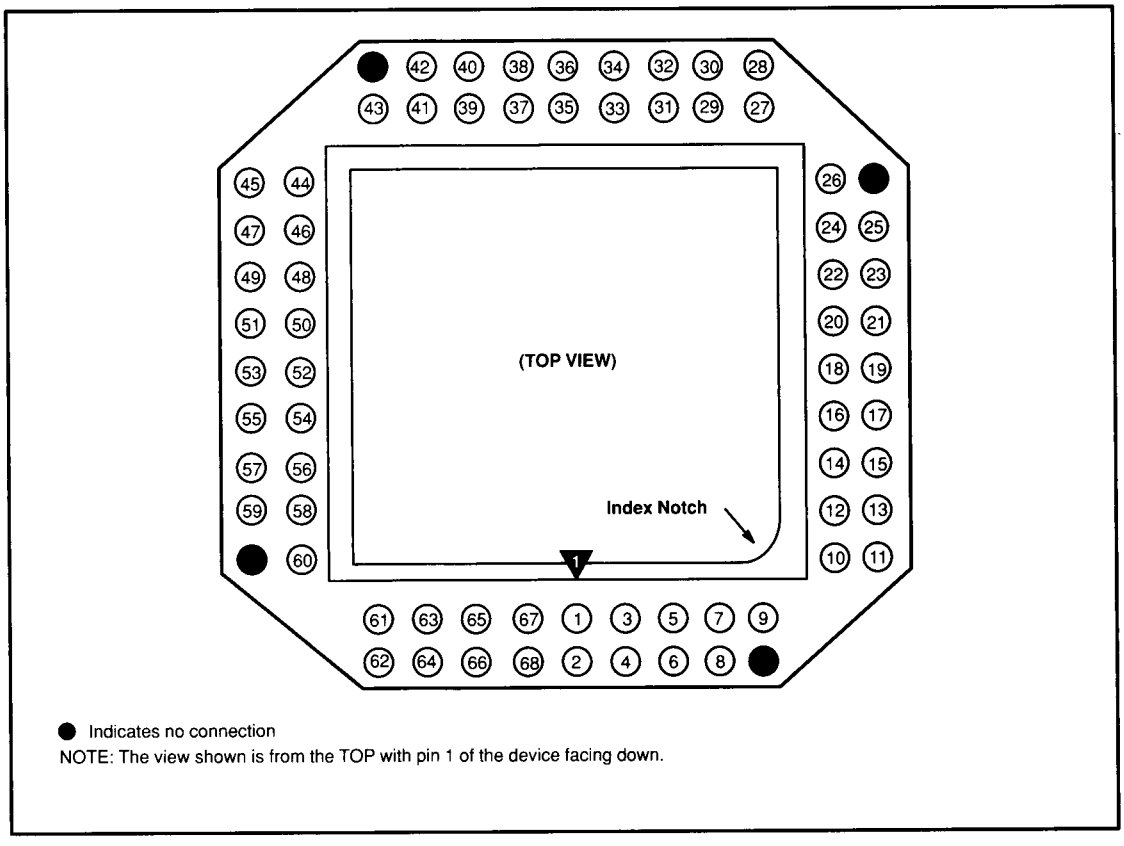
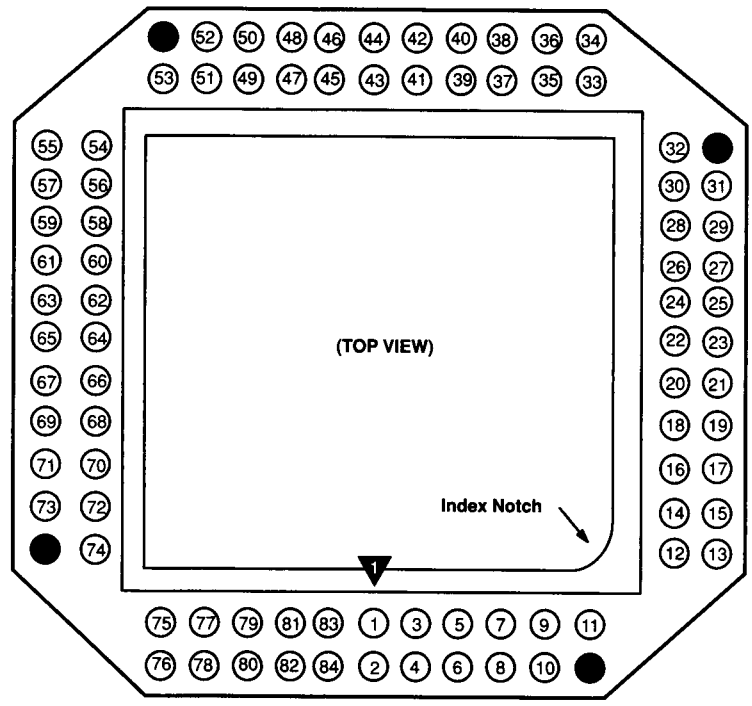


Figure 44. 68-Pin PLCC Actionprobe

actionprobe pin assignments (continued)



● Indicates no connection

NOTE: The view shown is from the TOP with pin 1 of the device facing down.

Figure 45. 84-Pin PLCC Actionprobe

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actionprobe pin assignments (continued)

The 84-pin pin-grid-array (PGA) Actionprobe has a number of pins around the socket connected to the device pins. The exact ordering of these pins is not obvious.

Figure 46 shows the Actionprobe with the top view up, which is how the device sits in the socket. Pin A1 is at the top left. Looking at the Actionprobe, pin A1 appears on the circuit board for reference.

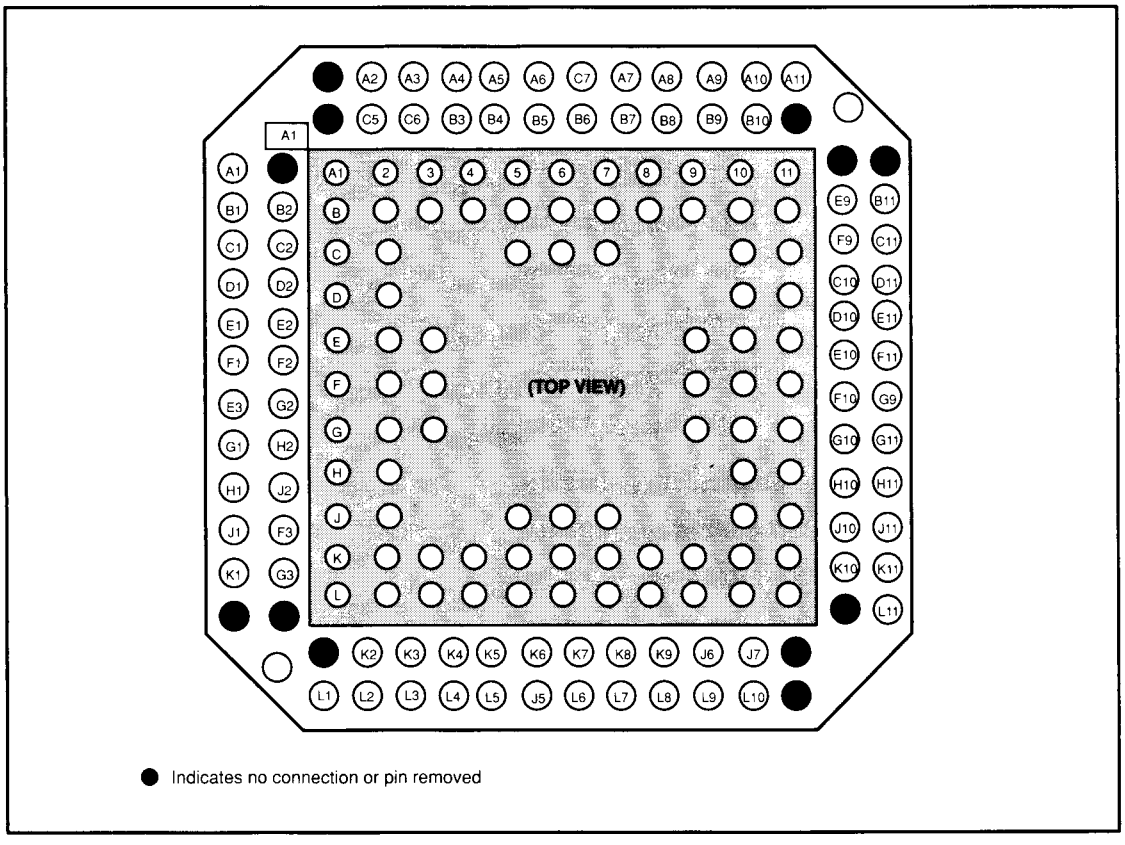
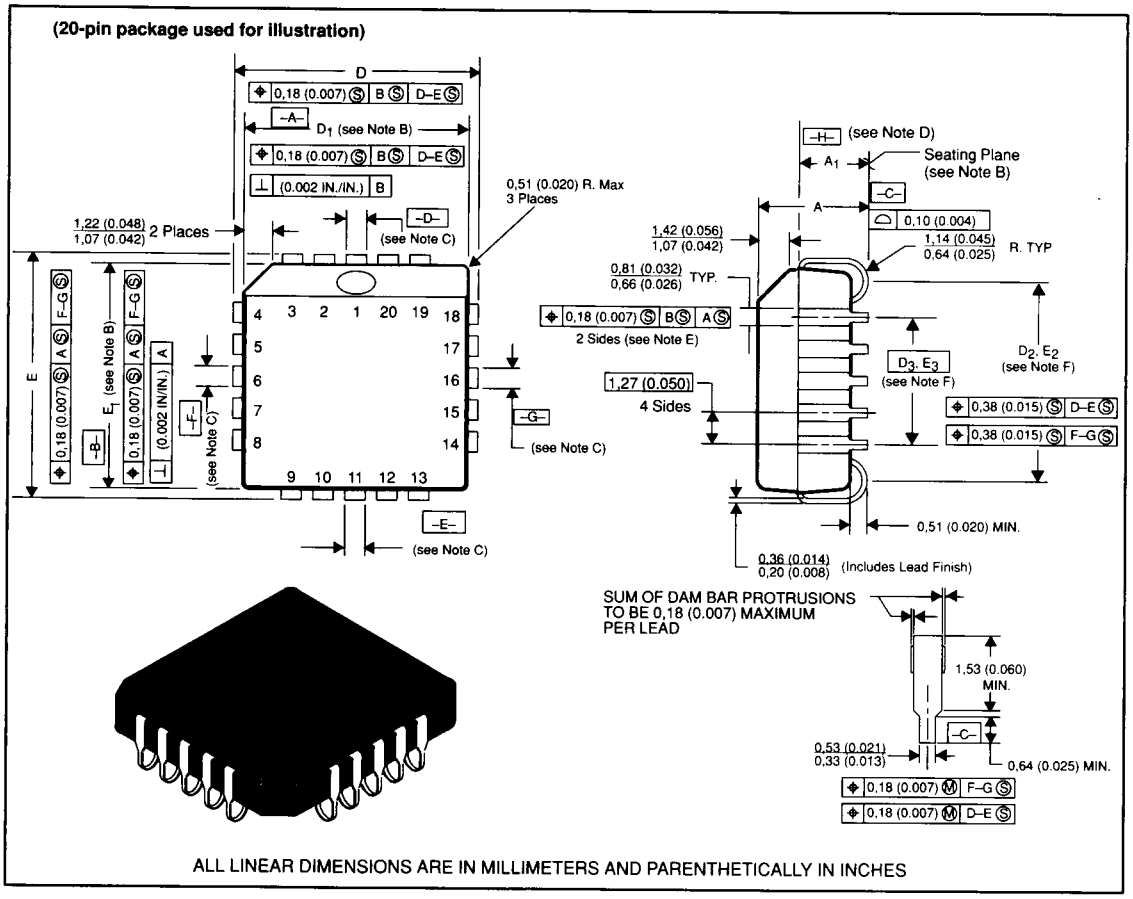


Figure 46. 84-Pin PGA Actionprobe



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

JEDEC OUTLINE	DIMS / PINS	A MIN	A MAX	A1 MIN	A1 MAX	D, E MIN	D, E MAX	D1, E1 MIN	D1, E1 MAX	D2, E2 MIN	D2, E2 MAX	D3, E3 BASIC
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,04 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M-1982.

B. Dimension D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (.010) on any side.

C. Datums D–E and F–G for center leads are determined at datum –H–

D. Datum –H– is located at top of leads where they exit plastic body.

E. Location to datums –A– and –B– to be determined at datum –H–

F. Determined at seating plane –C–

Figure 47. Plastic Leaded Chip Carriers

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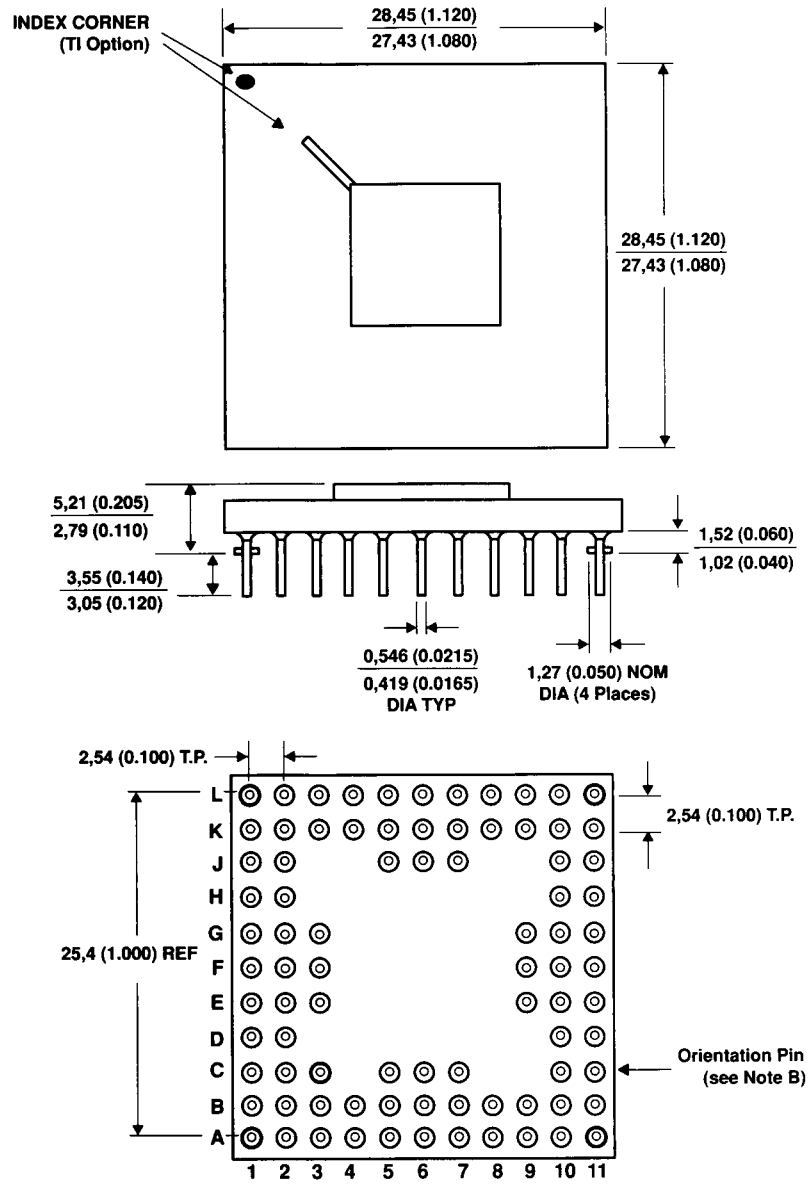
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



NOTES: A. Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,381 (0.051) radius relative to the center of the ceramic.
B. Orientation pin C3 is connected internally to pin C2.

Figure 48. 84-Pin Ceramic Pin-Grid-Array Package

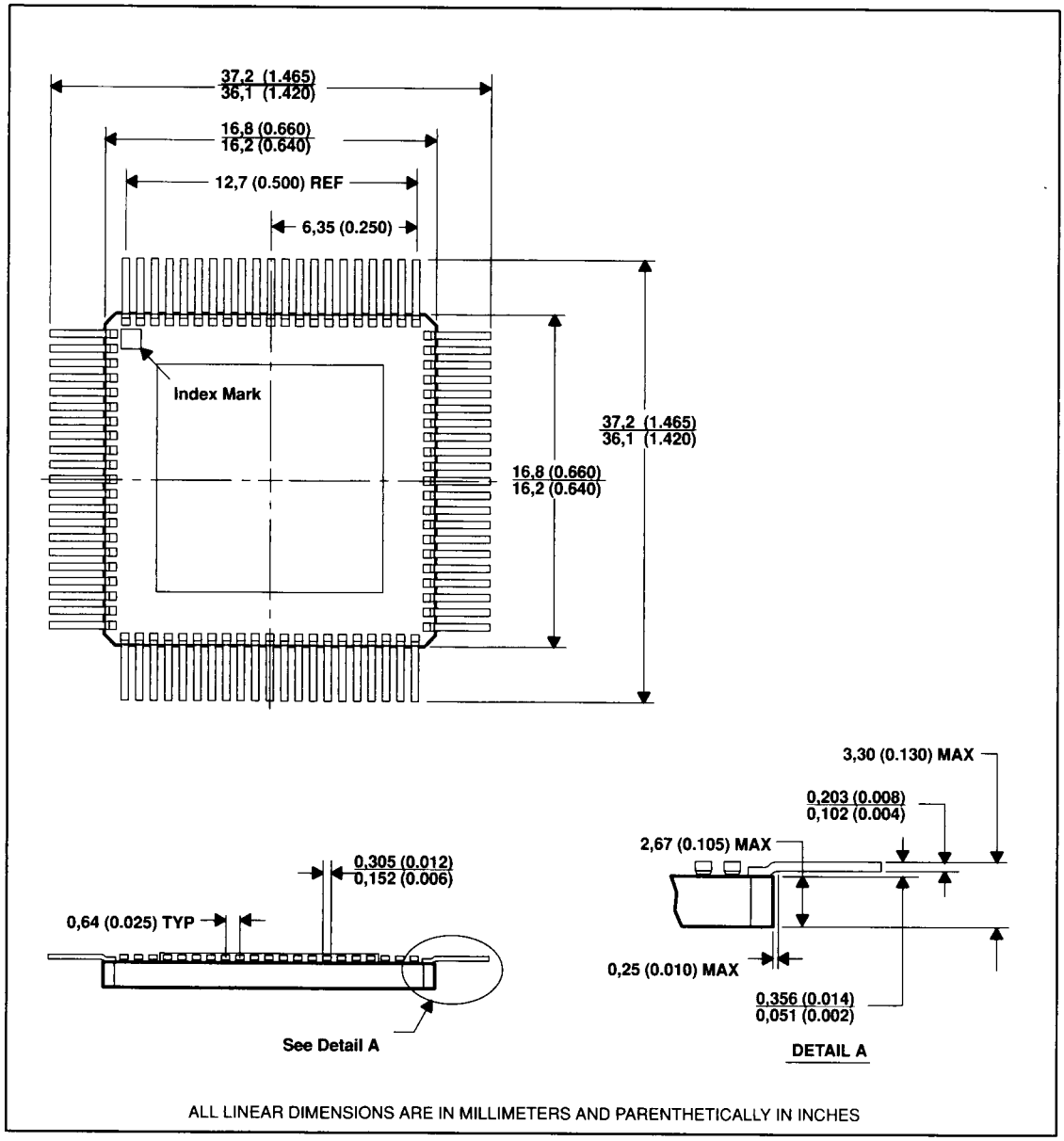


Figure 49. 84-Pin Ceramic Quad Flat Package

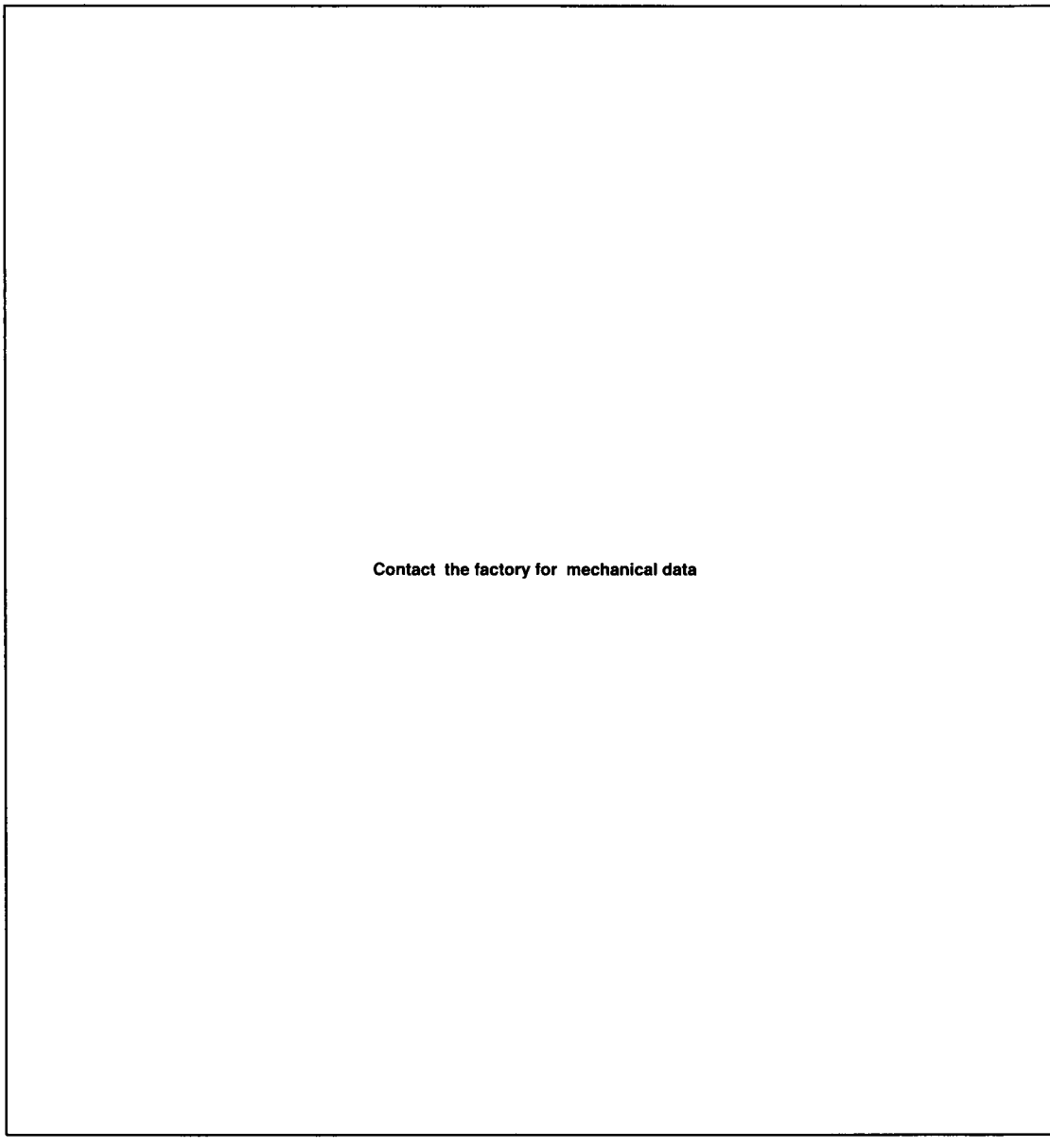


Figure 50. 84-Pin Ceramic Quad Flat Package With Nonconductive Tie Bar

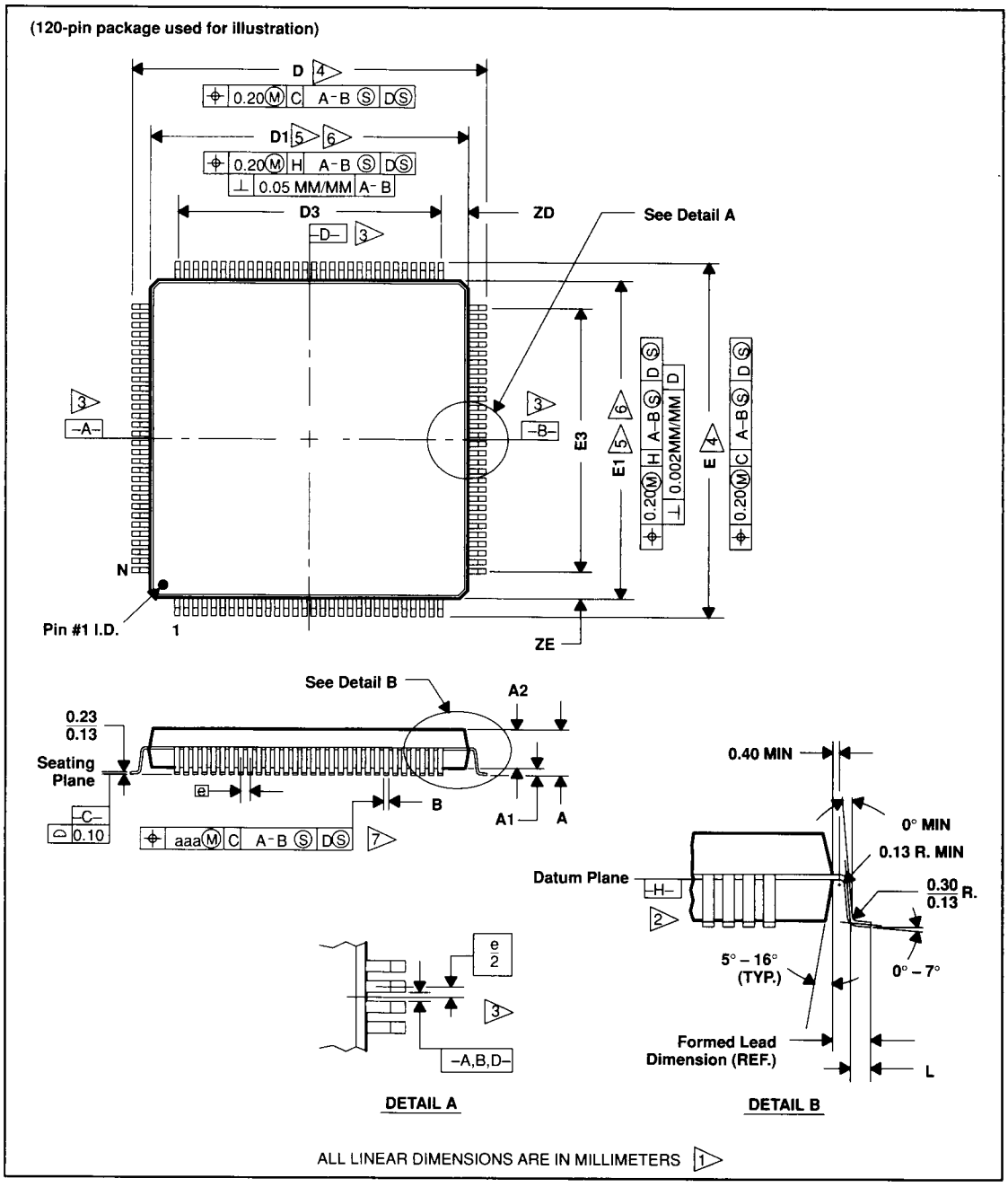


Figure 51. Plastic Quad Flat Packages

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JEDEC OUTLINE	# PINS	PKG TYPE	A MAX	A1 MIN	A2 MAX MIN	D MAX MIN	D1 MAX MIN	D3 (REF)	ZD (REF)	E MAX MIN	E1 MAX MIN	E3 (REF)	ZE (REF)	L MAX MIN	e BASIC	B MAX MIN	aaa	ND	NE	FORMED LEAD DIM. (REF)
MO-108/CC-1	100	RECT	3,40	0,25	3,05 2,55	23,45 22,95	20,10 19,90	18,85	0,58	17,45 16,95	14,10 13,90	12,35	0,83	0,95 0,65	0,65	0,38 0,22	0,12	30	20	1,60

NOTES:
1. All dimensions are millimeters (mm), and conform to JEDEC specification MO-108 (issue A/October 1990). Dimensions and tolerancing per ANSI Y14.5M-1982.
2. Datum plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
3. Datums A–B and –D– for center leads are determined at datum –H– .
4. Determined at seating plane –C–
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane –H– .
6. Determined at datum plane –H–
7. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. A minimum solder finish thickness of 0.0051 is guaranteed.

Following are the pin loadings for the TPC10 Series 1.2-µm and 1.0-µm CMOS Field-Programmable Gate Arrays. Use this with the TPC10 Series Data Sheet and the Critical Path Analysis for FPGAs application report located in the Applications Chapter in this manual, to estimate manually the achievable system speed for a design implemented in a TI TPC10 Series FPGA. The index below will help you find the desired item in this supplement.

Name	Page	Table
DLP1D	2-67	32
DLP1E	2-67	32
FA1	2-66	22
FA1A	2-66	22
FA1B	2-66	22
FA2A	2-66	23
FADD12	2-66	25
FADD16	2-66	26
FADD24	2-66	27
FADD32	2-67	28
FADD8	2-66	24
GAND2	2-71	49
GMX4	2-71	50
GNAND2	2-71	49
GNOR2	2-71	49
GOR2	2-71	49
GXOR2	2-71	49
HA1	2-66	21
HA1A	2-66	21
HA1B	2-66	21
HA1C	2-66	21
ICMP4	2-71	53
ICMP8	2-71	53
INBUF	2-65	11
INV	2-64	10
INVA	2-64	10
JKF	2-70	45
JKF1B	2-70	45
JKF2A	2-70	45
JKF2B	2-70	45
JKF2C	2-70	45
JKF2D	2-70	45
JKF3A	2-70	45
JKF3B	2-70	45
JKF3C	2-70	45
JKF3D	2-70	45
JKF4B	2-70	45
JKFPC	2-70	45
MAJ3	2-64	8
MCMP16	2-72	54
MCMPC2	2-72	54
MCMPC4	2-72	54
MCMPC8	2-72	54
MX16	2-65	17
MX2	2-65	12
MX2A	2-65	12
MX2B	2-65	12
MX2C	2-65	12
MX4	2-65	13
MX8	2-65	16
MX8A	2-65	16
MXC1	2-65	15
MXT	2-65	14
NAND2	2-62	1
NAND2A	2-62	1
NAND2B	2-62	1
NAND3	2-62	2
NAND3A	2-62	2
NAND3B	2-62	2
NAND3C	2-62	2
NAND4	2-63	3
NAND4A	2-63	3
NAND4B	2-63	3
NAND4C	2-63	3
NAND4D	2-63	3
NOR2	2-62	1
NOR2A	2-62	1
NOR2B	2-62	1
NOR3	2-62	2
NOR3A	2-62	2
NOR3B	2-62	2
NOR3C	2-62	2
NOR4	2-63	3
NOR4A	2-63	3
NOR4B	2-63	3
NOR4C	2-63	3
NOR4D	2-63	3
OA1	2-64	9
OA1A	2-64	9
OA1B	2-64	9
OA1C	2-64	9
OA2	2-64	9
OA2A	2-64	9
OA3	2-64	9
OA3A	2-64	9
OA3B	2-64	9
OA4A	2-64	9
OA5	2-64	9
OAI1	2-64	9
OAI2A	2-64	9
OAI3	2-64	9
OAI3A	2-64	9
OR2	2-62	1
OR2A	2-62	1
OR2B	2-62	1
OR3	2-62	2
OR3A	2-62	2
OR3B	2-62	2
OR3C	2-62	2
OR4	2-63	3
OR4A	2-63	3
OR4B	2-63	3
OR4C	2-63	3
OR4D	2-63	3
OUTBUF	2-65	11
REGE8A	2-71	51
REGE8B	2-71	51
SMULT8	2-73	67
SREG4A	2-73	63
SREG8A	2-73	63
TA138	2-73	61
TA139	2-72	60
TA151	2-65	18
TA153	2-66	19
TA157	2-66	20
TA161	2-72	57
TA164	2-73	64
TA169	2-72	57
TA194	2-73	65
TA195	2-73	66
TA269	2-72	58
TA273	2-71	52
TA280	2-72	55
TA377	2-71	52
TRIBUFF	2-65	11
UDCNT4A	2-72	59
XO1	2-63	5
XO1A	2-63	5
XA1	2-63	6
XA1A	2-63	6
XNOR	2-63	4
XOR	2-63	4

Table 1. 2-Input Gates

	A	B	Y
AND2	1	1	0
AND2A	1	1	0
AND2B	1	1	0
NAND2	1	1	0
NAND2A	1	1	0
NAND2B	1	1	0
OR2	1	1	0
OR2A	1	1	0
OR2B	1	1	0
NOR2	1	1	0
NOR2A	1	1	0
NOR2B	1	1	0

Table 2. 3-Input Gates

	A	B	C	Y
AND3	1	1	1	0
AND3A	1	1	1	0
AND3B	1	1	1	0
AND3C	1	1	1	0
NAND3	1	1	1	0
NAND3A	1	1	1	0
NAND3B	1	1	1	0
NAND3C	1	1	1	0
OR3	1	1	1	0
OR3A	1	1	1	0
OR3B	1	1	1	0
OR3C	1	1	1	0
NOR3	1	1	1	0
NOR3A	1	1	1	0
NOR3B	1	1	1	0
NOR3C	1	1	1	0

Table 3. 4-Input Gates

	A	B	C	D	Y
AND4	1	1	1	1	0
AND4A	1	1	1	1	0
AND4B	1	1	1	1	0
AND4C	1	1	1	1	0
AND4D	1	1	1	1	0
NAND4	1	1	1	1	0
NAND4A	1	1	1	1	0
NAND4B	1	1	1	1	0
NAND4C	1	1	1	1	0
NAND4D	1	1	1	1	0
OR4	1	1	1	1	0
OR4A	1	1	1	1	0
OR4B	1	1	1	1	0
OR4C	1	1	1	1	0
OR4D	1	1	1	1	0
NOR4	1	1	1	1	0
NOR4A	1	1	1	1	0
NOR4B	1	1	1	1	0
NOR4C	1	1	1	1	0
NOR4D	1	1	1	1	0

Table 4. XNOR/XOR Gates

	A	B	Y
XNOR	1	1	0
XOR	1	1	0

Table 5. XOR-OR/XNOR-OR Gates

	A	B	C	Y
XO1	1	1	2	0
XO1A	1	1	2	0

Table 6. XOR-AND/XNOR-AND Gates

	A	B	C	Y
XA1	1	1	2	0
XA1A	1	1	2	0

Table 7. AND-XOR/AND-XNOR Gates

	A	B	C	Y
AX1	2	2	1	0
AX1A	2	2	1	0
AX1B	1	1	1	0

Table 8. AND-OR/AND-NOR Gates

	A	B	C	D	Y
AO1	1	1	1	NA	0
AO1A	1	1	2	NA	0
AO1B	1	1	1	NA	0
AO1C	1	1	1	NA	0
AO2	1	1	1	1	0
AO2A	1	1	2	2	0
AO3	1	1	1	2	0
AO4A	1	1	1	1	0
AO5A	1	1	1	1	0
AOI1	1	1	1	NA	0
AOI1A	1	1	1	NA	0
AOI1B	1	1	2	NA	0
AOI2A	1	1	1	1	0
AOI2B	1	1	2	2	0
AOI3A	2	1	1	1	0
AOI4	1	1	1	1	0
MAJ3	2	2	2	NA	0

Table 9. OR-AND/OR-NAND Gates

	A	B	C	D	Y
OA1	1	1	1	NA	0
OA1A	1	1	2	NA	0
OA1B	1	1	1	NA	0
OA1C	1	1	1	NA	0
OA3	1	1	1	1	0
OA3A	1	1	1	2	0
OA3B	1	1	2	2	0
OA2	1	1	1	1	0
OA2A	1	1	1	1	0
OA4A	1	1	1	2	0
OA5	2	1	1	1	0
OAI1	1	1	1	NA	0
OAI2A	1	1	1	2	0
OAI3	1	1	1	1	0
OAI3A	1	1	2	2	0

Table 10. Buffers

	A	Y2
BUF	1	0
BUFA	1	0
INV	1	0
INVA	1	0

Table 11. I/O Buffers

	D	E	Y
INBUF	NA	NA	0
CLKBUF	NA	NA	0
OUTBUF	1	NA	0
TRIBUFF	1	1	0
BIBUF	1	1	0
CLKBIBUF	1	1	0

Table 12. 2:1 Multiplexers

	A	B	S	Y
MX2	1	1	1	0
MX2A	1	1	2	0
MX2B	1	1	1	0
MX2C	1	1	2	0

Table 13. 4:1 Multiplexer

	D0	D1	D2	D3	S1	S0	Y
MX4	1	1	1	1	1	1	0

Table 14. 4:1 Multiplexer

	D0	D1	D2	D3	S0A	S0B	S1	Y
MXT	1	1	1	1	1	1	1	0

Table 15. Other Multiplexer

	S	A	B	C	D	Y
MXC1	1	1	1	2	2	0

Table 16. 8:1 Multiplexer

	S2	S1	S0	D0–D7	Y
MX8	1	2	2	1	0
MX8A	2	2	2	1	0

Table 17. 16:1 Multiplexer

	S3	S2	S1	S0	D0–D15	Y
MX16	1	1	4	4	1	0

Table 18. 8:1 Multiplexer

	A	B	C	EN	D0–D7	Y	W
TA151	2	2	1	2	1	0	0

Table 19. 4:1 Multiplexer

	A	B	EN	C0	C1	C2	C3	Y
TA153	1	1	1	1	1	1	1	0

Table 20. 2:1 Multiplexer

	A	B	S	EN	Y
TA157	1	1	1	1	0

Table 21. Half Adders

	A	B	CO	S
HA1	2	2	0	0
HA1A	2	2	0	0
HA1B	2	2	0	0
HA1C	2	2	0	0

Table 22. Full Adders

	A	B	CI	CO	S
FA1	2	4	5	0	0
FA1A	3	3	3	2	0
FA1B	2	3	3	2	0

Table 23. Full Adder

	A0	A1	B	CI	CO	S
FA2A	2	2	3	3	2	0

Table 24. 8-Bit Fast Adder

	A0, A1	A2–A7	B0, B1	B2–B7	CI	S0–S7	CO
FADD8	2	4	3	6	3	0	0

Table 25. 12-Bit Fast Adder

	A0, A1	A2–A11	B0, B1	B2–B11	CI	S0–S11	CO
FADD12	2	4	3	6	3	0	0

Table 26. 16-Bit Fast Adder

	A0, A1	A2–A15	B0, B1	B2–B15	CI	S0–S15	CO
FADD16	2	4	3	6	3	0	0

Table 27. 24-Bit Fast Adder

	A0, A1	A2–A23	B0, B1	B2–B23	CI	S0–S23	CO
FADD24	2	4	3	6	3	0	0

Table 28. 32-Bit Fast Adder

	A0, A1	A2–A31	B0, B1	B2–B31	CI	S0–S31	CO
FADD32	2	4	3	6	3	0	0

Table 29. D-Type Latches

	D	G	Q/QN
DL1	1	1	1
DL1A	1	1	1
DL1B	1	1	1
DL1C	1	1	1

Table 30. D-Type Latches with Clear

	D	G	CLR	Q
DLC	1	1	1	1
DLCA	1	1	1	1
DLC1	1	1	1	1
DLC1A	1	1	1	1
DLC1F	1	1	2	1
DLC1G	1	1	2	1

Table 31. D-Type Latch with Clear

	G	CLR	D0–D7	Q0–Q7
DLC8A	8	8	1	1

Table 32. D-Type Latches with Preset

	D	G	PRE	Q
DLP1	1	1	2	1
DLP1A	1	1	2	1
DLP1B	1	1	1	1
DLP1C	1	1	1	1
DLP1D	1	1	2	1
DLP1E	1	1	2	1

Table 33. D-Type Latches with Clear and Preset

	D	G	PRE	CLR	Q/QN
DL2A	1	1	2	2	1
DL2B	1	1	2	2	1
DL2C	1	1	2	2	1
DL2D	1	1	2	2	1

Table 34. D-Type Latches with Enable

	D	E	G	Q
DLE	1	1	1	2
DLEA	1	1	1	2
DLEB	1	1	1	2
DLEC	1	1	1	2
DLE1D	1	1	1	1

Table 35. D-Type Latches with Enable, Clear, and Preset

	D	E	G	PRE	CLR	Q
DLE2A	1	1	1	NA	2	2
DLE2B	1	1	1	NA	1	1
DLE2C	1	1	1	NA	1	1
DLE3A	1	1	1	2	NA	2
DLE3B	1	1	1	1	NA	1
DLE3C	1	1	1	1	NA	1

Table 36. D-Type Latch with Enable

	G	E	D0–D7	Q0–Q7
DLE8	8	8	1	2

Table 37. D-Type Latches with Multiplexed Inputs

	A	B	S	E	G	Q	CLR
DLM	1	1	1	NA	1	1	NA
DLM2A	1	1	1	NA	1	1	2
DLMA	1	1	1	NA	1	1	NA
DLME1A	1	1	1	1	1	1	NA

Table 38. D-Type Latch with Multiplexed Inputs

	G	S	A0–A7	B0–B7	Q0–Q7
DLM8	8	8	1	1	1

Table 39. D-Type Flip-Flops

	D	CLK	Q/QN
DF1	1	2	1
DF1A	1	2	1
DF1B	1	2	1
DF1C	1	2	1

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Table 40. D-Type Flip-Flops with Clear

	D	CLK	CLR	Q/QN
DFC1	1	2	2	1
DFC1A	1	2	2	1
DFC1B	1	2	2	1
DFC1C	1	2	3	1
DFC1D	1	2	2	1
DFC1E	1	2	2	1
DFC1F	1	2	3	1
DFC1G	1	2	2	1

Table 41. D-Type Flip-Flops with Preset

	D	CLK	PRE	Q/QN
DFP1	1	2	3	1
DFP1A	1	2	3	1
DFP1B	1	2	2	1
DFP1C	1	2	2	1
DFP1D	1	2	2	1
DFP1E	1	2	2	1
DFP1F	1	2	2	1
DFP1G	1	2	2	1

Table 42. D-Type Flip-Flops with Preset and Clear

	D	CLR	PRE	CLK	Q
DFPC	1	3	3	2	1
DFPCA	1	3	3	2	1

Table 43. D-Type Flip-Flops with Enable

	D	E	CLK	Q
DFE	1	1	2	2
DFEA	1	1	2	2
DFE1B	1	1	2	2
DFE1C	1	1	2	2

Table 44. D-Type Flip-Flops with Enable, Preset, and Clear

	D	E	CLR	PRE	CLK	Q
DFEB	1	1	3	3	2	2
DFEC	1	1	3	3	2	2
DFED	1	1	3	3	2	2
DFE2D	1	1	3	3	2	2
DFE3A	1	1	2	NA	2	2
DFE3B	1	1	2	NA	2	2
DFE3C	1	1	2	NA	2	2
DFE3D	1	1	2	NA	2	2
DFE4	1	1	NA	3	2	2
DFE4A	1	1	NA	3	2	2
DFE4B	1	1	NA	3	2	2
DFE4C	1	1	NA	3	2	2

Table 45. J-K Flip-Flops

	J	K	PRE	CLR	CLK	Q
JKF	1	1	NA	NA	2	2
JKFPC	1	1	3	3	2	2
JKF1B	1	1	NA	NA	2	2
JKF2A	1	1	NA	2	2	2
JKF2B	1	1	NA	2	2	2
JKF2C	1	1	NA	2	2	2
JKF2D	1	1	NA	2	2	2
JKF3A	1	1	2	NA	2	2
JKF3B	1	1	2	NA	2	2
JKF3C	1	1	3	NA	2	2
JKF3D	1	1	3	NA	2	2
JKF4B	1	1	3	3	2	2

Table 46. Multiplexed-Input Flip-Flops

	A	B	S	CLR	E	CLK	Q
DFM	1	1	1	NA	NA	2	1
DFMA	1	1	1	NA	NA	2	1
DFMB	1	1	1	2	NA	2	1
DFME1A	1	1	1	NA	2	2	2
DFM1B	1	1	1	NA	NA	2	1
DFM1C	1	1	1	NA	NA	2	1
DFM3	1	1	1	2	NA	2	1
DFM3B	1	1	1	2	NA	2	1
DFM3E	1	1	1	2	NA	2	1
DFM3F	1	1	1	3	NA	2	1
DFM3G	1	1	1	3	NA	2	1

Table 47. Multiplexed-Input Flip-Flops with Preset

	A	B	S	PRE	CLK	Q
DFM4	1	1	1	3	2	1
DFM4A	1	1	1	2	2	1
DFM4B	1	1	1	2	2	1
DFM4C	1	1	1	3	2	1
DFM4D	1	1	1	3	2	1
DFM4E	1	1	1	3	2	1

Table 48. Multiplexed-Input Flip-Flops with Preset and Clear

	A	B	S	CLR	PRE	CLK	Q
DFM5A	1	1	1	3	3	3	1
DFM5B	1	1	1	3	3	2	1

Table 49. Clock Buffer (CLKBUF) Interface

	A	G	Y
GAND2	1	1	0
GNAND2	1	1	0
GOR2	1	1	0
GNOR2	1	1	0
GXOR2	1	1	0

Table 50. Clock Buffer (CLKBUF) Interface

	D0	D1	D2	D3	G	S0	Y
GMX4	1	1	1	1	1	1	0

Table 51. Octal D-Type Flip-Flops and Registers

	CLK	CLR	D0–D7	Q0–Q7	PRE	E
REGE8A	16	2	1	2	2	8
REGE8B	16	2	1	2	2	8

Table 52. Octal D-Type Flip-Flops and Registers

	CLK	CLR	EN	D1–D8	Q1–Q8
TA273	16	2	NA	1	1
TA377	16	NA	8	1	2

Table 53. Identity Comparators

	An	Bn	AEB
ICMP4	1	1	0
ICMP8	1	1	0

Table 54. Magnitude Comparators

	An	Bn	ALBI	AEBI	AGBI	ALB	AEB	AGB
MCMP16	3	3	NA	NA	NA	0	0	0
MCMPC2	3	3	1	1	1	0	0	0
MCMPC4	3	3	1	1	1	0	0	0
MCMPC8	3	3	1	1	1	0	0	0

Table 55. Parity Checker

	A	B	C	D	E	F	G	H	I	ODD	EVEN
TA280	1	1	1	1	1	1	1	1	1	0	0

Table 56. Binary Counters

	CLR	CLK	LD	CI	P0–P3	Q0	Q1	Q2	Q3	CO
CNT4A	8	8	4	8	1	6	5	4	3	0
CNT4B	8	8	4	9	1	6	4	3	3	0

Table 57. Synchronous Counters

	LD	UD	ENT	ENP	CLR	CLK	A	B	C	D	QA	QB	QC	QD	RCO
TA161	1	NA	2	1	1	8	1	1	1	1	6	5	4	3	0
TA169	4	5	3	3	NA	8	1	1	1	1	7	6	4	4	0

Table 58. Synchronous Counter

	CLK	LD	UD	ENP	ENT	A–H	QA, QE	QB, QF	QC, QD, QG, QH	RCO
TA269	16	8	1	3	3	1	7	6	4	0

Table 59. Synchronous Counter

	LD	UD	CI	CLK	P0–P3	Q0	Q1	Q2	Q3	CO
UDCNT4A	4	5	9	8	1	7	6	4	4	0

Table 60. 2-to-4 Decoders

	A	B	E/EN	Y0–Y3
DEC2X4	4	4	NA	0
DEC2X4A	4	4	NA	0
DECE2X4	4	4	4	0
DECE2X4A	4	4	4	0
TA139	4	4	4	0

Table 61. 3-to-8 Decoders

	A	B	C	E	G1	G2A	G2B	Y0–77
DEC3X8	8	8	8	NA	NA	NA	NA	0
DEC3X8A	8	8	8	NA	NA	NA	NA	0
DECE3X8	5	5	5	8	NA	NA	NA	0
DECE3X8A	5	5	5	8	NA	NA	NA	0
TA138	5	5	5	NA	1	1	1	0

Table 62. 4-to-16 Decoder

	A	B	C	D	Y0–Y15
DEC4X16A	9	9	9	9	0

Table 63. Shift Registers

	CLR	CLK	SHLD	SI	Pn	SO
SREG4A	8	8	4	1	1	1
SREG8A	2	16	8	1	1	1

Table 64. Shift Register

	CLK	CLR	A	B	QA	QB	QC	QD	QE	QF	QG	QH
TA164	16	2	1	1	2	2	2	2	2	2	2	1

Table 65. Shift Register

	CLK	CLR	S1	S0	SLSI	SRSI	A	B	C	D	QA	QB	QC	QD
TA194	8	8	1	1	1	1	1	1	1	1	3	4	4	3

Table 66. Shift Register

	CLK	CLR	J	K	SHLD	A	B	C	D	QA	QB	QC	QD	QDN
TA195	8	8	1	1	4	1	1	1	1	4	2	2	2	0

Table 67. 8-Bit Multiplier

	A0–A2, A4–A6	A3	A7	B0, B4	B1–B3, B5–B7	P0–P15
SMULT8	6	9	14	8	4	0

Table 68. Logic Module

	A0, A1	B0, B1	SA, SB	S0, S1	Y
CM8A	1	1	1	1	0