Features

- High Performance, Low Power AVR®32 32-Bit Microcontroller
  - 210 DMIPS throughput at 150 MHz
  - 16 KB instruction cache and 16 KB data caches
  - Memory Management Unit enabling use of operating systems
  - Single-cycle RISC instruction set including SIMD and DSP instructions
  - Java Hardware Acceleration
- Pixel Co-Processor
  - Pixel Co-Processor for video acceleration through color-space conversion (YUV<->RGB), image scaling and filtering, quarter pixel motion compensation
- Multi-hierarchy bus system
  - High-performance data transfers on separate buses for increased performance
- Data Memories
  - 32KBytes SRAM
- External Memory Interface
  - SDRAM, DataFlash™, SRAM, Multi Media Card (MMC), Secure Digital (SD),
  - Compact Flash, Smart Media, NAND Flash
- Direct Memory Access Controller
  - External Memory access without CPU intervention
- Interrupt Controller
  - Individually maskable Interrupts
  - Each interrupt request has a programmable priority and autovector address
- System Functions
  - Power and Clock Manager
  - Crystal Oscillator with Phase-Lock-Loop (PLL)
  - Watchdog Timer
  - Real-time Clock
- 6 Multifunction timer/counters
  - Three external clock inputs, I/O pins, PWM, capture and various counting capabilities
- 4 Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - 115.2 kbps IrDA Modulation and Demodulation
  - Hardware and software handshaking
- 3 Synchronous Serial Protocol controllers
  - Supports I2S, SPI and generic frame-based protocols
- Two-Wire Interface
  - Sequential Read/Write Operations, Philips' $I^2C^{©}$ compliant
- Liquid Crystal Display (LCD) interface
  - Supports TFT displays
  - Configurable pixel resolution supporting QCIF/QVGA/VGA/SVGA configurations.
- Image Sensor Interface
  - 12-bit Data Interface for CMOS cameras
- Universal Serial Bus (USB) 2.0 High Speed (480 Mbps) Device
  - On-chip Transceivers with physical interface
- 2 Ethernet MAC 10/100 Mbps interfaces
  - 802.3 Ethernet Media Access Controller
  - Supports Media Independent Interface (MII) and Reduced MII (RMII)
- 16-bit stereo audio bitstream DAC
  - Sample rates up to 50 kHz
- On-Chip Debug System
  - Nexus Class 3
  - Full speed, non-intrusive data and program trace
  - Runtime control and JTAG interface
- Package/Pins
  - AT32AP7000: 256-ball CTBGA 1.0 mm pitch/160 GPIO pins
- Power supplies
  - 1.65V to1.95V VDDCORE
  - 3.0V to 3.6V VDDIO

AVR®32 32-bit Microcontroller

AT32AP7000

Preliminary

32003M-AVR32-09/09

1. Part Description

The AT32AP7000 is a complete System-on-chip application processor with an AVR32 RISC processor achieving 210 DMIPS running at 150 MHz. AVR32 is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high application performance.

AT32AP7000 implements a Memory Management Unit (MMU) and a flexible interrupt controller supporting modern operating systems and real-time operating systems. The processor also includes a rich set of DSP and SIMD instructions, specially designed for multimedia and telecom applications.

AT32AP7000 incorporates SRAM memories on-chip for fast and secure access. For applications requiring additional memory, external 16-bit SRAM is accessible. Additionally, an SDRAM controller provides off-chip volatile memory access as well as controllers for all industry standard off-chip non-volatile memories, like Compact Flash, MultiMedia Card (MMC), Secure Digital (SD)-card, SmartCard, NAND Flash and Atmel DataFlash™.

The Direct Memory Access controller for all the serial peripherals enables data transfer between memories without processor intervention. This reduces the processor overhead when transferring continuous and large data streams between modules in the MCU.

The Timer/Counters includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

AT32AP7000 also features an onboard LCD Controller, supporting single and double scan monochrome and color passive STN LCD modules and single scan active TFT LCD modules. On monochrome STN displays, up to 16 gray shades are supported using a time-based dithering algorithm and Frame Rate Control (FRC) method. This method is also used in color STN displays to generate up to 4096 colors.

The LCD Controller is programmable for supporting resolutions up to 2048 x 2048 with a pixel depth from 1 to 24 bits per pixel.

A pixel co-processor provides color space conversions for images and video, in addition to a wide variety of hardware filter support

The media-independent interface (MII) and reduced MII (RMII) 10/100 Ethernet MAC modules provides on-chip solutions for network-connected devices.

Synchronous Serial Controllers provide easy access to serial communication protocols, audio standards like I2S and frame-based protocols.

The Java hardware acceleration implementation in AVR32 allows for a very high-speed Java byte-code execution. AVR32 implements Java instructions in hardware, reusing the existing RISC data path, which allows for a near-zero hardware overhead and cost with a very high performance.

The Image Sensor Interface supports cameras with up to 12-bit data buses.

PS2 connectivity is provided for standard input devices like mice and keyboards.

AT32AP7000 integrates a class 3 Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

The C-compiler is closely linked to the architecture and is able to utilize code optimization features, both for size and speed.

2. Signals Description

The following table gives details on the signal name classified by peripheral. The pinout multiplexing of these signals is given in the Peripheral Muxing table in the Peripherals chapter.

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
AVDDPLL	PLL Power Supply	Power		1.65 to 1.95 V
AVDDUSB	USB Power Supply	Power		1.65 to 1.95 V
AVDDOSC	Oscillator Power Supply	Power		1.65 to 1.95 V
VDDCORE	Core Power Supply	Power		1.65 to 1.95 V
VDDIO	I/O Power Supply	Power		3.0 to 3.6V
AGNDPLL	PLL Ground	Ground		
AGNDUSB	USB Ground	Ground		
AGNDOSC	Oscillator Ground	Ground		
GND	Ground	Ground		
Clocks, Oscillators, and PLL's				
XIN0, XIN1, XIN32	Crystal 0, 1, 32 Input	Analog		
XOUT0, XOUT1, XOUT32	Crystal 0, 1, 32 Output	Analog		
PLL0, PLL1	PLL 0,1 Filter Pin	Analog		
JTAG				
TCK	Test Clock	Input		
TDI	Test Data In	Input		
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		
TRST_N	Test Reset	Input	Low	
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO0 - MDO5	Trace Data Output	Output		
MSEO0 - MSEO1	Trace Frame Control	Output		
EVTI_N	Event In	Input	Low	

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
EVTO_N	Event Out	Output	Low	
Power Manager - PM				
GCLK0 - GCLK4	Generic Clock Pins	Output		
OSCEN_N	Oscillator Enable	Input	Low	
RESET_N	Reset Pin	Input	Low	
WAKE_N	Wake Pin	Input	Low	
External Interrupt Controller - EIC				
EXTINT0 - EXTINT3	External Interrupt Pins	Input		
NMI_N	Non-Maskable Interrupt Pin	Input	Low	
AC97 Controller - AC97C				
SCLK	AC97 Clock Signal	Input		
SDI	AC97 Receive Signal	Output		
SDO	AC97 Transmit Signal	Output		
SYNC	AC97 Frame Synchronization Signal	Input		
Audio Bitstream DAC - ABDAC				
DATA0 - DATA1	D/A Data Out	Output		
DATAN0 - DATAN1	D/A Inverted Data Out	Output		
Ethernet MAC - MACB0, MACB1				
COL	Collision Detect	Input		
CRS	Carrier Sense and Data Valid	Input		
MDC	Management Data Clock	Output		
MDIO	Management Data Input/Output	I/O		
RXD0 - RXD3	Receive Data	Input		
RX_CLK	Receive Clock	Input		
RX_DV	Receive Data Valid	Input		
RX_ER	Receive Coding Error	Input		
SPEED	Speed	Output		
TXD0 - TXD3	Transmit Data	Output		

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
TX_CLK	Transmit Clock or Reference Clock	Input		
TX_EN	Transmit Enable	Output		
TX_ER	Transmit Coding Error	Output		
External Bus Interface - EBI				
PX0 - PX53	I/O Controlled by EBI	I/O		
ADDR0 - ADDR25	Address Bus	Output		
CAS	Column Signal	Output	Low	
CFCE1	Compact Flash 1 Chip Enable	Output	Low	
CFCE2	Compact Flash 2 Chip Enable	Output	Low	
CFRNW	Compact Flash Read Not Write	Output		
DATA0 - DATA31	Data Bus	I/O		
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NCS0 - NCS5	Chip Select	Output	Low	
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
NWE3	Write Enable 3	Output	Low	
RAS	Row Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output		
SDWE	SDRAM Write Enable	Output	Low	
Image Sensor Interface - ISI				
DATA0 - DATA11	Image Sensor Data	Input		
HSYNC	Horizontal Synchronization	Input		
PCLK	Image Sensor Data Clock	Input		

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
VSYNC	Vertical Synchronization	Input		
LCD Controller - LCDC				
CC	LCD Contrast Control	Output		
DATA0 - DATA23	LCD Data Bus	Input		
DVAL	LCD Data Valid	Output		
GPL0 - GPL7	LCD General Purpose Lines	Output		
HSYNC	LCD Horizontal Synchronization	Output		
MODE	LCD Mode	Output		
PCLK	LCD Clock	Output		
PWR	LCD Power	Output		
VSYNC	LCD Vertical Synchronization	Output		
MultiMedia Card Interface - MCI				
CLK	Multimedia Card Clock	Output		
CMD0 - CMD1	Multimedia Card Command	I/O		
DATA0 - DATA7	Multimedia Card Data	I/O		
Parallel Input/Output - PIOA, PIOB, PIOC, PIOD, PIOE				
PA0 - PA31	Parallel I/O Controller PIOA	I/O		
PB0 - PB30	Parallel I/O Controller PIOB	I/O		
PC0 - PC31	Parallel I/O Controller PIOC	I/O		
PD0 - PD17	Parallel I/O Controller PIOD	I/O		
PE0 - PE26	Parallel I/O Controller PIOE	I/O		
PS2 Interface - PSIF				
CLOCK0 - CLOCK1	PS2 Clock	Input		
DATA0 - DATA1	PS2 Data	I/O		
Serial Peripheral Interface - SPI0, SPI1				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS0 - NPCS3	SPI Peripheral Chip Select	I/O	Low	

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
SCK	Clock	Output		
Synchronous Serial Controller - SSC0, SSC1, SSC2				
RX_CLOCK	SSC Receive Clock	I/O		
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
DMA Controller - DMACA				
DMARQ0 - DMARQ3	DMA Requests	Input		
Timer/Counter - TIMER0, TIMER1				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI				
SCL	Serial Clock	I/O		
SDA	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input		
RTS	Request To Send	Output		
RXD	Receive Data	Input		

Table 2-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
TXD	Transmit Data	Output		
Pulse Width Modulator - PWM				
PWM0 - PWM3	PWM Output Pins	Output		
USB Interface - USBA				
HSDM	High Speed USB Interface Data -	Analog		
FSDM	Full Speed USB Interface Data -	Analog		
HSDP	High Speed USB Interface Data +	Analog		
FSDP	Full Speed USB Interface Data +	Analog		
VBG	USB bandgap	Analog		Connected to a 6810 Ohm ± 0.5% resistor to gound and a 10 pF capacitor to ground.

3. Power Considerations

3.1 Power Supplies

The AT32AP7000 has several types of power supply pins:

- **VDDCORE pins: Power the core, memories, and peripherals. Voltage is 1.8V nominal.**
- **VDDIO pins: Power I/O lines. Voltage is 3.3V nominal.**
- **VDDPLL pin: Powers the PLL. Voltage is 1.8V nominal.**
- **VDDUSB pin: Powers the USB. Voltage is 1.8V nominal.**
- **VDDOSC pin: Powers the oscillators. Voltage is 1.8V nominal.**

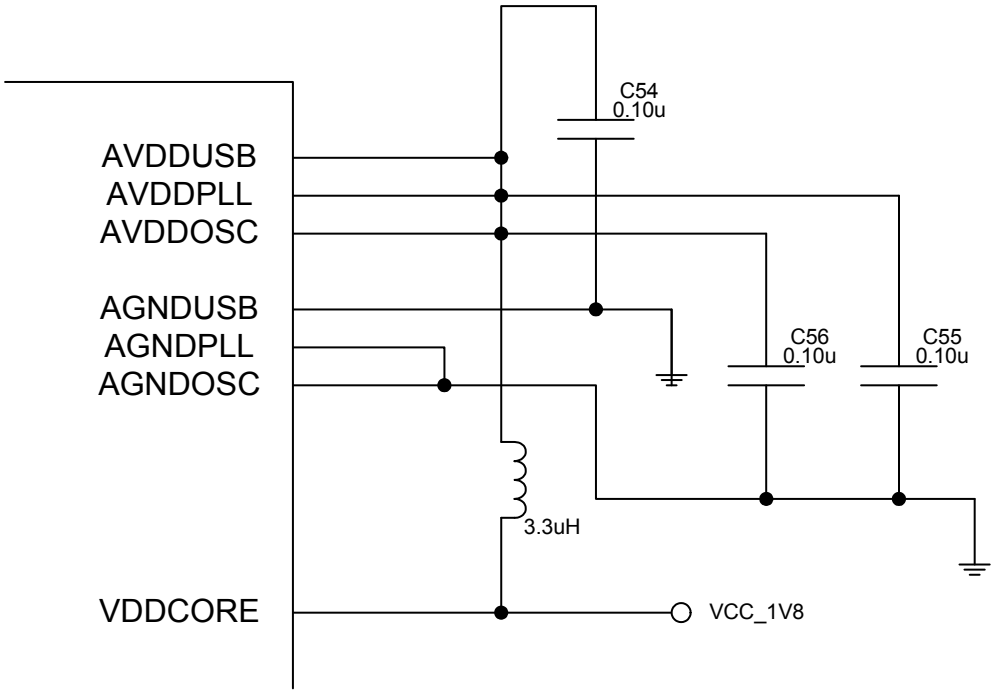
The ground pins GND are common to VDDCORE and VDDIO. The ground pin for VDDPLL is GNDPLL, and the GND pin for VDDOSC is GNDOSC.

See ”Electrical Characteristics” on page 930 for power consumption on the various supply pins.

3.2 Power Supply Connections

Special considerations should be made when connecting the power and ground pins on a PCB. Figure 3-1 shows how this should be done.

Figure 3-1. Connecting analog power supplies



3.3 Package and PinoutAVR32AP7000

Figure 3-2. 256 CTBGA Pinout

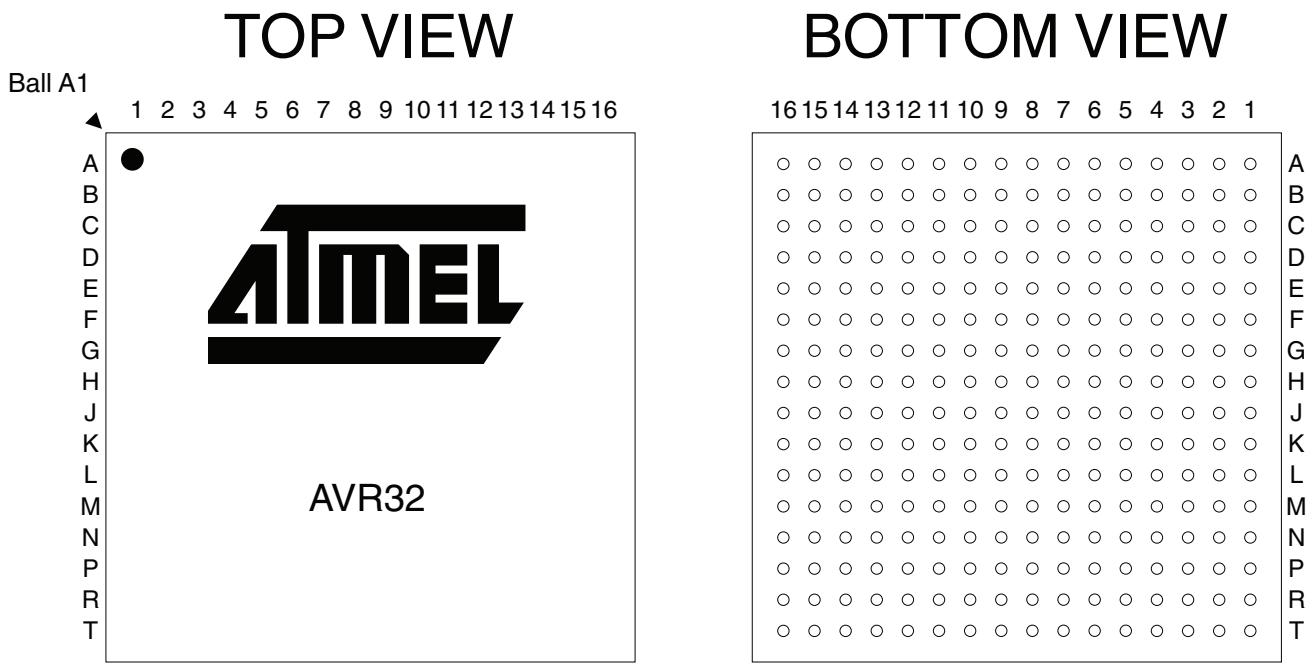


Table 3-1. CTBGA256 Package Pinout A1..T8

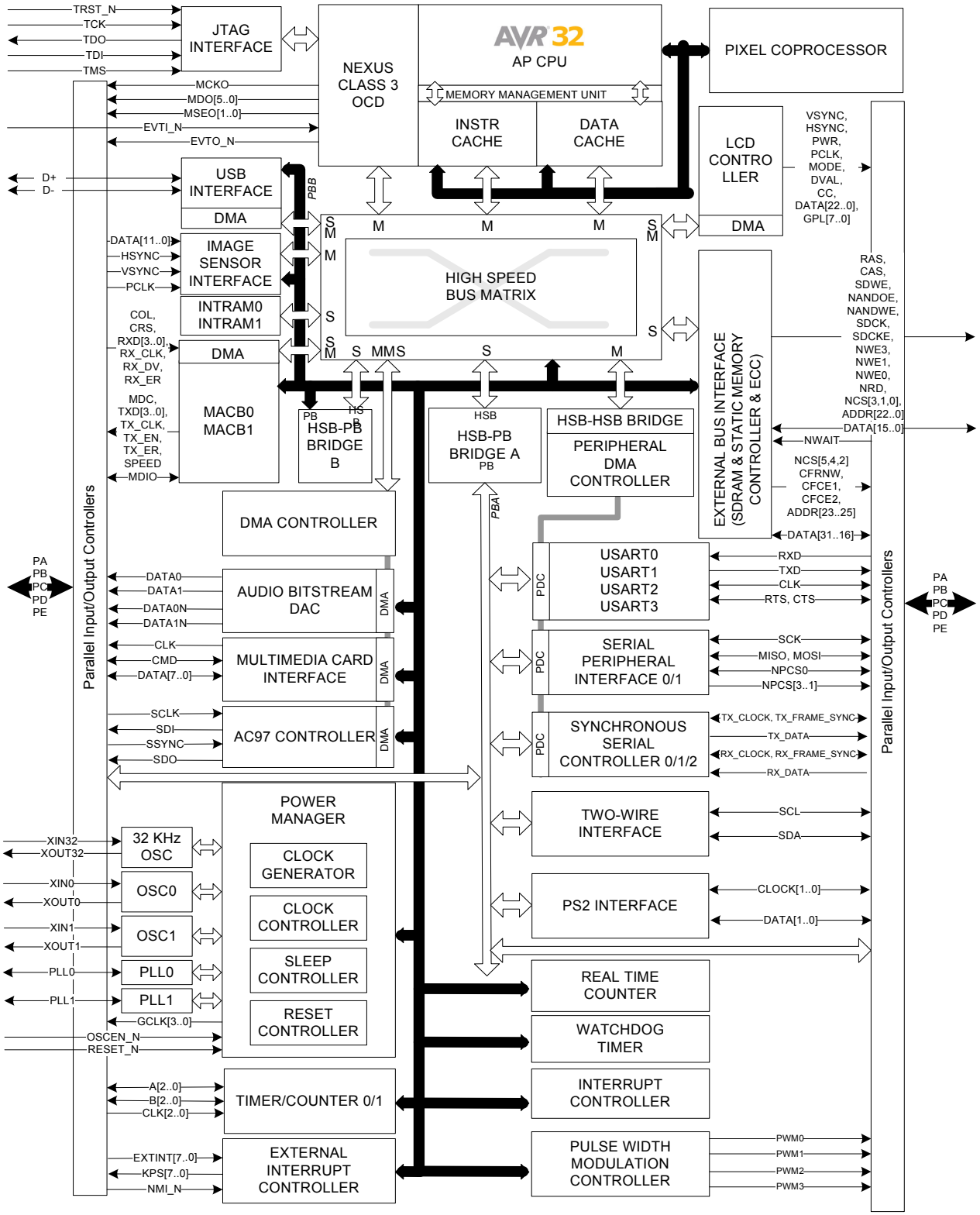
	1	2	3	4	5	6	7	8
A	VDDIO	PE15	PE13	PE11	PE07	PE02	AGNDPLL	OSCEN_N
B	GNDIO	PE16	PE12	PE09	PE04	PLL0	AVDDOSC	PC30
C	PD01	PD00	PE14	PE10	PE06	PE00	PLL1	PC31
D	PE17	PE18	PD02	PE08	PE03	GND	AGNDOSC	PC29
E	PX48	PX50	PX49	PX47	PE05	PE01	XOUT32	PC28
F	PX32	PX00	PX33	VDDIO	PX51	AVDDPLL	XIN0	PC27
G	PX04	VDDCORE	PX05	PX03	PX02	PX01	XOUT0	PC26
H	PD06	VDDIO	PD07	PD05	PD04	PD03	GND	XIN32
J	TRST_N	TMS	TDI	TCK	TDO	PD09	PD08	EVTI_N
K	PA05	PA01	PA02	PA00	RESET_N	PA03	PA04	HSDP
L	PA09	PB25	VDDIO	PA08	GND	PB24	AGNDUSB	VDDCORE
M	PA14	PA11	PA13	PA10	PA12	VDDIO	VDDIO	GND
N	PA18	PA16	PA17	PA15	PD14	GND	FSDM	VBG
P	PA20	PA19	PA21	PD11	PD16	XOUT1	GND	PA25
R	PA22	PD10	PA23	PD13	PD17	AVDDUSB	HSDM	PA26
T	VDDIO	GND	PA24	PD12	PD15	XIN1	FSDP	VDDIO

Table 3-2. CTBGA256 Package Pinout A9..T16

	9	10	11	12	13	14	15	16
A	PC23	PA06	PB21	PB16	PB13	PB11	GND	VDDIO
B	PC25	PC19	PB23	PB18	PB14	PB10	PC17	PC16
C	PC24	PA07	PB22	PB17	PB12	PB09	PB07	PB08
D	PC22	PC18	PB20	PB15	PB03	PB05	PB04	PB06
E	VDDIO	GND	PB19	PB00	PX46	PB01	VDDIO	PB02
F	PC21	VDDCORE	GND	PX44	PX42	PX43	PX40	PX45
G	PC20	PC15	PC14	PC10	PC11	PC13	PC12	VDDCORE
H	PC09	PC05	PC06	PE26	VDDIO	PC07	PX39	PC08
J	PB27	PX27	PX28	PX29	PX30	VDDCORE	GND	PX31
K	PA27	GND	PX22	PX23	PX24	PX26	VDDIO	PX25
L	PA28	VDDIO	PE24	PX38	PX18	PX20	PX21	PX19
M	PA29	PB28	PE20	PX08	PX34	PX36	PX37	PX35
N	PA30	PX53	PE22	PX06	PX11	PX15	PX17	PX16
P	WAKE_N	PX41	PE21	PX09	PB30	PC02	PX13	PX14
R	PA31	PX52	PE23	PX07	PB29	PC00	PC04	GND
T	PB26	PE25	PE19	PX10	PX12	PC01	PC03	VDDIO

4. Blockdiagram

Figure 4-1. Blockdiagram



4.0.1 AVR32AP CPU

- 32-bit load/store AVR32B RISC architecture.
  - Up to 15 general-purpose 32-bit registers.
  - 32-bit Stack Pointer, Program Counter and Link Register reside in register file.
  - Fully orthogonal instruction set.
  - Privileged and unprivileged modes enabling efficient and secure Operating Systems.
  - Innovative instruction set together with variable instruction length ensuring industry leading code density.
  - DSP extention with saturating arithmetic, and a wide variety of multiply instructions.
  - SIMD extention for media applications.
- 7 stage pipeline allows one instruction per clock cycle for most instructions.
  - Java Hardware Acceleration.
  - Byte, half-word, word and double word memory access.
  - Unaligned memory access.
  - Shadowed interrupt context for INT3 and multiple interrupt priority levels.
  - Dynamic branch prediction and return address stack for fast change-of-flow.
  - Coprocessor interface.
- Full MMU allows for operating systems with memory protection.
- 16Kbyte Instruction and 16Kbyte data caches.
  - Virtually indexed, physically tagged.
  - 4-way associative.
  - Write-through or write-back.
- Nexus Class 3 On-Chip Debug system.
  - Low-cost NanoTrace supported.

4.0.2 Pixel Coprocessor (PICO)

- Coprocessor coupled to the AVR32 CPU Core through the TCB Bus.
  - Coprocessor number one on the TCB bus.
- Three parallel Vector Multiplication Units (VMU) where each unit can:
  - Multiply three pixel components with three coefficients.
  - Add the products from the multiplications together.
  - Accumulate the result or add an offset to the sum of the products.
- Can be used for accelerating:
  - Image Color Space Conversion.
    - Configurable Conversion Coefficients.
    - Supports packed and planar input and output formats.
    - Supports subsampled input color spaces (i.e 4:2:2, 4:2:0).
  - Image filtering/scaling.
    - Configurable Filter Coefficients.
    - Throughput of one sample per cycle for a 9-tap FIR filter.
    - Can use the built-in accumulator to extend the FIR filter to more than 9-taps.
    - Can be used for bilinear/bicubic interpolations.
  - MPEG-4/H.264 Quarter Pixel Motion Compensation.
- Flexible input Pixel Selector.
  - Can operate on numerous different image storage formats.
- Flexible Output Pixel Inserter.
  - Scales and saturates the results back to 8-bit pixel values.
  - Supports packed and planar output formats.

- Configurable coefficients with flexible fixed-point representation.

4.0.3 Debug and Test system

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 3
- Auxiliary port for high-speed trace information
- Hardware support for 6 Program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership, and Watchpoint trace supported

4.0.4 DMA Controller

- 2 HSB Master Interfaces
- 3 Channels
- Software and Hardware Handshaking Interfaces
  - 11 Hardware Handshaking Interfaces
- Memory/Non-Memory Peripherals to Memory/Non-Memory Peripherals Transfer
- Single-block DMA Transfer
- Multi-block DMA Transfer
  - Linked Lists
  - Auto-Reloading
  - Contiguous Blocks
- DMA Controller is Always the Flow Controller
- Additional Features
  - Scatter and Gather Operations
  - Channel Locking
  - Bus Locking
  - FIFO Mode
  - Pseudo Fly-by Operation

4.0.5 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Eighteen channels
  - Two for each USART
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface

4.0.6 Bus system

- HSB bus matrix with 10 Masters and 8 Slaves handled
  - Handles Requests from the CPU Icache, CPU Dcache, HSB bridge, HISI, USB 2.0 Controller, LCD Controller, Ethernet Controller 0, Ethernet Controller 1, DMA Controller 0, DMA Controller 1, and to internal SRAM 0, internal SRAM 1, PB A, PB B, EBI and, USB.

  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
  - One Address Decoder Provided per Master
- 2 Peripheral buses allowing each bus to run on different bus speeds.
  - PB A intended to run on low clock speeds, with peripherals connected to the PDC.
  - PB B intended to run on higher clock speeds, with peripherals connected to the DMACA.
- HSB-HSB Bridge providing a low-speed HSB bus running at the same speed as PBA
  - Allows PDC transfers between a low-speed PB bus and a bus matrix of higher clock speeds

An overview of the bus system is given in Figure 4-1 on page 13. All modules connected to the same bus use the same clock, but the clock to each module can be individually shut off by the Power Manager. The figure identifies the number of master and slave interfaces of each module connected to the HSB bus, and which DMA controller is connected to which peripheral.

5. I/O Line Considerations

5.1 JTAG pins

The TMS, TDI and TCK pins have pull-up resistors. TDO is an output, driven at up to VDDIO, and have no pull-up resistor. The TRST_N pin is used to initialize the embedded JTAG TAP Controller when asserted at a low level. It is a schmitt input and integrates permanent pull-up resistor to VDDIO, so that it can be left unconnected for normal operations.

5.2 WAKE_N pin

The WAKE_N pin is a schmitt trigger input integrating a permanent pull-up resistor to VDDIO.

5.3 RESET_N pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

5.4 EVTI_N pin

The EVTI_N pin is a schmitt input and integrates a non-programmable pull-up resistor to VDDIO.

5.5 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as PIO pins.

5.6 PIO pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, I/O lines default as inputs with pull-up resistors enabled, except when indicated otherwise in the column “Reset State” of the PIO Controller multiplexing tables.

6. AVR32 AP CPU

Rev.: 1.0.0.0

This chapter gives an overview of the AVR32 AP CPU. AVR32 AP is an implementation of the AVR32 architecture. A summary of the programming model, instruction set, caches and MMU is presented. For further details, see the *AVR32 Architecture Manual* and the *AVR32 AP Technical Reference Manual*.

6.1 AVR32 Architecture

AVR32 is a new, high-performance 32-bit RISC microprocessor architecture, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption and high code density. In addition, the instruction set architecture has been tuned to allow a variety of microarchitectures, enabling the AVR32 to be implemented as low-, mid- or high-performance processors. AVR32 extends the AVR family into the world of 32- and 64-bit applications.

Through a quantitative approach, a large set of industry recognized benchmarks has been compiled and analyzed to achieve the best code density in its class. In addition to lowering the memory requirements, a compact code size also contributes to the core's low power characteristics. The processor supports byte and half-word data types without penalty in code size and performance.

Memory load and store operations are provided for byte, half-word, word and double word data with automatic sign- or zero extension of half-word and byte data.

In order to reduce code size to a minimum, some instructions have multiple addressing modes. As an example, instructions with immediates often have a compact format with a smaller immediate, and an extended format with a larger immediate. In this way, the compiler is able to use the format giving the smallest code size.

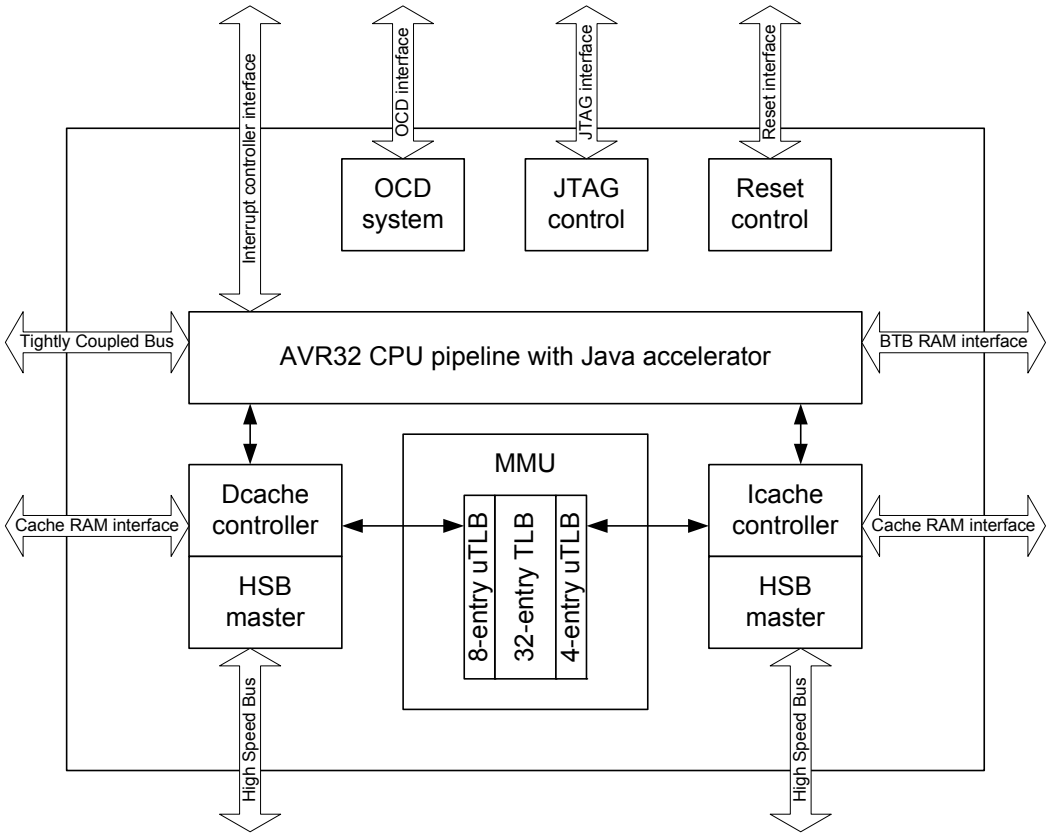
Another feature of the instruction set is that frequently used instructions, like add, have a compact format with two operands as well as an extended format with three operands. The larger format increases performance, allowing an addition and a data move in the same instruction in a single cycle. Load and store instructions have several different formats in order to reduce code size and speed up execution.

The register file is organized as sixteen 32-bit registers and includes the Program Counter, the Link Register, and the Stack Pointer. In addition, register R12 is designed to hold return values from function calls and is used implicitly by some instructions.

6.2 The AVR32 AP CPU

AVR32 AP targets high-performance applications, and provides an advanced OCD system, efficient data and instruction caches, and a full MMU. Figure 6-1 on page 19 displays the contents of AVR32 AP.

Figure 6-1. Overview of the AVR32 AP CPU

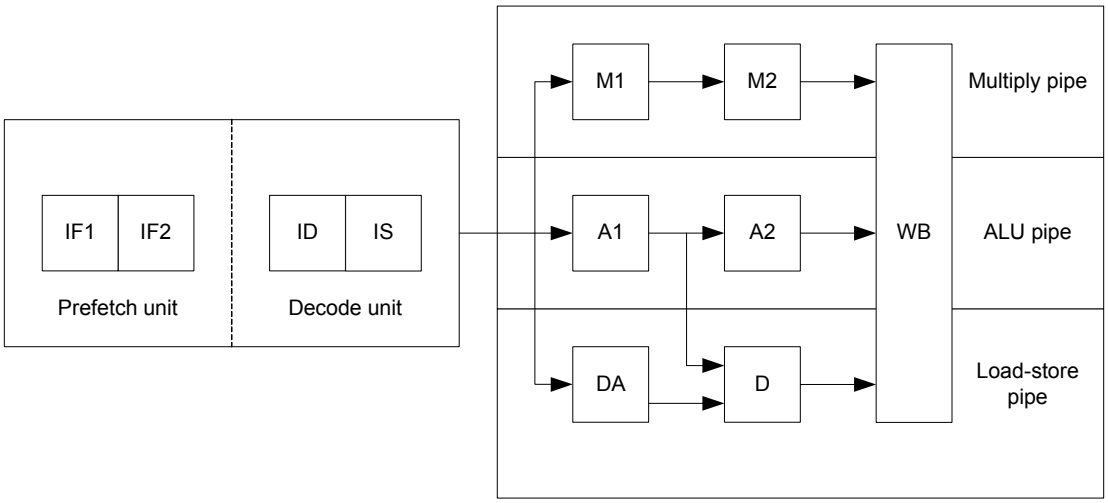


6.2.1 Pipeline Overview

AVR32 AP is a pipelined processor with seven pipeline stages. The pipeline has three subpipes, namely the Multiply pipe, the Execute pipe and the Data pipe. These pipelines may execute different instructions in parallel. Instructions are issued in order, but may complete out of order (OOO) since the subpipes may be stalled individually, and certain operations may use a subpipe for several clock cycles.

Figure 6-2 on page 20 shows an overview of the AVR32 AP pipeline stages.

Figure 6-2. The AVR32 AP Pipeline



.The follwing abbreviations are used in the figure:

- IF1, IF2 - Instruction Fetch stage 1 and 2
- ID - Instruction Decode
- IS - Instruction Issue
- A1, A2 - ALU stage 1 and 2
- M1, M2 - Multiply stage 1 and 2
- DA - Data Address calculation stage
- D - Data cache access
- WB - Writeback

6.2.2 AVR32B Microarchitecture Compliance

AVR32 AP implements an AVR32B microarchitecture. The AVR32B microarchitecture is targeted at applications where interrupt latency is important. The AVR32B therefore implements dedicated registers to hold the status register and return address for interrupts, exceptions and supervisor calls. This information does not need to be written to the stack, and latency is therefore reduced. Additionally, AVR32B allows hardware shadowing of the registers in the register file.

The *scall*, *rete* and *rets* instructions use the dedicated return status registers and return address registers in their operation. No stack accesses are performed by these instructions.

6.2.3 Java Support

AVR32 AP provides Java hardware acceleration in the form of a Java Virtual Machine hardware implementation. Refer to the *AVR32 Java Technical Reference Manual* for details.

6.2.4 Memory management

AVR32 AP implements a full MMU as specified by the AVR32 architecture. The page sizes provided are 1K, 4K, 64K and 1M. A 32-entry fully-associative common TLB is implemented, as well as a 4-entry micro-ITLB and 8-entry micro-DTLB. Instruction and data accesses perform lookups in the micro-TLBs. If the access misses in the micro-TLBs, an access in the common TLB is performed. If this access misses, a page miss exception is issued.

6.2.5 Caches and write buffer

AVR32 AP implements 16K data and 16K instruction caches. The caches are 4-way set associative. Each cache has a 32-bit System Bus master interface connecting it to the bus. The instruction cache has a 32-bit interface to the fetch pipeline stage, and the data cache has a 64-bit interface to the load-store pipeline. The caches use a least recently used allocate-on-read-miss replacement policy. The caches are virtually tagged, physically indexed, avoiding the need to flush them on task switch.

The caches provide locking on a per-line basis, allowing code and data to be permanently locked in the caches for timing-critical code. The data cache also allows prefetching of data using the *pref* instruction.

Accesses to the instruction and data caches are tagged as cacheable or uncacheable on a per-page basis by the MMU. Data cache writes are tagged as write-through or writeback on a per-page basis by the MMU.

The data cache has a 32-byte combining write buffer, to avoid stalling the CPU when writing to external memory. Writes are tagged as bufferable or unbufferable on a per-page basis by the MMU. Bufferable writes to sequential addresses are placed in the buffer, allowing for example a sequence of byte writes from the CPU to be combined into word transfers on the bus. A *sync* instruction is provided to explicitly flush the write buffer.

6.2.6 Unaligned reference handling

AVR32 AP has hardware support for performing unaligned memory accesses. This will reduce the memory footprint needed by some applications, as well as speed up other applications operating on unaligned data.

AVR32 AP is able to perform certain word-sized load and store instructions of any alignment, and word-aligned *st.d* and *ld.d*. Any other unaligned memory access will cause an MMU address exception. All coprocessor memory access instructions require word-aligned pointers. Double-word-sized accesses with word-aligned pointers will automatically be performed as two word-sized accesses.

The following table shows the instructions with support for unaligned addresses. All other instructions require aligned addresses. Accessing an unaligned address may require several clock cycles, refer to the *AVR32 AP Technical Reference Manual* for details.

Table 6-1. Instructions with unaligned reference support

Instruction	Supported alignment
ld.w	Any
st.w	Any
lddsp	Any
lddpc	Any
stdsp	Any
ld.d	Word
st.d	Word
All coprocessor memory access instruction	Word

6.2.7 Unimplemented instructions

The following instructions are unimplemented in AVR32 AP, and will cause an Unimplemented Instruction Exception if executed:

- mems
- memc
- memt

6.2.8 Exceptions and Interrupts

AVR32 AP incorporates a powerful exception handling scheme. The different exception sources, like Illegal Op-code and external interrupt requests, have different priority levels, ensuring a well-defined behavior when multiple exceptions are received simultaneously. Additionally, pending exceptions of a higher priority class may preempt handling of ongoing exceptions of a lower priority class. Each priority class has dedicated registers to keep the return address and status register thereby removing the need to perform time-consuming memory operations to save this information.

There are four levels of external interrupt requests, all executing in their own context. The INT3 context provides dedicated shadow registers ensuring low latency for these interrupts. An interrupt controller does the priority handling of the external interrupts and provides the autovector offset to the CPU.

The addresses and priority of simultaneous events are shown in Table 6-2 on page 23.

Table 6-2. Priority and handler addresses for events

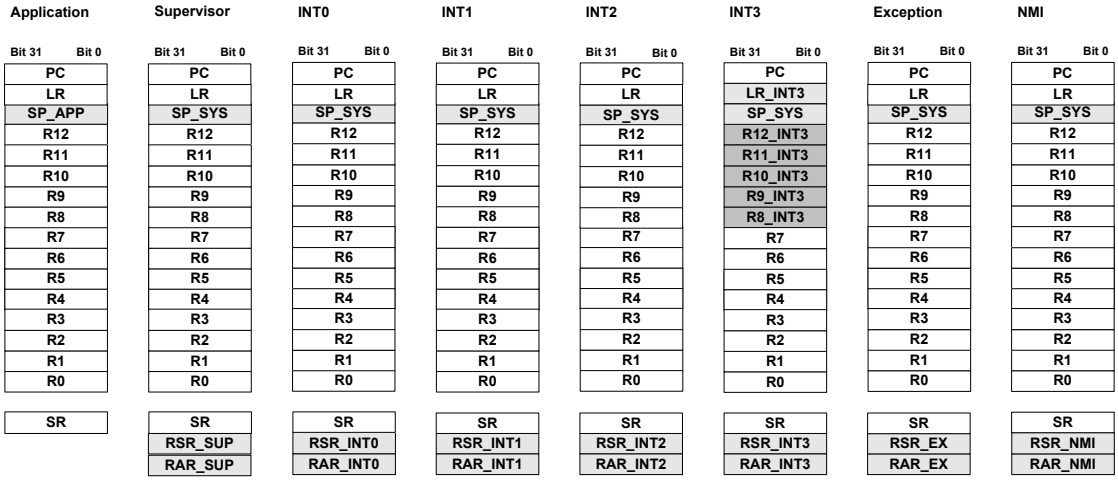
Priority	Handler Address	Name	Event source	Stored Return Address
1	0xA000_0000	Reset	External input	Undefined
2	Provided by OCD system	OCD Stop CPU	OCD system	First non-completed instruction
3	EVBA+0x00	Unrecoverable exception	Internal	PC of offending instruction
4	EVBA+0x04	TLB multiple hit	Internal signal	PC of offending instruction
5	EVBA+0x08	Bus error data fetch	Data bus	First non-completed instruction
6	EVBA+0x0C	Bus error instruction fetch	Data bus	First non-completed instruction
7	EVBA+0x10	NMI	External input	First non-completed instruction
8	Autovectored	Interrupt 3 request	External input	First non-completed instruction
9	Autovectored	Interrupt 2 request	External input	First non-completed instruction
10	Autovectored	Interrupt 1 request	External input	First non-completed instruction
11	Autovectored	Interrupt 0 request	External input	First non-completed instruction
12	EVBA+0x14	Instruction Address	ITLB	PC of offending instruction
13	EVBA+0x50	ITLB Miss	ITLB	PC of offending instruction
14	EVBA+0x18	ITLB Protection	ITLB	PC of offending instruction
15	EVBA+0x1C	Breakpoint	OCD system	First non-completed instruction
16	EVBA+0x20	Illegal Opcode	Instruction	PC of offending instruction
17	EVBA+0x24	Unimplemented instruction	Instruction	PC of offending instruction
18	EVBA+0x28	Privilege violation	Instruction	PC of offending instruction
19	EVBA+0x2C	Floating-point	FP Hardware	PC of offending instruction
20	EVBA+0x30	Coprocessor absent	Instruction	PC of offending instruction
21	EVBA+0x100	Supervisor call	Instruction	PC(Supervisor Call) +2
22	EVBA+0x34	Data Address (Read)	DTLB	PC of offending instruction
23	EVBA+0x38	Data Address (Write)	DTLB	PC of offending instruction
24	EVBA+0x60	DTLB Miss (Read)	DTLB	PC of offending instruction
25	EVBA+0x70	DTLB Miss (Write)	DTLB	PC of offending instruction
26	EVBA+0x3C	DTLB Protection (Read)	DTLB	PC of offending instruction
27	EVBA+0x40	DTLB Protection (Write)	DTLB	PC of offending instruction
28	EVBA+0x44	DTLB Modified	DTLB	PC of offending instruction

6.3 Programming Model

6.3.1 Register file configuration

The AVR32B architecture specifies that the exception contexts may have a different number of shadowed registers in different implementations. Figure 6-3 on page 24 shows the model used in AVR32 AP.

Figure 6-3. The AVR32 AP Register File



6.3.2 Status register configuration

The Status Register (SR) is splitted into two halfwords, one upper and one lower, see Figure 6-4 on page 24 and Figure 6-5 on page 25. The lower word contains the C, Z, N, V and Q condition code flags and the R, T and L bits, while the upper halfword contains information about the mode and state the processor executes in. Refer to the *AVR32 Architecture Manual* for details.

Figure 6-4. The Status Register High Halfword

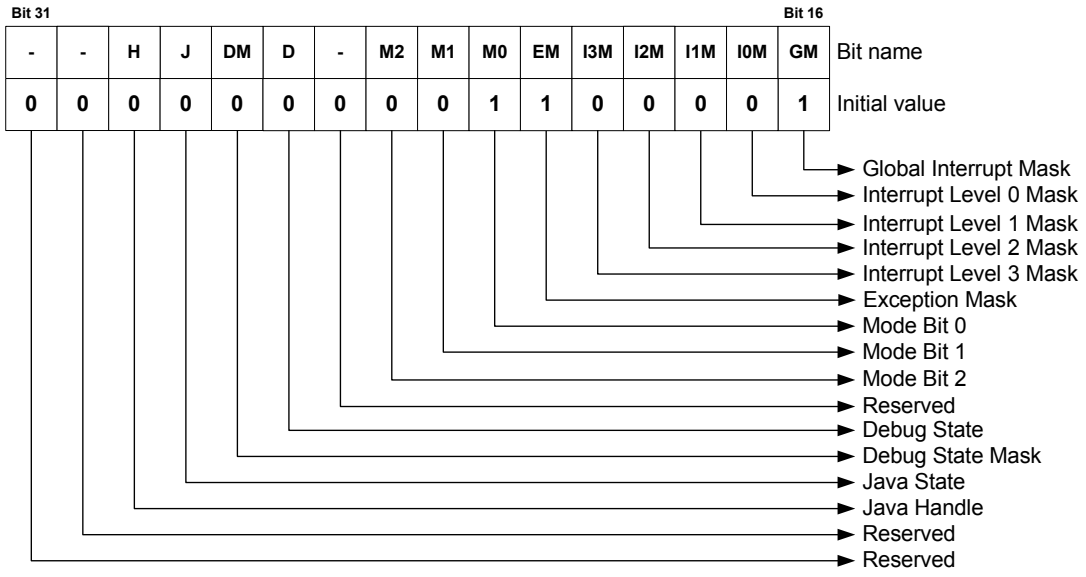
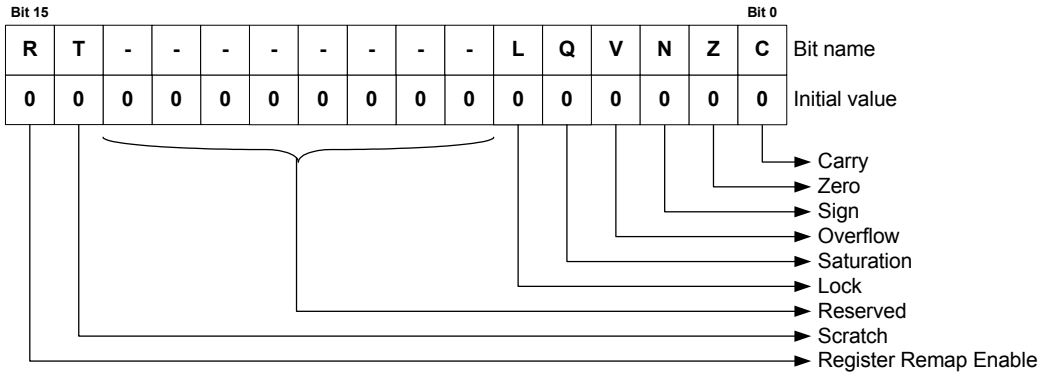


Figure 6-5. The Status Register Low Halfword



6.3.3 Processor States

6.3.3.1 Normal RISC State

The AVR32 processor supports several different execution contexts as shown in Table 6-3 on page 25.

Table 6-3. Overview of execution modes, their priorities and privilege levels.

Priority	Mode	Security	Description
1	Non Maskable Interrupt	Privileged	Non Maskable high priority interrupt mode
2	Exception	Privileged	Execute exceptions
3	Interrupt 3	Privileged	General purpose interrupt mode
4	Interrupt 2	Privileged	General purpose interrupt mode
5	Interrupt 1	Privileged	General purpose interrupt mode
6	Interrupt 0	Privileged	General purpose interrupt mode
N/A	Supervisor	Privileged	Runs supervisor calls
N/A	Application	Unprivileged	Normal program execution mode

Mode changes can be made under software control, or can be caused by external interrupts or exception processing. A mode can be interrupted by a higher priority mode, but never by one with lower priority. Nested exceptions can be supported with a minimal software overhead.

When running an operating system on the AVR32, user processes will typically execute in the application mode. The programs executed in this mode are restricted from executing certain instructions. Furthermore, most system registers together with the upper halfword of the status register cannot be accessed. Protected memory areas are also not available. All other operating modes are privileged and are collectively called System Modes. They have full access to all privileged and unprivileged resources. After a reset, the processor will be in supervisor mode.

6.3.3.2 Debug State

The AVR32 can be set in a debug state, which allows implementation of software monitor routines that can read out and alter system information for use during application development. This implies that all system and application registers, including the status registers and program counters, are accessible in debug state. The privileged instructions are also available.

All interrupt levels are by default disabled when debug state is entered, but they can individually be switched on by the monitor routine by clearing the respective mask bit in the status register.

Debug state can be entered as described in the *AVR32 AP Technical Reference Manual*.

Debug state is exited by the *retd* instruction.

6.3.3.3 Java State

AVR32 AP implements a Java Extension Module (JEM). The processor can be set in a Java State where normal RISC operations are suspended. Refer to the *AVR32 Java Technical Reference Manual* for details.

7. Pixel Coprocessor (PICO)

Rev.: 1.0.0.0

7.1 Features

- Coprocessor coupled to the AVR32 CPU Core through the TCB Bus.
- Three parallel Vector Multiplication Units (VMU) where each unit can:
  - Multiply three pixel components with three coefficients.
  - Add the products from the multiplications together.
  - Accumulate the result or add an offset to the sum of the products.
- Can be used for accelerating:
  - Image Color Space Conversion.
    - Configurable Conversion Coefficients.
    - Supports packed and planar input and output formats.
    - Supports subsampled input color spaces (i.e 4:2:2, 4:2:0).
  - Image filtering/scaling.
    - Configurable Filter Coefficients.
    - Throughput of one sample per cycle for a 9-tap FIR filter.
    - Can use the built-in accumulator to extend the FIR filter to more than 9-taps.
    - Can be used for bilinear/bicubic interpolations.
  - MPEG-4/H.264 Quarter Pixel Motion Compensation.
- Flexible input Pixel Selector.
  - Can operate on numerous different image storage formats.
- Flexible Output Pixel Inserter.
  - Scales and saturates the results back to 8-bit pixel values.
  - Supports packed and planar output formats.
- Configurable coefficients with flexible fixed-point representation.

7.2 Description

The Pixel Coprocessor (PICO) is a coprocessor coupled to the AVR32 CPU through the TCB (Tightly Coupled Bus) interface. The PICO consists of three Vector Multiplication Units (VMU0, VMU1, VMU2), an Input Pixel Selector and an Output Pixel Inserter. Each VMU can perform a vector multiplication of a 1x3 12-bit coefficient vector with a 3x1 8-bit pixel vector. In addition a 12-bit offset can be added to the result of this vector multiplication.

The PICO can be used for transforming the pixel components in a given color space (i.e. RGB, YCrCb, YUV) to any other color space as long as the transformation is linear. The flexibility of the Input Pixel Selector and Output Pixel Insertion logic makes it easy to efficiently support different pixel storage formats with regards to issues such as byte ordering of the color components, if the color components constituting an image are packed/interleaved or stored as separate images or if any of the color components are subsampled.

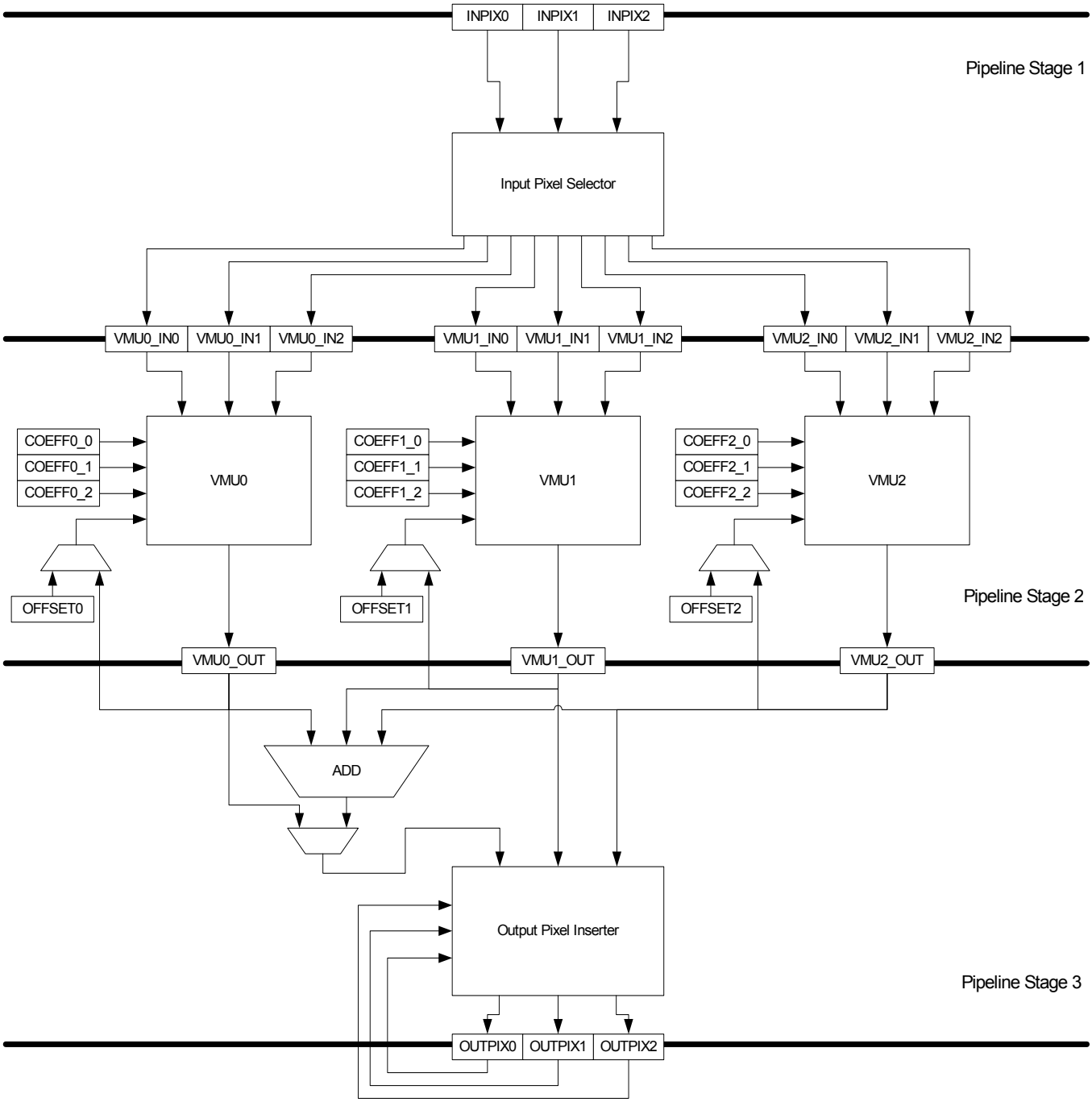
The three Vector Multiplication Units can also be connected together to form one large vector multiplier which can perform a vector multiplication of a 1x9 12-bit coefficient vector with a 9x1 8-bit pixel vector. This can be used to implement FIR filters, bilinear interpolations filters for smoothing/scaling images etc. By allowing the outputs from the Vector Multiplication units to accumulate it is also possible to extend the order of the filter to more than 9-taps.

The results from the VMUs are scaled and saturated back to unsigned 8-bit pixel values in the Output Pixel Inserter.

The PICO is divided into three pipeline stages with a throughput of one operation per cpu clock cycle.

7.3 Block Diagram

Figure 7-1. Pixel Coprocessor Block Diagram

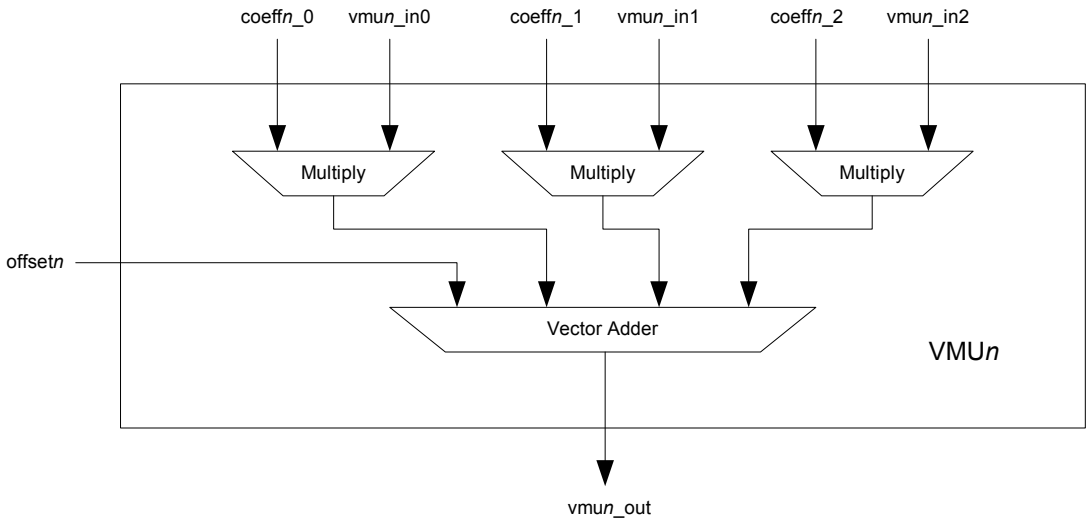


7.4 Vector Multiplication Unit (VMU)

Each VMU consists of three multipliers used for multiplying unsigned 8-bit pixel components with signed 12-bit coefficients.The result from each multiplication is a 20-bit signed number that is input to a 22-bit vector adder along with an offset as shown in Figure 7-2 on page 29. The operation is equal to the offsetted vector multiplication given in the following equation:

$$\text{vmu_out} = \begin{bmatrix}\text{coeff0} & \text{coeff1} & \text{coeff2}\end{bmatrix}\begin{bmatrix}\text{vmu_in0}\\ \text{vmu_in1}\\ \text{vmu_in2}\end{bmatrix} + \text{offset}$$

Figure 7-2. Inside VMU*n* ($n \in \{0,1,2\}$)



7.5 Input Pixel Selector

The Input Pixel Selector uses the ISM (Input Selection Mode) field in the CONFIG register and the three input pixel source addresses given in the PICO operation instructions to decide which pixels to select for inputs to the VMUs.

7.5.1 Transformation Mode

When the Input Selection Mode is set to Transformation Mode the input pixel source addresses INx, INy and INz directly maps to three pixels in the INPIX*n* registers. These three pixels are then input to each of the VMUs. The following expression then represents what is computed by the VMUs in Transformation Mode:

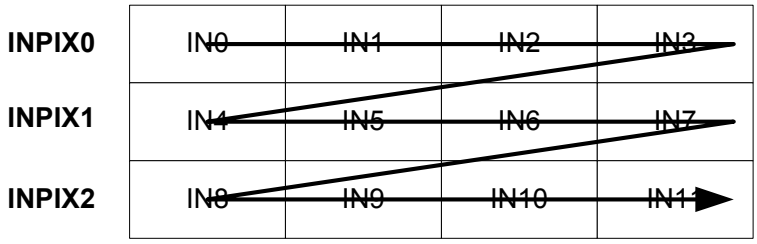
$$\begin{bmatrix}\text{VMU0_OUT}\\ \text{VMU1_OUT}\\ \text{VMU2_OUT}\end{bmatrix} = \begin{bmatrix}\text{COEFF0_0} & \text{COEFF0_1} & \text{COEFF0_2}\\ \text{COEFF1_0} & \text{COEFF1_1} & \text{COEFF1_2}\\ \text{COEFF2_0} & \text{COEFF2_1} & \text{COEFF2_2}\end{bmatrix}\begin{bmatrix}\text{INx}\\ \text{INy}\\ \text{INz}\end{bmatrix} + \begin{bmatrix}\text{OFFSET0 or VMU0_OUT}\\ \text{OFFSET1 or VMU1_OUT}\\ \text{OFFSET2 or VMU2_OUT}\end{bmatrix}$$

7.5.2 Horizontal Filter Mode

In Horizontal Filter Mode the input pixel source addresses INx, INy and INz represents the base pixel address of a pixel triplet. The pixel triplet {IN(x), IN(x+1), IN(x+2)} is input to VMU0, the pixel triplet {IN(y), IN(y+1), IN(y+2)} is input to VMU1 and the pixel triplet {IN(z), IN(z+1), IN(z+2)}

is input to VMU2. Figure 7-3 on page 30 shows how the pixel triplet is found by taking the pixel addressed by the base address and following the arrow to find the next two pixels which makes up the triplet.

Figure 7-3. Horizontal Filter Mode Pixel Addressing



The following expression represents what is computed by the VMUs in Horizontal Filter Mode:

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN(x+0) \\ IN(x+1) \\ IN(x+2) \end{bmatrix} + (OFFSET0 \text{ or } VMU0_OUT)$$

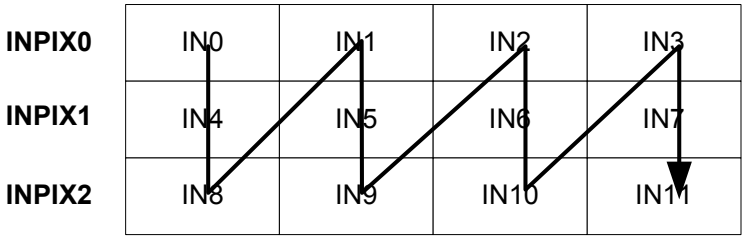
$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN(y+0) \\ IN(y+1) \\ IN(y+2) \end{bmatrix} + (OFFSET1 \text{ or } VMU1_OUT)$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN(z+0) \\ IN(z+1) \\ IN(z+2) \end{bmatrix} + (OFFSET2 \text{ or } VMU2_OUT)$$

7.5.3 Vertical Filter Mode

In Vertical Filter Mode the input pixel source addresses INx, INy and INz represent the base of a pixel triplet found by following the vertical arrow shown in Figure 7-4 on page 30. The pixel triplet {IN(x), IN((x+4)%11), IN((x+8)%11)} is input to VMU0, the pixel triplet {IN(y), IN((y+4)%11), IN((y+8)%11)} is input to VMU1 and the pixel triplet {IN(z), IN((z+4)%11), IN((z+8)%11)} is input to VMU2.

Figure 7-4. Vertical Filter Mode Pixel Addressing



The following expression represents what is computed by the VMUs in Vertical Filter Mode:

$$VMU0_OUT = \left[COEFF0_0\ COEFF0_1\ COEFF0_2\right]\begin{bmatrix} IN((x+0)\%11) \\ IN((x+4)\%11) \\ IN((x+8)\%11) \end{bmatrix} + (OFFSET0 \text{ or } VMU0_OUT)$$

$$VMU1_OUT = \left[COEFF1_0\ COEFF1_1\ COEFF1_2\right]\begin{bmatrix} IN((y+0)\%11) \\ IN((y+4)\%11) \\ IN((y+8)\%11) \end{bmatrix} + (OFFSET1 \text{ or } VMU1_OUT)$$

$$VMU2_OUT = \left[COEFF2_0\ COEFF2_1\ COEFF2_2\right]\begin{bmatrix} IN((z+0)\%11) \\ IN((z+4)\%11) \\ IN((z+8)\%11) \end{bmatrix} + (OFFSET2 \text{ or } VMU2_OUT)$$

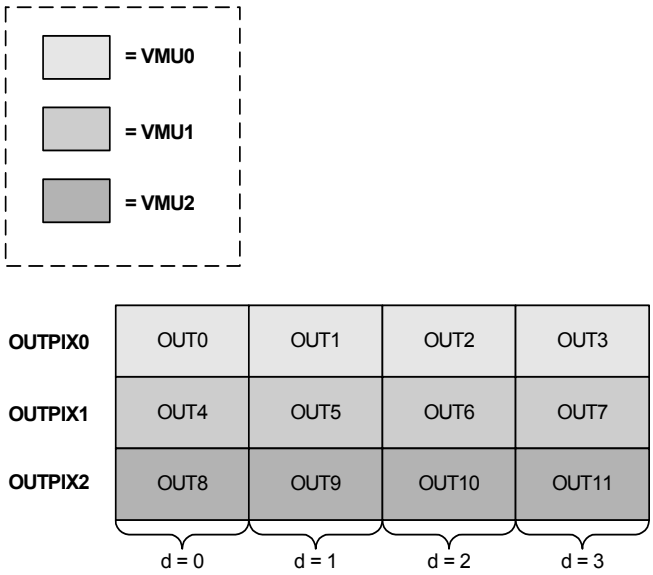
7.6 Output Pixel Inserter

The Output Pixel Inserter uses the OIM (Output Insertion Mode) field in the CONFIG register and the destination pixel address given in the PICO operation instructions to decide which three of the twelve possible OUT*n* pixels to write back the scaled and saturated results from the VMUs to. The 22-bit results from each VMU is first scaled by performing an arithmetical right shift by COEFF_FRAC_BITS in order to remove the fractional part of the results and obtain the integer part. The integer part is then saturated to an unsigned 8-bit number in the range 0 to 255.

7.6.1 Planar Insertion Mode

In Planar Insertion Mode the destination pixel address OUTd specifies which pixel in each of the registers OUTPIX0, OUTPIX1 and OUTPIX2 will be updated. VMU*n* writes to OUTPIX*n*. This can be seen in *Figure 7-5 on page 31* and *Table 7-2 on page 49*. This mode is useful when transforming from one color space to another where the resulting color components should be stored in separate images.

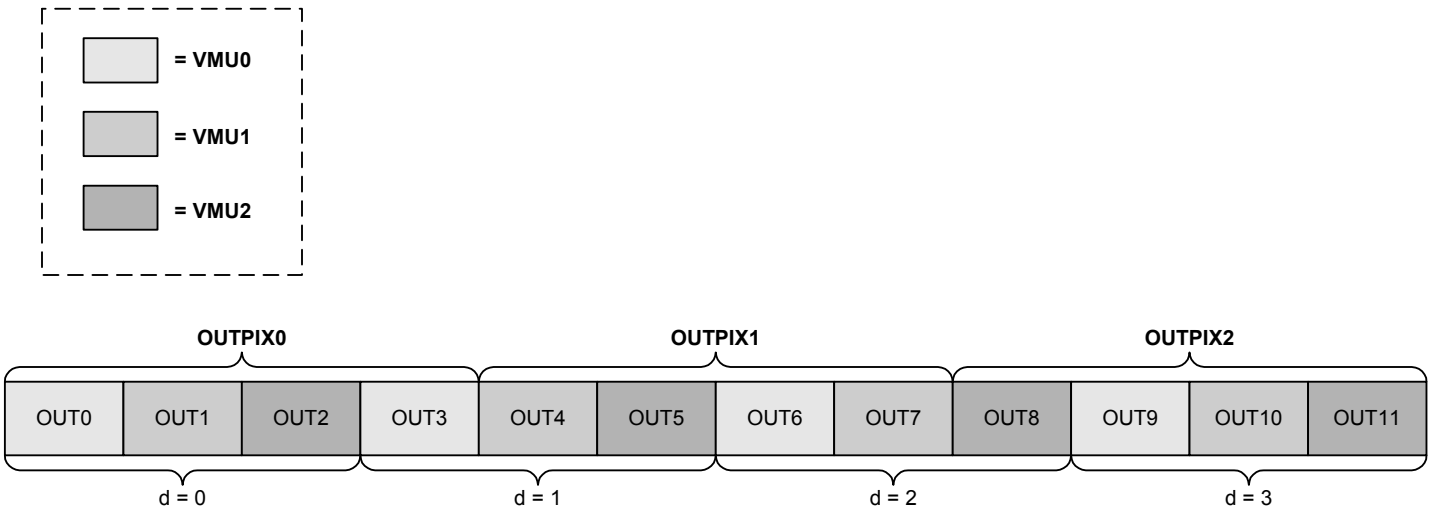
Figure 7-5. Planar Pixel Insertion



7.6.2 Packed Insertion Mode

In Packed Insertion Mode the three output registers OUTPIX0, OUTPIX1 and OUTPIX2 are divided into four pixel triplets as seen in Figure 7-6 on page 32 and Table 7-2 on page 49. The destination pixel address is then the address of the pixel triplet. VMU*n* writes to pixel *n* of the pixel triplet.This mode is useful when transforming from one color space to another where the resulting color components should be packed together.

Figure 7-6. Packed Pixel Insertion.



7.7 User Interface

The PICO uses the TCB interface to communicate with the CPU and the user can read from or write to the PICO Register File by using the PICO load/store/move instructions which maps to generic coprocessor instructions.

7.7.1 Register File

The PICO register file can be accessed from the CPU by using the *picomv.x, picold.x, picost.x, picoldm and picostm* instructions.

Table 7-1. PICO Register File

Cp Reg #	Register	Name	Access
cr0	Input Pixel Register 2	INPIX2	Read/Write
cr1	Input Pixel Register 1	INPIX1	Read/Write
cr2	Input Pixel Register 0	INPIX0	Read/Write
cr3	Output Pixel Register 2	OUTPIX2	Read Only
cr4	Output Pixel Register 1	OUTPIX1	Read Only
cr5	Output Pixel Register 0	OUTPIX0	Read Only
cr6	Coefficient Register A for VMU0	COEFF0_A	Read/Write
cr7	Coefficient Register B for VMU0	COEFF0_B	Read/Write
cr8	Coefficient Register A for VMU1	COEFF1_A	Read/Write
cr9	Coefficient Register B for VMU1	COEFF1_B	Read/Write
cr10	Coefficient Register A for VMU2	COEFF2_A	Read/Write
cr11	Coefficient Register B for VMU2	COEFF2_B	Read/Write
cr12	Output from VMU0	VMU0_OUT	Read/Write
cr13	Output from VMU1	VMU1_OUT	Read/Write
cr14	Output from VMU2	VMU2_OUT	Read/Write
cr15	PICO Configuration Register	CONFIG	Read/Write

7.7.1.1 Input Pixel Register 0

Register Name: INPIX0

Access Type: Read/Write

31	30	29	28	27	26	25	24
IN0							
23	22	21	20	19	18	17	16
IN1							
15	14	13	12	11	10	9	8
IN2							
7	6	5	4	3	2	1	0
IN3							

- **IN0: Input Pixel 0**

Input Pixel number 0 to the Input Pixel Selector Unit.

- **IN1: Input Pixel 1**

Input Pixel number 1 to the Input Pixel Selector Unit.

- **IN2: Input Pixel 2**

Input Pixel number 2 to the Input Pixel Selector Unit.

- **IN3: Input Pixel 3**

Input Pixel number 3 to the Input Pixel Selector Unit.

7.7.1.2 Input Pixel Register 1

Register Name: INPIX1

Access Type: Read/Write

31	30	29	28	27	26	25	24
IN4							
23	22	21	20	19	18	17	16
IN5							
15	14	13	12	11	10	9	8
IN6							
7	6	5	4	3	2	1	0
IN7							

- **IN0: Input Pixel 4**

Input Pixel number 4 to the Input Pixel Selector Unit.

- **IN1: Input Pixel 5**

Input Pixel number 5 to the Input Pixel Selector Unit.

- **IN2: Input Pixel 6**

Input Pixel number 6 to the Input Pixel Selector Unit.

- **IN3: Input Pixel 7**

Input Pixel number 7 to the Input Pixel Selector Unit.

7.7.1.3 Input Pixel Register 2

Register Name: INPIX2

Access Type: Read/Write

31	30	29	28	27	26	25	24
IN8							
23	22	21	20	19	18	17	16
IN9							
15	14	13	12	11	10	9	8
IN10							
7	6	5	4	3	2	1	0
IN11							

- **IN0: Input Pixel 8**

Input Pixel number 8 to the Input Pixel Selector Unit.

- **IN1: Input Pixel 9**

Input Pixel number 9 to the Input Pixel Selector Unit.

- **IN2: Input Pixel 10**

Input Pixel number 10 to the Input Pixel Selector Unit.

- **IN3: Input Pixel 11**

Input Pixel number 11 to the Input Pixel Selector Unit.

7.7.1.4 *Output Pixel Register 0*

Register Name: OUTPIX0

Access Type: Read

31	30	29	28	27	26	25	24
OUT0							
23	22	21	20	19	18	17	16
OUT1							
15	14	13	12	11	10	9	8
OUT2							
7	6	5	4	3	2	1	0
OUT3							

- **OUT0: Output Pixel 0**

Output Pixel number 0 from the Output Pixel Inserter Unit.

- **OUT1: Output Pixel 1**

Output Pixel number 1 from the Output Pixel Inserter Unit.

- **OUT2: Output Pixel 2**

Output Pixel number 2 from the Output Pixel Inserter Unit.

- **OUT3: Output Pixel 3**

Output Pixel number 3 from the Output Pixel Inserter Unit.

7.7.1.5 Output Pixel Register 1

Register Name: OUTPIX1

Access Type: Read

31	30	29	28	27	26	25	24
OUT4							
23	22	21	20	19	18	17	16
OUT5							
15	14	13	12	11	10	9	8
OUT6							
7	6	5	4	3	2	1	0
OUT7							

- **OUT4: Output Pixel 4**

Output Pixel number 4 from the Output Pixel Inserter Unit.

- **OUT5: Output Pixel 5**

Output Pixel number 5 from the Output Pixel Inserter Unit.

- **OUT6: Output Pixel 6**

Output Pixel number 6 from the Output Pixel Inserter Unit.

- **OUT7: Output Pixel 7**

Output Pixel number 7 from the Output Pixel Inserter Unit.

7.7.1.6 Output Pixel Register 2

Register Name: OUTPIX2

Access Type: Read

31	30	29	28	27	26	25	24
OUT8							
23	22	21	20	19	18	17	16
OUT9							
15	14	13	12	11	10	9	8
OUT10							
7	6	5	4	3	2	1	0
OUT11							

- **OUT8: Output Pixel 8**

Output Pixel number 8 from the Output Pixel Inserter Unit.

- **OUT9: Output Pixel 9**

Output Pixel number 9 from the Output Pixel Inserter Unit.

- **OUT10: Output Pixel 10**

Output Pixel number 10 from the Output Pixel Inserter Unit.

- **OUT11: Output Pixel 11**

Output Pixel number 11 from the Output Pixel Inserter Unit.

7.7.1.7 Coefficient Register A for VMU0

Register Name: COEFF0_A

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	COEFF0_0			
23	22	21	20	19	18	17	16
COEFF0_0							
15	14	13	12	11	10	9	8
-	-	-	-	COEFF0_1			
7	6	5	4	3	2	1	0
COEFF0_1							

- **COEFF0_0: Coefficient 0 for VMU0**

Coefficient 0 input to VMU0. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF0_0 / 2^{COEFF_FRAC_BITS}$, where the COEFF0_0 value is interpreted as a 2's complement integer. When reading this register, COEFF0_0 is sign-extended to 16-bits in order to fill in the unused bits in the upper halfword of this register.

- **COEFF0_1: Coefficient 1 for VMU0**

Coefficient 1 input to VMU0. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF0_1 / 2^{COEFF_FRAC_BITS}$, where the COEFF0_1 value is interpreted as a 2's complement integer. When reading this register, COEFF0_1 is sign-extended to 16-bits in order to fill in the unused bits in the lower halfword of this register.

7.7.1.8 Coefficient Register B for VMU0

Register Name: COEFF0_B

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	COEFF0_2			
23	22	21	20	19	18	17	16
COEFF0_2							
15	14	13	12	11	10	9	8
-	-	-	-	OFFSET0			
7	6	5	4	3	2	1	0
OFFSET0							

- **COEFF0_2: Coefficient 2 for VMU0**

Coefficient 2 input to VMU0. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF0_2 / 2^{COEFF_FRAC_BITS}$, where the COEFF0_2 value is interpreted as a 2's complement integer. When reading this register, COEFF0_2 is sign-extended to 16-bits in order to fill in the unused bits in the upper halfword of this register.

- **OFFSET0: Offset for VMU0**

Offset input to VMU0 in case of non-accumulating operations. A signed 12-bit fixed-point number where the number of fractional bits is given by the OFFSET_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $OFFSET0 / 2^{OFFSET_FRAC_BITS}$, where the OFFSET0 value is interpreted as a 2's complement integer. When reading this register, OFFSET0 is sign-extended to 16-bits in order to fill in the unused bits in the lower halfword of this register.

7.7.1.9 Coefficient Register A for VMU1

Register Name: COEFF1_A

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	COEFF1_0			
23	22	21	20	19	18	17	16
COEFF1_0							
15	14	13	12	11	10	9	8
-	-	-	-	COEFF1_1			
7	6	5	4	3	2	1	0
COEFF1_1							

- **COEFF1_0: Coefficient 0 for VMU1**

Coefficient 0 input to VMU1. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF1_0 / 2^{COEFF_FRAC_BITS}$, where the COEFF1_0 value is interpreted as a 2's complement integer. When reading this register, COEFF1_0 is sign-extended to 16-bits in order to fill in the unused bits in the upper halfword of this register.

- **COEFF1_1: Coefficient 1 for VMU1**

Coefficient 1 input to VMU0. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF1_1 / 2^{COEFF_FRAC_BITS}$, where the COEFF1_1 value is interpreted as a 2's complement integer. When reading this register, COEFF1_1 is sign-extended to 16-bits in order to fill in the unused bits in the lower halfword of this register.

7.7.1.10 Coefficient Register B for VMU1

Register Name: COEFF1_B

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	COEFF1_2			
23	22	21	20	19	18	17	16
COEFF1_2							
15	14	13	12	11	10	9	8
-	-	-	-	OFFSET1			
7	6	5	4	3	2	1	0
OFFSET1							

- **COEFF1_2: Coefficient 2 for VMU1**

Coefficient 2 input to VMU1. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF1_2 / 2^{COEFF_FRAC_BITS}$, where the COEFF1_2 value is interpreted as a 2's complement integer. When reading this register, COEFF1_2 is sign-extended to 16-bits in order to fill in the unused bits in the upper halfword of this register.

- **OFFSET1: Offset for VMU1**

Offset input to VMU1 in case of non-accumulating operations. A signed 12-bit fixed-point number where the number of fractional bits is given by the OFFSET_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $OFFSET1 / 2^{OFFSET_FRAC_BITS}$, where the OFFSET1 value is interpreted as a 2's complement integer. When reading this register, OFFSET1 is sign-extended to 16-bits in order to fill in the unused bits in the lower halfword of this register.

7.7.1.11 Coefficient Register A for VMU2

Register Name: COEFF2_A

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	COEFF2_0			
23	22	21	20	19	18	17	16
COEFF2_0							
15	14	13	12	11	10	9	8
-	-	-	-	COEFF2_1			
7	6	5	4	3	2	1	0
COEFF2_1							

- **COEFF2_0: Coefficient 0 for VMU2**

Coefficient 0 input to VMU2. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF2_0 / 2^{COEFF_FRAC_BITS}$, where the COEFF2_0 value is interpreted as a 2's complement integer. When reading this register, COEFF2_0 is sign-extended to 16-bits in order to fill in the unused bits in the upper halfword of this register.

- **COEFF2_1: Coefficient 1 for VMU2**

Coefficient 1 input to VMU2. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF2_1 / 2^{COEFF_FRAC_BITS}$, where the COEFF2_1 value is interpreted as a 2's complement integer. When reading this register, COEFF2_1 is sign-extended to 16-bits in order to fill in the unused bits in the lower halfword of this register.

7.7.1.12 Coefficient Register B for VMU2

Register Name: COEFF2_B

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	COEFF2_2			
23	22	21	20	19	18	17	16
COEFF2_2							
15	14	13	12	11	10	9	8
-	-	-	-	OFFSET2			
7	6	5	4	3	2	1	0
OFFSET2							

- **COEFF2_2: Coefficient 2 for VMU2**

Coefficient 2 input to VMU2. A signed 12-bit fixed-point number where the number of fractional bits is given by the COEFF_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $COEFF2_2 / 2^{COEFF_FRAC_BITS}$, where the COEFF2_2 value is interpreted as a 2's complement integer. When reading this register, COEFF2_2 is sign-extended to 16-bits in order to fill in the unused bits in the upper halfword of this register.

- **OFFSET2: Offset for VMU2**

Offset input to VMU2 in case of non-accumulating operations. A signed 12-bit fixed-point number where the number of fractional bits is given by the OFFSET_FRAC_BITS field in the CONFIG register. The actual fractional number is equal to $OFFSET2 / 2^{OFFSET_FRAC_BITS}$, where the OFFSET2 value is interpreted as a 2's complement integer. When reading this register, OFFSET2 is sign-extended to 16-bits in order to fill in the unused bits in the lower halfword of this register.

7.7.1.13 VMU0 Output Register

Register Name: VMU0_OUT

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	VMU0_OUT					
15	14	13	12	11	10	9	8
VMU0_OUT							
7	6	5	4	3	2	1	0
VMU0_OUT							

- **VMU0_OUT: Output from VMU0**

This register is used for directly accessing the output from VMU0 or for setting the initial value of the accumulator for accumulating operations. The output from VMU0 is a signed 22-bit fixed-point number where the number of fractional bits are given by the COEFF_FRAC_BITS field in the CONFIG register. When reading this register the signed 22-bit value is sign-extended to 32-bits.

7.7.1.14 VMU1 Output Register

Register Name: VMU1_OUT

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	VMU1_OUT					
15	14	13	12	11	10	9	8
VMU1_OUT							
7	6	5	4	3	2	1	0
VMU1_OUT							

- **VMU1_OUT: Output from VMU1**

This register is used for directly accessing the output from VMU1 or for setting the initial value of the accumulator for accumulating operations. The output from VMU1 is a signed 22-bit fixed-point number where the number of fractional bits are given by the COEFF_FRAC_BITS field in the CONFIG register. When reading this register the signed 22-bit value is sign-extended to 32-bits.

7.7.1.15 VMU2 Output Register

Register Name: VMU2_OUT

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	VMU2_OUT					
15	14	13	12	11	10	9	8
VMU2_OUT							
7	6	5	4	3	2	1	0
VMU2_OUT							

- **VMU2_OUT: Output from VMU2**

This register is used for directly accessing the output from VMU2 or for setting the initial value of the accumulator for accumulating operations. The output from VMU2 is a signed 22-bit fixed-point number where the number of fractional bits are given by the COEFF_FRAC_BITS field in the CONFIG register. When reading this register the signed 22-bit value is sign-extended to 32-bits.

7.7.1.16 PICO Configuration Register

Register Name: CONFIG

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	OIM	ISM	

7	6	5	4	3	2	1	0
OFFSET_FRAC_BITS				COEFF_FRAC_BITS			

- **OIM: Output Insertion Mode**

The OIM bit specifies the semantics of the OUTd output pixel address parameter to the *pico(s)v(mul/mac)* instructions. The OIM together with the output pixel address parameter specify which of the 12 output bytes (OUT*n*) of the OUTPIX*n* registers will be updated with the results from the VMUs. Table 7-2 on page 49 describes the different Output Insertion Modes. See Section 7.6 "Output Pixel Inserter" on page 31 for a description of the Output Pixel Inserter.

Table 7-2. Output Insertion Modes

OIM	Mode	Description
0	Packed Insertion Mode	{OUTPIX0, OUTPIX1, OUTPIX2} is treated as one large register containing 4 sequential 24-bit pixel triplets. The DST_ADR field specifies which of the sequential triplets will be updated. *OUT(d*3 + 0) ← Scaled and saturated output from VMU0* *OUT(d*3 + 1) ← Scaled and saturated output from VMU1* *OUT(d*3 + 2) ← Scaled and saturated output from VMU2*
1	Planar Insertion Mode	Each of the OUTPIX*n* registers will get one of the resulting pixels. The triplet address specifies what byte in each of the OUTPIX*n* registers the results will be written to. *OUT(d + 0) ← Scaled and saturated output from VMU0* *OUT(d+ 4) ← Scaled and saturated output from VMU1* *OUT(d + 8) ← Scaled and saturated output from VMU2*

- **ISM: Input Selection Mode**

The ISM field specifies the semantics of the input pixel address parameters INx, INy and INz to the *pico(s)v(mul/mac)* instructions. Together with the three input pixel addresses the ISM field specifies to the Input Pixel Selector which of the input pixels (IN*n*) that should be selected as inputs to the VMUs.Table 7-3 on page 50 describes the

different Input Selection Modes. See Section 7.5 ”Input Pixel Selector” on page 29 for a description of the Input Pixel

Table 7-3. Input Selection Modes

ISM		Mode	
0	0	Transformation Mode	VMU0, VMU1 and VMU2 get the same pixel inputs. These three pixels can be freely selected from the INPIX*n* registers.
0	1	Horizontal Filter Mode	Pixel triplets are selected for input to each of the VMUs by addressing horizontal pixel triplets from the INPIX*n* registers.
1	0	Vertical Filter Mode	Pixel triplets are selected for input to each of the VMUs by addressing vertical pixel triplets from the INPIX*n* registers.
1	1	Reserved	N.A

Selector.

- **OFFSET_FRAC_BITS: Offset Fractional Bits**

Specifies the number of fractional bits in the fixed-point offsets input to each VMU. Must be in the range from 0 to COEFF_FRAC_BITS. Other values gives undefined results.This value is used for scaling the OFFSET*n* values before being input to VMU*n* so that the offset will have the same fixed-point format as the outputs from the multiplication stages before performing the vector addition in the VMU.

- **COEFF_FRAC_BITS: Coefficient Fractional Bits**

Specifies the number of fractional bits in the fixed-point coefficients input to each VMU. Must be in the range from 0 to 11, since at least one bit of the coefficient must be used for the sign. Other values gives undefined results. COEFF_FRAC_BITS is used in the Output Pixel Inserter to scale the fixed-point results from the VMUs back to unsigned 8-bit integers.

7.8 PICO Instructions

7.8.1 PICO Instructions Nomenclature

7.8.1.1 Registers and Operands

R{d, s, …}	The uppercase '**R**' denotes a 32-bit (word) register.
R**d**	The lowercase '**d**' denotes the *destination* register number.
R**s**	The lowercase '**s**' denotes the *source* register number.
R**b**	The lowercase '**b**' denotes the *base* register number for indexed addressing modes.
R**i**	The lowercase '**i**' denotes the *index* register number for indexed addressing modes.
R**p**	The lowercase '**p**' denotes the *pointer* register number.
IN{x, y, z}	The uppercase '**IN**' denotes a pixel in the INPIX*n* registers.
IN**x**	The lowercase '**x**' denotes the first input pixel number for the PICO operation instructions.
IN**y**	The lowercase '**y**' denotes the second input pixel number for the PICO operation instructions.
IN**z**	The lowercase '**z**' denotes the third input pixel number for the PICO operation instructions.
OUTd	The uppercase '**OUT**' denotes a pixel in the OUTPIX*n* registers.
OUT**d**	The lowercase '**d**' denotes the destination pixel number for the PICO operation instructions.
Pr	PICO register. See **Section 7.7.1 "Register File" on page 33** for a complete list of registers.
PrHi:PrLo	PICO register pair. Only register pairs corresponding to valid coprocessor double registers are valid. E.g. INPIX1:INPIX2 (cr1:cr0). The low part must correspond to an even coprocessor register number *n* and the high part must then correspond to coprocessor register *n+1*. See Table 7-1 on page 33 for a mapping between PICO register names and coprocessor register numbers.
PC	Program Counter, equal to R15
LR	Link Register, equal to R14
SP	Stack Pointer, equal to R13
PICORegList	Register List used in the *picoldm* and *picostm* instructions. See instruction description for which register combinations are allowed in the register list.
disp	Displacement
sa	Shift amount
[i]	Denotes bit **i** in a immediate value. Example: imm6[4] denotes bit 4 in an 6-bit immediate value.
[i:j]	Denotes bit **i** to **j** in an immediate value.

Some instructions access or use doubleword operands. These operands must be placed in two consecutive register addresses where the first register must be an even register. The even register contains the least significant part and the odd register contains the most significant part. This ordering is reversed in comparison with how data is organized in memory (where the most significant part would receive the lowest address) and is intentional.

The programmer is responsible for placing these operands in properly aligned register pairs. This is also specified in the "Operands" section in the detailed description of each instruction. Failure to do so will result in an undefined behavior.

7.8.1.2 Operations

ASR(x, n)	SE(x, Bits(x) + n) >> n
SATSU(x, n)	Signed to Unsigned Saturation (x is treated as a signed value):
	If (x > (2^n-1)) then (2^{n-1}-1); elseif (x < 0) then 0; else x;
SE(x, n)	Sign Extend x to an n-bit value

7.8.1.3 Data Type Extensions

.d	Double (64-bit) operation.
.w	Word (32-bit) operation.

7.8.2 PICO Instruction Summary

Table 7-4. PICO instruction summary

Mnemonics		Operands / Syntax	Description	Operation
picosvmac	E	OUTd, INx, INy, INz	PICO single vector multiplication and accumulation.	See PICO instruction set reference
picosvmul	E	OUTd, INx, INy, INz	PICO single vector multiplication	See PICO instruction set reference
picovmac	E	OUTd, INx, INy, INz	PICO vector multiplications and accumulations.	See PICO instruction set reference
picovmul	E	OUTd, INx, INy, INz	PICO vector multiplications.	See PICO instruction set reference
picold.d	E	PrHi:PrLo, Rp[disp]	Load PICO register pair	PrHi:PrLo ← *(Rp+ZE(disp8<<2))
	E	PrHi:PrLo, --Rp	Load PICO register pair with pre-decrement	PrHi:PrLo ← *(--Rp)
	E	PrHi:PrLo, Rb[Ri<<sa]	Load PICO register pair with indexed addressing	PrHi:PrLo ← *(Rb+(Ri << sa2))
picold.w	E	Pr, Rp[disp]	Load PICO register	Pr ← *(Rp+ZE(disp8<<2))
	E	Pr, --Rp	Load PICO register with pre-decrement	Pr ← *(--Rp)
	E	Pr, Rb[Ri<<sa]	Load PICO register with indexed addressing	Pr ← *(Rb+(Ri << sa2))
picoldm	E	Rp{++}, PICORegList	Load multiple PICO registers	See PICO instruction set reference
picomv.d	E	Rd, PrHi:PrLo	Move from PICO register pair to CPU register pair	Rd+1:Rd ← PrHi:PrLo
	E	PrHi:PrLo, Rd	Move from CPU register pair to PICO register pair	PrHi:PrLo ← Rd+1:Rd
picomv.w	E	Rd, Pr	Move from PICO register to CPU register	Rd ← Pr
	E	Pr, Rd	Move from CPU register to PICO register	Pr ← Rd
picost.d	E	Rp[disp], PrHi:PrLo	Store PICO register pair	*(Rp+ZE(disp8<<2)) ← PrHi:PrLo
	E	Rp++, PrHi:PrLo	Store PICO register pair with post-increment	*(Rp--) ← PrHi:PrLo
	E	Rb[Ri<<sa], PrHi:PrLo	Store PICO register pair with indexed addressing	*(Rb+(Ri << sa2)) ← PrHi:PrLo
picost.w	E	Rp[disp], Pr	Store PICO register	*(Rp+ZE(disp8<<2)) ← Pr
	E	Rp++, Pr	Store PICO register with post-increment	*(Rp--) ← Pr
	E	Rb[Ri<<sa], Pr	Store PICO register with indexed addressing	*(Rb+(Ri << sa2)) ← Pr
picostm	E	{--}Rp, PICORegList	Store multiple PICO registers	See PICO instruction set reference

PICOSVMAC – PICO Single Vector Multiplication and Accumulation

Description

Performs three vector multiplications where the input pixels taken from the INPIX*n* registers depends on the Input Selection Mode and the input pixel addresses given in the instruction. The values in the VMU*n*_OUT registers are then accumulated with the new results from the vector multiplications. The results from each Vector Multiplication Unit (VMU) are then added together for one of the outputs to the Output Pixels Inserter to form the result of a single vector multiplication of two 9-element vectors. The results from the VMUs are then scaled and saturated to unsigned 8-bit values before being inserted into the OUTPIX*n* registers. Which pixels to update in the OUTPIX*n* registers depend upon the Output Insertion Mode and the output pixel address given in the instruction.

Operation:

I. if (Input Selection Mode == Horizontal Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN(x+0) \\ IN(x+1) \\ IN(x+2) \end{bmatrix} + VMU0_OUT$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN(y+0) \\ IN(y+1) \\ IN(y+2) \end{bmatrix} + VMU1_OUT$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN(z+0) \\ IN(z+1) \\ IN(z+2) \end{bmatrix} + VMU2_OUT$$

else if (Input Selection Mode == Vertical Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN((x+0)\%11) \\ IN((x+4)\%11) \\ IN((x+8)\%11) \end{bmatrix} + VMU0_OUT$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN((y+0)\%11) \\ IN((y+4)\%11) \\ IN((y+8)\%11) \end{bmatrix} + VMU1_OUT$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN((z+0)\%11) \\ IN((z+4)\%11) \\ IN((z+8)\%11) \end{bmatrix} + VMU2_OUT$$

else if (Input Selection Mode == Transformation Mode) then

$$\begin{bmatrix} VMU0_OUT \\ VMU1_OUT \\ VMU2_OUT \end{bmatrix} = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \\ COEFF1_0 & COEFF1_1 & COEFF1_2 \\ COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} INx \\ INy \\ INz \end{bmatrix} + \begin{bmatrix} VMU0_OUT \\ VMU1_OUT \\ VMU2_OUT \end{bmatrix}$$

if (Output Insertion Mode == Packed Insertion Mode) then
OUT(d*3 + 0) ← SATSU(ASR(VMU0_OUT + VMU1_OUT + VMU2_OUT, COEFF_FRAC_BITS) , 8);
OUT(d*3 + 1) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);
OUT(d*3 + 2) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);
else if (Output Insertion Mode == Planar Insertion Mode) then
OUT(d + 0) ← SATSU(ASR(VMU0_OUT + VMU1_OUT+ VMU2_OUT, COEFF_FRAC_BITS), 8);
OUT(d + 4) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);
OUT(d + 8) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);

Syntax:

I. picosvmac OUTd, INx, INy, INz

Operands:

I. d ∈ {0, 1, 2, 3}
x, y, z ∈ {0, 1, ..., 11}

Opcode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	0	0	0	1	1	0	1	0	0	1	1	OUT d[1]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			OUT d[0]	INx				INy				INz			

Example:

```
/*
        Inner loop of a 16-tap symmetric FIR filter with coefficients {c0, c1, c2, c3, c4, c5, c6, c7, c7, ..., c0} set to filter the
        pixels pointed to by r12 storing the result to the memory pointed to by r11. The coefficients in the PICO are already
        set to the following values: COEFF0_0 = c0, COEFF0_1 = c1, COEFF0_2 = c2, COEFF1_0 = c3, COEFF1_1 = c4,
        COEFF1_2 = c5, COEFF2_0 = c6, COEFF2_1 = c7, COEFF2_2 = 0, OFFSET0 = 0.5 (For rounding the result),
        OFFSET1 = 0, OFFSET2 = 0.


        The Input Selection Mode is set to Horizontal Filter Mode while the Output Insertion Mode is set to Planar Insertion
        Mode.
        The input image pointer might be unaligned, hence the use of ld.w instead of picold.w.
*/
...
ld.w            r1, r12[0]              /* r1 = *((int *)src) */
ld.w            r0, r12[4]              /* r0 = *(((int *)src) + 1) */
ld.w            r2, r12[8]              /* r2 = *(((int *)src) + 2) */
ld.w            r3, r12[12]             /* r3 = *(((int *)src) + 3) */
picomv.d        INPIX1:INPIX2, r0       /* INPIX1={src[0],src[1],src[2],src[3]}, INPIX2={src[4],src[5],src[6],src[7]}*/
swap.b          r2                      /* r2 = {src[11],src[10],src[9],src[8]}*/
swap.b          r3                      /* r3 = {src[15],src[14],src[13],src[12]}*/
picosvmul       OUT3, IN4, IN7, IN10    /*      VMU0_OUT = c0*src[0]+c1*src[1]+c2*src[2] + 0.5
                                                VMU1_OUT = c3*src[3]+c4*src[4]+c5*src[5]
                                                VMU2_OUT = c6*src[6]+c7*src[7] */
picomv.d        INPIX1:INPIX2, r2       /*      INPIX1={src[15],src[14],src[13],src[12]},
                                                INPIX2 ={src[11],src[10],src[9],src[8]} */
picosvmac       OUT3, IN4, IN7, IN10    /*      VMU0_OUT += c0*src[15]+c1*src[14]+c2*src[13]
                                                VMU1_OUT += c3*src[12]+c4*src[11]+c5*src[10]
                                                VMU2_OUT += c6*src[9]+c7*src[8]
                                                OUT3 = satscaled(VMU0_OUT+VMU1_OUT+VMU2_OUT)*/

sub             r12, -1                 /* src++ */
picomv.w        r4, OUTPIX0             /* r4 = { OUT0, OUT1, OUT2, OUT3 }
st.b            r11++, r4               /* *dst = OUT3 */
...
```

PICOSVMUL – PICO Single Vector Multiplication

Description

Performs three vector multiplications where the input pixels taken from the INPIX*n* registers depends on the Input Selection Mode and the input pixel addresses given in the instruction. The results from each Vector Multiplication Unit (VMU) are then added together for one of the outputs to the Output Pixels Inserter to form the result of a single vector multiplication of two 9-element vectors. The results from the VMUs are then scaled and saturated to unsigned 8-bit values before being inserted into the OUTPIX*n* registers. Which pixels to update in the OUTPIX*n* registers depend upon the Output Insertion Mode and the output pixel address given in the instruction.

Operation:

I. OFFSET_SCALE = COEFF_FRAC_BITS - OFFSET_FRAC_BITS

if (Input Selection Mode == Horizontal Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN(x+0) \\ IN(x+1) \\ IN(x+2) \end{bmatrix} + OFFSET0 << OFFSET_SCALE$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN(y+0) \\ IN(y+1) \\ IN(y+2) \end{bmatrix} + OFFSET1 << OFFSET_SCALE$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN(z+0) \\ IN(z+1) \\ IN(z+2) \end{bmatrix} + OFFSET2 << OFFSET_SCALE$$

else if (Input Selection Mode == Vertical Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN((x+0)\%11) \\ IN((x+4)\%11) \\ IN((x+8)\%11) \end{bmatrix} + OFFSET0 << OFFSET_SCALE$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN((y+0)\%11) \\ IN((y+4)\%11) \\ IN((y+8)\%11) \end{bmatrix} + OFFSET1 << OFFSET_SCALE$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN((z+0)\%11) \\ IN((z+4)\%11) \\ IN((z+8)\%11) \end{bmatrix} + OFFSET2 << OFFSET_SCALE$$

else if (Input Selection Mode == Transformation Mode) then

$$\begin{bmatrix} VMU0_OUT \\ VMU1_OUT \\ VMU2_OUT \end{bmatrix} = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \\ COEFF1_0 & COEFF1_1 & COEFF1_2 \\ COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} INx \\ INy \\ INz \end{bmatrix} + \begin{bmatrix} OFFSET0 << OFFSET_SCALE \\ OFFSET1 << OFFSET_SCALE \\ OFFSE20 << OFFSET_SCALE \end{bmatrix}$$

if (Output Insertion Mode == Packed Insertion Mode) then

OUT(d*3 + 0) ← SATSU(ASR(VMU0_OUT + VMU1_OUT + VMU2_OUT, COEFF_FRAC_BITS), 8);

OUT(d*3 + 1) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);

OUT(d*3 + 2) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);

else if (Output Insertion Mode == Planar Insertion Mode) then

OUT(d + 0) ← SATSU(ASR(VMU0_OUT + VMU1_OUT+ VMU2_OUT, COEFF_FRAC_BITS), 8);

OUT(d + 4) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);

OUT(d + 8) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);

Syntax:

I. picosvmul OUTd, INx, INy, INz

Operands:

I. d ∈ {0, 1, 2, 3}
x, y, z ∈ {0, 1, ... , 11}

Opcode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	0	0	0	1	1	0	1	0	0	1	0	OUT d[1]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			OUT d[0]	INx				INy				INz			

Example:

```
/*
        Excerpt from inner loop of bilinear interpolation filter operating on image component stored in an array pointed to by
        r12. The width of the image is stored in r11 while the resulting filtered image is pointed to by r10. The coefficients of
        the filter: A, B, C, D are already set before this code is executed. COEFF0_0 = A, COEFF0_1 = B, COEFF0_2 = 0,
        COEFF1_0 = C, COEFF1_1 = D, COEFF1_2 = 0, COEFF2_0 = 0, COEFF2_1 = 0, COEFF2_2 = 0, OFFSET0 = 0.5
        (For rounding the result), OFFSET1 = 0, OFFSET2 = 0.

        The Input Selection Mode is set to Horizontal Filter Mode while the Output Insertion Mode is set to Planar Insertion
        Mode.

        The input image pointer might be unaligned, hence the use of ld.w instead of picold.w, while the output image pointer
        is word aligned.

        Four output pixels are computed in this example which show an example of a bilinear interpolation filter found in
        the Motion Compensation used in the H.264 Video Standard.
*/
...
ld.w        r1, r12[0]          /* r1 = *((int *)src) */
ld.w        r0, r12[r11]        /* r0 = *((int *)(src + width)) */
sub         r12, -2             /* src+=2 */
ld.w        r3, r12[0]          /* r3 = *((int *)src) */
ld.w        r2, r12[r11]        /* r2 = *((int *)(src + width)) */
picomv.d    INPIX1:INPIX2, r0   /* INPIX1 = r1, INPIX2 = r0 */
picosvmul   OUT0, IN4, IN8, IN0 /* OUT0 = A*src[j][i+0] + B*src[j][i+1] C*src[j+1][i] + D*src[j+1][i+1] */
picosvmul   OUT1, IN5, IN9, IN0 /* OUT1 = A*src[j][i+1] + B*src[j][i+2] C*src[j+1][i+1] + D*src[j+1][i+2] */
picomv.d    INPIX1:INPIX2, r2   /* INPIX1 = r3, INPIX2 = r2 */
picosvmul   OUT2, IN4, IN8, IN0 /* OUT2 = A*src[j][i+2] + B*src[j][i+3] C*src[j+1][i+2] + D*src[j+1][i+3] */
picosvmul   OUT3, IN5, IN9, IN0 /* OUT3 = A*src[j][i+3] + B*src[j][i+4] C*src[j+1][i+3] + D*src[j+1][i+4] */
sub         r12, -2             /* src+=2 */
picost.w    r10++, OUTPIX0      /* *((int *)src) = { OUT0, OUT1, OUT2, OUT3 } */
...
```

PICOVMAC – PICO Vector Multiplication and Accumulation

Description

Performs three vector multiplications where the input pixels taken from the INPIX*n* registers depends on the Input Selection Mode and the input pixel addresses given in the instruction. The values in the VMU*n*_OUT registers are then accumulated with the new results from the vector multiplications. The results from the VMUs are then scaled and saturated to unsigned 8-bit values before being inserted into the OUTPIX*n* registers. Which pixels to update in the OUTPIX*n* registers depend upon the Output Insertion Mode and the output pixel address given in the instruction.

Operation:

I. if (Input Selection Mode == Horizontal Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN(x+0) \\ IN(x+1) \\ IN(x+2) \end{bmatrix} + VMU0_OUT$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN(y+0) \\ IN(y+1) \\ IN(y+2) \end{bmatrix} + VMU1_OUT$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN(z+0) \\ IN(z+1) \\ IN(z+2) \end{bmatrix} + VMU2_OUT$$

else if (Input Selection Mode == Vertical Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN((x+0)\%11) \\ IN((x+4)\%11) \\ IN((x+8)\%11) \end{bmatrix} + VMU0_OUT$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN((y+0)\%11) \\ IN((y+4)\%11) \\ IN((y+8)\%11) \end{bmatrix} + VMU1_OUT$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN((z+0)\%11) \\ IN((z+4)\%11) \\ IN((z+8)\%11) \end{bmatrix} + VMU2_OUT$$

else if (Input Selection Mode == Transformation Mode) then

$$\begin{bmatrix} VMU0_OUT \\ VMU1_OUT \\ VMU2_OUT \end{bmatrix} = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \\ COEFF1_0 & COEFF1_1 & COEFF1_2 \\ COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} INx \\ INy \\ INz \end{bmatrix} + \begin{bmatrix} VMU0_OUT \\ VMU1_OUT \\ VMU2_OUT \end{bmatrix}$$

if (Output Insertion Mode == Packed Insertion Mode) then
OUT(d*3 + 0) ← SATSU(ASR(VMU0_OUT, COEFF_FRAC_BITS), 8);
OUT(d*3 + 1) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);
OUT(d*3 + 2) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);
else if (Output Insertion Mode == Planar Insertion Mode) then
OUT(d + 0) ← SATSU(ASR(VMU0_OUT, COEFF_FRAC_BITS), 8);
OUT(d + 4) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);
OUT(d + 8) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);

Syntax:

I. picovmac OUTd, INx, INy, INz

Operands:

I. d ∈ {0, 1, 2, 3}
x, y, z ∈ {0, 1, ... , 11}

Opcode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	0	0	0	1	1	0	1	0	0	0	1	OUT d[1]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			OUT d[0]	INx				INy				INz			

Example:

```
/*
        Inner loop of a 6-tap symmetric FIR filter with coefficients {c0, c1, c2, c2, c1, c0 } set to filter in the vertical direction
        of the image pointed to by r12 with the width of the image stored in r11 and the destination image stored in r10. The
        coefficients in the PICO are already set to the following values: COEFF0_0 = c0, COEFF0_1 = c1, COEFF0_2 = c2,
        COEFF1_0 = c0, COEFF1_1 = c1, COEFF1_2 = c2, COEFF2_0 = c0, COEFF2_1 = c1, COEFF2_2 = c2,
        OFFSET0 = OFFSET1 = OFFSET2 = 0.5 (For rounding the result).
        The Input Selection Mode is set to Vertical Filter Mode while the Output Insertion Mode is set to Packed Insertion
        Mode.

        The input image is assumed to be word aligned.
*/
...
picold.w        INPIX0, r12[0]          /* INPIX0 = {src[0][0], src[0][1], src[0][2], src[0][3] }*/
picold.w        INPIX1, r12[r11]        /* INPIX1 = {src[1][0], src[1][1], src[1][2], src[1][3] }*/
picold.w        INPIX2, r12[r11 << 1]   /* INPIX2 = {src[2][0], src[2][1], src[2][2], src[2][3] }*/
add             r9, r12, r11            /* r9 = src + width */
picovmul        OUT0, IN0, IN1, IN2     /*      VMU0_OUT = c0*src[0][0]+c1*src[1][0]+c2*src[2][0] + 0.5
                                                VMU1_OUT = c0*src[0][1]+c1*src[1][1]+c2*src[2][1] + 0.5
                                                VMU2_OUT = c0*src[0][2]+c1*src[1][2]+c2*src[2][2] + 0.5*/
picold.w        INPIX2, r9[r11 << 1]    /* INPIX2 = {src[3][0], src[3][1], src[3][2], src[3][3] }*/
picold.w        INPIX1, r12[r11 << 2]   /* INPIX1 = {src[4][0], src[4][1], src[4][2], src[4][3] }*/
picold.w        INPIX0, r9[r11 << 2]    /* INPIX0 = {src[5][0], src[5][1], src[5][2], src[5][3] }*/
picovmac        OUT0, IN0, IN1, IN2     /*      VMU0_OUT += c0*src[5][0]+c1*src[4][0]+c2*src[3][0]
                                                VMU1_OUT += c0*src[5][1]+c1*src[4][1]+c2*src[3][1]
                                                VMU2_OUT += c0*src[5][2]+c1*src[4][2]+c2*src[3][2]
                                                OUT0 = satscale(VMU0_OUT), OUT1 = satscale(VMU1_OUT),
                                                OUT2 = satscale(VMU2_OUT) */
....
```

PICOVMUL – PICO Vector Multiplication

Description

Performs three vector multiplications where the input pixels taken from the INPIX*n* registers depends on the Input Selection Mode and the input pixel addresses given in the instruction. The results from the VMUs are then scaled and saturated to unsigned 8-bit values before being inserted into the OUTPIX*n* registers. Which pixels to update in the OUTPIX*n* registers depend upon the Output Insertion Mode and the output pixel address given in the instruction.

Operation:

I. OFFSET_SCALE = COEFF_FRAC_BITS - OFFSET_FRAC_BITS

if (Input Selection Mode == Horizontal Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN(x+0) \\ IN(x+1) \\ IN(x+2) \end{bmatrix} + OFFSET0 << OFFSET_SCALE$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN(y+0) \\ IN(y+1) \\ IN(y+2) \end{bmatrix} + OFFSET1 << OFFSET_SCALE$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN(z+0) \\ IN(z+1) \\ IN(z+2) \end{bmatrix} + OFFSET2 << OFFSET_SCALE$$

else if (Input Selection Mode == Vertical Filter Mode) then

$$VMU0_OUT = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \end{bmatrix} \begin{bmatrix} IN((x+0)\%11) \\ IN((x+4)\%11) \\ IN((x+8)\%11) \end{bmatrix} + OFFSET0 << OFFSET_SCALE$$

$$VMU1_OUT = \begin{bmatrix} COEFF1_0 & COEFF1_1 & COEFF1_2 \end{bmatrix} \begin{bmatrix} IN((y+0)\%11) \\ IN((y+4)\%11) \\ IN((y+8)\%11) \end{bmatrix} + OFFSET1 << OFFSET_SCALE$$

$$VMU2_OUT = \begin{bmatrix} COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} IN((z+0)\%11) \\ IN((z+4)\%11) \\ IN((z+8)\%11) \end{bmatrix} + OFFSET2 << OFFSET_SCALE$$

else if (Input Selection Mode == Transformation Mode) then

$$\begin{bmatrix} VMU0_OUT \\ VMU1_OUT \\ VMU2_OUT \end{bmatrix} = \begin{bmatrix} COEFF0_0 & COEFF0_1 & COEFF0_2 \\ COEFF1_0 & COEFF1_1 & COEFF1_2 \\ COEFF2_0 & COEFF2_1 & COEFF2_2 \end{bmatrix} \begin{bmatrix} INx \\ INy \\ INz \end{bmatrix} + \begin{bmatrix} OFFSET0 << OFFSET_SCALE \\ OFFSET1 << OFFSET_SCALE \\ OFFSE20 << OFFSET_SCALE \end{bmatrix}$$

if (Output Insertion Mode == Packed Insertion Mode) then

OUT(d*3 + 0) ← SATSU(ASR(VMU0_OUT, COEFF_FRAC_BITS), 8);
OUT(d*3 + 1) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);
OUT(d*3 + 2) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);

else if (Output Insertion Mode == Planar Insertion Mode) then

OUT(d + 0) ← SATSU(ASR(VMU0_OUT, COEFF_FRAC_BITS), 8);
OUT(d + 4) ← SATSU(ASR(VMU1_OUT, COEFF_FRAC_BITS), 8);
OUT(d + 8) ← SATSU(ASR(VMU2_OUT, COEFF_FRAC_BITS), 8);

Syntax:

I. picovmul OUTd, INx, INy, INz

Operands:

I. d ∈ {0, 1, 2, 3}
x, y, z ∈ {0, 1, ... , 11}

Opcode:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	0	0	0	1	1	0	1	0	0	0	0	OUT d[1]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			OUT d[0]	INx				INy				INz			

Example:

```
/*
        Excerpt from inner loop of YCrCb 4:2:2 planar format to RGB packed format image color conversion. The
        coefficients of the transform is already set before this code is executed. In transforms like this, the inputs Y, Cr and
        Cb are often offsetted with a given amount. This offset can be factored out and included in the offsets like this:
        1.164*(Y - 16) = 1.164*Y - 18.625.
        The pointer to the Y component is in r12, the pointer to the Cr component in r11 and the pointer to the Cb component
        in r10. The pointer to the RGB output image is in r9.

        The Input Selection Mode is set to Transform Mode while the Output Insertion Mode is set to Packed Insertion
        Mode.

        It is assumed that all the input and output pointers are word aligned.

        Four RGB triplets are computed in this example. */

...
picold.w        INPIX0, r12++           /* INPIX0= { Y[0], Y[1], Y[2], Y[3] }*/
picold.w        INPIX1, r11++           /* INPIX1= { Cr[0], Cr[1], Cr[2], Cr[3] }*/
picold.w        INPIX2, r10++           /* INPIX2= { Cb[0], Cb[1], Cb[2], Cb[3] }*/
picovmul        OUT0, IN0, IN4, IN8     /* OUT0 = r[0], OUT1 = g[0], OUT2 = b[0] */
picovmul        OUT1, IN1, IN4, IN8     /* OUT3 = r[1], OUT4 = g[1], OUT5 = b[1] */
picovmul        OUT2, IN2, IN5, IN9     /* OUT6 = r[2], OUT7 = g[2], OUT8 = b[2] */
picovmul        OUT3, IN3, IN5, IN9     /* OUT9 = r[3], OUT10 = g[3], OUT11 = b[3] */
picostm         r9, OUTPIX2, OUTPIX1, OUTPIX0/* RGB = {r[0],g[0],b[0],r[1],g[1],b[1],r[2],g[2],b[2],r[3],g[3],b[3]} */
...
```

PICOLD.{D,W} – Load PICO Register(s)

Description
Reads the memory location specified into the given coprocessor register(s).

Operation:
I. PrHi:PrLo ← *(Rp + (ZE(disp8) << 2));
II. Rp ← Rp-8;
PrHi:PrLo ← *(Rp);
III. PrHi:PrLo ← *(Rb + (Ri << sa2));
IV. Pr ← *(Rp + (ZE(disp8) << 2));
V. Rp ← Rp-4;
Pr ← *(Rp);
VI. Pr ← *(Rb + (Ri << sa2));

Syntax:
I. picold.d PrHi:PrLo, Rp[disp]
II. picold.d PrHi:PrLo, --Rp
III. picold.d PrHi:PrLo, Rb[Ri<<sa]
IV. picold.w Pr, Rp[disp]
V. picold.w Pr, --Rp
VI. picold.w Pr, Rb[Ri<<sa]

Operands:
I-III. PrHi:PrLo ∈ { INPIX1:INPIX2, COEFF0_B:COEFF0_A, COEFF1_B:COEFF1_A, COEFF2_B:COEFF2_A, VMU1_OUT:VMU0_OUT, CONFIG:VMU2_OUT}
IV-VI. Pr ∈ { INPIX0, INPIX1, INPIX2, COEFF0_A, COEFF0_B, COEFF1_A, COEFF1_B, COEFF2_A, COEFF2_B, VMU0_OUT, VMU1_OUT, VMU2_OUT, CONFIG}
I-II, IV-V.p ∈ {0, 1, …, 15}
I, IV. disp ∈ {0, 4, …, 1020}
III, VI. {b, i} ∈ {0, 1, …, 15}
III, VI. sa ∈ {0, 1, 2, 3}

Opcode
I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	0	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			1	PrLo[3:1]			0	disp8							

II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	PrLo[3:1]			0	0	1	0	1	0	0	0	0

III.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			1	PrLo[3:1]			0	0	1	Shamt		Ri			

IV.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	0	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	Pr				disp8							

V.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	Pr				0	1	0	0	0	0	0	0

VI.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			1	Pr				0	0	Shamt		Ri			

Example:

```
picold.d        COEFF0_B:COEFF0_A, r12[4]
```

PICOLDM – Load Multiple PICO Registers

Description
Reads the memory locations specified into the given PICO registers. The pointer register can optionally be updated after the operation.

Operation:

```
I. II. III.  Loadaddress  ←Rp;
        if ( PICORegList contains CONFIG )
                CONFIG ← *(Loadaddress++);
        if ( PICORegList contains VMU2_OUT )
                VMU2_OUT ← *(Loadaddress++);
        if ( PICORegList contains VMU1_OUT )
                VMU1_OUT ← *(Loadaddress++);
        if ( PICORegList contains VMU0_OUT )
                VMU0_OUT ← *(Loadaddress++);
        if ( PICORegList contains COEFF2_B)
                COEFF2_B ← *(Loadaddress++);
        if ( PICORegList contains COEFF2_A)
                COEFF2_A ← *(Loadaddress++);
        if ( PICORegList contains COEFF1_B)
                COEFF1_B ← *(Loadaddress++);
        if ( PICORegList contains COEFF1_A)
                COEFF1_A ← *(Loadaddress++);
        if ( PICORegList contains COEFF0_B)
                COEFF0_B ← *(Loadaddress++);
        if ( PICORegList contains COEFF0_A)
                COEFF0_A ← *(Loadaddress++);
        if ( PICORegList contains OUTPIX0)
                Loadaddress++;
        if ( PICORegList contains OUTPIX1)
                Loadaddress++;
        if ( PICORegList contains OUTPIX2)
                Loadaddress++;
        if ( PICORegList contains INPIX0)
                INPIX0 ← *(Loadaddress++);
        if ( PICORegList contains INPIX1)
                INPIX1 ← *(Loadaddress++);
        if ( PICORegList contains INPIX2)
                INPIX2 ← *(Loadaddress++);

        if Opcode[++] == 1 then
                Rp   ←  Loadaddress;
```

Syntax:

I.	picoldm	Rp{++}, PICORegList
II.	picoldm	Rp{++}, PICORegList
III.	picoldm	Rp{++}, PICORegList

Operands:

I. PICORegList ∈ { {INPIX1, INPIX2}, {OUTPIX2, INPIX0}, {OUTPIX0, OUTPIX1}, {COEFF0_B, COEFF0_A}, {COEFF1_B, COEFF1_A}, {COEFF2_B, COEFF2_A}, {VMU1_OUT, VMU0_OUT},

{CONFIG, VMU2_OUT} }

II. PICORegList ∈ { INPIX0, INPIX1, INPIX2, OUTPIX0, OUTPIX1, OUTPIX2, COEFF0_A, COEFF0_B }

III. PICORegList ∈ { COEFF1_A, COEFF1_B, COEFF2_A,COEFF2_B, VMU0_OUT,VMU1_OUT, VMU2_OUT, CONFIG, }

I-III. p ∈ {0, 1, …, 15}

Opcode

I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			W	0	1	0	0	CONFIG VMU2_OUT	VMU1_OUT VMU0_OUT	COEFF2_B COEFF2_A	COEFF1_B COEFF1_A	COEFF0_B COEFF0_A	OUTPIX0 OUTPIX1	OUTPIX2 INPIX0	INPIX1 INPIX2

II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			W	0	0	0	0	COEFF0_B	COEFF0_A	OUTPIX0	OUTPIX1	OUTPIX2	INPIX0	INPIX1	INPIX2

III.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			W	0	0	0	1	CONFIG	VMU2_OUT	VMU1_OUT	VMU0_OUT	COEFF2_B	COEFF2_A	COEFF1_B	COEFF1_A

Example:

I. picoldm r7++, COEFF0_A, COEFF0_B, COEFF1_A, COEFF1_B, COEFF2_A, COEFF2_B

II. picoldm r0, INPIX0, INPIX1, INPIX2

III. picoldm r12, VMU0_OUT, VMU1_OUT, VMU2_OUT

PICOMV.{D,W} – Move between PICO Register(s) and Register File

Description
Move the specified PICO register(s) to register(s) in the Register File or move register(s) in the Register File to PICO register(s).

Operation:
I. PrHi:PrLo ← (Rs+1:Rs);
II. Pr ← Rs;
III. (Rd+1:Rd) ← PrHi:PrLo;
IV. Rd ← Pr;

Syntax:

I.	picomv.d	PrHi:PrLo, Rs
II.	picomv.w	Pr, Rs
III.	picomv.d	Rd, PrHi:PrLo
IV.	picomv.w	Rd, Pr

Operands:
I, II. PrHi:PrLo ∈ { INPIX1:INPIX2, OUTPIX2:INPIX0, OUTPIX0:OUTPIX1, COEFF0_B:COEFF0_A, COEFF1_B:COEFF1_A, COEFF2_B:COEFF2_A, VMU1_OUT:VMU0_OUT, CONFIG:VMU2_OUT }
II, IV. Pr ∈ { INPIX0, INPIX1, INPIX2, OUTPIX0, OUTPIX1, OUTPIX2, COEFF0_A, COEFF0_B, COEFF1_A, COEFF1_B, COEFF2_A, COEFF2_B, VMU0_OUT, VMU1_OUT, VMU2_OUT, CONFIG}
I. s ∈ {0, 2, 4, …, 14}
III. d ∈ {0, 2, 4, …, 14}
II. s ∈ {0, 1, …, 15}
IV. d ∈ {0, 1, …, 15}

Opcode
I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rs			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	PrLo[3:1]			0	0	0	1	1	0	0	0	0

II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rs			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	Pr			0	0	1	0	0	0	0	0	0

III.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rd			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	PrLo[3:1]			0	0	0	0	1	0	0	0	0

IV.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rd			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	Pr			0	0	0	0	0	0	0	0	0

Example:

```
picomv.d    r2, OUTPIX0:OUTPIX1
picomv.w    CONFIG, lr
```

PICOST.{D,W} – Store PICO Register(s)

Description
Stores the PICO register value(s) to the memory location specified by the addressing mode.

Operation:
I. *(Rp + (ZE(disp8) << 2)) ← PrHi:PrLo;
II. *(Rp) ← PrHi:PrLo;
Rp ← Rp+8;
III. *(Rb + (Ri << sa2)) ← PrHi:PrLo;
IV. *(Rp + (ZE(disp8) << 2)) ← Pr;
V. *(Rp) ← Pr;
Rp ← Rp-4;
VI. *(Rb + (Ri << sa2)) ← Pr;

Syntax:
I. picost.d Rp[disp], PrHi:PrLo
II. picost.d Rp++, PrHi:PrLo
III. picost.d Rb[Ri<<sa], PrHi:PrLo
IV. picost.w Rp[disp], Pr
V. picost.w Rp++, Pr
VI. picost.w Rb[Ri<<sa], Pr

Operands:
I-III. PrHi:PrLo ∈ { INPIX1:INPIX2, OUTPIX2:INPIX0, OUTPIX0:OUTPIX1, COEFF0_B:COEFF0_A, COEFF1_B:COEFF1_A, COEFF2_B:COEFF2_A, VMU1_OUT:VMU0_OUT, CONFIG:VMU2_OUT }
IV-VI. Pr ∈ { INPIX0, INPIX1, INPIX2, OUTPIX0, OUTPIX1, OUTPIX2, COEFF0_A, COEFF0_B, COEFF1_A, COEFF1_B, COEFF2_A, COEFF2_B, VMU0_OUT, VMU1_OUT, VMU2_OUT, CONFIG}
I-II, IV-V.p ∈ {0, 1, …, 15}
I, IV. disp ∈ {0, 4, …, 1020}
III, VI. {b, i} ∈ {0, 1, …, 15}
III, VI. sa ∈ {0, 1, 2, 3}

Opcode
I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	0	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			1	PrLo[3:1]			0	disp8							

II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	PrLo[3:1]			0	0	1	1	1	0	0	0	0

III.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			1	PrLo[3:1]			0	1	1	Shamt		Ri			

IV.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	0	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	Pr				disp8							

V.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			0	Pr				0	1	1	0	0	0	0	0

VI.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	1	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			1	Pr				1	0	Shamt		Ri			

Example:

```
picost.w        r10++, OUTPIX0
```

PICOSTM – Store Multiple PICO Registers

Description
Writes the PICO registers specified in the register list into the specified memory locations.

Operation:
I. II. III.

```
if Opcode[--] == 1 then
        Rp ← Rp - 4*RegistersInList;
Storeaddress ←Rp;

if ( PICORegList contains CONFIG )
        *(Storeaddress++) ← CONFIG;
if ( PICORegList contains VMU2_OUT )
        *(Storeaddress++) ← VMU2_OUT;
if ( PICORegList contains VMU1_OUT )
        *(Storeaddress++) ← VMU1_OUT;
if ( PICORegList contains VMU0_OUT )
        *(Storeaddress++) ← VMU0_OUT;
if ( PICORegList contains COEFF2_B)
        *(Storeaddress++) ← COEFF2_B;
if ( PICORegList contains COEFF2_A)
        *(Storeaddress++) ← COEFF2_A;
if ( PICORegList contains COEFF1_B)
        *(Storeaddress++) ← COEFF1_B;
if ( PICORegList contains COEFF1_A)
        *(Storeaddress++) ← COEFF1_A;
if ( PICORegList contains COEFF0_B)
        *(Storeaddress++) ← COEFF0_B;
if ( PICORegList contains COEFF0_A)
        *(Storeaddress++) ← COEFF0_A;
if ( PICORegList contains OUTPIX0)
        *(Storeaddress++) ← OUTPIX0;
if ( PICORegList contains OUTPIX1)
        *(Storeaddress++) ← OUTPIX1;
if ( PICORegList contains OUTPIX2)
        *(Storeaddress++) ← OUTPIX2;
if ( PICORegList contains INPIX0)
        *(Storeaddress++) ←INPIX0 ;
if ( PICORegList contains INPIX1)
        *(Storeaddress++) ←INPIX1 ;
if ( PICORegList contains INPIX2)
        *(Storeaddress++) ←INPIX2 ;
```

Syntax:

I.	picostm	{--}Rp, PICORegList
II.	picostm	{--}Rp, PICORegList
III.	picostm	{--}Rp, PICORegList

Operands:
I. PICORegList ∈ { {INPIX1, INPIX2}, {OUTPIX2, INPIX0}, {OUTPIX0, OUTPIX1}, {COEFF0_B, COEFF0_A}, {COEFF1_B, COEFF1_A}, {COEFF2_B, COEFF2_A}, {VMU1_OUT, VMU0_OUT},

{CONFIG, VMU2_OUT} }

II. PICORegList ∈ { INPIX0, INPIX1, INPIX2, OUTPIX0, OUTPIX1, OUTPIX2, COEFF0_A, COEFF0_B }

III. PICORegList ∈ { COEFF1_A, COEFF1_B, COEFF2_A,COEFF2_B, VMU0_OUT,VMU1_OUT, VMU2_OUT, CONFIG, }

I-III. p ∈ {0, 1, …, 15}

Opcode

I.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			W	0	1	0	1	CONFIG VMU2_OUT	VMU1_OUT VMU0_OUT	COEFF2_B COEFF2_A	COEFF1_B COEFF1_A	COEFF0_B COEFF0_A	OUTPIX0 OUTPIX1	OUTPIX2 INPIX0	INPIX1 INPIX2

II.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			W	0	0	1	0	COEFF0_B	COEFF0_A	OUTPIX0	OUTPIX1	OUTPIX2	INPIX0	INPIX1	INPIX2

III.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	1	1	0	1	1	0	1	1	0	1	0	Rp			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PICO CP#			W	0	0	1	1	CONFIG	VMU2_OUT	VMU1_OUT	VMU0_OUT	COEFF2_B	COEFF2_A	COEFF1_B	COEFF1_A

Example:

I. picostm --r7, COEFF0_A, COEFF0_B, COEFF1_A, COEFF1_B, COEFF2_A, COEFF2_B

II. picostm r2, OUTPIX0, OUTPIX1, OUTPIX2

III. picostm r11, VMU0_OUT, VMU1_OUT, VMU2_OUT

7.9 Data Hazards

Data hazards are caused by data dependencies between instructions which are in different stages of the pipeline and reads/writes registers which are common to several pipeline stages. Because of the 3-stage pipeline employed in the PICO data hazards might exist between instructions. Data hazards are handled by hardware interlocks which can stall a new read command from or write command to the PICO register file.

Table 7-5. Data Hazards

Instruction	Next Instruction	Condition	Stall Cycles
picovmul picovmac picosvmul picosvmac	picomv.x Pr,... picold.x picoldm	Write-After-Read (WAR) or Write-After-Write (WAW) Hazard will occur if writing COEFF*n*_A/B, VMU*n*_OUT or CONFIG since these are accessed when the PICO command is in Pipeline Stage 2 and Pipeline Stage 3.	1
		Writes to INPIX*n* registers produces no hazard since they are only accessed in Pipeline Stage 1.	0
	picomv.x Rd,... picost.x picostm	Read-After-Write Hazard (RAW) will occur if reading the PICO register file while a command is in the pipeline.	2

8. Memories

8.1 Embedded Memories

- **32 Kbyte SRAM**
  - **Implemented as two 16Kbyte blocks**
  - **Single cycle access at full bus speed**

8.2 Physical Memory Map

The system bus is implemented as an HSB bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even in boot. Note that AT32AP7000 by default uses segment translation, as described in the AVR32 Architecture Manual. The 32 bit physical address space is mapped as follows:

Table 8-1. AT32AP7000 Physical Memory Map

Start Address	Size	Device
0x0000_0000	64 Mbyte	EBI SRAM CS0
0x0400_0000	64 Mbyte	EBI SRAM CS4
0x0800_0000	64 Mbyte	EBI SRAM CS2
0x0C00_0000	64 Mbyte	EBI SRAM CS3
0x1000_0000	256 Mbyte	EBI SRAM/SDRAM CS1
0x2000_0000	64 Mbyte	EBI SRAM CS5
0x2400_0000	16 Kbyte	Internal SRAM 0
0x2400_4000	16 Kbyte	Internal SRAM1
0xFF00_0000	4 Kbyte	LCDC configuration
0xFF20_0000	1 KByte	DMACA configuration
0xFF30_0000	1 MByte	USBA Data
0xFFE0_0000	1 MByte	PBA
0xFFF0_0000	1 MByte	PBB

Accesses to unused areas returns an error result to the master requesting such an access.

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table below can be used to index the HMATRIX control registers. For example, MCFG2 is associated with the HSB-HSB bridge.

Table 8-2. HSB masters

Master 0	CPU Dcache
Master 1	CPU Icache
Master 2	HSB-HSB Bridge
Master 3	ISI DMA
Master 4	USBA DMA
Master 5	LCD Controller DMA
Master 6	Ethernet MAC0 DMA
Master 7	Ethernet MAC1 DMA
Master 8	DMAC Master Interface 0
Master 9	DMAC Master Interface 1

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with PBB.

Table 8-3. HSB slaves

Slave 0	Internal SRAM 0
Slave 1	Internal SRAM1
Slave 2	PBA
Slave 3	PBB
Slave 4	EBI
Slave 5	USBA data
Slave 6	LCDC configuration
Slave 7	DMACA configuration

9. Peripherals

9.1 Peripheral address map

Table 9-1. Peripheral Address Mapping

Address		Peripheral Name	Bus
0xFF000000	LCDC	LCD Controller Slave Interface - LCDC	HSB
0xFF200000	DMACA	DMA Controller Slave Interface- DMACA	HSB
0xFF300000	USBA	USB Slave Interface - USBA	HSB
0xFFE00000	SPI0	Serial Peripheral Interface - SPI0	PB A
0xFFE00400	SPI1	Serial Peripheral Interface - SPI1	PB A
0xFFE00800	TWI	Two-wire Interface - TWI	PB A
0xFFE00C00	USART0	Universal Synchronous Asynchronous Receiver Transmitter - USART0	PB A
0xFFE01000	USART1	Universal Synchronous Asynchronous Receiver Transmitter - USART1	PB A
0xFFE01400	USART2	Universal Synchronous Asynchronous Receiver Transmitter - USART2	PB A
0xFFE01800	USART3	Universal Synchronous Asynchronous Receiver Transmitter - USART3	PB A
0xFFE01C00	SSC0	Synchronous Serial Controller - SSC0	PB A
0xFFE02000	SSC1	Synchronous Serial Controller - SSC1	PB A
0xFFE02400	SSC2	Synchronous Serial Controller - SSC2	PB A
0xFFE02800	PIOA	Parallel Input/Output 2 - PIOA	PB A
0xFFE02C00	PIOB	Parallel Input/Output 2 - PIOB	PB A
0xFFE03000	PIOC	Parallel Input/Output 2 - PIOC	PB A
0xFFE03400	PIOD	Parallel Input/Output 2 - PIOD	PB A

Table 9-1. Peripheral Address Mapping (Continued)

Address		Peripheral Name	Bus
0xFFE03800	PIOE	Parallel Input/Output 2 - PIOE	PB A
0xFFE03C00	PSIF	PS2 Interface - PSIF	PB A
0xFFF00000	PM	Power Manager - PM	PB B
0xFFF00080	RTC	Real Time Counter- RTC	PB B
0xFFF000B0	WDT	WatchDog Timer- WDT	PB B
0xFFF00100	EIC	External Interrupt Controller - EIC	PB B
0xFFF00400	INTC	Interrupt Controller - INTC	PB B
0xFFF00800	HMATRIX	HSB Matrix - HMATRIX	PB B
0xFFF00C00	TC0	Timer/Counter - TC0	PB B
0xFFF01000	TC1	Timer/Counter - TC1	PB B
0xFFF01400	PWM	Pulse Width Modulation Controller - PWM	PB B
0xFFF01800	MACB0	Ethernet MAC - MACB0	PB B
0xFFF01C00	MACB1	Ethernet MAC - MACB1	PB B
0xFFF02000	ABDAC	Audio Bitstream DAC - ABDAC	PB B
0xFFF02400	MCI	MultiMedia Card Interface - MCI	PB B
0xFFF02800	AC97C	AC97 Controller - AC97C	PB B
0xFFF02C00	ISI	Image Sensor Interface - ISI	PB B
0xFFF03000	USBA	USB Configuration Interface - USBA	PB B
0xFFF03400	SMC	Static Memory Controller - SMC	PB B

Table 9-1. Peripheral Address Mapping (Continued)

Address		Peripheral Name	Bus
0xFFF03800	SDRAMC	SDRAM Controller - SDRAMC	PB B
0xFFF03C00	ECC	Error Correcting Code Controller - ECC	PB B

9.2 Interrupt Request Signal Map

The various modules may output interrupt request signals. These signals are routed to the Interrupt Controller (INTC). The Interrupt Controller supports up to 64 groups of interrupt requests. Each group can have up to 32 interrupt request signals. All interrupt signals in the same group share the same autovector address and priority level. Refer to the documentation for the individual submodules for a description of the semantic of the different interrupt requests.

The interrupt request signals in AT32AP7000 are connected to the INTC as follows:

Table 9-2. Interrupt Request Signal Map

Group	Line	Signal
0	0	COUNT-COMPARE match
	1	Performance Counter Overflow
1	0	LCDC EOF
	1	LCDC LN
	2	LCDC LSTLN
	3	LCDC MER
	4	LCDC OWR
	5	LCDC UFLW
2	0	DMACA BLOCK
	1	DMACA DSTT
	2	DMACA ERR
	3	DMACA SRCT
	4	DMACA TFR
3	0	SPI 0
4	0	SPI 1
5	0	TWI
6	0	USART0
7	0	USART1
8	0	USART2
9	0	USART3
10	0	SSC0
11	0	SSC1

Table 9-2. Interrupt Request Signal Map

Group	Line	Signal
12	0	SSC2
13	0	PIOA
14	0	PIOB
15	0	PIOC
16	0	PIOD
17	0	PIOE
18	0	PSIF
19	0	EIC0
	1	EIC1
	2	EIC2
	3	EIC3
20	0	PM
21	0	RTC
22	0	TC00
	1	TC01
	2	TC02
23	0	TC10
	1	TC11
	2	TC12
24	0	PWM
25	0	MACB0
26	0	MACB1
27	0	ABDAC
28	0	MCI
29	0	AC97C
30	0	ISI
31	0	USBA
32	0	EBI

9.3 DMACA Handshake Interface Map

The following table details the hardware handshake map between the DMACA and the peripherals attached to it: :

Table 9-3. Hardware Handshaking Connection

Request	Hardware Handshaking Interface
MCI RX	0
MCI TX	1
ABDAC TX	2
AC97C CHANNEL A RX	3
AC97C CHANNEL A TX	4
AC97C CHANNEL B RX	5
AC97C CHANNEL B TX	6
EXTERNAL DMA REQUEST 0	7
EXTERNAL DMA REQUEST 1	8
EXTERNAL DMA REQUEST 2	9
EXTERNAL DMA REQUEST 3	10

9.4 Clock Connections

9.4.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 9-4. Timer/Counter clock connections

Timer/Counter	Source	Name	Connection
0	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 9.7
		XC1	
		XC2	
1	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 9.7
		XC1	
		XC2	

9.4.2 USARTs

Each USART can be connected to an internally divided clock:

Table 9-5. USART clock connections

USART	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 8
1			
2			
3			

9.4.3 SPIs

Each SPI can be connected to an internally divided clock:

Table 9-6. SPI clock connections

SPI	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 32
1			

9.4.4 USBA

OSC1 is connected to the USB HS Phy and must be 12 MHz when using the USBA.

9.5 External Interrupt Pin Mapping

External interrupt requests are connected to the following pins::

Table 9-7. External Interrupt Pin Mapping

Source	Connection
NMI_N	PB24
EXTINT0	PB25
EXTINT1	PB26
EXTINT2	PB27
EXTINT3	PB28

9.6 Nexus OCD AUX port connections

If the OCD trace system is enabled, the trace system will take control over a number of pins, irrespectively of the PIO configuration. Two different OCD trace pin mappings are possible, depending on the configuration of the OCD AXS register. For details, see the *AVR32 AP Technical Reference Manual.*

Table 9-8. Nexus OCD AUX port connections

Pin	AXS=0	AXS=1
EVTI_N	EVTI_N	EVTI_N
MDO[5]	PB09	PC18
MDO[4]	PB08	PC14
MDO[3]	PB07	PC12
MDO[2]	PB06	PC11
MDO[1]	PB05	PC06
MDO[0]	PB04	PC05
EVTO_N	PB03	PB28
MCKO	PB02	PC02
MSEO[1]	PB01	PC01
MSEO[0]	PB00	PC00

9.7 Peripheral Multiplexing on IO lines

The AT32AP7000 features five PIO controllers, PIOA to PIOE, that multiplex the I/O lines of the peripheral set. Each PIO Controller controls up to thirty-two lines.

Each line can be assigned to one of two peripheral functions, A or B. The tables in the following pages define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers.

Note that some output only peripheral functions might be duplicated within the tables.

9.7.1 PIO Controller A Multiplexing

Table 9-9. PIO Controller A Multiplexing

CTBGA256	I/O Line	Peripheral A	Peripheral B
K4	PA00	SPI0 - MISO	SSC1 - RX_FRAME_SYNC
K2	PA01	SPI0 - MOSI	SSC1 - TX_FRAME_SYNC
K3	PA02	SPI0 - SCK	SSC1 - TX_CLOCK
K6	PA03	SPI0 - NPCS[0]	SSC1 - RX_CLOCK
K7	PA04	SPI0 - NPCS[1]	SSC1 - TX_DATA
K1	PA05	SPI0 - NPCS[2]	SSC1 - RX_DATA
A10	PA06	TWI - SDA	USART0 - RTS
C10	PA07	TWI - SCL	USART0 - CTS
L4	PA08	PSIF - CLOCK	USART0 - RXD
L1	PA09	PSIF - DATA	USART0 - TXD
M4	PA10	MCI - CLK	USART0 - CLK
M2	PA11	MCI - CMD	TC0 - CLK0
M5	PA12	MCI - DATA[0]	TC0 - A0
M3	PA13	MCI - DATA[1]	TC0 - A1
M1	PA14	MCI - DATA[2]	TC0 - A2
N4	PA15	MCI - DATA[3]	TC0 - B0
N2	PA16	USART1 - CLK	TC0 - B1
N3	PA17	USART1 - RXD	TC0 - B2
N1	PA18	USART1 - TXD	TC0 - CLK2
P2	PA19	USART1 - RTS	TC0 - CLK1
P1	PA20	USART1 - CTS	SPI0 - NPCS[3]
P3	PA21	SSC0 - RX_FRAME_SYNC	PWM - PWM[2]
R1	PA22	SSC0 - RX_CLOCK	PWM - PWM[3]
R3	PA23	SSC0 - TX_CLOCK	TC1 - A0
T3	PA24	SSC0 - TX_FRAME_SYNC	TC1 - A1
P8	PA25	SSC0 - TX_DATA	TC1 - B0
R8	PA26	SSC0 - RX_DATA	TC1 - B1
K9	PA27	SPI1 - NPCS[3]	TC1 - CLK0
L9	PA28	PWM - PWM[0]	TC1 - A2

Table 9-9. PIO Controller A Multiplexing

M9	PA29	PWM - PWM[1]	TC1 - B2
N9	PA30	PM - GCLK[0]	TC1 - CLK1
R9	PA31	PM - GCLK[1]	TC1 - CLK2

9.7.2 PIO Controller B Multiplexing

Table 9-10. PIO Controller B Multiplexing

CTBGA256	I/O Line	Peripheral A	Peripheral B
E12	PB00	ISI - DATA[0]	SPI1 - MISO
E14	PB01	ISI - DATA[1]	SPI1 - MOSI
E16	PB02	ISI - DATA[2]	SPI1 - NPCS[0]
D13	PB03	ISI - DATA[3]	SPI1 - NPCS[1]
D15	PB04	ISI - DATA[4]	SPI1 - NPCS[2]
D14	PB05	ISI - DATA[5]	SPI1 - SCK
D16	PB06	ISI - DATA[6]	MCI - CMD[1]
C15	PB07	ISI - DATA[7]	MCI - DATA[4]
C16	PB08	ISI - HSYNC	MCI - DATA[5]
C14	PB09	ISI - VSYNC	MCI - DATA[6]
B14	PB10	ISI - PCLK	MCI - DATA[7]
A14	PB11	PSIF - CLOCK[1]	ISI - DATA[8]
C13	PB12	PSIF - DATA[1]	ISI - DATA[9]
A13	PB13	SSC2 - TX_DATA	ISI - DATA[10]
B13	PB14	SSC2 - RX_DATA	ISI - DATA[11]
D12	PB15	SSC2 - TX_CLOCK	USART3 - CTS
A12	PB16	SSC2 - TX_FRAME_SYNC	USART3 - RTS
C12	PB17	SSC2 - RX_FRAME_SYNC	USART3 - TXD
B12	PB18	SSC2 - RX_CLOCK	USART3 - RXD
E11	PB19	PM - GCLK[2]	USART3 - CLK
D11	PB20	ABDAC - DATA[1]	AC97C - SDO
A11	PB21	ABDAC - DATA[0]	AC97C - SYNC
C11	PB22	ABDAC - DATAN[1]	AC97C - SCLK
B11	PB23	ABDAC - DATAN[0]	AC97C - SDI
L6	PB24	NMI_N	DMACA - DMARQ[0]
L2	PB25	EXTINT0	DMACA - DMARQ[1]
T9	PB26	EXTINT1	USART2 - RXD
J9	PB27	EXTINT2	USART2 - TXD
M10	PB28	EXTINT3	USART2 - CLK
R13	PB29	PM - GCLK[3]	USART2 - CTS
P13	PB30	PM - GCLK[4]	USART2 - RTS

9.7.3 PIO Controller C Multiplexing

Table 9-11. PIO Controller C Multiplexing

CTBGA256	I/O Line	Peripheral A	Peripheral B
R14	PC00	MACB0 - COL	
T14	PC01	MACB0 - CRS	
P14	PC02	MACB0 - TX_ER	
T15	PC03	MACB0 - TXD[0]	
R15	PC04	MACB0 - TXD[1]	
H10	PC05	MACB0 - TXD[2]	DMACA - DMARQ[2]
H11	PC06	MACB0 - TXD[3]	DMACA - DMARQ[3]
H14	PC07	MACB0 - TX_EN	
H16	PC08	MACB0 - TX_CLK	
H9	PC09	MACB0 - RXD[0]	
G12	PC10	MACB0 - RXD[1]	
G13	PC11	MACB0 - RXD[2]	
G15	PC12	MACB0 - RXD[3]	
G14	PC13	MACB0 - RX_ER	
G11	PC14	MACB0 - RX_CLK	
G10	PC15	MACB0 - RX_DV	
B16	PC16	MACB0 - MDC	
B15	PC17	MACB0 - MDIO	
D10	PC18	MACB0 - SPEED	
B10	PC19	LCDC - CC	MACB1 - COL
G9	PC20	LCDC - HSYNC	
F9	PC21	LCDC - PCLK	
D9	PC22	LCDC - VSYNC	
A9	PC23	LCDC - DVAL	MACB1 - CRS
C9	PC24	LCDC - MODE	MACB1 - RX_CLK
B9	PC25	LCDC - PWR	
G8	PC26	LCDC - DATA[0]	MACB1 - TX_ER
F8	PC27	LCDC - DATA[1]	MACB1 - TXD[2]
E8	PC28	LCDC - DATA[2]	MACB1 - TXD[3]
D8	PC29	LCDC - DATA[3]	MACB1 - RXD[2]
B8	PC30	LCDC - DATA[4]	MACB1 - RXD[3]
C8	PC31	LCDC - DATA[5]	

9.7.4 PIO Controller D Multiplexing

Table 9-12. PIO Controller D Multiplexing

CTBGA256	I/O Line	Peripheral A	Peripheral B
C2	PD00	LCDC - DATA[6]	
C1	PD01	LCDC - DATA[7]	
D3	PD02	LCDC - DATA[8]	MACB1 - MDIO
H6	PD03	LCDC - DATA[9]	MACB1 - MDC
H5	PD04	LCDC - DATA[10]	MACB1 - RX_DV
H4	PD05	LCDC - DATA[11]	MACB1 - RX_ER
H1	PD06	LCDC - DATA[12]	MACB1 - RXD[1]
H3	PD07	LCDC - DATA[13]	
J7	PD08	LCDC - DATA[14]	
J6	PD09	LCDC - DATA[15]	
R2	PD10	LCDC - DATA[16]	MACB1 - RXD[0]
P4	PD11	LCDC - DATA[17]	MACB1 - TX_EN
T4	PD12	LCDC - DATA[18]	MACB1 - TX_CLK
R4	PD13	LCDC - DATA[19]	MACB1 - TXD[0]
N5	PD14	LCDC - DATA[20]	MACB1 - TXD[1]
T5	PD15	LCDC - DATA[21]	MACB1 - SPEED
P5	PD16	LCDC - DATA[22]	
R5	PD17	LCDC - DATA[23]	

9.7.5 PIO Controller E Multiplexing

Table 9-13. PIO Controller E Multiplexing

CTBGA256	I/O Line	Peripheral A	Peripheral B
C6	PE00	EBI - DATA[16]	LCDC - CC
E6	PE01	EBI - DATA[17]	LCDC - DVAL
A6	PE02	EBI - DATA[18]	LCDC - MODE
D5	PE03	EBI - DATA[19]	LCDC - DATA[0]
B5	PE04	EBI - DATA[20]	LCDC - DATA[1]
E5	PE05	EBI - DATA[21]	LCDC - DATA[2]
C5	PE06	EBI - DATA[22]	LCDC - DATA[3]
A5	PE07	EBI - DATA[23]	LCDC - DATA[4]
D4	PE08	EBI - DATA[24]	LCDC - DATA[8]
B4	PE09	EBI - DATA[25]	LCDC - DATA[9]
C4	PE10	EBI - DATA[26]	LCDC - DATA[10]
A4	PE11	EBI - DATA[27]	LCDC - DATA[11]

Table 9-13. PIO Controller E Multiplexing

B3	PE12	EBI - DATA[28]	LCDC - DATA[12]
A3	PE13	EBI - DATA[29]	LCDC - DATA[16]
C3	PE14	EBI - DATA[30]	LCDC - DATA[17]
A2	PE15	EBI - DATA[31]	LCDC - DATA[18]
B2	PE16	EBI - ADDR[23]	LCDC - DATA[19]
D1	PE17	EBI - ADDR[24]	LCDC - DATA[20]
D2	PE18	EBI - ADDR[25]	LCDC - DATA[21]
T11	PE19	EBI - CFCE1	
M11	PE20	EBI - CFCE2	
P11	PE21	EBI - NCS[4]	
N11	PE22	EBI - NCS[5]	
R11	PE23	EBI - CFRNW	
L11	PE24	EBI - NWAIT	
T10	PE25	EBI - NCS[2]	

9.7.6 IO Pins Without Multiplexing

Many of the external EBI pins are not controlled by the PIO modules, but directly driven by the EBI. These pins have programmable pullup resistors. These resistors are controlled by Special Function Register 4 (SFR4) in the HMATRIX. The pullup on the lines multiplexed with PIO is controlled by the appropriate PIO control register.

This SFR can also control CompactFlash, SmartMedia or NandFlash Support, see the EBI chapter for details

9.7.6.1 HMatrix SFR4 EBI Control Register

Name: HMATRIX_SFR4

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	EBI_DBPUC
7	6	5	4	3	2	1	0
–	–	EBI_CS5A	EBI_CS4A	EBI_CS3A	–	EBI_CS1A	-

- **CS1A: Chip Select 1 Assignment**

0 = Chip Select 1 is assigned to the Static Memory Controller.

1 = Chip Select 1 is assigned to the SDRAM Controller.

- **CS3A: Chip Select 3 Assignment**

0 = Chip Select 3 is only assigned to the Static Memory Controller and NCS3 behaves as defined by the SMC.

1 = Chip Select 3 is assigned to the Static Memory Controller and the NAND Flash/SmartMedia Logic is activated.

- **CS4A: Chip Select 4 Assignment**

0 = Chip Select 4 is assigned to the Static Memory Controller and NCS4, NCS5 and NCS6 behave as defined by the SMC.

1 = Chip Select 4 is assigned to the Static Memory Controller and the CompactFlash Logic is activated.

- **CS5A: Chip Select 5 Assignment**

0 = Chip Select 5 is assigned to the Static Memory Controller and NCS4, NCS5 and NCS6 behave as defined by the SMC.

1 = Chip Select 5 is assigned to the Static Memory Controller and the CompactFlash Logic is activated.

Accessing the address space reserved to NCS5 and NCS6 may lead to an unpredictable outcome.

- **EBI_DBPUC: EBI Data Bus Pull-up Control**

0: EBI D[15:0] are internally pulled up to the VDDIO power supply. The pull-up resistors are enabled after reset.

1: EBI D[15:0] are not internally pulled up.

Table 9-14. IO Pins without multiplexing

I/O Line	Function
PX00	EBI - DATA[0]
PX01	EBI - DATA[1]
PX02	EBI - DATA[2]
PX03	EBI - DATA[3]
PX04	EBI - DATA[4]
PX05	EBI - DATA[5]
PX06	EBI - DATA[6]
PX07	EBI - DATA[7]
PX08	EBI - DATA[8]
PX09	EBI - DATA[9]
PX10	EBI - DATA[10]
PX11	EBI - DATA[11]
PX12	EBI - DATA[12]
PX13	EBI - DATA[13]
PX14	EBI - DATA[14]
PX15	EBI - DATA[15]
PX16	EBI - ADDR[0]
PX17	EBI - ADDR[1]
PX18	EBI - ADDR[2]
PX19	EBI - ADDR[3]
PX20	EBI - ADDR[4]
PX21	EBI - ADDR[5]
PX22	EBI - ADDR[6]
PX23	EBI - ADDR[7]
PX24	EBI - ADDR[8]
PX25	EBI - ADDR[9]
PX26	EBI - ADDR[10]
PX27	EBI - ADDR[11]
PX28	EBI - ADDR[12]
PX29	EBI - ADDR[13]
PX30	EBI - ADDR[14]
PX31	EBI - ADDR[15]

Table 9-14. IO Pins without multiplexing (Continued)

PX32	EBI - ADDR[16]
PX33	EBI - ADDR[17]
PX34	EBI - ADDR[18]
PX35	EBI - ADDR[19]
PX36	EBI - ADDR[20]
PX37	EBI - ADDR[21]
PX38	EBI - ADDR[22]
PX39	EBI - NCS[0]
PX40	EBI - NCS[1]
PX41	EBI - NCS[3]
PX42	EBI - NRD
PX43	EBI - NWE0
PX44	EBI - NWE1
PX45	EBI - NWE3
PX46	EBI - SDCK
PX47	EBI - SDCKE
PX48	EBI - RAS
PX49	EBI - CAS
PX50	EBI - SDWE
PX51	EBI - SDA10
PX52	EBI - NANDOE
PX53	EBI - NANDWE

9.8 Peripheral overview

9.8.1 External Bus Interface

- Optimized for Application Memory Space support
- Integrates Three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional Logic for NAND Flash/SmartMedia™ and CompactFlash™ Support
  - SmartMedia support: 8-bit as well as 16-bit devices are supported
  - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and _ATA SEL (True IDE mode) are not handled.
- Optimized External Bus:
  - 16- or 32-bit Data Bus
  - Up to 26-bit Address Bus, Up to 64-Mbytes Addressable
  - Optimized pin multiplexing to reduce latencies on External Memories
- Up to 6 Chip Selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash/SmartMedia™ Support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash™ Support

9.8.2 Static Memory Controller

- 6 Chip Selects Available
- 64-Mbyte Address Space per Chip Select
- 8-, 16- or 32-bit Data Bus
- Word, Halfword, Byte Transfers
- Byte Write or Byte Select Lines
- Programmable Setup, Pulse And Hold Time for Read Signals per Chip Select
- Programmable Setup, Pulse And Hold Time for Write Signals per Chip Select
- Programmable Data Float Time per Chip Select
- Compliant with LCD Module
- External Wait Request
- Automatic Switch to Slow Clock Mode
- Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes

9.8.3 SDRAM Controller

- Numerous Configurations Supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with Two or Four Internal Banks
  - SDRAM with 16- or 32-bit Data Path
- Programming Facilities
  - Word, Half-word, Byte Access
  - Automatic Page Break When Memory Boundary Has Been Reached
  - Multibank Ping-pong Access
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable

- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported
  - Supports Mobile SDRAM Devices
- Error Detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by Software
- CAS Latency of 1, 2, 3 Supported
- Auto Precharge Command Not Used

9.8.4 Error Corrected Code Controller

- Hardware Error Corrected Code (ECC) Generation
  - Detection and Correction by Software
- Supports NAND Flash and SmartMedia™ Devices with 8- or 16-bit Data Path.
- Supports NAND Flash/SmartMedia with Page Sizes of 528, 1056, 2112 and 4224 Bytes, Specified by Software

9.8.5 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash™ and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

9.8.6 Two-wire Interface

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

9.8.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes 46
  - Remote Loopback, Local Loopback, Automatic Echo

9.8.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

9.8.9 AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Capable to Interface with a Single Analog Front end
- Three independent RX Channels and three independent TX Channels
  - One RX and one TX channel dedicated to the AC97 Analog Front end control
  - One RX and one TX channel for data transfers, connected to the DMACA
  - One RX and one TX channel for data transfers, connected to the DMACA
- Time Slot Assigner allowing to assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20 bit sample length - Variable sampling rate AC97 Codec Interface (48KHz and below)

9.8.10 Audio Bitstream DAC

- Digital Stereo DAC
- Oversampled D/A conversion architecture
  - Oversampling ratio fixed 128x
  - FIR equalization filter
  - Digital interpolation filter: Comb4
  - 3rd Order Sigma-Delta D/A converters
- Digital bitstream outputs
- Parallel interface
- Connected to DMA Controller for background transfer without CPU intervention

9.8.11 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

9.8.12 Pulse Width Modulation Controller

- 4 channels, one 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock
  - Independent Period and Duty Cycle, with Double Bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

9.8.13 MultiMedia Card Interface

- 2 double-channel MultiMedia Card Interface, allowing concurrent transfers with 2 cards
- Compatibility with MultiMedia Card Specification Version 2.2
- Compatibility with SD Memory Card Specification Version 1.0
- Compatibility with SDIO Specification Version V1.0.
- Cards clock rate up to Master Clock divided by 2
- Embedded power management to slow down clock rate when not used
- Each MCI has two slot, each supporting
  - One slot for one MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
- Support for stream, block and multi-block data read and write

9.8.14 PS/2 Interface

- Peripheral Bus slave
- PS/2 Host
- Receive and transmit capability
- Parity generation and error detection
- Overrun error detection

9.8.15 USB Interface

- Supports Hi (480Mbps) and Full (12Mbps) speed communication
- Compatible with the USB 2.0 specification
- UTMI Compliant
- 7 Endpoints
- Embedded Dual-port RAM for Endpoints
- Suspend/Resume Logic (Command of UTMI)
- Up to Three Memory Banks for Endpoints (Not for Control Endpoint)
- 4 KBytes of DPRAM

9.8.16 LCD Controller

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048x2048
- 2D-DMA Controller for management of virtual Frame Buffer
  - Allows management of frame buffer larger than the screen size and moving the view over this virtual frame buffer
- Automatic resynchronization of the frame buffer pointer to prevent flickering
- Configurable coefficients with flexible fixed-point representation.

9.8.17 Ethernet MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data in

9.8.18 Image Sensor Interface

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats
- Preview scaler to generate smaller size image 50
- Programmable frame capture rate

10. Power Manager (PM)

Rev: 1.0.2.8

10.1 Features

- **Controls oscillators and PLLs**
- **Generates clocks and resets for digital logic**
- **Supports 2 high-speed crystal oscillators**
- **Supports 2 PLLs**
- **Supports 32KHz ultra-low power oscillator**
- **On-the fly frequency change of CPU, HSB, and PB frequency**
- **Sleep modes allow simple disabling of logic clocks, PLL's and oscillators**
- **Module-level clock gating through maskable peripheral clocks**
- **Wake-up from interrupts or external pin**
- **Generic clocks with wide frequency range provided**
- **Automatic identification of reset sources**

10.2 Description

The Power Manager (PM) controls the oscillators, PLL's, and generates the clocks and resets in the device. The PM controls two fast crystal oscillators, as well as two PLL's, which can multiply the clock from either oscillator to provide higher frequencies. Additionally, a low-power 32KHz oscillator is used to generate a slow clock for real-time counters.

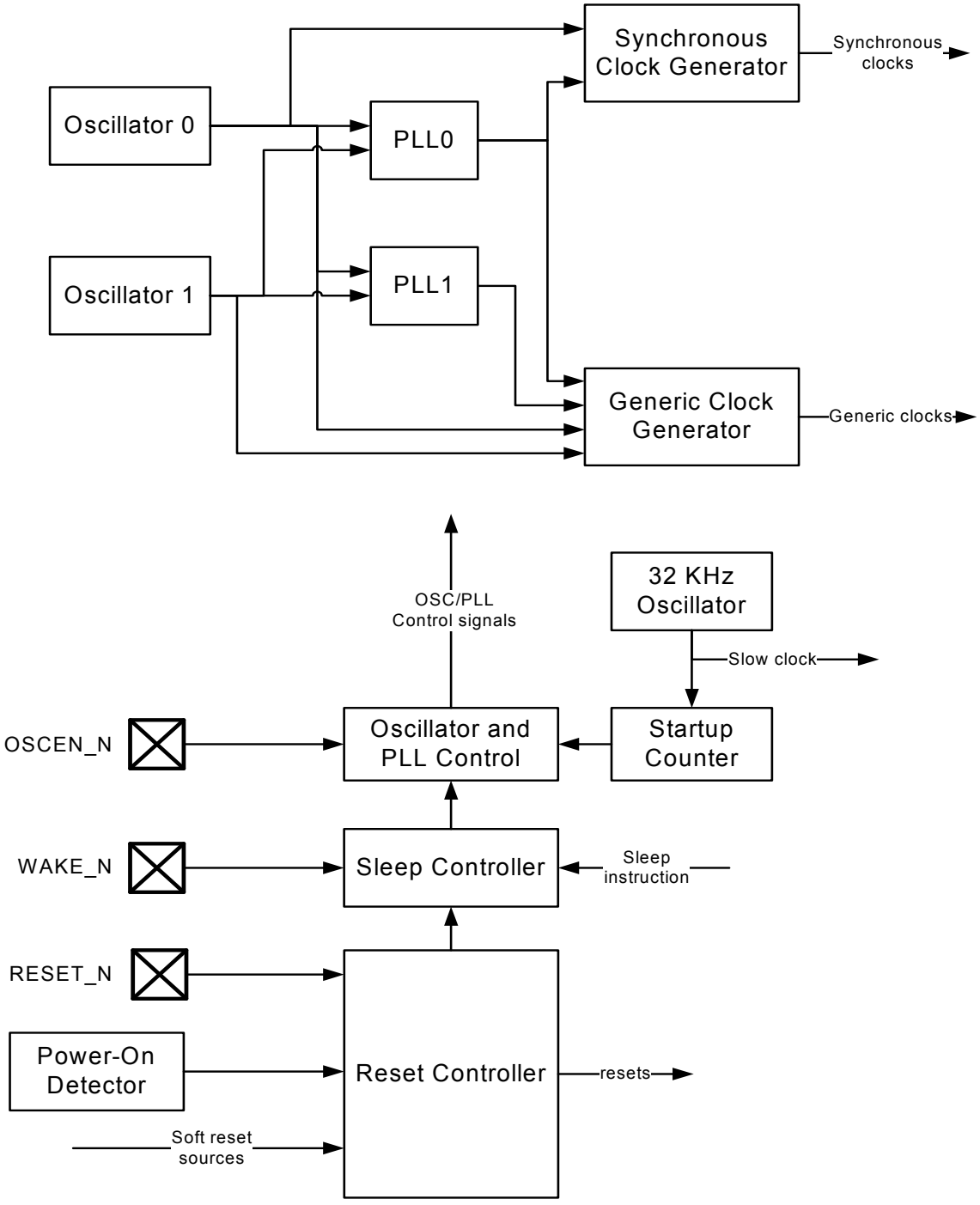
The provided clocks are divided into synchronous and generic clocks. The synchronous clocks are used to clock the main digital logic in the device, namely the CPU, and the modules and peripherals connected to the HSB, PBA, and PBB buses. The generic clocks are asynchronous clocks, which can be tuned precisely within a wide frequency range, which makes them suitable for peripherals that require specific frequencies, such as timers and communication modules.

The PM also contains advanced power-saving features, allowing the user to optimize the power consumption for an application. The synchronous clocks are divided into four clock domains, for the CPU, and modules on the HSB, PBA, and PBB buses. The four clocks can run at different speeds, so the user can save power by running peripherals at a relatively low clock, while maintaining a high CPU performance. Additionally, the clocks can be independently changed on-the fly, without halting any peripherals. This enables the user to adjust the speed of the CPU and memories to the dynamic load of the application, without disturbing or re-configuring active peripherals.

Each module also has a separate clock, enabling the user to switch off the clock for inactive modules, to save further power. Additionally, clocks and oscillators can be automatically swithced off during idle periods by using the sleep instruction on the CPU. The system will return to normal on occurence of interrupts or an event on the WAKE_N pin.

The Power Manager also cointains a Reset Controller, which collects all possible reset sources, generates hard and soft resets, and allows the reset source to be identifed by software.

10.3 Block Diagram



10.4 Product Dependencies

10.4.1 I/O Lines

The PM provides a number of generic clock outputs, which can be connected to output pins, multiplexed with PIO lines. The programmer must first program the PIO controller to assign these pins to their peripheral function. If the I/O pins of the PM are not used by the application, they can be used for other purposes by the PIO controller.

The PM also has a dedicated WAKE_N pin, as well as a number of pins for oscillators and PLL's, which do not require the PIO controller to be programmed.

10.4.2 Interrupt

The PM interrupt line is connected to one of the internal sources of the interrupt controller. Using the PM interrupt requires the interrupt controller to be programmed first.

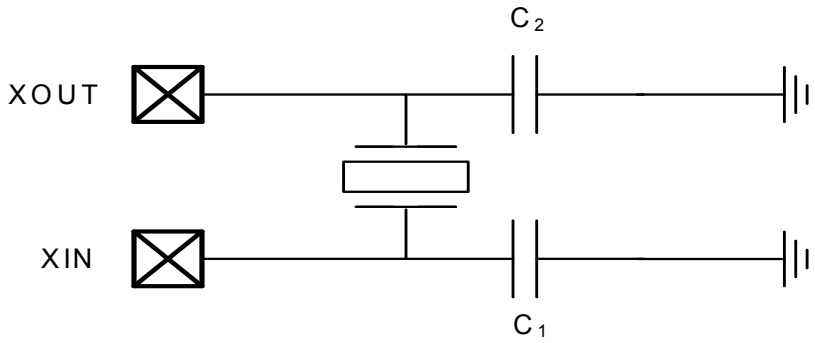
10.5 Functional Description

10.5.1 Oscillator 0 and 1 operation

The two main oscillators are designed to be used with an external high frequency crystal, as shown in Figure 10-1. See Electrical Characteristics for the allowed frequency range. The main oscillators are enabled by default after reset, and are only switched off in sleep modes, as described in Section 10.5.6 on page 104. After a power-on reset, or when waking up from a sleep mode that disabled the main oscillators, the oscillators need 128 slow clock cycles to stabilize on the correct frequency. (1) The PM masks the main oscillator outputs during this start-up period, to ensure that no unstable clocks propagate to the digital logic.

The oscillators can be bypassed by pulling the OSCEN_N pin high. This disables the oscillators, and an external clock must be applied on XIN. No start-up time applies to this clock.

Figure 10-1. Oscillator connections



Typ. values: $C_2 = C_2 = 22$ pF

10.5.2 32 KHz oscillator operation

The 32 KHz oscillator operates similarly to Oscillator 0 and 1 described above, and is used to generate the slow clock in the device. A 32768 Hz crystal must be connected between XIN32 and XOUT32 as shown in Figure 10-1. The 32 KHz oscillator is is an ultra-low power design, and remains enabled in all sleep modes except static mode, as described in Section 10.5.6 on page

1. When waking up from Stop mode using external interrupts, the startup time is 32768 slow clock cycles.

104. The oscillator has a rather long start-up time of 32768 clock cycles, and no clocks will be generated in the device during this start-up time.

Note that in static sleep mode the startup counter will start at the negedge of reset and not at the posedge.

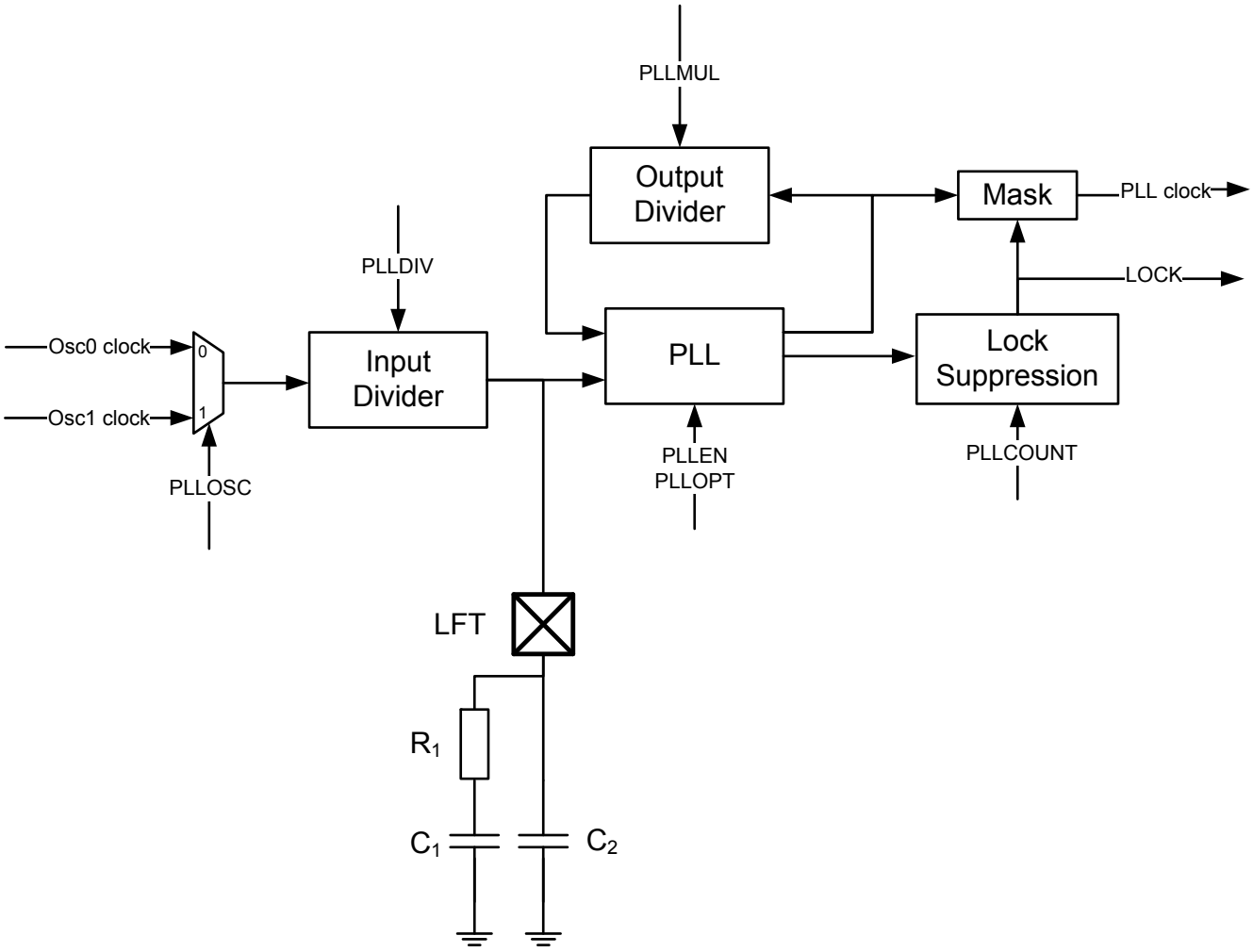
Pulling OSCEN_N high will also disable the 32 KHz oscillator, and a 32 KHz clock must be applied on the XIN32 pin. No start-up time applies to this clock.

10.5.3 PLL operation

The device contains two PLL's, PLL0 and PLL1. These are disabled by default, but can be enabled to provide high frequency source clocks for synchronous or generic clocks. The PLL's can take either Oscillator 0 or 1 as clock source. Each PLL has an input divider, which divides the source clock, creating the reference clock for the PLL. The PLL output is divided by a user-defined factor, and the PLL compares the resulting clock to the reference clock. The PLL will adjust its output frequency until the two compared clocks are equal, thus locking the output frequency to a multiple of the reference clock frequency.

When the PLL is switched on, or when changing the clock source or multiplication or division factor for the PLL, the PLL is unlocked and the output frequency is undefined. The PLL clock for the digital logic is automatically masked when the PLL is unlocked, to prevent connected digital logic from receiving a too high frequency and thus become unstable.

Figure 10-2. PLL with control logic and filters



10.5.3.1 Enabling the PLL

PLLn is enabled by writing the PLLEN bit in the PLLn register. PLLOSC selects Oscillator 0 or 1 as clock source. The PLLDIV and PLLMUL bitfields must be written with the division and multiplication factor, respectively, creating the PLL frequency:

$$f_{PLL} = (PLLMUL+1) / (PLLDIV+1) \bullet f_{OSC}$$

The LOCKn flag in ISR is set when PLLn becomes locked. The bit will stay high until cleared by writing 1 to ICR:LOCKn. The Power Manager interrupt can be triggered by writing IER:LOCKn to 1.

Note that the input frequency for the PLL must be within the range inidicated in the Electrical Characteristics chapter. The input frequency for the PLL relates to the oscillator frequency and PLLDIV setting as follows:

$$f_{PLLIN} = 2 \bullet f_{OSC} / (PLLDIV+1)\bullet$$

10.5.3.2 *Lock suppression*

When using high division or multiplication factors, there is a possibility that the PLL can give false lock indications while sweeping to the correct frequency. To prevent false lock indications from setting the LOCKn flag, the lock indication can be suppressed for a number of slow clock cycles indicated in the PLLn:COUNT field. Typical start-up times can be found using the Atmel filter caluclator (see below).

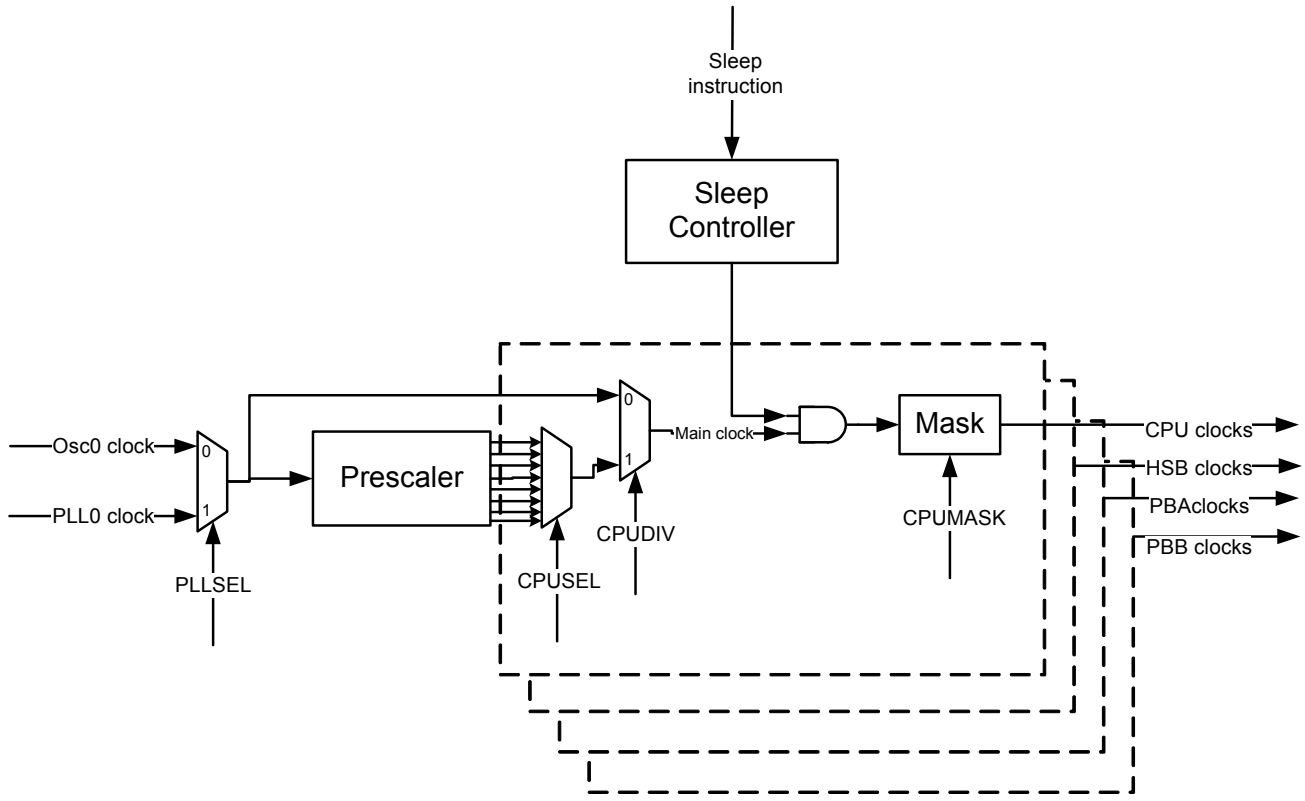
10.5.3.3 *Operating range selection*

To use PLLn, a passive RC filter should be connected to the LFTn pin, as shown in Figure 10-2. Filter values depend on the PLL reference and output frequency range. Atmel provides a tool named “Atmel PLL LFT Filter Calculator AT91”. The PLL for AT32AP7000 can be selected in this tool by selecting “AT91RM9200 (58A07F)” and leave “Icp = ‘1’” (default).

10.5.4 Synchronous clocks

Oscillator 0 (default) or PLL0 provides the source for the main clocks, which is the common root for the synchronous clocks for the CPU, and HSB, PBA, and PBB modules. The main clock is divided by an 8-bit prescaler, and each of these four synchronous clocks can run from any tapping of this prescaler, or the undivided main clock, as long as $f_{CPU} \geq f_{HSB} \geq f_{PBx}$ and $f_{PBB}=f_{HSB}$. The synchronous clock source can be changed on-the fly, responding to varying load in the application. The clock domains can be shut down in sleep mode, as described in ”Sleep modes” on page 104. Additionally, the clocks for each module in the four domains can be individually masked, to avoid power consumption in inactive modules.

Figure 10-3. Synchronous clock generation



10.5.4.1 Selecting PLL or oscillator for the main clock

The common main clock can be connected to Oscillator 0 or PLL0. By default, the main clock will be connected to the Oscillator 0 output. The user can connect the main clock to the PLL0 output by writing the PLLSEL bit in the Main Clock Control Register (MCCTRL) to 1. This must only be done after PLL0 has been enabled, otherwise a deadlock will occur. Care should also be taken that the new frequency of the synchronous clocks does not exceed the maximum frequency for each clock domain.

10.5.4.2 Selecting synchronous clock division ratio

The main clock feeds an 8-bit prescaler, which can be used to generate the synchronous clocks. By default, the synchronous clocks run on the undivided main clock. The user can select a prescaler division for the CPU clock by writing CKSEL:CPUDIV to 1 and CPUSEL to the prescaling value, resulting in a CPU clock frequency:

$$f_{CPU} = f_{main} / 2^{(CPUSEL+1)}$$

Similarly, the clock for HSB, PBA, and PBB can be divided by writing their respective bitfields. To ensure correct operation, frequencies must be selected so that $f_{CPU} \geq f_{HSB} \geq f_{PBA,B}$. Also, frequencies must never exceed the specified maximum frequency for each clock domain.

CKSEL can be written without halting or disabling peripheral modules. Writing CKSEL allows a new clock setting to be written to all synchronous clocks at the same time. It is possible to keep one or more clocks unchanged by writing the same value a before to the xxxDIV and xxxSEL bitfields. This way, it is possible to e.g. scale CPU and HSB speed according to the required performance, while keeping the PBA and PBB frequency constant.

10.5.4.3 Clock Ready flag

There is a slight delay from CKSEL is written and the new clock setting becomes effective. During this interval, the Clock Ready (CKRDY) flag in ISR will read as 0. If IER:CKRDY is written to 1, the Power Manager interrupt can be triggered when the new clock setting is effective. CKSEL must not be re-written while CKRDY is 0, or the system may become unstable or hang.

10.5.5 Peripheral clock masking

By default, the clock for all modules are enabled, regardless of which modules are actually being used. It is possible to disable the clock for a module in the CPU, HSB, PBA, or PBB clock domain by writing the corresponding bit in the Clock Mask register (CPU/HSB/PBA/PBB) to 0. When a module is not clocked, it will cease operation, and its registers cannot be read or written. The module can be re-enabled later by writing the corresponding mask bit to 1.

A module may be connected to several clock domains, in which case it will have several mask bits.

Table 10-1 contains a list of implemented maskable clocks.

10.5.5.1 Cautionary note

Note that clocks should only be switched off if it is certain that the module will not be used. Switching off the clock for the internal RAM will cause a problem if the stack is mapped there. Switching off the clock to the Power Manager (PM), which contains the mask registers, or the corresponding PB bridge, will make it impossible to write the mask registers again. In this case, they can only be re-enabled by a system reset.

10.5.5.2 Mask Ready flag

Due to synchronization in the clock generator, there is a slight delay from a mask register is written until the new mask setting goes into effect. When clearing mask bits, this delay can usually be ignored. However, when setting mask bits, the registers in the corresponding module must not be written until the clock has actually be re-enabled. The status flag MSKRDY in ISR provides the required mask status information. When writing either mask register with any value, this bit is cleared. The bit is set when the clocks have been enabled and disabled according to the new mask setting. Optionally, the Power Manager interrupt can be enabled by writing the MSKRDY bit in IER.

Table 10-1. Maskable module clocks in AT32AP7000.

Bit	CPUMASK	HSBMASK	PBAMASK	PBBMASK
0	PICO	EBI	SPI0	PM/EIC/RTC/WDT
1	-	PBA	SPI1	INTC
2	-	PBB	TWI	HMATRIX
3	-	HRAMC	USART0	TC0
4	-	HSB-HSB Bridge	USART1	TC1
5	-	ISI	USART2	PWM
6	-	USB	USART3	MACB0
7	-	LCDC	SSC0	MACB1
8	-	MACB0	SSC1	DAC
9	-	MACB1	SSC2	MCI
10	-	DMA	PIOA	AC97C
11	-	-	PIOB	ISI
12	-	-	PIOC	USB
13	-	-	PIOD	SMC
14	-	-	PIOE	SDRAMC
15	-	-	PSIF	ECC
16	-	-	PDC	-
31:17	-	-	-	-

10.5.6 Sleep modes

In normal operation, all clock domains are active, allowing software execution and peripheral operation. When the CPU is idle, it is possible to switch off the CPU clock and optionally other clock domains to save power. This is activated by the sleep instruction, which takes the sleep mode index number as argument.

10.5.6.1 Entering and exiting sleep modes

The sleep instruction will halt the CPU and all modules belonging to the stopped clock domains. The modules will be halted regardless of the bit settings of the mask registers.

Oscillators and PLL's can also be switched off to save power. These modules have a relatively long start-up time, and are only switched off when very low power consumption is required.

The CPU and affected modules are restarted when the sleep mode is exited. This occurs when an interrupt triggers, or the WAKE_N pin is asserted. Note that even though an interrupt is enabled in sleep mode, it may not trigger if the source module is not clocked.

10.5.6.2 Supported sleep modes

The following sleep modes are supported. These are detailed in Table 10-2.

•Idle: The CPU is stopped, the rest of the chip is operating. Wake-up sources are any interrupt, or WAKE_N pin.

•Frozen: The CPU and HSB modules are stopped, peripherals are operating. Wake-up sources are any interrupt from PB modules, or WAKE_N pin.

•Standby: All synchronous clocks are stopped, but oscillators and PLL's are running, allowing quick wake-up to normal mode. Wake-up sources are RTC or external interrupt, or WAKE_N pin.

•Stop: As Standby, but Oscillator 0 and 1, and the PLL's are stopped. 32 KHz oscillator and RTC/WDT still operates. Wake-up sources are RTC or external interrupt, or WAKE_N pin.

•Static: All oscillators and clocks are stopped. Wake-up sources are external interrupt or WAKE_N pin.•

Table 10-2. Sleep modes

Index	Sleep Mode	CPU	HSB	PBA,B + GCLK	Osc0,1 + PLL0,1	Osc32 + RTC/WDT
0	Idle	Off	On	On	On	On
1	Frozen	Off	Off	On	On	On
2	Standby	Off	Off	Off	On	On
3	Stop	Off	Off	Off	Off	On
5	Static	Off	Off	Off	Off	Off

10.5.6.3 Precautions when entering sleep mode

Modules communicating with external circuits should normally be disabled before entering a sleep mode that will stop the module operation. This prevents erratic behavior when entering or exiting sleep mode. Please refer to the relevant module documentation for recommended actions.

Communication between the synchronous clock domains is disturbed when entering and exiting sleep modes. This means that bus transactions are not allowed between clock domains affected by the sleep mode. The system may hang if the bus clocks are stopped in the middle of a bus transaction.

The CPU and caches are automatically stopped in a safe state to ensure that all CPU bus operations are complete when the sleep mode goes into effect. Thus, when entering Idle mode, no further action is necessary.

When entering a deeper sleep mode than Idle mode, all other HSB masters must be stopped before entering the sleep mode. Also, if there is a chance that any PB write operations are incomplete, the CPU should perform a read operation from any register on the PB bus before executing the sleep instruction. This will stall the CPU while waiting for any pending PB operations to complete.

The Power manager will normally turn of all debug related clocks in the system in the static sleep mode, making it impossible for a debugger to communicate with the system. If a

NEXUS_ACCESS or a MEMORY_ACCESS JTAG command is loaded into the instruction register before entering sleep mode some clocks are left running to enable debugging of the system. This will increase the power consumption of the device. If the part entered static mode without a NEXUS_ACCESS ot MEMORY_ACCESS instruction loaded into the JTAG instruction register an external reset is the only way for the debugger to get the part out of the sleep mode.

When not debugging a program and using sleep modes the JTAG should always have the IDCODE instruction loaded into the JTAG instruction register and the OCD system should be disabled. Otherwise some clocks may be left running, increasing the power consumption.

10.5.7 Generic clocks

Timers, communication modules, and other modules connected to external circuitry may require specific clock frequencies to operate correctly. The Power Manager contains an implementation defined number of generic clocks, that can provide a wide range of accurate clock frequencies.

Each generic clock module runs from either Oscillator 0 or 1, or PLL0 or 1. The selected source can optionally be divided by any even integer up to 512. Each clock can be independently enabled and disabled, and is also automatically disabled along with peripheral clocks by the Sleep Controller.

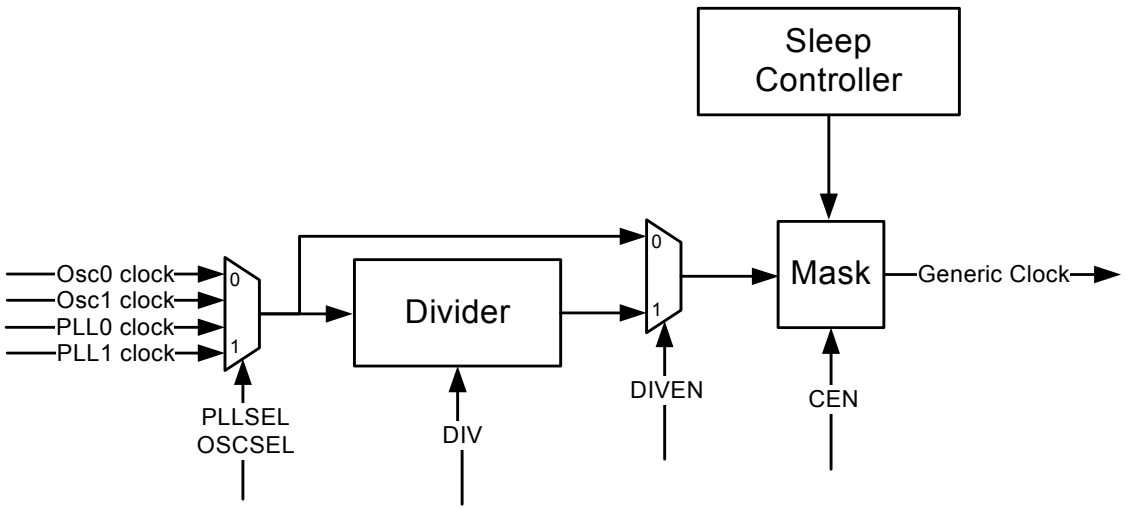


Figure 10-4. Generic clock generation

10.5.7.1 Enabling a generic clock

A generic clock is enabled by writing the CEN bit in GCCTRL to 1. Each generic clock can use either Oscillator 0 or 1 or PLL0 or 1 as source, as selected by the PLLSEL and OSCSEL bits. The source clock can optionally be divided by writing DIVEN to 1 and the division factor to DIV, resulting in the output frequency:

$$f_{GCLK} = f_{SRC} / (2*(DIV+1))$$

10.5.7.2 *Disabling a generic clock*

The generic clock can be disabled by writing CEN to 0 or entering a sleep mode that disables the PB clocks. In either case, the generic clock will be switched off on the first falling edge after the disabling event, to ensure that no glitches occur. If CEN is written to 0, the bit will still read as 1 until the next falling edge occurs, and the clock is actually switched off. When writing CEN to 0, the other bits in GCCTRL should not be changed until CEN reads as 0, to avoid glitches on the generic clock.

When the clock is disabled, both the prescaler and output are reset.

10.5.7.3 *Changing clock frequency*

When changing generic clock frequency by writing GCCTRL, the clock should be switched off by the procedure above, before being re-enabled with the new clock source or division setting. This prevents glitches during the transition.

10.5.7.4 *Generic clock implementation*

In AT32AP7000, there are 8 generic clocks. These are allocated to different functions as shown in Table 10-3.

Table 10-3. Generic clock allocation

Clock number	Function
0	GCLK0 pin
1	GCLK1 pin
2	GCLK2 pin
3	GCLK3 pin
4	GCLK4 pin
5	Reserved for internal use
6	DAC
7	LCD Controller

10.5.8 Divided PB clocks

The clock generator in the Power Manager provides divided PBA and PBB clocks for use by peripherals that require a prescaled PB clock. This is described in the documentation for the relevant modules.

The divided clocks are not directly maskable, but are stopped in sleep modes where the PB clocks are stopped.

10.5.9 Debug operation

During a debug session, the user may need to halt the system to inspect memory and CPU registers. The clocks normally keep running during this debug operation, but some peripherals may require the clocks to be stopped, e.g. to prevent timer overflow, which would cause the program to fail. For this reason, peripherals on the PBA and PBB buses may use “debug qualified” PB clocks. This is described in the documentation for the relevant modules. The divided PB clocks are always debug qualified clocks.

Debug qualified PB clocks are stopped during debug operation. The debug system can optionally keep these clocks running during the debug operation. This is described in the documentation for the On-Chip Debug system.

10.5.10 Reset Controller

The Reset Controller collects the various reset sources in the system and generates hard and soft resets for the digital logic.

The device contains a Power-On Detector, which keeps the system reset until power is stable. This eliminates the need for external reset circuitry to guarantee stable operation when powering up the device.

It is also possible to reset the device by asserting the RESET_N pin. This pin has an internal pull-up, and does not need to be driven externally when negated.

Table 10-4 lists these and other reset sources supported by the Reset Controller.

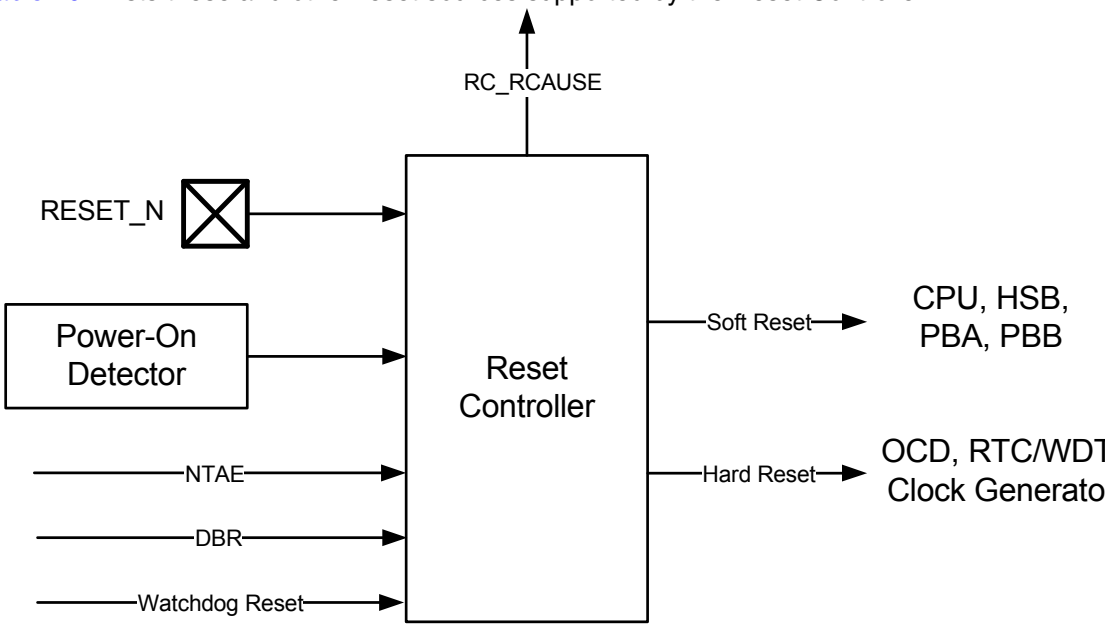


Figure 10-5. Reset Controller block diagram

Reset sources are divided into hard and soft resets. Hard resets imply that the system could have become unstable, and virtually all logic will be reset. The clock generator, which also controls the oscillators, will also be reset. If the device is reset due to a power-on reset, or reset occurred when the device was in a sleep mode that disabled the oscillators, the normal oscillator startup time will apply.

A soft reset will reset most digital logic in the device, such as CPU, HSB, and PB modules, but not the OCD system, clock generator, Watchdog Timer and RTC, allowing some functions, including the oscillators, to remain active during the reset. The startup time from a soft reset is thus negligible. Note that all PB registers are reset, except those in the RTC/WDT. The MCCTRL and CKSEL registers are reset, and the device will restart using Oscillator 0 as clock source for all synchronous clocks.

In addition to the listed reset types, the JTAG can keep parts of the device statically reset through the JTAG Reset Register. See JTAG documentation for details.

The cause of the last reset can be read from the RC_RCAUSE register. This register contains one bit for each reset source, and can be identified during the boot sequence of an application to determine the proper action to be taken.

Table 10-4. Reset types

Reset source	Description	Type
Power-on Reset	Supply voltage below the power-on reset detector threshold voltage	Hard
External	RESET_N pin asserted	Hard
NanoTrace Access Error	See On-Chip Debug documentation.	Soft
Watchdog Timer	See watchdog timer documentation.	Soft
OCD	See On-Chip Debug documentation	Soft

10.6 User Interface

Offset	Register	Register Name	Access	Reset
0x00	Main Clock Control	MCCTRL	Read/Write	0x0
0x04	Clock Select	CKSEL	Read/Write	0x0
0x08	CPU Clock Mask	CPUMASK	Read/Write	Impl. defined
0x0C	HSB Clock Mask	HSBMASK	Read/Write	Impl. defined
0x10	PBA Clock Mask	PBAMASK	Read/Write	Impl. defined
0x14	PBB Clock Mask	PBBMASK	Read/Write	Impl. defined
0x20	PLL0 Control	PLL0	Read/Write	0x0
0x24	PLL1 Control	PLL1	Read/Write	0x0
0x40	Interrupt Enable	IER	Write-only	0x0
0x44	Interrupt Disable	IDR	Write-only	0x0
0x48	Interrupt Mask	IMR	Read-only	0x0
0x4C	Interrupt Status	ISR	Read-only	0x0
0x50	Interrupt Clear	ICR	Write-only	0x0
0x60	Generic Clock Control 0	GCCTRL0	Read/Write	0x0
0x64	Generic Clock Control 1	GCCTRL1	Read/Write	0x0
0x68	Generic Clock Control 2	GCCTRL2	Read/Write	0x0
0x6C	Generic Clock Control 3	GCCTRL3	Read/Write	0x0
0x70	Generic Clock Control 4	GCCTRL4	Read/Write	0x0
0x74	Generic Clock Control 5	GCCTRL5	Read/Write	0x0
0x78	Generic Clock Control 6	GCCTRL6	Read/Write	0x0
0x7C	Generic Clock Control 7	GCCTRL7	Read/Write	0x0
0x80 - 0xBC	Reserved			
0xC0	Reset Cause	RCAUSE	Read	

10.6.1 Main Clock Control

Name: MCCTRL

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	PLLSEL	-

- **PLLSEL: PLL Select**
  0: Oscillator 0 is source for the main clock
  1: PLL0 is source for the main clock

10.6.2 Clock Select

Name: CKSEL

Access Type: Read/Write

31	30	29	28	27	26	25	24
PBBDIV	-	-	-	-	PBBSEL		

23	22	21	20	19	18	17	16
PBADIV	-	-	-	-	PBASEL		

15	14	13	12	11	10	9	8
HSBDIV	-	-	-	-	HSBSEL		

7	6	5	4	3	2	1	0
CPUDIV	-	-	-	-	CPUSEL		

- **PBBDIV, PBBSEL: PBB Division and Clock Select**
  PBBDIV = 0: PBB clock equals main clock.
  PBBDIV = 1: PBB clock equals main clock divided by $2^{(PBBSEL+1)}$.
- **PBADIV, PBASEL: PBA Division and Clock Select**
  PBADIV = 0: PBA clock equals main clock.
  PBADIV = 1: PBA clock equals main clock divided by $2^{(PBASEL+1)}$.
- **HSBDIV, HSBSEL: HSB Division and Clock Select**
  HSBDIV = 0: HSB clock equals main clock.
  HSBDIV = 1: HSB clock equals main clock divided by $2^{(HSBSEL+1)}$.
- **CPUDIV, CPUSEL: CPU Division and Clock Select**
  CPUDIV = 0: CPU clock equals main clock.
  CPUDIV = 1: CPUclock equals main clock divided by $2^{(CPUSEL+1)}$.

Note that if xxxDIV is written to 0, xxxSEL should also be written to 0 to ensure correct operation.

Also note that writing this register clears ISR:CKRDY. The register must not be re-written until CKRDY goes high.

10.6.3 Clock Mask

Name: CPU/HSB/PBA/PBBMASK

Access Type: Read/Write

31	30	29	28	27	26	25	24
MASK[31:24]							

23	22	21	20	19	18	17	16
MASK[23:16]							

15	14	13	12	11	10	9	8
MASK[15:8]							

7	6	5	4	3	2	1	0
MASK[7:0]							

- **MASK: Clock Mask**

  If bit n is cleared, the clock for module n is stopped. If bit n is set, the clock for module n is enabled according to the current power mode. The number of implemented bits in each mask register, as well as which module clock is controlled by each bit, is implementation dependent.

10.6.4 PLL Control

Name: PLL0,1

Access Type: Read/Write

31	30	29	28	27	26	25	24
PLLTEST	-	PLLCOUNT					

23	22	21	20	19	18	17	16
PLLMUL							

15	14	13	12	11	10	9	8
PLLDIV							

7	6	5	4	3	2	1	0
-	-	-	PLLOPT			PLLOSC	PLLEN

- **PLLTEST: PLL Test**

  Reserved for internal use. Always write to 0.
- **PLLCOUNT: PLL Count**

  Specifies the number of slow clock cycles before ISR:LOCKn will be set after PLLn has been written, or after PLLn has been automatically re-enabled after exiting a sleep mode.
- **PLLMUL: PLL Multiply Factor**
- **PLLDIV: PLL Division Factor**

  These bitfields determine the ratio of the PLL output frequency to the source oscillator frequency:

  $f_{PLL} = (PLLMUL+1)/(PLLDIV+1) \bullet f_{OSC}$
- **PLLOPT: PLL Option**

  This field should be written to 100.

  Other values are reserved.
- **PLLOSC: PLL Oscillator Select**

  0: Oscillator 0 is the source for the PLL.

  1: Oscillator 1 is the source for the PLL.
- **PLLEN: PLL Enable**

  0: PLL is disabled.

  1: PLL is enabled.

10.6.5 Interrupt Enable/Disable/Mask/Status/Clear

Name: IER/IDR/IMR/ISR/ICR

Access Type: IER/IDR/ICR: Write-only

IMR/ISR: Read-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MSKRDY	CKRDY	VMRDY	VOK	WAKE	LOCK1	LOCK0

- **MSKRDY: Mask Ready**
  0: Either xxxMASK register has been written, and clocks are not yet enabled or disabled according to the new mask value.
  1: Clocks are enabled and disabled as indicated in the xxxMASK registers.
  Note: Writing ICR:MSKRDY to 1 has no effect.
- **CKRDY: Clock Ready**
  0: The CKSEL register has been written, and the new clock setting is not yet effective.
  1: The synchronous clocks have frequencies as indicated in the CKSEL register.
  Note: Writing ICR:CKRDY to 1 has no effect.
- **VMRDY, VOK**
  These bits are for internal use only. In ISR, the value of these bits is undefined. In IER, these bits should be written to 0.
- **WAKE: Wake Pin Asserted**
  0: The WAKE_N pin is not asserted, or has been asserted for less than one PB clock period.
  1: The WAKE_N pin is asserted for longer than one PB clock period.
- **LOCK1: PLL1 locked**
- **LOCK0: PLL0 locked**
  0: The PLL is unlocked, and cannot be used as clock source.
  1: The PLL is locked, and can be used as clock source.

The effect of writing or reading the bits listed above depends on which register is being accessed:

- **IER (Write-only)**
  0: No effect
  1: Enable Interrupt
- **IDR (Write-only)**
  0: No effect
  1: Disable Interrupt

- **IMR (Read-only)**
  - 0: Interrupt is disabled
  - 1: Interrupt is enabled
- **ISR (Read-only)**
  - 0: An interrupt event has occurred
  - 1: An interrupt even has not occurred
- **ICR (Write-only)**
  - 0: No effect
  - 1: Clear interrupt event

10.6.6 Generic Clock Control

Name: GCCTRL0... GCCTRL7

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
DIV[7:0]							

7	6	5	4	3	2	1	0
-	-	-	DIVEN	-	CEN	PLLSEL	OSCSEL

There is one GCCTRL register per generic clock in the design.

- **DIV: Division Factor**
- **DIVEN: Divide Enable**
  0: The generic clock equals the undivided source clock.
  1: The generic clock equals the source clock divided by 2*(DIV+1).
- **CEN: Clock Enable**
  0: Clock is stopped.
  1: Clock is running.
- **PLLSEL: PLL Select**
  0: Oscillator is source for the generic clock.
  1: PLL is source for the generic clock.
- **OSCSEL: Oscillator Select**
  0: Oscillator (or PLL) 0 is source for the generic clock.
  1: Oscillator (or PLL) 1is source for the generic clock.

10.6.7 Reset Cause

Name: RC_RCAUSE

Access Type: Read-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	SERP	JTAG	WDT	EXT	-	POR

- **SERP: Serious Problem Error**
  This bit is set if a reset occured due to a serious problem in the CPU, like Nanotrace access error, for instance.
- **JTAG: JTAG Reset**
  This bit is set if a reset occurred due to a JTAG reset.
- **WDT: Watchdog Timer**
  This bit is set if a reset occurred due to a timeout of the Watchdog Timer.
- **EXT: External Reset**
  This bit is set if a reset occurred due to assertion of the RESET_N pin.
- **POR: Power-On Detector**
  This bit is set if a reset was caused by the Power-On Detector.

11. Real Time Counter (RTC)

Rev: 1.0.1.1

11.1 Features

- **32-bit real-time counter with 16-bit prescaler**
- **Clocked from 32 kHz oscillator**
- **High resolution: Max count frequency 16KHz**
- **Long delays**
  - **Max timeout 272 years**
- **Extremely low power consumption**
- **Available in all sleep modes except Deepdown**
- **Optional wrap at max value**
- **Interrupt on wrap**

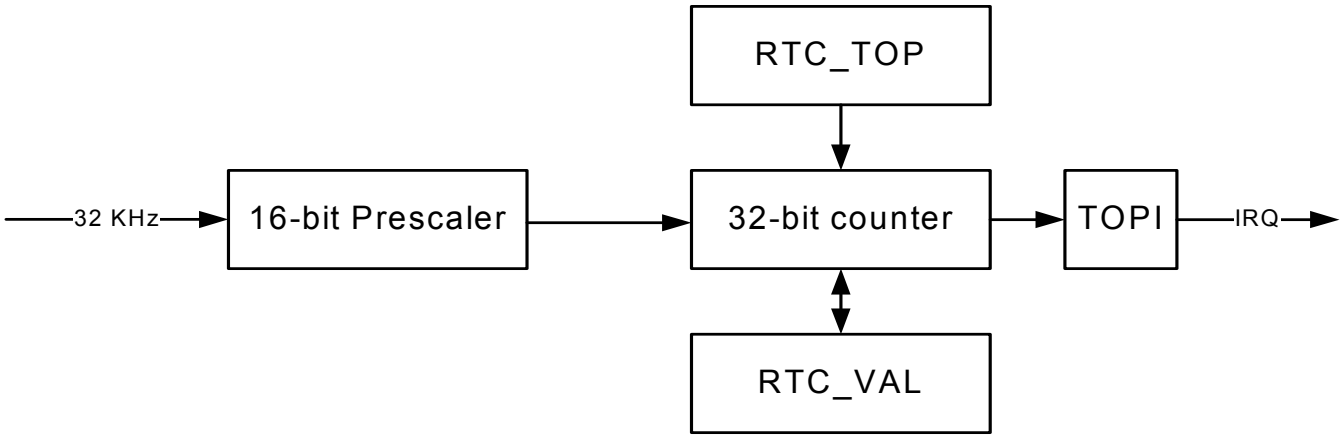
11.2 Description

The Real Time Counter (RTC) enables periodic interrupts at long intervals, or accurate measurement of real-time sequences. The RTC is fed from a 16-bit prescaler, which is clocked from the 32 kHz oscillator. Any tapping of the prescaler can be selected as clock source for the RTC, enabling both high resolution and long timeouts. The prescaler cannot be written directly, but can be cleared by the user.

The RTC can generate an interrupt when the counter wraps around the top value of 0xFFFFFFFF. Optionally, the RTC can wrap at a lower value, producing accurate periodic interrupts.

11.3 Block Diagram

Figure 11-1. Real Time Counter module block diagram



11.4 Product Dependencies

11.4.1 I/O Lines

None.

11.4.2 Power Management

The RTC is continously clocked, and remains operating in all sleep modes except Static.

11.4.3 Interrupt

The RTC interrupt line is connected to one of the internal sources of the interrupt controller. Using the RTC interrupt requires the interrupt controller to be programmed first.

11.4.4 Debug Operation

The RTC prescaler and watchdog timer are frozen during debug operation, unless the OCD system keeps peripherals running in debug operation.

11.5 Functional Description

11.5.1 RTC operation

11.5.1.1 Source clock

The RTC is enabled by writing the EN bit in the CTRL register. This also enables the clock for the prescaler. The PSEL bitfield in the same register selects the prescaler tapping, selecting the source clock for the RTC:

$$f_{RTC} = 2^{-(PSEL+1)} * 32KHz$$

Note that if the RTC is used in stop mode, PSEL must be 2 or higher to ensure no ticks are missed when entering or leaving sleep mode.

11.5.1.2 Counter operation

The RTC count value can be read from or written to the register VAL. The prescaler cannot be written directly, but can be reset by writing the strobe PCLR in CTRL.

When enabled, the RTC will then up-count until it reaches 0xFFFFFFFF, and then wrap to 0x0.

Writing CTRL:TOPEN to one causes the RTC to wrap at the value written to TOP. The status bit TOPI in ISR is set when this occurs.

11.5.1.3 RTC Interrupt

Writing the TOPI bit in IER enables the RTC interrupt, while writing the corresponding bit in IDR disables the RTC interrupt. IMR can be read to see whether or not the interrupt is enabled. If enabled, an interrupt will be generated if the TOPI flag in ISR is set. The flag can be cleared by writing TOPI in ICR to one.

11.6 User Interface

Offset	Register	Register Name	Access	Reset
0x00	RTC Control	CTRL	Read/Write	0x0
0x04	RTC Value	VAL	Read/Write	0x0
0x08	RTC Top	TOP	Read/Write	0x0
0x10	RTC Interrupt Enable	IER	Write-only	0x0
0x14	RTC Interrupt Disable	IDR	Write-only	0x0
0x18	RTC Interrupt Mask	IMR	Read-only	0x0
0x1C	RTC Interrupt Status	ISR	Read-only	0x0
0x20	RTC Interrupt Clear	ICR	Write-only	0x0

11.6.1 RTC Control

Name: CTRL

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	PSEL[3:0]			

7	6	5	4	3	2	1	0
-	-	-	-	-	TOPEN	PCLR	EN

- **PSEL: Prescale Select**
  Selects prescaler bit PSEL as source clock for the RTC.
- **TOPEN: Top Enable**
  0: RTC wraps at 0xFFFFFFFF
  1: RTC wraps at RTC_TOP
- **PCLR: Prescaler Clear**
  Writing this strobe clears the prescaler. Note that this also resets the watchdog timer.
- **EN: Enable**
  0: RTC is disabled
  1: RTC is enabled

11.6.2 RTC Value

Name: VAL

Access Type: Read/Write

31	30	29	28	27	26	25	24
VAL[31:24]							

23	22	21	20	19	18	17	16
VAL[23:16]							

15	14	13	12	11	10	9	8
VAL[15:8]							

7	6	5	4	3	2	1	0
VAL[7:0]							

- **VAL: RTC Value**
  This value is incremented on every rising edge of the source clock.

11.6.3 RTC Top

Name: TOP

Access Type: Read/Write

31	30	29	28	27	26	25	24
TOP[31:24]							

23	22	21	20	19	18	17	16
TOP[23:16]							

15	14	13	12	11	10	9	8
TOP[15:8]							

7	6	5	4	3	2	1	0
TOP[7:0]							

- **TOP: RTC Top Value**

  VAL wraps at this value if CTRL:TOPEN is 1.

11.6.4 RTC Interrupt Enable/Disable/Mask/Status/Clear

Name: IER/IDR/IMR/ISR/ICR

Access Type: IER/IDR/ICR: Write-only

IMR/ISR: Read-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	TOPI

- **TOPI: Top Interrupt**
  VAL has wrapped at its TOP.

The effect of writing or reading this bit depends on which register is being accessed:

- **IER (Write-only)**
  0: No effect
  1: Enable Interrupt
- **IDR (Write-only)**
  0: No effect
  1: Disable Interrupt
- **IMR (Read-only)**
  0: Interrupt is disabled
  1: Interrupt is enabled
- **ISR (Read-only)**
  0: An interrupt event has not occurred
  1: An interrupt event has occurred. Note that this is only set when the RTC is configured to wrap at TOP.
- **ICR (Write-only)**
  0: No effect
  1: Clear interrupt event

12. Watchdog Timer (WDT)

Rev: 1.0.1

12.1 Features

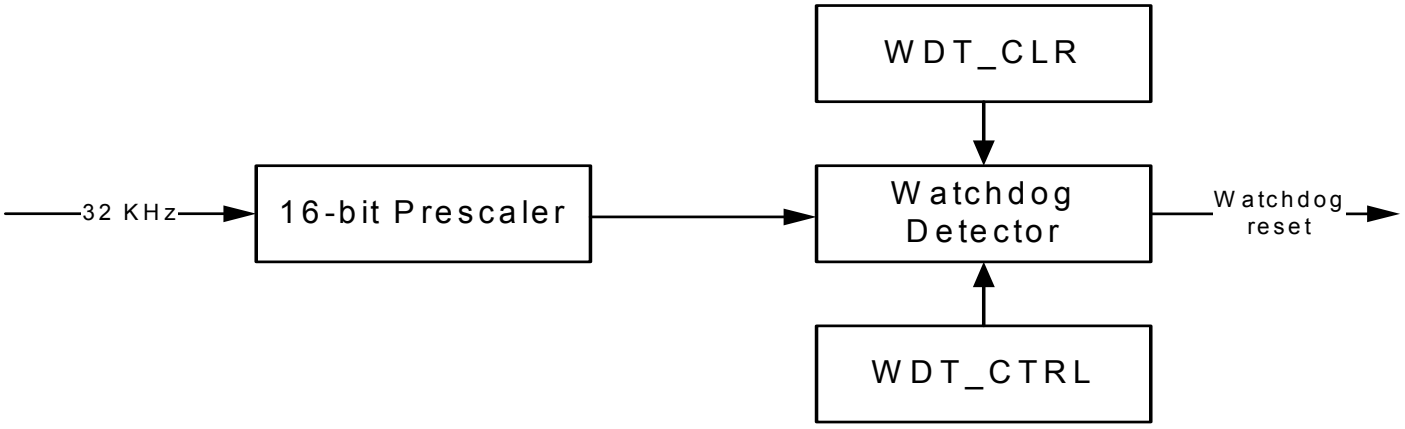
- **Watchdog timer with 16-bit prescaler**

12.2 Description

The Watchdog Timer (WDT) is fed from a 16-bit prescaler, which is clocked from the 32 kHz oscillator. Any tapping of the prescaler can be selected as clock source for the WDT.The watchdog timer must be periodically reset by software within the timeout period, ot herwise, the device is reset and starts executing from the boot vector. This allows the device to recover from a condition that has caused the system to be unstable.

12.3 Block Diagram

Figure 12-1. Real Time Counter module block diagram



12.4 Product Dependencies

12.4.1 I/O Lines

None

12.4.2 Power Management

The WDT is continously clocked, and remains operating in all sleep modes. However, if the WDT is enabled and the user tries to enter a sleepmode where the 32 KHz oscillator is turned off the system will enter the STOP sleepmode instead. This is to ensure the WDT is still running.

12.4.3 Debug Operation

The watchdog timer is frozen during debug operation, unless the OCD system keeps peripherals running in debug operation.

12.5 Functional Description

12.5.1 Watchdog Timer

The WDT is enabled by writing the EN bit in the CTRL register. This also enables the clock for the prescaler. The PSEL bitfield in the same register selects the watchdog timeout period:

$$T_{WDT} = 2^{(PSEL+1)} * 30.518\mu s$$

To avoid accidental disabling of the watchdog, the CTRL register must be written twice, first with the KEY field set to 0x55, then 0xAA without changing the other bitfields. Failure to do so will cause the write operation to be ignored, and CTRL does not change value.

The CLR register must be written with any value with regular intervals shorter than the watchdog timeout period. Otherwise, the device will receive a soft reset, and the code will start executing from the boot vector.

12.6 User Interface

Offset	Register	Register Name	Access	Reset
0x30	WDT Control	CTRL	Read/Write	0x0
0x34	WDT Clear	CLR	Write-only	0x0

12.6.1 WDT Control

Name: CTRL

Access Type: Read/Write

31	30	29	28	27	26	25	24
KEY[7:0]							
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	PSEL[3:0]			
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EN

- **KEY**

  This bitfield must be written twice, first with key value 0x55, then 0xAA, for a write operation to be effective. This bitfield always reads as zero.
- **PSEL: Prescale Select**

  Prescaler bit PSEL is used as watchdog timeout period.
- **EN: WDT Enable**

  0: WDT is disabled.

  1: WDT is enabled.

12.6.2 WDT Clear

Name: CLR

Access Type: Write-only

When the watchdog timer is enabled, this register must be periodically written, with any value, within the watchdog timeout period, to prevent a watchdog reset.

13. Interrupt Controller (INTC)

Rev: 1.0.0.4

13.1 Features

- **Autovectored low latency interrupt service with programmable priority**
  - **4 priority levels for regular, maskable interrupts**
  - **One Non-Maskable Interrupt**
- **Up to 64 groups of interrupts with up to 32 interrupt requests in each group**

13.2 Overview

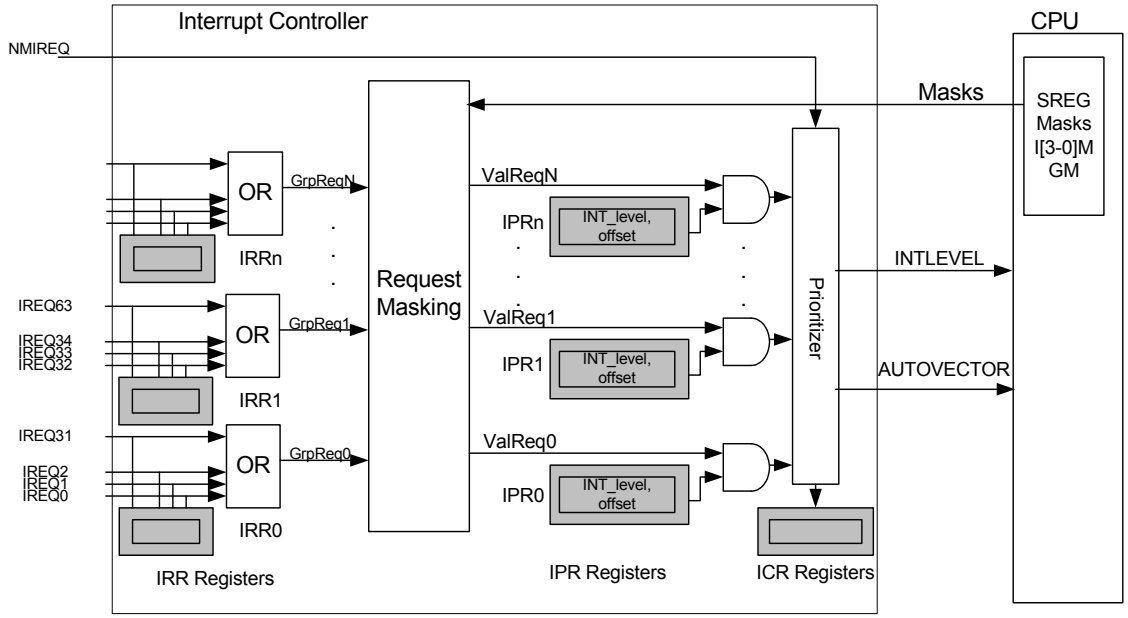
The INTC collects interrupt requests from the peripherals, prioritizes them, and delivers an interrupt request and an autovector to the CPU. The AVR32 architecture supports 4 priority levels for regular, maskable interrupts, and a Non-Maskable Interrupt (NMI).

The INTC supports up to 64 groups of interrupts. Each group can have up to 32 interrupt request lines, these lines are connected to the peripherals. Each group has an Interrupt Priority Register (IPR) and an Interrupt Request Register (IRR). The IPRs are used to assign a priority level and an autovector to each group, and the IRRs are used to identify the active interrupt request within each group. If a group has only one interrupt request line, an active interrupt group uniquely identifies the active interrupt request line, and the corresponding IRR is not needed. The INTC also provides one Interrupt Cause Register (ICR) per priority level. These registers identify the group that has a pending interrupt of the corresponding priority level. If several groups have a pending interrupt of the same level, the group with the lowest number takes priority.

13.3 Block Diagram

Figure 13-1 gives an overview of the INTC. The grey boxes represent registers that can be accessed via the user interface. The interrupt requests from the peripherals (IREQn) and the NMI are input on the left side of the figure. Signals to and from the CPU are on the right side of the figure.

Figure 13-1. INTC Block Diagram



13.4 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

13.4.1 Power Management

If the CPU enters a sleep mode that disables clocks used by the INTC, the INTC will stop functioning and resume operation after the system wakes up from sleep mode.

13.4.2 Clocks

The clock for the INTC bus interface (CLK_INTC) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager.

13.4.3 Debug Operation

When an external debugger forces the CPU into debug mode, the INTC continues normal operation.

13.5 Functional Description

All of the incoming interrupt requests (IREQs) are sampled into the corresponding Interrupt Request Register (IRR). The IRRs must be accessed to identify which IREQ within a group that is active. If several IREQs within the same group are active, the interrupt service routine must prioritize between them. All of the input lines in each group are logically ORed together to form the GrpReqN lines, indicating if there is a pending interrupt in the corresponding group.

The Request Masking hardware maps each of the GrpReq lines to a priority level from INT0 to INT3 by associating each group with the Interrupt Level (INTLEVEL) field in the corresponding Interrupt Priority Register (IPR). The GrpReq inputs are then masked by the mask bits from the CPU status register. Any interrupt group that has a pending interrupt of a priority level that is not masked by the CPU status register, gets its corresponding ValReq line asserted.

Masking of the interrupt requests is done based on five interrupt mask bits of the CPU status register, namely Interrupt Level 3 Mask (I3M) to Interrupt Level 0 Mask (I0M), and Global Interrupt Mask (GM). An interrupt request is masked if either the GM or the corresponding interrupt level mask bit is set.

The Prioritizer hardware uses the ValReq lines and the INTLEVEL field in the IPRs to select the pending interrupt of the highest priority. If an NMI interrupt request is pending, it automatically gets the highest priority of any pending interrupt. If several interrupt groups of the highest pending interrupt level have pending interrupts, the interrupt group with the highest number is selected.

The INTLEVEL and handler autovector offset (AUTOVECTOR) of the selected interrupt are transmitted to the CPU for interrupt handling and context switching. The CPU does not need to know which interrupt is requesting handling, but only the level and the offset of the handler address. The IRR registers contain the interrupt request lines of the groups and can be read via user interface registers for checking which interrupts of the group are actually active.

13.5.1 Non-Maskable Interrupts

A NMI request has priority over all other interrupt requests. NMI has a dedicated exception vector address defined by the AVR32 architecture, so AUTOVECTOR is undefined when INTLEVEL indicates that an NMI is pending.

13.5.2 CPU Response

When the CPU receives an interrupt request it checks if any other exceptions are pending. If no exceptions of higher priority are pending, interrupt handling is initiated. When initiating interrupt handling, the corresponding interrupt mask bit is set automatically for this and lower levels in status register. E.g, if an interrupt of level 3 is approved for handling, the interrupt mask bits I3M, I2M, I1M, and I0M are set in status register. If an interrupt of level 1 is approved, the masking bits I1M and I0M are set in status register. The handler address is calculated by adding AUTOVECTOR to the CPU system register Exception Vector Base Address (EVBA). The CPU will then jump to the calculated address and start executing the interrupt handler.

Setting the interrupt mask bits prevents the interrupts from the same and lower levels to be passed through the interrupt controller. Setting of the same level mask bit prevents also multiple requests of the same interrupt to happen.

It is the responsibility of the handler software to clear the interrupt request that caused the interrupt before returning from the interrupt handler. If the conditions that caused the interrupt are not cleared, the interrupt request remains active.

13.5.3 Clearing an Interrupt Request

Clearing of the interrupt request is done by writing to registers in the corresponding peripheral module, which then clears the corresponding NMIREQ/IREQ signal.

The recommended way of clearing an interrupt request is a store operation to the controlling peripheral register, followed by a dummy load operation from the same register. This causes a pipeline stall, which prevents the interrupt from accidentally re-triggering in case the handler is exited and the interrupt mask is cleared before the interrupt request is cleared.

13.6 User Interface

Table 13-1. INTC Register Memory Map

Offset	Register	Register Name	Access	Reset
0x000	Interrupt Priority Register 0	IPR0	Read/Write	0x00000000
0x004	Interrupt Priority Register 1	IPR1	Read/Write	0x00000000
...	...	...	...	...
0x0FC	Interrupt Priority Register 63	IPR63	Read/Write	0x00000000
0x100	Interrupt Request Register 0	IRR0	Read-only	N/A
0x104	Interrupt Request Register 1	IRR1	Read-only	N/A
...	...	...	...	...
0x1FC	Interrupt Request Register 63	IRR63	Read-only	N/A
0x200	Interrupt Cause Register 3	ICR3	Read-only	N/A
0x204	Interrupt Cause Register 2	ICR2	Read-only	N/A
0x208	Interrupt Cause Register 1	ICR1	Read-only	N/A
0x20C	Interrupt Cause Register 0	ICR0	Read-only	N/A

13.6.1 Interrupt Priority Registers

Register Name: IPR0...IPR63

Access Type: Read/Write

Offset: 0x000 - 0x0FC

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
INTLEVEL[1:0]		-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	AUTOVECTOR[13:8]					
7	6	5	4	3	2	1	0
AUTOVECTOR[7:0]							

- **INTLEVEL: Interrupt Level**
  Indicates the EVBA-relative offset of the interrupt handler of the corresponding group:
  00: INT0
  01: INT1
  10: INT2
  11: INT3
- **AUTOVECTOR: Autovector Address**
  Handler offset is used to give the address of the interrupt handler. The least significant bit should be written to zero to give halfword alignment.

13.6.2 Interrupt Request Registers

Name: IRR0...IRR63

Access Type: Read-only

Offset: 0x0FF - 0x1FC

Reset Value: N/A

31	30	29	28	27	26	25	24
IRR[32*x+31]	IRR[32*x+30]	IRR[32*x+29]	IRR[32*x+28]	IRR[32*x+27]	IRR[32*x+26]	IRR[32*x+25]	IRR[32*x+24]
23	22	21	20	19	18	17	16
IRR[32*x+23]	IRR[32*x+22]	IRR[32*x+21]	IRR[32*x+20]	IRR[32*x+19]	IRR[32*x+18]	IRR[32*x+17]	IRR[32*x+16]
15	14	13	12	11	10	9	8
IRR[32*x+15]	IRR[32*x+14]	IRR[32*x+13]	IRR[32*x+12]	IRR[32*x+11]	IRR[32*x+10]	IRR[32*x+9]	IRR[32*x+8]
7	6	5	4	3	2	1	0
IRR[32*x+7]	IRR[32*x+6]	IRR[32*x+5]	IRR[32*x+4]	IRR[32*x+3]	IRR[32*x+2]	IRR[32*x+1]	IRR[32*x+0]

- **IRR: Interrupt Request line**

  This bit is cleared when no interrupt request is pending on this input request line.

  This bit is set when an interrupt request is pending on this input request line.

  The are 64 IRRs, one for each group. Each IRR has 32 bits, one for each possible interrupt request, for a total of 2048 possible input lines. The IRRs are read by the software interrupt handler in order to determine which interrupt request is pending. The IRRs are sampled continuously, and are read-only.

13.6.3 Interrupt Cause Registers

Register Name: ICR0...ICR3

Access Type: Read-only

Offset: 0x200 - 0x20C

Reset Value: N/A

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	CAUSE					

- **CAUSE: Interrupt Group Causing Interrupt of Priority n**
  ICRn identifies the group with the highest priority that has a pending interrupt of level n. This value is only defined when at least one interrupt of level n is pending.

14. External Interrupt Controller (EIC)

Rev: 1.0.0.1

14.1 Features

- **Dedicated interrupt requests for each interrupt**
- **Individually maskable interrupts**
- **Interrupt on rising or falling edge**
- **Interrupt on high or low level**
- **Maskable NMI interrupt**

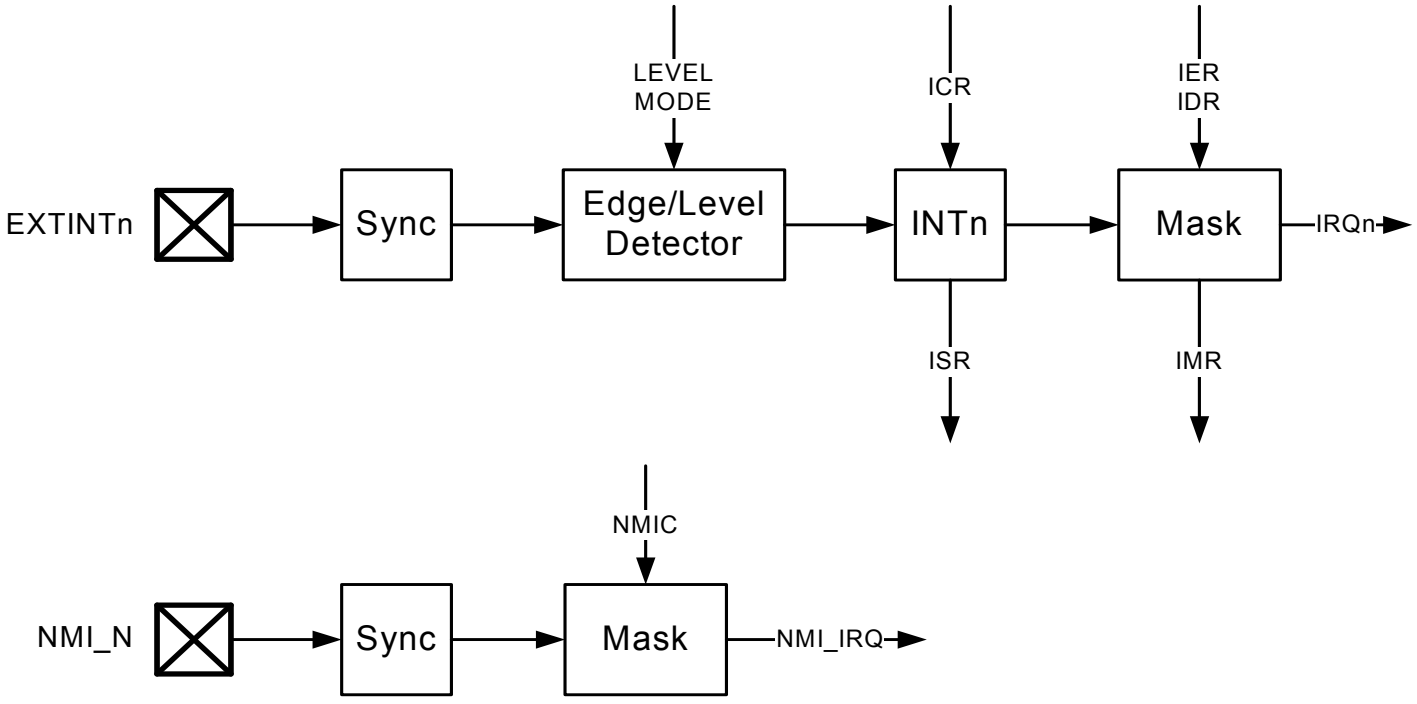
14.2 Description

The External Interrupt Controller allows 4 pins to be configured as external interrupts. Each pin has its own interrupt request, and can be individually masked. Each pin can generate an interrupt on rising or falling edge, or high or low level.

The module also masks the NMI_N pin, which generates the NMI interrupt for the CPU.

14.3 Block Diagram

Figure 14-1. External Interrupt Controller block diagram



14.4 Product Dependencies

14.4.1 I/O Lines

The External Interrupt and NMI pins are multiplexed with PIO lines. To act as external interrupts, these pins must be configured as inputs pins by the PIO controller. It is also possible to trigger the interrupt by driving these pins from registers in the PIO controller, or another peripheral output connected to the same pin.

14.4.2 Power Management

Edge triggered interrupts are available in all sleep modes except Deepdown. Level triggered interrupts and the NMI interrupt are available in all sleep modes.

14.4.3 Interrupt

The EIC interrupt lines are connected to internal sources of the interrupt controller. Using the External Interrutps requires the interrupt controller to be programmed first.

Using the Non-Maskable Interrupt does not require the interrupt controller to be programmed.

14.5 Functional Description

14.5.1 External Interrupts

Each external interrupt pin EXTINTn can be configured to produce an interrupt on rising or falling edge, or high or low level. External interrupts are configured by the MODE, EDGE, and LEVEL registers. Each interrupt n has a bit INTn in each of these registers.

Similarly, each interrupt has a corresponding bit in each of the interrupt control and status registers. Writing 1 to the INTn strobe in IER enables the external interrupt on pin EXTINTn, while writing 1 to INTn in IDR disables the external interrupt. IMR can be read to check which interrupts are enabled. When the interrupt triggers, the corresponding bit in ISR will be set. For edge triggered interrupts, the flag remains set until the corresponding strobe bit in ICR is written to 1. For level triggered interrupts, the flag remains set for as long as the interrupt condition is present on the pin.

Writing INTn in MODE to 0 enables edge triggered interrupts, while writing the bit to 1 enables level triggered interrupts.

If EXTINTn is configured as an edge triggered interrupt, writing INTn in EDGE to 0 will trigger the interrupt on falling edge, while writing the bit to 1 will trigger the interrupt on rising edge.

If EXTINTn is configured as a level triggered interrupt, writing INTn in LEVEL to 0 will trigger the interrupt on low level, while writing the bit to 1 will trigger the interrupt on high level.

14.5.1.1 Synchronization of external interrupts

The pin value of the EXTINTn pins is normally synchronized to the CPU clock, so spikes shorter than a CPU clock cycle are not guaranteed to produce an interrupt. In Stop mode, spikes shorter than a 32KHz clock cycle are not guaranteed to produce an interrupt. In Deepdown mode, only unsynchronized level interrupts remain active, and any short spike on this interrupt will wake up the device.

14.5.2 NMI Control

The Non-Maskable Interrupt of the CPU is connected to the NMI_N pin through masking logic in the External Interrupt Controller. This masking ensures that the NMI will not trigger before the CPU has been set up to handle interrupts. Writing the EN bit in the NMIC register enables the NMI interrupt, while writing EN to 0 disables the NMI interrupt. When enabled, the interrupt triggers whenever the NMI_N pin is negated.

The NMI_N pin is synchronized the same way as external level interrupts.

14.6 User Interface

Offset	Register	Register Name	Access	Reset
0x00	EIC Interrupt Enable	IER	Write-only	0x0
0x04	EIC Interrupt Disable	IDR	Write-only	0x0
0x08	EIC Interrupt Mask	IMR	Read-only	0x0
0x0C	EIC Interrupt Status	ISR	Read-only	0x0
0x10	EIC Interrupt Clear	ICR	Write-only	0x0
0x14	External Interrupt Mode	MODE	Read/Write	0x0
0x18	External Interrupt Edge	EDGE	Read/Write	0x0
0x1C	External Interrupt Level	LEVEL	Read/Write	0x0
0x24	External Interrupt NMI Control	NMIC	Read/Write	0x0

14.6.1 EIC Interrupt Enable/Disable/Mask/Status/Clear

Name: IER/IDR/IMR/ISR/ICR

Access Type: IER/IDR/ICR: Write-only

IMR/ISR: Read-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	INT3	INT2	INT1	INT0

- **INTn: External Interrupt n**
  0: External Interrupt has not triggered
  1: External Interrupt has triggered

The effect of writing or reading the bits listed above depends on which register is being accessed:

- **IER (Write-only)**
  0: No effect
  1: Enable Interrupt
- **IDR (Write-only)**
  0: No effect
  1: Disable Interrupt
- **IMR (Read-only)**
  0: Interrupt is disabled
  1: Interrupt is enabled
- **ISR (Read-only)**
  0: An interrupt event has occurred
  1: An interrupt even has not occurred
- **ICR (Write-only)**
  0: No effect
  1: Clear interrupt event

14.6.2 External Interrupt Mode/Edge/Level

Name: MODE/EDGE/LEVEL

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	INT3	INT2	INT1	INT0

- **INTn: External Interrupt n**

The bit interpretation is register specific:

- **MODE**
  - 0: Interrupt is edge triggered
  - 1: Interrupt is level triggered
- **EDGE**
  - 0: Interrupt triggers on falling edge
  - 1: Interrupt triggers on rising edge
- **LEVEL**
  - 0: Interrupt triggers on low level
  - 1: Interrupt triggers on high level

14.6.3 NMI Control

Name: NMIC

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EN

- **EN: Enable**
  0: NMI disabled. Asserting the NMI pin does not generate an NMI request.
  1: NMI enabled. Asserting the NMI pin generate an NMI request.

15. HSB Bus Matrix (HMATRIX)

Rev: 2.0.0.2

15.1 Features

- **User Interface on peripheral bus**
- **Configurable Number of Masters (Up to sixteen)**
- **Configurable Number of Slaves (Up to sixteen)**
- **One Decoder for Each Master**
- **Three Different Memory Mappings for Each Master (Internal and External boot, Remap)**
- **One Remap Function for Each Master**
- **Programmable Arbitration for Each Slave**
  - **Round-Robin**
  - **Fixed Priority**
- **Programmable Default Master for Each Slave**
  - **No Default Master**
  - **Last Accessed Default Master**
  - **Fixed Default Master**
- **One Cycle Latency for the First Access of a Burst**
- **Zero Cycle Latency for Default Master**
- **One Special Function Register for Each Slave (Not dedicated)**

15.2 Overview

The Bus Matrix implements a multi-layer bus structure, that enables parallel access paths between multiple High Speed Bus (HSB) masters and slaves in a system, thus increasing the overall bandwidth. The Bus Matrix interconnects up to 16 HSB Masters to up to 16 HSB Slaves. The normal latency to connect a master to a slave is one cycle except for the default master of the accessed slave which is connected directly (zero cycle latency). The Bus Matrix provides 16 Special Function Registers (SFR) that allow the Bus Matrix to support application specific features.

15.3 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

15.3.1 Clocks

The clock for the HMATRIX bus interface (CLK_HMATRIX) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager. It is recommended to disable the HMATRIX before disabling the clock, to avoid freezing the HMATRIX in an undefined state.

15.4 Functional Description

15.4.1 Memory Mapping

The Bus Matrix provides one decoder for every HSB Master Interface. The decoder offers each HSB Master several memory mappings. In fact, depending on the product, each memory area

may be assigned to several slaves. Booting at the same address while using different HSB slaves (i.e. external RAM, internal ROM or internal Flash, etc.) becomes possible.

The Bus Matrix user interface provides Master Remap Control Register (MRCR) that performs remap action for every master independently.

15.4.2 Special Bus Granting Mechanism

The Bus Matrix provides some speculative bus granting techniques in order to anticipate access requests from some masters. This mechanism reduces latency at first access of a burst or single transfer. This bus granting mechanism sets a different default master for every slave.

At the end of the current access, if no other request is pending, the slave remains connected to its associated default master. A slave can be associated with three kinds of default masters: no default master, last access master and fixed default master.

15.4.2.1 No Default Master

At the end of the current access, if no other request is pending, the slave is disconnected from all masters. No Default Master suits low-power mode.

15.4.2.2 Last Access Master

At the end of the current access, if no other request is pending, the slave remains connected to the last master that performed an access request.

15.4.2.3 Fixed Default Master

At the end of the current access, if no other request is pending, the slave connects to its fixed default master. Unlike last access master, the fixed master does not change unless the user modifies it by a software action (field FIXED_DEFMSTR of the related SCFG).

To change from one kind of default master to another, the Bus Matrix user interface provides the Slave Configuration Registers, one for each slave, that set a default master for each slave. The Slave Configuration Register contains two fields: DEFMSTR_TYPE and FIXED_DEFMSTR. The 2-bit DEFMSTR_TYPE field selects the default master type (no default, last access master, fixed default master), whereas the 4-bit FIXED_DEFMSTR field selects a fixed default master provided that DEFMSTR_TYPE is set to fixed default master. Please refer to the Bus Matrix user interface description.

15.4.3 Arbitration

The Bus Matrix provides an arbitration mechanism that reduces latency when conflict cases occur, i.e. when two or more masters try to access the same slave at the same time. One arbiter per HSB slave is provided, thus arbitrating each slave differently.

The Bus Matrix provides the user with the possibility of choosing between 2 arbitration types for each slave:

1. Round-Robin Arbitration (default)
2. Fixed Priority Arbitration

This choice is made via the field ARBT of the Slave Configuration Registers (SCFG).

Each algorithm may be complemented by selecting a default master configuration for each slave.

When a re-arbitration must be done, specific conditions apply. See Section 15.4.3.1 ”Arbitration Rules” on page 146.

15.4.3.1 *Arbitration Rules*

Each arbiter has the ability to arbitrate between two or more different master requests. In order to avoid burst breaking and also to provide the maximum throughput for slave interfaces, arbitration may only take place during the following cycles:

1. Idle Cycles: When a slave is not connected to any master or is connected to a master which is not currently accessing it.
2. Single Cycles: When a slave is currently doing a single access.
3. End of Burst Cycles: When the current cycle is the last cycle of a burst transfer. For defined length burst, predicted end of burst matches the size of the transfer but is managed differently for undefined length burst. See Section “•” on page 146.
4. Slot Cycle Limit: When the slot cycle counter has reached the limit value indicating that the current master access is too long and must be broken. See Section “•” on page 146.

• Undefined Length Burst Arbitration

In order to avoid long slave handling during undefined length bursts (INCR), the Bus Matrix provides specific logic in order to re-arbitrate before the end of the INCR transfer. A predicted end of burst is used as a defined length burst transfer and can be selected from among the following five possibilities:

1. Infinite: No predicted end of burst is generated and therefore INCR burst transfer will never be broken.
2. One beat bursts: Predicted end of burst is generated at each single transfer inside the INCP transfer.
3. Four beat bursts: Predicted end of burst is generated at the end of each four beat boundary inside INCR transfer.
4. Eight beat bursts: Predicted end of burst is generated at the end of each eight beat boundary inside INCR transfer.
5. Sixteen beat bursts: Predicted end of burst is generated at the end of each sixteen beat boundary inside INCR transfer.

This selection can be done through the field ULBT of the Master Configuration Registers (MCFG).

• Slot Cycle Limit Arbitration

The Bus Matrix contains specific logic to break long accesses, such as very long bursts on a very slow slave (e.g., an external low speed memory). At the beginning of the burst access, a counter is loaded with the value previously written in the SLOT_CYCLE field of the related Slave Configuration Register (SCFG) and decreased at each clock cycle. When the counter reaches zero, the arbiter has the ability to re-arbitrate at the end of the current byte, half word or word transfer.

15.4.3.2 Round-Robin Arbitration

This algorithm allows the Bus Matrix arbiters to dispatch the requests from different masters to the same slave in a round-robin manner. If two or more master requests arise at the same time, the master with the lowest number is first serviced, then the others are serviced in a round-robin manner.

There are three round-robin algorithms implemented:

1. Round-Robin arbitration without default master
2. Round-Robin arbitration with last default master
3. Round-Robin arbitration with fixed default master

• Round-Robin Arbitration without Default Master

This is the main algorithm used by Bus Matrix arbiters. It allows the Bus Matrix to dispatch requests from different masters to the same slave in a pure round-robin manner. At the end of the current access, if no other request is pending, the slave is disconnected from all masters. This configuration incurs one latency cycle for the first access of a burst. Arbitration without default master can be used for masters that perform significant bursts.

• Round-Robin Arbitration with Last Default Master

This is a biased round-robin algorithm used by Bus Matrix arbiters. It allows the Bus Matrix to remove the one latency cycle for the last master that accessed the slave. In fact, at the end of the current transfer, if no other master request is pending, the slave remains connected to the last master that performed the access. Other non privileged masters still get one latency cycle if they want to access the same slave. This technique can be used for masters that mainly perform single accesses.

• Round-Robin Arbitration with Fixed Default Master

This is another biased round-robin algorithm. It allows the Bus Matrix arbiters to remove the one latency cycle for the fixed default master per slave. At the end of the current access, the slave remains connected to its fixed default master. Every request attempted by this fixed default master will not cause any latency whereas other non privileged masters will still get one latency cycle. This technique can be used for masters that mainly perform single accesses.

15.4.3.3 Fixed Priority Arbitration

This algorithm allows the Bus Matrix arbiters to dispatch the requests from different masters to the same slave by using the fixed priority defined by the user. If two or more master requests are active at the same time, the master with the highest priority number is serviced first. If two or more master requests with the same priority are active at the same time, the master with the highest number is serviced first.

For each slave, the priority of each master may be defined through the Priority Registers for Slaves (PRAS and PRBS).

15.4.4 Slave and Master assignation

The index number assigned to Bus Matrix slaves and masters are described in Memories chapter.

15.5 User Interface

Table 15-1. HMATRIX Register Memory Map

Offset	Register	Name	Access	Reset Value
0x0000	Master Configuration Register 0	MCFG0	Read/Write	0x00000002
0x0004	Master Configuration Register 1	MCFG1	Read/Write	0x00000002
0x0008	Master Configuration Register 2	MCFG2	Read/Write	0x00000002
0x000C	Master Configuration Register 3	MCFG3	Read/Write	0x00000002
0x0010	Master Configuration Register 4	MCFG4	Read/Write	0x00000002
0x0014	Master Configuration Register 5	MCFG5	Read/Write	0x00000002
0x0018	Master Configuration Register 6	MCFG6	Read/Write	0x00000002
0x001C	Master Configuration Register 7	MCFG7	Read/Write	0x00000002
0x0020	Master Configuration Register 8	MCFG8	Read/Write	0x00000002
0x0024	Master Configuration Register 9	MCFG9	Read/Write	0x00000002
0x0028	Master Configuration Register 10	MCFG10	Read/Write	0x00000002
0x002C	Master Configuration Register 11	MCFG11	Read/Write	0x00000002
0x0030	Master Configuration Register 12	MCFG12	Read/Write	0x00000002
0x0034	Master Configuration Register 13	MCFG13	Read/Write	0x00000002
0x0038	Master Configuration Register 14	MCFG14	Read/Write	0x00000002
0x003C	Master Configuration Register 15	MCFG15	Read/Write	0x00000002
0x0040	Slave Configuration Register 0	SCFG0	Read/Write	0x00000010
0x0044	Slave Configuration Register 1	SCFG1	Read/Write	0x00000010
0x0048	Slave Configuration Register 2	SCFG2	Read/Write	0x00000010
0x004C	Slave Configuration Register 3	SCFG3	Read/Write	0x00000010
0x0050	Slave Configuration Register 4	SCFG4	Read/Write	0x00000010
0x0054	Slave Configuration Register 5	SCFG5	Read/Write	0x00000010
0x0058	Slave Configuration Register 6	SCFG6	Read/Write	0x00000010
0x005C	Slave Configuration Register 7	SCFG7	Read/Write	0x00000010
0x0060	Slave Configuration Register 8	SCFG8	Read/Write	0x00000010
0x0064	Slave Configuration Register 9	SCFG9	Read/Write	0x00000010
0x0068	Slave Configuration Register 10	SCFG10	Read/Write	0x00000010
0x006C	Slave Configuration Register 11	SCFG11	Read/Write	0x00000010
0x0070	Slave Configuration Register 12	SCFG12	Read/Write	0x00000010
0x0074	Slave Configuration Register 13	SCFG13	Read/Write	0x00000010
0x0078	Slave Configuration Register 14	SCFG14	Read/Write	0x00000010
0x007C	Slave Configuration Register 15	SCFG15	Read/Write	0x00000010
0x0080	Priority Register A for Slave 0	PRAS0	Read/Write	0x00000000
0x0084	Priority Register B for Slave 0	PRBS0	Read/Write	0x00000000
0x0088	Priority Register A for Slave 1	PRAS1	Read/Write	0x00000000

Table 15-1. HMATRIX Register Memory Map (Continued)

Offset	Register	Name	Access	Reset Value
0x008C	Priority Register B for Slave 1	PRBS1	Read/Write	0x00000000
0x0090	Priority Register A for Slave 2	PRAS2	Read/Write	0x00000000
0x0094	Priority Register B for Slave 2	PRBS2	Read/Write	0x00000000
0x0098	Priority Register A for Slave 3	PRAS3	Read/Write	0x00000000
0x009C	Priority Register B for Slave 3	PRBS3	Read/Write	0x00000000
0x00A0	Priority Register A for Slave 4	PRAS4	Read/Write	0x00000000
0x00A4	Priority Register B for Slave 4	PRBS4	Read/Write	0x00000000
0x00A8	Priority Register A for Slave 5	PRAS5	Read/Write	0x00000000
0x00AC	Priority Register B for Slave 5	PRBS5	Read/Write	0x00000000
0x00B0	Priority Register A for Slave 6	PRAS6	Read/Write	0x00000000
0x00B4	Priority Register B for Slave 6	PRBS6	Read/Write	0x00000000
0x00B8	Priority Register A for Slave 7	PRAS7	Read/Write	0x00000000
0x00BC	Priority Register B for Slave 7	PRBS7	Read/Write	0x00000000
0x00C0	Priority Register A for Slave 8	PRAS8	Read/Write	0x00000000
0x00C4	Priority Register B for Slave 8	PRBS8	Read/Write	0x00000000
0x00C8	Priority Register A for Slave 9	PRAS9	Read/Write	0x00000000
0x00CC	Priority Register B for Slave 9	PRBS9	Read/Write	0x00000000
0x00D0	Priority Register A for Slave 10	PRAS10	Read/Write	0x00000000
0x00D4	Priority Register B for Slave 10	PRBS10	Read/Write	0x00000000
0x00D8	Priority Register A for Slave 11	PRAS11	Read/Write	0x00000000
0x00DC	Priority Register B for Slave 11	PRBS11	Read/Write	0x00000000
0x00E0	Priority Register A for Slave 12	PRAS12	Read/Write	0x00000000
0x00E4	Priority Register B for Slave 12	PRBS12	Read/Write	0x00000000
0x00E8	Priority Register A for Slave 13	PRAS13	Read/Write	0x00000000
0x00EC	Priority Register B for Slave 13	PRBS13	Read/Write	0x00000000
0x00F0	Priority Register A for Slave 14	PRAS14	Read/Write	0x00000000
0x00F4	Priority Register B for Slave 14	PRBS14	Read/Write	0x00000000
0x00F8	Priority Register A for Slave 15	PRAS15	Read/Write	0x00000000
0x00FC	Priority Register B for Slave 15	PRBS15	Read/Write	0x00000000
0x0100	Master Remap Control Register	MRCR	Read/Write	0x00000000
0x0110	Special Function Register 0	SFR0	Read/Write	–
0x0114	Special Function Register 1	SFR1	Read/Write	–
0x0118	Special Function Register 2	SFR2	Read/Write	–
0x011C	Special Function Register 3	SFR3	Read/Write	–
0x0120	Special Function Register 4	SFR4	Read/Write	–
0x0124	Special Function Register 5	SFR5	Read/Write	–

Table 15-1. HMATRIX Register Memory Map (Continued)

Offset	Register	Name	Access	Reset Value
0x0128	Special Function Register 6	SFR6	Read/Write	–
0x012C	Special Function Register 7	SFR7	Read/Write	–
0x0130	Special Function Register 8	SFR8	Read/Write	–
0x0134	Special Function Register 9	SFR9	Read/Write	–
0x0138	Special Function Register 10	SFR10	Read/Write	–
0x013C	Special Function Register 11	SFR11	Read/Write	–
0x0140	Special Function Register 12	SFR12	Read/Write	–
0x0144	Special Function Register 13	SFR13	Read/Write	–
0x0148	Special Function Register 14	SFR14	Read/Write	–
0x014C	Special Function Register 15	SFR15	Read/Write	–

15.5.1 Master Configuration Registers

Name: MCFG0...MCFG15

Access Type: Read/Write

Offset: 0x00 - 0x3C

Reset Value: 0x00000002

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	ULBT		

- **ULBT: Undefined Length Burst Type**

  0: Infinite Length Burst

  No predicted end of burst is generated and therefore INCR bursts coming from this master cannot be broken.

  1: Single Access

  The undefined length burst is treated as a succession of single accesses, allowing re-arbitration at each beat of the INCR burst.

  2: Four Beat Burst

  The undefined length burst is split into a four-beat burst, allowing re-arbitration at each four-beat burst end.

  3: Eight Beat Burst

  The undefined length burst is split into an eight-beat burst, allowing re-arbitration at each eight-beat burst end.

  4: Sixteen Beat Burst

  The undefined length burst is split into a sixteen-beat burst, allowing re-arbitration at each sixteen-beat burst end.

15.5.2 Slave Configuration Registers

Name: SCFG0...SCFG15

Access Type: Read/Write

Offset: 0x40 - 0x7C

Reset Value: 0x00000010

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	ARBT

23	22	21	20	19	18	17	16
–	–	FIXED_DEFMSTR				DEFMSTR_TYPE	

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
SLOT_CYCLE							

- **ARBT: Arbitration Type**
  0: Round-Robin Arbitration
  1: Fixed Priority Arbitration
- **FIXED_DEFMSTR: Fixed Default Master**
  This is the number of the Default Master for this slave. Only used if DEFMSTR_TYPE is 2. Specifying the number of a master which is not connected to the selected slave is equivalent to setting DEFMSTR_TYPE to 0.
  The size of this field depends on the number of masters. This size is log2(number of masters).
- **DEFMSTR_TYPE: Default Master Type**
  0: No Default Master
  At the end of the current slave access, if no other master request is pending, the slave is disconnected from all masters.
  This results in a one cycle latency for the first access of a burst transfer or for a single access.
  1: Last Default Master
  At the end of the current slave access, if no other master request is pending, the slave stays connected to the last master having accessed it.
  This results in not having one cycle latency when the last master tries to access the slave again.
  2: Fixed Default Master
  At the end of the current slave access, if no other master request is pending, the slave connects to the fixed master the number that has been written in the FIXED_DEFMSTR field.
  This results in not having one cycle latency when the fixed master tries to access the slave again.
- **SLOT_CYCLE: Maximum Number of Allowed Cycles for a Burst**
  When the SLOT_CYCLE limit is reached for a burst, it may be broken by another master trying to access this slave.
  This limit has been placed to avoid locking a very slow slave when very long bursts are used.
  This limit must not be very small. Unreasonably small values break every burst and the Bus Matrix arbitrates without performing any data transfer. 16 cycles is a reasonable value for SLOT_CYCLE.

15.5.3 Bus Matrix Priority Registers A For Slaves

Name: PRAS0...PRAS15

Access Type: Read/Write

Offset: -

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
M7PR				M6PR			

23	22	21	20	19	18	17	16
M5PR				M4PR			

15	14	13	12	11	10	9	8
M3PR				M2PR			

7	6	5	4	3	2	1	0
M1PR				M0PR			

- **MxPR: Master x Priority**

  Fixed priority of Master x for accessing the selected slave. The higher the number, the higher the priority.

15.5.4 Priority Registers B For Slaves

Name: PRBS0...PRBS15

Access Type: Read/Write

Offset: -

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
M15PR				M14PR			

23	22	21	20	19	18	17	16
M13PR				M12PR			

15	14	13	12	11	10	9	8
M11PR				M10PR			

7	6	5	4	3	2	1	0
M9PR				M8PR			

- **MxPR: Master x Priority**

  Fixed priority of Master x for accessing the selected slave. The higher the number, the higher the priority.

15.5.5 Master Remap Control Register

Name: MRCR

Access Type: Read/Write

Offset: 0x100

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
RCB15	RCB14	RCB13	RCB12	RCB11	RCB10	RCB9	RCB8

7	6	5	4	3	2	1	0
RCB7	RCB6	RCB5	RCB4	RCB3	RCB2	RCB1	RCB0

- **RCB: Remap Command Bit for Master x**
  0: Disable remapped address decoding for the selected Master
  1: Enable remapped address decoding for the selected Master

15.5.6 Special Function Registers

Name: SFR0...SFR15

Access Type: Read/Write

Offset: 0x110 - 0x115

Reset Value: -

31	30	29	28	27	26	25	24
SFR							

23	22	21	20	19	18	17	16
SFR							

15	14	13	12	11	10	9	8
SFR							

7	6	5	4	3	2	1	0
SFR							

- **SFR: Special Function Register Fields**

  Those registers are not a HMATRIX specific register. The field of those will be defined where they are used.

16. External Bus Interface (EBI)

Rev: 1.0.1.2

16.1 Features

- **Optimized for Application Memory Space support**
- **Integrates Three External Memory Controllers:**
  - **Static Memory Controller**
  - **SDRAM Controller**
  - **ECC Controller**
- **Additional Logic for NAND Flash/SmartMedia™ and CompactFlash™ Support**
  - **NAND Flash support: 8-bit as well as 16-bit devices are supported**
  - **CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and _ATA SEL (True IDE mode) are not handled.**
- **Optimized External Bus:**
  - **16- or 32-bit Data Bus**
  - **Up to 26-bit Address Bus, Up to 64-Mbytes Addressable**
  - **Optimized pin multiplexing to reduce latencies on External Memories**
- **Up to 6 Chip Selects, Configurable Assignment:**
  - **Static Memory Controller on NCS0**
  - **SDRAM Controller or Static Memory Controller on NCS1**
  - **Static Memory Controller on NCS2**
  - **Static Memory Controller on NCS3, Optional NAND Flash Support**
  - **Static Memory Controller on NCS4 - NCS5, Optional CompactFlash™ Support**

16.2 Description

The External Bus Interface (EBI) is designed to ensure the successful data transfer between several external devices and the embedded Memory Controller of an AVR32 device. The Static Memory, SDRAM and ECC Controllers are all featured external Memory Controllers on the EBI. These external Memory Controllers are capable of handling several types of external memory and peripheral devices, such as SRAM, PROM, EPROM, EEPROM, Flash, and SDRAM.

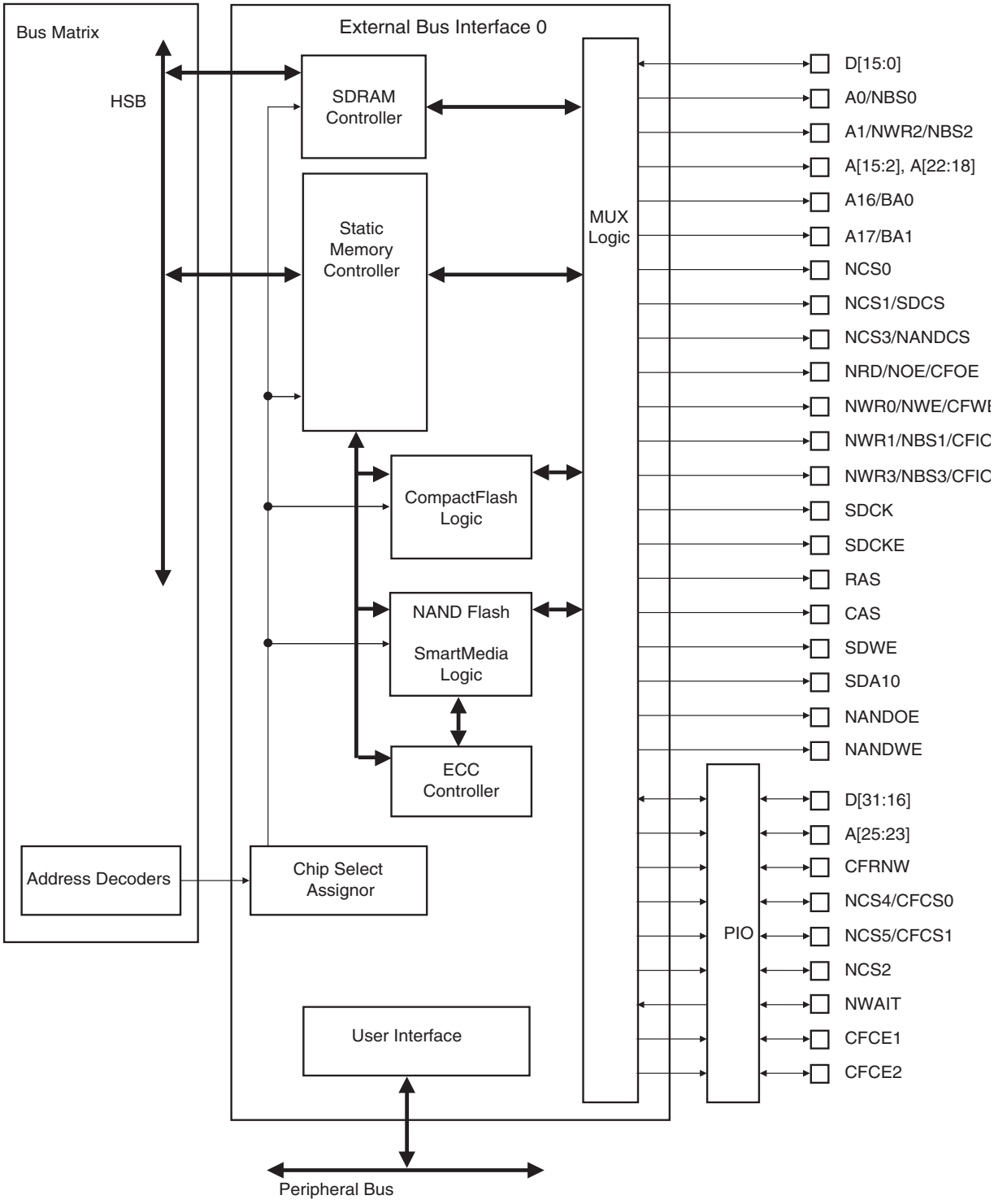
The EBI also supports the CompactFlash and the NAND Flash/SmartMedia protocols via integrated circuitry that greatly reduces the requirements for external components. Furthermore, the EBI handles data transfers with up to six external devices, each assigned to six address spaces defined by the embedded Memory Controller. Data transfers are performed through a 16-bit or 32-bit data bus, an address bus of up to 26 bits, up to six chip select lines (NCS[5:0]) and several control pins that are generally multiplexed between the different external Memory Controllers.

16.3 Block Diagram

16.3.1 External Bus Interface

Figure 16-1 shows the organization of the External Bus Interface.

Figure 16-1. Organization of the External Bus Interface



16.4 I/O Lines Description

Table 16-1. EBI I/O Lines Description

Name	Function	Type	Active Level
EBI			
D0 - D31	Data Bus	I/O	
A0 - A25	Address Bus	Output	
NWAIT	External Wait Signal	Input	Low
SMC			
NCS0 - NCS5	Chip Select Lines	Output	Low
NWR0 - NWR3	Write Signals	Output	Low
NOE	Output Enable	Output	Low
NRD	Read Signal	Output	Low
NWE	Write Enable	Output	Low
NBS0 - NBS3	Byte Mask Signals	Output	Low
EBI for CompactFlash Support			
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low
CFOE	CompactFlash Output Enable	Output	Low
CFWE	CompactFlash Write Enable	Output	Low
CFIOR	CompactFlash I/O Read Signal	Output	Low
CFIOW	CompactFlash I/O Write Signal	Output	Low
CFRNW	CompactFlash Read Not Write Signal	Output	
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low
EBI for NAND Flash/SmartMedia Support			
NANDCS	NAND Flash Chip Select Line	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
SDRAM Controller			
SDCK	SDRAM Clock	Output	
SDCKE	SDRAM Clock Enable	Output	High
SDCS	SDRAM Controller Chip Select Line	Output	Low
BA0 - BA1	Bank Select	Output	
SDWE	SDRAM Write Enable	Output	Low
RAS - CAS	Row and Column Signal	Output	Low
NWR0 - NWR3	Write Signals	Output	Low
NBS0 - NBS3	Byte Mask Signals	Output	Low
SDA10	SDRAM Address 10 Line	Output	

Depending on the Memory Controller in use, all signals are not connected directly through the Mux Logic.

Table 16-2 on page 161 details the connections between the two Memory Controllers and the EBI pins.

Table 16-2. EBI Pins and Memory Controllers I/O Lines Connections

EBI Pins	SDRAMC I/O Lines	SMC I/O Lines
NWR1/NBS1/CFIOR	NBS1	NWR1/NUB
A0/NBS0	Not Supported	SMC_A0/NLB
A1/NBS2/NWR2	Not Supported	SMC_A1
A[11:2]	SDRAMC_A[9:0]	SMC_A[11:2]
SDA10	SDRAMC_A10	Not Supported
A12	Not Supported	SMC_A12
A[14:13]	SDRAMC_A[12:11]	SMC_A[14:13]
A[22:15]	Not Supported	SMC_A[22:15]
A[25:23]	Not Supported	SMC_A[25:23]
D[31:0]	D[31:0]	D[31:0]

16.5 Application Example

16.5.1 Hardware Interface

Table 16-3 on page 162 details the connections to be applied between the EBI pins and the external devices for each Memory Controller.

Table 16-3. EBI Pins and External Static Devices Connections

Signals	Pins of the Interfaced Device					
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	4 x 8-bit Static Devices	2 x 16-bit Static Devices	32-bit Static Device
Controller	**SMC**					
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15
D16 - D23	–	–	–	D16 - D23	D16 - D23	D16 - D23
D24 - D31	–	–	–	D24 - D31	D24 - D31	D24 - D31
A0/NBS0	A0	–	NLB	–	NLB(3)	BE0(5)
A1/NWR2/NBS2	A1	A0	A0	WE(2)	NLB(4)	BE2(5)
A2 - A22	A[2:22]	A[1:21]	A[1:21]	A[0:20]	A[0:20]	A[0:20]
A23 - A25	A[23:25]	A[22:24]	A[22:24]	A[21:23]	A[21:23]	A[21:23]
NCS0	CS	CS	CS	CS	CS	CS
NCS1/SDCS	CS	CS	CS	CS	CS	CS
NCS2	CS	CS	CS	CS	CS	CS
NCS3/NANDCS	CS	CS	CS	CS	CS	CS
NCS4/CFCS0	CS	CS	CS	CS	CS	CS
NCS5/CFCS1	CS	CS	CS	CS	CS	CS
NRD/NOE/CFOE	OE	OE	OE	OE	OE	OE
NWR0/NWE	WE	WE(1)	WE	WE(2)	WE	WE
NWR1/NBS1	–	WE(1)	NUB	WE(2)	NUB(3)	BE1(5)
NWR3/NBS3	–	–	–	WE(2)	NUB(4)	BE3(5)

Notes:
1. NWR1 enables upper byte writes. NWR0 enables lower byte writes.
2. NWRx enables corresponding byte x writes. (x = 0,1,2 or 3)
3. NBS0 and NBS1 enable respectively lower and upper bytes of the lower 16-bit word.
4. NBS2 and NBS3 enable respectively lower and upper bytes of the upper 16-bit word.
5. BEx: Byte x Enable (x = 0,1,2 or 3)

Table 16-4. EBI Pins and External Devices Connections

Signals	Pins of the Interfaced Device			
	SDRAM	Compact Flash	Compact Flash True IDE Mode	Smart Media or NAND Flash
Controller	**SDRAMC**	**SMC**		
D0 - D7	D0 - D7	D0 - D7	D0 - D7	AD0-AD7
D8 - D15	D8 - D15	D8 - 15	D8 - 15	AD8-AD15
D16 - D31	D16 - D31	–	–	–
A0/NBS0	DQM0	A0	A0	–
A1/NWR2/NBS2	DQM2	A1	A1	–
A2 - A10	A[0:8]	A[2:10]	A[2:10]	–
A11	A9	–	–	–
SDA10	A10	–	–	–
A12	–	–	–	–
A13 - A14	A[11:12]	–	–	–
A15	–	–	–	–
A16/BA0	BA0	–	–	–
A17/BA1	BA1	–	–	–
A18 - A20	–	–	–	–
A21	–	–	–	CLE(3)
A22	–	REG	REG	ALE(3)
A23 - A24	–	–	–	–
A25	–	–	–	–
NCS0	–	–	–	–
NCS1/SDCS	CS[0]	–	–	–
NCS2	–	–	–	–
NCS3/NANDCS	–	–	–	–
NCS4/CFCS0	–	CFCS0(1)	CFCS0(1)	–
NCS5/CFCS1	–	CFCS1(1)	CFCS1(1)	–
NANDOE	–	–	–	OE
NANDWE	–	–	–	WE
NRD/NOE/CFOE	–	OE	–	–
NWR0/NWE/CFWE	–	WE	WE	–
NWR1/NBS1/CFIOR	DQM1	IOR	IOR	–
NWR3/NBS3/CFIOW	DQM3	IOW	IOW	–
CFRNW	–	CFRNW(1)	CFRNW(1)	–
CFCE1	–	CE1	CS0	–
CFCE2	–	CE2	CS1	–

Table 16-4. EBI Pins and External Devices Connections (Continued)

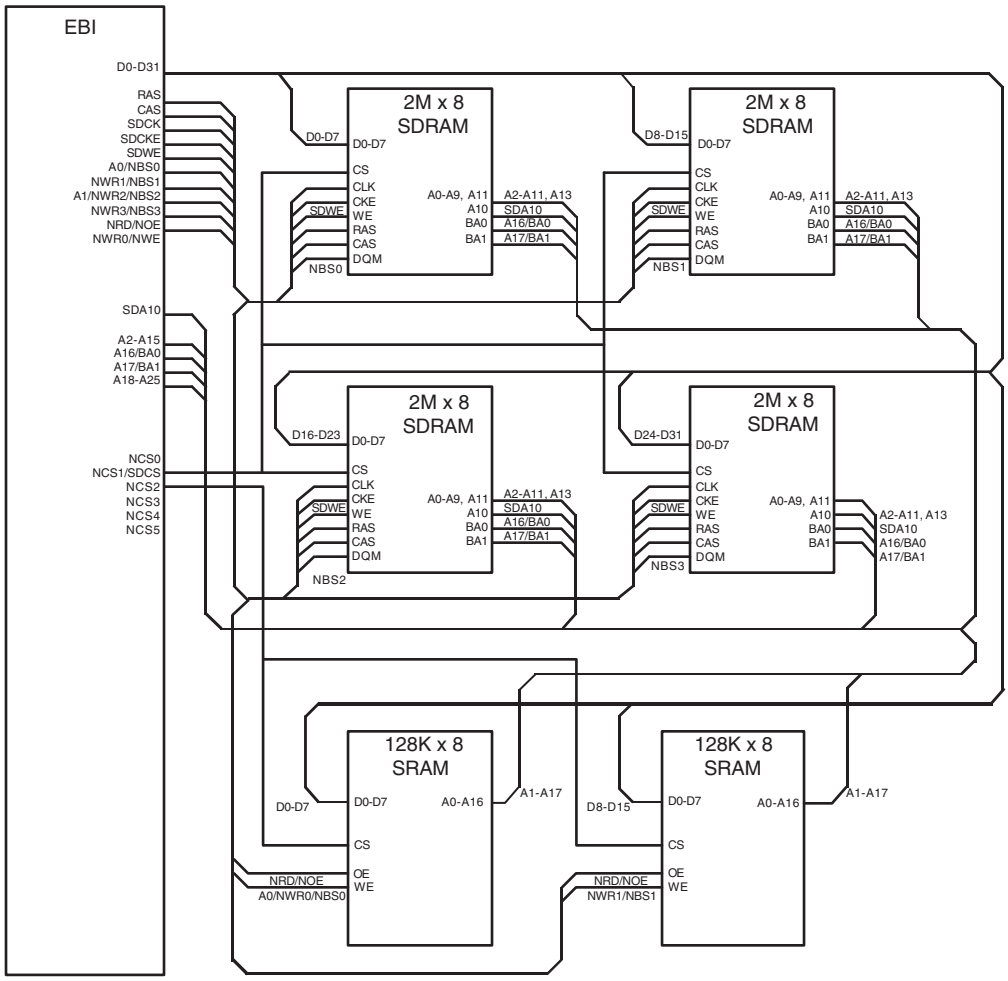
Signals	Pins of the Interfaced Device			
	SDRAM	Compact Flash	Compact Flash True IDE Mode	Smart Media or NAND Flash
Controller	**SDRAMC**	**SMC**		
SDCK	CLK	–	–	–
SDCKE	CKE	–	–	–
RAS	RAS	–	–	–
CAS	CAS	–	–	–
SDWE	WE	–	–	–
NWAIT	–	WAIT	WAIT	–
Pxx[2]	–	CD1 or CD2	CD1 or CD2	–
Pxx[2]	–	–	–	CE
Pxx[2]	–	–	–	RDY

Note:
1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.
2. Any PIO line.
3. The CLE and ALE signals of the NAND Flash device may be driven by any address bit. For details, see "SmartMedia and NAND Flash Support" on page 171.
4.

16.5.2 Connection Examples

Figure 16-2 shows an example of connections between the EBI and external devices.

Figure 16-2. EBI Connections to Memory Devices



16.6 Product Dependencies

16.6.1 I/O Lines

The pins used for interfacing the External Bus Interface may be multiplexed with the PIO lines. The programmer must first program the PIO controller to assign the External Bus Interface pins to their peripheral function. If I/O lines of the External Bus Interface are not used by the application, they can be used for other purposes by the PIO Controller.

16.7 Functional Description

The EBI transfers data between the internal HSB Bus (handled by the HMatrix) and the external memories or peripheral devices. It controls the waveforms and the parameters of the external address, data and control busses and is composed of the following elements:

- The Static Memory Controller (SMC)
- The SDRAM Controller (SDRAMC)
- The ECC Controller (ECC)
- A chip select assignment feature that assigns an HSB address space to the external devices
- A multiplex controller circuit that shares the pins between the different Memory Controllers
- Programmable CompactFlash support logic
- Programmable SmartMedia and NAND Flash support logic

16.7.1 Bus Multiplexing

The EBI offers a complete set of control signals that share the 32-bit data lines, the address lines of up to 26 bits and the control signals through a multiplex logic operating in function of the memory area requests.

Multiplexing is specifically organized in order to guarantee the maintenance of the address and output control lines at a stable state while no external access is being performed. Multiplexing is also designed to respect the data float times defined in the Memory Controllers. Furthermore, refresh cycles of the SDRAM are executed independently by the SDRAM Controller without delaying the other external Memory Controller accesses.

16.7.2 Pull-up Control

A specific HMATRIX_SFR register in the Matrix User Interface permit enabling of on-chip pull-up resistors on the data bus lines not multiplexed with the PIO Controller lines. For details on this register, refer to the Peripherals Section. The pull-up resistors are enabled after reset. Setting the EBI_DBPUC bit disables the pull-up resistors on lines not muxed with PIO. Enabling the pull-up resistor on lines multiplexed with PIO lines can be performed by programming the appropriate PIO controller.

16.7.3 Static Memory Controller

For information on the Static Memory Controller, refer to the Static Memory Controller Section.

16.7.4 SDRAM Controller

For information on the SDRAM Controller, refer to the SDRAM Section.

16.7.5 ECC Controller

For information on the ECC Controller, refer to the ECC Section.

16.7.6 CompactFlash Support

The External Bus Interface integrates circuitry that interfaces to CompactFlash devices.

The CompactFlash logic is driven by the Static Memory Controller (SMC) on the NCS4 and/or NCS5 address space. Programming the EBI_CS4A and/or EBI_CS5A bits in a HMATRIX_SFR Register to the appropriate value enables this logic. For details on this register, refer to the Peripherals Section. Access to an external CompactFlash device is then made by accessing the address space reserved to NCS4 and/or NCS5 (i.e., between 0x04000 0000 and 0x07FF FFFF for NCS4 and between 0x2000 0000 and 0x23FF FFFF for NCS5).

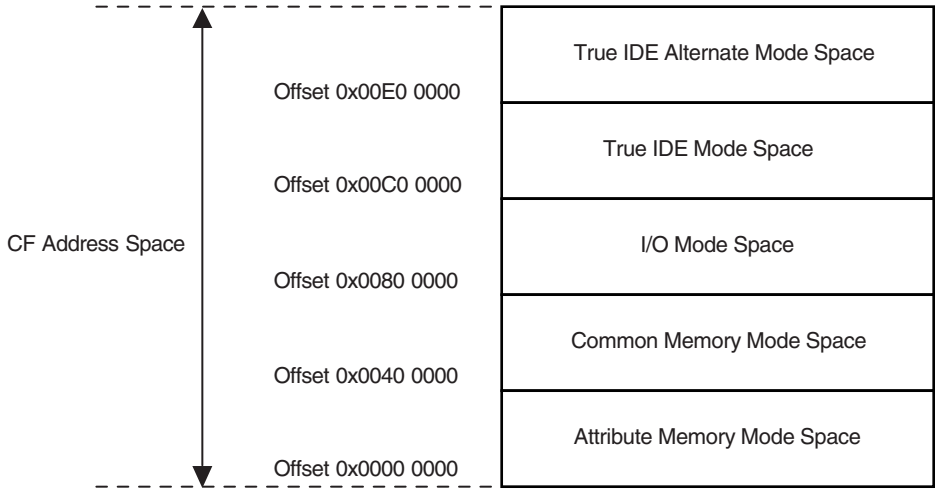
All CompactFlash modes (Attribute Memory, Common Memory, I/O and True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and _ATA SEL (True IDE mode) are not handled.

16.7.6.1 I/O Mode, Common Memory Mode, Attribute Memory Mode and True IDE Mode

Within the NCS4 and/or NCS5 address space, the current transfer address is used to distinguish I/O mode, common memory mode, attribute memory mode and True IDE mode.

The different modes are accessed through a specific memory mapping as illustrated on Figure 16-3. A[23:21] bits of the transfer address are used to select the desired mode as described in Table 16-5 on page 168.

Figure 16-3. CompactFlash Memory Mapping



Note: The A22 pin is used to drive the REG signal of the CompactFlash Device (except in True IDE mode).

Table 16-5. CompactFlash Mode Selection

A[23:21]	Mode Base Address
000	Attribute Memory
010	Common Memory
100	I/O Mode
110	True IDE Mode
111	Alternate True IDE Mode

16.7.6.2 CFCE1 and CFCE2 signals

To cover all types of access, the SMC must be alternatively set to drive 8-bit data bus or 16-bit data bus. The odd byte access on the D[7:0] bus is only possible when the SMC is configured to drive 8-bit memory devices on the corresponding NCS pin (NCS4 or NCS5). The Chip Select Register (DBW field in the corresponding Chip Select Register) of the NCS4 and/or NCS5 address space must be set as shown in Table 16-6 to enable the required access type.

NBS1 and NBS0 are the byte selection signals from SMC and are available when the SMC is set in Byte Select mode on the corresponding Chip Select.

The CFCE1 and CFCE2 waveforms are identical to the corresponding NCSx waveform. For details on these waveforms and timings, refer to the Static Memory Controller Section.

Table 16-6. CFCE1 and CFCE2 Truth Table

Mode	CFCE2	CFCE1	DBW	Comment	SMC Access Mode
Attribute Memory	NBS1	NBS0	16 bits	Access to Even Byte on D[7:0]	Byte Select
Common Memory	NBS1	NBS0	16bits	Access to Even Byte on D[7:0] Access to Odd Byte on D[15:8]	Byte Select
	1	0	8 bits	Access to Odd Byte on D[7:0]	
I/O Mode	NBS1	NBS0	16 bits	Access to Even Byte on D[7:0] Access to Odd Byte on D[15:8]	Byte Select
	1	0	8 bits	Access to Odd Byte on D[7:0]	
True IDE Mode					
Task File	1	0	8 bits	Access to Even Byte on D[7:0] Access to Odd Byte on D[7:0]	
Data Register	1	0	16 bits	Access to Even Byte on D[7:0] Access to Odd Byte on D[15:8]	Byte Select
Alternate True IDE Mode					
Control Register Alternate Status Read	0	1	Don't Care	Access to Even Byte on D[7:0]	Don't Care
Drive Address	0	1	8 bits	Access to Odd Byte on D[7:0]	
Standby Mode or Address Space is not assigned to CF	1	1	–	–	–

16.7.6.3 *Read/Write Signals*

In I/O mode and True IDE mode, the CompactFlash logic drives the read and write command signals of the SMC on CFIOR and CFIOW signals, while the CFOE and CFWE signals are deactivated. Likewise, in common memory mode and attribute memory mode, the SMC signals are driven on the CFOE and CFWE signals, while the CFIOR and CFIOW are deactivated. Figure 16-4 on page 169 demonstrates a schematic representation of this logic.

Attribute memory mode, common memory mode and I/O mode are supported by setting the address setup and hold time on the NCS4 (and/or NCS5) chip select to the appropriate values. For details on these signal waveforms, please refer to the section: Setup and Hold Cycles of the Static Memory Controller Section.

Figure 16-4. CompactFlash Read/Write Control Signals

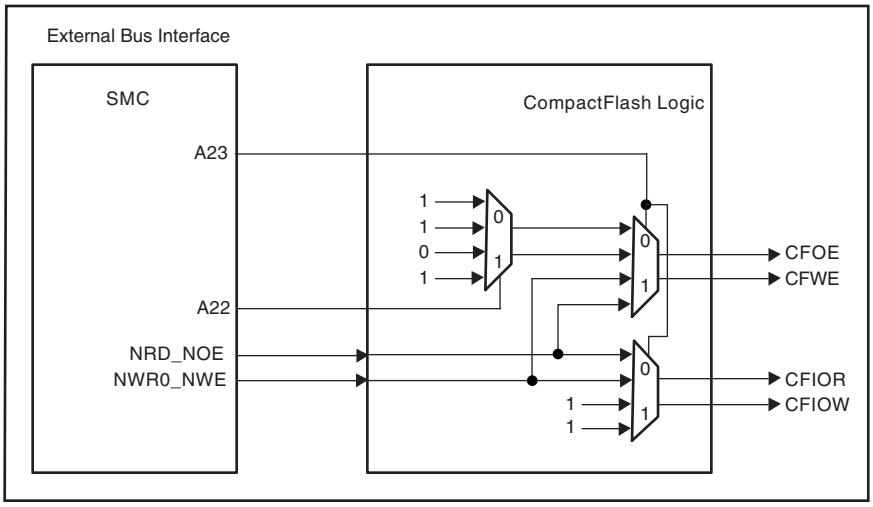


Table 16-7. CompactFlash Mode Selection

Mode Base Address	CFOE	CFWE	CFIOR	CFIOW
Attribute Memory Common Memory	NRD_NOE	NWR0_NWE	1	1
I/O Mode	1	1	NRD_NOE	NWR0_NWE
True IDE Mode	0	1	NRD_NOE	NWR0_NWE

16.7.6.4 *Multiplexing of CompactFlash Signals on EBI Pins*

Table 16-8 on page 170 and Table 16-9 on page 170 illustrate the multiplexing of the CompactFlash logic signals with other EBI signals on the EBI pins. The EBI pins in Table 16-8 are strictly dedicated to the CompactFlash interface as soon as the EBI_CS4A and/or EBI_CS5A field of a specific HMATRIX_SFR Register is set, see the Peripherals Section for details. These pins must not be used to drive any other memory devices.

The EBI pins in Table 16-9 on page 170 remain shared between all memory areas when the corresponding CompactFlash interface is enabled (EBI_CS4A = 1 and/or EBI_CS5A = 1).

Table 16-8. Dedicated CompactFlash Interface Multiplexing

Pins	CompactFlash Signals		EBI Signals	
	CS4A = 1	**CS5A = 1**	**CS4A = 0**	**CS5A = 0**
NCS4/CFCS0	CFCS0		NCS4	
NCS5/CFCS1		CFCS1		NCS5

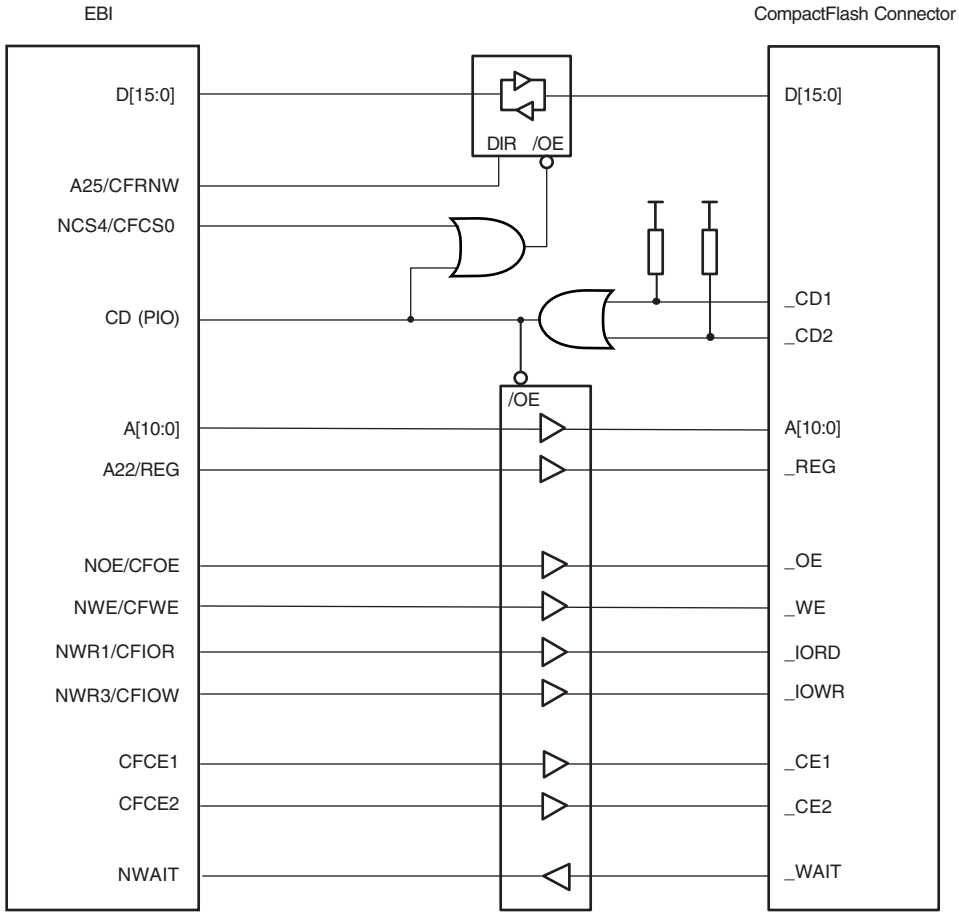
Table 16-9. Shared CompactFlash Interface Multiplexing

	Access to CompactFlash Device	**Access to Other EBI Devices**
Pins	**CompactFlash Signals**	**EBI Signals**
NOE/NRD/CFOE	CFOE	NRD/NOE
NWR0/NWE/CFWE	CFWE	NWR0/NWE
NWR1/NBS1/CFIOR	CFIOR	NWR1/NBS1
NWR3/NBS3/CFIOW	CFIOW	NWR3/NBS3
A25/CFRNW	CFRNW	A25

16.7.6.5 Application Example

Figure 16-5 on page 171 illustrates an example of a CompactFlash application. CFCS0 and CFRNW signals are not directly connected to the CompactFlash slot 0, but do control the direction and the output enable of the buffers between the EBI and the CompactFlash Device. The timing of the CFCS0 signal is identical to the NCS4 signal. Moreover, the CFRNW signal remains valid throughout the transfer, as does the address bus. The CompactFlash _WAIT signal is connected to the NWAIT input of the Static Memory Controller. For details on these waveforms and timings, refer to the Static Memory Controller Section.

Figure 16-5. CompactFlash Application Example



16.7.7 SmartMedia and NAND Flash Support

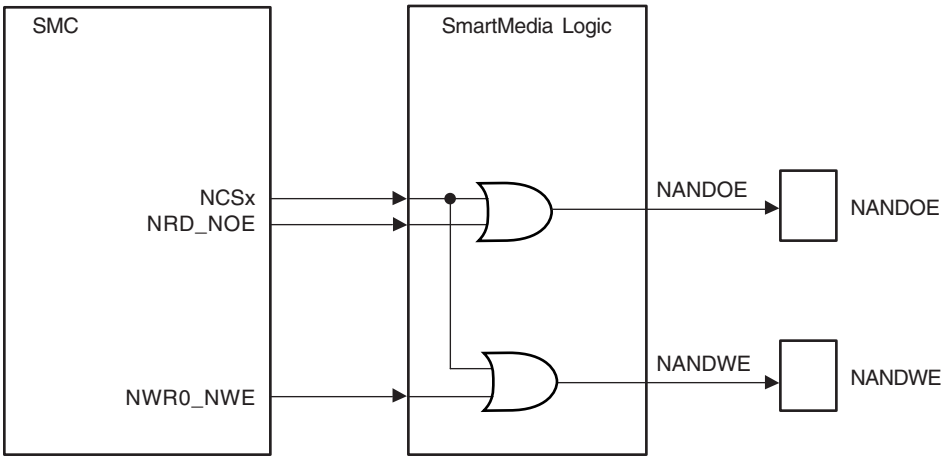
The External Bus Interface integrates circuitry that interfaces to SmartMedia and NAND Flash devices.

The NAND Flash logic is driven by the Static Memory Controller on the NCS3 address space. Programming the EBI_CS3A field in a specific HMATRIX_SFR Register to the appropriate value enables the NAND Flash logic. For details on this register, refer to the Peripherals Section. Access to an external NAND Flash device is then made by accessing the address space reserved to NCS3 (i.e., between 0x0C00 0000 and 0x0FFF FFFF).

The NAND Flash Logic drives the read and write command signals of the SMC on the NANDOE and NANDWE signals when the NCS3 signal is active. NANDOE and NANDWE are invalidated as soon as the transfer address fails to lie in the NCS3 address space. See Figure ”NAND Flash Signal Multiplexing on EBI Pins” on page 172 for more informations. For details on these waveforms, refer to the Static Memory Controller Section.

The SmartMedia device is connected the same way as the NAND Flash device.

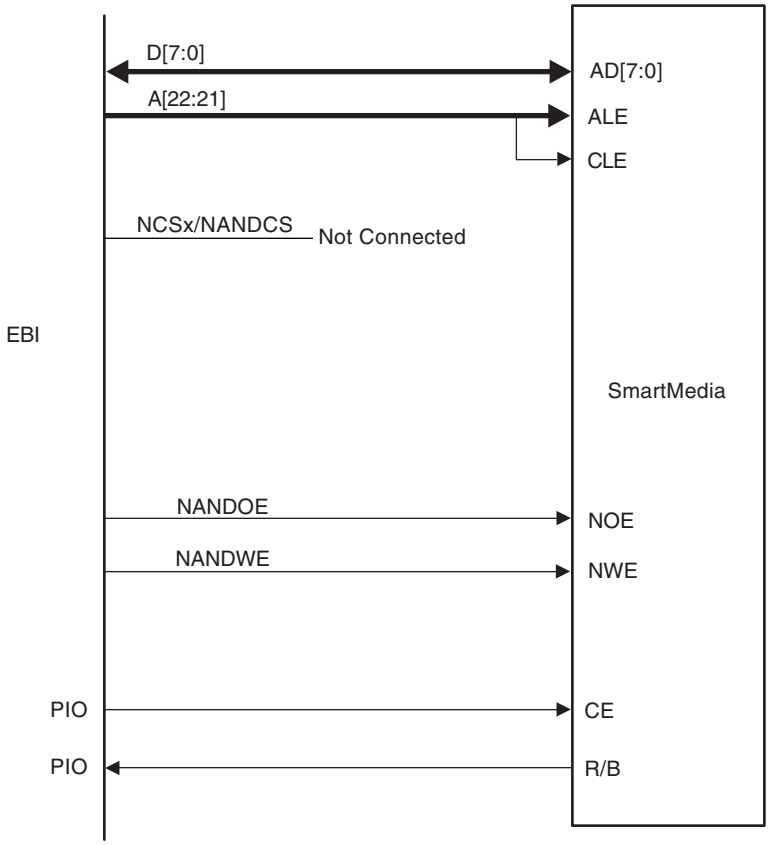
Figure 16-6. NAND Flash Signal Multiplexing on EBI Pins



16.7.7.1 NAND Flash Signals

The address latch enable and command latch enable signals on the NAND Flash device are driven by address bits A22 and A21 of the EBI address bus. The user should note that any bit on the EBI address bus can also be used for this purpose. The command, address or data words on the data bus of the NAND Flash device are distinguished by using their address within the NCSx address space. The chip enable (CE) signal of the device and the ready/busy (R/B) signals are connected to PIO lines. The CE signal then remains asserted even when NCSx is not selected, preventing the device from returning to standby mode.

Figure 16-7. NAND Flash Application Example



Note: The External Bus Interfaces is also able to support 16-bits devices.

17. DMA Controller (DMACA)

Rev: 2.0.0.6

17.1 Features

- 2 HSB Master Interfaces
- 3 Channels
- Software and Hardware Handshaking Interfaces
  - 11 Hardware Handshaking Interfaces
- Memory/Non-Memory Peripherals to Memory/Non-Memory Peripherals Transfer
- Single-block DMA Transfer
- Multi-block DMA Transfer
  - Linked Lists
  - Auto-Reloading
  - Contiguous Blocks
- DMA Controller is Always the Flow Controller
- Additional Features
  - Scatter and Gather Operations
  - Channel Locking
  - Bus Locking
  - FIFO Mode
  - Pseudo Fly-by Operation

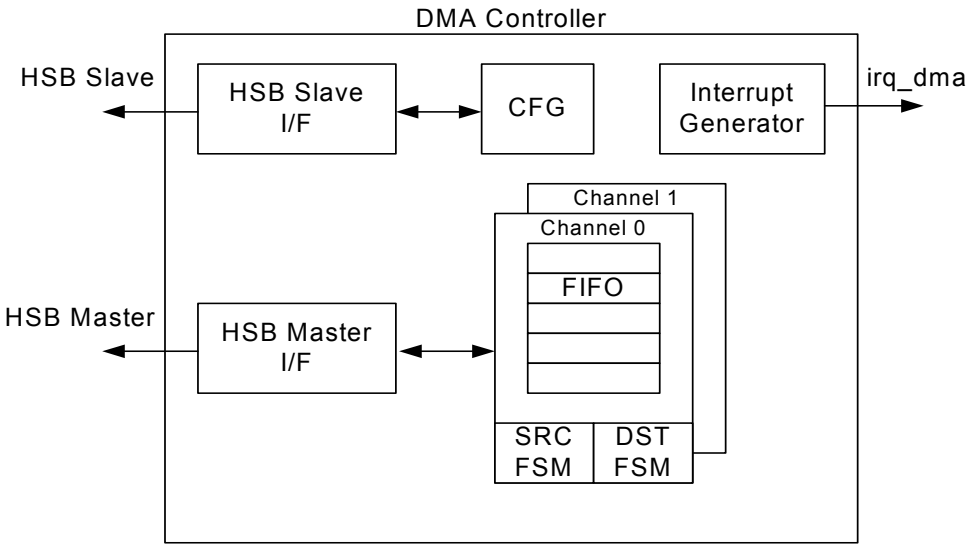
17.2 Overview

The DMA Controller (DMACA) is an HSB-central DMA controller core that transfers data from a source peripheral to a destination peripheral over one or more System Bus. One channel is required for each source/destination pair. In the most basic configuration, the DMACA has one master interface and one channel. The master interface reads the data from a source and writes it to a destination. Two System Bus transfers are required for each DMA data transfer. This is also known as a dual-access transfer.

The DMACA is programmed via the HSB slave interface.

17.3 Block Diagram

Figure 17-1. DMA Controller (DMACA) Block Diagram



17.4 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

17.4.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with GPIO lines. The user must first program the GPIO controller to assign the DMACA pins to their peripheral functions.

17.4.2 Power Management

To prevent bus errors the DMACA operation must be terminated before entering sleep mode.

17.4.3 Clocks

The CLK_DMACA to the DMACA is generated by the Power Manager (PM). Before using the DMACA, the user must ensure that the DMACA clock is enabled in the power manager.

17.4.4 Interrupts

The DMACA interface has an interrupt line connected to the Interrupt Controller. Handling the DMACA interrupt requires programming the interrupt controller before configuring the DMACA.

17.4.5 Peripherals

Both the source peripheral and the destination peripheral must be set up correctly prior to the DMA transfer.

17.5 Functional Description

17.5.1 Basic Definitions

Source peripheral: Device on a System Bus layer from where the DMACA reads data, which is then stored in the channel FIFO. The source peripheral teams up with a destination peripheral to form a channel.

Destination peripheral: Device to which the DMACA writes the stored data from the FIFO (previously read from the source peripheral).

Memory: Source or destination that is always “ready” for a DMA transfer and does not require a handshaking interface to interact with the DMACA. A peripheral should be assigned as memory only if it does not insert more than 16 wait states. If more than 16 wait states are required, then the peripheral should use a handshaking interface (the default if the peripheral is not programmed to be memory) in order to signal when it is ready to accept or supply data.

Channel: Read/write datapath between a source peripheral on one configured System Bus layer and a destination peripheral on the same or different System Bus layer that occurs through the channel FIFO. If the source peripheral is not memory, then a source handshaking interface is assigned to the channel. If the destination peripheral is not memory, then a destination handshaking interface is assigned to the channel. Source and destination handshaking interfaces can be assigned dynamically by programming the channel registers.

Master interface: DMACA is a master on the HSB bus reading data from the source and writing it to the destination over the HSB bus.

Slave interface: The HSB interface over which the DMACA is programmed. The slave interface in practice could be on the same layer as any of the master interfaces or on a separate layer.

Handshaking interface: A set of signal registers that conform to a protocol and *handshake* between the DMACA and source or destination peripheral to control the transfer of a single or burst transaction between them. This interface is used to request, acknowledge, and control a DMACA transaction. A channel can receive a request through one of three types of handshaking interface: hardware, software, or peripheral interrupt.

Hardware handshaking interface: Uses hardware signals to control the transfer of a single or burst transaction between the DMACA and the source or destination peripheral.

Software handshaking interface: Uses software registers to control the transfer of a single or burst transaction between the DMACA and the source or destination peripheral. No special DMACA handshaking signals are needed on the I/O of the peripheral. This mode is useful for interfacing an existing peripheral to the DMACA without modifying it.

Peripheral interrupt handshaking interface: A simple use of the hardware handshaking interface. In this mode, the interrupt line from the peripheral is tied to the dma_req input of the hardware handshaking interface. Other interface signals are ignored.

Flow controller: The device (either the DMACA or source/destination peripheral) that determines the length of and terminates a DMA block transfer. If the length of a block is known before enabling the channel, then the DMACA should be programmed as the flow controller. If the length of a block is not known prior to enabling the channel, the source or destination peripheral needs to terminate a block transfer. In this mode, the peripheral is the flow controller.

Flow control mode (CFGx.FCMODE): Special mode that only applies when the destination peripheral is the flow controller. It controls the pre-fetching of data from the source peripheral.

Transfer hierarchy: Figure 17-2 on page 177 illustrates the hierarchy between DMACA transfers, block transfers, transactions (single or burst), and System Bus transfers (single or burst) for non-memory peripherals. Figure 17-3 on page 177 shows the transfer hierarchy for memory.

Figure 17-2. DMACA Transfer Hierarchy for Non-Memory Peripheral

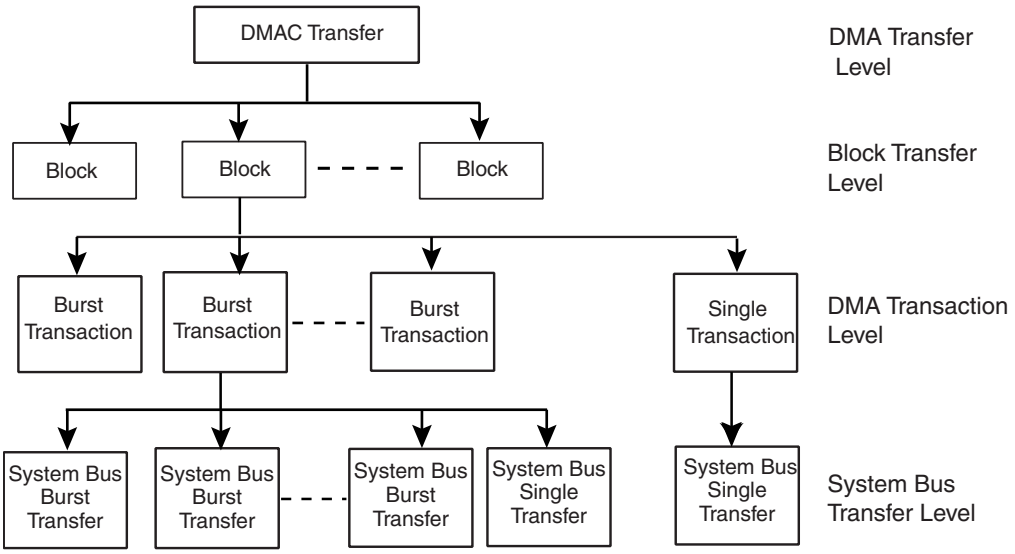
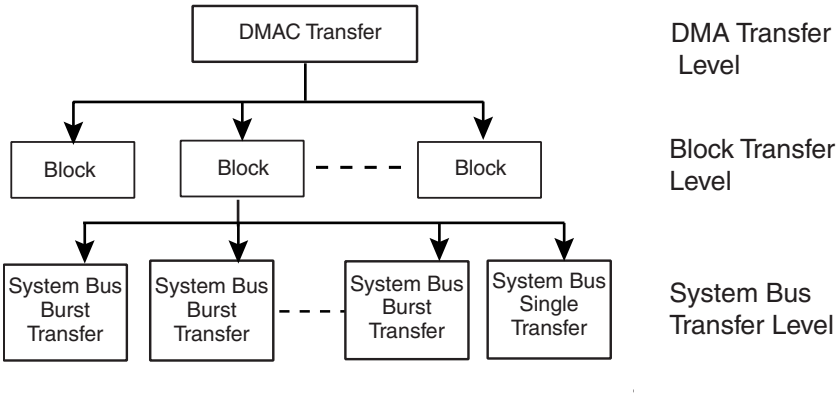


Figure 17-3. DMACA Transfer Hierarchy for Memory



Block: A block of DMACA data. The amount of data (block length) is determined by the flow controller. For transfers between the DMACA and memory, a block is broken directly into a sequence of System Bus bursts and single transfers. For transfers between the DMACA and a non-memory peripheral, a block is broken into a sequence of DMACA transactions (single and bursts). These are in turn broken into a sequence of System Bus transfers.

Transaction: A basic unit of a DMACA transfer as determined by either the hardware or software handshaking interface. A transaction is only relevant for transfers between the DMACA and a source or destination peripheral if the source or destination peripheral is a non-memory device. There are two types of transactions: single and burst.

- **Single transaction:** The length of a single transaction is always 1 and is converted to a single System Bus transfer.
- **Burst transaction:** The length of a burst transaction is programmed into the DMACA. The burst transaction is converted into a sequence of System Bus bursts and single transfers. DMACA executes each burst transfer by performing incremental bursts that are no longer than the maximum System Bus burst size set. The burst transaction length is under program control and normally bears some relationship to the FIFO sizes in the DMACA and in the source and destination peripherals.

DMA transfer: Software controls the number of blocks in a DMACA transfer. Once the DMA transfer has completed, then hardware within the DMACA disables the channel and can generate an interrupt to signal the completion of the DMA transfer. You can then re-program the channel for a new DMA transfer.

Single-block DMA transfer: Consists of a single block.

Multi-block DMA transfer: A DMA transfer may consist of multiple DMACA blocks. Multi-block DMA transfers are supported through block chaining (linked list pointers), auto-reloading of channel registers, and contiguous blocks. The source and destination can independently select which method to use.

- **Linked lists (block chaining) –** A linked list pointer (LLP) points to the location in system memory where the next linked list item (LLI) exists. The LLI is a set of registers that describe the next block (block descriptor) and an LLP register. The DMACA fetches the LLI at the beginning of every block when block chaining is enabled.
- **Auto-reloading –** The DMACA automatically reloads the channel registers at the end of each block to the value when the channel was first enabled.
- **Contiguous blocks –** Where the address between successive blocks is selected to be a continuation from the end of the previous block.

Scatter: Relevant to destination transfers within a block. The destination System Bus address is incremented or decremented by a programmed amount -the scatter increment- when a scatter boundary is reached. The destination System Bus address is incremented or decremented by the value stored in the destination scatter increment (DSRx.DSI) field, multiplied by the number of bytes in a single HSB transfer to the destination (decoded value of CTLx.DST_TR_WIDTH)/8. The number of destination transfers between successive scatter boundaries is programmed into the Destination Scatter Count (DSC) field of the DSRx register.

Scatter is enabled by writing a ‘1’ to the CTLx.DST_SCATTER_EN bit. The CTLx.DINC field determines if the address is incremented, decremented or remains fixed when a scatter boundary is reached. If the CTLx.DINC field indicates a fixed-address control throughout a DMA transfer, then the CTLx.DST_SCATTER_EN bit is ignored, and the scatter feature is automatically disabled.

Gather: Relevant to source transfers within a block. The source System Bus address is incremented or decremented by a programmed amount when a gather boundary is reached. The number of System Bus transfers between successive gather boundaries is programmed into the Source Gather Count (SGRx.SGC) field. The source address is incremented or decremented by the value stored in the source gather increment (SGRx.SGI) field multiplied by the number of bytes in a single HSB transfer from the source -(decoded value of CTLx.SRC_TR_WIDTH)/8 - when a gather boundary is reached.

Gather is enabled by writing a ‘1’ to the CTLx.SRC_GATHER_EN bit. The CTLx.SINC field determines if the address is incremented, decremented or remains fixed when a gather bound-

ary is reached. If the CTLx.SINC field indicates a fixed-address control throughout a DMA transfer, then the CTLx.SRC_GATHER_EN bit is ignored and the gather feature is automatically disabled.

Note: For multi-block transfers, the counters that keep track of the number of transfer left to reach a gather/scatter boundary are re-initialized to the source gather count (SGRx.SGC) and destination scatter count (DSRx.DSC), respectively, at the start of each block transfer.

Figure 17-4. Destination Scatter Transfer

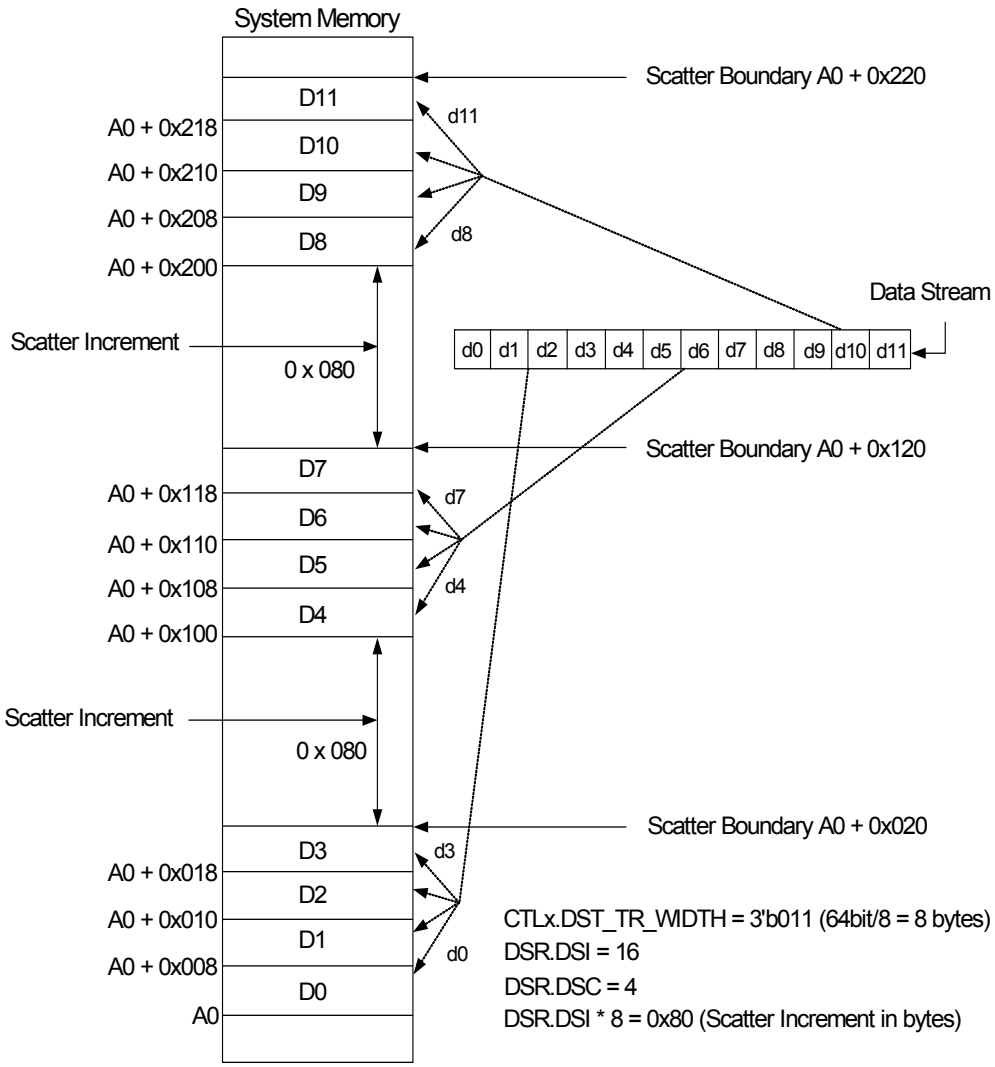
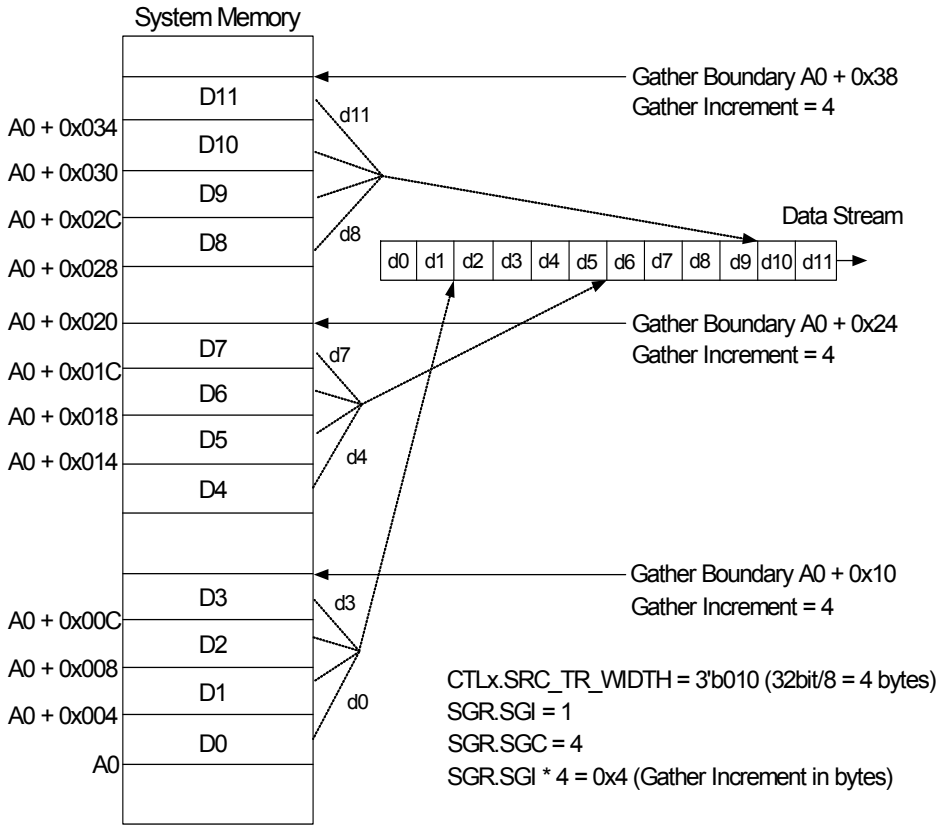


Figure 17-5. Source Gather Transfer



Channel locking: Software can program a channel to keep the HSB master interface by locking the arbitration for the master bus interface for the duration of a DMA transfer, block, or transaction (single or burst).

Bus locking: Software can program a channel to maintain control of the System Bus bus by asserting hlock for the duration of a DMA transfer, block, or transaction (single or burst). Channel locking is asserted for the duration of bus locking at a minimum.

FIFO mode: Special mode to improve bandwidth. When enabled, the channel waits until the FIFO is less than half full to fetch the data from the source peripheral and waits until the FIFO is greater than or equal to half full to send data to the destination peripheral. Thus, the channel can transfer the data using System Bus bursts, eliminating the need to arbitrate for the HSB master interface for each single System Bus transfer. When this mode is not enabled, the channel only waits until the FIFO can transmit/accept a single System Bus transfer before requesting the master bus interface.

Pseudo fly-by operation: Typically, it takes two System Bus cycles to complete a transfer, one for reading the source and one for writing to the destination. However, when the source and destination peripherals of a DMA transfer are on different System Bus layers, it is possible for the DMACA to fetch data from the source and store it in the channel FIFO at the same time as the DMACA extracts data from the channel FIFO and writes it to the destination peripheral. This activity is known as *pseudo fly-by operation*. For this to occur, the master interface for both source and destination layers must win arbitration of their HSB layer. Similarly, the source and destination peripherals must win ownership of their respective master interfaces.

17.6 Arbitration for HSB Master Interface

Each DMACA channel has two request lines that request ownership of a particular master bus interface: channel source and channel destination request lines.

Source and destination arbitrate separately for the bus. Once a source/destination state machine gains ownership of the master bus interface and the master bus interface has ownership of the HSB bus, then HSB transfers can proceed between the peripheral and the DMACA.

An arbitration scheme decides which of the request lines (2 * DMAH_NUM_CHANNELS) is granted the particular master bus interface. Each channel has a programmable priority. A request for the master bus interface can be made at any time, but is granted only after the current HSB transfer (burst or single) has completed. Therefore, if the master interface is transferring data for a lower priority channel and a higher priority channel requests service, then the master interface will complete the current burst for the lower priority channel before switching to transfer data for the higher priority channel.

If only one request line is active at the highest priority level, then the request with the highest priority wins ownership of the HSB master bus interface; it is not necessary for the priority levels to be unique.

If more than one request is active at the highest requesting priority, then these competing requests proceed to a second tier of arbitration:

If equal priority requests occur, then the lower-numbered channel is granted.

In other words, if a peripheral request attached to Channel 7 and a peripheral request attached to Channel 8 have the same priority, then the peripheral attached to Channel 7 is granted first.

17.7 Memory Peripherals

Figure 17-3 on page 177 shows the DMA transfer hierarchy of the DMACA for a memory peripheral. There is no handshaking interface with the DMACA, and therefore the memory peripheral can never be a flow controller. Once the channel is enabled, the transfer proceeds immediately without waiting for a transaction request. The alternative to not having a transaction-level handshaking interface is to allow the DMACA to attempt System Bus transfers to the peripheral once the channel is enabled. If the peripheral slave cannot accept these System Bus transfers, it inserts wait states onto the bus until it is ready; it is not recommended that more than 16 wait states be inserted onto the bus. By using the handshaking interface, the peripheral can signal to the DMACA that it is ready to transmit/receive data, and then the DMACA can access the peripheral without the peripheral inserting wait states onto the bus.

17.8 Handshaking Interface

Handshaking interfaces are used at the transaction level to control the flow of single or burst transactions. The operation of the handshaking interface is different and depends on whether the peripheral or the DMACA is the flow controller.

The peripheral uses the handshaking interface to indicate to the DMACA that it is ready to transfer/accept data over the System Bus. A non-memory peripheral can request a DMA transfer through the DMACA using one of two handshaking interfaces:

- Hardware handshaking
- Software handshaking

Software selects between the hardware or software handshaking interface on a per-channel basis. Software handshaking is accomplished through memory-mapped registers, while hardware handshaking is accomplished using a dedicated handshaking interface.

17.8.1 Software Handshaking

When the slave peripheral requires the DMACA to perform a DMA transaction, it communicates this request by sending an interrupt to the CPU or interrupt controller.

The interrupt service routine then uses the software registers to initiate and control a DMA transaction. These software registers are used to implement the software handshaking interface.

The HS_SEL_SRC/HS_SEL_DST bit in the CFGx channel configuration register must be set to enable software handshaking.

When the peripheral is not the flow controller, then the last transaction registers LstSrcReg and LstDstReg are not used, and the values in these registers are ignored.

17.8.1.1 Burst Transactions

Writing a 1 to the ReqSrcReg[x]/ReqDstReg[x] register is always interpreted as a burst transaction request, where *x* is the channel number. However, in order for a burst transaction request to start, software must write a 1 to the SglReqSrcReg[x]/SglReqDstReg[x] register.

You can write a 1 to the SglReqSrcReg[*x*]/SglReqDstReg[*x*] and ReqSrcReg[*x*]/ReqDstReg[*x*] registers in any order, but both registers must be asserted in order to initiate a burst transaction. Upon completion of the burst transaction, the hardware clears the SglReqSrcReg[*x*]/SglReqDstReg[*x*] and ReqSrcReg[*x*]/ReqDstReg[*x*] registers.

17.8.1.2 Single Transactions

Writing a 1 to the SglReqSrcReg/SglReqDstReg initiates a single transaction. Upon completion of the single transaction, both the SglReqSrcReg/SglReqDstReg and ReqSrcReg/ReqDstReg bits are cleared by hardware. Therefore, writing a 1 to the ReqSrcReg/ReqDstReg is ignored while a single transaction has been initiated, and the requested burst transaction is not serviced.

Again, writing a 1 to the ReqSrcReg/ReqDstReg register is always a burst transaction request. However, in order for a burst transaction request to start, the corresponding channel bit in the SglReqSrcReg/SglReqDstReg must be asserted. Therefore, to ensure that a burst transaction is serviced, you must write a 1 to the ReqSrcReg/ReqDstReg before writing a 1 to the SglReqSrcReg/SglReqDstReg register.

Software can poll the relevant channel bit in the SglReqSrcReg/ SglReqDstReg and ReqSrcReg/ReqDstReg registers. When both are 0, then either the requested burst or single transaction has completed. Alternatively, the IntSrcTran or IntDstTran interrupts can be enabled and unmasked in order to generate an interrupt when the requested source or destination transaction has completed.

Note: The transaction-complete interrupts are triggered when both single and burst transactions are complete. The same transaction-complete interrupt is used for both single and burst transactions.

17.8.2 Hardware Handshaking

There are 11 hardware handshaking interfaces between the DMACA and peripherals. Refer to the module configuration chapter for the device-specific mapping of these interfaces.

17.8.2.1 External DMA Request Definition

When an external slave peripheral requires the DMACA to perform DMA transactions, it communicates its request by asserting the external nDMAREQx signal. This signal is resynchronized to ensure a proper functionality (see "External DMA Request Timing" on page 183).

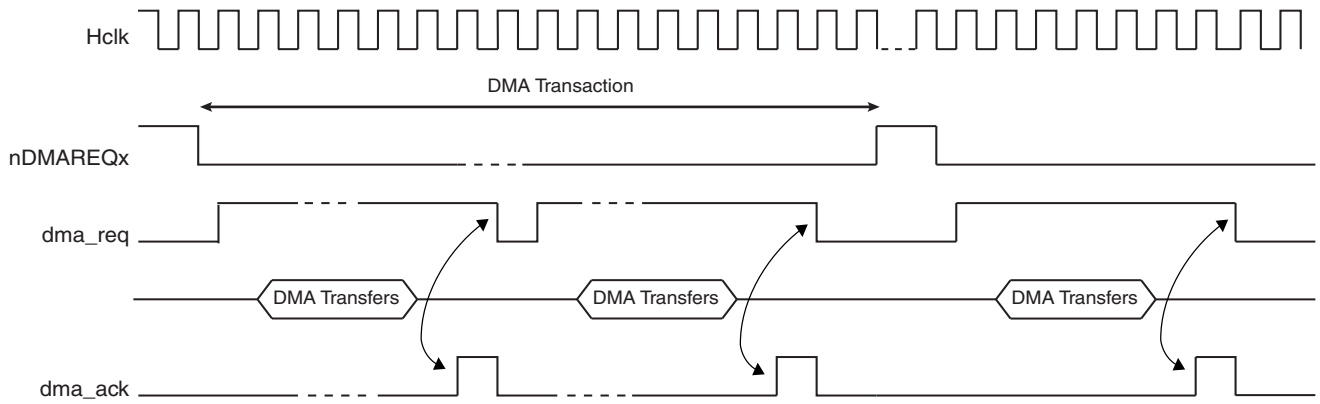
The external nDMAREQx signal should be asserted when the source threshold level is reached. After resynchronization, the rising edge of dma_req starts the transfer.

The external nDMAREQx signal must be de-asserted after the last transfer and re-asserted again before a new transaction starts.

For a source FIFO, an active edge should be triggered on nDMAREQx when the source FIFO exceeds a watermark level. For a destination FIFO, an active edge should be triggered on nDMAREQx when the destination FIFO drops below the watermark level.

The source transaction length, CTLx.SRC_MSIZE, and destination transaction length, CTLx.DEST_MSIZE, must be set according to watermark levels on the source/destination peripherals.

Figure 17-6. External DMA Request Timing



17.9 DMACA Transfer Types

A DMA transfer may consist of single or multi-block transfers. On successive blocks of a multi-block transfer, the SARx/DARx register in the DMACA is reprogrammed using either of the following methods:

- Block chaining using linked lists
- Auto-reloading
- Contiguous address between blocks

On successive blocks of a multi-block transfer, the CTLx register in the DMACA is re-programmed using either of the following methods:

- Block chaining using linked lists
- Auto-reloading

When block chaining, using linked lists is the multi-block method of choice, and on successive blocks, the LLPx register in the DMACA is re-programmed using the following method:

- Block chaining using linked lists

A block descriptor (LLI) consists of following registers, SARx, DARx, LLPx, CTL. These registers, along with the CFGx register, are used by the DMACA to set up and describe the block transfer.

17.9.1 Multi-block Transfers

17.9.1.1 Block Chaining Using Linked Lists

In this case, the DMACA re-programs the channel registers prior to the start of each block by fetching the block descriptor for that block from system memory. This is known as an LLI update.

DMACA block chaining is supported by using a Linked List Pointer register (LLPx) that stores the address in memory of the next linked list item. Each LLI (block descriptor) contains the corresponding block descriptor (SARx, DARx, LLPx, CTLx).

To set up block chaining, a sequence of linked lists must be programmed in memory.

The SARx, DARx, LLPx and CTLx registers are fetched from system memory on an LLI update. The updated contents of the CTLx register are written back to memory on block completion. Figure 17-7 on page 184 shows how to use chained linked lists in memory to define multi-block transfers using block chaining.

The Linked List multi-block transfers is initiated by programming LLPx with LLPx(0) (LLI(0) base address) and CTLx with CTLx.LLP_S_EN and CTLx.LLP_D_EN.

Figure 17-7. Multi-block Transfer Using Linked Lists

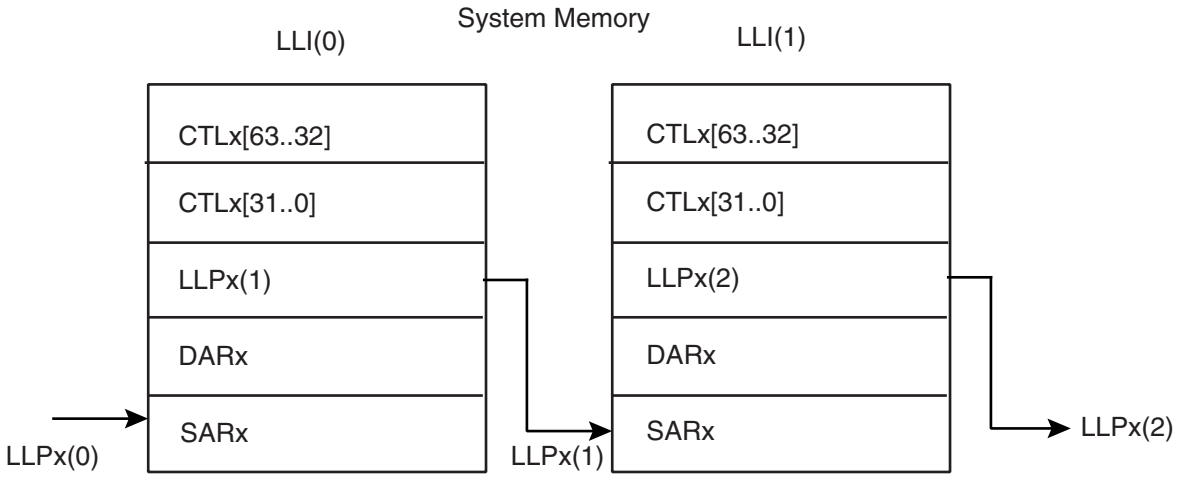


Table 17-1. Programming of Transfer Types and Channel Register Update Method (DMACA State Machine Table)

Transfer Type	LLP.LOC = 0	LLP_S_EN (CTLx)	RELOAD_SR (CFGx)	LLP_D_EN (CTLx)	RELOAD_DS (CFGx)	CTLx, LLPx Update Method	SARx Update Method	DARx Update Method	Write Back
1) Single Block or last transfer of multi-Block	Yes	0	0	0	0	None, user reprograms	None (single)	None (single)	No
2) Auto Reload multi-block transfer with contiguous SAR	Yes	0	0	0	1	CTLx,LLPx are reloaded from initial values.	Contiguous	Auto-Reload	No
3) Auto Reload multi-block transfer with contiguous DAR	Yes	0	1	0	0	CTLx,LLPx are reloaded from initial values.	Auto-Reload	Con-tiguous	No
4) Auto Reload multi-block transfer	Yes	0	1	0	1	CTLx,LLPx are reloaded from initial values.	Auto-Reload	Auto-Reload	No
5) Single Block or last transfer of multi-block	No	0	0	0	0	None, user reprograms	None (single)	None (single)	Yes
6) Linked List multi-block transfer with contiguous SAR	No	0	0	1	0	CTLx,LLPx loaded from next Linked List item	Contiguous	Linked List	Yes
7) Linked List multi-block transfer with auto-reload SAR	No	0	1	1	0	CTLx,LLPx loaded from next Linked List item	Auto-Reload	Linked List	Yes
8) Linked List multi-block transfer with contiguous DAR	No	1	0	0	0	CTLx,LLPx loaded from next Linked List item	Linked List	Con-tiguous	Yes
9) Linked List multi-block transfer with auto-reload DAR	No	1	0	0	1	CTLx,LLPx loaded from next Linked List item	Linked List	Auto-Reload	Yes
10) Linked List multi-block transfer	No	1	0	1	0	CTLx,LLPx loaded from next Linked List item	Linked List	Linked List	Yes

17.9.1.2 Auto-reloading of Channel Registers

During auto-reloading, the channel registers are reloaded with their initial values at the completion of each block and the new values used for the new block. Depending on the row number in Table 17-1 on page 185, some or all of the SARx, DARx and CTLx channel registers are reloaded from their initial value at the start of a block transfer.

17.9.1.3 Contiguous Address Between Blocks

In this case, the address between successive blocks is selected to be a continuation from the end of the previous block. Enabling the source or destination address to be contiguous between

blocks is a function of CTLx.LLP_S_EN, CFGx.RELOAD_SR, CTLx.LLP_D_EN, and CFGx.RELOAD_DS registers (see Figure 17-1 on page 175).

Note: Both SARx and DARx updates cannot be selected to be contiguous. If this functionality is required, the size of the Block Transfer (CTLx.BLOCK_TS) must be increased. If this is at the maximum value, use Row 10 of Table 17-1 on page 185 and setup the LLI.SARx address of the block descriptor to be equal to the end SARx address of the previous block. Similarly, setup the LLI.DARx address of the block descriptor to be equal to the end DARx address of the previous block.

17.9.1.4 Suspension of Transfers Between Blocks

At the end of every block transfer, an end of block interrupt is asserted if:

- interrupts are enabled, CTLx.INT_EN = 1
- the channel block interrupt is unmasked, MaskBlock[n] = 0, where n is the channel number.

Note: The block complete interrupt is generated at the completion of the block transfer to the destination.

For rows 6, 8, and 10 of Table 17-1 on page 185, the DMA transfer does not stall between block transfers. For example, at the end of block N, the DMACA automatically proceeds to block N + 1.

For rows 2, 3, 4, 7, and 9 of Table 17-1 on page 185 (SARx and/or DARx auto-reloaded between block transfers), the DMA transfer automatically stalls after the end of block. Interrupt is asserted if the end of block interrupt is enabled and unmasked.

The DMACA does not proceed to the next block transfer until a write to the block interrupt clear register, ClearBlock[n], is performed by software. This clears the channel block complete interrupt.

For rows 2, 3, 4, 7, and 9 of Table 17-1 on page 185 (SARx and/or DARx auto-reloaded between block transfers), the DMA transfer does not stall if either:

- interrupts are disabled, CTLx.INT_EN = 0, or
- the channel block interrupt is masked, MaskBlock[n] = 1, where n is the channel number.

Channel suspension between blocks is used to ensure that the end of block ISR (interrupt service routine) of the next-to-last block is serviced before the start of the final block commences. This ensures that the ISR has cleared the CFGx.RELOAD_SR and/or CFGx.RELOAD_DS bits before completion of the final block. The reload bits CFGx.RELOAD_SR and/or CFGx.RELOAD_DS should be cleared in the ‘end of block ISR’ for the next-to-last block transfer.

17.9.2 Ending Multi-block Transfers

All multi-block transfers must end as shown in either Row 1 or Row 5 of Table 17-1 on page 185. At the end of every block transfer, the DMACA samples the row number, and if the DMACA is in Row 1 or Row 5 state, then the previous block transferred was the last block and the DMA transfer is terminated.

Note: Row 1 and Row 5 are used for single block transfers or terminating multiblock transfers. Ending in Row 5 state enables status fetch for the last block. Ending in Row 1 state disables status fetch for the last block.

For rows 2,3 and 4 of Table 17-1 on page 185, (LLPx = 0 and CFGx.RELOAD_SR and/or CFGx.RELOAD_DS is set), multi-block DMA transfers continue until both the CFGx.RELOAD_SR and CFGx.RELOAD_DS registers are cleared by software. They should be

programmed to zero in the end of block interrupt service routine that services the next-to-last block transfer. This puts the DMACA into Row 1 state.

For rows 6, 8, and 10 (both CFGx.RELOAD_SR and CFGx.RELOAD_DS cleared) the user must setup the last block descriptor in memory such that both LLI.CTLx.LLP_S_EN and LLI.CTLx.LLP_D_EN are zero. If the LLI.LLPx register of the last block descriptor in memory is non-zero, then the DMA transfer is terminated in Row 5. If the LLI.LLPx register of the last block descriptor in memory is zero, then the DMA transfer is terminated in Row 1.

For rows 7 and 9, the end-of-block interrupt service routine that services the next-to-last block transfer should clear the CFGx.RELOAD_SR and CFGx.RELOAD_DS reload bits. The last block descriptor in memory should be set up so that both the LLI.CTLx.LLP_S_EN and LLI.CTLx.LLP_D_EN are zero. If the LLI.LLPx register of the last block descriptor in memory is non-zero, then the DMA transfer is terminated in Row 5. If the LLI.LLPx register of the last block descriptor in memory is zero, then the DMA transfer is terminated in Row 1.

Note: The only allowed transitions between the rows of Table 17-1 on page 185are from any row into row 1 or row 5. As already stated, a transition into row 1 or row 5 is used to terminate the DMA transfer. All other transitions between rows are not allowed. Software must ensure that illegal transitions between rows do not occur between blocks of a multi-block transfer. For example, if block N is in row 10 then the only allowed rows for block N + 1 are rows 10, 5 or 1.

17.10 Programming a Channel

Three registers, the LLPx, the CTLx and CFGx, need to be programmed to set up whether single or multi-block transfers take place, and which type of multi-block transfer is used. The different transfer types are shown in Table 17-1 on page 185.

The “Update Method” column indicates where the values of SARx, DARx, CTLx, and LLPx are obtained for the next block transfer when multi-block DMACA transfers are enabled.

Note: In Table 17-1 on page 185, all other combinations of LLPx.LOC = 0, CTLx.LLP_S_EN, CFGx.RELOAD_SR, CTLx.LLP_D_EN, and CFGx.RELOAD_DS are illegal, and causes indeterminate or erroneous behavior.

17.10.1 Programming Examples

17.10.1.1 Single-block Transfer (Row 1)

Row 5 in Table 17-1 on page 185 is also a single block transfer.

1. Read the Channel Enable register to choose a free (disabled) channel.
2. Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.
3. Program the following channel registers:
   a. Write the starting source address in the SARx register for channel x.
   b. Write the starting destination address in the DARx register for channel x.
   c. Program CTLx and CFGx according to Row 1 as shown in Table 17-1 on page 185. Program the LLPx register with ‘0’.
   d. Write the control information for the DMA transfer in the CTLx register for channel x. For example, in the register, you can program the following:

   – i. Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TT_FC of the CTLx register.

– ii. Set up the transfer characteristics, such as:
  – Transfer width for the source in the SRC_TR_WIDTH field.
  – Transfer width for the destination in the DST_TR_WIDTH field.
  – Source master layer in the SMS field where source resides.
  – Destination master layer in the DMS field where destination resides.
  – Incrementing/decrementing or fixed address for source in SINC field.
  – Incrementing/decrementing or fixed address for destination in DINC field.

e. Write the channel configuration information into the CFGx register for channel x.

– i. Designate the handshaking interface type (hardware or software) for the source and destination peripherals. This is not required for memory. This step requires programming the HS_SEL_SRC/HS_SEL_DST bits, respectively. Writing a '0' activates the hardware handshaking interface to handle source/destination requests. Writing a '1' activates the software handshaking interface to handle source/destination requests.

– ii. If the hardware handshaking interface is activated for the source or destination peripheral, assign a handshaking interface to the source and destination peripheral. This requires programming the SRC_PER and DEST_PER bits, respectively.

4. After the DMACA selected channel has been programmed, enable the channel by writing a '1' to the ChEnReg.CH_EN bit. Make sure that bit 0 of the DmaCfgReg register is enabled.
5. Source and destination request single and burst DMA transactions to transfer the block of data (assuming non-memory peripherals). The DMACA acknowledges at the completion of every transaction (burst and single) in the block and carry out the block transfer.
6. Once the transfer completes, hardware sets the interrupts and disables the channel. At this time you can either respond to the Block Complete or Transfer Complete interrupts, or poll for the Channel Enable (ChEnReg.CH_EN) bit until it is cleared by hardware, to detect when the transfer is complete.

17.10.1.2 Multi-block Transfer with Linked List for Source and Linked List for Destination (Row 10)

1. Read the Channel Enable register to choose a free (disabled) channel.
2. Set up the chain of Linked List Items (otherwise known as block descriptors) in memory. Write the control information in the LLI.CTLx register location of the block descriptor for each LLI in memory (see Figure 17-7 on page 184) for channel x. For example, in the register, you can program the following:

   a. Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TT_FC of the CTLx register.

   b. Set up the transfer characteristics, such as:

   – i. Transfer width for the source in the SRC_TR_WIDTH field.

   – ii. Transfer width for the destination in the DST_TR_WIDTH field.

   – iii. Source master layer in the SMS field where source resides.

   – iv. Destination master layer in the DMS field where destination resides.

   – v. Incrementing/decrementing or fixed address for source in SINC field.

   – vi. Incrementing/decrementing or fixed address for destination DINC field.

3. Write the channel configuration information into the CFGx register for channel x.

   a. Designate the handshaking interface type (hardware or software) for the source and destination peripherals. This is not required for memory. This step requires program-

ming the HS_SEL_SRC/HS_SEL_DST bits, respectively. Writing a ‘0’ activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a ‘1’ activates the software handshaking interface to handle source/destination requests.

b. If the hardware handshaking interface is activated for the source or destination peripheral, assign the handshaking interface to the source and destination peripheral. This requires programming the SRC_PER and DEST_PER bits, respectively.

4. Make sure that the LLI.CTLx register locations of all LLI entries in memory (except the last) are set as shown in Row 10 of Table 17-1 on page 185. The LLI.CTLx register of the last Linked List Item must be set as described in Row 1 or Row 5 of Table 17-1 on page 185. Figure 17-9 on page 191 shows a Linked List example with two list items.
5. Make sure that the LLI.LLPx register locations of all LLI entries in memory (except the last) are non-zero and point to the base address of the next Linked List Item.
6. Make sure that the LLI.SARx/LLI.DARx register locations of all LLI entries in memory point to the start source/destination block address preceding that LLI fetch.
7. Make sure that the LLI.CTLx.DONE field of the LLI.CTLx register locations of all LLI entries in memory are cleared.
8. Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.
9. Program the CTLx, CFGx registers according to Row 10 as shown in Table 17-1 on page 185.
10. Program the LLPx register with LLPx(0), the pointer to the first Linked List item.
11. Finally, enable the channel by writing a ‘1’ to the ChEnReg.CH_EN bit. The transfer is performed.
12. The DMACA fetches the first LLI from the location pointed to by LLPx(0).

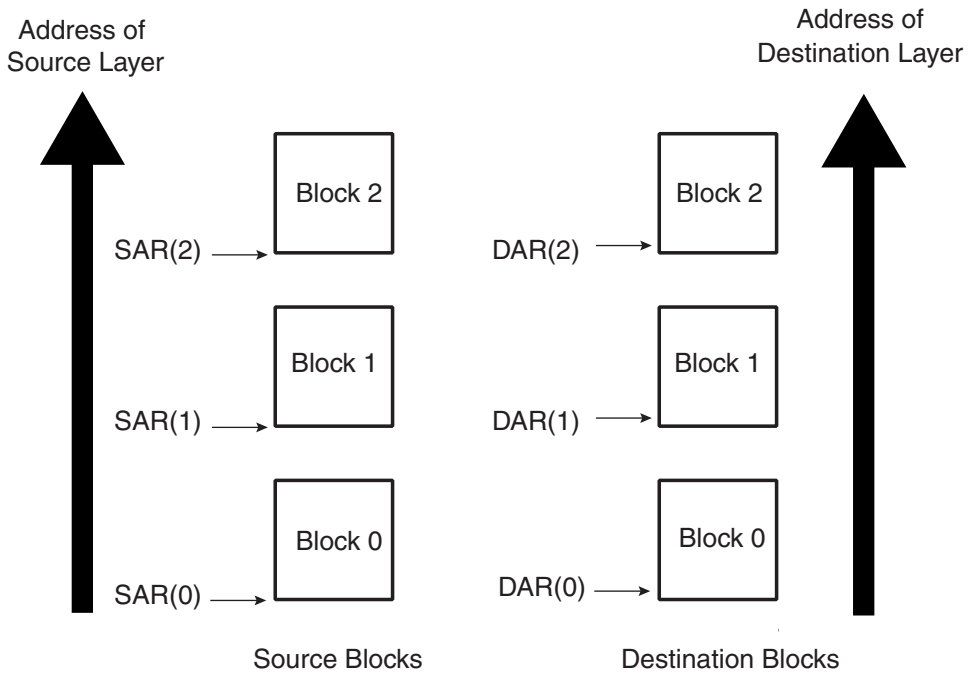
Note: The LLI.SARx, LLI. DARx, LLI.LLPx and LLI.CTLx registers are fetched. The DMACA automatically reprograms the SARx, DARx, LLPx and CTLx channel registers from the LLPx(0).

13. Source and destination request single and burst DMA transactions to transfer the block of data (assuming non-memory peripheral). The DMACA acknowledges at the completion of every transaction (burst and single) in the block and carry out the block transfer.

Note: Table 17-1 on page 185

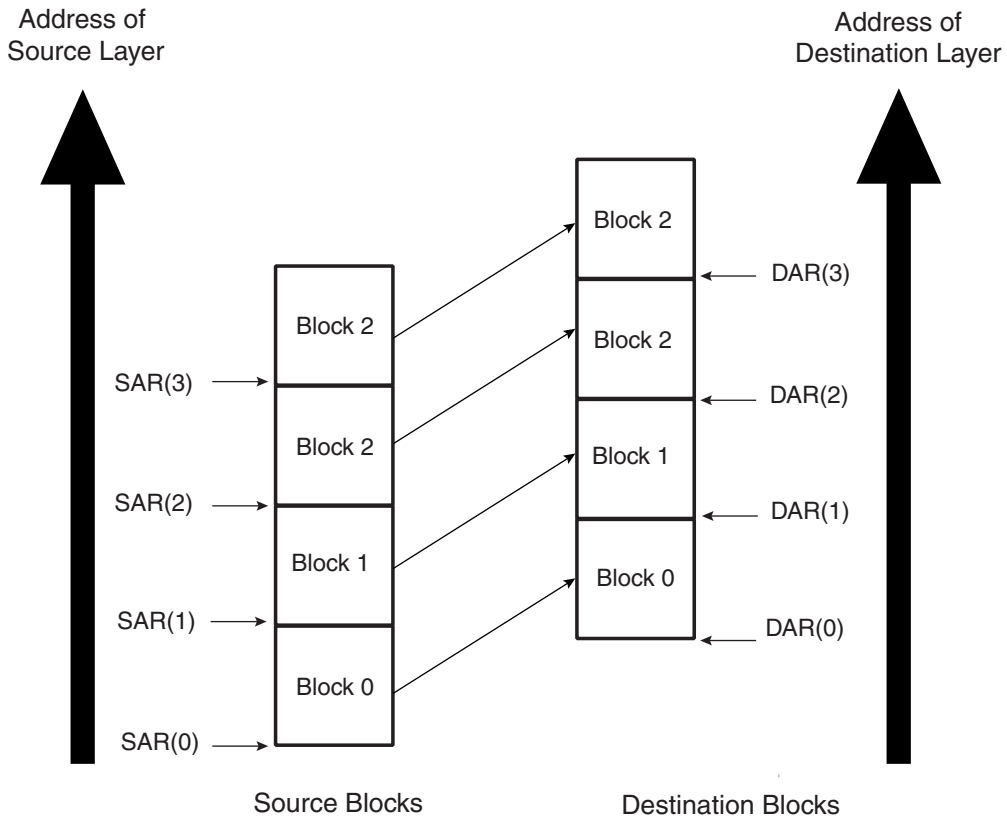
14. The DMACA does not wait for the block interrupt to be cleared, but continues fetching the next LLI from the memory location pointed to by current LLPx register and automatically reprograms the SARx, DARx, LLPx and CTLx channel registers. The DMA transfer continues until the DMACA determines that the CTLx and LLPx registers at the end of a block transfer match that described in Row 1 or Row 5 of Table 17-1 on page 185. The DMACA then knows that the previous block transferred was the last block in the DMA transfer. The DMA transfer might look like that shown in Figure 17-8 on page 190.

Figure 17-8. Multi-Block with Linked List Address for Source and Destination



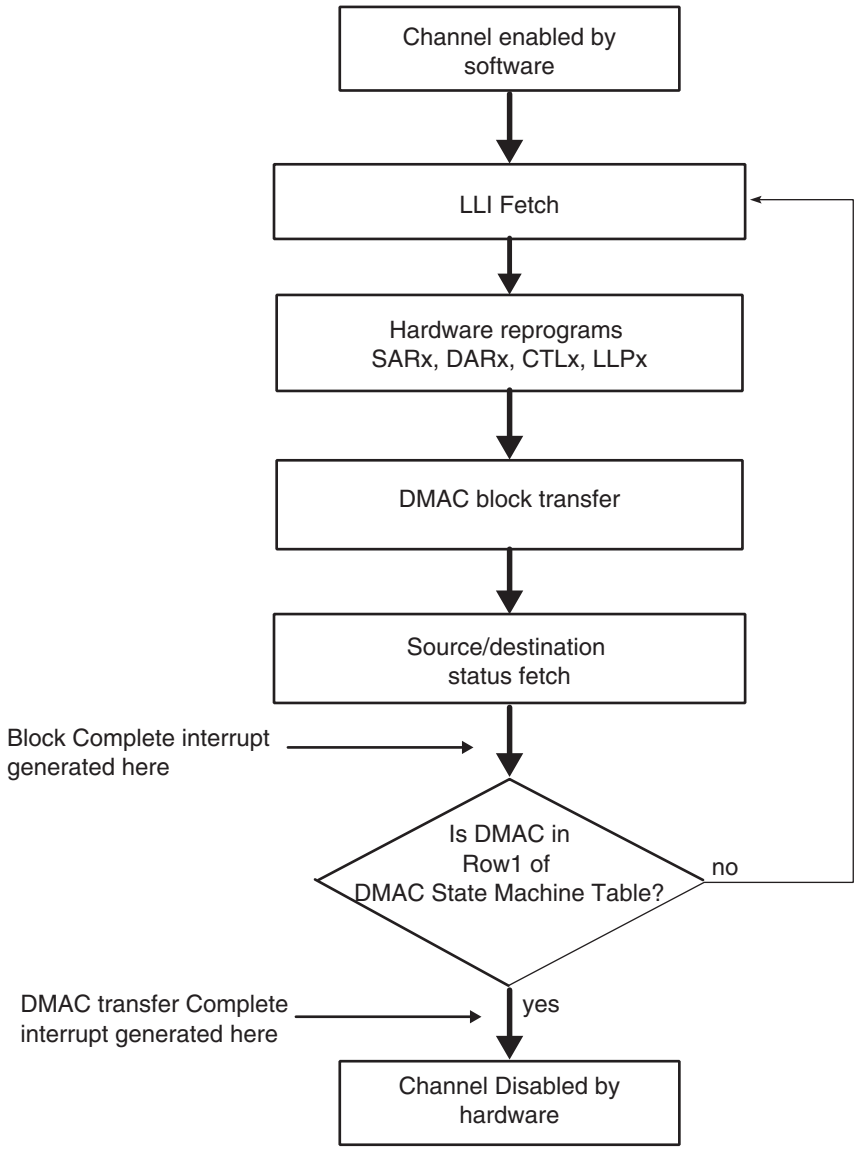
If the user needs to execute a DMA transfer where the source and destination address are contiguous but the amount of data to be transferred is greater than the maximum block size CTLx.BLOCK_TS, then this can be achieved using the type of multi-block transfer as shown in Figure 17-9 on page 191.

Figure 17-9. Multi-Block with Linked Address for Source and Destination Blocks are Contiguous



The DMA transfer flow is shown in Figure 17-11 on page 194.

Figure 17-10. DMA Transfer Flow for Source and Destination Linked List Address



17.10.1.3 Multi-block Transfer with Source Address Auto-reloaded and Destination Address Auto-reloaded (Row 4)

1. Read the Channel Enable register to choose an available (disabled) channel.
2. Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.
3. Program the following channel registers:

a. Write the starting source address in the SARx register for channel x.
b. Write the starting destination address in the DARx register for channel x.
c. Program CTLx and CFGx according to Row 4 as shown in Table 17-1 on page 185. Program the LLPx register with '0'.
d. Write the control information for the DMA transfer in the CTLx register for channel x. For example, in the register, you can program the following:

– i. Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TT_FC of the CTLx register.
– ii. Set up the transfer characteristics, such as:
  – Transfer width for the source in the SRC_TR_WIDTH field.
  – Transfer width for the destination in the DST_TR_WIDTH field.
  – Source master layer in the SMS field where source resides.
  – Destination master layer in the DMS field where destination resides.
  – Incrementing/decrementing or fixed address for source in SINC field.
  – Incrementing/decrementing or fixed address for destination in DINC field.

e. Write the channel configuration information into the CFGx register for channel x. Ensure that the reload bits, CFGx. RELOAD_SR and CFGx.RELOAD_DS are enabled.

– i. Designate the handshaking interface type (hardware or software) for the source and destination peripherals. This is not required for memory. This step requires programming the HS_SEL_SRC/HS_SEL_DST bits, respectively. Writing a '0' activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a '1' activates the software handshaking interface to handle source/destination requests.
– ii. If the hardware handshaking interface is activated for the source or destination peripheral, assign handshaking interface to the source and destination peripheral. This requires programming the SRC_PER and DEST_PER bits, respectively.

4. After the DMACA selected channel has been programmed, enable the channel by writing a '1' to the ChEnReg.CH_EN bit. Make sure that bit 0 of the DmaCfgReg register is enabled.
5. Source and destination request single and burst DMACA transactions to transfer the block of data (assuming non-memory peripherals). The DMACA acknowledges on completion of each burst/single transaction and carry out the block transfer.
6. When the block transfer has completed, the DMACA reloads the SARx, DARx and CTLx registers. Hardware sets the Block Complete interrupt. The DMACA then samples the row number as shown in Table 17-1 on page 185. If the DMACA is in Row 1, then the DMA transfer has completed. Hardware sets the transfer complete interrupt and disables the channel. So you can either respond to the Block Complete or Transfer Complete interrupts, or poll for the Channel Enable (ChEnReg.CH_EN) bit until it is disabled, to detect when the transfer is complete. If the DMACA is not in Row 1, the next step is performed.
7. The DMA transfer proceeds as follows:
   a. If interrupts are enabled (CTLx.INT_EN = 1) and the block complete interrupt is unmasked (MaskBlock[x] = 1'b1, where x is the channel number) hardware sets the block complete interrupt when the block transfer has completed. It then stalls until the block complete interrupt is cleared by software. If the next block is to be the last block in the DMA transfer, then the block complete ISR (interrupt service routine) should

clear the reload bits in the CFGx.RELOAD_SR and CFGx.RELOAD_DS registers. This put the DMACA into Row 1 as shown in Table 17-1 on page 185. If the next block is not the last block in the DMA transfer, then the reload bits should remain enabled to keep the DMACA in Row 4.

b. If interrupts are disabled (CTLx.INT_EN = 0) or the block complete interrupt is masked (MaskBlock[x] = 1'b0, where x is the channel number), then hardware does not stall until it detects a write to the block complete interrupt clear register but starts the next block transfer immediately. In this case software must clear the reload bits in the CFGx.RELOAD_SR and CFGx.RELOAD_DS registers to put the DMACA into ROW 1 of Table 17-1 on page 185 before the last block of the DMA transfer has completed. The transfer is similar to that shown in Figure 17-11 on page 194. The DMA transfer flow is shown in Figure 17-12 on page 195.

Figure 17-11. Multi-Block DMA Transfer with Source and Destination Address Auto-reloaded

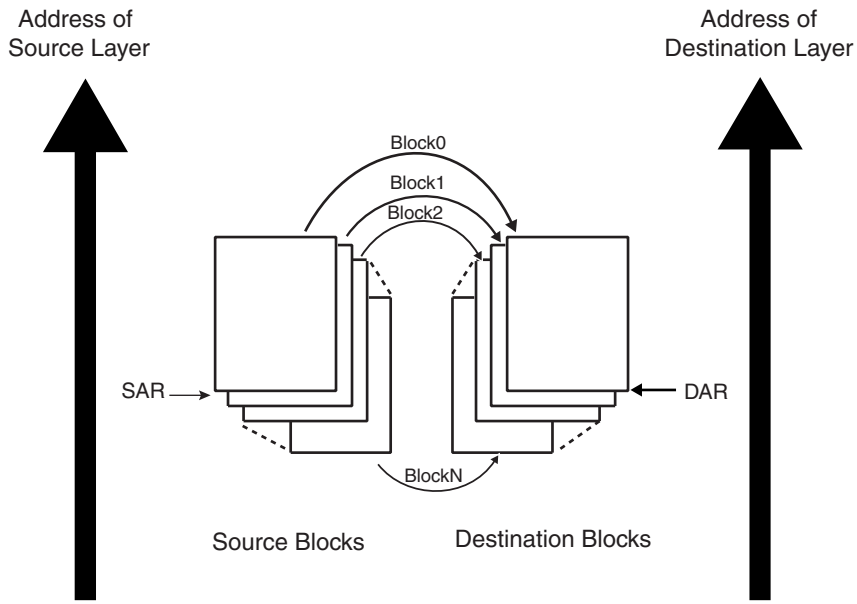
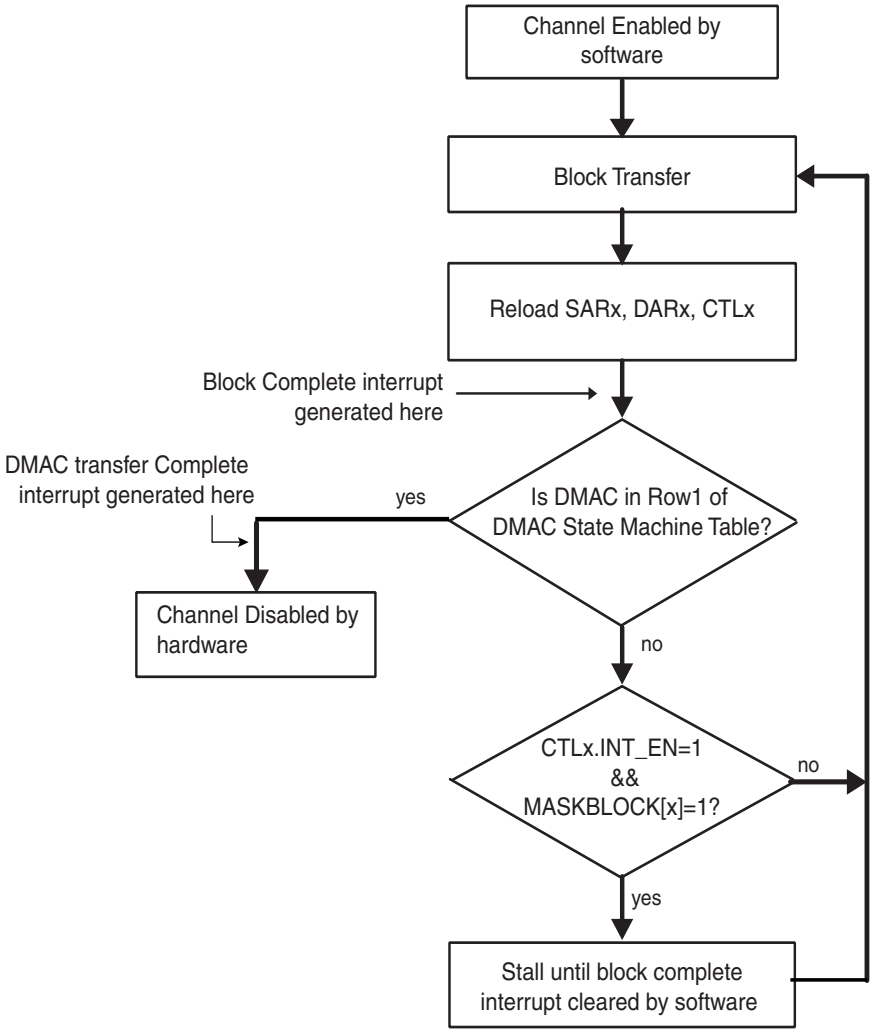


Figure 17-12. DMA Transfer Flow for Source and Destination Address Auto-reloaded



17.10.1.4 Multi-block Transfer with Source Address Auto-reloaded and Linked List Destination Address (Row7)

1. Read the Channel Enable register to choose a free (disabled) channel.
2. Set up the chain of linked list items (otherwise known as block descriptors) in memory. Write the control information in the LLI.CTLx register location of the block descriptor for each LLI in memory for channel x. For example, in the register you can program the following:
   a. Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control peripheral by programming the TT_FC of the CTLx register.
   b. Set up the transfer characteristics, such as:

– i. Transfer width for the source in the SRC_TR_WIDTH field.

– ii. Transfer width for the destination in the DST_TR_WIDTH field.

– iii. Source master layer in the SMS field where source resides.

– iv. Destination master layer in the DMS field where destination resides.

– v. Incrementing/decrementing or fixed address for source in SINC field.

– vi. Incrementing/decrementing or fixed address for destination DINC field.

3. Write the starting source address in the SARx register for channel x.

Note: The values in the LLI.SARx register locations of each of the Linked List Items (LLIs) setup up in memory, although fetched during a LLI fetch, are not used.

4. Write the channel configuration information into the CFGx register for channel x.
   a. Designate the handshaking interface type (hardware or software) for the source and destination peripherals. This is not required for memory. This step requires programming the HS_SEL_SRC/HS_SEL_DST bits, respectively. Writing a '0' activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a '1' activates the software handshaking interface source/destination requests.
   b. If the hardware handshaking interface is activated for the source or destination peripheral, assign handshaking interface to the source and destination peripheral. This requires programming the SRC_PER and DEST_PER bits, respectively.
5. Make sure that the LLI.CTLx register locations of all LLIs in memory (except the last) are set as shown in Row 7 of Table 17-1 on page 185 while the LLI.CTLx register of the last Linked List item must be set as described in Row 1 or Row 5 of Table 17-1 on page 185. Figure 17-7 on page 184 shows a Linked List example with two list items.
6. Make sure that the LLI.LLPx register locations of all LLIs in memory (except the last) are non-zero and point to the next Linked List Item.
7. Make sure that the LLI.DARx register location of all LLIs in memory point to the start destination block address proceeding that LLI fetch.
8. Make sure that the LLI.CTLx.DONE field of the LLI.CTLx register locations of all LLIs in memory is cleared.
9. Clear any pending interrupts on the channel from the previous DMA transfer by writing to the Interrupt Clear registers: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.
10. Program the CTLx, CFGx registers according to Row 7 as shown in Table 17-1 on page 185.
11. Program the LLPx register with LLPx(0), the pointer to the first Linked List item.
12. Finally, enable the channel by writing a '1' to the ChEnReg.CH_EN bit. The transfer is performed. Make sure that bit 0 of the DmaCfgReg register is enabled.
13. The DMACA fetches the first LLI from the location pointed to by LLPx(0).

Note: The LLI.SARx, LLI.DARx, LLI. LLPx and LLI.CTLx registers are fetched. The LLI.SARx register although fetched is not used.

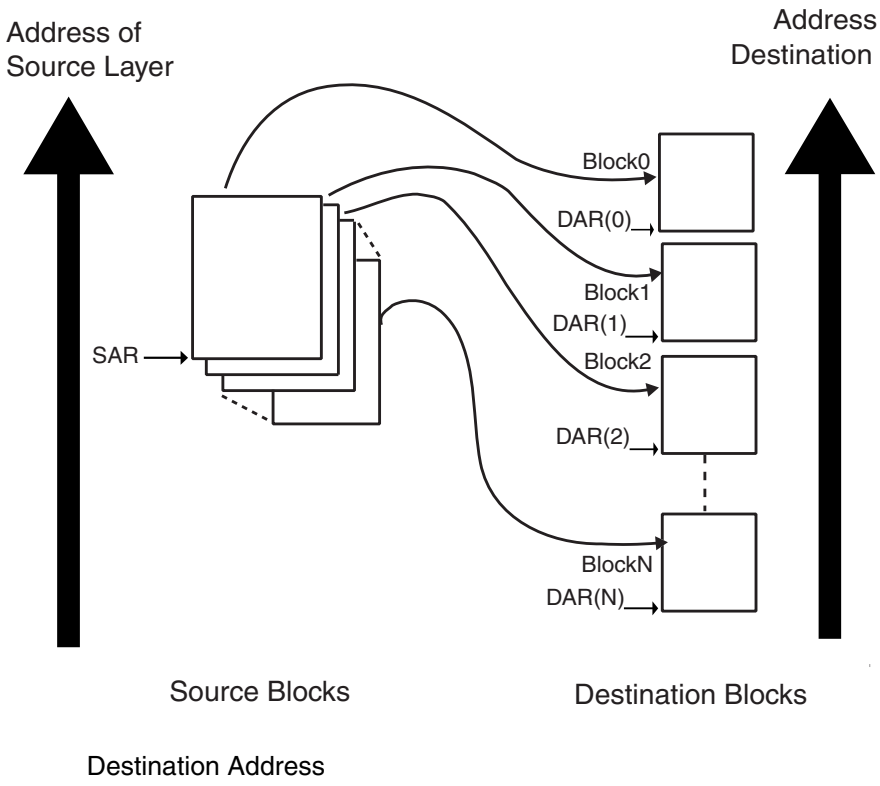
14. Source and destination request single and burst DMACA transactions to transfer the block of data (assuming non-memory peripherals). DMACA acknowledges at the completion of every transaction (burst and single) in the block and carry out the block transfer.
15. Table 17-1 on page 185The DMACA reloads the SARx register from the initial value. Hardware sets the block complete interrupt. The DMACA samples the row number as shown in Table 17-1 on page 185. If the DMACA is in Row 1 or 5, then the DMA transfer has completed. Hardware sets the transfer complete interrupt and disables the channel. You can either respond to the Block Complete or Transfer Complete interrupts, or poll for the Channel Enable (ChEnReg.CH_EN) bit until it is cleared by hardware, to detect when the transfer is complete. If the DMACA is not in Row 1 or 5 as shown in Table 17-1 on page 185 the following steps are performed.
16. The DMA transfer proceeds as follows:
   a. If interrupts are enabled (CTLx.INT_EN = 1) and the block complete interrupt is unmasked (MaskBlock[x] = 1'b1, where x is the channel number) hardware sets the block complete interrupt when the block transfer has completed. It then stalls until the

block complete interrupt is cleared by software. If the next block is to be the last block in the DMA transfer, then the block complete ISR (interrupt service routine) should clear the CFGx.RELOAD_SR source reload bit. This puts the DMACA into Row1 as shown in Table 17-1 on page 185. If the next block is not the last block in the DMA transfer, then the source reload bit should remain enabled to keep the DMACA in Row 7 as shown in Table 17-1 on page 185.

b. If interrupts are disabled (CTLx.INT_EN = 0) or the block complete interrupt is masked (MaskBlock[x] = 1'b0, where x is the channel number) then hardware does not stall until it detects a write to the block complete interrupt clear register but starts the next block transfer immediately. In this case, software must clear the source reload bit, CFGx.RELOAD_SR, to put the device into Row 1 of Table 17-1 on page 185 before the last block of the DMA transfer has completed.

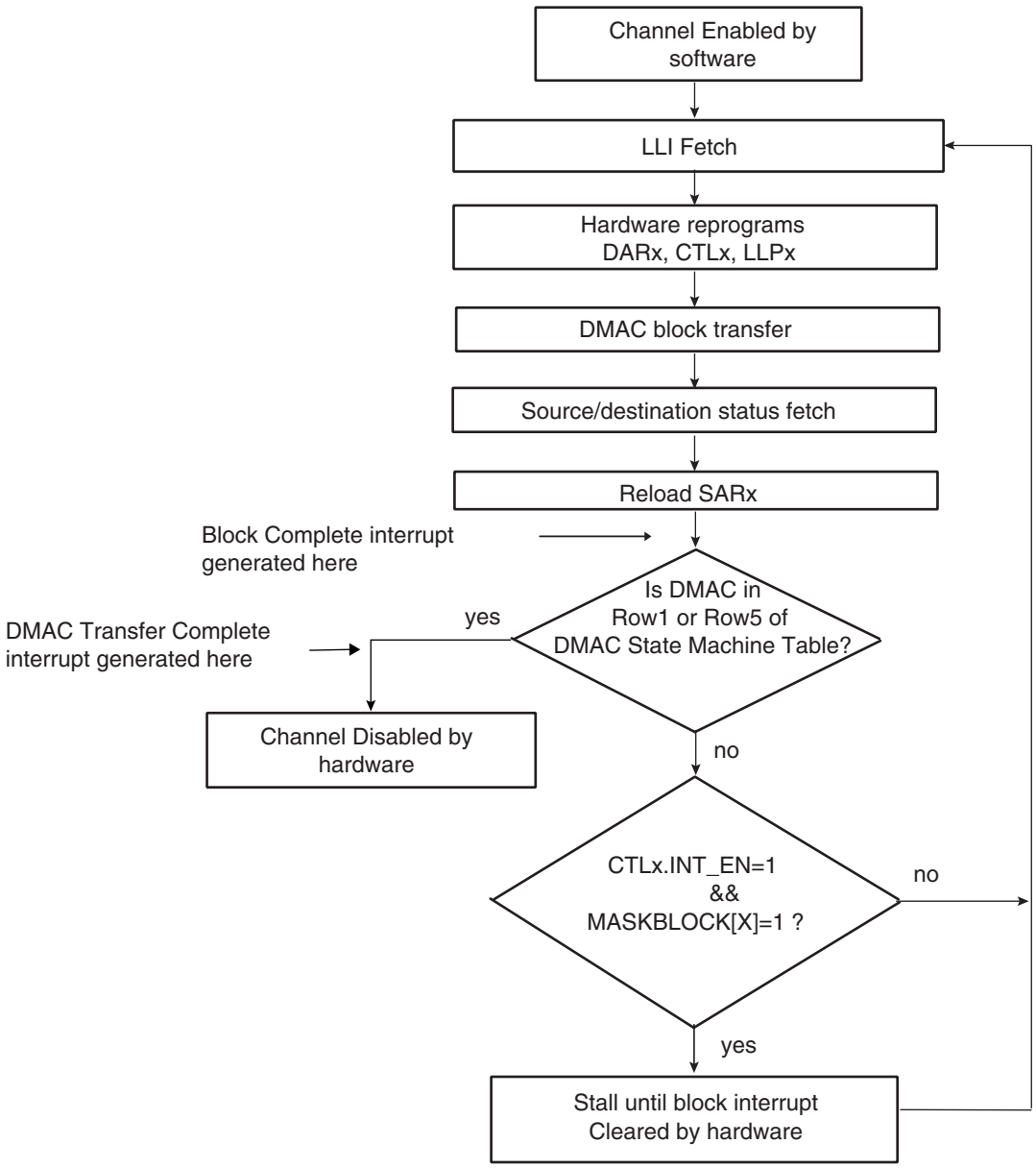
17. The DMACA fetches the next LLI from memory location pointed to by the current LLPx register, and automatically reprograms the DARx, CTLx and LLPx channel registers. Note that the SARx is not re-programmed as the reloaded value is used for the next DMA block transfer. If the next block is the last block of the DMA transfer then the CTLx and LLPx registers just fetched from the LLI should match Row 1 or Row 5 of Table 17-1 on page 185. The DMA transfer might look like that shown in Figure 17-13 on page 197.

Figure 17-13. Multi-Block DMA Transfer with Source Address Auto-reloaded and Linked List



The DMA Transfer flow is shown in Figure 17-14 on page 198.

Figure 17-14. DMA Transfer Flow for Source Address Auto-reloaded and Linked List Destination Address



17.10.1.5 Multi-block Transfer with Source Address Auto-reloaded and Contiguous Destination Address (Row 3)

1. Read the Channel Enable register to choose a free (disabled) channel.
2. Clear any pending interrupts on the channel from the previous DMA transfer by writing a '1' to the Interrupt Clear registers: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.
3. Program the following channel registers:
   a. Write the starting source address in the SARx register for channel x.
   b. Write the starting destination address in the DARx register for channel x.
   c. Program CTLx and CFGx according to Row 3 as shown in Table 17-1 on page 185. Program the LLPx register with '0'.
   d. Write the control information for the DMA transfer in the CTLx register for channel x. For example, in this register, you can program the following:
   – i. Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TT_FC of the CTLx register.
   – ii. Set up the transfer characteristics, such as:
      – Transfer width for the source in the SRC_TR_WIDTH field.
      – Transfer width for the destination in the DST_TR_WIDTH field.
      – Source master layer in the SMS field where source resides.
      – Destination master layer in the DMS field where destination resides.
      – Incrementing/decrementing or fixed address for source in SINC field.
      – Incrementing/decrementing or fixed address for destination in DINC field.
   e. Write the channel configuration information into the CFGx register for channel x.
   – i. Designate the handshaking interface type (hardware or software) for the source and destination peripherals. This is not required for memory. This step requires programming the HS_SEL_SRC/HS_SEL_DST bits, respectively. Writing a '0' activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a '1' activates the software handshaking interface to handle source/destination requests.
   – ii. If the hardware handshaking interface is activated for the source or destination peripheral, assign handshaking interface to the source and destination peripheral. This requires programming the SRC_PER and DEST_PER bits, respectively.
4. After the DMACA channel has been programmed, enable the channel by writing a '1' to the ChEnReg.CH_EN bit. Make sure that bit 0 of the DmaCfgReg register is enabled.
5. Source and destination request single and burst DMACA transactions to transfer the block of data (assuming non-memory peripherals). The DMACA acknowledges at the completion of every transaction (burst and single) in the block and carries out the block transfer.
6. When the block transfer has completed, the DMACA reloads the SARx register. The DARx register remains unchanged. Hardware sets the block complete interrupt. The DMACA then samples the row number as shown in Table 17-1 on page 185. If the DMACA is in Row 1, then the DMA transfer has completed. Hardware sets the transfer complete interrupt and disables the channel. So you can either respond to the Block Complete or Transfer Complete interrupts, or poll for the Channel Enable (ChEn-

Reg.CH_EN) bit until it is cleared by hardware, to detect when the transfer is complete. If the DMACA is not in Row 1, the next step is performed.

7. The DMA transfer proceeds as follows:
   a. If interrupts are enabled (CTLx.INT_EN = 1) and the block complete interrupt is unmasked (MaskBlock[x] = 1'b1, where x is the channel number) hardware sets the block complete interrupt when the block transfer has completed. It then stalls until the block complete interrupt is cleared by software. If the next block is to be the last block in the DMA transfer, then the block complete ISR (interrupt service routine) should clear the source reload bit, CFGx.RELOAD_SR. This puts the DMACA into Row1 as shown in Table 17-1 on page 185. If the next block is not the last block in the DMA transfer then the source reload bit should remain enabled to keep the DMACA in Row3 as shown in Table 17-1 on page 185.
   b. If interrupts are disabled (CTLx.INT_EN = 0) or the block complete interrupt is masked (MaskBlock[x] = 1'b0, where x is the channel number) then hardware does not stall until it detects a write to the block complete interrupt clear register but starts the next block transfer immediately. In this case software must clear the source reload bit, CFGx.RELOAD_SR, to put the device into ROW 1 of Table 17-1 on page 185 before the last block of the DMA transfer has completed.

The transfer is similar to that shown in Figure 17-15 on page 200.

The DMA Transfer flow is shown in Figure 17-16 on page 201.

Figure 17-15. Multi-block Transfer with Source Address Auto-reloaded and Contiguous Destination Address

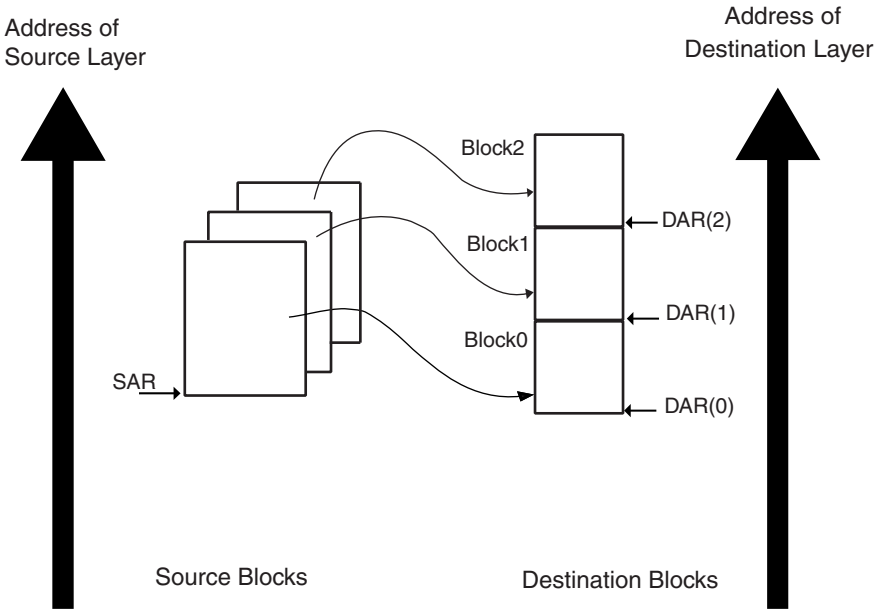
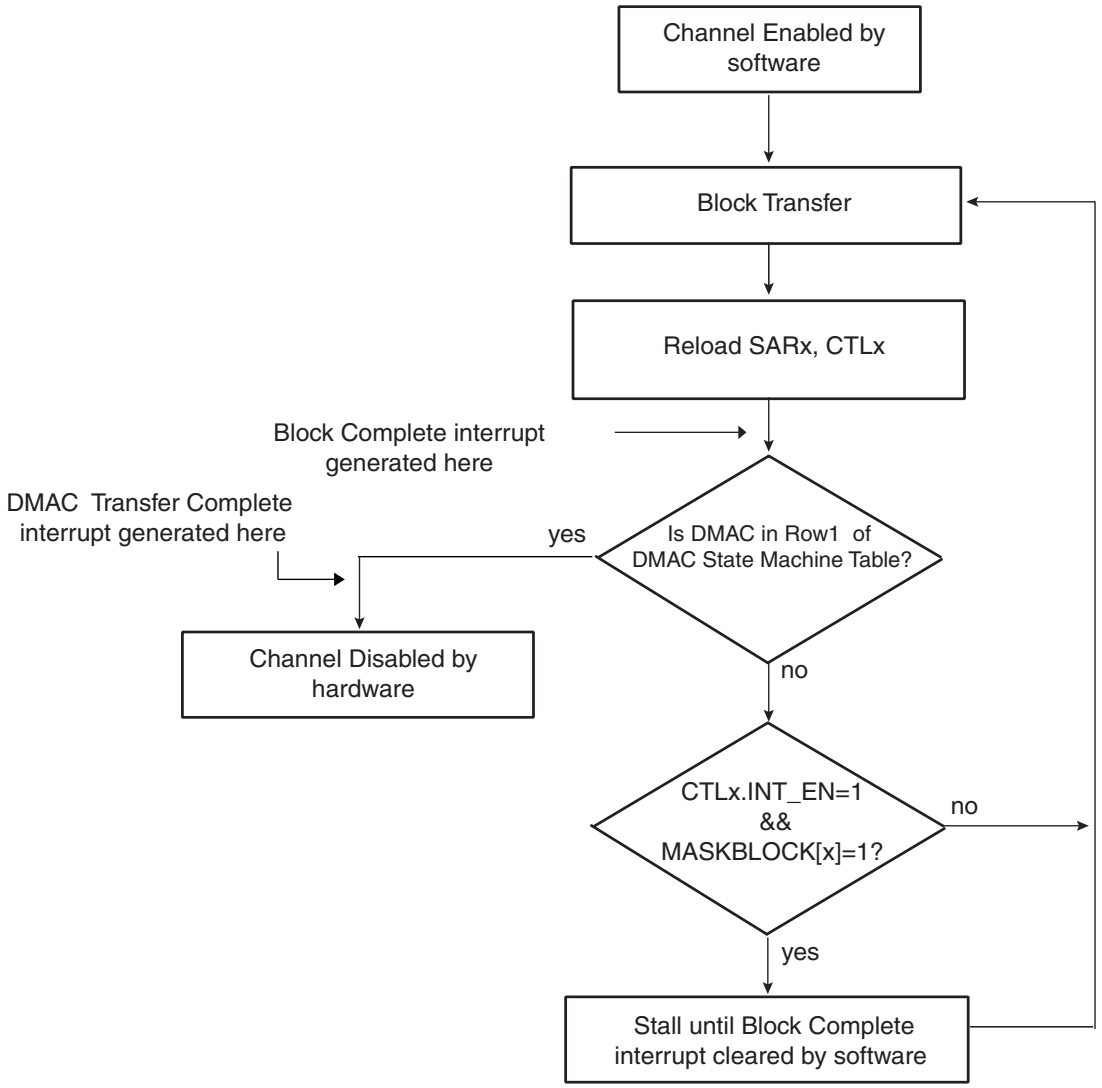


Figure 17-16. DMA Transfer for Source Address Auto-reloaded and Contiguous Destination Address



17.10.1.6 Multi-block DMA Transfer with Linked List for Source and Contiguous Destination Address (Row 8)

1. Read the Channel Enable register to choose a free (disabled) channel.
2. Set up the linked list in memory. Write the control information in the LLI. CTLx register location of the block descriptor for each LLI in memory for channel x. For example, in the register, you can program the following:
   a. Set up the transfer type (memory or non-memory peripheral for source and destination) and flow control device by programming the TT_FC of the CTLx register.
   b. Set up the transfer characteristics, such as:
   – i. Transfer width for the source in the SRC_TR_WIDTH field.
   – ii. Transfer width for the destination in the DST_TR_WIDTH field.
   – iii. Source master layer in the SMS field where source resides.
   – iv. Destination master layer in the DMS field where destination resides.
   – v. Incrementing/decrementing or fixed address for source in SINC field.

– vi. Incrementing/decrementing or fixed address for destination DINC field.

3. Write the starting destination address in the DARx register for channel x.

Note: The values in the LLI.DARx register location of each Linked List Item (LLI) in memory, although fetched during an LLI fetch, are not used.

4. Write the channel configuration information into the CFGx register for channel x.
   a. Designate the handshaking interface type (hardware or software) for the source and destination peripherals. This is not required for memory. This step requires programming the HS_SEL_SRC/HS_SEL_DST bits, respectively. Writing a '0' activates the hardware handshaking interface to handle source/destination requests for the specific channel. Writing a '1' activates the software handshaking interface to handle source/destination requests.
   b. If the hardware handshaking interface is activated for the source or destination peripheral, assign handshaking interface to the source and destination peripherals. This requires programming the SRC_PER and DEST_PER bits, respectively.
5. Make sure that all LLI.CTLx register locations of the LLI (except the last) are set as shown in Row 8 of Table 17-1 on page 185, while the LLI.CTLx register of the last Linked List item must be set as described in Row 1 or Row 5 of Table 17-1 on page 185. Figure 17-7 on page 184 shows a Linked List example with two list items.
6. Make sure that the LLI.LLPx register locations of all LLIs in memory (except the last) are non-zero and point to the next Linked List Item.
7. Make sure that the LLI.SARx register location of all LLIs in memory point to the start source block address proceeding that LLI fetch.
8. Make sure that the LLI.CTLx.DONE field of the LLI.CTLx register locations of all LLIs in memory is cleared.
9. Clear any pending interrupts on the channel from the previous DMA transfer by writing a '1' to the Interrupt Clear registers: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr. Reading the Interrupt Raw Status and Interrupt Status registers confirms that all interrupts have been cleared.
10. Program the CTLx, CFGx registers according to Row 8 as shown in Table 17-1 on page 185
11. Program the LLPx register with LLPx(0), the pointer to the first Linked List item.
12. Finally, enable the channel by writing a '1' to the ChEnReg.CH_EN bit. The transfer is performed. Make sure that bit 0 of the DmaCfgReg register is enabled.
13. The DMACA fetches the first LLI from the location pointed to by LLPx(0).

Note: The LLI.SARx, LLI.DARx, LLI.LLPx and LLI.CTLx registers are fetched. The LLI.DARx register location of the LLI although fetched is not used. The DARx register in the DMACA remains unchanged.

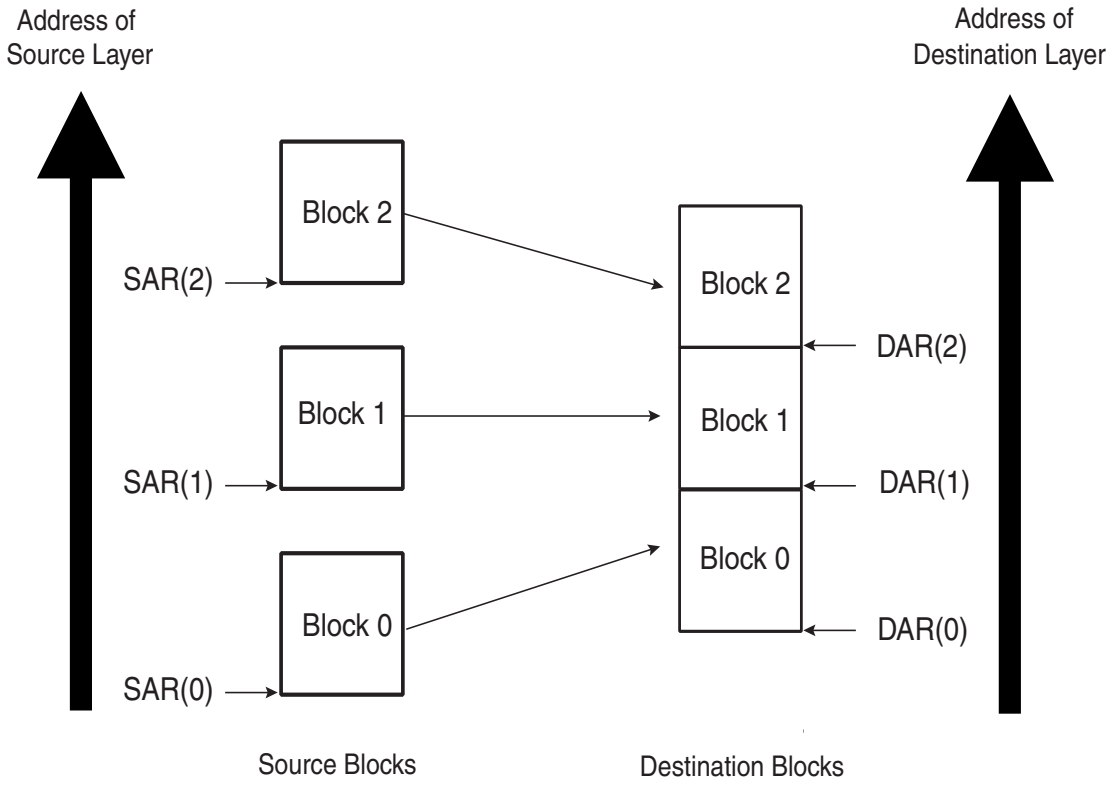
14. Source and destination requests single and burst DMACA transactions to transfer the block of data (assuming non-memory peripherals). The DMACA acknowledges at the completion of every transaction (burst and single) in the block and carry out the block transfer.

Note:

15. The DMACA does not wait for the block interrupt to be cleared, but continues and fetches the next LLI from the memory location pointed to by current LLPx register and automatically reprograms the SARx, CTLx and LLPx channel registers. The DARx register is left unchanged. The DMA transfer continues until the DMACA samples the CTLx and LLPx registers at the end of a block transfer match that described in Row 1 or Row 5 of Table 17-1 on page 185. The DMACA then knows that the previous block transferred was the last block in the DMA transfer.

The DMACA transfer might look like that shown in Figure 17-17 on page 203 Note that the destination address is decrementing.

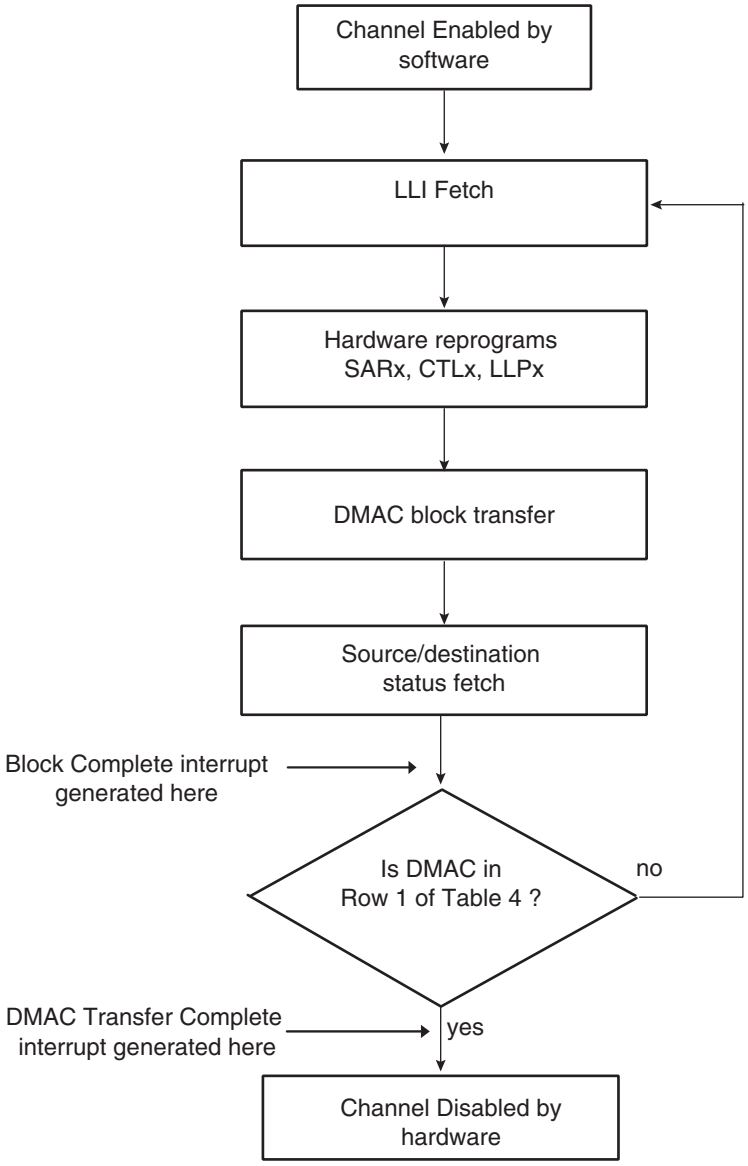
Figure 17-17. DMA Transfer with Linked List Source Address and Contiguous Destination Address



The DMA transfer flow is shown in Figure 17-19 on page 204.

Figure 17-18.

Figure 17-19. DMA Transfer Flow for Source Address Auto-reloaded and Contiguous Destination Address



17.11 Disabling a Channel Prior to Transfer Completion

Under normal operation, software enables a channel by writing a '1' to the Channel Enable Register, ChEnReg.CH_EN, and hardware disables a channel on transfer completion by clearing the ChEnReg.CH_EN register bit.

The recommended way for software to disable a channel without losing data is to use the CH_SUSP bit in conjunction with the FIFO_EMPTY bit in the Channel Configuration Register (CFGx) register.

1. If software wishes to disable a channel prior to the DMA transfer completion, then it can set the CFGx.CH_SUSP bit to tell the DMACA to halt all transfers from the source peripheral. Therefore, the channel FIFO receives no new data.
2. Software can now poll the CFGx.FIFO_EMPTY bit until it indicates that the channel FIFO is empty.
3. The ChEnReg.CH_EN bit can then be cleared by software once the channel FIFO is empty.

When CTLx.SRC_TR_WIDTH is less than CTLx.DST_TR_WIDTH and the CFGx.CH_SUSP bit is high, the CFGx.FIFO_EMPTY is asserted once the contents of the FIFO do not permit a single word of CTLx.DST_TR_WIDTH to be formed. However, there may still be data in the channel FIFO but not enough to form a single transfer of CTLx.DST_TR_WIDTH width. In this configuration, once the channel is disabled, the remaining data in the channel FIFO are not transferred to the destination peripheral. It is permitted to remove the channel from the suspension state by writing a '0' to the CFGx.CH_SUSP register. The DMA transfer completes in the normal manner.

Note: If a channel is disabled by software, an active single or burst transaction is not guaranteed to receive an acknowledgement.

17.11.1 Abnormal Transfer Termination

A DMACA DMA transfer may be terminated abruptly by software by clearing the channel enable bit, ChEnReg.CH_EN. This does not mean that the channel is disabled immediately after the ChEnReg.CH_EN bit is cleared over the HSB slave interface. Consider this as a request to disable the channel. The ChEnReg.CH_EN must be polled and then it must be confirmed that the channel is disabled by reading back 0. A case where the channel is not be disabled after a channel disable request is where either the source or destination has received a split or retry response. The DMACA must keep re-attempting the transfer to the system HADDR that originally received the split or retry response until an OKAY response is returned. To do otherwise is an System Bus protocol violation.

Software may terminate all channels abruptly by clearing the global enable bit in the DMACA Configuration Register (DmaCfgReg[0]). Again, this does not mean that all channels are disabled immediately after the DmaCfgReg[0] is cleared over the HSB slave interface. Consider this as a request to disable all channels. The ChEnReg must be polled and then it must be confirmed that all channels are disabled by reading back '0'.

Note: If the channel enable bit is cleared while there is data in the channel FIFO, this data is not sent to the destination peripheral and is not present when the channel is re-enabled. For read sensitive source peripherals such as a source FIFO this data is therefore lost. When the source is not a read sensitive device (i.e., memory), disabling a channel without waiting for the channel FIFO to empty may be acceptable as the data is available from the source peripheral upon request and is not lost.

Note: If a channel is disabled by software, an active single or burst transaction is not guaranteed to receive an acknowledgement.

17.12 User Interface

Table 17-2. DMA Controller Memory Map

Offset	Register	Register Name	Access	Reset Value
0x000	Channel 0 Source Address Register	SAR0	Read/Write	0x00000000
0x008	Channel 0 Destination Address Register	DAR0	Read/Write	0x00000000
0x010	Channel 0 Linked List Pointer Register	LLP0	Read/Write	0x00000000
0x018	Channel 0 Control Register Low	CTL0L	Read/Write	0x00304801
0x01C	Channel 0 Control Register High	CTL0H	Read/Write	0x00000002
0x040	Channel 0 Configuration Register Low	CFG0L	Read/Write	0x00000c00
0x044	Channel 0 Configuration Register High	CFG0H	Read/Write	0x00000004
0x048	Channel 0 Source Gather Register	SGR0	Read/Write	0x00000000
0x050	Channel 0 Destination Scatter Register	DSR0	Read/Write	0x00000000
0x058	Channel 1 Source Address Register	SAR1	Read/Write	0x00000000
0x060	Channel 1 Destination Address Register	DAR1	Read/Write	0x00000000
0x068	Channel 1 Linked List Pointer Register	LLP1	Read/Write	0x00000000
0x070	Channel 1 Control Register Low	CTL1L	Read/Write	0x00304801
0x074	Channel 1 Control Register High	CTL1H	Read/Write	0x00000002
0x098	Channel 1 Configuration Register Low	CFG1L	Read/Write	0x00000c20
0x09C	Channel 1 Configuration Register High	CFG1H	Read/Write	0x00000004
0x0A0	Channel 1Source Gather Register	SGR1	Read/Write	0x00000000
0x0A8	Channel 1 Destination Scatter Register	DSR1	Read/Write	0x00000000
0x0B0	Channel 2 Source Address Register	SAR2	Read/Write	0x00000000
0x0B8	Channel 2 Destination Address Register	DAR2	Read/Write	0x00000000
0x0C0	Channel 2 Linked List Pointer Register	LLP2	Read/Write	0x00000000
0x0C8	Channel 2 Control Register Low	CTL2L	Read/Write	0x00304801
0x0CC	Channel 2 Control Register High	CTL2H	Read/Write	0x00000002
0x0F0	Channel 2 Configuration Register Low	CFG2L	Read/Write	0x00000c40
0x0F4	Channel 2 Configuration Register High	CFG2H	Read/Write	0x00000004
0x0F8	Channel 2 Source Gather Register	SGR2	Read/Write	0x00000000
0x100	Channel 2 Destination Scatter Register	DSR2	Read/Write	0x00000000
0x2C0	Raw Status for IntTfr Interrupt	RawTfr	Read-only	0x00000000
0x2C8	Raw Status for IntBlock Interrupt	RawBlock	Read-only	0x00000000
0x2D0	Raw Status for IntSrcTran Interrupt	RawSrcTran	Read-only	0x00000000
0x2D8	Raw Status for IntDstTran Interrupt	RawDstTran	Read-only	0x00000000
0x2E0	Raw Status for IntErr Interrupt	RawErr	Read-only	0x00000000
0x2E8	Status for IntTfr Interrupt	StatusTfr	Read-only	0x00000000
0x2F0	Status for IntBlock Interrupt	StatusBlock	Read-only	0x00000000
0x2F8	Status for IntSrcTran Interrupt	StatusSrcTran	Read-only	0x00000000

Table 17-2. DMA Controller Memory Map (Continued)

Offset	Register	Register Name	Access	Reset Value
0x300	Status for IntDstTran Interrupt	StatusDstTran	Read-only	0x00000000
0x308	Status for IntErr Interrupt	StatusErr	Read-only	0x00000000
0x310	Mask for IntTfr Interrupt	MaskTfr	Read/Write	0x00000000
0x318	Mask for IntBlock Interrupt	MaskBlock	Read/Write	0x00000000
0x320	Mask for IntSrcTran Interrupt	MaskSrcTran	Read/Write	0x00000000
0x328	Mask for IntDstTran Interrupt	MaskDstTran	Read/Write	0x00000000
0x330	Mask for IntErr Interrupt	MaskErr	Read/Write	0x00000000
0x338	Clear for IntTfr Interrupt	ClearTfr	Write-only	0x00000000
0x340	Clear for IntBlock Interrupt	ClearBlock	Write-only	0x00000000
0x348	Clear for IntSrcTran Interrupt	ClearSrcTran	Write-only	0x00000000
0x350	Clear for IntDstTran Interrupt	ClearDstTran	Write-only	0x00000000
0x358	Clear for IntErr Interrupt	ClearErr	Write-only	0x00000000
0x360	Status for each interrupt type	StatusInt	Read-only	0x00000000
0x368	Source Software Transaction Request Register	ReqSrcReg	Read/Write	0x00000000
0x370	Destination Software Transaction Request Register	ReqDstReg	Read/Write	0x00000000
0x378	Single Source Transaction Request Register	SglReqSrcReg	Read/Write	0x00000000
0x380	Single Destination Transaction Request Register	SglReqDstReg	Read/Write	0x00000000
0x388	Last Source Transaction Request Register	LstSrcReg	Read/Write	0x00000000
0x390	Last Destination Transaction Request Register	LstDstReg	Read/Write	0x00000000
0x398	DMA Configuration Register	DmaCfgReg	Read/Write	0x00000000
0x3A0	DMA Channel Enable Register	ChEnReg	Read/Write	0x00000000
0x3F8	DMA Component ID Register Low	DmaCompIdRegL	Read-only	0x44571110
0x3FC	DMA Component ID Register High	DmaCompIdRegH	Read-only	0x3230362A

17.12.1 Channel x Source Address Register

Name: SARx

Access Type: Read/Write

Offset: 0x000 + [x * 0x58]

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
SADD[31:24]							

23	22	21	20	19	18	17	16
SADD[23:16]							

15	14	13	12	11	10	9	8
SADD[15:8]							

7	6	5	4	3	2	1	0
SADD[7:0]							

- **SADD: Source Address of DMA transfer**

The starting System Bus source address is programmed by software before the DMA channel is enabled or by a LLI update before the start of the DMA transfer. As the DMA transfer is in progress, this register is updated to reflect the source address of the current System Bus transfer.

Updated after each source System Bus transfer. The SINC field in the CTLx register determines whether the address increments, decrements, or is left unchanged on every source System Bus transfer throughout the block transfer.

17.12.2 Channel x Destination Address Register

Name: DARx

Access Type: Read/Write

Offset: 0x008 + [x * 0x58]

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DADD[31:24]							

23	22	21	20	19	18	17	16
DADD[23:16]							

15	14	13	12	11	10	9	8
DADD[15:8]							

7	6	5	4	3	2	1	0
DADD[7:0]							

- **DADD: Destination Address of DMA transfer**

The starting System Bus destination address is programmed by software before the DMA channel is enabled or by a LLI update before the start of the DMA transfer. As the DMA transfer is in progress, this register is updated to reflect the destination address of the current System Bus transfer.

Updated after each destination System Bus transfer. The DINC field in the CTLx register determines whether the address increments, decrements or is left unchanged on every destination System Bus transfer throughout the block transfer.

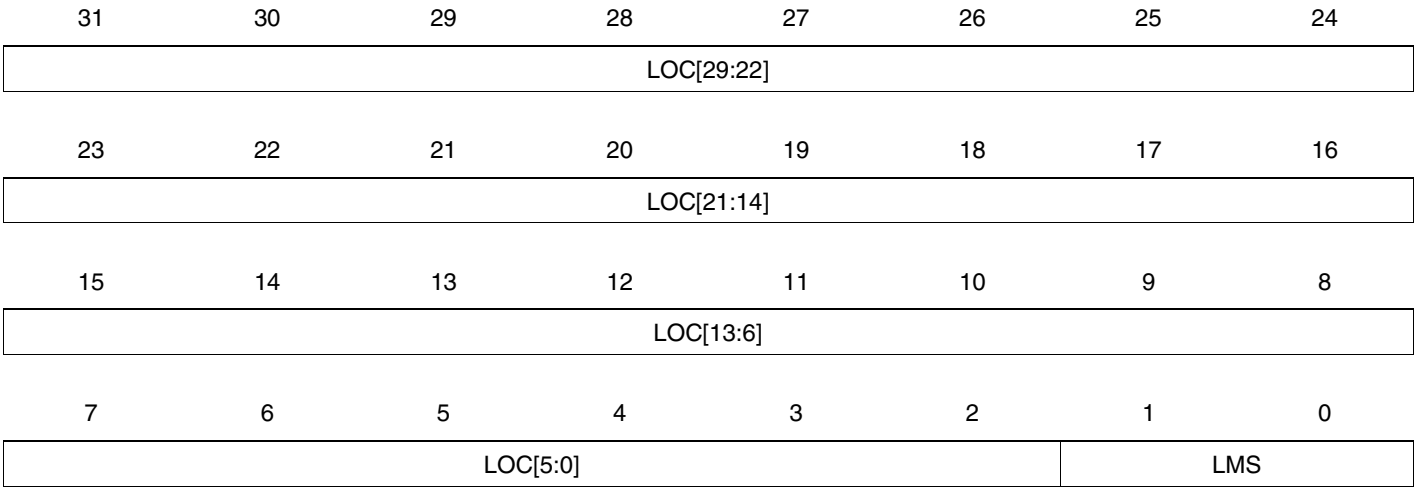
17.12.3 Linked List Pointer Register for Channel x

Name: LLPx

Access Type: Read/Write

Offset: 0x010 + [x * 0x58]

Reset Value: 0x00000000



- **LOC: Address of the next LLI**

Starting address in memory of next LLI if block chaining is enabled.

The user need to program this register to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

The LLP register has two functions:

The logical result of the equation LLP.LOC != 0 is used to set up the type of DMA transfer (single or multi-block).

If LLP.LOC is set to 0x0, then transfers using linked lists are NOT enabled. This register must be programmed prior to enabling the channel in order to set up the transfer type.

It (LLP.LOC != 0) contains the pointer to the next Linked Listed Item for block chaining using linked lists.

The LLPx register is also used to point to the address where write back of the control and source/destination status information occurs after block completion.

- **LMS: List Master Select**

Identifies the High speed bus interface for the device that stores the next linked list item:

Table 17-3. List Master Select

LMS	HSB Master
0	HSB master 1
1	HSB master 2
Other	Reserved

17.12.4 Control Register for Channel x Low

Name: CTLxL

Access Type: Read/Write

Offset: 0x018 + [x * 0x58]

Reset Value: 0x00304801

31	30	29	28	27	26	25	24
			LLP_SRC_EN	LLP_DST_EN	SMS		DMS[1]

23	22	21	20	19	18	17	16
DMS[0]	TT_FC				DST_GATHER_EN	SRC_GATHER_EN	SRC_MSIZE[2]

15	14	13	12	11	10	9	8
SRC_MSIZE[1:0]		DEST_MSIZE			SINC		DINC[1]

7	6	5	4	3	2	1	0
DINC[0]	SRC_TR_WIDTH			DST_TR_WIDTH			INT_EN

This register contains fields that control the DMA transfer. The CTLxL register is part of the block descriptor (linked list item) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

- **LLP_SRC_EN**

Block chaining is only enabled on the source side if the *LLP_SRC_EN* field is high and LLPx.LOC is non-zero.

- **LLP_DST_EN**

Block chaining is only enabled on the destination side if the *LLP_DST_EN* field is high and LLPx.LOC is non-zero.

- **SMS: Source Master Select**

Identifies the Master Interface layer where the source device (peripheral or memory) is accessed from

Table 17-4. Source Master Select

SMS	HSB Master
0	HSB master 1
1	HSB master 2
Other	Reserved

- **DMS: Destination Master Select**

Identifies the Master Interface layer where the destination device (peripheral or memory) resides

Table 17-5. Destination Master Select

DMS	HSB Master
0	HSB master 1
1	HSB master 2
Other	Reserved

- **TT_FC: Transfer Type and Flow Control**

The four following transfer types are supported:

• Memory to Memory, Memory to Peripheral, Peripheral to Memory and Peripheral to Peripheral.

The DMACA is always the Flow Controller.

TT_FC	Transfer Type	Flow Controller
000	Memory to Memory	DMACA
001	Memory to Peripheral	DMACA
010	Peripheral to Memory	DMACA
011	Peripheral to Peripheral	DMACA
Other	Reserved	Reserved

- **DST_SCATTER_EN: Destination Scatter Enable**

  0 = Scatter disabled

  1 = Scatter enabled

Scatter on the destination side is applicable only when the CTL*x*.DINC bit indicates an incrementing or decrementing address control.

Important note: This bit is only implemented for channel 1, not for channels 0 and 2.

- **SRC_GATHER_EN: Source Gather Enable**

  0 = Gather disabled

  1 = Gather enabled

Gather on the source side is applicable only when the CTL*x*.SINC bit indicates an incrementing or decrementing address control.

Important note: This bit is only implemented for channel 1, not for channels 0 and 2.

- **SRC_MSIZE: Source Burst Transaction Length**

Number of data items, each of width *CTLx.SRC_TR_WIDTH*, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface.

SRC_MSIZE	Size (items number)
0	1
1	4
2	8
Other	Reserved

- **DST_MSIZE: Destination Burst Transaction Length**

Number of data items, each of width *CTLx.DST_TR_WIDTH*, to be written to the destination every time a destination burst transaction request is made from either the corresponding hardware or software handshaking interface.

DST_MSIZE	Size (items number)
0	1
1	4
2	8
Other	Reserved

- **SINC: Source Address Increment**

Indicates whether to increment or decrement the source address on every source System Bus transfer. If your device is fetching data from a source peripheral FIFO with a fixed address, then set this field to “No change”

SINC	Source Address Increment
0	Increment
1	Decrement
Other	No change

- **DINC: Destination Address Increment**

Indicates whether to increment or decrement the destination address on every destination System Bus transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to “No change”

DINC	Destination Address Increment
0	Increment
1	Decrement
Other	No change

- **SRT_TR_WIDTH: Source Transfer Width**
- **DSC_TR_WIDTH: Destination Transfer Width**

SRC_TR_WIDTH/DST_TR_WIDTH	Size (bits)
0	8
1	16
2	32
Other	Reserved

- **INT_EN: Interrupt Enable Bit**

If set, then all five interrupt generating sources are enabled.

17.12.5 Control Register for Channel x High

Name: CTLxH

Access Type: Read/Write

Offset: 0x01C + [x * 0x58]

Reset Value: 0x00000002

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	DONE	BLOCK_TS[11:8]			

7	6	5	4	3	2	1	0
BLOCK_TS[7:0]							

- **DONE: Done Bit**

Software can poll this bit to see when a block transfer is complete

- **BLOCK_TS: Block Transfer Size**

When the DMACA is flow controller, this field is written by the user before the channel is enabled to indicate the block size.

The number programmed into BLOCK_TS indicates the total number of single transactions to perform for every block transfer, unless the transfer is already in progress, in which case the value of BLOCK_TS indicates the number of single transactions that have been performed so far.

The width of the single transaction is determined by CTLx.SRC_TR_WIDTH.

17.12.6 Configuration Register for Channel x Low

Name: CFGxL

Access Type: Read/Write

Offset: 0x040 + [x * 0x58]

- **Reset Value: 0x00000C00 + [x * 0x20]**

31	30	29	28	27	26	25	24
RELOAD_DST	RELOAD_SRC	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	SRC_HS_POL	DST_HS_POL	-	-
15	14	13	12	11	10	9	8
-		-		HS_SEL_SRC	HS_SEL_DST	FIFO_EMPTY	CH_SUSP
7	6	5	4	3	2	1	0
CH_PRIOR			-	-	-	-	-

- **RELOAD_DST: Automatic Destination Reload**

The DARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.

- **RELOAD_SRC: Automatic Source Reload**

The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.

- **SRC_HS_POL: Source Handshaking Interface Polarity**
  0 = Active high
  1 = Active low
- **DST_HS_POL: Destination Handshaking Interface Polarity**
  0 = Active high
  1 = Active low
- **HS_SEL_SRC: Source Software or Hardware Handshaking Select**

This register selects which of the handshaking interfaces, hardware or software, is active for source requests on this channel.

0 = Hardware handshaking interface. Software-initiated transaction requests are ignored.
1 = Software handshaking interface. Hardware-initiated transaction requests are ignored.

If the source peripheral is memory, then this bit is ignored.

- **HS_SEL_DST: Destination Software or Hardware Handshaking Select**

This register selects which of the handshaking interfaces, hardware or software, is active for destination requests on this channel.

0 = Hardware handshaking interface. Software-initiated transaction requests are ignored.

1 = Software handshaking interface. Hardware Initiated transaction requests are ignored.

If the destination peripheral is memory, then this bit is ignored.

- **FIFO_EMPTY**

Indicates if there is data left in the channel's FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel.

1 = Channel's FIFO empty

0 = Channel's FIFO not empty

- **CH_SUSP: Channel Suspend**

Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data.

0 = Not Suspended.

1 = Suspend. Suspend DMA transfer from the source.

- **CH_PRIOR: Channel priority**

A priority of 7 is the highest priority, and 0 is the lowest. This field must be programmed within the following range [0, x-1].

A programmed value outside this range causes erroneous behavior.

17.12.7 Configuration Register for Channel x High

Name: CFGxH

Access Type: Read/Write

Offset: 0x044 + [x * 0x58]

Reset Value: 0x00000004

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	DEST_PER				SRC_PER[3:1]		

7	6	5	4	3	2	1	0
SRC_PER[0]	-	-	PROTCTL			FIFO_MODE	FCMODE

- **DEST_PER: Destination Hardware Handshaking Interface**

Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the destination of channel *x* if the CFGx.HS_SEL_DST field is 0. Otherwise, this field is ignored. The channel can then communicate with the destination peripheral connected to that interface via the assigned hardware handshaking interface.

For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

- **SRC_PER: Source Hardware Handshaking Interface**

Assigns a hardware handshaking interface (0 - DMAH_NUM_HS_INT-1) to the source of channel *x* if the CFGx.HS_SEL_SRC field is 0. Otherwise, this field is ignored. The channel can then communicate with the source peripheral connected to that interface via the assigned hardware handshaking interface.

For correct DMACA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

- **PROTCTL: Protection Control**

Bits used to drive the System Bus HPROT[3:1] bus. The *System Bus Specification* recommends that the default value of HPROT indicates a non-cached, nonbuffered, privileged data access. The reset value is used to indicate such an access.

HPROT[0] is tied high as all transfers are data accesses as there are no opcode fetches. There is a one-to-one mapping of these register bits to the HPROT[3:1] master interface signals.

- **FIFO_MODE: R/W 0x0 FIFO Mode Select**

Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced.

0 = Space/data available for single System Bus transfer of the specified transfer width.

1 = Space/data available is greater than or equal to half the FIFO depth for destination transfers and less than half the FIFO depth for source transfers. The exceptions are at the end of a burst transaction request or at the end of a block transfer.

- **FCMODE: Flow Control Mode**

Determines when source transaction requests are serviced when the Destination Peripheral is the flow controller.

0 = Source transaction requests are serviced when they occur. Data pre-fetching is enabled.

1 = Source transaction requests are not serviced until a destination transaction request occurs. In this mode the amount of data transferred from the source is limited such that it is guaranteed to be transferred to the destination prior to block termination by the destination. Data pre-fetching is disabled.

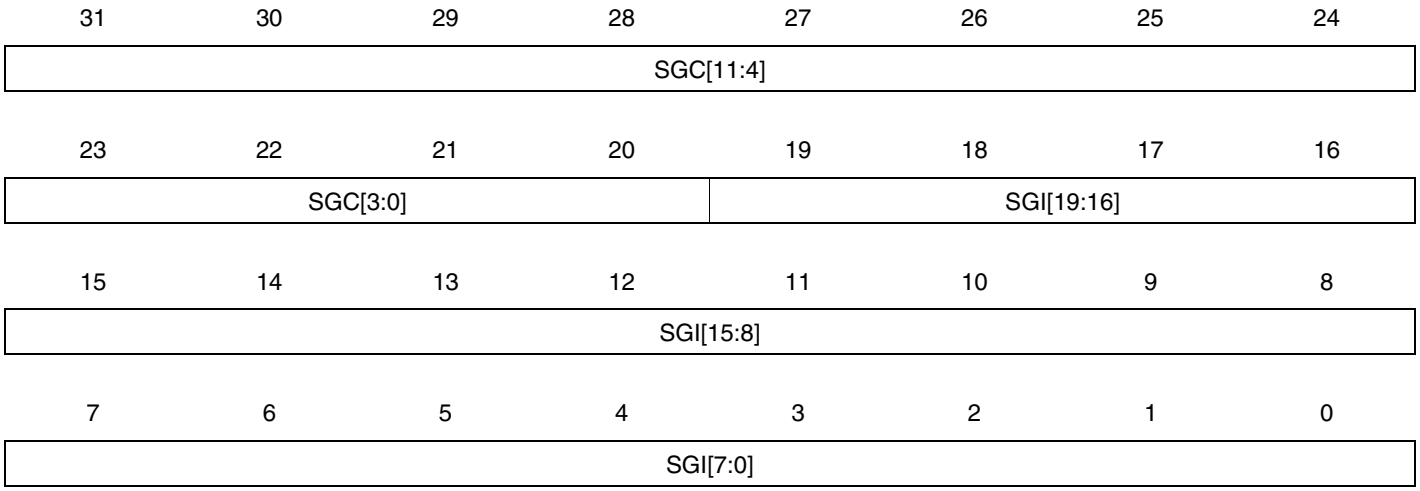
17.12.8 Source Gather Register for Channel x

Name: SGRx

Access Type: Read/Write

Offset: 0x048 + [x * 0x58]

Reset Value: 0x00000000



- **SGC: Source Gather Count**

Specifies the number of contiguous source transfers of CTL*x*.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary.

- **SGI: Source Gather Interval**

Specifies the source address increment/decrement in multiples of CTL*x*.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer.

Important note: This register is only implemented for channel 1, not for channels 0 and 2.

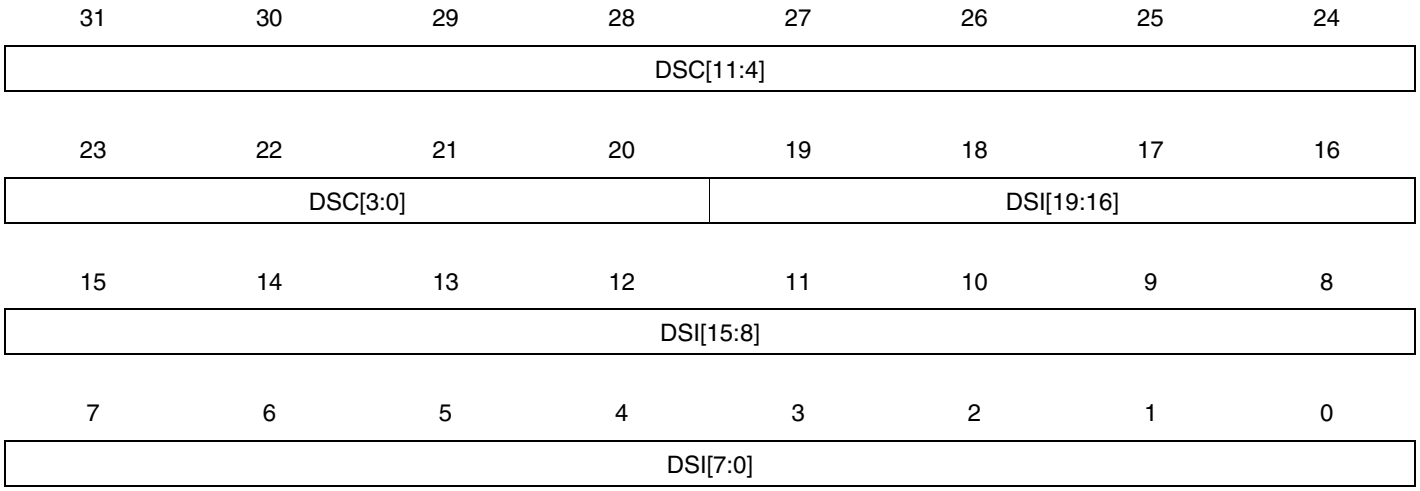
17.12.9 Destination Scatter Register for Channel x

Name: DSRx

Access Type: Read/Write

Offset: 0x050 + [x * 0x58]

Reset Value: 0x00000000



- **DSC: Destination Scatter Count**

Specifies the number of contiguous destination transfers of CTL*x*.DST_TR_WIDTH between successive scatter boundaries.

- **DSI: Destination Scatter Interval**

Specifies the destination address increment/decrement in multiples of CTL*x*.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer.

Important note: This register is only implemented for channel 1, not for channels 0 and 2.

17.12.10 Interrupt Registers

The following sections describe the registers pertaining to interrupts, their status, and how to clear them. For each channel, there are five types of interrupt sources:

- IntTfr: DMA Transfer Complete Interrupt

This interrupt is generated on DMA transfer completion to the destination peripheral.

- IntBlock: Block Transfer Complete Interrupt

This interrupt is generated on DMA block transfer completion to the destination peripheral.

- IntSrcTran: Source Transaction Complete Interrupt

This interrupt is generated after completion of the last System Bus transfer of the requested single/burst transaction from the handshaking interface on the source side.

If the source for a channel is memory, then that channel never generates a IntSrcTran interrupt and hence the corresponding bit in this field is not set.

- IntDstTran: Destination Transaction Complete Interrupt

This interrupt is generated after completion of the last System Bus transfer of the requested single/burst transaction from the handshaking interface on the destination side.

If the destination for a channel is memory, then that channel never generates the IntDstTran interrupt and hence the corresponding bit in this field is not set.

- IntErr: Error Interrupt

This interrupt is generated when an ERROR response is received from an HSB slave on the HRESP bus during a DMA transfer. In addition, the DMA transfer is cancelled and the channel is disabled.

17.12.11 Interrupt Raw Status Registers

Name: RawTfr, RawBlock, RawSrcTran, RawDstTran, RawErr

Access Type: Read-only

Offset: 0x2C0, 0x2C8, 0x2D0, 0x2D8, 0x2E0

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	RAW2	RAW1	RAW0

- **RAW[2:0]Raw interrupt for each channel**

Interrupt events are stored in these Raw Interrupt Status Registers before masking: RawTfr, RawBlock, RawSrcTran, RawDstTran, RawErr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr[2] is Channel 2's raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers.

17.12.12 Interrupt Status Registers

Name: StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr

Access Type: Read-only

Offset: 0x2E8, 0x2F0, 0x2F8, 0x300, 0x308

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	STATUS2	STATUS1	STATUS0

- **STATUS[2:0]**

All interrupt events from all channels are stored in these Interrupt Status Registers after masking: StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr[2] is Channel 2's status transfer complete interrupt.The contents of these registers are used to generate the interrupt signals leaving the DMACA.

17.12.13 Interrupt Mask Registers

Name: MaskTfr, MaskBlock, MaskSrcTran, MaskDstTran, MaskErr

Access Type: Read/Write

Offset: 0x310, 0x318, 0x320, 0x328, 0x330

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	INT_M_WE2	INT_M_WE1	INT_M_WE0

7	6	5	4	3	2	1	0
-	-	-	-	-	INT_MASK2	INT_MASK1	INT_MASK0

The contents of the Raw Status Registers are masked with the contents of the Mask Registers: MaskTfr, MaskBlock, MaskSrcTran, MaskDstTran, MaskErr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr[2] is the mask bit for Channel 2's transfer complete interrupt.

A channel's INT_MASK bit is only written if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same System Bus write transfer. This allows software to set a mask bit without performing a read-modified write operation.

For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr[0], while MaskTfr[7:1] remains unchanged. Writing hex 00*xx* leaves MaskTfr[7:0] unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMACA to set the appropriate bit in the Status Registers.

- **INT_M_WE[10:8]: Interrupt Mask Write Enable**
  0 = Write disabled
  1 = Write enabled
- **INT_MASK[2:0]: Interrupt Mask**
  0= Masked
  1 = Unmasked

17.12.14 Interrupt Clear Registers

Name: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr

Access Type: Write-only

Offset: 0x338, 0x340, 0x348, 0x350, 0x358

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	CLEAR2	CLEAR1	CLEAR0

- **CLEAR[2:0]: Interrupt Clear**
  0 = No effect
  1 = Clear interrupt

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr[2] is the clear bit for Channel 2's transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

17.12.15 Combined Interrupt Status Registers

Name: StatusInt

Access Type: Read-only

Offset: 0x360

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	ERR	DSTT	SRCT	BLOCK	TFR

The contents of each of the five Status Registers (StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran, StatusErr) is OR'ed to produce a single bit per interrupt type in the Combined Status Register (StatusInt).

- **ERR**

OR of the contents of StatusErr Register.

- **DSTT**

OR of the contents of StatusDstTran Register.

- **SRCT**

OR of the contents of StatusSrcTran Register.

- **BLOCK**

OR of the contents of StatusBlock Register.

- **TFR**

OR of the contents of StatusTfr Register.

17.12.16 Source Software Transaction Request Register

Name: ReqSrcReg

Access Type: Read/write

Offset: 0x368

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	REQ_WE2	REQ_WE1	REQ_WE0

7	6	5	4	3	2	1	0
-	-	-	-	-	SRC_REQ2	SRC_REQ1	SRC_REQ0

A bit is assigned for each channel in this register. ReqSrcReg[*n*] is ignored when software handshaking is not enabled for the source of channel *n*.

A channel SRC_REQ bit is written only if the corresponding channel write enable bit in the REQ_WE field is asserted on the same System Bus write transfer.

For example, writing 0x101 writes a 1 into ReqSrcReg[0], while ReqSrcReg[4:1] remains unchanged. Writing hex 0x0*yy* leaves ReqSrcReg[4:0] unchanged. This allows software to set a bit in the ReqSrcReg register without performing a read-modified write

- **REQ_WE[10:8]: Request write enable**
  0 = Write disabled
  1 = Write enabled
- **SRC_REQ[2:0]: Source request**

17.12.17 Destination Software Transaction Request Register

Name: ReqDstReg

Access Type: Read/write

Offset: 0x370

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	REQ_WE2	REQ_WE1	REQ_WE0
7	6	5	4	3	2	1	0
-	-	-	-	-	DST_REQ2	DST_REQ1	DST_REQ0

A bit is assigned for each channel in this register. ReqDstReg[*n*] is ignored when software handshaking is not enabled for the source of channel *n*.

A channel DST_REQ bit is written only if the corresponding channel write enable bit in the REQ_WE field is asserted on the same System Bus write transfer.

- **REQ_WE[10:8]: Request write enable**
  0 = Write disabled
  1 = Write enabled
- **DST_REQ[2:0]: Destination request**

17.12.18 Single Source Transaction Request Register

Name: SglReqSrcReg

Access Type: Read/write

Offset: 0x378

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	REQ_WE2	REQ_WE1	REQ_WE0
7	6	5	4	3	2	1	0
-	-	-	-	-	S_SG_REQ2	S_SG_REQ1	S_SG_REQ0

A bit is assigned for each channel in this register. SglReqSrcReg[*n*] is ignored when software handshaking is not enabled for the source of channel *n*.

A channel S_SG_REQ bit is written only if the corresponding channel write enable bit in the REQ_WE field is asserted on the same System Bus write transfer.

- **REQ_WE[10:8]: Request write enable**
  0 = Write disabled
  1 = Write enabled
- **S_SG_REQ[2:0]: Source single request**

17.12.19 Single Destination Transaction Request Register

Name: SglReqDstReg

Access Type: Read/write

Offset: 0x380

Reset Value: 0x0000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	REQ_WE2	REQ_WE1	REQ_WE0

7	6	5	4	3	2	1	0
-	-	-	-	-	D_SG_REQ2	D_SG_REQ1	D_SG_REQ0

A bit is assigned for each channel in this register. SglReqDstReg[*n*] is ignored when software handshaking is not enabled for the source of channel *n*.

A channel D_SG_REQ bit is written only if the corresponding channel write enable bit in the REQ_WE field is asserted on the same System Bus write transfer.

- **REQ_WE[10:8]: Request write enable**
  0 = Write disabled
  1 = Write enabled
- **D_SG_REQ[2:0]: Destination single request**

17.12.20 Last Source Transaction Request Register

Name: LstSrcReg

Access Type: Read/write

Offset: 0x388

Reset Value: 0x0000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	LSTSRC_WE2	LSTSRC_WE1	LSTSRC_WE0

7	6	5	4	3	2	1	0
-	-	-	-	-	LSTSRC2	LSTSRC1	LSTSRC0

A bit is assigned for each channel in this register. LstSrcReg[*n*] is ignored when software handshaking is not enabled for the source of channel *n*.

A channel LSTSRC bit is written only if the corresponding channel write enable bit in the LSTSRC_WE field is asserted on the same System Bus write transfer.

- **LSTSRC_WE[10:8]: Source Last Transaction request write enable**
  0 = Write disabled
  1 = Write enabled
- **LSTSRC[2:0]: Source Last Transaction request**

17.12.21 Last Destination Transaction Request Register

Name: LstDstReg

Access Type: Read/write

Offset: 0x390

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	LSTDST_WE 2	LSTDST_WE 1	LSTDST_WE 0

7	6	5	4	3	2	1	0
-	-	-	-	-	LSTDST2	LSTDST1	LSTDST0

A bit is assigned for each channel in this register. LstDstReg[*n*] is ignored when software handshaking is not enabled for the source of channel *n*.

A channel LSTDST bit is written only if the corresponding channel write enable bit in the LSTDST_WE field is asserted on the same System Bus write transfer.

- **LSTDST_WE[10:8]: Destination Last Transaction request write enable**
  0 = Write disabled
  1 = Write enabled
- **LSTDST[2:0]: Destination Last Transaction request**

17.12.22 DMA Configuration Register

Name: DmaCfgReg

Access Type: Read/Write

Offset: 0x398

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DMA_EN

- **DMA_EN: DMA Controller Enable**
  0 = DMACA Disabled
  1 = DMACA Enabled.

This register is used to enable the DMACA, which must be done before any channel activity can begin.

If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns ‘1’ to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns ‘0’.

17.12.23 DMA Channel Enable Register

Name: ChEnReg

Access Type: Read/Write

Offset: 0x3A0

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	CH_EN_WE2	CH_EN_WE1	CH_EN_WE0
7	6	5	4	3	2	1	0
-	-	-	-	-	CH_EN2	CH_EN1	CH_EN0

- **CH_EN_WE[10:8]: Channel Enable Write Enable**

The channel enable bit, CH_EN, is only written if the corresponding channel write enable bit, CH_EN_WE, is asserted on the same System Bus write transfer.

For example, writing 0x101 writes a 1 into ChEnReg[0], while ChEnReg[7:1] remains unchanged.

- **CH_EN[2:0]**

  0 = Disable the Channel

  1 = Enable the Channel

Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel.

The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last System Bus transfer of the DMA transfer to the destination has completed.Software can therefore poll this bit to determine when a DMA transfer has completed.

17.12.24 DMACA Component Id Register Low

Name: DmaCompIdRegL

Access Type: Read-only

Offset: 0x3F8

Reset Value: 0x44571110

31	30	29	28	27	26	25	24
DMA_COMP_TYPE[31:24]							

23	22	21	20	19	18	17	16
DMA_COMP_TYPE[23:16]							

15	14	13	12	11	10	9	8
DMA_COMP_TYPE[15:8]							

7	6	5	4	3	2	1	0
DMA_COMP_TYPE[7:0]							

- **DMA_COMP_TYPE**

DesignWare component type number = 0x44571110.

This assigned unique hex value is constant and is derived from the two ASCII letters “DW” followed by a 32-bit unsigned number

17.12.25 DMACA Component Id Register High

Name: DmaCompIdRegH

Access Type: Read-only

Offset: 0x3FC

Reset Value: 0x3230362A

31	30	29	28	27	26	25	24
DMA_COMP_VERSION[31:24]							
23	22	21	20	19	18	17	16
DMA_COMP_VERSION[23:16]							
15	14	13	12	11	10	9	8
DMA_COMP_VERSION[15:8]							
7	6	5	4	3	2	1	0
DMA_COMP_VERSION[7:0]							

- **DMA_COMP_VERSION: Version of the component**

18. Peripheral DMA Controller (PDC)

Rev: 1.0.0.1

18.1 Features

- **Generates Transfers to/from Peripherals such as USART, SSC and SPI**
- **Supports Up to 20 Channels (Product Dependent)**
- **One Master Clock Cycle Needed for a Transfer from Memory to Peripheral**
- **Two Master Clock Cycles Needed for a Transfer from Peripheral to Memory**

18.2 Description

The Peripheral DMA Controller (PDC) transfers data between on-chip serial peripherals such as the UART, USART, SSC, SPI, and the on- and off-chip memories. Using the Peripheral DMA Controller avoids processor intervention and removes the processor interrupt-handling overhead. This significantly reduces the number of clock cycles required for a data transfer and, as a result, improves the performance of the microcontroller and makes it more power efficient.

The PDC channels are implemented in pairs, each pair being dedicated to a particular peripheral. One channel in the pair is dedicated to the receiving channel and one to the transmitting channel of each UART, USART, SSC and SPI.

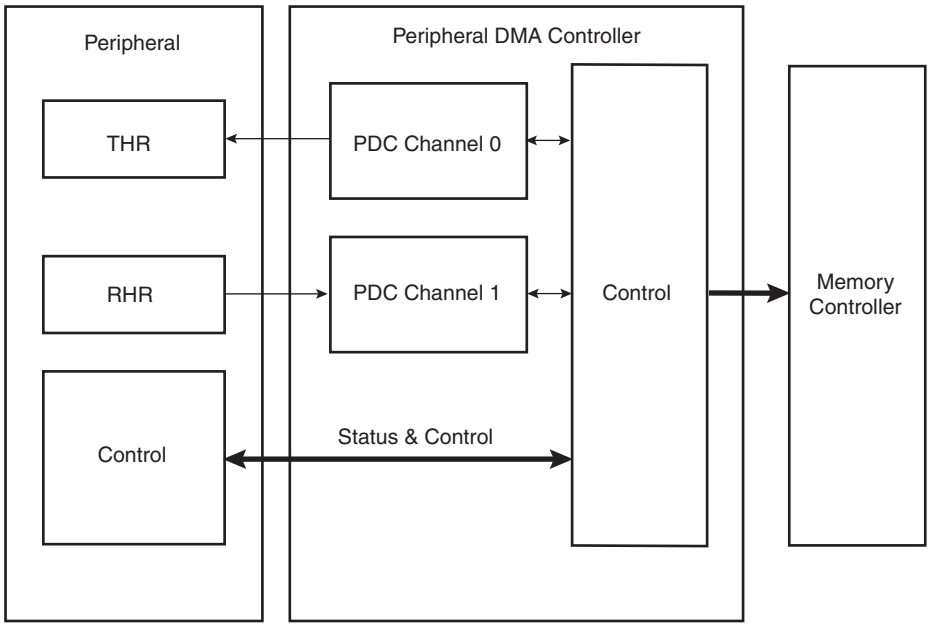
The user interface of a PDC channel is integrated in the memory space of each peripheral. It contains:

- A 32-bit memory pointer register
- A 16-bit transfer count register
- A 32-bit register for next memory pointer
- A 16-bit register for next transfer count

The peripheral triggers PDC transfers using transmit and receive signals. When the programmed data is transferred, an end of transfer interrupt is generated by the corresponding peripheral.

18.3 Block Diagram

Figure 18-1. Block Diagram



18.4 Product Dependencies

18.4.1 Power Management

The PDC clock is generated by the Power Manager. The PDC also depends on the HSB-HSB bridge clock. Before using the PDC, the programmer must ensure that the PDC clock and HSB-HSB bridge clock are enabled in the Power Manager.

To prevent bus errors the PDC operation must be terminated before entering sleep mode

18.4.2 Interrupt

The PDC has an interrupt line for each channel connected to the Interrupt Controller via the corresponding peripheral. Handling the PDC interrupt requires programming the interrupt controller before configuring the PDC.

18.4.3 Peripherals

Before using each PDC channel the corresponding peripheral has to be configured correctly.

18.5 Functional Description

18.5.1 Configuration

The PDC channels user interface enables the user to configure and control the data transfers for each channel. The user interface of a PDC channel is integrated into the user interface of the peripheral (offset 0x100), which it is related to.

Per peripheral, it contains four 32-bit Pointer Registers (RPR, RNPR, TPR, and TNPR) and four 16-bit Counter Registers (RCR, RNCR, TCR, and TNCR).

The size of the buffer (number of transfers) is configured in an internal 16-bit transfer counter register, and it is possible, at any moment, to read the number of transfers left for each channel.

The memory base address is configured in a 32-bit memory pointer by defining the location of the first address to access in the memory. It is possible, at any moment, to read the location in memory of the next transfer and the number of remaining transfers. The PDC has dedicated status registers which indicate if the transfer is enabled or disabled for each channel. The status for each channel is located in the peripheral status register. Transfers can be enabled and/or disabled by setting TXTEN/TXTDIS and RXTEN/RXTDIS in PDC Transfer Control Register. These control bits enable reading the pointer and counter registers safely without any risk of their changing between both reads.

The PDC sends status flags to the peripheral visible in its status-register (ENDRX, ENDTX, RXBUFF, and TXBUFE).

ENDRX flag is set when the PERIPH_RCR register reaches zero.

RXBUFF flag is set when both PERIPH_RCR and PERIPH_RNCR reach zero.

ENDTX flag is set when the PERIPH_TCR register reaches zero.

TXBUFE flag is set when both PERIPH_TCR and PERIPH_TNCR reach zero.

These status flags are described in the peripheral status register.

18.5.2 Memory Pointers

Each peripheral is connected to the PDC by a receiver data channel and a transmitter data channel. Each channel has an internal 32-bit memory pointer. Each memory pointer points to a location anywhere in the memory space (on-chip memory or external bus interface memory).

Depending on the type of transfer (byte, half-word or word), the memory pointer is incremented by 1, 2 or 4, respectively for peripheral transfers. The size of the transfer is setup up in the peripheral's control register and automatically sensed by the PDC. The size is always rounded up to wither byte, half-word or word.

If a memory pointer is reprogrammed while the PDC is in operation, the transfer address is changed, and the PDC performs transfers using the new address.

18.5.3 Transfer Counters

There is one internal 16-bit transfer counter for each channel used to count the size of the block already transferred by its associated channel. These counters are decremented after each data transfer. When the counter reaches zero, the transfer is complete and the PDC stops transferring data.

If the Next Counter Register is equal to zero, the PDC disables the trigger while activating the related peripheral end flag.

If the counter is reprogrammed while the PDC is operating, the number of transfers is updated and the PDC counts transfers from the new value.

Programming the Next Counter/Pointer registers chains the buffers. The counters are decremented after each data transfer as stated above, but when the transfer counter reaches zero, the values of the Next Counter/Pointer are loaded into the Counter/Pointer registers in order to re-enable the triggers.

For each channel, two status bits indicate the end of the current buffer (ENDRX, ENTX) and the end of both current and next buffer (RXBUFF, TXBUFE). These bits are directly mapped to the peripheral status register and can trigger an interrupt request to the Interrupt Controller.

The peripheral end flag is automatically cleared when one of the counter-registers (Counter or Next Counter Register) is written.

Note: When the Next Counter Register is loaded into the Counter Register, it is set to zero.

18.5.4 Data Transfers

The peripheral triggers PDC transfers using transmit (TXRDY) and receive (RXRDY) signals.

When the peripheral receives an external character, it sends a Receive Ready signal to the PDC which then requests access to the system bus. When access is granted, the PDC starts a read of the peripheral Receive Holding Register (RHR) and then triggers a write in the memory.

After each transfer, the relevant PDC memory pointer is incremented and the number of transfers left is decremented. When the memory block size is reached, a signal is sent to the peripheral and the transfer stops.

The same procedure is followed, in reverse, for transmit transfers.

18.5.5 Priority of PDC Transfer Requests

The Peripheral DMA Controller handles transfer requests from the channel according to priorities fixed for each product.These priorities are defined in the product datasheet.

If simultaneous requests of the same type (receiver or transmitter) occur on identical peripherals, the priority is determined by the numbering of the peripherals.

If transfer requests are not simultaneous, they are treated in the order they occurred. Requests from the receivers are handled first and then followed by transmitter requests.

18.6 Peripheral DMA Controller (PDC) User Interface

Table 18-1. Register Mapping

Offset	Register	Register Name	Read/Write	Reset
0x100	Receive Pointer Register	PERIPH[(1)]_RPR	Read/Write	0x0
0x104	Receive Counter Register	PERIPH_RCR	Read/Write	0x0
0x108	Transmit Pointer Register	PERIPH_TPR	Read/Write	0x0
0x10C	Transmit Counter Register	PERIPH_TCR	Read/Write	0x0
0x110	Receive Next Pointer Register	PERIPH_RNPR	Read/Write	0x0
0x114	Receive Next Counter Register	PERIPH_RNCR	Read/Write	0x0
0x118	Transmit Next Pointer Register	PERIPH_TNPR	Read/Write	0x0
0x11C	Transmit Next Counter Register	PERIPH_TNCR	Read/Write	0x0
0x120	PDC Transfer Control Register	PERIPH_PTCR	Write-only	-
0x124	PDC Transfer Status Register	PERIPH_PTSR	Read-only	0x0

Note: 1. PERIPH: Ten registers are mapped in the peripheral memory space at the same offset. These can be defined by the user according to the function and the peripheral desired (USART, SSC, SPI, etc).

18.6.1 PDC Receive Pointer Register

Register Name: PERIPH_RPR

Access Type: Read/Write

31	30	29	28	27	26	25	24
RXPTR							
23	22	21	20	19	18	17	16
RXPTR							
15	14	13	12	11	10	9	8
RXPTR							
7	6	5	4	3	2	1	0
RXPTR							

- **RXPTR: Receive Pointer Address**

Address of the next receive transfer.

18.6.2 PDC Receive Counter Register

Register Name: PERIPH_RCR

Access Type: Read/Write

31	30	29	28	27	26	25	24
--							
23	22	21	20	19	18	17	16
--							
15	14	13	12	11	10	9	8
RXCTR							
7	6	5	4	3	2	1	0
RXCTR							

- **RXCTR: Receive Counter Value**

Number of receive transfers to be performed.

18.6.3 PDC Transmit Pointer Register

Register Name: PERIPH_TPR

Access Type: Read/Write

31	30	29	28	27	26	25	24
TXPTR							

23	22	21	20	19	18	17	16
TXPTR							

15	14	13	12	11	10	9	8
TXPTR							

7	6	5	4	3	2	1	0
TXPTR							

- **TXPTR: Transmit Pointer Address**

Address of the transmit buffer.

18.6.4 PDC Transmit Counter Register

Register Name: PERIPH_TCR

Access Type: Read/Write

31	30	29	28	27	26	25	24
--							
23	22	21	20	19	18	17	16
--							
15	14	13	12	11	10	9	8
TXCTR							
7	6	5	4	3	2	1	0
TXCTR							

- **TXCTR: Transmit Counter Value**

TXCTR is the size of the transmit transfer to be performed. At zero, the peripheral data transfer is stopped.

18.6.5 PDC Receive Next Pointer Register

Register Name: PERIPH_RNPR

Access Type: Read/Write

31	30	29	28	27	26	25	24
RXNPTR							
23	22	21	20	19	18	17	16
RXNPTR							
15	14	13	12	11	10	9	8
RXNPTR							
7	6	5	4	3	2	1	0
RXNPTR							

- **RXNPTR: Receive Next Pointer Address**

RXNPTR is the address of the next buffer to fill with received data when the current buffer is full.

18.6.6 PDC Receive Next Counter Register

Register Name: PERIPH_RNCR

Access Type: Read/Write

31	30	29	28	27	26	25	24
--							
23	22	21	20	19	18	17	16
--							
15	14	13	12	11	10	9	8
RXNCR							
7	6	5	4	3	2	1	0
RXNCR							

- **RXNCR: Receive Next Counter Value**

RXNCR is the size of the next buffer to receive.

18.6.7 PDC Transmit Next Pointer Register

Register Name: PERIPH_TNPR

Access Type: Read/Write

31	30	29	28	27	26	25	24
TXNPTR							
23	22	21	20	19	18	17	16
TXNPTR							
15	14	13	12	11	10	9	8
TXNPTR							
7	6	5	4	3	2	1	0
TXNPTR							

- **TXNPTR: Transmit Next Pointer Address**

TXNPTR is the address of the next buffer to transmit when the current buffer is empty.

18.6.8 PDC Transmit Next Counter Register

Register Name: PERIPH_TNCR

Access Type: Read/Write

31	30	29	28	27	26	25	24
--							
23	22	21	20	19	18	17	16
--							
15	14	13	12	11	10	9	8
TXNCR							
7	6	5	4	3	2	1	0
TXNCR							

- **TXNCR: Transmit Next Counter Value**

TXNCR is the size of the next buffer to transmit.

18.6.9 PDC Transfer Control Register

Register Name: PERIPH_PTCR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXTDIS	TXTEN
7	6	5	4	3	2	1	0
–	–	–	–	–	–	RXTDIS	RXTEN

- **RXTEN: Receiver Transfer Enable**

0 = No effect.

1 = Enables the receiver PDC transfer requests if RXTDIS is not set.

- **RXTDIS: Receiver Transfer Disable**

0 = No effect.

1 = Disables the receiver PDC transfer requests.

- **TXTEN: Transmitter Transfer Enable**

0 = No effect.

1 = Enables the transmitter PDC transfer requests.

- **TXTDIS: Transmitter Transfer Disable**

0 = No effect.

1 = Disables the transmitter PDC transfer requests

18.6.10 PDC Transfer Status Register

Register Name: PERIPH_PTSR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	TXTEN
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	RXTEN

- **RXTEN: Receiver Transfer Enable**

0 = Receiver PDC transfer requests are disabled.

1 = Receiver PDC transfer requests are enabled.

- **TXTEN: Transmitter Transfer Enable**

0 = Transmitter PDC transfer requests are disabled.

1 = Transmitter PDC transfer requests are enabled.

19. Parallel Input/Output Controller (PIO)

Rev: 2.0.2.3

19.1 Features

- **Up to 32 Programmable I/O Lines**
- **Fully Programmable through Set/Clear Registers**
- **Multiplexing of Two Peripheral Functions per I/O Line**
- **For each I/O Line (Whether Assigned to a Peripheral or Used as General Purpose I/O)**
  - **Input Change Interrupt**
  - **Glitch Filter**
  - **Programmable Pull Up on Each I/O Line**
  - **Pin Data Status Register, Supplies Visibility of the Level on the Pin at Any Time**
- **Synchronous Output, Provides Set and Clear of Several I/O lines in a Single Write**

19.2 Description

The Parallel Input/Output Controller (PIO) manages up to 32 fully programmable input/output lines. Each I/O line may be dedicated as a general-purpose I/O or be assigned to a function of an embedded peripheral. This assures effective optimization of the pins of a product.

Each I/O line is associated with a bit number in all of the 32-bit registers of the 32-bit wide User Interface.

Each I/O line of the PIO Controller features:

- An input change interrupt enabling level change detection on any I/O line.
- A glitch filter providing rejection of pulses lower than one-half of clock cycle.
- Control of the the pull-up of the I/O line.
- Input visibility and output control.

The PIO Controller also features a synchronous output providing up to 32 bits of data output in a single write operation.

19.3 Block Diagram

Figure 19-1. Block Diagram

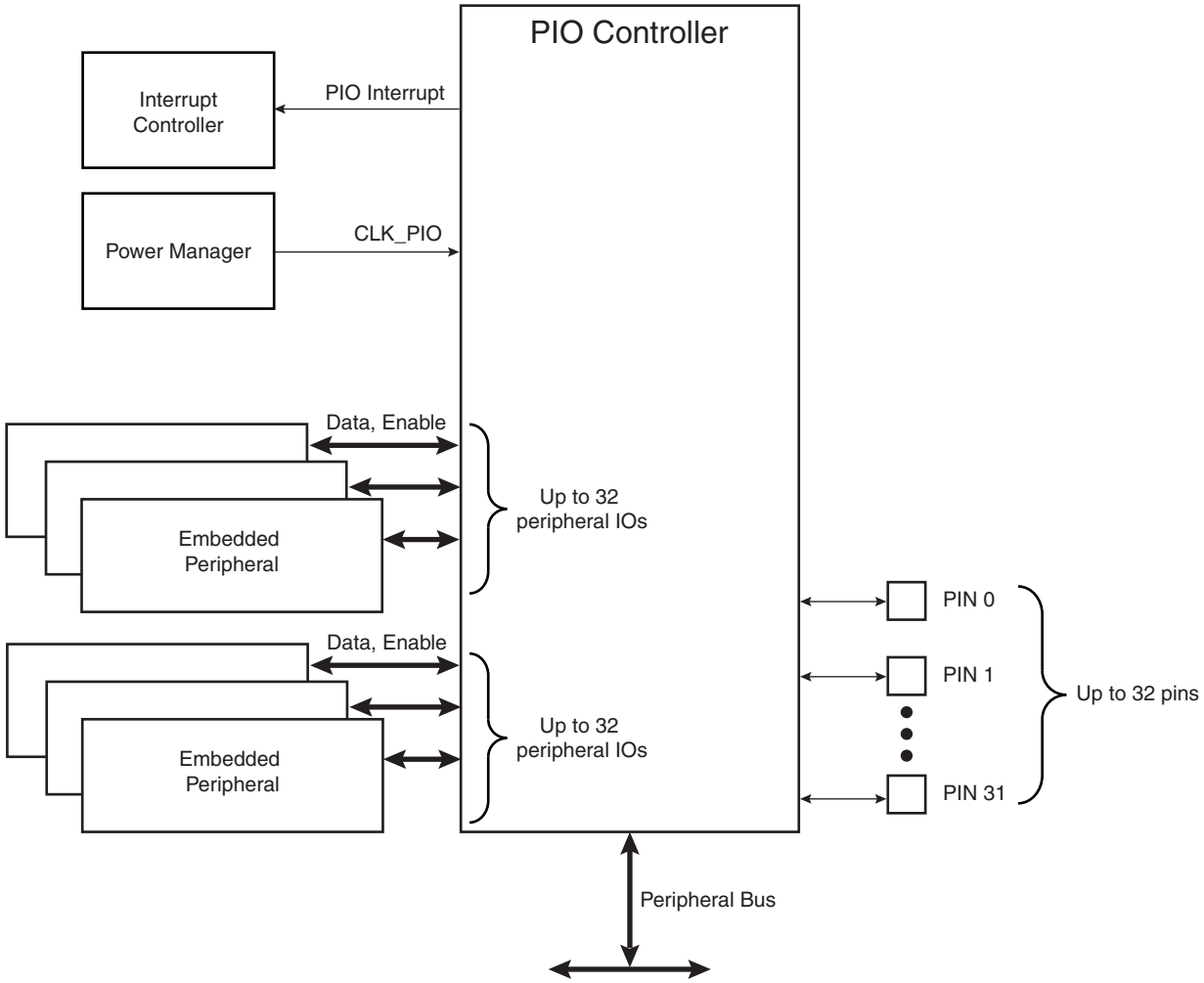
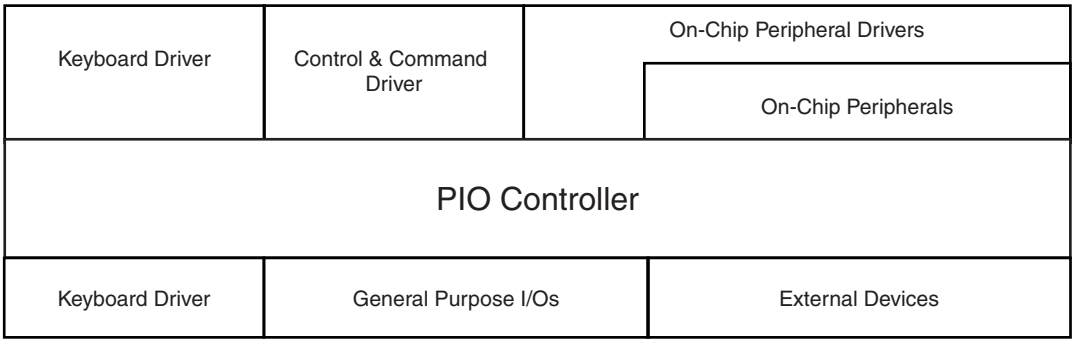


Figure 19-2. Application Block Diagram



19.4 Product Dependencies

19.4.1 Pin Multiplexing

Each pin is configurable, according to product definition as either a general-purpose I/O line only, or as an I/O line multiplexed with one or two peripheral I/Os. As the multiplexing is hardware-defined and thus product-dependent, the hardware designer and programmer must carefully determine the configuration of the PIO controllers required by their application. When an I/O line is general-purpose only, i.e. not multiplexed with any peripheral I/O, programming of the PIO Controller regarding the assignment to a peripheral has no effect and only the PIO Controller can control how the pin is driven by the product.

19.4.2 External Interrupt Lines

The external interrupt request signals are most generally multiplexed through the PIO Controllers. However, it is not necessary to assign the I/O line to the interrupt function as the PIO Controller has no effect on inputs and the external interrupt lines are used only as inputs.

19.4.3 Power Management

The PIO clock (CLK_PIO) is generated by the Power Manager. Before accessing the PIO, the programmer must ensure that CLK_PIO is enabled in the Power Manager. Note that CLK_PIO must be enabled when using the Input Change interrupt.

In the PIO description, CLK_PIO is the clock of the peripheral bus to which the PIO is connected.

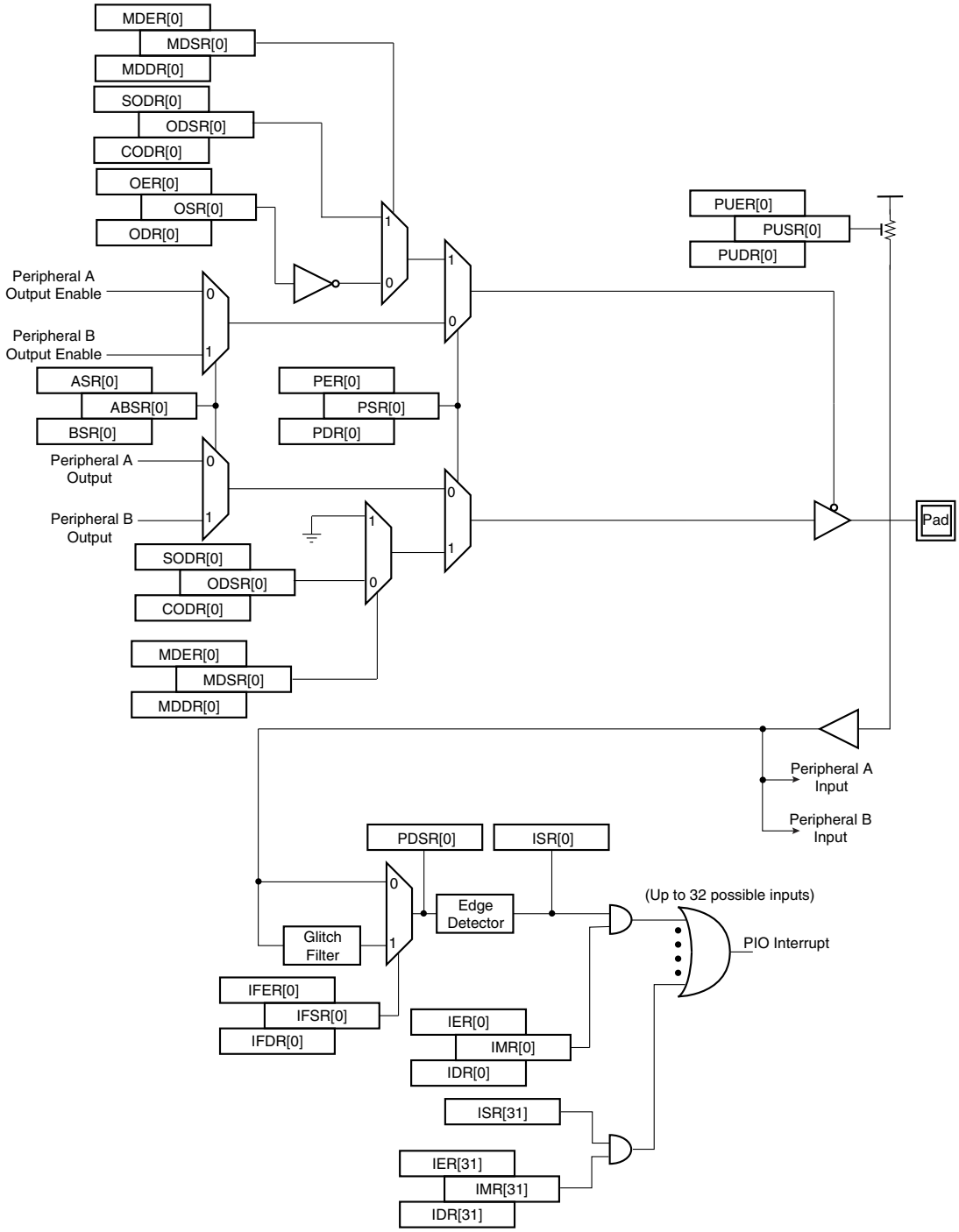
19.4.4 Interrupt Generation

The PIO interrupt line is connected to the Interrupt Controller. Using the PIO interrupt requires the Interrupt Controller to be programmed first.

19.5 Functional Description

The PIO Controller features up to 32 fully-programmable I/O lines. Most of the control logic associated to each I/O is represented in Figure 19-3. In this description each signal shown represents but one of up to 32 possible indexes.

Figure 19-3. I/O Line Control Logic



19.5.1 Pull-up Resistor Control

Each I/O line is designed with an embedded pull-up resistor. The pull-up resistor can be enabled or disabled by writing respectively PUER (Pull-up Enable Register) and PUDR (Pull-up Disable Resistor). Writing in these registers results in setting or clearing the corresponding bit in PUSR (Pull-up Status Register). Reading a 1 in PUSR means the pull-up is disabled and reading a 0 means the pull-up is enabled.

Control of the pull-up resistor is possible regardless of the configuration of the I/O line.

After reset, all of the pull-ups are enabled, i.e. PUSR resets at the value 0x0.

19.5.2 I/O Line or Peripheral Function Selection

When a pin is multiplexed with one or two peripheral functions, the selection is controlled with the registers PER (PIO Enable Register) and PDR (PIO Disable Register). The register PSR (PIO Status Register) is the result of the set and clear registers and indicates whether the pin is controlled by the corresponding peripheral or by the PIO Controller. A value of 0 indicates that the pin is controlled by the corresponding on-chip peripheral selected in the ABSR (AB Select Status Register). A value of 1 indicates the pin is controlled by the PIO controller.

If a pin is used as a general purpose I/O line (not multiplexed with an on-chip peripheral), PER and PDR have no effect and PSR returns 1 for the corresponding bit.

After reset, most generally, the I/O lines are controlled by the PIO controller, i.e. PSR resets at 1. However, in some events, it is important that PIO lines are controlled by the peripheral (as in the case of memory chip select lines that must be driven inactive after reset or for address lines that must be driven low for booting out of an external memory). Thus, the reset value of PSR is defined at the product level, depending on the multiplexing of the device.

19.5.3 Peripheral A or B Selection

The PIO Controller provides multiplexing of up to two peripheral functions on a single pin. The selection is performed by writing ASR (A Select Register) and BSR (Select B Register). ABSR (AB Select Status Register) indicates which peripheral line is currently selected. For each pin, the corresponding bit at level 0 means peripheral A is selected whereas the corresponding bit at level 1 indicates that peripheral B is selected.

Note that multiplexing of peripheral lines A and B only affects the output line. The peripheral input lines are always connected to the pin input.

After reset, ABSR is 0, thus indicating that all the PIO lines are configured on peripheral A. However, peripheral A generally does not drive the pin as the PIO Controller resets in I/O line mode.

Writing in ASR and BSR manages ABSR regardless of the configuration of the pin. However, assignment of a pin to a peripheral function requires a write in the corresponding peripheral selection register (ASR or BSR) in addition to a write in PDR.

19.5.4 Output Control

When the I/0 line is assigned to a peripheral function, i.e. the corresponding bit in PSR is at 0, the drive of the I/O line is controlled by the peripheral. Peripheral A or B, depending on the value in ABSR, determines whether the pin is driven or not.

When the I/O line is controlled by the PIO controller, the pin can be configured to be driven. This is done by writing OER (Output Enable Register) and ODR (Output Disable Register). The results of these write operations are detected in OSR (Output Status Register). When a bit in this

register is at 0, the corresponding I/O line is used as an input only. When the bit is at 1, the corresponding I/O line is driven by the PIO controller.

The level driven on an I/O line can be determined by writing in SODR (Set Output Data Register) and CODR (Clear Output Data Register). These write operations respectively set and clear ODSR (Output Data Status Register), which represents the data driven on the I/O lines. Writing in OER and ODR manages OSR whether the pin is configured to be controlled by the PIO controller or assigned to a peripheral function. This enables configuration of the I/O line prior to setting it to be managed by the PIO Controller.

Similarly, writing in SODR and CODR effects ODSR. This is important as it defines the first level driven on the I/O line.

19.5.5 Multi-drive capability

The PIO is able to configure each pin as open drain to support external drivers on the same pin. This is done by writing MDER (Multi-Drive Enable Register) and MDDR (Multi-Drive Disable Register). The result of these write operations are detected in MDSR (multui-Drive Status Register). The multi-drive mode is only available when the PIO is controlling the pin, i.e. PSR is set.

When using multi-drive the PIO will tri-state the pin when ODSR is set and drive the pin low when ODSR is cleared. writing to OER or ODR will have no effect.

19.5.6 Synchronous Data Output

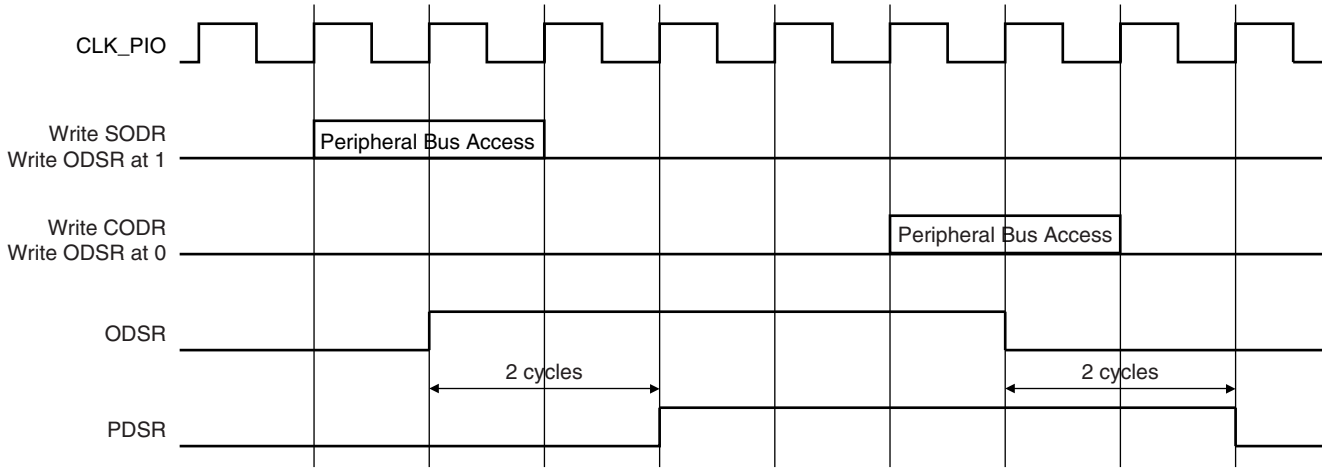
Controlling all parallel busses using several PIOs requires two successive write operations in the SODR and CODR registers. This may lead to unexpected transient values. The PIO controller offers a direct control of PIO outputs by single write access to ODSR (Output Data Status Register). Only bits unmasked by OWSR (Output Write Status Register) are written. The mask bits in the OWSR are set by writing to OWER (Output Write Enable Register) and cleared by writing to OWDR (Output Write Disable Register).

After reset, the synchronous data output is disabled on all the I/O lines as OWSR resets at 0x0.

19.5.7 Output Line Timings

Figure 19-4 shows how the outputs are driven either by writing SODR or CODR, or by directly writing ODSR. This last case is valid only if the corresponding bit in OWSR is set. Figure 19-4 also shows when the feedback in PDSR is available.

Figure 19-4. Output Line Timings



19.5.8 Inputs

The level on each I/O line can be read through PDSR (Pin Data Status Register). This register indicates the level of the I/O lines regardless of their configuration, whether uniquely as an input or driven by the PIO controller or driven by a peripheral.

Reading the I/O line levels requires the clock of the PIO controller to be enabled, otherwise PDSR reads the levels present on the I/O line at the time the clock was disabled.

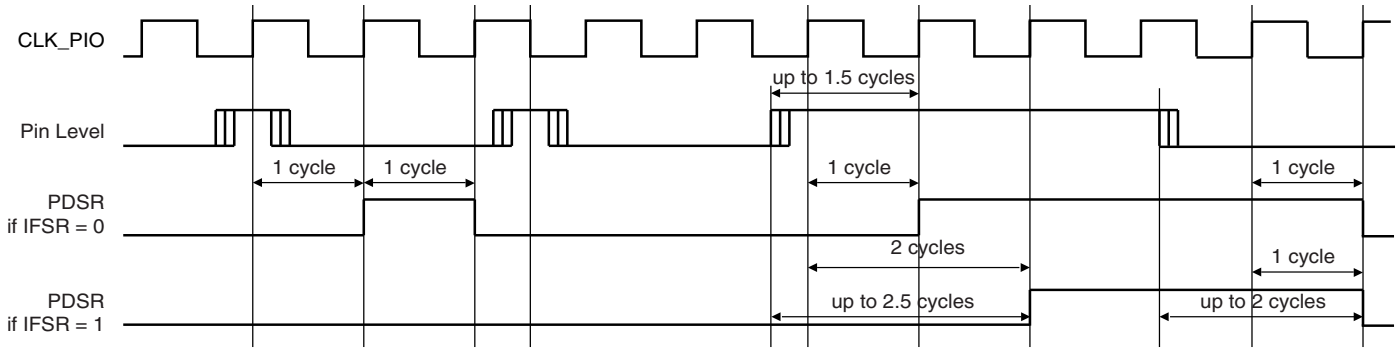
19.5.9 Input Glitch Filtering

Optional input glitch filters are independently programmable on each I/O line. When the glitch filter is enabled, a glitch with a duration of less than 1/2 CLK_PIO cycle is automatically rejected, while a pulse with a duration of 1 CLK_PIO cycle or more is accepted. For pulse durations between 1/2 CLK_PIO cycle and 1 CLK_PIO cycle the pulse may or may not be taken into account, depending on the precise timing of its occurrence. Thus for a pulse to be visible it must exceed 1 CLK_PIO cycle, whereas for a glitch to be reliably filtered out, its duration must not exceed 1/2 CLK_PIO cycle. The filter introduces one CLK_PIO cycle latency if the pin level change occurs before a rising edge. However, this latency does not appear if the pin level change occurs before a falling edge. This is illustrated in Figure 19-5.

The glitch filters are controlled by the register set; IFER (Input Filter Enable Register), IFDR (Input Filter Disable Register) and IFSR (Input Filter Status Register). Writing IFER and IFDR respectively sets and clears bits in IFSR. This last register enables the glitch filter on the I/O lines.

When the glitch filter is enabled, it does not modify the behavior of the inputs on the peripherals. It acts only on the value read in PDSR and on the input change interrupt detection. The glitch filters require that the PIO Controller clock is enabled.

Figure 19-5. Input Glitch Filter Timing



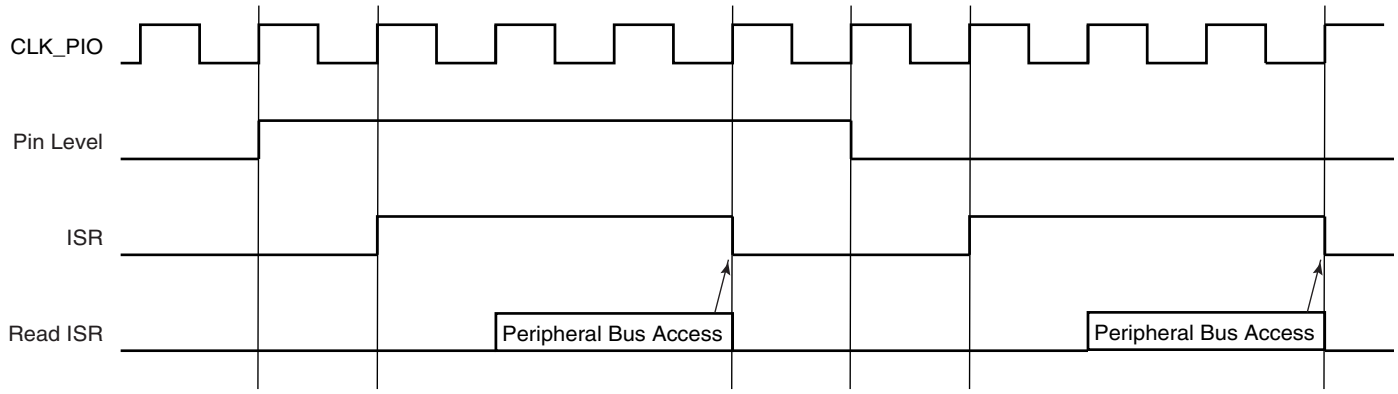
19.5.10 Input Change Interrupt

The PIO Controller can be programmed to generate an interrupt when it detects an input change on an I/O line. The Input Change Interrupt is controlled by writing IER (Interrupt Enable Register) and IDR (Interrupt Disable Register), which respectively enable and disable the input change interrupt by setting and clearing the corresponding bit in IMR (Interrupt Mask Register). As Input change detection is possible only by comparing two successive samplings of the input of the I/O line, the PIO Controller clock must be enabled. The Input Change Interrupt is available, regardless of the configuration of the I/O line, i.e. configured as an input only, controlled by the PIO Controller or assigned to a peripheral function.

When an input change is detected on an I/O line, the corresponding bit in ISR (Interrupt Status Register) is set. If the corresponding bit in IMR is set, the PIO Controller interrupt line is asserted. The interrupt signals of the thirty-two channels are ORed-wired together to generate a single interrupt signal to the Interrupt Controller.

When the software reads ISR, all the interrupts are automatically cleared. This signifies that all the interrupts that are pending when ISR is read must be handled.

Figure 19-6. Input Change Interrupt Timings



19.6 I/O Lines Programming Example

The programing example as shown in Table 19-1 below is used to define the following configuration.

- 4-bit output port on I/O lines 0 to 3, (should be written in a single write operation)
- Four output signals on I/O lines 4 to 7 (to drive LEDs for example)
- Four input signals on I/O lines 8 to 11 (to read push-button states for example), with pull-up resistors, glitch filters and input change interrupts
- Four input signals on I/O line 12 to 15 to read an external device status (polled, thus no input change interrupt), no pull-up resistor, no glitch filter
- I/O lines 16 to 19 assigned to peripheral A functions with pull-up resistor
- I/O lines 20 to 23 assigned to peripheral B functions, no pull-up resistor
- I/O line 24 to 27 assigned to peripheral A with Input Change Interrupt and pull-up resistor

Table 19-1. Programming Example

Register	Value to be Written
PER	0x0000 FFFF
PDR	0x0FFF 0000
OER	0x0000 00FF
ODR	0x0FFF FF00
IFER	0x0000 0F00
IFDR	0x0FFF F0FF
SODR	0x0000 0000
CODR	0x0FFF FFFF
IER	0x0F00 0F00
IDR	0x00FF F0FF
PUDR	0x00F0 00F0
PUER	0x0F0F FF0F
ASR	0x0F0F 0000
BSR	0x00F0 0000
OWER	0x0000 000F
OWDR	0x0FFF FFF0

19.7 User Interface

Each I/O line controlled by the PIO Controller is associated with a bit in each of the PIO Controller User Interface registers. Each register is 32 bits wide. If a parallel I/O line is not defined, writing to the corresponding bits has no effect. Undefined bits read zero. If the I/O line is not multiplexed with any peripheral, the I/O line is controlled by the PIO Controller and PSR returns 1 systematically.

Table 19-2. Register Mapping

Offset	Register	Name	Access	Reset Value
0x0000	PIO Enable Register	PER	Write-only	–
0x0004	PIO Disable Register	PDR	Write-only	–
0x0008	PIO Status Register	PSR	Read-only	(1)
0x000C	Reserved			
0x0010	Output Enable Register	OER	Write-only	–
0x0014	Output Disable Register	ODR	Write-only	–
0x0018	Output Status Register	OSR	Read-only	0x0000 0000
0x001C	Reserved			
0x0020	Glitch Input Filter Enable Register	IFER	Write-only	–
0x0024	Glitch Input Filter Disable Register	IFDR	Write-only	–
0x0028	Glitch Input Filter Status Register	IFSR	Read-only	0x0000 0000
0x002C	Reserved			
0x0030	Set Output Data Register	SODR	Write-only	–
0x0034	Clear Output Data Register	CODR	Write-only	–
0x0038	Output Data Status Register	ODSR	Read-only or Read/Write(2)	0x0000 0000
0x003C	Pin Data Status Register(3)	PDSR	Read-only	
0x0040	Interrupt Enable Register	IER	Write-only	–
0x0044	Interrupt Disable Register	IDR	Write-only	–
0x0048	Interrupt Mask Register	IMR	Read-only	0x0000 0000
0x004C	Interrupt Status Register(4)	ISR	Read-only	0x0000 0000
0x0050	Multi-driver Enable Register	MDER	Write-only	
0x0054	Multi-driver Disable Register	MDDR	Write-only	
0x0058	Multi-driver Status Register	MDSR	Read-only	
0x005C	Reserved			
0x0060	Pull-up Disable Register	PUDR	Write-only	–
0x0064	Pull-up Enable Register	PUER	Write-only	–
0x0068	Pad Pull-up Status Register	PUSR	Read-only	0x0000 0000

Table 19-2. Register Mapping (Continued)

Offset	Register	Name	Access	Reset Value
0x006C	Reserved			
0x0070	Peripheral A Select Register(5)	ASR	Write-only	–
0x0074	Peripheral B Select Register(5)	BSR	Write-only	–
0x0078	AB Status Register(5)	ABSR	Read-only	0x0000 0000
0x007C to 0x009C	Reserved			
0x00A0	Output Write Enable	OWER	Write-only	–
0x00A4	Output Write Disable	OWDR	Write-only	–
0x00A8	Output Write Status Register	OWSR	Read-only	0x0000 0000
0x00AC- 0x00FC	Reserved			

Notes:
1. Reset value of PSR depends on the product implementation.
2. ODSR is Read-only or Read/Write depending on OWSR I/O lines.
3. Reset value of PDSR depends on the level of the I/O lines.
4. ISR is reset at 0x0. However, the first read of the register may read a different value as input changes may have occurred.
5. Only this set of registers clears the status by writing 1 in the first register and sets the status by writing 1 in the second register.

19.7.1 PIO Controller PIO Enable Register

Name: PER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: PIO Enable**

0 = No effect.

1 = Enables the PIO to control the corresponding pin (disables peripheral control of the pin).

19.7.2 PIO Controller PIO Disable Register

Name: PDR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: PIO Disable**

0 = No effect.

1 = Disables the PIO from controlling the corresponding pin (enables peripheral control of the pin).

19.7.3 PIO Controller PIO Status Register

Name: PSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: PIO Status**

0 = PIO is inactive on the corresponding I/O line (peripheral is active).

1 = PIO is active on the corresponding I/O line (peripheral is inactive).

19.7.4 PIO Controller Output Enable Register

Name: OER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Enable**

0 = No effect.

1 = Enables the output on the I/O line.

19.7.5 PIO Controller Output Disable Register

Name: ODR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Disable**

0 = No effect.

1 = Disables the output on the I/O line.

19.7.6 PIO Controller Output Status Register

Name: OSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Status**

0 = The I/O line is a pure input.

1 = The I/O line is enabled in output.

19.7.7 PIO Controller Glitch Input Filter Enable Register

Name: IFER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Filter Enable**

0 = No effect.

1 = Enables the input glitch filter on the I/O line.

19.7.8 PIO Controller Glitch Input Filter Disable Register

Name: IFDR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Filter Disable**

0 = No effect.

1 = Disables the input glitch filter on the I/O line.

19.7.9 PIO Controller Glitch Input Filter Status Register

Name: IFSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Filer Status**

0 = The input glitch filter is disabled on the I/O line.

1 = The input glitch filter is enabled on the I/O line.

19.7.10 PIO Controller Set Output Data Register

Name: SODR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Set Output Data**

0 = No effect.

1 = Sets the data to be driven on the I/O line.

19.7.11 PIO Controller Clear Output Data Register

Name: CODR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Set Output Data**

0 = No effect.

1 = Clears the data to be driven on the I/O line.

19.7.12 PIO Controller Output Data Status Register

Name: ODSR

Access Type: Read-only or Read/Write

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Data Status**

0 = The data to be driven on the I/O line is 0.

1 = The data to be driven on the I/O line is 1.

19.7.13 PIO Controller Pin Data Status Register

Name: PDSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Data Status**

0 = The I/O line is at level 0.

1 = The I/O line is at level 1.

19.7.14 PIO Controller Interrupt Enable Register

Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Change Interrupt Enable**

0 = No effect.

1 = Enables the Input Change Interrupt on the I/O line.

19.7.15 PIO Controller Interrupt Disable Register

Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Change Interrupt Disable**

0 = No effect.

1 = Disables the Input Change Interrupt on the I/O line.

19.7.16 PIO Controller Interrupt Mask Register

Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Change Interrupt Mask**

0 = Input Change Interrupt is disabled on the I/O line.

1 = Input Change Interrupt is enabled on the I/O line.

19.7.17 PIO Controller Interrupt Status Register

Name: ISR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Input Change Interrupt Status**

0 = No Input Change has been detected on the I/O line since ISR was last read or since reset.

1 = At least one Input Change has been detected on the I/O line since ISR was last read or since reset.

19.7.18 PIO Controller Multi-driver Enable Register

Name: MDER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register is used to enable PIO output drivers to be configured as open drain to support external drivers on the same pin.

- **P0-P31:**

0 = No effect.

1 = Enables multi-drive option on the corresponding pin.

19.7.19 PIO Controller Multi-driver Disable Register

Name: MDDR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register is used to diasble the open drain configuration of the output buffer.

- **P0-P31:**

0 = No effect.

1 = Disables multi-drive option on the corresponding pin.

19.7.20 PIO Controller Multi-driver Status Register

Name: MDSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register indicates which pins are configured with open drain drivers.

- **P0-P31:**

0 = PIO is not configured as an open drain.

1 = PIO is configured as an open drain.

19.7.21 PIO Pull Up Disable Register

Name: PUDR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Pull Up Disable.**

0 = No effect.

1 = Disables the pull up resistor on the I/O line.

19.7.22 PIO Pull Up Enable Register

Name: PUER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Pull Up Enable.**

0 = No effect.

1 = Enables the pull up resistor on the I/O line.

19.7.23 PIO Pull Up Status Register

Name: PUSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Pull Up Status.**

0 = Pull Up resistor is enabled on the I/O line.

1 = Pull Up resistor is disabled on the I/O line.

19.7.24 PIO Peripheral A Select Register

Name: ASR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Peripheral A Select.**

0 = No effect.

1 = Assigns the I/O line to the Peripheral A function.

19.7.25 PIO Peripheral B Select Register

Name: BSR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Peripheral B Select.**

0 = No effect.

1 = Assigns the I/O line to the peripheral B function.

19.7.26 PIO Peripheral A B Status Register

Name: ABSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Peripheral A B Status.**

0 = The I/O line is assigned to the Peripheral A.

1 = The I/O line is assigned to the Peripheral B.

19.7.27 PIO Output Write Enable Register

Name: OWER

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Write Enable.**

0 = No effect.

1 = Enables writing ODSR for the I/O line.

19.7.28 PIO Output Write Disable Register

Name: OWDR

Access Type: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Write Disable.**

0 = No effect.

1 = Disables writing ODSR for the I/O line.

19.7.29 PIO Output Write Status Register

Name: OWSR

Access Type: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: Output Write Status.**

0 = Writing ODSR does not affect the I/O line.

1 = Writing ODSR affects the I/O line.

20. Serial Peripheral Interface (SPI)

Rev: 1.7.1.3

20.1 Features

- **Supports Communication with Serial External Devices**
  - **Four Chip Selects with External Decoder Support Allow Communication with Up to 15 Peripherals**
  - **Serial Memories, such as DataFlash and 3-wire EEPROMs**
  - **Serial Peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors**
  - **External Co-processors**
- **Master or Slave Serial Peripheral Bus Interface**
  - **8- to 16-bit Programmable Data Length Per Chip Select**
  - **Programmable Phase and Polarity Per Chip Select**
  - **Programmable Transfer Delays Between Consecutive Transfers and Between Clock and Data Per Chip Select**
  - **Programmable Delay Between Consecutive Transfers**
  - **Selectable Mode Fault Detection**
- **Connection to PDC Channel Capabilities Optimizes Data Transfers**
  - **One Channel for the Receiver, One Channel for the Transmitter**
  - **Next Buffer Support**

20.2 Description

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave Mode. It also enables communication between processors if an external processor is connected to the system.

The Serial Peripheral Interface is essentially a shift register that serially transmits data bits to other SPIs. During a data transfer, one SPI system acts as the “master”' which controls the data flow, while the other devices act as “slaves'' which have data shifted into and out by the master. Different CPUs can take turn being masters (Multiple Master Protocol opposite to Single Master Protocol where one CPU is always the master while all of the others are always slaves) and one master may simultaneously shift data into multiple slaves. However, only one slave may drive its output to write data back to the master at any given time.

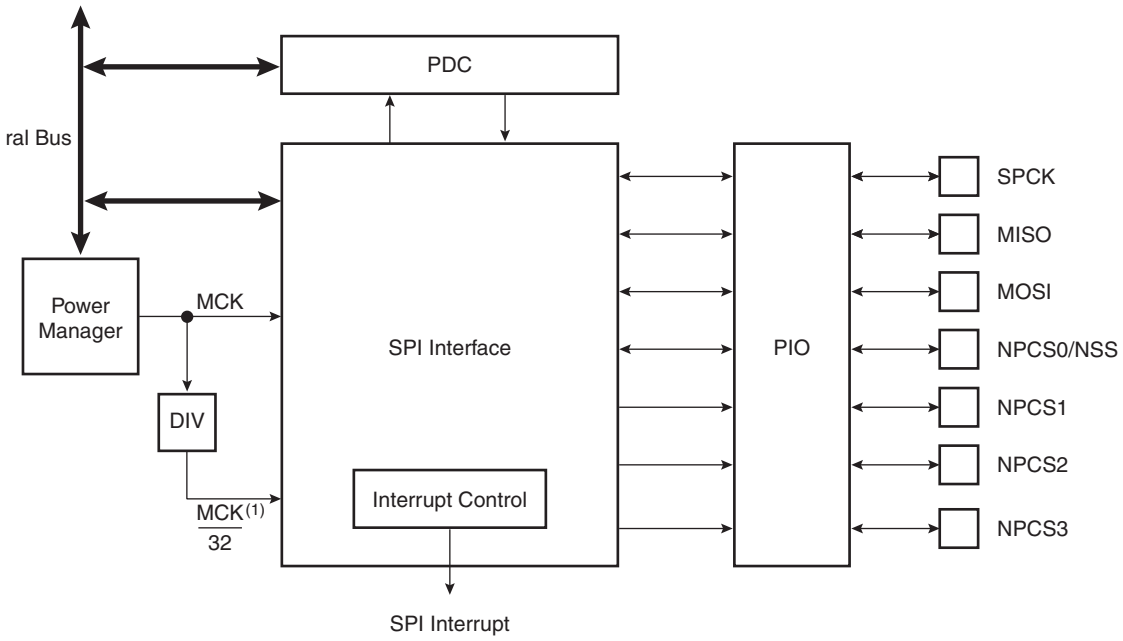
A slave device is selected when the master asserts its NSS signal. If multiple slave devices exist, the master generates a separate slave select signal for each slave (NPCS).

The SPI system consists of two data lines and two control lines:

- Master Out Slave In (MOSI): This data line supplies the output data from the master shifted into the input(s) of the slave(s).
- Master In Slave Out (MISO): This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer.
- Serial Clock (SPCK): This control line is driven by the master and regulates the flow of the data bits. The master may transmit data at a variety of baud rates; the SPCK line cycles once for each bit that is transmitted.
- Slave Select (NSS): This control line allows slaves to be turned on and off by hardware.

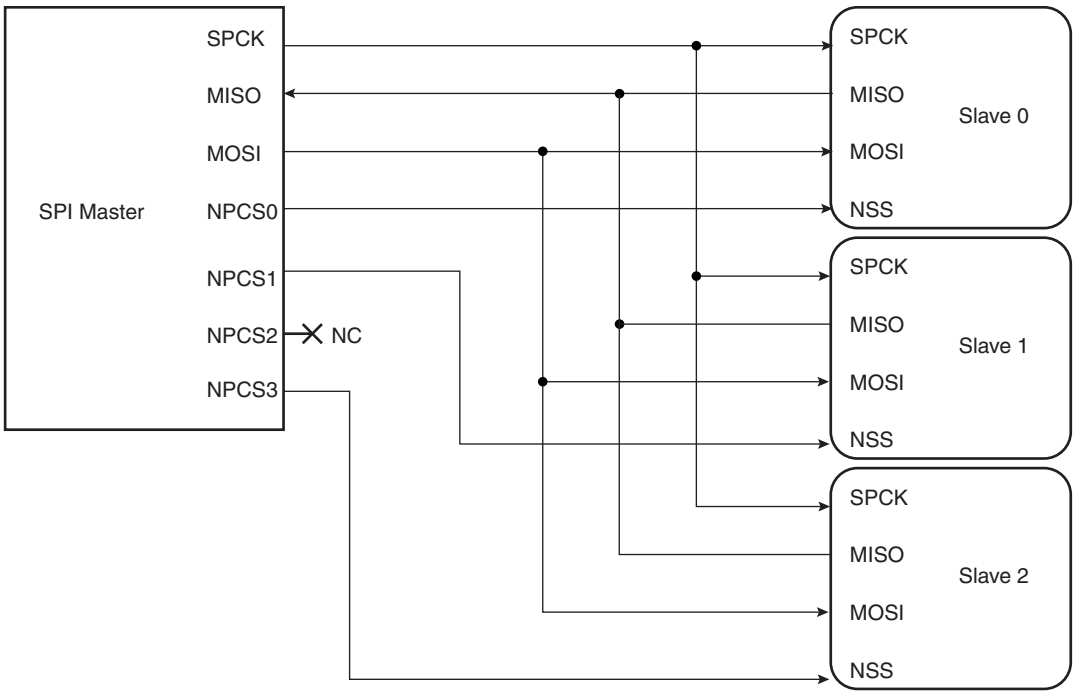
20.3 Block Diagram

Figure 20-1. Block Diagram



20.4 Application Block Diagram

Figure 20-2. Application Block Diagram: Single Master/Multiple Slave Implementation



20.5 Signal Description

Table 20-1. Signal Description

Pin Name	Pin Description	Type	
		Master	Slave
MISO	Master In Slave Out	Input	Output
MOSI	Master Out Slave In	Output	Input
SPCK	Serial Clock	Output	Input
NPCS1-NPCS3	Peripheral Chip Selects	Output	Unused
NPCS0/NSS	Peripheral Chip Select/Slave Select	Output	Input

20.6 Product Dependencies

20.6.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the SPI pins to their peripheral functions. To use the local loopback function the SPI pins must be controlled by the SPI.

20.6.2 Power Management

The SPI clock is generated by the Power Manager. Before using the SPI, the programmer must ensure that the SPI clock is enabled in the Power Manager.

In the SPI description, Master Clock (MCK) is the clock of the peripheral bus to which the SPI is connected.

20.6.3 Interrupt

The SPI interface has an interrupt line connected to the Interrupt Controller. Handling the SPI interrupt requires programming the interrupt controller before configuring the SPI.

20.7 Functional Description

20.7.1 Modes of Operation

The SPI operates in Master Mode or in Slave Mode.

Operation in Master Mode is programmed by writing at 1 the MSTR bit in the Mode Register. The pins NPCS0 to NPCS3 are all configured as outputs, the SPCK pin is driven, the MISO line is wired on the receiver input and the MOSI line driven as an output by the transmitter.

If the MSTR bit is written at 0, the SPI operates in Slave Mode. The MISO line is driven by the transmitter output, the MOSI line is wired on the receiver input, the SPCK pin is driven by the transmitter to synchronize the receiver. The NPCS0 pin becomes an input, and is used as a Slave Select signal (NSS). The pins NPCS1 to NPCS3 are not driven and can be used for other purposes.

The data transfers are identically programmable for both modes of operations. The baud rate generator is activated only in Master Mode.

20.7.2 Data Transfer

Four combinations of polarity and phase are available for data transfers. The clock polarity is programmed with the CPOL bit in the Chip Select Register. The clock phase is programmed with the NCPHA bit. These two parameters determine the edges of the clock signal on which data is driven and sampled. Each of the two parameters has two possible states, resulting in four possible combinations that are incompatible with one another. Thus, a master/slave pair must use the same parameter pair values to communicate. If multiple slaves are used and fixed in different configurations, the master must reconfigure itself each time it needs to communicate with a different slave.

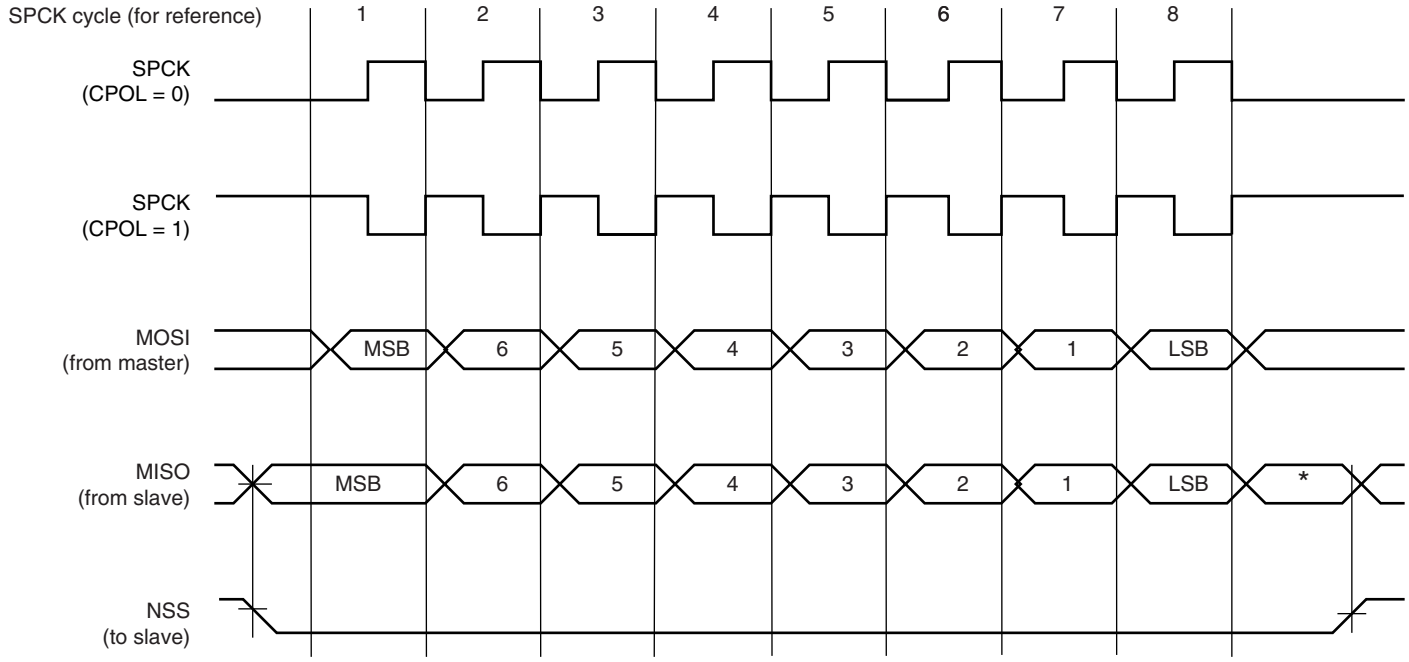
Table 20-2 shows the four modes and corresponding parameter settings.

Table 20-2. SPI Bus Protocol Mode

SPI Mode	CPOL	NCPHA
0	0	1
1	0	0
2	1	1
3	1	0

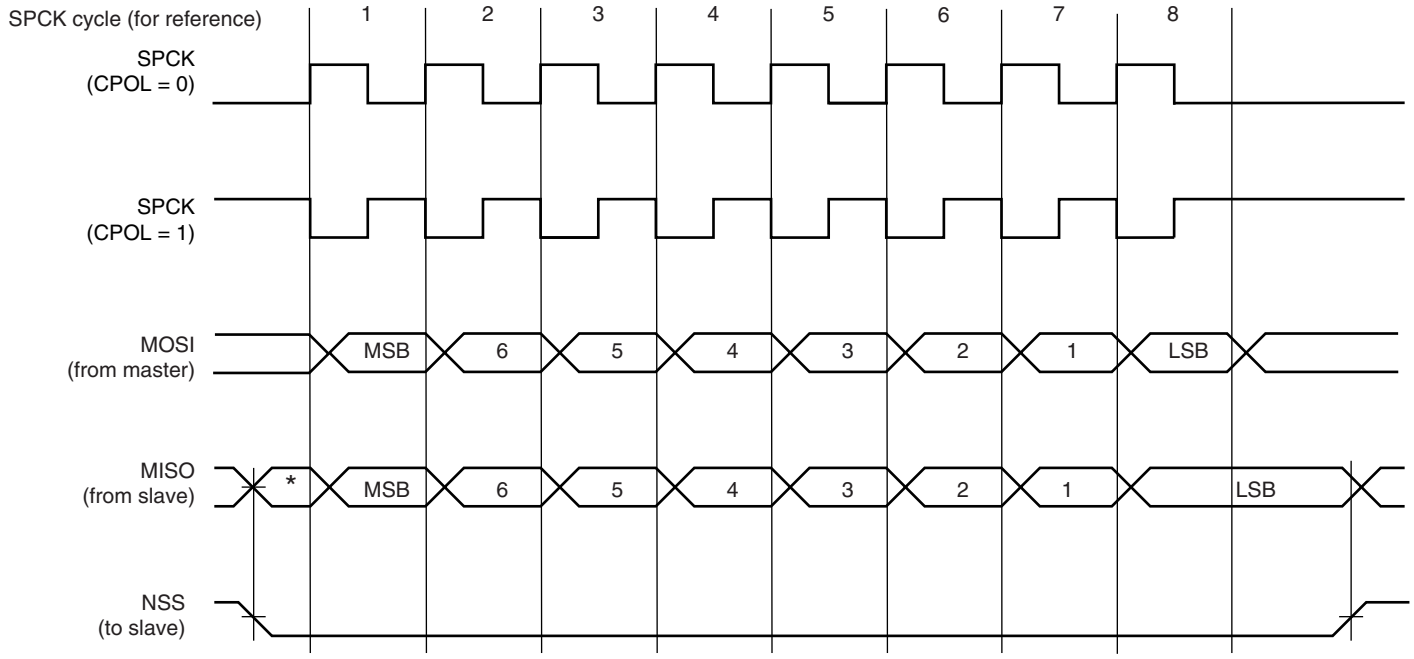
Figure 20-3 and Figure 20-4 show examples of data transfers.

Figure 20-3. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)



* Not defined, but normally MSB of previous character received.

Figure 20-4. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)



* Not defined but normally LSB of previous character transmitted.

20.7.3 Master Mode Operations

When configured in Master Mode, the SPI uses the internal programmable baud rate generator as clock source. It fully controls the data transfers to and from the slave(s) connected to the SPI bus. The SPI drives the chip select line to the slave and the serial clock signal (SPCK).

The SPI features two holding registers, the Transmit Data Register and the Receive Data Register, and a single Shift Register. The holding registers maintain the data flow at a constant rate.

After enabling the SPI, a data transfer begins when the processor writes to the TDR (Transmit Data Register). The written data is immediately transferred in the Shift Register and transfer on the SPI bus starts. While the data in the Shift Register is shifted on the MOSI line, the MISO line is sampled and shifted in the Shift Register. Transmission cannot occur without reception.

Before writing the TDR, the PCS field must be set in order to select a slave.

If new data is written in TDR during the transfer, it stays in it until the current transfer is completed. Then, the received data is transferred from the Shift Register to RDR, the data in TDR is loaded in the Shift Register and a new transfer starts.

The transfer of a data written in TDR in the Shift Register is indicated by the TDRE bit (Transmit Data Register Empty) in the Status Register (SR). When new data is written in TDR, this bit is cleared. The TDRE bit is used to trigger the Transmit PDC channel.

The end of transfer is indicated by the TXEMPTY flag in the SR register. If a transfer delay (DLYBCT) is greater than 0 for the last transfer, TXEMPTY is set after the completion of said delay. The master clock (MCK) can be switched off at this time.

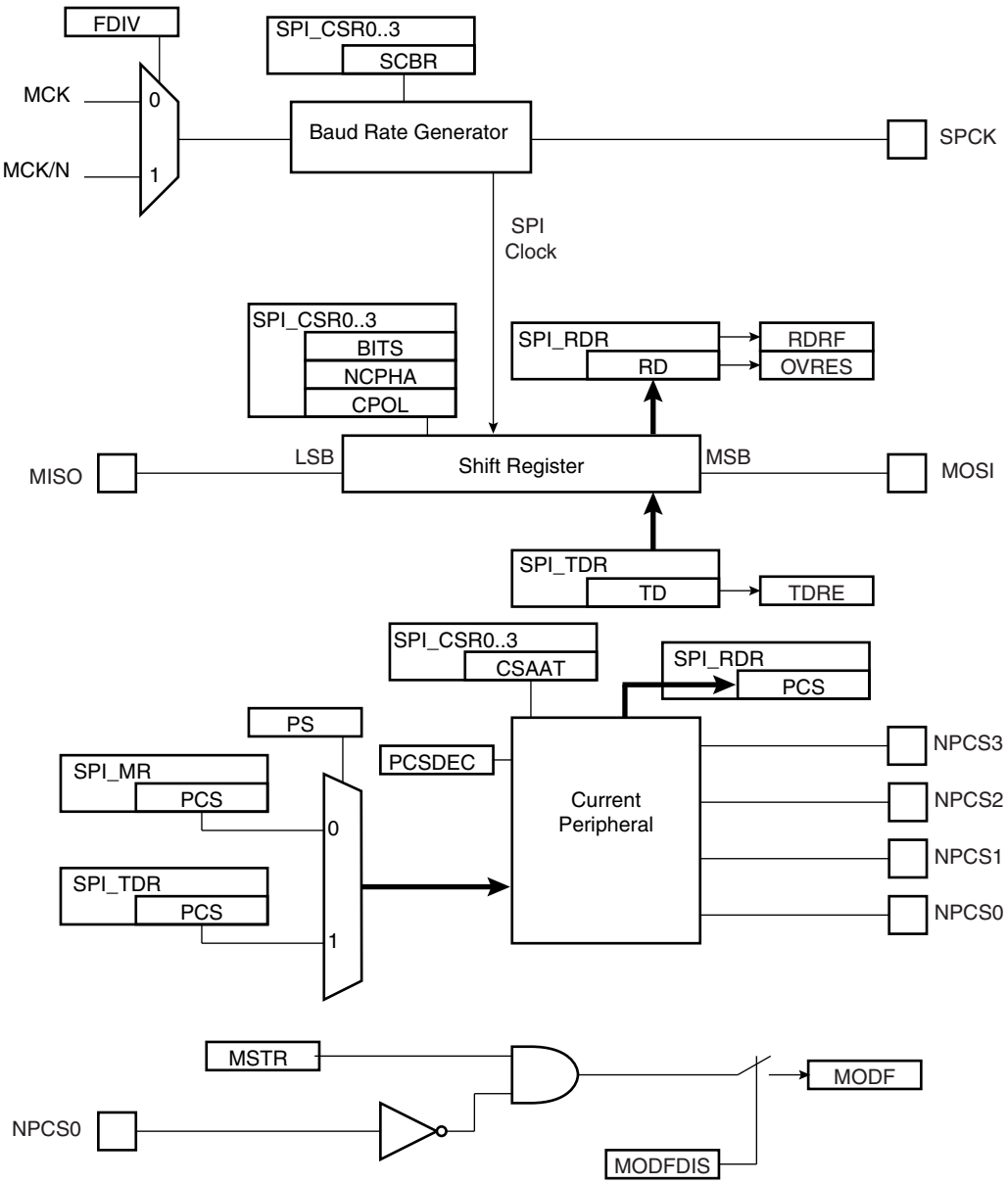
The transfer of received data from the Shift Register in RDR is indicated by the RDRF bit (Receive Data Register Full) in the Status Register (SR). When the received data is read, the RDRF bit is cleared.

If the RDR (Receive Data Register) has not been read before new data is received, the Overrun Error bit (OVRES) in SR is set. When this bit is set the SPI will continue to update RDR when data is received, overwriting the previously received data. The user has to read the status register to clear the OVRES bit.

Figure 20-5 on page 301 shows a block diagram of the SPI when operating in Master Mode. Figure 20-6 on page 302 shows a flow chart describing how transfers are handled.

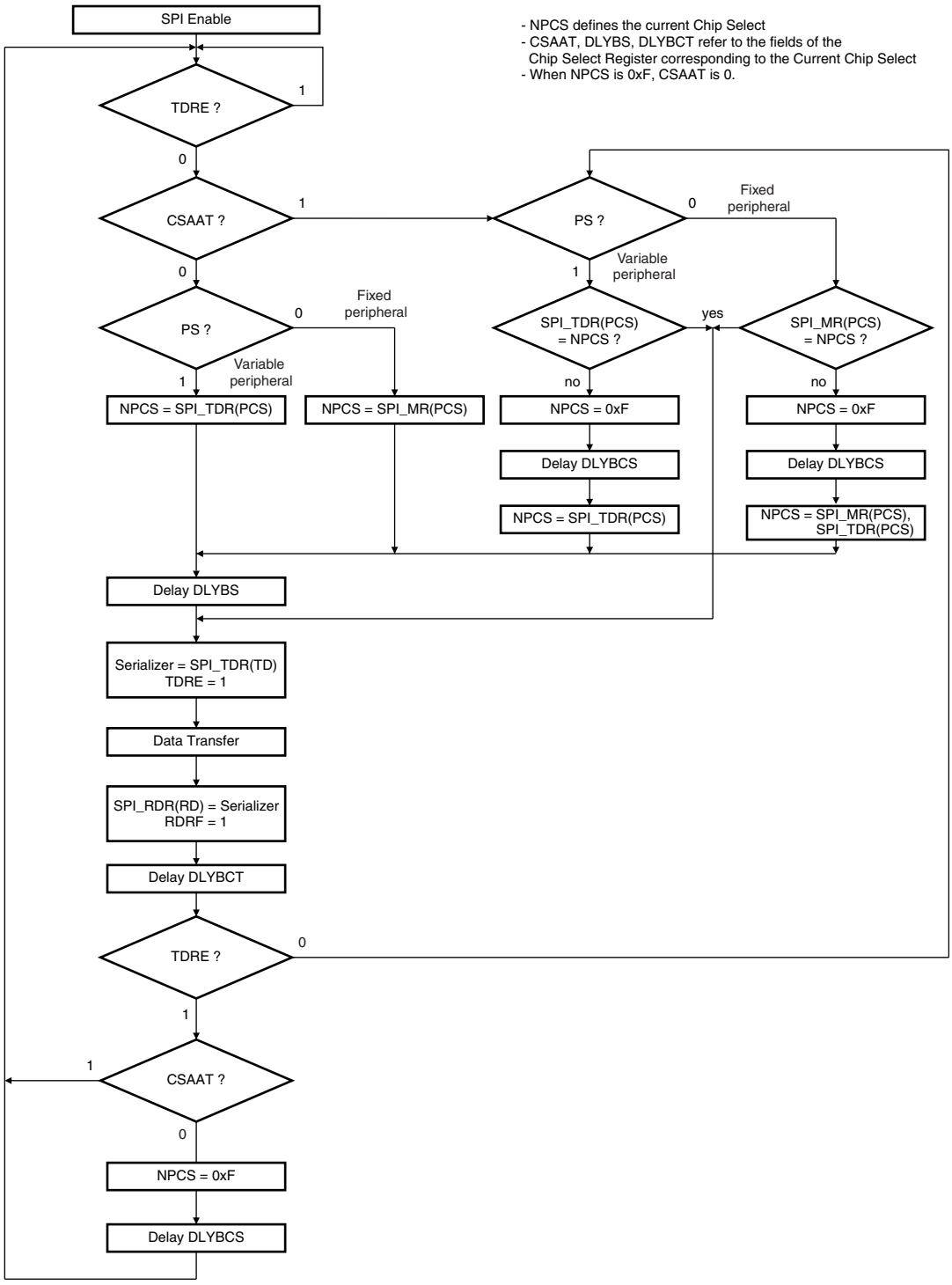
20.7.3.1 Master Mode Block Diagram

Figure 20-5. Master Mode Block Diagram



20.7.3.2 Master Mode Flow Diagram

Figure 20-6. Master Mode Flow Diagram S



20.7.3.3 Clock Generation

The SPI Baud rate clock is generated by dividing the Master Clock (MCK) or the Master Clock divided by 32, by a value between 1 and 255. The selection between Master Clock or Master Clock divided by 32 is done by the FDIV value set in the Mode Register

This allows a maximum operating baud rate at up to Master Clock and a minimum operating baud rate of MCK divided by 255*32.

Programming the SCBR field at 0 is forbidden. Triggering a transfer while SCBR is at 0 can lead to unpredictable results.

At reset, SCBR is 0 and the user has to program it at a valid value before performing the first transfer.

The divisor can be defined independently for each chip select, as it has to be programmed in the SCBR field of the Chip Select Registers. This allows the SPI to automatically adapt the baud rate for each interfaced peripheral without reprogramming.

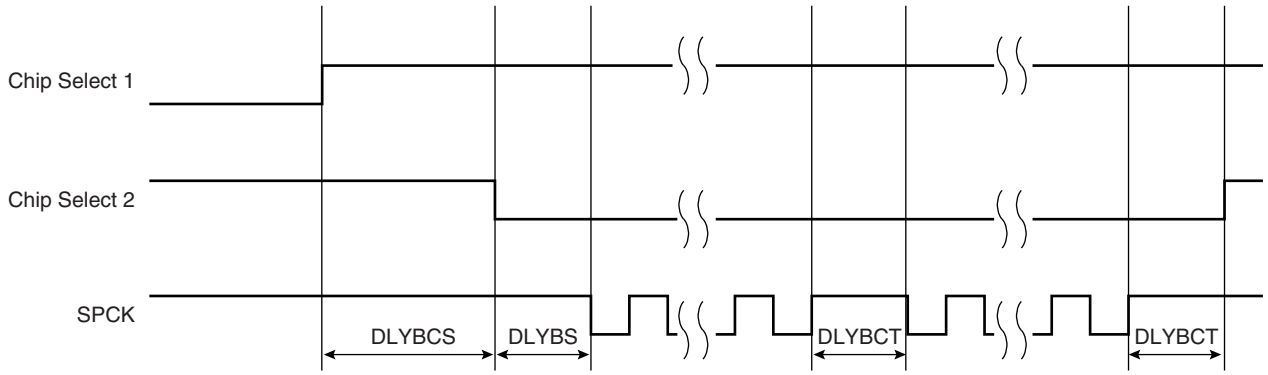
20.7.3.4 Transfer Delays

Figure 20-7 shows a chip select transfer change and consecutive transfers on the same chip select. Three delays can be programmed to modify the transfer waveforms:

- The delay between chip selects, programmable only once for all the chip selects by writing the DLYBCS field in the Mode Register. Allows insertion of a delay between release of one chip select and before assertion of a new one.
- The delay before SPCK, independently programmable for each chip select by writing the field DLYBS. Allows the start of SPCK to be delayed after the chip select has been asserted.
- The delay between consecutive transfers, independently programmable for each chip select by writing the DLYBCT field. Allows insertion of a delay between two transfers occurring on the same chip select

These delays allow the SPI to be adapted to the interfaced peripherals and their speed and bus release time.

Figure 20-7. Programmable Delays



20.7.3.5 Peripheral Selection

The serial peripherals are selected through the assertion of the NPCS0 to NPCS3 signals. By default, all the NPCS signals are high before and after each transfer.

The peripheral selection can be performed in two different ways:

- Fixed Peripheral Select: SPI exchanges data with only one peripheral
- Variable Peripheral Select: Data can be exchanged with more than one peripheral

Fixed Peripheral Select is activated by writing the PS bit to zero in MR (Mode Register). In this case, the current peripheral is defined by the PCS field in MR and the PCS field in TDR have no effect.

Variable Peripheral Select is activated by setting PS bit to one. The PCS field in TDR is used to select the current peripheral. This means that the peripheral selection can be defined for each new data.

The Fixed Peripheral Selection allows buffer transfers with a single peripheral. Using the PDC is an optimal means, as the size of the data transfer between the memory and the SPI is either 8 bits or 16 bits. However, changing the peripheral selection requires the Mode Register to be reprogrammed.

The Variable Peripheral Selection allows buffer transfers with multiple peripherals without reprogramming the Mode Register. Data written in TDR is 32 bits wide and defines the real data to be transmitted and the peripheral it is destined to. Using the PDC in this mode requires 32-bit wide buffers, with the data in the LSBs and the PCS and LASTXFER fields in the MSBs, however the SPI still controls the number of bits (8 to16) to be transferred through MISO and MOSI lines with the chip select configuration registers. This is not the optimal means in term of memory size for the buffers, but it provides a very effective means to exchange data with several peripherals without any intervention of the processor.

20.7.3.6 Peripheral Chip Select Decoding

The user can program the SPI to operate with up to 15 peripherals by decoding the four Chip Select lines, NPCS0 to NPCS3 with an external logic. This can be enabled by writing the PCSDEC bit at 1 in the Mode Register (MR).

When operating without decoding, the SPI makes sure that in any case only one chip select line is activated, i.e. driven low at a time. If two bits are defined low in a PCS field, only the lowest numbered chip select is driven low.

When operating with decoding, the SPI directly outputs the value defined by the PCS field of either the Mode Register or the Transmit Data Register (depending on PS).

As the SPI sets a default value of 0xF on the chip select lines (i.e. all chip select lines at 1) when not processing any transfer, only 15 peripherals can be decoded.

The SPI has only four Chip Select Registers, not 15. As a result, when decoding is activated, each chip select defines the characteristics of up to four peripherals. As an example, CRS0 defines the characteristics of the externally decoded peripherals 0 to 3, corresponding to the PCS values 0x0 to 0x3. Thus, the user has to make sure to connect compatible peripherals on the decoded chip select lines 0 to 3, 4 to 7, 8 to 11 and 12 to 14.

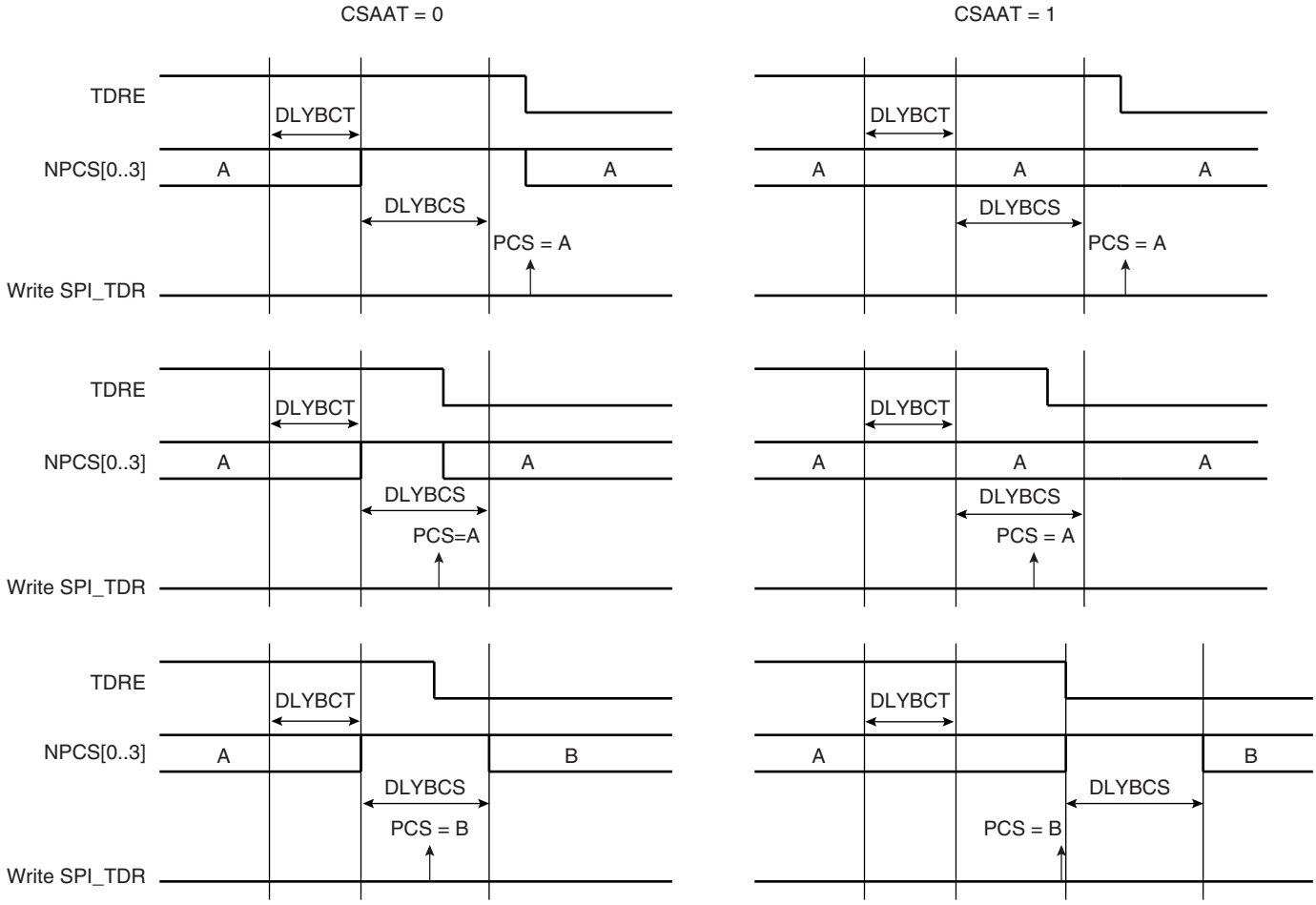
20.7.3.7 Peripheral Deselection

When operating normally, as soon as the transfer of the last data written in TDR is completed, the NPCS lines all rise. This might lead to runtime error if the processor is too long in responding to an interrupt, and thus might lead to difficulties for interfacing with some serial peripherals requiring the chip select line to remain active during a full set of transfers.

To facilitate interfacing with such devices, the Chip Select Register can be programmed with the CSAAT bit (Chip Select Active After Transfer) at 1. This allows the chip select lines to remain in their current state (low = active) until transfer to another peripheral is required.

Figure 20-8 shows different peripheral deselection cases and the effect of the CSAAT bit.

Figure 20-8. Peripheral Deselection



20.7.3.8 Mode Fault Detection

A mode fault is detected when the SPI is programmed in Master Mode and a low level is driven by an external master on the NPCS0/NSS signal. NPCS0, MOSI, MISO and SPCK must be configured in open-drain through the PIO controller, so that external pull up resistors are needed to guarantee high level.

When a mode fault is detected, the MODF bit in the SR is set until the SR is read and the SPI is automatically disabled until re-enabled by writing the SPIEN bit in the CR (Control Register) at 1.

By default, the Mode Fault detection circuitry is enabled. The user can disable Mode Fault detection by setting the MODFDIS bit in the SPI Mode Register (MR).

20.7.4 SPI Slave Mode

When operating in Slave Mode, the SPI processes data bits on the clock provided on the SPI clock pin (SPCK).

The SPI waits for NSS to go active before receiving the serial clock from an external master. When NSS falls, the clock is validated on the serializer, which processes the number of bits defined by the BITS field of the Chip Select Register 0 (CSR0). These bits are processed following a phase and a polarity defined respectively by the NCPHA and CPOL bits of the CSR0. Note that BITS, CPOL and NCPHA of the other Chip Select Registers have no effect when the SPI is programmed in Slave Mode.

The bits are shifted out on the MISO line and sampled on the MOSI line.

When all the bits are processed, the received data is transferred in the Receive Data Register and the RDRF bit rises. If RDRF is already high when the data is transferred, the Overrun bit rises and the data transfer to RDR is aborted.

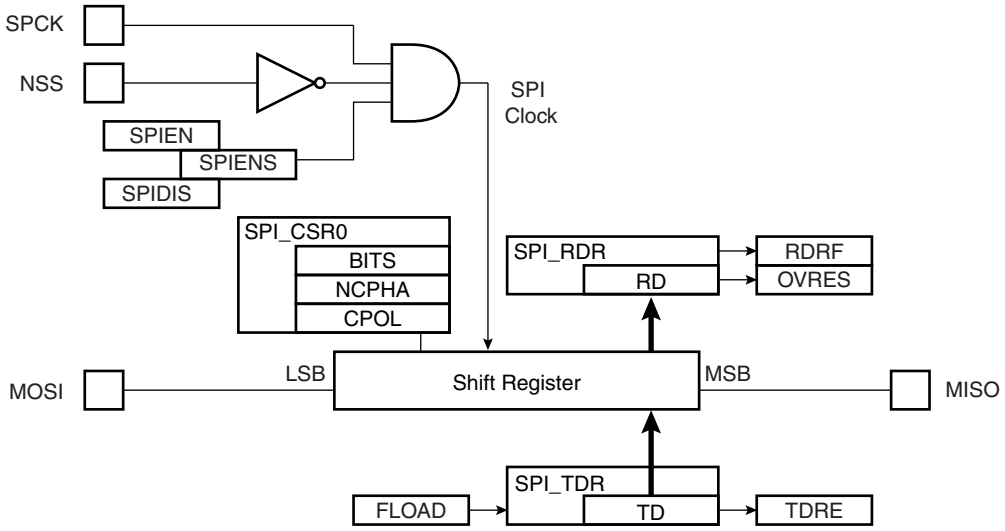
When a transfer starts, the data shifted out is the data present in the Shift Register. If no data has been written in the Transmit Data Register (TDR), the last data received is transferred. If no data has been received since the last reset, all bits are transmitted low, as the Shift Register resets at 0.

When a first data is written in TDR, it is transferred immediately in the Shift Register and the TDRE bit rises. If new data is written, it remains in TDR until a transfer occurs, i.e. NSS falls and there is a valid clock on the SPCK pin. When the transfer occurs, the last data written in TDR is transferred in the Shift Register and the TDRE bit rises. This enables frequent updates of critical variables with single transfers.

Then, a new data is loaded in the Shift Register from the Transmit Data Register. In case no character is ready to be transmitted, i.e. no character has been written in TDR since the last load from TDR to the Shift Register, the Shift Register is not modified and the last received character is retransmitted.

Figure 20-9 shows a block diagram of the SPI when operating in Slave Mode.

Figure 20-9. Slave Mode Functional Block Diagram



20.8 Serial Peripheral Interface (SPI) User Interface

Table 20-3. SPI Register Mapping

Offset	Register	Register Name	Access	Reset
0x00	Control Register	CR	Write-only	---
0x04	Mode Register	MR	Read/Write	0x0
0x08	Receive Data Register	RDR	Read-only	0x0
0x0C	Transmit Data Register	TDR	Write-only	---
0x10	Status Register	SR	Read-only	0x000000F0
0x14	Interrupt Enable Register	IER	Write-only	---
0x18	Interrupt Disable Register	IDR	Write-only	---
0x1C	Interrupt Mask Register	IMR	Read-only	0x0
0x20 - 0x2C	Reserved			
0x30	Chip Select Register 0	CSR0	Read/Write	0x0
0x34	Chip Select Register 1	CSR1	Read/Write	0x0
0x38	Chip Select Register 2	CSR2	Read/Write	0x0
0x3C	Chip Select Register 3	CSR3	Read/Write	0x0
0x004C - 0x00F8	Reserved	–	–	–
0x00FC	Version Register	VERSION	Read-only	0x- (1)
0x100 - 0x124	Reserved for the PDC			

Note: 1. Values in the Version Register vary with the version of the IP block implementation.

20.8.1 SPI Control Register

Name: CR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	LASTXFER
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	–	–	SPIDIS	SPIEN

- **SPIEN: SPI Enable**

0 = No effect.

1 = Enables the SPI to transfer and receive data.

- **SPIDIS: SPI Disable**

0 = No effect.

1 = Disables the SPI.

As soon as SPDIS is set, SPI finishes its transfer.

All pins are set in input mode and no data is received or transmitted.

If a transfer is in progress, the transfer is finished before the SPI is disabled.

If both SPIEN and SPIDIS are equal to one when the control register is written, the SPI is disabled.

- **SWRST: SPI Software Reset**

0 = No effect.

1 = Reset the SPI. A software-triggered hardware reset of the SPI interface is performed.

The SPI is in slave mode after a software reset.

PDC channels are not affected by software reset.

- **LASTXFER: Last Transfer**

0 = No effect.

1 = The current NPCS will be deasserted after the character written in TD has been transferred. When CSAAT is set, this allows to close the communication with the current serial peripheral by raising the corresponding NPCS line as soon as TD transfer has completed.

20.8.2 SPI Mode Register

Name: MR

Access Type: Read/Write

31	30	29	28	27	26	25	24
DLYBCS							
23	22	21	20	19	18	17	16
–	–	–	–	PCS			
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
LLB	–	–	MODFDIS	FDIV	PCSDEC	PS	MSTR

- **MSTR: Master/Slave Mode**

0 = SPI is in Slave mode.

1 = SPI is in Master mode.

- **PS: Peripheral Select**

0 = Fixed Peripheral Select.

1 = Variable Peripheral Select.

- **PCSDEC: Chip Select Decode**

0 = The chip selects are directly connected to a peripheral device.

1 = The four chip select lines are connected to a 4- to 16-bit decoder.

When PCSDEC equals one, up to 15 Chip Select signals can be generated with the four lines using an external 4- to 16-bit decoder. The Chip Select Registers define the characteristics of the 15 chip selects according to the following rules:

CSR0 defines peripheral chip select signals 0 to 3.

CSR1 defines peripheral chip select signals 4 to 7.

CSR2 defines peripheral chip select signals 8 to 11.

CSR3 defines peripheral chip select signals 12 to 14.

- **FDIV: Clock Selection**

0 = The SPI operates at MCK.

1 = The SPI operates at MCK/N.

- **MODFDIS: Mode Fault Detection**

0 = Mode fault detection is enabled.

1 = Mode fault detection is disabled.

- **LLB: Local Loopback Enable**

0 = Local loopback path disabled.

1 = Local loopback path enabled.

LLB controls the local loopback on the data serializer for testing in Master Mode only. MISO is internally connected to MOSI.

- **PCS: Peripheral Chip Select**

This field is only used if Fixed Peripheral Select is active (PS = 0).

If PCSDEC = 0:

PCS = xxx0	NPCS[3:0] = 1110
PCS = xx01	NPCS[3:0] = 1101
PCS = x011	NPCS[3:0] = 1011
PCS = 0111	NPCS[3:0] = 0111
PCS = 1111	forbidden (no peripheral is selected)

(x = don't care)

If PCSDEC = 1:

NPCS[3:0] output signals = PCS.

- **DLYBCS: Delay Between Chip Selects**

This field defines the delay from NPCS inactive to the activation of another NPCS. The DLYBCS time guarantees non-overlapping chip selects and solves bus contentions in case of peripherals having long data float times.

If DLYBCS is less than or equal to six, six MCK periods (or 6*N MCK periods if FDIV is set) will be inserted by default.

Otherwise, the following equation determines the delay:

If FDIV is 0:

$$\text{Delay Between Chip Selects} = \frac{DLYBCS}{MCK}$$

If FDIV is 1:

$$\text{Delay Between Chip Selects} = \frac{DLYBCS \times N}{MCK}$$

20.8.3 SPI Receive Data Register

Name: RDR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	PCS			
15	14	13	12	11	10	9	8
RD							
7	6	5	4	3	2	1	0
RD							

- **RD: Receive Data**

Data received by the SPI Interface is stored in this register right-justified. Unused bits read zero.

- **PCS: Peripheral Chip Select**

In Master Mode only, these bits indicate the value on the NPCS pins at the end of a transfer. Otherwise, these bits read zero.

20.8.4 SPI Transmit Data Register

Name: TDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	LASTXFER

23	22	21	20	19	18	17	16
–	–	–	–	PCS			

15	14	13	12	11	10	9	8
TD							

7	6	5	4	3	2	1	0
TD							

- **TD: Transmit Data**

Data to be transmitted by the SPI Interface is stored in this register. Information to be transmitted must be written to the transmit data register in a right-justified format.

- **PCS: Peripheral Chip Select**

This field is only used if Variable Peripheral Select is active (PS = 1).

If PCSDEC = 0:

PCS = xxx0 NPCS[3:0] = 1110

PCS = xx01 NPCS[3:0] = 1101

PCS = x011 NPCS[3:0] = 1011

PCS = 0111 NPCS[3:0] = 0111

PCS = 1111 forbidden (no peripheral is selected)

(x = don't care)

If PCSDEC = 1:

NPCS[3:0] output signals = PCS

- **LASTXFER: Last Transfer**

0 = No effect.

1 = The current NPCS will be deasserted after the character written in TD has been transferred. When CSAAT is set, this allows to close the communication with the current serial peripheral by raising the corresponding NPCS line as soon as TD transfer has completed.

This field is only used if Variable Peripheral Select is active (PS = 1).

20.8.5 SPI Status Register

Name: SR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	SPIENS
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
TXBUFE	RXBUFF	ENDTX	ENDRX	OVRES	MODF	TDRE	RDRF

- **RDRF: Receive Data Register Full**

0 = No data has been received since the last read of RDR

1 = Data has been received and the received data has been transferred from the serializer to RDR since the last read of RDR.

- **TDRE: Transmit Data Register Empty**

0 = Data has been written to TDR and not yet transferred to the serializer.

1 = The last data written in the Transmit Data Register has been transferred to the serializer.

TDRE equals zero when the SPI is disabled or at reset. The SPI enable command sets this bit to one.

- **MODF: Mode Fault Error**

0 = No Mode Fault has been detected since the last read of SR.

1 = A Mode Fault occurred since the last read of the SR.

- **OVRES: Overrun Error Status**

0 = No overrun has been detected since the last read of SR.

1 = An overrun has occurred since the last read of SR.

An overrun occurs when RDR is loaded at least twice from the serializer since the last read of the RDR.

- **ENDRX: End of RX buffer**

0 = The Receive Counter Register has not reached 0 since the last write in RCR or RNCR.

1 = The Receive Counter Register has reached 0 since the last write in RCR or RNCR.

- **ENDTX: End of TX buffer**

0 = The Transmit Counter Register has not reached 0 since the last write in TCR or TNCR.

1 = The Transmit Counter Register has reached 0 since the last write in TCR or TNCR.

- **RXBUFF: RX Buffer Full**

0 = RCR or RNCR has a value other than 0.

1 = Both RCR and RNCR has a value of 0.

- **TXBUFE: TX Buffer Empty**

0 = TCR or TNCR has a value other than 0.

1 = Both TCR and TNCR has a value of 0.

- **NSSR: NSS Rising**

0 = No rising edge detected on NSS pin since last read.

1 = A rising edge occurred on NSS pin since last read.

- **TXEMPTY: Transmission Registers Empty**

0 = As soon as data is written in TDR.

1 = TDR and internal shifter are empty. If a transfer delay has been defined, TXEMPTY is set after the completion of such delay.

- **SPIENS: SPI Enable Status**

0 = SPI is disabled.

1 = SPI is enabled.

20.8.6 SPI Interrupt Enable Register

Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
TXBUFE	RXBUFF	ENDTX	ENDRX	OVRES	MODF	TDRE	RDRF

- **RDRF: Receive Data Register Full Interrupt Enable**
- **TDRE: SPI Transmit Data Register Empty Interrupt Enable**
- **MODF: Mode Fault Error Interrupt Enable**
- **OVRES: Overrun Error Interrupt Enable**
- **ENDRX: End of Receive Buffer Interrupt Enable**
- **ENDTX: End of Transmit Buffer Interrupt Enable**
- **RXBUFF: Receive Buffer Full Interrupt Enable**
- **TXBUFE: Transmit Buffer Empty Interrupt Enable**
- **TXEMPTY: Transmission Registers Empty Enable**
- **NSSR: NSS Rising Interrupt Enable**

0 = No effect.

1 = Enables the corresponding interrupt.

20.8.7 SPI Interrupt Disable Register

Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
TXBUFE	RXBUFF	ENDTX	ENDRX	OVRES	MODF	TDRE	RDRF

- **RDRF: Receive Data Register Full Interrupt Disable**
- **TDRE: SPI Transmit Data Register Empty Interrupt Disable**
- **MODF: Mode Fault Error Interrupt Disable**
- **OVRES: Overrun Error Interrupt Disable**
- **ENDRX: End of Receive Buffer Interrupt Disable**
- **ENDTX: End of Transmit Buffer Interrupt Disable**
- **RXBUFF: Receive Buffer Full Interrupt Disable**
- **TXBUFE: Transmit Buffer Empty Interrupt Disable**
- **TXEMPTY: Transmission Registers Empty Disable**
- **NSSR: NSS Rising Interrupt Disable**

0 = No effect.

1 = Disables the corresponding interrupt.

20.8.8 SPI Interrupt Mask Register

Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
TXBUFE	RXBUFF	ENDTX	ENDRX	OVRES	MODF	TDRE	RDRF

- **RDRF: Receive Data Register Full Interrupt Mask**
- **TDRE: SPI Transmit Data Register Empty Interrupt Mask**
- **MODF: Mode Fault Error Interrupt Mask**
- **OVRES: Overrun Error Interrupt Mask**
- **ENDRX: End of Receive Buffer Interrupt Mask**
- **ENDTX: End of Transmit Buffer Interrupt Mask**
- **RXBUFF: Receive Buffer Full Interrupt Mask**
- **TXBUFE: Transmit Buffer Empty Interrupt Mask**
- **TXEMPTY: Transmission Registers Empty Mask**
- **NSSR: NSS Rising Interrupt Mask**

0 = The corresponding interrupt is not enabled.

1 = The corresponding interrupt is enabled.

20.8.9 SPI Chip Select Register

Name: CSR0... CSR3

Access Type: Read/Write

31	30	29	28	27	26	25	24
DLYBCT							
23	22	21	20	19	18	17	16
DLYBS							
15	14	13	12	11	10	9	8
SCBR							
7	6	5	4	3	2	1	0
BITS				CSAAT	–	NCPHA	CPOL

- **CPOL: Clock Polarity**

0 = The inactive state value of SPCK is logic level zero.

1 = The inactive state value of SPCK is logic level one.

CPOL is used to determine the inactive state value of the serial clock (SPCK). It is used with NCPHA to produce the required clock/data relationship between master and slave devices.

- **NCPHA: Clock Phase**

0 = Data is changed on the leading edge of SPCK and captured on the following edge of SPCK.

1 = Data is captured on the leading edge of SPCK and changed on the following edge of SPCK.

NCPHA determines which edge of SPCK causes data to change and which edge causes data to be captured. NCPHA is used with CPOL to produce the required clock/data relationship between master and slave devices.

- **CSAAT: Chip Select Active After Transfer**

0 = The Peripheral Chip Select Line rises as soon as the last transfer is achieved.

1 = The Peripheral Chip Select does not rise after the last transfer is achieved. It remains active until a new transfer is requested on a different chip select.

- **BITS: Bits Per Transfer**

The BITS field determines the number of data bits transferred. Reserved values should not be used, see Table 20-4 on page 320.

Table 20-4. BITS, Bits Per Transfer

BITS	Bits Per Transfer
0000	8
0001	9
0010	10
0011	11
0100	12
0101	13
0110	14
0111	15
1000	16
1001	Reserved
1010	Reserved
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

- **SCBR: Serial Clock Baud Rate**

In Master Mode, the SPI Interface uses a modulus counter to derive the SPCK baud rate from the Master Clock MCK. The Baud rate is selected by writing a value from 1 to 255 in the SCBR field. The following equations determine the SPCK baud rate:

If FDIV is 0:

$$\text{SPCK Baudrate} = \frac{MCK}{SCBR}$$

If FDIV is 1:

$$\text{SPCK Baudrate} = \frac{MCK}{(N \times SCBR)}$$

Note: N = 32

Programming the SCBR field at 0 is forbidden. Triggering a transfer while SCBR is at 0 can lead to unpredictable results.

At reset, SCBR is 0 and the user has to program it at a valid value before performing the first transfer.

- **DLYBS: Delay Before SPCK**

This field defines the delay from NPCS valid to the first valid SPCK transition.

When DLYBS equals zero, the NPCS valid to SPCK transition is 1/2 the SPCK clock period.

Otherwise, the following equations determine the delay:

If FDIV is 0:

$$\text{Delay Before SPCK} = \frac{DLYBS}{MCK}$$

If FDIV is 1:

$$\text{Delay Before SPCK} = \frac{N \times DLYBS}{MCK}$$

Note: N = 32

- **DLYBCT: Delay Between Consecutive Transfers**

This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

When DLYBCT equals zero, no delay between consecutive transfers is inserted and the clock keeps its duty cycle over the character transfers.

Otherwise, the following equation determines the delay:

If FDIV is 0:

$$\text{Delay Between Consecutive Transfers} = \frac{32 \times DLYBCT}{MCK} + \frac{SCBR}{2MCK}$$

If FDIV is 1:

$$\text{Delay Between Consecutive Transfers} = \frac{32 \times N \times DLYBCT}{MCK} + \frac{N \times SCBR}{2MCK}$$

Note: N = 32

21. Two-wire Interface (TWI)

Rev: 1.8.0.1

21.1 Features

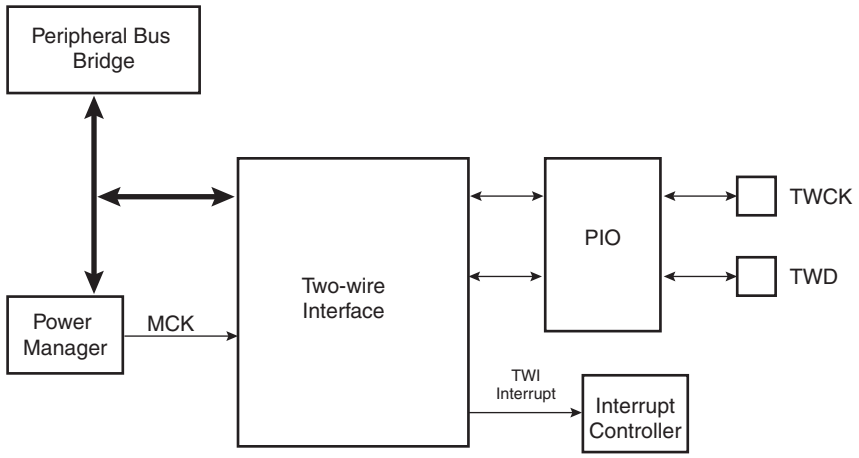
- **Compatible with Philips' I²C protocol**
- **One, Two or Three Bytes for Slave Address**
- **Sequential Read/Write Operations**

21.2 Description

The Two-wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format. It can be used with any Atmel two-wire bus Serial EEPROM. The TWI is programmable as a master with sequential or single-byte access. A configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies.

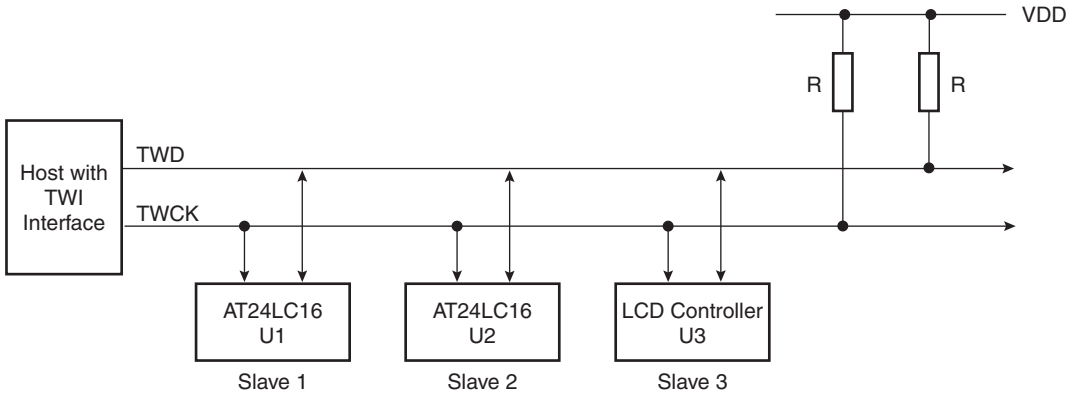
21.3 Block Diagram

Figure 21-1. Block Diagram



21.4 Application Block Diagram

Figure 21-2. Application Block Diagram



21.4.1 I/O Lines Description

Table 21-1. I/O Lines Description

Pin Name	Pin Description	Type
TWD	Two-wire Serial Data	Input/Output
TWCK	Two-wire Serial Clock	Input/Output

21.5 Product Dependencies

21.5.1 I/O Lines

Both TWD and TWCK are bi-directional lines, connected to a positive supply voltage via a current source or pull-up resistor (see Figure 21-2 on page 322). When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

TWD and TWCK pins may be multiplexed with PIO lines. To enable the TWI, the programmer must program the PIO controller to dedicate TWD and TWCK as peripheral lines.

21.5.2 Power Management

The TWI clock is generated by the power manager. Before using the TWI, the programmer must ensure that the TWI clock is enabled in the power manager.

In the TWI description, Master Clock (MCK) is the clock of the peripheral bus to which the TWI is connected.

21.5.3 Interrupt

The TWI interface has an interrupt line connected to the interrupt controller. In order to handle interrupts, the interrupt controller must be programmed before configuring the TWI.

21.6 Functional Description

21.6.1 Transfer format

The data put on the TWD line must be 8 bits long. Data is transferred MSB first; each byte must be followed by an acknowledgement. The number of bytes per transfer is unlimited (see Figure 21-4 on page 324).

Each transfer begins with a START condition and terminates with a STOP condition (see Figure 21-3 on page 324).

- A high-to-low transition on the TWD line while TWCK is high defines the START condition.
- A low-to-high transition on the TWD line while TWCK is high defines a STOP condition.

Figure 21-3. START and STOP Conditions

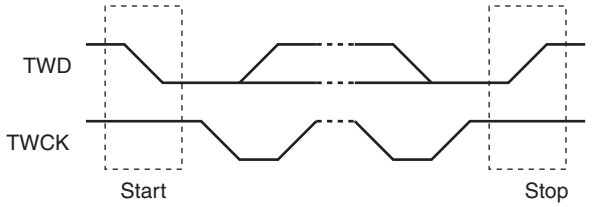
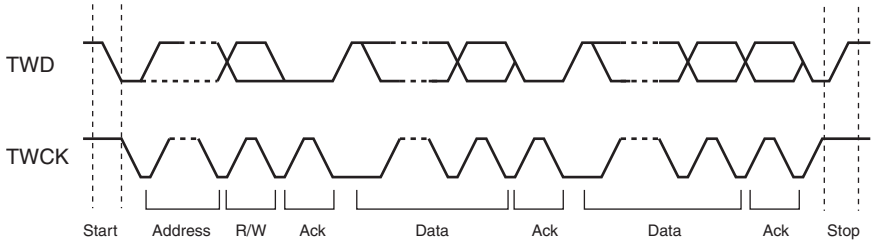


Figure 21-4. Transfer Format



21.6.2 Modes of Operation

The TWI has two modes of operation:

- Master transmitter mode
- Master receiver mode

The TWI Control Register (CR) allows configuration of the interface in Master Mode. In this mode, it generates the clock according to the value programmed in the Clock Waveform Generator Register (CWGR). This register defines the TWCK signal completely, enabling the interface to be adapted to a wide range of clocks.

21.6.3 Transmitting Data

After the master initiates a Start condition, it sends a 7-bit slave address, configured in the Master Mode register (DADR in MMR), to notify the slave device. The bit following the slave address indicates the transfer direction (write or read). If this bit is 0, it indicates a write operation (transmit operation). If the bit is 1, it indicates a request for data read (receive operation).

The TWI transfers require the slave to acknowledge each received byte. During the acknowledge clock pulse, the master releases the data line (HIGH), enabling the slave to pull it down in order to generate the acknowledge. The master polls the data line during this clock pulse and sets the **NAK** bit in the status register if the slave does not acknowledge the byte. As with the

other status bits, an interrupt can be generated if enabled in the interrupt enable register (IER). After writing in the transmit-holding register (THR), setting the START bit in the control register starts the transmission. The data is shifted in the internal shifter and when an acknowledge is detected, the TXRDY bit is set until a new write in the THR (see Figure 21-6 below). The master generates a stop condition to end the transfer.

The read sequence begins by setting the START bit. When the RXRDY bit is set in the status register, a character has been received in the receive-holding register (RHR). The RXRDY bit is reset when reading the RHR.

The TWI interface performs various transfer formats (7-bit slave address, 10-bit slave address). The three internal address bytes are configurable through the Master Mode register (MMR). If the slave device supports only a 7-bit address, **IADRSZ** must be set to 0. For a slave address higher than 7 bits, the user must configure the address size **(IADRSZ**) and set the other slave address bits in the internal address register (IADR).

Figure 21-5. Master Write with One, Two or Three Bytes Internal Address and One Data Byte

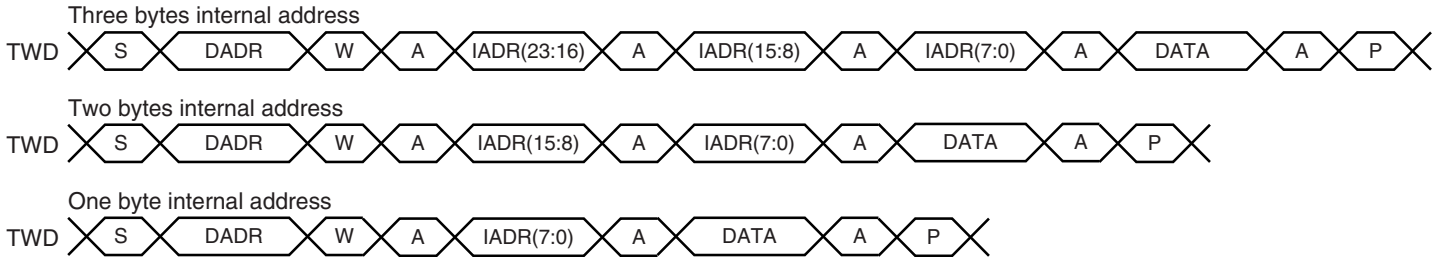


Figure 21-6. Master Write with One Byte Internal Address and Multiple Data Bytes

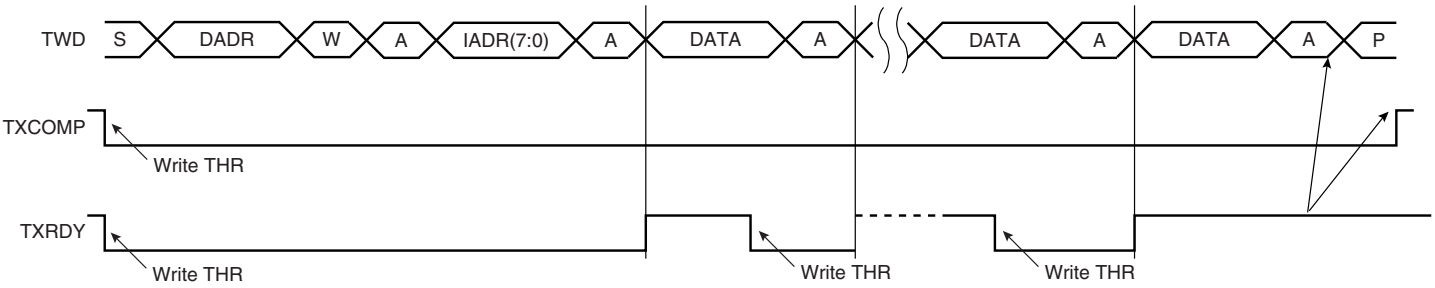


Figure 21-7. Master Read with One, Two or Three Bytes Internal Address and One Data Byte

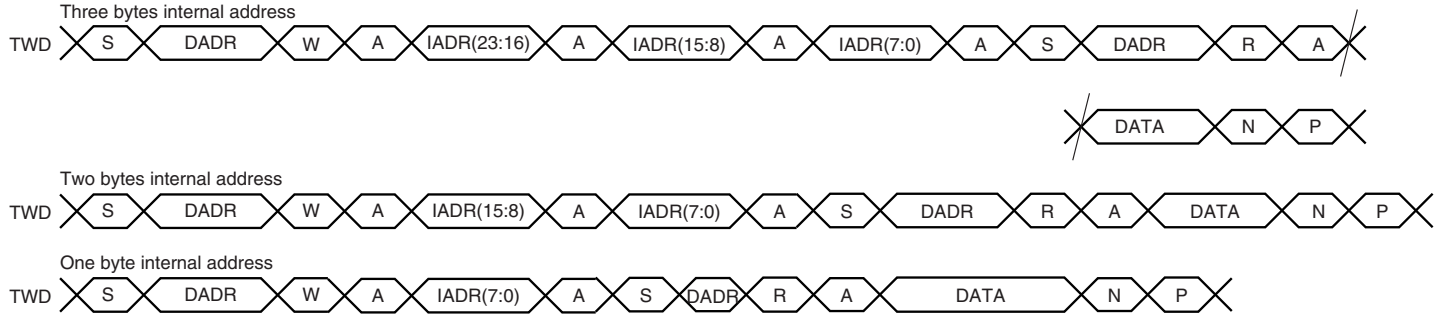
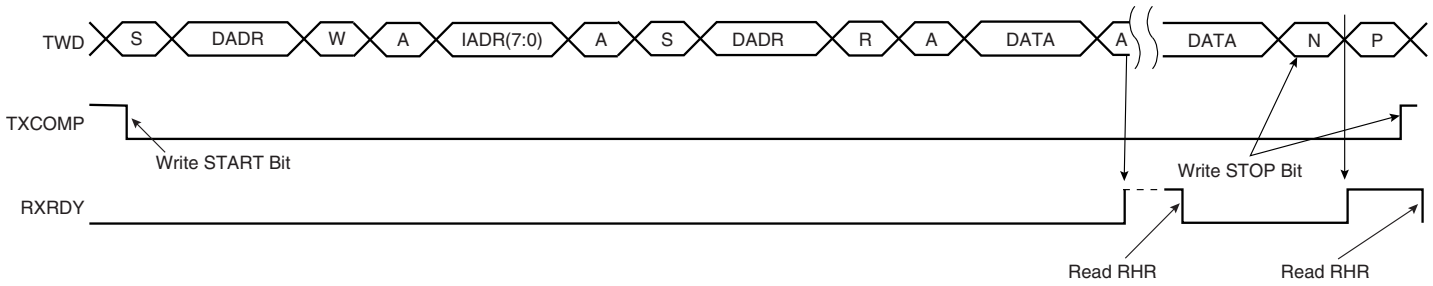


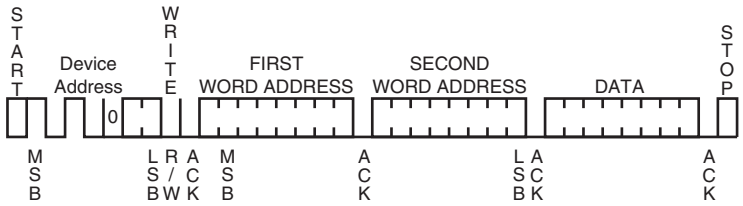
Figure 21-8. Master Read with One Byte Internal Address and Multiple Data Bytes



- S = Start
- P = Stop
- W = Write
- R = Read
- A = Acknowledge
- N = Not Acknowledge
- DADR= Device Address
- IADR = Internal Address

Figure 21-9 below shows a byte write to an Atmel AT24LC512 EEPROM. This demonstrates the use of internal addresses to access the device.

Figure 21-9. Internal Address Usage



21.6.4 Read/Write Flowcharts

The following flowcharts shown in Figure 21-10 on page 327 and in Figure 21-11 on page 328 give examples for read and write operations in Master Mode. A polling or interrupt method can be used to check the status bits. The interrupt method requires that the interrupt enable register (IER) be configured first.

Figure 21-10. TWI Write in Master Mode

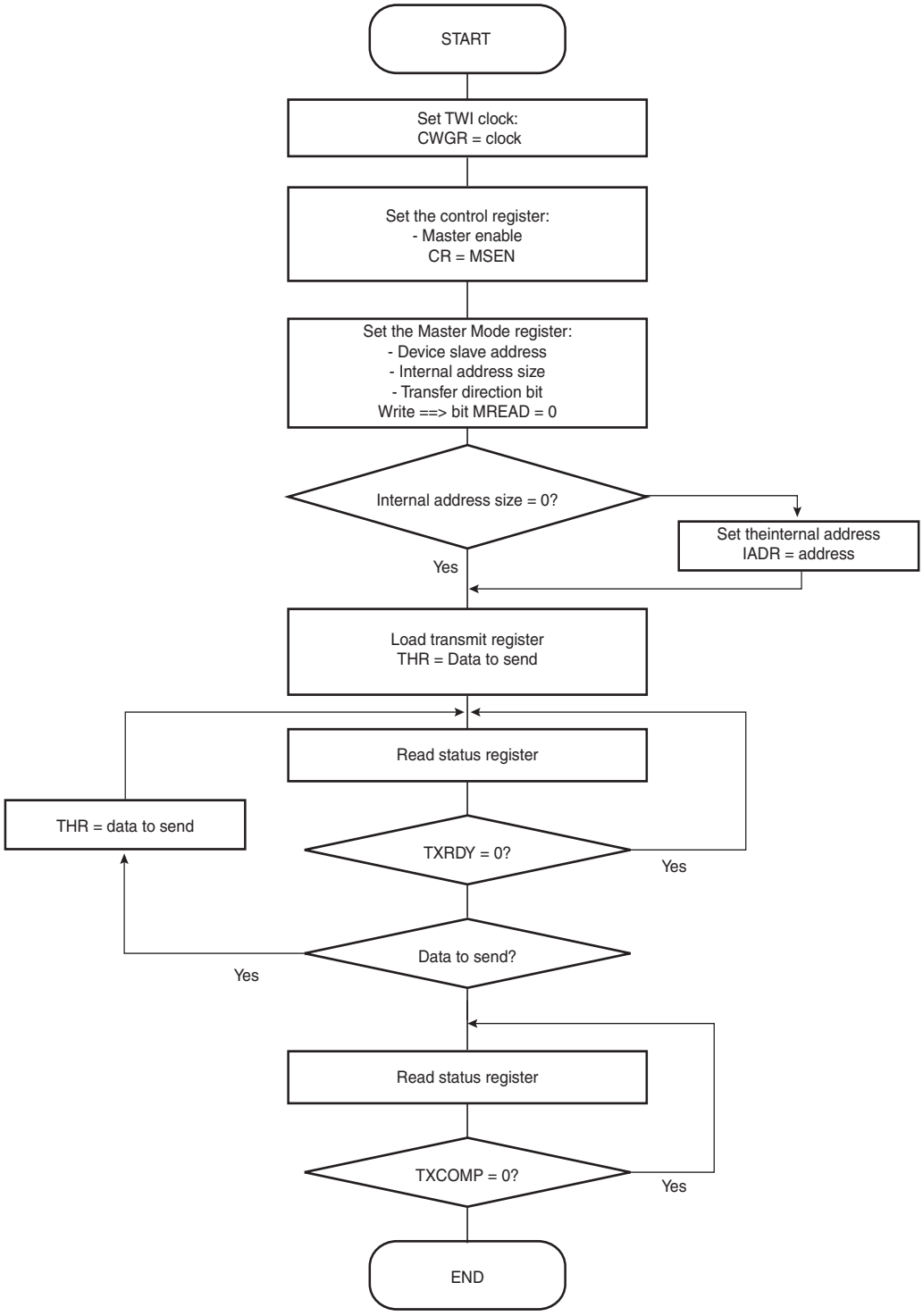
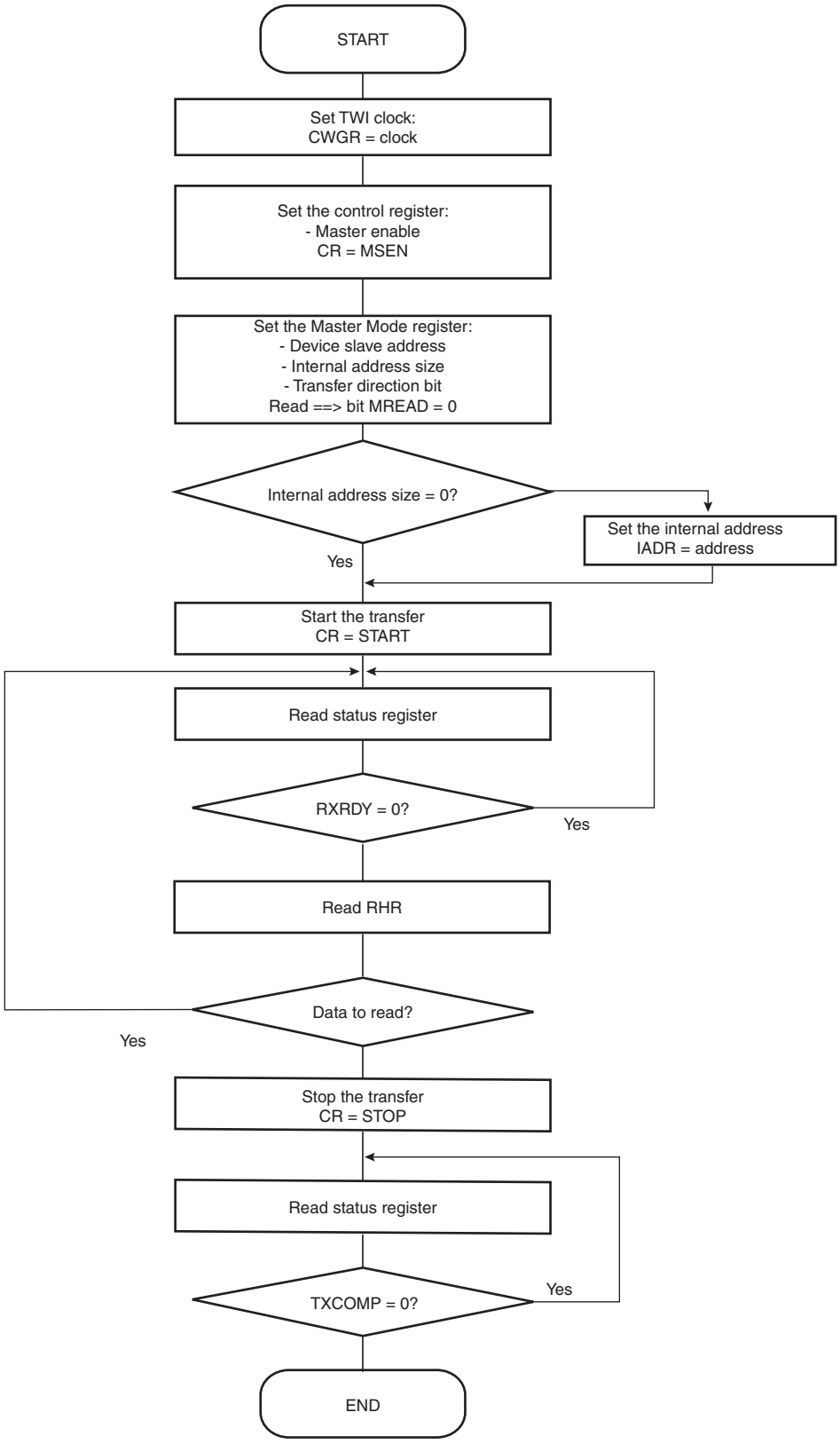


Figure 21-11. TWI Read in Master Mode



21.7 TWI User Interface

21.7.1 Register Mapping

Table 21-2. Two-wire Interface (TWI) User Interface

Offset	Register	Name	Access	Reset Value
0x0000	Control Register	CR	Write-only	N/A
0x0004	Master Mode Register	MMR	Read/Write	0x0000
0x0008	Reserved	-	-	-
0x000C	Internal Address Register	IADR	Read/Write	0x0000
0x0010	Clock Waveform Generator Register	CWGR	Read/Write	0x0000
0x0020	Status Register	SR	Read-only	0x0008
0x0024	Interrupt Enable Register	IER	Write-only	N/A
0x0028	Interrupt Disable Register	IDR	Write-only	N/A
0x002C	Interrupt Mask Register	IMR	Read-only	0x0000
0x0030	Receive Holding Register	RHR	Read-only	0x0000
0x0034	Transmit Holding Register	THR	Read/Write	0x0000

21.7.2 TWI Control Register

Register Name: CR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	MSDIS	MSEN	STOP	START

- **START: Send a START Condition**

0 = No effect.

1 = A frame beginning with a START bit is transmitted according to the settings in the mode register.

This action is necessary when the TWI peripheral wants to read data from a slave. When configured in Master Mode with a write operation, a frame is sent with the mode register as soon as the user writes a character in the holding register.

- **STOP: Send a STOP Condition**

0 = No effect.

1 = STOP Condition is sent just after completing the current byte transmission in master read or write mode.

In single data byte master read or write, the START and STOP must both be set.

In multiple data bytes master read or write, the STOP must be set before ACK/NACK bit transmission.

In master read mode, if a NACK bit is received, the STOP is automatically performed.

In multiple data write operation, when both THR and shift register are empty, a STOP condition is automatically sent.

- **MSEN: TWI Master Transfer Enabled**

0 = No effect.

1 = If MSDIS = 0, the master data transfer is enabled.

- **MSDIS: TWI Master Transfer Disabled**

0 = No effect.

1 = The master data transfer is disabled, all pending data is transmitted. The shifter and holding characters (if they contain data) are transmitted in case of write operation. In read operation, the character being transferred must be completely received before disabling.

- **SWRST: Software Reset**

0 = No effect.

1 = Equivalent to a system reset.

21.7.3 TWI Master Mode Register

Register Name: MMR

Address Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	DADR						
15	14	13	12	11	10	9	8
–	–	–	MREAD	–	–	IADRSZ	
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

- **IADRSZ: Internal Device Address Size**

IADRSZ[9:8]		
0	0	No internal device address (Byte command protocol)
0	1	One-byte internal device address
1	0	Two-byte internal device address
1	1	Three-byte internal device address

- **MREAD: Master Read Direction**

0 = Master write direction.

1 = Master read direction.

- **DADR: Device Address**

The device address is used in Master Mode to access slave devices in read or write mode.

21.7.4 TWI Internal Address Register

Register Name: IADR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
IADR							
15	14	13	12	11	10	9	8
IADR							
7	6	5	4	3	2	1	0
IADR							

- **IADR: Internal Address**

0, 1, 2 or 3 bytes depending on IADRSZ.

– Low significant byte address in 10-bit mode addresses.

21.7.5 TWI Clock Waveform Generator Register

Register Name: CWGR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	CKDIV		
15	14	13	12	11	10	9	8
CHDIV							
7	6	5	4	3	2	1	0
CLDIV							

- **CLDIV: Clock Low Divider**

The SCL low period is defined as follows:

$$T_{low} = ((\text{CLDIV} \times 2^{\text{CKDIV}}) + 3) \times T_{MCK}$$

- **CHDIV: Clock High Divider**

The SCL high period is defined as follows:

$$T_{high} = ((\text{CHDIV} \times 2^{\text{CKDIV}}) + 3) \times T_{MCK}$$

- **CKDIV: Clock Divider**

The CKDIV is used to increase both SCL high and low periods.

21.7.6 TWI Status Register

Register Name: SR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	NACK
7	6	5	4	3	2	1	0
–	–	–	–	–	TXRDY	RXRDY	TXCOMP

- **TXCOMP: Transmission Completed**

0 = In master, during the length of the current frame. In slave, from START received to STOP received.

1 = When both holding and shift registers are empty and STOP condition has been sent (in Master), or when MSEN is set (enable TWI).

- **RXRDY: Receive Holding Register Ready**

0 = No character has been received since the last RHR read operation.

1 = A byte has been received in theRHR since the last read.

- **TXRDY: Transmit Holding Register Ready**

0 = The transmit holding register has not been transferred into shift register. Set to 0 when writing into THR register.

1 = As soon as data byte is transferred from THR to internal shifter or if a NACK error is detected, TXRDY is set at the same time as TXCOMP and NACK. TXRDY is also set when MSEN is set (enable TWI).

- **NACK: Not Acknowledged**

0 = Each data byte has been correctly received by the far-end side TWI slave component.

1 = A data byte has not been acknowledged by the slave component. Set at the same time as TXCOMP. Reset after read.

21.7.7 TWI Interrupt Enable Register

Register Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	NACK
7	6	5	4	3	2	1	0
–	–	–	–	–	TXRDY	RXRDY	TXCOMP

- **TXCOMP: Transmission Completed**
- **RXRDY: Receive Holding Register Ready**
- **TXRDY: Transmit Holding Register Ready**
- **NACK: Not Acknowledge**

0 = No effect.

1 = Enables the corresponding interrupt.

21.7.8 TWI Interrupt Disable Register

Register Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	NACK
7	6	5	4	3	2	1	0
–	–	–	–	–	TXRDY	RXRDY	TXCOMP

- **TXCOMP: Transmission Completed**
- **RXRDY: Receive Holding Register Ready**
- **TXRDY: Transmit Holding Register Ready**
- **NACK: Not Acknowledge**

0 = No effect.

1 = Disables the corresponding interrupt.

21.7.9 TWI Interrupt Mask Register

Register Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	NACK
7	6	5	4	3	2	1	0
–	–	–	–	–	TXRDY	RXRDY	TXCOMP

- **TXCOMP: Transmission Completed**
- **RXRDY: Receive Holding Register Ready**
- **TXRDY: Transmit Holding Register Ready**
- **NACK: Not Acknowledge**

0 = The corresponding interrupt is disabled.

1 = The corresponding interrupt is enabled.

21.7.10 TWI Receive Holding Register

Register Name: RHR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RXDATA							

- **RXDATA: Master or Slave Receive Holding Data**

21.7.11 TWI Transmit Holding Register

Register Name: THR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
TXDATA							

- **TXDATA: Master or Slave Transmit Holding Data**

22. PS/2 Module (PSIF)

Rev: 1.0.0.2

22.1 Features

- **PS/2 Host**
- **Receive and transmit capability**
- **Parity generation and error detection**
- **Overrun error detection**

22.2 Description

The PS/2 module provides host functionality allowing the MCU to interface PS/2 devices such as keyboard and mice. The module is capable of both host-to-device and device-to-host communication.

22.3 Product Dependencies

22.3.1 I/O Lines

The PS/2 may be multiplexed with PIO lines. The programmer must first program the PIO controller to give control of the pins to the PS/2 module.

22.3.2 Power Management

The clock for the PS/2 module is generated by the power manager. The programmer must ensure that the PS/2 clock is enabled in the power manager before using the PS/2 module.

22.3.3 Interrupt

The PS/2 module has an interrupt line connected to the interrupt controller. Handling the PS/2 interrupt requires programming the interrupt controller before configuring the PS/2 module.

22.4 The PS/2 Protocol

The PS/2 protocol is a bidirectional synchronous serial communication protocol. It connects a single master - referred to as the ‘host’ - to a single slave - referred to as the ‘device’. Communication is done through two lines called ‘data’ and ‘clock’. Both of these must be open-drain or open-collector with a pullup resistor to perform a wired-AND function. When the bus is idle, both lines are high.

The device always generates the clock signal, but the host may pull the clock low to inhibit transfers. The clock frequency is in the range 10-16.7 kHz. Both the host and the slave may initiate a transfer, but the host has ultimate control of the bus.

Data are transmitted one byte at a time in a frame consisting of 11-12 bits. The transfer format is described in detail below.

22.4.1 Device to host communication

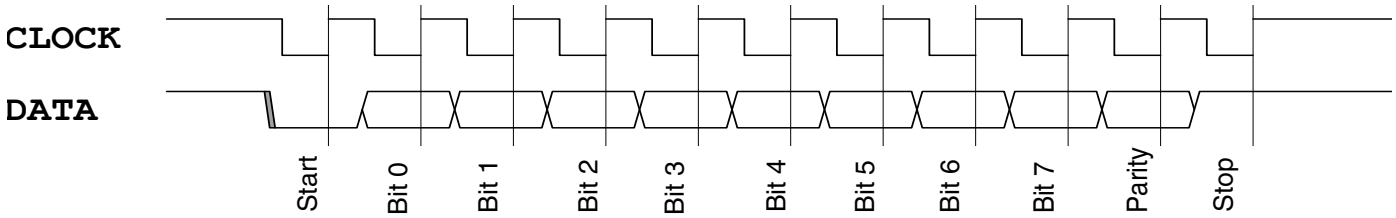
The device can only initiate a transfer when the bus is idle. If the host at any time pulls the clock low, the device must stop transferring data and prepare to receive data from the host.

The device transmits data using a 11-bit frame. The device writes a bit on the data line when the clock is high, and the host reads the bit when the clock is low.

The format of the frame is:

- 1 start bit - always 0.
- 8 data bits, least significant bit first.
- 1 parity bit - odd parity.
- 1 stop bit - always 1.

Figure 22-1. Device to host transfer



22.4.2 Host to device communication

Because the device always generates the clock, host to device communication is done differently than device to host communication.

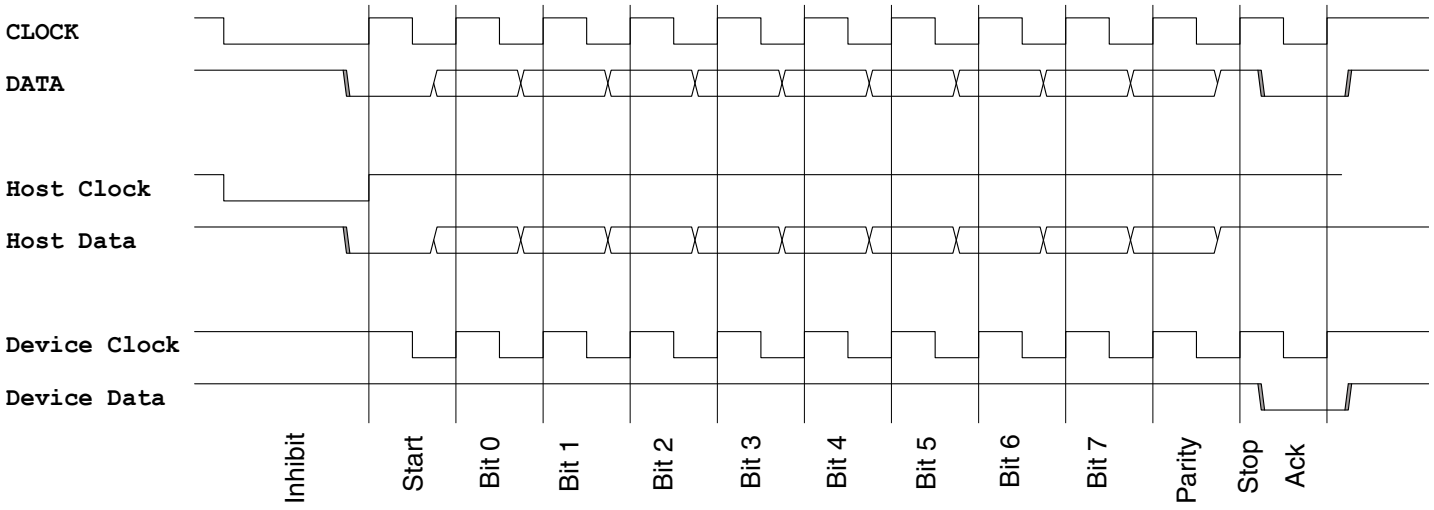
- The host starts by inhibiting communication by pulling clock low for a minimum of 100 microseconds.
- Then applies a “request-to-send” by releasing clock and pulling data low.

The device must check for this state at least every 10 milliseconds. Once it detects a request-to-send, it must start generating the clock and receive one frame of data. The host writes a data bit when the clock is low, and the device reads the bit when the clock is high.

The format of the frame is:

- 1 start bit - always 0.
- 8 data bits - least significant bit first.
- 1 parity bit - odd parity
- 1 stop bit - always one.
- 1 acknowledge bit - the device acknowledges by pulling data low.

Figure 22-2. Host to device transfer



22.5 Functional Description

22.5.1 Prescaler

For all data transfers on the PS/2 bus, the device is responsible for generating the clock and thus controlling the timing of the communications. When a host wants to initiate a transfer however, it needs to pull the clock line low for a given time (minimum 100µs). A clock prescaler controls the timing of the transfer request pulse.

Before initiating host to device transfers, the programmer must write PSR (Prescale Register). This value determines the length of the “transfer request” pulse and is found by:

```
PRSCV = Pulse length * PS/2 module frequency
```

According to the PS/2 specifications, the pulse length should be at least 100µs. The PS/2 module frequency is the frequency of the peripheral bus to which the module is connected.

22.5.2 Receiving data

The receiver is enabled by writing the RXEN bit in CR (Control Register) to ‘1’. When enabled, the receiver will continuously receive data transmitted by the device. The data is stored in RHR (Receive Holding Register). When a byte has been received, the RXRDY bit in SR (Status Register) is set.

For each received byte, the parity is calculated. If it doesn’t match the parity bit received from the device, the PARITY bit in SR is set. The received byte should then be discarded.

If a received byte in RHR is not read before a new byte has been received, the overrun bit - OVRUN in SR is set. The new data is stored in RHR overwriting the previously received byte.

22.5.3 Transmitting data

The transmitter is enabled by writing the TXEN bit in CR to ‘1’. When enabled, a data transfer to the device will be started by writing the transmit data to THR (Transmit Holding Register). Any ongoing transfer from the device will be aborted.

When the data written to THR has been transmitted to the device, the TXRDY bit in SR will be set and a new value can be loaded into THR.

At the end of the transfer, the device should acknowledge the transfer by pulling the data line low for one cycle. If an acknowledge is not detected, the NACK bit in SR will be set.

If the device fails to acknowledge the frame, the NACK bit in SR will be set. The software is responsible for any retries.

All transfers from host to device are started by the host pulling the clock line low for at least 100µs. The programmer must ensure that the prescaler is programmed to generate correct pulse length.

22.5.4 Interrupts

The PS/2 module can be configured to signal an interrupt when one of the bits in SR is set. The interrupt is enabled by writing to IER (Interrupt Enable Register) and disabled by writing to IDR (Interrupt Disable Register). The current setting of an interrupt line can be seen by reading IMR (Interrupt Mask Register).

22.6 User Interface

Offset	Register	Register Name	Access	Reset
0x000	PS/2 Control Register 0	CR0	Write-only	-
0x004	PS/2 Receive Holding Register 0	RHR0	Read-only	0x0
0x008	PS/2 Transmit Holding Register 0	THR0	Write-only	-
0x00C	RESERVED	-	-	-
0x010	PS/2 Status Register 0	SR0	Read-only	0x0
0x014	PS/2 Interrupt Enable Register 0	IER0	Write-only	-
0x018	PS/2 Interrupt Disable Register 0	IDR0	Write-only	-
0x01C	PS/2 Interrupt Mask Register 0	IMR0	Read-only	0x0
0x020	RESERVED	-	-	-
0x024	PS/2 Prescale Register 0	PSR0	Read/Write	0x0
0x100	PS/2 Control Register 1	CR1	Write-only	-
0x104	PS/2 Receive Holding Register 1	RHR1	Read-only	0x0
0x108	PS/2 Transmit Holding Register 1	THR1	Write-only	-
0x10C	RESERVED	-	-	-
0x110	PS/2 Status Register 1	SR1	Read-only	0x0
0x114	PS/2 Interrupt Enable Register 1	IER1	Write-only	-
0x118	PS/2 Interrupt Disable Register 1	IDR1	Write-only	-
0x11C	PS/2 Interrupt Mask Register 1	IMR1	Read-only	0x0
0x120	RESERVED	-	-	-
0x124	PS/2 Prescale Register 1	PSR1	Read/Write	0x0

22.6.1 PS/2 Control Register

Name: CR0, CR1

Access Type: Write-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
SWRST	-	-	-	-	-	TXDIS	TXEN

7	6	5	4	3	2	1	0
-	-	-	-	-	-	RXDIS	RXEN

- **SWRST: Software Reset**
  Writing this strobe causes a reset of the PS/2 interface module. Data shift registers are cleared and configuration registers are reset to default values.
- **TXDIS: Transmitter Disable**
  0: No effect.
  1: Disables the transmitter.
- **TXEN: Transmitter Enable**
  0: No effect.
  1: Enables the transmitter if TXDIS=0.
- **RXDIS: Receiver Disable**
  0: No effect.
  1: Disables the receiver.
- **RXEN: Receiver Enable**
  0: No effect.
  1: Enables the receiver if RXDIS=0.

22.6.2 PS/2 Receive Holding Register

Name: RHR0, RHR1

Access Type: Read-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
RXDATA							

- **RXDATA: Receive Data**

  Data received from the device.

22.6.3 PS/2 Transmit Holding Register

Name: THR0, THR1

Access Type: Write-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
TXDATA							

- **TXDATA: Transmit Data**

  Data to be transmitted to the device.

22.6.4 PS/2 Status Register

Name: SR0, SR1

Access Type: Read-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	PARITY	NACK
7	6	5	4	3	2	1	0
-	-	OVRUN	RXRDY	-	-	TXEMPTY	TXRDY

- **PARITY:**
  0: No parity errors detected on incoming data since last read of SR.
  1: At least one parity error detected on incoming data since last read of SR.
- **NACK: Not Acknowledge**
  0: All transmissions has been properly acknowledged by the device since last read of SR.
  1: At least one transmission was not properly acknowledged by the device since last read of SR.
- **OVRUN: Overrun**
  0: No receive overrun has occured since the last read of SR.
  1: At least one receive overrun condition has occured since the last read of SR.
- **RXRDY: Receiver Ready**
  0: RHR is empty.
  1: RHR contains valid data received from the device.
- **TXEMPTY: Transmitter Empty**
  0: Data remains in THR or is currently being transmitted from the shift register.
  1: Both THR and the shift register are empty.
- **TXRDY: Transmitter Ready**
  0: Data has been loaded in THR and is waiting to be loaded into the shift register.
  1: THR is empty.

22.6.5 PS/2 Interrupt Enable Register

Name: IER0, IER1

Access Type: Write-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	PARITY	NACK
7	6	5	4	3	2	1	0
-	-	OVRUN	RXRDY	-	-	TXEMPTY	TXRDY

- **PARITY: PARITY Interrupt Enable**
- **NACK: Not Acknowledge Interrupt Enable**
- **OVRUN: Overrun Interrupt Enable**
- **RXRDY: Overrun Interrupt Enable**
- **TXEMPTY: Overrun Interrupt Enable**
- **TXRDY: Overrun Interrupt Enable**

  0: No effect.

  1: Enables the corresponding interrupt.

22.6.6 PS/2 Interrupt Disable Register

Name: IDR0, IDR1

Access Type: Write-Only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	PARITY	NACK
7	6	5	4	3	2	1	0
-	-	OVRUN	RXRDY	-	-	TXEMPTY	TXRDY

- **PARITY: PARITY Interrupt Disable**
- **NACK: Not Acknowledge Interrupt Disable**
- **OVRUN: Overrun Interrupt Disable**
- **RXRDY: Overrun Interrupt Disable**
- **TXEMPTY: Overrun Interrupt Disable**
- **TXRDY: Overrun Interrupt Disable**

  0: No effect.

  1: Disables the corresponding interrupt.

22.6.7 PS/2 Interrupt Mask Register

Name: IMR0, IMR1

Access Type: Read-only

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	PARITY	NACK
7	6	5	4	3	2	1	0
-	-	OVRUN	RXRDY	-	-	TXEMPTY	TXRDY

- **PARITY: PARITY Interrupt Mask**
- **NACK: Not Acknowledge Interrupt Mask**
- **OVRUN: Overrun Interrupt Mask**
- **RXRDY: Overrun Interrupt Mask**
- **TXEMPTY: Overrun Interrupt Mask**
- **TXRDY: Overrun Interrupt Mask**

  0: The corresponding interrupt is disabled.

  1: The corresponding interrupt is enabled.

22.6.8 PS/2 Prescale Register

Name: PSR0, PSR1

Access Type: Read/Write

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	PRSCV			
7	6	5	4	3	2	1	0
PRSCV							

- **PRSCV: Prescale Value**

23. Synchronous Serial Controller (SSC)

Rev: 2.0.0.2

23.1 Features

- **Provides Serial Synchronous Communication Links Used in Audio and Telecom Applications**
- **Contains an Independent Receiver and Transmitter and a Common Clock Divider**
- **Interfaced with Two PDCA Channels (DMA Access) to Reduce Processor Overhead**
- **Offers a Configurable Frame Sync and Data Length**
- **Receiver and Transmitter Can be Programmed to Start Automatically or on Detection of Different Events on the Frame Sync Signal**
- **Receiver and Transmitter Include a Data Signal, a Clock Signal and a Frame Synchronization Signal**

23.2 Overview

The Atmel Synchronous Serial Controller (SSC) provides a synchronous communication link with external devices. It supports many serial synchronous communication protocols generally used in audio and telecom applications such as I2S, Short Frame Sync, Long Frame Sync, etc.

The SSC contains an independent receiver and transmitter and a common clock divider. The receiver and the transmitter each interface with three signals: the TX_DATA/RX_DATA signal for data, the TX_CLOCK/RX_CLOCK signal for the clock and the TX_FRAME_SYNC/RX_FRAME_SYNC signal for the Frame Sync. The transfers can be programmed to start automatically or on different events detected on the Frame Sync signal.

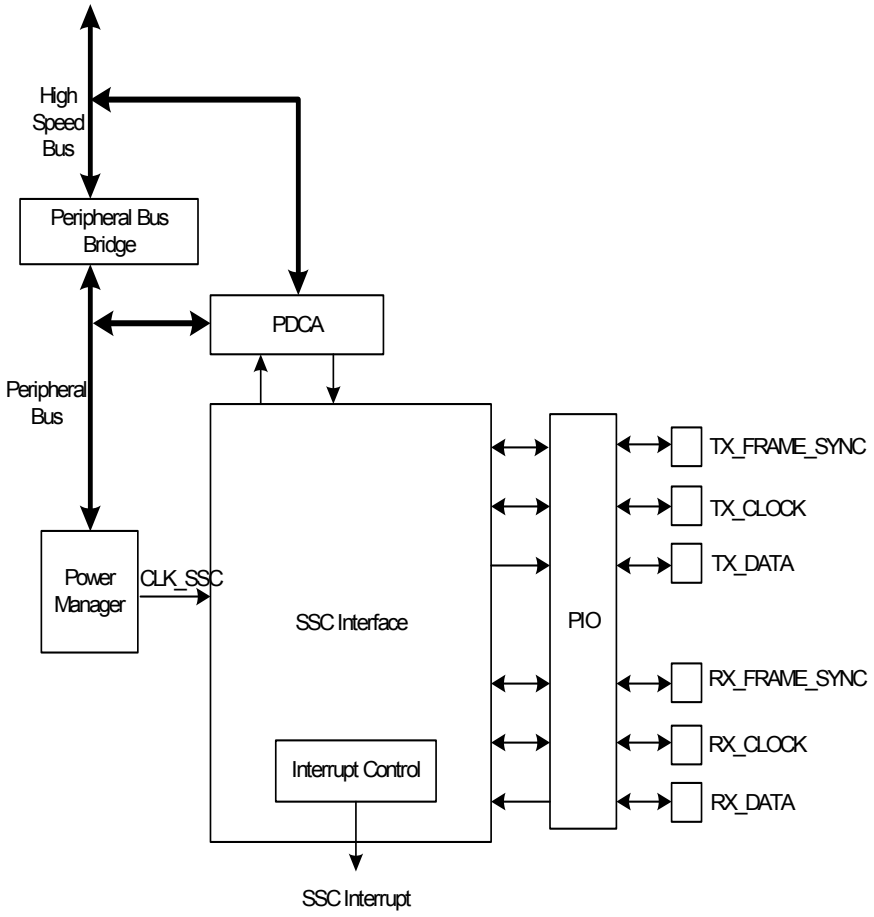
The SSC's high-level of programmability and its two dedicated PDCA channels of up to 32 bits permit a continuous high bit rate data transfer without processor intervention.

Featuring connection to two PDCA channels, the SSC permits interfacing with low processor overhead to the following:

- CODEC's in master or slave mode
- DAC through dedicated serial interface, particularly I2S
- Magnetic card reader

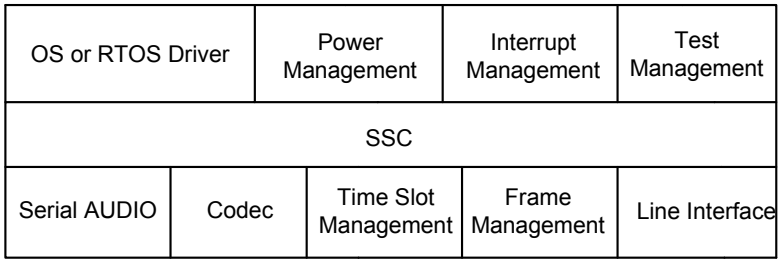
23.3 Block Diagram

Figure 23-1. Block Diagram



23.4 Application Block Diagram

Figure 23-2. Application Block Diagram



23.5 I/O Lines Description

Table 23-1. I/O Lines Description

Pin Name	Pin Description	Type
RX_FRAME_SYNC	Receiver Frame Synchro	Input/Output
RX_CLOCK	Receiver Clock	Input/Output
RX_DATA	Receiver Data	Input
TX_FRAME_SYNC	Transmitter Frame Synchro	Input/Output
TX_CLOCK	Transmitter Clock	Input/Output
TX_DATA	Transmitter Data	Output

23.6 Product Dependencies

23.6.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines.

Before using the SSC receiver, the PIO controller must be configured to dedicate the SSC receiver I/O lines to the SSC peripheral mode.

Before using the SSC transmitter, the PIO controller must be configured to dedicate the SSC transmitter I/O lines to the SSC peripheral mode.

23.6.2 Power Management

The SSC clock is generated by the power manager. Before using the SSC, the programmer must ensure that the SSC clock is enabled in the power manager.

In the SSC description, Master Clock (CLK_SSC) is the bus clock of the peripheral bus to which the SSC is connected.

23.6.3 Interrupt

The SSC interface has an interrupt line connected to the interrupt controller. Handling interrupts requires programming the interrupt controller before configuring the SSC.

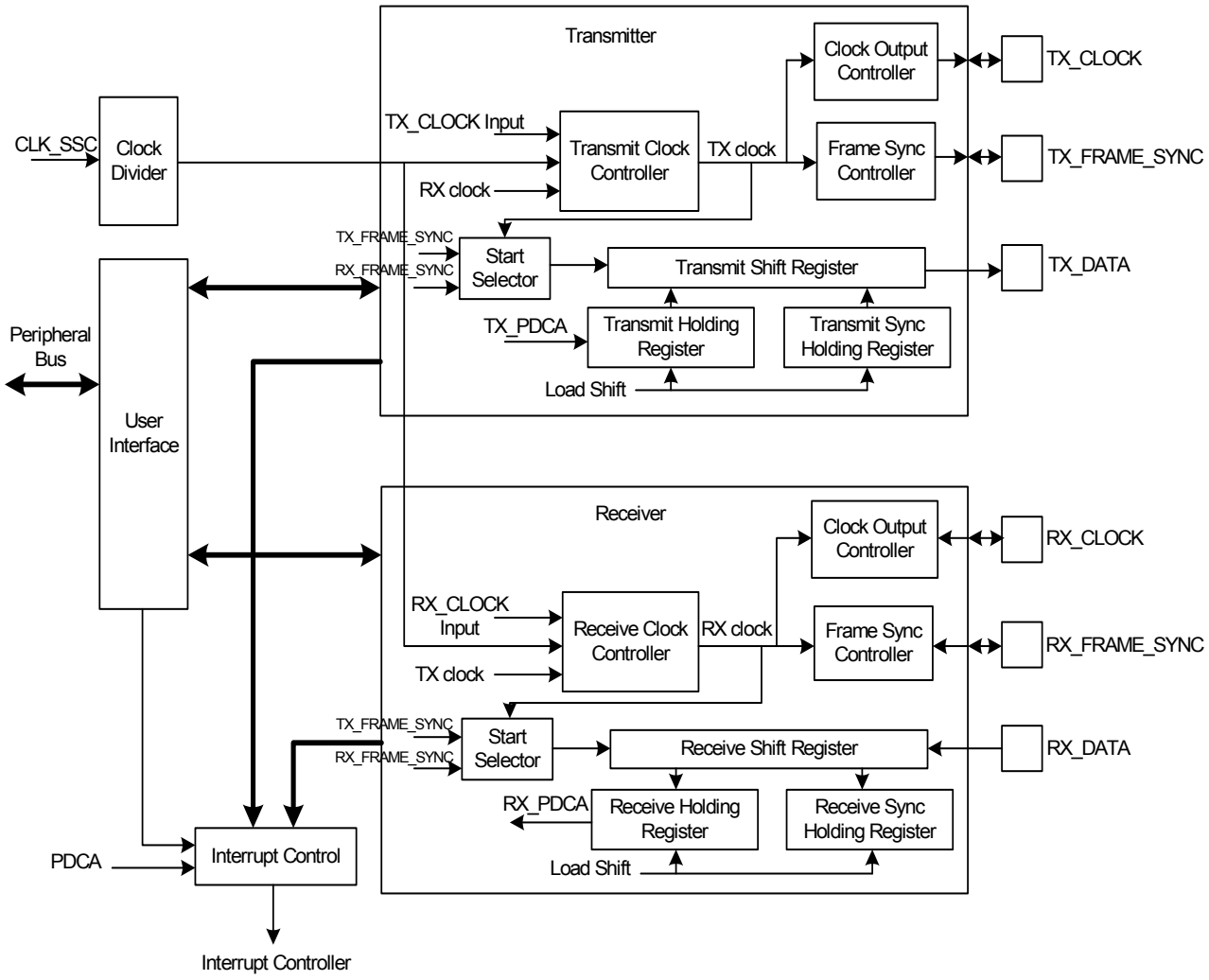
All SSC interrupts can be enabled/disabled configuring the SSC Interrupt mask register. Each pending and unmasked SSC interrupt will assert the SSC interrupt line. The SSC interrupt service routine can get the interrupt origin by reading the SSC interrupt status register.

23.7 Functional Description

This chapter contains the functional description of the following: SSC Functional Block, Clock Management, Data format, Start, Transmitter, Receiver and Frame Sync.

The receiver and transmitter operate separately. However, they can work synchronously by programming the receiver to use the transmit clock and/or to start a data transfer when transmission starts. Alternatively, this can be done by programming the transmitter to use the receive clock and/or to start a data transfer when reception starts. The transmitter and the receiver can be programmed to operate with the clock signals provided on either the TX_CLOCK or RX_CLOCK pins. This allows the SSC to support many slave-mode data transfers. The maximum clock speed allowed on the TX_CLOCK and RX_CLOCK pins is the master clock divided by 2.

Figure 23-3. SSC Functional Block Diagram



23.7.1 Clock Management

The transmitter clock can be generated by:

- an external clock received on the TX_CLOCK I/O pad
- the receiver clock
- the internal clock divider

The receiver clock can be generated by:

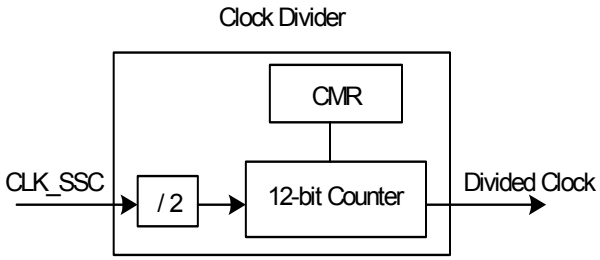
- an external clock received on the RX_CLOCK I/O pad
- the transmitter clock
- the internal clock divider

Furthermore, the transmitter block can generate an external clock on the TX_CLOCK I/O pad, and the receiver block can generate an external clock on the RX_CLOCK I/O pad.

This allows the SSC to support many Master and Slave Mode data transfers.

23.7.1.1 Clock Divider

Figure 23-4. Divided Clock Block Diagram



The Master Clock divider is determined by the 12-bit field DIV counter and comparator (so its maximal value is 4095) in the Clock Mode Register CMR, allowing a Master Clock division by up to 8190. The Divided Clock is provided to both the Receiver and Transmitter. When this field is programmed to 0, the Clock Divider is not used and remains inactive.

When DIV is set to a value equal to or greater than 1, the Divided Clock has a frequency of Master Clock divided by 2 times DIV. Each level of the Divided Clock has a duration of the Master Clock multiplied by DIV. This ensures a 50% duty cycle for the Divided Clock regardless of whether the DIV value is even or odd.

Figure 23-5. Divided Clock Generation

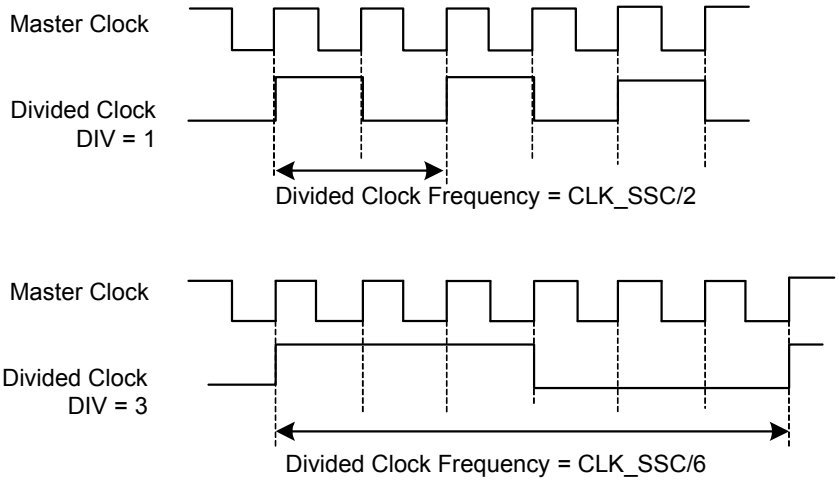


Table 23-2.

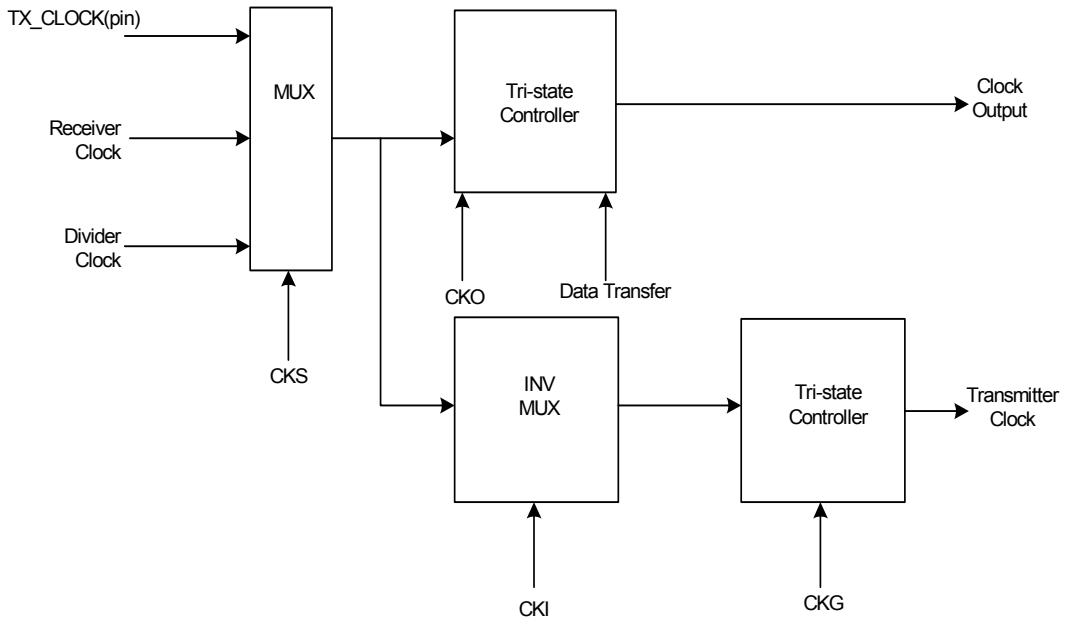
Maximum	Minimum
CLK_SSC / 2	CLK_SSC / 8190

23.7.1.2 Transmitter Clock Management

The transmitter clock is generated from the receiver clock or the divider clock or an external clock scanned on the TX_CLOCK I/O pad. The transmitter clock is selected by the CKS field in TCMR (Transmit Clock Mode Register). Transmit Clock can be inverted independently by the CKI bits in TCMR.

The transmitter can also drive the TX_CLOCK I/O pad continuously or be limited to the actual data transfer. The clock output is configured by the TCMR register. The Transmit Clock Inversion (CKI) bits have no effect on the clock outputs. Programming the TCMR register to select TX_CLOCK pin (CKS field) and at the same time Continuous Transmit Clock (CKO field) might lead to unpredictable results.

Figure 23-6. Transmitter Clock Management

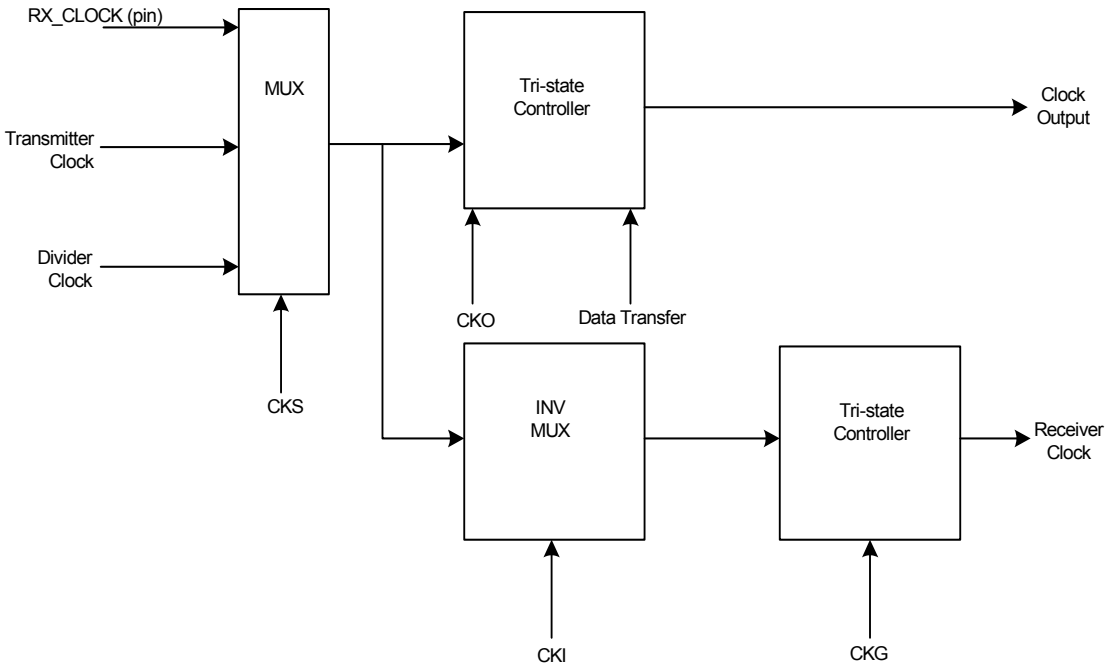


23.7.1.3 Receiver Clock Management

The receiver clock is generated from the transmitter clock or the divider clock or an external clock scanned on the RX_CLOCK I/O pad. The Receive Clock is selected by the CKS field in RCMR (Receive Clock Mode Register). Receive Clocks can be inverted independently by the CKI bits in RCMR.

The receiver can also drive the RX_CLOCK I/O pad continuously or be limited to the actual data transfer. The clock output is configured by the RCMR register. The Receive Clock Inversion (CKI) bits have no effect on the clock outputs. Programming the RCMR register to select RX_CLOCK pin (CKS field) and at the same time Continuous Receive Clock (CKO field) can lead to unpredictable results.

Figure 23-7. Receiver Clock Management



23.7.1.4 Serial Clock Ratio Considerations

The Transmitter and the Receiver can be programmed to operate with the clock signals provided on either the TX_CLOCK or RX_CLOCK pins. This allows the SSC to support many slave-mode data transfers. In this case, the maximum clock speed allowed on the RX_CLOCK pin is:

–Master Clock divided by 2 if Receiver Frame Synchro is input

–Master Clock divided by 3 if Receiver Frame Synchro is output

In addition, the maximum clock speed allowed on the TX_CLOCK pin is:

–Master Clock divided by 6 if Transmit Frame Synchro is input

–Master Clock divided by 2 if Transmit Frame Synchro is output

23.7.2 Transmitter Operations

A transmitted frame is triggered by a start event and can be followed by synchronization data before data transmission.

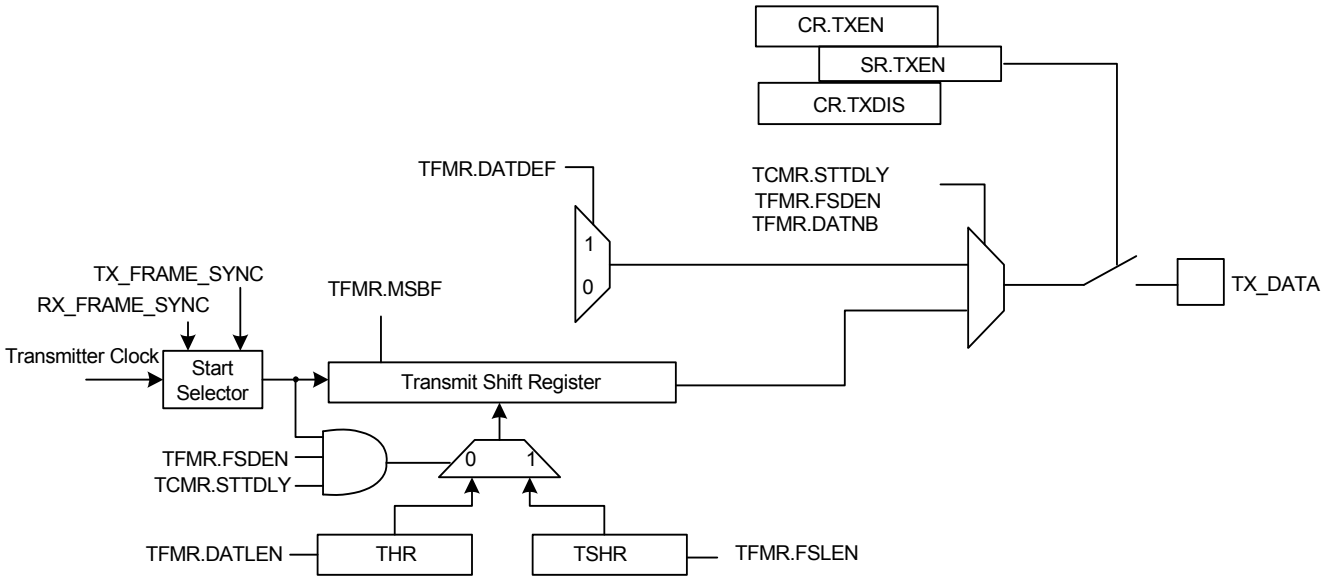
The start event is configured by setting the Transmit Clock Mode Register (TCMR). See Section “23.7.4” on page 360.

The frame synchronization is configured setting the Transmit Frame Mode Register (TFMR). See Section “23.7.5” on page 362.

To transmit data, the transmitter uses a shift register clocked by the transmitter clock signal and the start mode selected in the TCMR. Data is written by the application to the THR register then transferred to the shift register according to the data format selected.

When both the THR and the transmit shift register are empty, the status flag TXEMPTY is set in SR. When the Transmit Holding register is transferred in the Transmit shift register, the status flag TXRDY is set in SR and additional data can be loaded in the holding register.

Figure 23-8. Transmitter Block Diagram



23.7.3 Receiver Operations

A received frame is triggered by a start event and can be followed by synchronization data before data transmission.

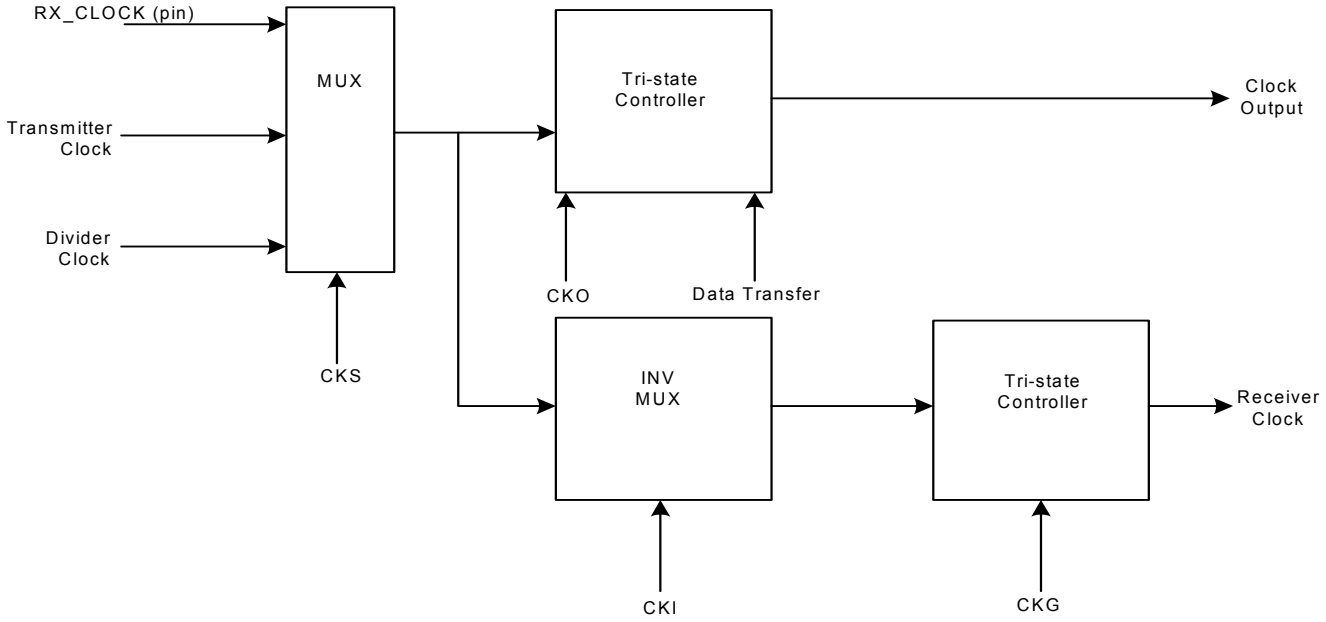
The start event is configured setting the Receive Clock Mode Register (RCMR). See Section “23.7.4” on page 360.

The frame synchronization is configured setting the Receive Frame Mode Register (RFMR). See Section “23.7.5” on page 362.

The receiver uses a shift register clocked by the receiver clock signal and the start mode selected in the RCMR. The data is transferred from the shift register depending on the data format selected.

When the receiver shift register is full, the SSC transfers this data in the holding register, the status flag RXRDY is set in SR and the data can be read in the receiver holding register. If another transfer occurs before read of the RHR register, the status flag OVERUN is set in SR and the receiver shift register is transferred in the RHR register.

Figure 23-9. Receiver Block Diagram



23.7.4 Start

The transmitter and receiver can both be programmed to start their operations when an event occurs, respectively in the Transmit Start Selection (START) field of TCMR and in the Receive Start Selection (START) field of RCMR.

Under the following conditions the start event is independently programmable:

- Continuous. In this case, the transmission starts as soon as a word is written in THR and the reception starts as soon as the Receiver is enabled.
- Synchronously with the transmitter/receiver
- On detection of a falling/rising edge on TX_FRAME_SYNC/RX_FRAME_SYNC
- On detection of a low level/high level on TX_FRAME_SYNC/RX_FRAME_SYNC
- On detection of a level change or an edge on TX_FRAME_SYNC/RX_FRAME_SYNC

A start can be programmed in the same manner on either side of the Transmit/Receive Clock Register (RCMR/TCMR). Thus, the start could be on TX_FRAME_SYNC (Transmit) or RX_FRAME_SYNC (Receive).

Moreover, the Receiver can start when data is detected in the bit stream with the Compare Functions.

Detection on TX_FRAME_SYNC/RX_FRAME_SYNC input/output is done by the field FSOS of the Transmit/Receive Frame Mode Register (TFMR/RFMR).

Figure 23-10. Transmit Start Mode

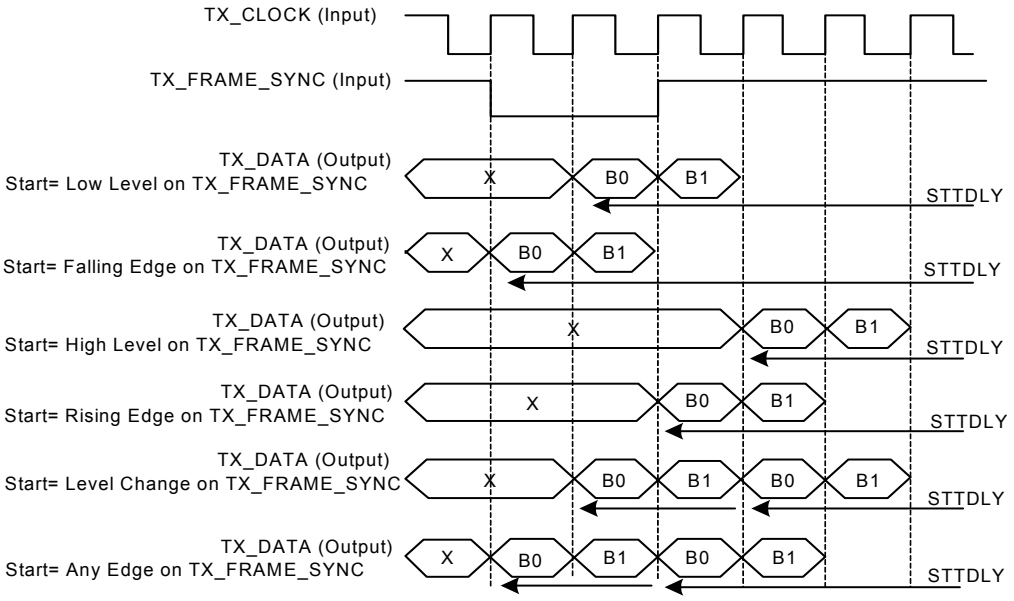
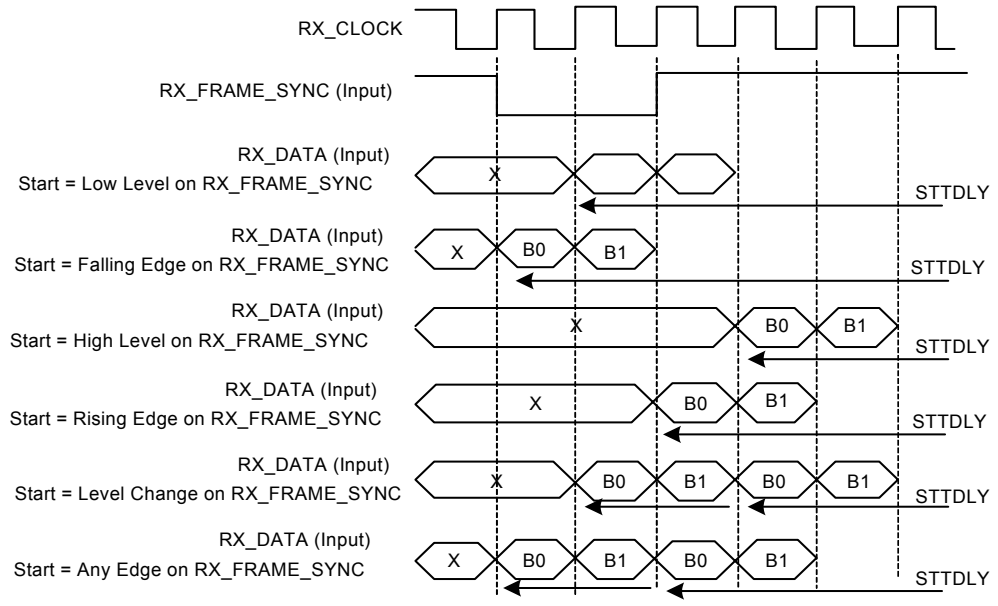


Figure 23-11. Receive Pulse/Edge Start Modes



23.7.5 Frame Sync

The Transmitter and Receiver Frame Sync pins, TX_FRAME_SYNC and RX_FRAME_SYNC, can be programmed to generate different kinds of frame synchronization signals. The Frame Sync Output Selection (FSOS) field in the Receive Frame Mode Register (RFMR) and in the Transmit Frame Mode Register (TFMR) are used to select the required waveform.

- Programmable low or high levels during data transfer are supported.
- Programmable high levels before the start of data transfers or toggling are also supported.

If a pulse waveform is selected, the Frame Sync Length (FSLEN) field in RFMR and TFMR programs the length of the pulse, from 1 bit time up to 16 bit time.

The periodicity of the Receive and Transmit Frame Sync pulse output can be programmed through the Period Divider Selection (PERIOD) field in RCMR and TCMR.

23.7.5.1 Frame Sync Data

Frame Sync Data transmits or receives a specific tag during the Frame Sync signal.

During the Frame Sync signal, the Receiver can sample the RX_DATA line and store the data in the Receive Sync Holding Register and the transmitter can transfer Transmit Sync Holding Register in the Shifter Register. The data length to be sampled/shifted out during the Frame Sync signal is programmed by the FSLEN field in RFMR/TFMR.

Concerning the Receive Frame Sync Data operation, if the Frame Sync Length is equal to or lower than the delay between the start event and the actual data reception, the data sampling operation is performed in the Receive Sync Holding Register through the Receive Shift Register.

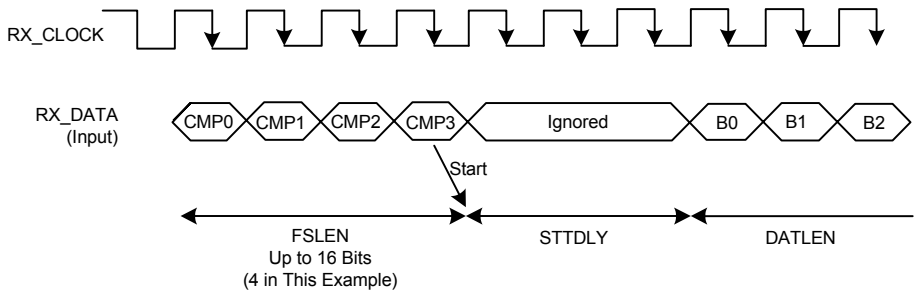
The Transmit Frame Sync Operation is performed by the transmitter only if the bit Frame Sync Data Enable (FSDEN) in TFMR is set. If the Frame Sync length is equal to or lower than the delay between the start event and the actual data transmission, the normal transmission has priority and the data contained in the Transmit Sync Holding Register is transferred in the Transmit Register, then shifted out.

23.7.5.2 Frame Sync Edge Detection

The Frame Sync Edge detection is programmed by the FSEDGE field in RFMR/TFMR. This sets the corresponding flags RXSYN/TXSYN in the SSC Status Register (SR) on frame synchro edge detection (signals RX_FRAME_SYNC/TX_FRAME_SYNC).

23.7.6 Receive Compare Modes

Figure 23-12. Receive Compare Modes



23.7.6.1 Compare Functions

Compare 0 can be one start event of the Receiver. In this case, the receiver compares at each new sample the last FSLEN bits received at the FSLEN lower bit of the data contained in the Compare 0 Register (RC0R). When this start event is selected, the user can program the Receiver to start a new data transfer either by writing a new Compare 0, or by receiving continuously until Compare 1 occurs. This selection is done with the bit (STOP) in RCMR.

23.7.7 Data Format

The data framing format of both the transmitter and the receiver are programmable through the Transmitter Frame Mode Register (TFMR) and the Receiver Frame Mode Register (RFMR). In either case, the user can independently select:

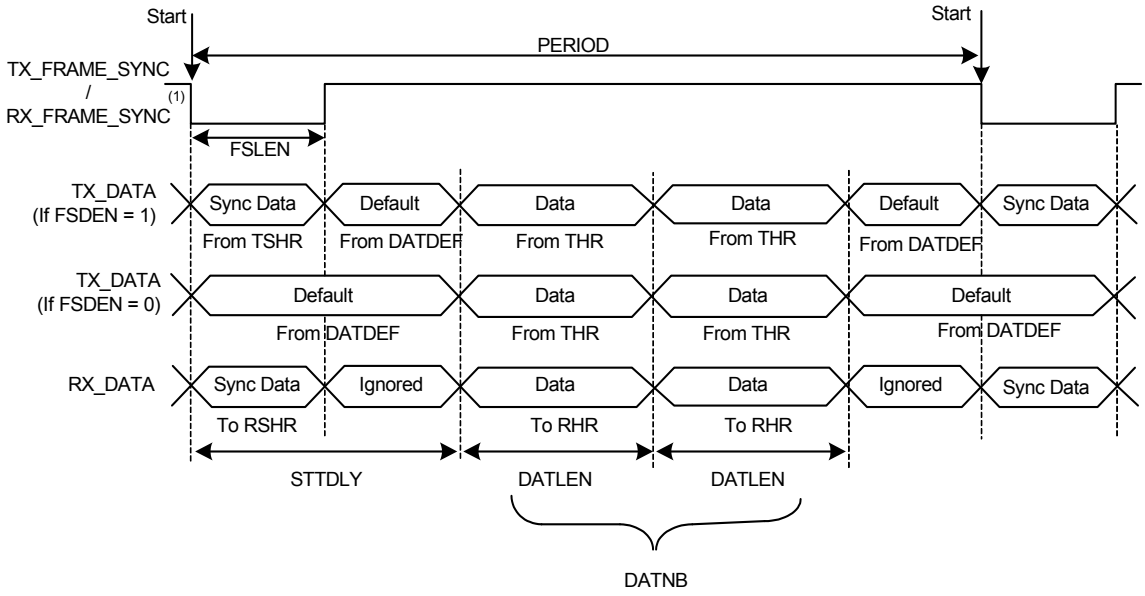
- the event that starts the data transfer (START)
- the delay in number of bit periods between the start event and the first data bit (STTDLY)
- the length of the data (DATLEN)
- the number of data to be transferred for each start event (DATNB).
- the length of synchronization transferred for each start event (FSLEN)
- the bit sense: most or lowest significant bit first (MSBF).

Additionally, the transmitter can be used to transfer synchronization and select the level driven on the TX_DATA pin while not in data transfer operation. This is done respectively by the Frame Sync Data Enable (FSDEN) and by the Data Default Value (DATDEF) bits in TFMR.

Table 23-3. Data Frame Registers

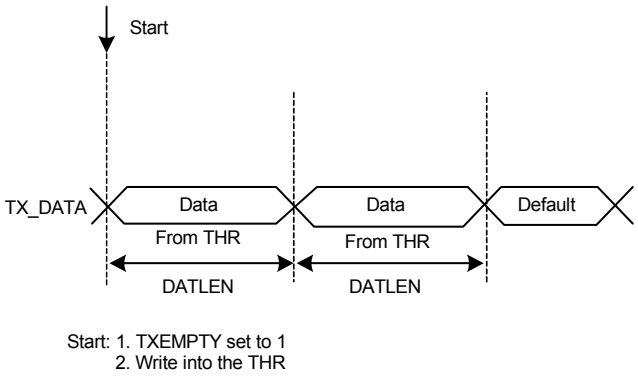
Transmitter	Receiver	Field	Length	Comment
TFMR	RFMR	DATLEN	Up to 32	Size of word
TFMR	RFMR	DATNB	Up to 16	Number of words transmitted in frame
TFMR	RFMR	MSBF		Most significant bit first
TFMR	RFMR	FSLEN	Up to 16	Size of Synchro data register
TFMR		DATDEF	0 or 1	Data default value ended
TFMR		FSDEN		Enable send TSHR
TCMR	RCMR	PERIOD	Up to 512	Frame size
TCMR	RCMR	STTDLY	Up to 255	Size of transmit start delay

Figure 23-13. Transmit and Receive Frame Format in Edge/Pulse Start Modes



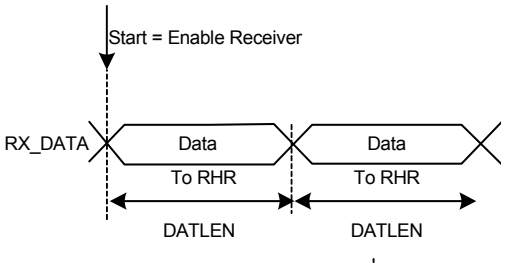
Note: 1. Example of input on falling edge of TX_FRAME_SYNC/RX_FRAME_SYNC.

Figure 23-14. Transmit Frame Format in Continuous Mode



Note: 1. STTDLY is set to 0. In this example, THR is loaded twice. FSDEN value has no effect on the transmission. SyncData cannot be output in continuous mode.

Figure 23-15. Receive Frame Format in Continuous Mode



Note: 1. STTDLY is set to 0.

23.7.8 Loop Mode

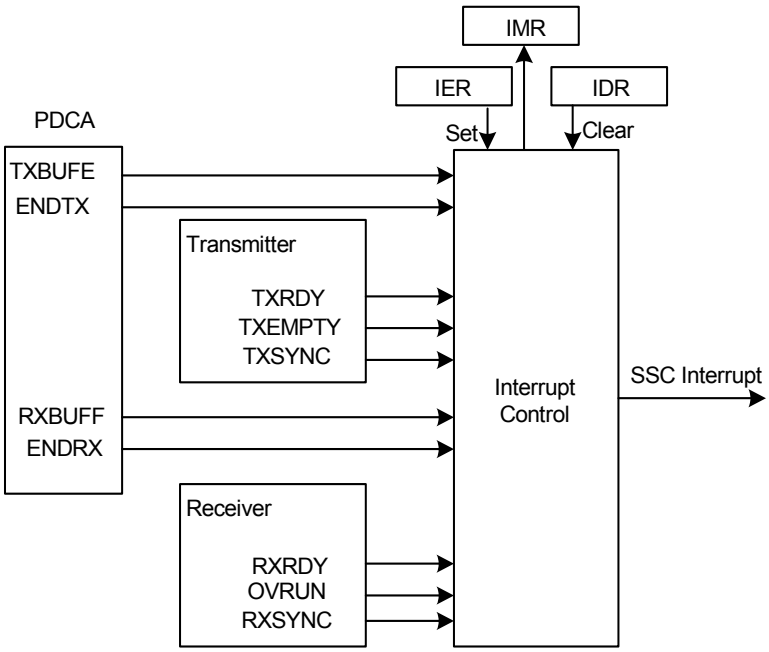
The receiver can be programmed to receive transmissions from the transmitter. This is done by setting the Loop Mode (LOOP) bit in RFMR. In this case, RX_DATA is connected to TX_DATA, RX_FRAME_SYNC is connected to TX_FRAME_SYNC and RX_CLOCK is connected to TX_CLOCK.

23.7.9 Interrupt

Most bits in SR have a corresponding bit in interrupt management registers.

The SSC can be programmed to generate an interrupt when it detects an event. The interrupt is controlled by writing IER (Interrupt Enable Register) and IDR (Interrupt Disable Register) These registers enable and disable, respectively, the corresponding interrupt by setting and clearing the corresponding bit in IMR (Interrupt Mask Register), which controls the generation of interrupts by asserting the SSC interrupt line connected to the interrupt controller.

Figure 23-16. Interrupt Block Diagram



23.8 SSC Application Examples

The SSC can support several serial communication modes used in audio or high speed serial links. Some standard applications are shown in the following figures. All serial link applications supported by the SSC are not listed here.

Figure 23-17. Audio Application Block Diagram

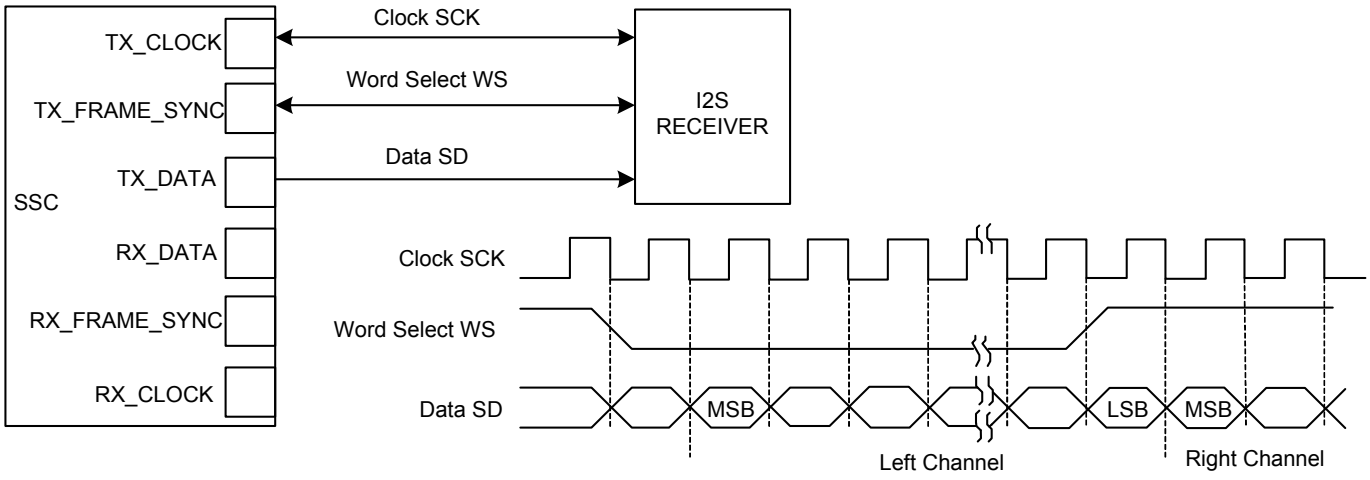


Figure 23-18. Codec Application Block Diagram

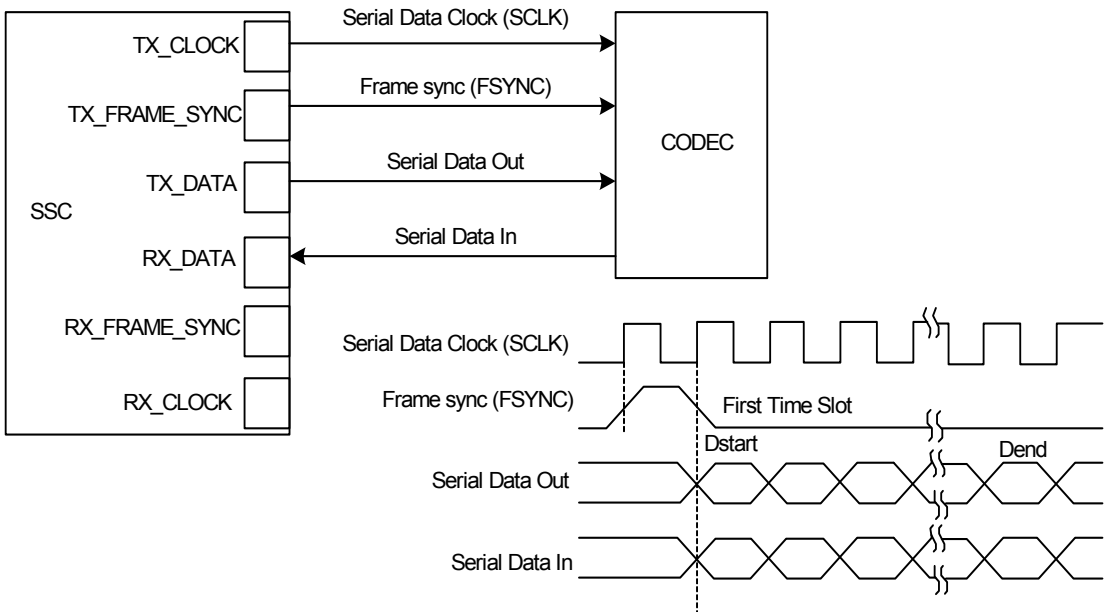
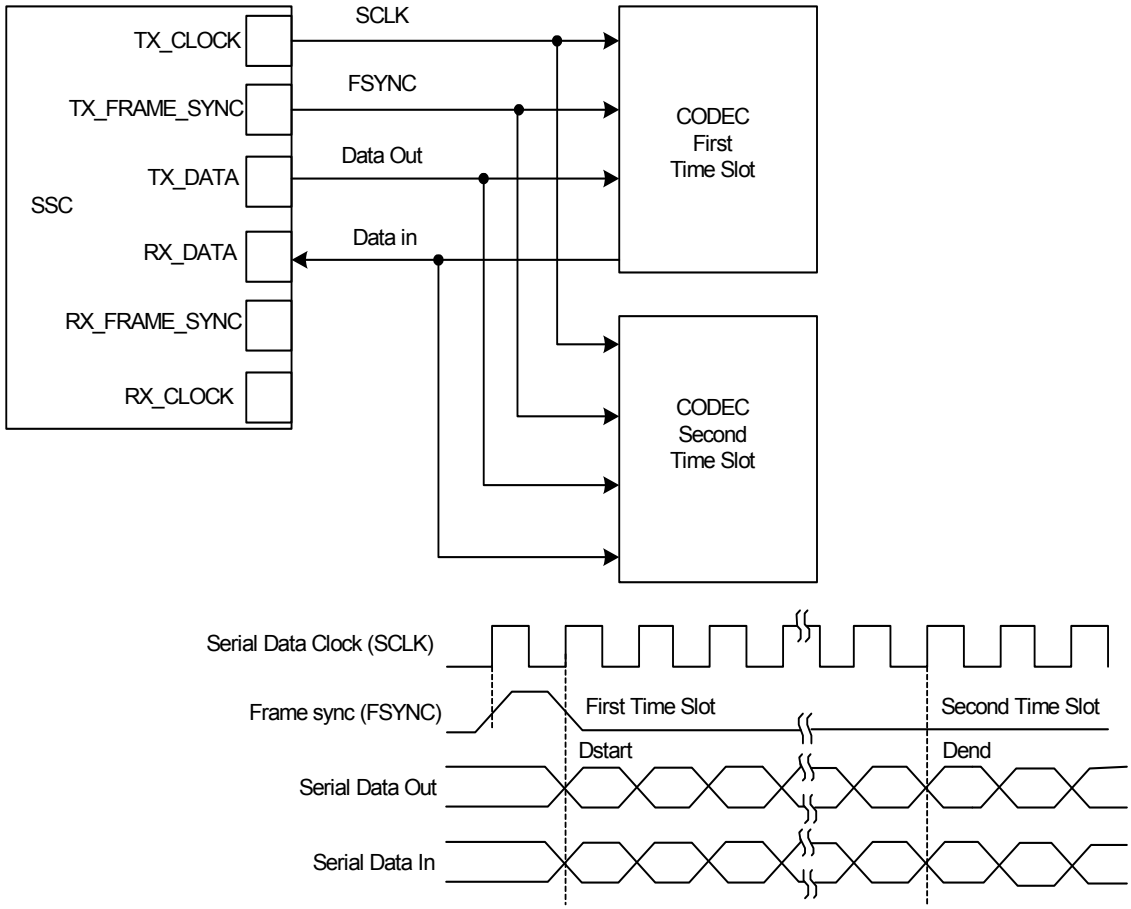


Figure 23-19. Time Slot Application Block Diagram



23.9 User Interface

Table 23-4. Register Mapping

Offset	Register	Register Name	Access	Reset
0x0	Control Register	CR	Write	–
0x4	Clock Mode Register	CMR	Read/Write	0x0
0x8	Reserved	–	–	–
0xC	Reserved	–	–	–
0x10	Receive Clock Mode Register	RCMR	Read/Write	0x0
0x14	Receive Frame Mode Register	RFMR	Read/Write	0x0
0x18	Transmit Clock Mode Register	TCMR	Read/Write	0x0
0x1C	Transmit Frame Mode Register	TFMR	Read/Write	0x0
0x20	Receive Holding Register	RHR	Read	0x0
0x24	Transmit Holding Register	THR	Write	–
0x28	Reserved	–	–	–
0x2C	Reserved	–	–	–
0x30	Receive Sync. Holding Register	RSHR	Read	0x0
0x34	Transmit Sync. Holding Register	TSHR	Read/Write	0x0
0x38	Receive Compare 0 Register	RC0R	Read/Write	0x0
0x3C	Receive Compare 1 Register	RC1R	Read/Write	0x0
0x40	Status Register	SR	Read	0x000000CC
0x44	Interrupt Enable Register	IER	Write	–
0x48	Interrupt Disable Register	IDR	Write	–
0x4C	Interrupt Mask Register	IMR	Read	0x0
0x50-0xFC	Reserved	–	–	–

23.9.1 Control Register

Name: CR

Access Type: Write-only

Offset: 0x00

Reset value: -

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
SWRST	–	–	–	–	–	TXDIS	TXEN
7	6	5	4	3	2	1	0
–	–	–	–	–	–	RXDIS	RXEN

- **SWRST: Software Reset**

0: No effect.

1: Performs a software reset. Has priority on any other bit in CR.

- **TXDIS: Transmit Disable**

0: No effect.

1: Disables Transmit. If a character is currently being transmitted, disables at end of current character transmission.

- **TXEN: Transmit Enable**

0: No effect.

1: Enables Transmit if TXDIS is not set.

- **RXDIS: Receive Disable**

0: No effect.

1: Disables Receive. If a character is currently being received, disables at end of current character reception.

- **RXEN: Receive Enable**

0: No effect.

1: Enables Receive if RXDIS is not set.

23.9.2 Clock Mode Register

Name: CMR

Access Type: Read/Write

Offset: 0x04

Reset value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	DIV			

7	6	5	4	3	2	1	0
DIV							

- **DIV: Clock Divider**

0: The Clock Divider is not active.

Any Other Value: The Divided Clock equals the Master Clock divided by 2 times DIV. The maximum bit rate is CLK_SSC/2. The minimum bit rate is CLK_SSC/2 x 4095 = CLK_SSC/8190.

23.9.3 Receive Clock Mode Register

Name: RCMR

Access Type: Read/Write

Offset: 0x10

Reset value: 0x00000000

31	30	29	28	27	26	25	24
PERIOD							

23	22	21	20	19	18	17	16
STTDLY							

15	14	13	12	11	10	9	8
–	–	–	STOP	START			

7	6	5	4	3	2	1	0
CKG		CKI	CKO			CKS	

- **PERIOD: Receive Period Divider Selection**

This field selects the divider to apply to the selected Receive Clock in order to generate a new Frame Sync Signal. If 0, no PERIOD signal is generated. If not 0, a PERIOD signal is generated each 2 x (PERIOD+1) Receive Clock.

- **STTDLY: Receive Start Delay**

If STTDLY is not 0, a delay of STTDLY clock cycles is inserted between the start event and the actual start of reception. When the Receiver is programmed to start synchronously with the Transmitter, the delay is also applied.

Note: It is very important that STTDLY be set carefully. If STTDLY must be set, it should be done in relation to TAG (Receive Sync Data) reception.

- **STOP: Receive Stop Selection**

0: After completion of a data transfer when starting with a Compare 0, the receiver stops the data transfer and waits for a new compare 0.

1: After starting a receive with a Compare 0, the receiver operates in a continuous mode until a Compare 1 is detected.

- **START: Receive Start Selection**

START	Receive Start
0x0	Continuous, as soon as the receiver is enabled, and immediately after the end of transfer of the previous data.
0x1	Transmit start
0x2	Detection of a low level on RX_FRAME_SYNC signal
0x3	Detection of a high level on RX_FRAME_SYNC signal
0x4	Detection of a falling edge on RX_FRAME_SYNC signal
0x5	Detection of a rising edge on RX_FRAME_SYNC signal
0x6	Detection of any level change on RX_FRAME_SYNC signal
0x7	Detection of any edge on RX_FRAME_SYNC signal
0x8	Compare 0
0x9-0xF	Reserved

- **CKG: Receive Clock Gating Selection**

CKG	Receive Clock Gating
0x0	None, continuous clock
0x1	Receive Clock enabled only if RX_FRAME_SYNC Low
0x2	Receive Clock enabled only if RX_FRAME_SYNC High
0x3	Reserved

- **CKI: Receive Clock Inversion**

0: The data inputs (Data and Frame Sync signals) are sampled on Receive Clock falling edge. The Frame Sync signal output is shifted out on Receive Clock rising edge.

1: The data inputs (Data and Frame Sync signals) are sampled on Receive Clock rising edge. The Frame Sync signal output is shifted out on Receive Clock falling edge.

CKI affects only the Receive Clock and not the output clock signal.

- **CKO: Receive Clock Output Mode Selection**

CKO	Receive Clock Output Mode	RX_CLOCK pin
0x0	None	Input-only
0x1	Continuous Receive Clock	Output
0x2	Receive Clock only during data transfers	Output
0x3-0x7	Reserved	

- **CKS: Receive Clock Selection**

CKS	Selected Receive Clock
0x0	Divided Clock
0x1	TX_CLOCK Clock signal
0x2	RX_CLOCK pin
0x3	Reserved

23.9.4 Receive Frame Mode Register

Name: RFMR

Access Type: Read/Write

Offset: 0x14

Reset value: 0x00000000

31	30	29	28	27	26	25	24
FSLENHI				–	–	–	FSEDGE

23	22	21	20	19	18	17	16
–	FSOS			FSLEN			

15	14	13	12	11	10	9	8
–	–	–	–	DATNB			

7	6	5	4	3	2	1	0
MSBF	–	LOOP	DATLEN				

- **FSLENHI: Receive Frame Sync Length High part**

The four MSB of the FSLEN bitfield.

- **FSEDGE: Frame Sync Edge Detection**

Determines which edge on Frame Sync will generate the interrupt RXSYN in the SSC Status Register.

FSEDGE	Frame Sync Edge Detection
0x0	Positive Edge Detection
0x1	Negative Edge Detection

- **FSOS: Receive Frame Sync Output Selection**

FSOS	Selected Receive Frame Sync Signal	RX_FRAME_SYNC Pin
0x0	None	Input-only
0x1	Negative Pulse	Output
0x2	Positive Pulse	Output
0x3	Driven Low during data transfer	Output
0x4	Driven High during data transfer	Output
0x5	Toggling at each start of data transfer	Output
0x6-0x7	Reserved	Undefined

- **FSLEN: Receive Frame Sync Length**

This field defines the length of the Receive Frame Sync Signal and the number of bits sampled and stored in the Receive Sync Data Register. When this mode is selected by the START field in the Receive Clock Mode Register, it also determines the length of the sampled data to be compared to the Compare 0 or Compare 1 register. Note: The four most significant bits fo this bitfield are in the FSLENHI bitfield.

Pulse length is equal to ({FSLENHI,FSLEN} + 1) Receive Clock periods. Thus, if {FSLENHI,FSLEN} is 0, the Receive Frame Sync signal is generated during one Receive Clock period.

- **DATNB: Data Number per Frame**

This field defines the number of data words to be received after each transfer start, which is equal to (DATNB + 1).

- **MSBF: Most Significant Bit First**

0: The lowest significant bit of the data register is sampled first in the bit stream.

1: The most significant bit of the data register is sampled first in the bit stream.

- **LOOP: Loop Mode**

0: Normal operating mode.

1: RX_DATA is driven by TX_DATA, RX_FRAME_SYNC is driven by TX_FRAME_SYNC and TX_CLOCK drives RX_CLOCK.

- **DATLEN: Data Length**

0: Forbidden value (1-bit data length not supported).
Any other value: The bit stream contains DATLEN + 1 data bits. Moreover, it defines the transfer size performed by the PDCA assigned to the Receiver. If DATLEN is lower or equal to 7, data transfers are in bytes. If DATLEN is between 8 and 15 (included), half-words are transferred, and for any other value, 32-bit words are transferred.

23.9.5 Transmit Clock Mode Register

Name: TCMR

Access Type: Read/Write

Offset: 0x18

Reset value: 0x00000000

31	30	29	28	27	26	25	24
PERIOD							

23	22	21	20	19	18	17	16
STTDLY							

15	14	13	12	11	10	9	8
–	–	–	–	START			

7	6	5	4	3	2	1	0
CKG		CKI	CKO			CKS	

- **PERIOD: Transmit Period Divider Selection**

This field selects the divider to apply to the selected Transmit Clock to generate a new Frame Sync Signal. If 0, no period signal is generated. If not 0, a period signal is generated at each 2 x (PERIOD+1) Transmit Clock.

- **STTDLY: Transmit Start Delay**

If STTDLY is not 0, a delay of STTDLY clock cycles is inserted between the start event and the actual start of transmission of data. When the Transmitter is programmed to start synchronously with the Receiver, the delay is also applied.

Note: STTDLY must be set carefully. If STTDLY is too short in respect to TAG (Transmit Sync Data) emission, data is emitted instead of the end of TAG.

- **START: Transmit Start Selection**

START	Transmit Start
0x0	Continuous, as soon as a word is written in the THR Register (if Transmit is enabled), and immediately after the end of transfer of the previous data.
0x1	Receive start
0x2	Detection of a low level on TX_FRAME_SYNC signal
0x3	Detection of a high level on TX_FRAME_SYNC signal
0x4	Detection of a falling edge on TX_FRAME_SYNC signal
0x5	Detection of a rising edge on TX_FRAME_SYNC signal
0x6	Detection of any level change on TX_FRAME_SYNC signal
0x7	Detection of any edge on TX_FRAME_SYNC signal
0x8 - 0xF	Reserved

- **CKG: Transmit Clock Gating Selection**

CKG	Transmit Clock Gating
0x0	None, continuous clock
0x1	Transmit Clock enabled only if TX_FRAME_SYNC Low
0x2	Transmit Clock enabled only if TX_FRAME_SYNC High
0x3	Reserved

- **CKI: Transmit Clock Inversion**

0: The data outputs (Data and Frame Sync signals) are shifted out on Transmit Clock falling edge. The Frame sync signal input is sampled on Transmit clock rising edge.

1: The data outputs (Data and Frame Sync signals) are shifted out on Transmit Clock rising edge. The Frame sync signal input is sampled on Transmit clock falling edge.

CKI affects only the Transmit Clock and not the output clock signal.

- **CKO: Transmit Clock Output Mode Selection**

CKO	Transmit Clock Output Mode	TX_CLOCK pin
0x0	None	Input-only
0x1	Continuous Transmit Clock	Output
0x2	Transmit Clock only during data transfers	Output
0x3-0x7	Reserved	

- **CKS: Transmit Clock Selection**

CKS	Selected Transmit Clock
0x0	Divided Clock
0x1	RX_CLOCK Clock signal
0x2	TX_CLOCK Pin
0x3	Reserved

23.9.6 Transmit Frame Mode Register

Name: TFMR

Access Type: Read/Write

Offset: 0x1C

Reset value: 0x00000000

31	30	29	28	27	26	25	24
FSLENHI				–	–	–	FSEDGE

23	22	21	20	19	18	17	16
FSDEN	FSOS			FSLEN			

15	14	13	12	11	10	9	8
–	–	–	–	DATNB			

7	6	5	4	3	2	1	0
MSBF	–	DATDEF	DATLEN				

- **FSLENHI: Transmit Frame Sync Length High part**

The four MSB of the FSLEN bitfield.

- **FSEDGE: Frame Sync Edge Detection**

Determines which edge on frame sync will generate the interrupt TXSYN (Status Register).

FSEDGE	Frame Sync Edge Detection
0x0	Positive Edge Detection
0x1	Negative Edge Detection

- **FSDEN: Frame Sync Data Enable**

0: The TX_DATA line is driven with the default value during the Transmit Frame Sync signal.

1: TSHR value is shifted out during the transmission of the Transmit Frame Sync signal.

- **FSOS: Transmit Frame Sync Output Selection**

FSOS	Selected Transmit Frame Sync Signal	TX_FRAME_SYNC Pin
0x0	None	Input-only
0x1	Negative Pulse	Output
0x2	Positive Pulse	Output
0x3	Driven Low during data transfer	Output
0x4	Driven High during data transfer	Output
0x5	Toggling at each start of data transfer	Output
0x6-0x7	Reserved	Undefined

- **FSLEN: Transmit Frame Sync Length**

This field defines the length of the Transmit Frame Sync signal and the number of bits shifted out from the Transmit Sync Data Register if FSDEN is 1. Note: The four most significant bits fo this bitfield are in the FSLENHI bitfield.

Pulse length is equal to ({FSLENHI,FSLEN} + 1) Transmit Clock periods, i.e., the pulse length can range from 1 to 16 Transmit Clock periods. If {FSLENHI,FSLEN} is 0, the Transmit Frame Sync signal is generated during one Transmit Clock period.

- **DATNB: Data Number per frame**

This field defines the number of data words to be transferred after each transfer start, which is equal to (DATNB +1).

- **MSBF: Most Significant Bit First**

0: The lowest significant bit of the data register is shifted out first in the bit stream.

1: The most significant bit of the data register is shifted out first in the bit stream.

- **DATDEF: Data Default Value**

This bit defines the level driven on the TX_DATA pin while out of transmission. Note that if the pin is defined as multi-drive by the PIO Controller, the pin is enabled only if the SCC TX_DATA output is 1.

- **DATLEN: Data Length**

0: Forbidden value (1-bit data length not supported).

Any other value: The bit stream contains DATLEN + 1 data bits. Moreover, it defines the transfer size performed by the PDCA assigned to the Transmit. If DATLEN is lower or equal to 7, data transfers are bytes, if DATLEN is between 8 and 15 (included), half-words are transferred, and for any other value, 32-bit words are transferred.

23.9.7 SSC Receive Holding Register

Name: RHR

Access Type: Read-only

Offset: 0x20

Reset value: 0x00000000

31	30	29	28	27	26	25	24
RDAT							

23	22	21	20	19	18	17	16
RDAT							

15	14	13	12	11	10	9	8
RDAT							

7	6	5	4	3	2	1	0
RDAT							

- **RDAT: Receive Data**

Right aligned regardless of the number of data bits defined by DATLEN in RFMR.

23.9.8 Transmit Holding Register

Name: THR

Access Type: Write-only

Offset: 0x24

Reset value: -

31	30	29	28	27	26	25	24
TDAT							

23	22	21	20	19	18	17	16
TDAT							

15	14	13	12	11	10	9	8
TDAT							

7	6	5	4	3	2	1	0
TDAT							

- **TDAT: Transmit Data**

Right aligned regardless of the number of data bits defined by DATLEN in TFMR.

23.9.9 Receive Synchronization Holding Register

Name: RSHR

Access Type: Read-only

Offset: 0x30

Reset value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
RSDAT							

7	6	5	4	3	2	1	0
RSDAT							

- **RSDAT: Receive Synchronization Data**

23.9.10 Transmit Synchronization Holding Register

Name: TSHR

Access Type: Read/Write

Offset: 0x34

Reset value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TSDAT							

7	6	5	4	3	2	1	0
TSDAT							

- **TSDAT: Transmit Synchronization Data**

23.9.11 Receive Compare 0 Register

Name: RC0R

Access Type: Read/Write

Offset: 0x38

Reset value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
CP0							

7	6	5	4	3	2	1	0
CP0							

- **CP0: Receive Compare Data 0**

23.9.12 Receive Compare 1 Register

Name: RC1R

Access Type: Read/Write

Offset: 0x3C

Reset value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
CP1							

7	6	5	4	3	2	1	0
CP1							

- **CP1: Receive Compare Data 1**

23.9.13 Status Register

Name: SR

Access Type: Read-only

Offset: 0x40

Reset value: 0x000000CC

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	RXEN	TXEN
15	14	13	12	11	10	9	8
–	–	–	–	RXSYN	TXSYN	CP1	CP0
7	6	5	4	3	2	1	0
RXBUFF	ENDRX	OVRUN	RXRDY	TXBUFE	ENDTX	TXEMPTY	TXRDY

- **RXEN: Receive Enable**

0: Receive is disabled.

1: Receive is enabled.

- **TXEN: Transmit Enable**

0: Transmit is disabled.

1: Transmit is enabled.

- **RXSYN: Receive Sync**

0: An Rx Sync has not occurred since the last read of the Status Register.

1: An Rx Sync has occurred since the last read of the Status Register.

- **TXSYN: Transmit Sync**

0: A Tx Sync has not occurred since the last read of the Status Register.

1: A Tx Sync has occurred since the last read of the Status Register.

- **CP1: Compare 1**

0: A compare 1 has not occurred since the last read of the Status Register.

1: A compare 1 has occurred since the last read of the Status Register.

- **CP0: Compare 0**

0: A compare 0 has not occurred since the last read of the Status Register.

1: A compare 0 has occurred since the last read of the Status Register.

- **RXBUFF: Receive Buffer Full**

0: RCR or RNCR have a value other than 0.

1: Both RCR and RNCR have a value of 0.

- **ENDRX: End of Reception**

0: Data is written on the Receive Counter Register or Receive Next Counter Register.

1: End of PDCA transfer when Receive Counter Register has arrived at zero.

- **OVRUN: Receive Overrun**

0: No data has been loaded in RHR while previous data has not been read since the last read of the Status Register.

1: Data has been loaded in RHR while previous data has not yet been read since the last read of the Status Register.

- **RXRDY: Receive Ready**

0: RHR is empty.

1: Data has been received and loaded in RHR.

- **TXBUFE: Transmit Buffer Empty**

0: TCR or TNCR have a value other than 0.

1: Both TCR and TNCR have a value of 0.

- **ENDTX: End of Transmission**

0: The register TCR has not reached 0 since the last write in TCR or TNCR.

1: The register TCR has reached 0 since the last write in TCR or TNCR.

- **TXEMPTY: Transmit Empty**

0: Data remains in THR or is currently transmitted from TSR.

1: Last data written in THR has been loaded in TSR and last data loaded in TSR has been transmitted.

- **TXRDY: Transmit Ready**

0: Data has been loaded in THR and is waiting to be loaded in the Transmit Shift Register (TSR).

1: THR is empty.

23.9.14 Interrupt Enable Register

Name: IER

Access Type: Write-only

Offset: 0x44

Reset value: -

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	RXSYN	TXSYN	CP1	CP0
7	6	5	4	3	2	1	0
RXBUFF	ENDRX	OVRUN	RXRDY	TXBUFE	ENDTX	TXEMPTY	TXRDY

- **RXSYN: Rx Sync Interrupt Enable**

0: No effect.

1: Enables the Rx Sync Interrupt.

- **TXSYN: Tx Sync Interrupt Enable**

0: No effect.

1: Enables the Tx Sync Interrupt.

- **CP1: Compare 1 Interrupt Enable**

0: No effect.

1: Enables the Compare 1 Interrupt.

- **CP0: Compare 0 Interrupt Enable**

0: No effect.

1: Enables the Compare 0 Interrupt.

- **RXBUFF: Receive Buffer Full Interrupt Enable**

0: No effect.

1: Enables the Receive Buffer Full Interrupt.

- **ENDRX: End of Reception Interrupt Enable**

0: No effect.

1: Enables the End of Reception Interrupt.

- **OVRUN: Receive Overrun Interrupt Enable**

0: No effect.

1: Enables the Receive Overrun Interrupt.

- **RXRDY: Receive Ready Interrupt Enable**

0: No effect.

1: Enables the Receive Ready Interrupt.

- **TXBUFE: Transmit Buffer Empty Interrupt Enable**

0: No effect.

1: Enables the Transmit Buffer Empty Interrupt

- **ENDTX: End of Transmission Interrupt Enable**

0: No effect.

1: Enables the End of Transmission Interrupt.

- **TXEMPTY: Transmit Empty Interrupt Enable**

0: No effect.

1: Enables the Transmit Empty Interrupt.

- **TXRDY: Transmit Ready Interrupt Enable**

0: No effect.

1: Enables the Transmit Ready Interrupt.

23.9.15 Interrupt Disable Register

Name: IDR

Access Type: Write-only

Offset: 0x48

Reset value: -

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	RXSYN	TXSYN	CP1	CP0
7	6	5	4	3	2	1	0
RXBUFF	ENDRX	OVRUN	RXRDY	TXBUFE	ENDTX	TXEMPTY	TXRDY

- **RXSYN: Rx Sync Interrupt Enable**

0: No effect.

1: Disables the Rx Sync Interrupt.

- **TXSYN: Tx Sync Interrupt Enable**

0: No effect.

1: Disables the Tx Sync Interrupt.

- **CP1: Compare 1 Interrupt Disable**

0: No effect.

1: Disables the Compare 1 Interrupt.

- **CP0: Compare 0 Interrupt Disable**

0: No effect.

1: Disables the Compare 0 Interrupt.

- **RXBUFF: Receive Buffer Full Interrupt Disable**

0: No effect.

1: Disables the Receive Buffer Full Interrupt.

- **ENDRX: End of Reception Interrupt Disable**

0: No effect.

1: Disables the End of Reception Interrupt.

- **OVRUN: Receive Overrun Interrupt Disable**

0: No effect.

1: Disables the Receive Overrun Interrupt.

- **RXRDY: Receive Ready Interrupt Disable**

0: No effect.

1: Disables the Receive Ready Interrupt.

- **TXBUFE: Transmit Buffer Empty Interrupt Disable**

0: No effect.

1: Disables the Transmit Buffer Empty Interrupt.

- **ENDTX: End of Transmission Interrupt Disable**

0: No effect.

1: Disables the End of Transmission Interrupt.

- **TXEMPTY: Transmit Empty Interrupt Disable**

0: No effect.

1: Disables the Transmit Empty Interrupt.

- **TXRDY: Transmit Ready Interrupt Disable**

0: No effect.

1: Disables the Transmit Ready Interrupt.

23.9.16 Interrupt Mask Register

Name: IMR

Access Type: Read-only

Offset: 0x4C

Reset value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	RXSYN	TXSYN	CP1	CP0
7	6	5	4	3	2	1	0
RXBUFF	ENDRX	OVRUN	RXRDY	TXBUFE	ENDTX	TXEMPTY	TXRDY

- **RXSYN: Rx Sync Interrupt Mask**

0: The Rx Sync Interrupt is disabled.

1: The Rx Sync Interrupt is enabled.

- **TXSYN: Tx Sync Interrupt Mask**

0: The Tx Sync Interrupt is disabled.

1: The Tx Sync Interrupt is enabled.

- **CP1: Compare 1 Interrupt Mask**

0: The Compare 1 Interrupt is disabled.

1: The Compare 1 Interrupt is enabled.

- **CP0: Compare 0 Interrupt Mask**

0: The Compare 0 Interrupt is disabled.

1: The Compare 0 Interrupt is enabled.

- **RXBUFF: Receive Buffer Full Interrupt Mask**

0: The Receive Buffer Full Interrupt is disabled.

1: The Receive Buffer Full Interrupt is enabled.

- **ENDRX: End of Reception Interrupt Mask**

0: The End of Reception Interrupt is disabled.

1: The End of Reception Interrupt is enabled.

- **OVRUN: Receive Overrun Interrupt Mask**

0: The Receive Overrun Interrupt is disabled.

1: The Receive Overrun Interrupt is enabled.

- **RXRDY: Receive Ready Interrupt Mask**

0: The Receive Ready Interrupt is disabled.

24. Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

Rev: 3.0.2.3

24.1 Features

- **Programmable Baud Rate Generator**
- **5- to 9-bit Full-duplex Synchronous or Asynchronous Serial Communications**
  - **1, 1.5 or 2 Stop Bits in Asynchronous Mode or 1 or 2 Stop Bits in Synchronous Mode**
  - **Parity Generation and Error Detection**
  - **Framing Error Detection, Overrun Error Detection**
  - **MSB- or LSB-first**
  - **Optional Break Generation and Detection**
  - **By 8 or by 16 Over-sampling Receiver Frequency**
  - **Optional Hardware Handshaking RTS-CTS**
  - **Receiver Time-out and Transmitter Timeguard**
  - **Optional Multidrop Mode with Address Generation and Detection**
- **RS485 with Driver Control Signal**
- **ISO7816, T = 0 or T = 1 Protocols for Interfacing with Smart Cards**
  - **NACK Handling, Error Counter with Repetition and Iteration Limit**
- **IrDA Modulation and Demodulation**
  - **Communication at up to 115.2 Kbps**
- **Test Modes**
  - **Remote Loopback, Local Loopback, Automatic Echo**
- **Supports Connection of Two Peripheral DMA Controller Channels (PDC)**
- **Offers Buffer Transfer without Processor Intervention**

24.2 Overview

The Universal Synchronous Asynchronous Receiver Transceiver (USART) provides one full duplex universal synchronous asynchronous serial link. Data frame format is widely programmable (data length, parity, number of stop bits) to support a maximum of standards. The receiver implements parity error, framing error and overrun error detection. The receiver time-out enables handling variable-length frames and the transmitter timeguard facilitates communications with slow remote devices. Multidrop communications are also supported through address bit handling in reception and transmission.

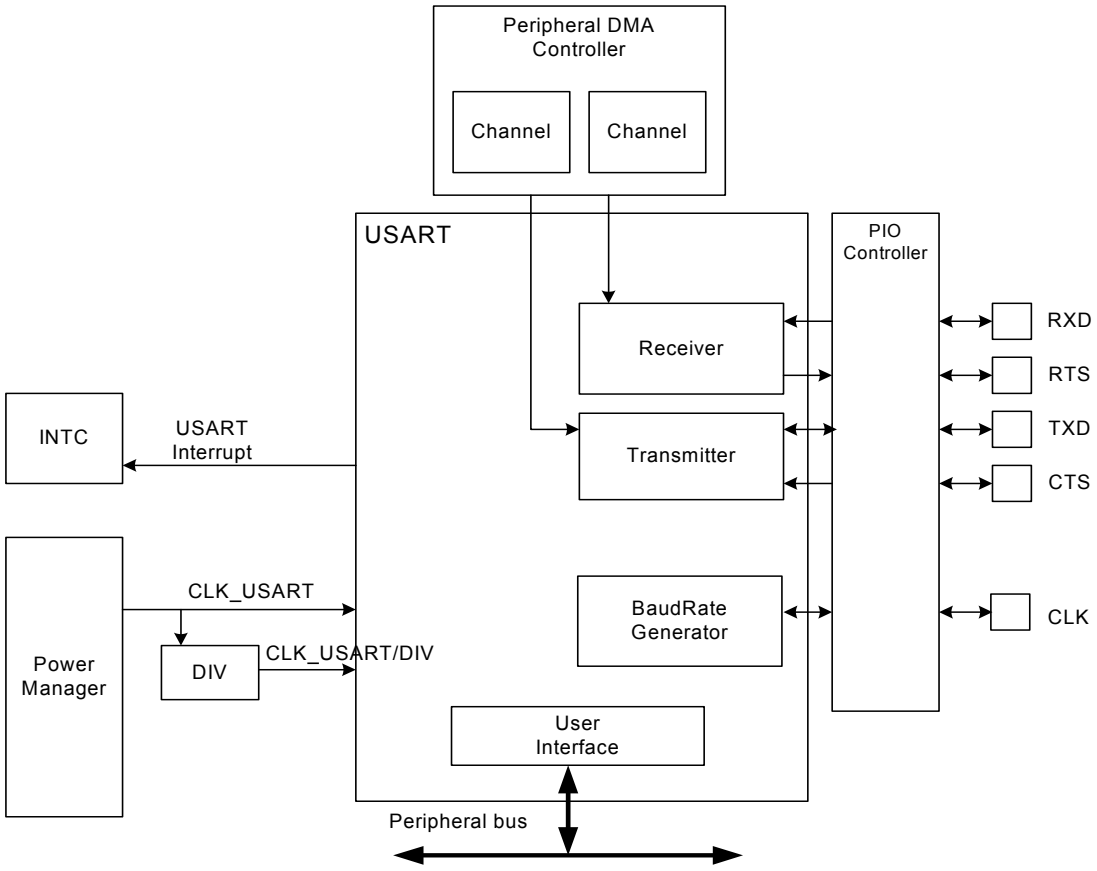
The USART features three test modes: remote loopback, local loopback and automatic echo.

The USART supports specific operating modes providing interfaces on RS485 buses, with ISO7816 T = 0 or T = 1 smart card slots and infrared transceivers. The hardware handshaking feature enables an out-of-band flow control by automatic management of the pins RTS and CTS.

The USART supports the connection to the Peripheral DMA Controller, which enables data transfers to the transmitter and from the receiver. The PDC provides chained buffer management without any intervention of the processor.

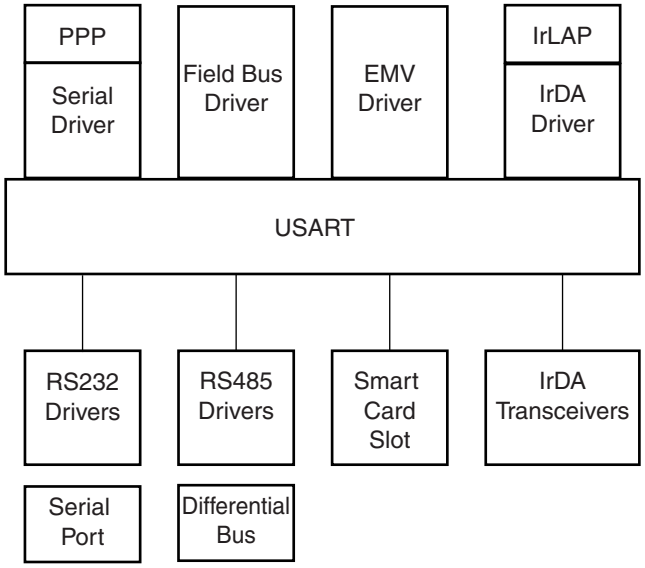
24.3 Block Diagram

Figure 24-1. USART Block Diagram



24.4 Application Block Diagram

Figure 24-2. Application Block Diagram



24.5 I/O Lines Description

Table 24-1. I/O Line Description

Name	Description	Type	Active Level
CLK	Serial Clock	I/O	
TXD	Transmit Serial Data	I/O	
RXD	Receive Serial Data	Input	
CTS	Clear to Send	Input	Low
RTS	Request to Send	Output	Low

24.6 Product Dependencies

24.6.1 I/O Lines

The pins used for interfacing the USART may be multiplexed with the PIO lines. The programmer must first program the PIO controller to assign the desired USART pins to their peripheral function. If I/O lines of the USART are not used by the application, they can be used for other purposes by the PIO Controller.

To prevent the TXD line from falling when the USART is disabled, the use of an internal pull up is mandatory.

24.6.2 Power Manager (PM)

The USART is not continuously clocked. The programmer must ensure that the USART clock is enabled in the Power Manager (PM) before using the USART. However, if the application does not require USART operations, the USART clock can be stopped when not needed and be restarted later. In this case, the USART will resume its operations where it left off. USART clock (CLK_USART) in the USART description is the clock for the peripheral bus to which the USART is connected.

24.6.3 Interrupt

The USART interrupt line is connected on one of the internal sources of the Interrupt Controller. Using the USART interrupt requires the interrupt controller to be programmed first.

24.7 Functional Description

The USART is capable of managing several types of serial synchronous or asynchronous communications.

It supports the following communication modes:

- 5- to 9-bit full-duplex asynchronous serial communication
  - MSB- or LSB-first
  - 1, 1.5 or 2 stop bits
  - Parity even, odd, marked, space or none
  - By 8 or by 16 over-sampling receiver frequency
  - Optional hardware handshaking
  - Optional break management
  - Optional multidrop serial communication
- High-speed 5- to 9-bit full-duplex synchronous serial communication
  - MSB- or LSB-first
  - 1 or 2 stop bits
  - Parity even, odd, marked, space or none
  - By 8 or by 16 over-sampling frequency
  - Optional hardware handshaking
  - Optional break management
  - Optional multidrop serial communication
- RS485 with driver control signal
- ISO7816, T0 or T1 protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- InfraRed IrDA Modulation and Demodulation
- Test modes
  - Remote loopback, local loopback, automatic echo

24.7.1 Baud Rate Generator

The Baud Rate Generator provides the bit period clock named the Baud Rate Clock to both the receiver and the transmitter.

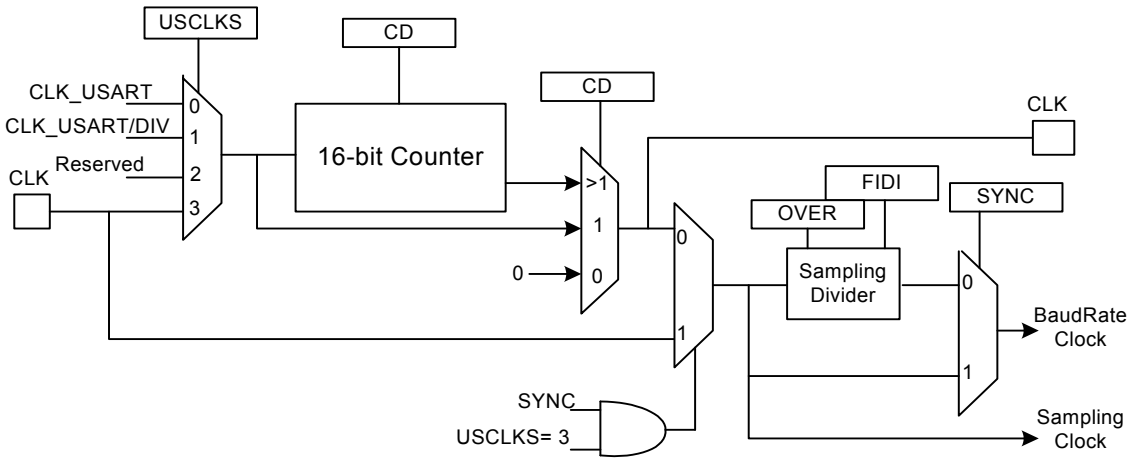
The Baud Rate Generator clock source can be selected by setting the USCLKS field in the Mode Register (MR) between:

- the CLK_USART
- a division of the CLK_USART, the divider being product dependent, but generally set to 8
- the external clock, available on the CLK pin

The Baud Rate Generator is based upon a 16-bit divider, which is programmed with the CD field of the Baud Rate Generator Register (BRGR). If CD is programmed at 0, the Baud Rate Generator does not generate any clock. If CD is programmed at 1, the divider is bypassed and becomes inactive.

If the external CLK clock is selected, the duration of the low and high levels of the signal provided on the CLK pin must be longer than a CLK_USART period. The frequency of the signal provided on CLK must be at least 4.5 times lower than CLK_USART.

Figure 24-3. Baud Rate Generator



24.7.1.1 *Baud Rate in Asynchronous Mode*

If the USART is programmed to operate in asynchronous mode, the selected clock is first divided by CD, which is field programmed in the Baud Rate Generator Register (BRGR). The resulting clock is provided to the receiver as a sampling clock and then divided by 16 or 8, depending on the programming of the OVER bit in MR.

If OVER is set to 1, the receiver sampling is 8 times higher than the baud rate clock. If OVER is cleared, the sampling is performed at 16 times the baud rate clock.

The following formula performs the calculation of the Baud Rate.

$$Baudrate = \frac{SelectedClock}{(8(2 - Over)CD)}$$

This gives a maximum baud rate of CLK_USART divided by 8, assuming that CLK_USART is the highest possible clock and that OVER is programmed at 1.

24.7.1.2 *Baud Rate Calculation Example*

Table 24-2 shows calculations of CD to obtain a baud rate at 38400 bauds for different source clock frequencies. This table also shows the actual resulting baud rate and the error.

Table 24-2. Baud Rate Example (OVER = 0)

Source Clock	Expected Baud Rate	Calculation Result	CD	Actual Baud Rate	Error
MHz	Bit/s			Bit/s	
3 686 400	38 400	6.00	6	38 400.00	0.00%
4 915 200	38 400	8.00	8	38 400.00	0.00%
5 000 000	38 400	8.14	8	39 062.50	1.70%

Table 24-2. Baud Rate Example (OVER = 0) (Continued)

Source Clock	Expected Baud Rate	Calculation Result	CD	Actual Baud Rate	Error
7 372 800	38 400	12.00	12	38 400.00	0.00%
8 000 000	38 400	13.02	13	38 461.54	0.16%
12 000 000	38 400	19.53	20	37 500.00	2.40%
12 288 000	38 400	20.00	20	38 400.00	0.00%
14 318 180	38 400	23.30	23	38 908.10	1.31%
14 745 600	38 400	24.00	24	38 400.00	0.00%
18 432 000	38 400	30.00	30	38 400.00	0.00%
24 000 000	38 400	39.06	39	38 461.54	0.16%
24 576 000	38 400	40.00	40	38 400.00	0.00%
25 000 000	38 400	40.69	40	38 109.76	0.76%
32 000 000	38 400	52.08	52	38 461.54	0.16%
32 768 000	38 400	53.33	53	38 641.51	0.63%
33 000 000	38 400	53.71	54	38 194.44	0.54%
40 000 000	38 400	65.10	65	38 461.54	0.16%
50 000 000	38 400	81.38	81	38 580.25	0.47%
60 000 000	38 400	97.66	98	38 265.31	0.35%
70 000 000	38 400	113.93	114	38 377.19	0.06%

The baud rate is calculated with the following formula:

$$BaudRate = (CLKUSART)/CD \times 16$$

The baud rate error is calculated with the following formula. It is not recommended to work with an error higher than 5%.

$$Error = 1 - \left(\frac{ExpectedBaudRate}{ActualBaudRate}\right)$$

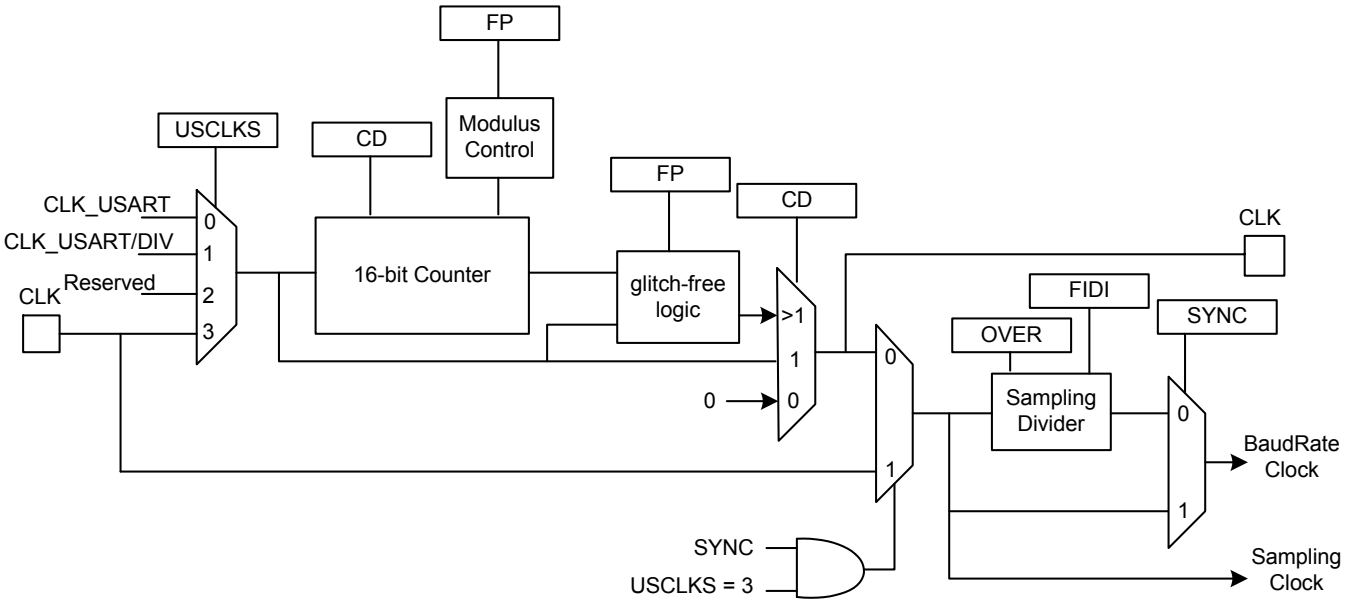
24.7.1.3 Fractional Baud Rate in Asynchronous Mode

The Baud Rate generator previously defined is subject to the following limitation: the output frequency changes by only integer multiples of the reference frequency. An approach to this problem is to integrate a fractional N clock generator that has a high resolution. The generator architecture is modified to obtain Baud Rate changes by a fraction of the reference source clock. This fractional part is programmed with the FP field in the Baud Rate Generator Register (BRGR). If FP is not 0, the fractional part is activated. The resolution is one eighth of the clock divider. This feature is only available when using USART normal mode. The fractional Baud Rate is calculated using the following formula:

$$Baudrate = \frac{SelectedClock}{\left(8(2 - Over)\left(CD + \frac{FP}{8}\right)\right)}$$

The modified architecture is presented below:

Figure 24-4. Fractional Baud Rate Generator



24.7.1.4 Baud Rate in Synchronous Mode

If the USART is programmed to operate in synchronous mode, the selected clock is simply divided by the field CD in BRGR.

$$BaudRate = \frac{SelectedClock}{CD}$$

In synchronous mode, if the external clock is selected (USCLKS = 3), the clock is provided directly by the signal on the USART CLK pin. No division is active. The value written in BRGR has no effect. The external clock frequency must be at least 4.5 times lower than the system clock.

When either the external clock CLK or the internal clock divided (CLK_USART/DIV) is selected, the value programmed in CD must be even if the user has to ensure a 50:50 mark/space ratio on the CLK pin. If the internal clock CLK_USART is selected, the Baud Rate Generator ensures a 50:50 duty cycle on the CLK pin, even if the value programmed in CD is odd.

24.7.1.5 Baud Rate in ISO 7816 Mode

The ISO7816 specification defines the bit rate with the following formula:

$$B = \frac{Di}{Fi} \times f$$

where:

- B is the bit rate
- Di is the bit-rate adjustment factor
- Fi is the clock frequency division factor
- f is the ISO7816 clock frequency (Hz)

Di is a binary value encoded on a 4-bit field, named DI, as represented in Table 24-3.

Table 24-3. Binary and Decimal Values for Di

DI field	0001	0010	0011	0100	0101	0110	1000	1001
Di (decimal)	1	2	4	8	16	32	12	20

Fi is a binary value encoded on a 4-bit field, named FI, as represented in Table 24-4.

Table 24-4. Binary and Decimal Values for Fi

FI field	0000	0001	0010	0011	0100	0101	0110	1001	1010	1011	1100	1101
Fi (decimal	372	372	558	744	1116	1488	1860	512	768	1024	1536	2048

Table 24-5 shows the resulting Fi/Di Ratio, which is the ratio between the ISO7816 clock and the baud rate clock.

Table 24-5. Possible Values for the Fi/Di Ratio

Fi/Di	372	558	774	1116	1488	1806	512	768	1024	1536	2048
1	372	558	744	1116	1488	1860	512	768	1024	1536	2048
2	186	279	372	558	744	930	256	384	512	768	1024
4	93	139.5	186	279	372	465	128	192	256	384	512
8	46.5	69.75	93	139.5	186	232.5	64	96	128	192	256
16	23.25	34.87	46.5	69.75	93	116.2	32	48	64	96	128
32	11.62	17.43	23.25	34.87	46.5	58.13	16	24	32	48	64
12	31	46.5	62	93	124	155	42.66	64	85.33	128	170.6
20	18.6	27.9	37.2	55.8	74.4	93	25.6	38.4	51.2	76.8	102.4

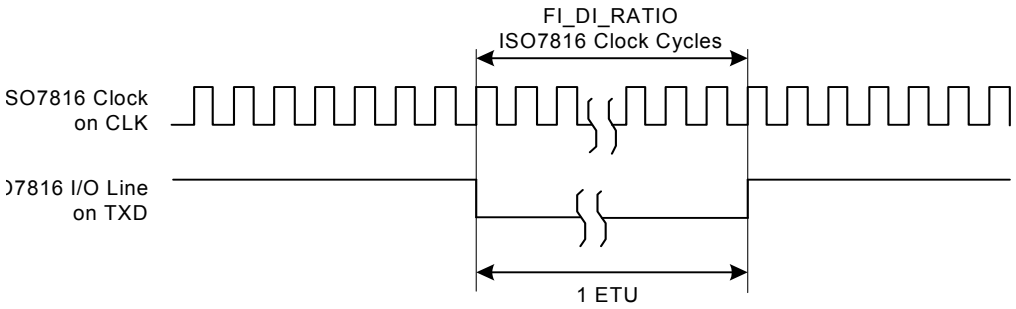
If the USART is configured in ISO7816 Mode, the clock selected by the USCLKS field in the Mode Register (MR) is first divided by the value programmed in the field CD in the Baud Rate Generator Register (BRGR). The resulting clock can be provided to the CLK pin to feed the smart card clock inputs. This means that the CLKO bit can be set in MR.

This clock is then divided by the value programmed in the FI_DI_RATIO field in the FI_DI_Ratio register (FIDI). This is performed by the Sampling Divider, which performs a division by up to 2047 in ISO7816 Mode. The non-integer values of the Fi/Di Ratio are not supported and the user must program the FI_DI_RATIO field to a value as close as possible to the expected value.

The FI_DI_RATIO field resets to the value 0x174 (372 in decimal) and is the most common divider between the ISO7816 clock and the bit rate (Fi = 372, Di = 1).

Figure 24-5 shows the relation between the Elementary Time Unit, corresponding to a bit time, and the ISO 7816 clock.

Figure 24-5. Elementary Time Unit (ETU)



24.7.2 Receiver and Transmitter Control

After reset, the receiver is disabled. The user must enable the receiver by setting the RXEN bit in the Control Register (CR). However, the receiver registers can be programmed before the receiver clock is enabled.

After reset, the transmitter is disabled. The user must enable it by setting the TXEN bit in the Control Register (CR). However, the transmitter registers can be programmed before being enabled.

The Receiver and the Transmitter can be enabled together or independently.

At any time, the software can perform a reset on the receiver or the transmitter of the USART by setting the corresponding bit, RSTRX and RSTTX respectively, in the Control Register (CR). The reset commands have the same effect as a hardware reset on the corresponding logic. Regardless of what the receiver or the transmitter is performing, the communication is immediately stopped.

The user can also independently disable the receiver or the transmitter by setting RXDIS and TXDIS respectively in CR. If the receiver is disabled during a character reception, the USART waits until the end of reception of the current character, then the reception is stopped. If the transmitter is disabled while it is operating, the USART waits the end of transmission of both the current character and character being stored in the Transmit Holding Register (THR). If a time-guard is programmed, it is handled normally.

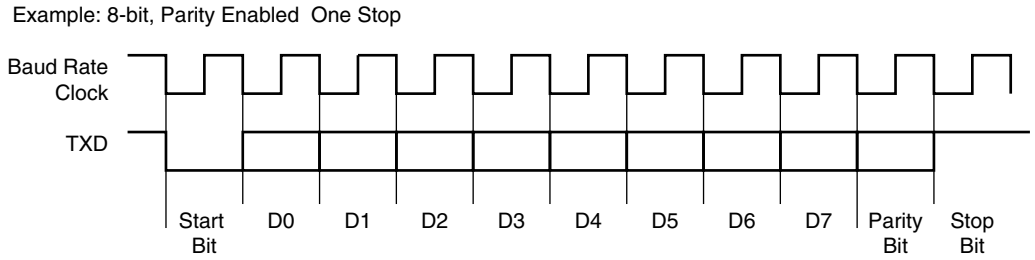
24.7.3 Synchronous and Asynchronous Modes

24.7.3.1 Transmitter Operations

The transmitter performs the same in both synchronous and asynchronous operating modes (SYNC = 0 or SYNC = 1). One start bit, up to 9 data bits, one optional parity bit and up to two stop bits are successively shifted out on the TXD pin at each falling edge of the programmed serial clock.

The number of data bits is selected by the CHRL field and the MODE 9 bit in the Mode Register (MR). Nine bits are selected by setting the MODE 9 bit regardless of the CHRL field. The parity bit is set according to the PAR field in MR. The even, odd, space, marked or none parity bit can be configured. The MSBF field in MR configures which data bit is sent first. If written at 1, the most significant bit is sent first. At 0, the less significant bit is sent first. The number of stop bits is selected by the NBSTOP field in MR. The 1.5 stop bit is supported in asynchronous mode only.

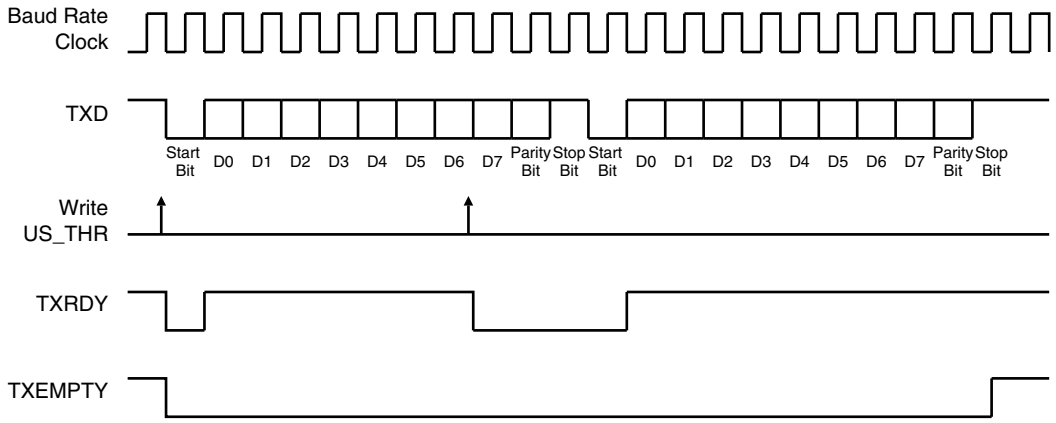
Figure 24-6. Character Transmit



The characters are sent by writing in the Transmit Holding Register (THR). The transmitter reports two status bits in the Channel Status Register (CSR): TXRDY (Transmitter Ready), which indicates that THR is empty and TXEMPTY, which indicates that all the characters written in THR have been processed. When the current character processing is completed, the last character written in THR is transferred into the Shift Register of the transmitter and THR becomes empty, thus TXRDY raises.

Both TXRDY and TXEMPTY bits are low since the transmitter is disabled. Writing a character in THR while TXRDY is active has no effect and the written character is lost.

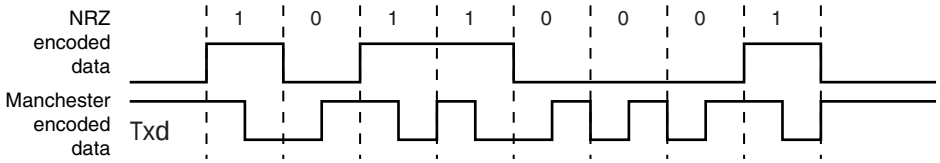
Figure 24-7. Transmitter Status



24.7.3.2 Manchester Encoder

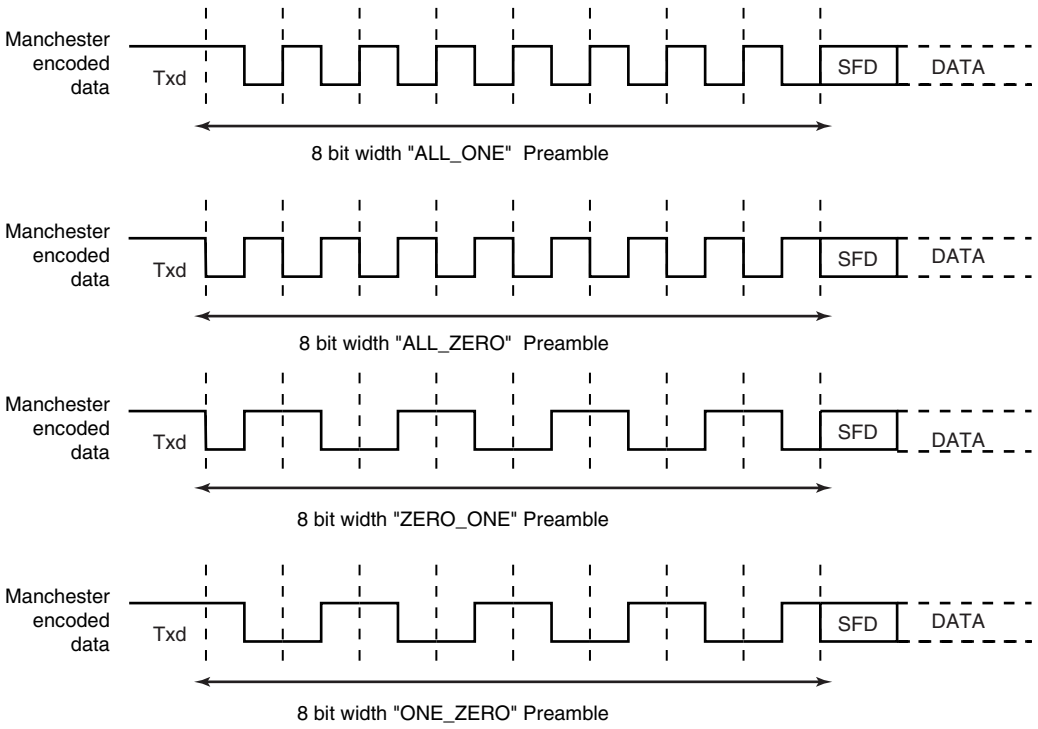
When the Manchester encoder is in use, characters transmitted through the USART are encoded based on biphase Manchester II format. To enable this mode, set the MAN field in the MR register to 1. Depending on polarity configuration, a logic level (zero or one), is transmitted as a coded signal one-to-zero or zero-to-one. Thus, a transition always occurs at the midpoint of each bit time. It consumes more bandwidth than the original NRZ signal (2x) but the receiver has more error control since the expected input must show a change at the center of a bit cell. An example of Manchester encoded sequence is: the byte 0xB1 or 10110001 encodes to 10 01 10 10 01 01 01 10, assuming the default polarity of the encoder. Figure 24-8 illustrates this coding scheme.

Figure 24-8. NRZ to Manchester Encoding



The Manchester encoded character can also be encapsulated by adding both a configurable preamble and a start frame delimiter pattern. Depending on the configuration, the preamble is a training sequence, composed of a pre-defined pattern with a programmable length from 1 to 15 bit times. If the preamble length is set to 0, the preamble waveform is not generated prior to any character. The preamble pattern is chosen among the following sequences: ALL_ONE, ALL_ZERO, ONE_ZERO or ZERO_ONE, writing the field TX_PP in the MAN register, the field TX_PL is used to configure the preamble length. Figure 24-9 illustrates and defines the valid patterns. To improve flexibility, the encoding scheme can be configured using the TX_MPOL field in the MAN register. If the TX_MPOL field is set to zero (default), a logic zero is encoded with a zero-to-one transition and a logic one is encoded with a one-to-zero transition. If the TX_MPOL field is set to one, a logic one is encoded with a one-to-zero transition and a logic zero is encoded with a zero-to-one transition.

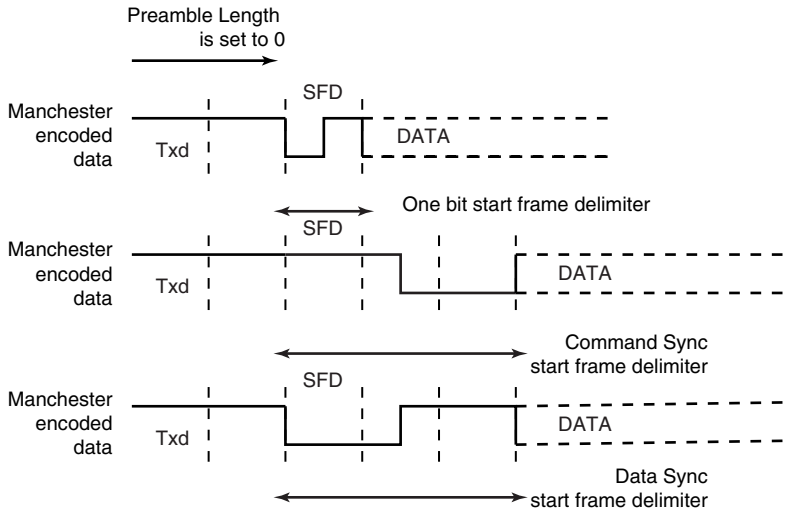
Figure 24-9. Preamble Patterns, Default Polarity Assumed



A start frame delimiter is to be configured using the ONEBIT field in the MR register. It consists of a user-defined pattern that indicates the beginning of a valid data. Figure 24-10 illustrates these patterns. If the start frame delimiter, also known as start bit, is one bit, (ONEBIT at 1), a logic zero is Manchester encoded and indicates that a new character is being sent serially on the line. If the start frame delimiter is a synchronization pattern also referred to as sync (ONEBIT at 0), a sequence of 3 bit times is sent serially on the line to indicate the start of a new character.

The sync waveform is in itself an invalid Manchester waveform as the transition occurs at the middle of the second bit time. Two distinct sync patterns are used: the command sync and the data sync. The command sync has a logic one level for one and a half bit times, then a transition to logic zero for the second one and a half bit times. If the MODSYNC field in the MR register is set to 1, the next character is a command. If it is set to 0, the next character is a data. When direct memory access is used, the MODSYNC field can be immediately updated with a modified character located in memory. To enable this mode, VAR_SYNC field in MR register must be set to 1. In this case, the MODSYNC field in MR is bypassed and the sync configuration is held in the TXSYNH in the THR register. The USART character format is modified and includes sync information.

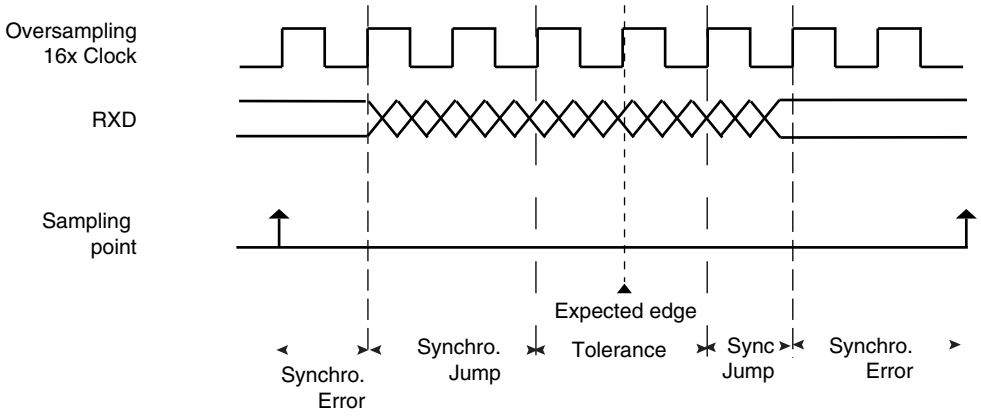
Figure 24-10. Start Frame Delimiter



24.7.3.3 Drift Compensation

Drift compensation is available only in 16X oversampling mode. An hardware recovery system allows a larger clock drift. To enable the hardware system, the bit in the MAN register must be set. If the RXD edge is one 16X clock cycle from the expected edge, this is considered as normal jitter and no corrective actions is taken. If the RXD event is between 4 and 2 clock cycles before the expected edge, then the current period is shortened by one clock cycle. If the RXD event is between 2 and 3 clock cycles after the expected edge, then the current period is lengthened by one clock cycle. These intervals are considered to be drift and so corrective actions are automatically taken.

Figure 24-11. Bit Resynchronization



24.7.3.4 Asynchronous Receiver

If the USART is programmed in asynchronous operating mode (SYNC = 0), the receiver oversamples the RXD input line. The oversampling is either 16 or 8 times the Baud Rate clock, depending on the OVER bit in the Mode Register (MR).

The receiver samples the RXD line. If the line is sampled during one half of a bit time at 0, a start bit is detected and data, parity and stop bits are successively sampled on the bit rate clock.

If the oversampling is 16, (OVER at 0), a start is detected at the eighth sample at 0. Then, data bits, parity bit and stop bit are sampled on each 16 sampling clock cycle. If the oversampling is 8 (OVER at 1), a start bit is detected at the fourth sample at 0. Then, data bits, parity bit and stop bit are sampled on each 8 sampling clock cycle.

The number of data bits, first bit sent and parity mode are selected by the same fields and bits as the transmitter, i.e. respectively CHRL, MODE9, MSBF and PAR. The number of stop bits has no effect on the receiver as it considers only one stop bit, regardless of the field NBSTOP, so that resynchronization between the receiver and the transmitter can occur. Moreover, as soon as the stop bit is sampled, the receiver starts looking for a new start bit so that resynchronization can also be accomplished when the transmitter is operating with one stop bit.

Figure 24-12 and Figure 24-13 illustrate start detection and character reception when USART operates in asynchronous mode.

Figure 24-12. Asynchronous Start Detection

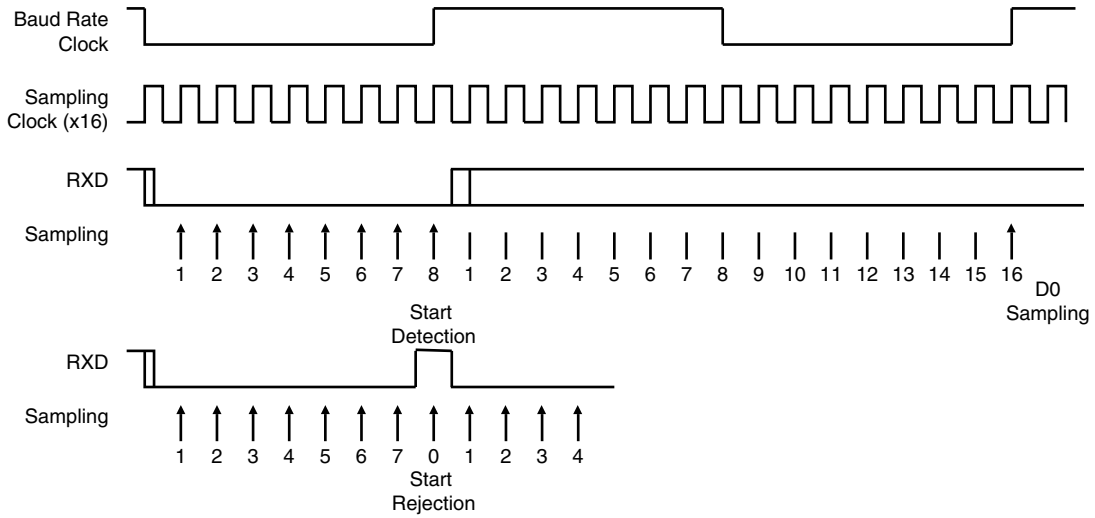
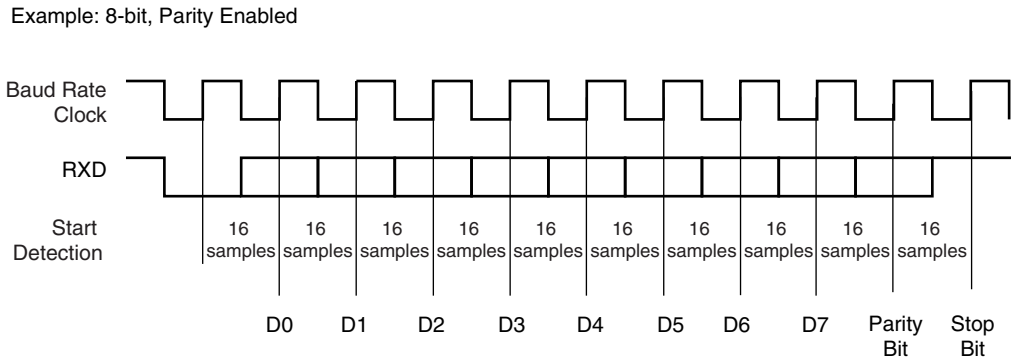


Figure 24-13. Asynchronous Character Reception



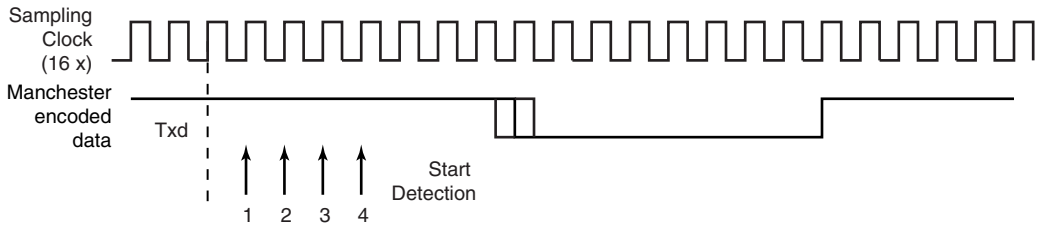
24.7.3.5 Manchester Decoder

When the MAN field in MR register is set to 1, the Manchester decoder is enabled. The decoder performs both preamble and start frame delimiter detection. One input line is dedicated to Manchester encoded input data.

An optional preamble sequence can be defined, its length is user-defined and totally independent of the emitter side. Use RX_PL in MAN register to configure the length of the preamble sequence. If the length is set to 0, no preamble is detected and the function is disabled. In addition, the polarity of the input stream is programmable with RX_MPOL field in MAN register. Depending on the desired application the preamble pattern matching is to be defined via the RX_PP field in MAN. See Figure 24-9 for available preamble patterns.

Unlike preamble, the start frame delimiter is shared between Manchester Encoder and Decoder. So, if ONEBIT field is set to 1, only a zero encoded Manchester can be detected as a valid start frame delimiter. If ONEBIT is set to 0, only a sync pattern is detected as a valid start frame delimiter. Decoder operates by detecting transition on incoming stream. If RXD is sampled during one quarter of a bit time at zero, a start bit is detected. See Figure 24-14. The sample pulse rejection mechanism applies.

Figure 24-14. Asynchronous Start Bit Detection



The receiver is activated and starts Preamble and Frame Delimiter detection, sampling the data at one quarter and then three quarters. If a valid preamble pattern or start frame delimiter is detected, the receiver continues decoding with the same synchronization. If the stream does not match a valid pattern or a valid start frame delimiter, the receiver re-synchronizes on the next valid edge.The minimum time threshold to estimate the bit value is three quarters of a bit time.

If a valid preamble (if used) followed with a valid start frame delimiter is detected, the incoming stream is decoded into NRZ data and passed to USART for processing. Figure 24-15 illustrates Manchester pattern mismatch. When incoming data stream is passed to the USART, the receiver is also able to detect Manchester code violation. A code violation is a lack of transition in the middle of a bit cell. In this case, MANE flag in CSR register is raised. It is cleared by writing the Control Register (CR) with the RSTSTA bit at 1. See Figure 24-16 for an example of Manchester error detection during data phase.

Figure 24-15. Preamble Pattern Mismatch

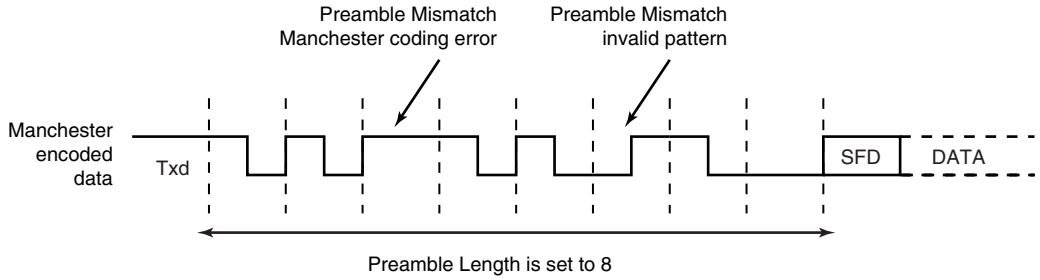
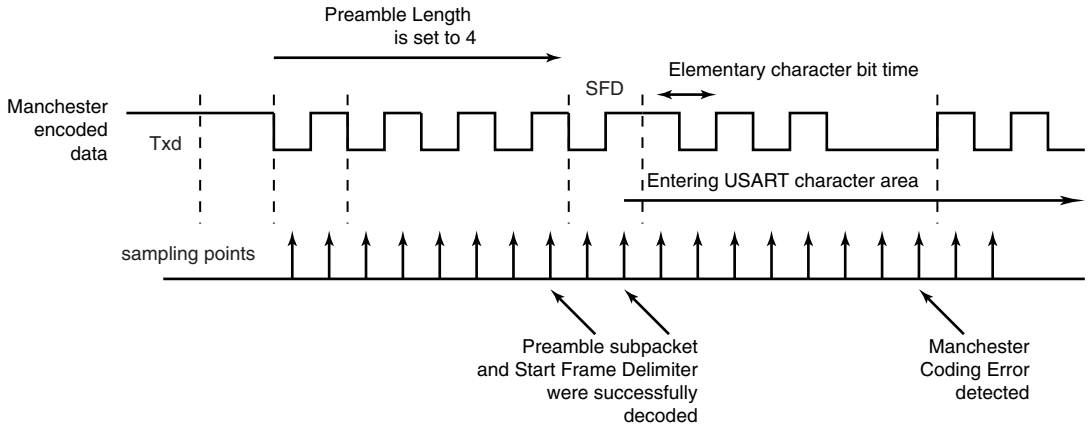


Figure 24-16. Manchester Error Flag



When the start frame delimiter is a sync pattern (ONEBIT field at 0), both command and data delimiter are supported. If a valid sync is detected, the received character is written as RXCHR

field in the RHR register and the RXSYNH is updated. RXCHR is set to 1 when the received character is a command, and it is set to 0 if the received character is a data. This mechanism alleviates and simplifies the direct memory access as the character contains its own sync field in the same register.

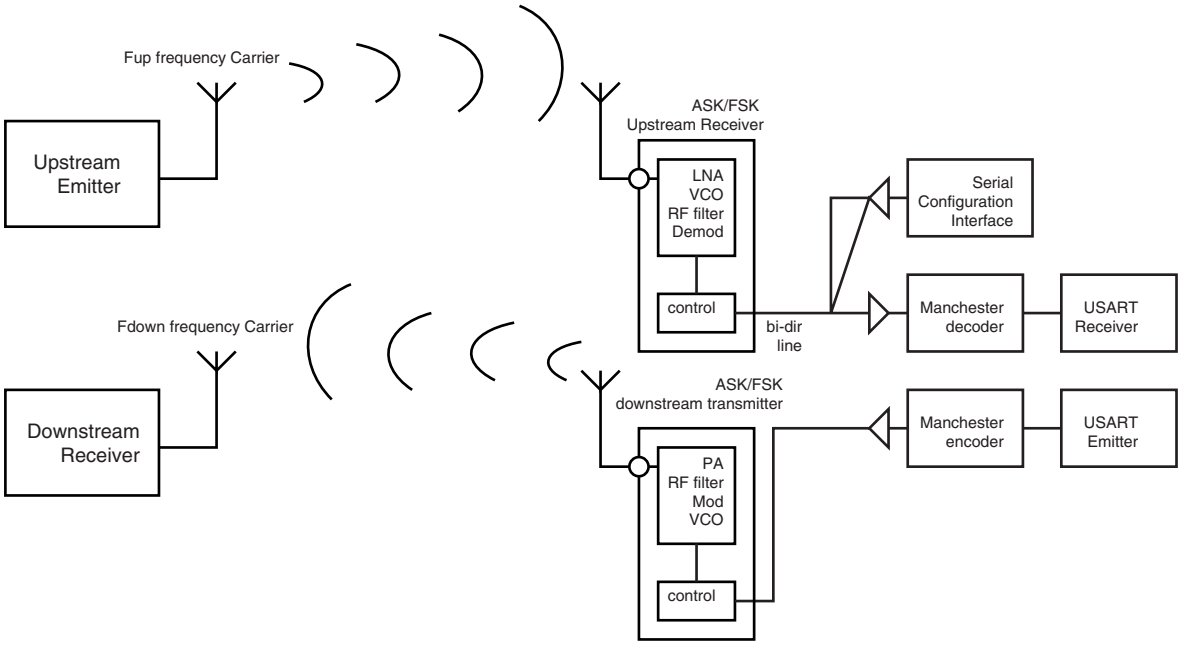
As the decoder is setup to be used in unipolar mode, the first bit of the frame has to be a zero-to-one transition.

24.7.3.6 *Radio Interface: Manchester Encoded USART Application*

This section describes low data rate RF transmission systems and their integration with a Manchester encoded USART. These systems are based on transmitter and receiver ICs that support ASK and FSK modulation schemes.

The goal is to perform full duplex radio transmission of characters using two different frequency carriers. See the configuration in Figure 24-17.

Figure 24-17. Manchester Encoded Characters RF Transmission



The USART module is configured as a Manchester encoder/decoder. Looking at the downstream communication channel, Manchester encoded characters are serially sent to the RF emitter. This may also include a user defined preamble and a start frame delimiter. Mostly, preamble is used in the RF receiver to distinguish between a valid data from a transmitter and signals due to noise. The Manchester stream is then modulated. See Figure 24-18 for an example of ASK modulation scheme. When a logic one is sent to the ASK modulator, the power amplifier, referred to as PA, is enabled and transmits an RF signal at downstream frequency. When a logic zero is transmitted, the RF signal is turned off. If the FSK modulator is activated, two different frequencies are used to transmit data. When a logic 1 is sent, the modulator outputs an RF signal at frequency F0 and switches to F1 if the data sent is a 0. See Figure 24-19.

From the receiver side, another carrier frequency is used. The RF receiver performs a bit check operation examining demodulated data stream. If a valid pattern is detected, the receiver switches to receiving mode. The demodulated stream is sent to the Manchester decoder. Because of bit checking inside RF IC, the data transferred to the microcontroller is reduced by a

user-defined number of bits. The Manchester preamble length is to be defined in accordance with the RF IC configuration.

Figure 24-18. ASK Modulator Output

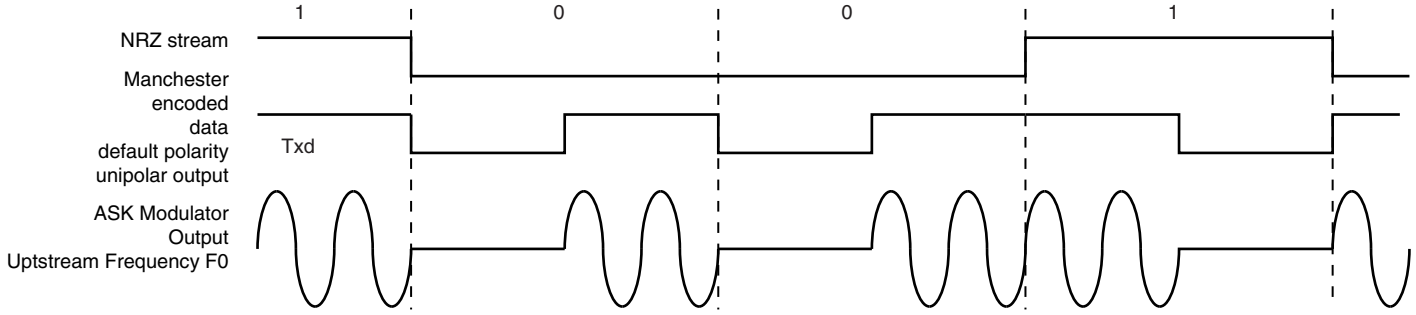
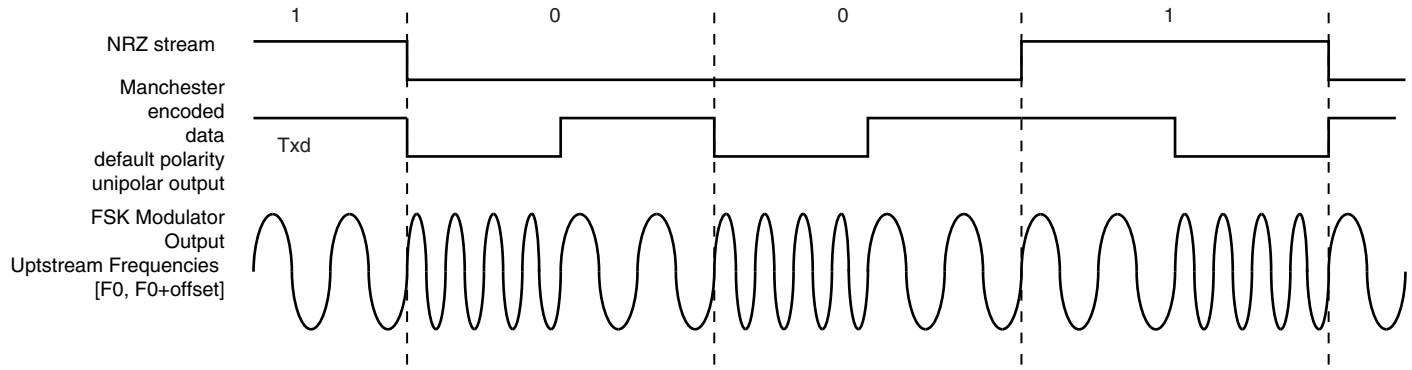


Figure 24-19. FSK Modulator Output



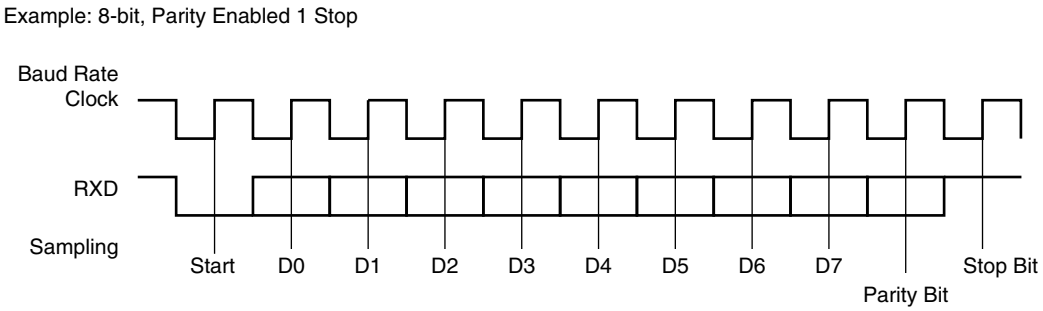
24.7.3.7 Synchronous Receiver

In synchronous mode (SYNC = 1), the receiver samples the RXD signal on each rising edge of the Baud Rate Clock. If a low level is detected, it is considered as a start. All data bits, the parity bit and the stop bits are sampled and the receiver waits for the next start bit. Synchronous mode operations provide a high speed transfer capability.

Configuration fields and bits are the same as in asynchronous mode.

Figure 24-20 illustrates a character reception in synchronous mode.

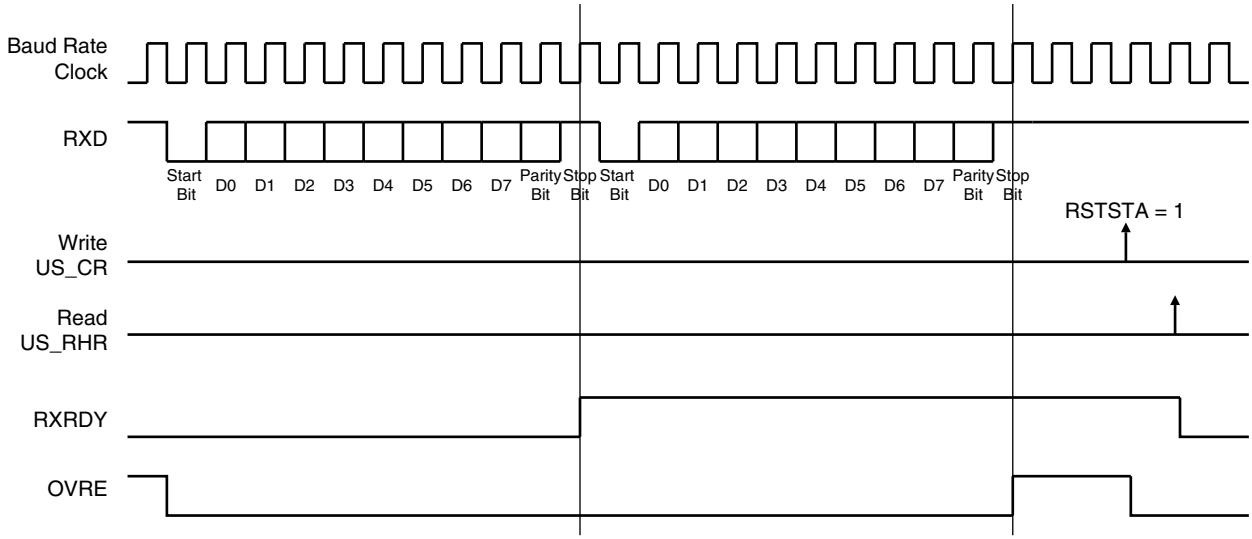
Figure 24-20. Synchronous Mode Character Reception



24.7.3.8 Receiver Operations

When a character reception is completed, it is transferred to the Receive Holding Register (RHR) and the RXRDY bit in the Status Register (CSR) rises. If a character is completed while the RXRDY is set, the OVRE (Overrun Error) bit is set. The last character is transferred into RHR and overwrites the previous one. The OVRE bit is cleared by writing the Control Register (CR) with the RSTSTA (Reset Status) bit at 1.

Figure 24-21. Receiver Status



24.7.3.9 Parity

The USART supports five parity modes selected by programming the PAR field in the Mode Register (MR). The PAR field also enables the Multidrop mode, see ”Multidrop Mode” on page 412. Even and odd parity bit generation and error detection are supported.

If even parity is selected, the parity generator of the transmitter drives the parity bit at 0 if a number of 1s in the character data bit is even, and at 1 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If odd parity is selected, the parity generator of the transmitter drives the parity bit at 1 if a number of 1s in the character data bit is even, and at 0 if the number of 1s is odd. Accordingly, the receiver parity checker counts the number of received 1s and reports a parity error if the sampled parity bit does not correspond. If the mark parity is used, the parity generator of the transmitter drives the parity bit at 1 for all characters. The receiver parity checker reports an error if the parity bit is sampled at 0. If the space parity is used, the parity generator of the transmitter drives the parity bit at 0 for all characters. The receiver parity checker reports an error if the parity bit is sampled at 1. If parity is disabled, the transmitter does not generate any parity bit and the receiver does not report any parity error.

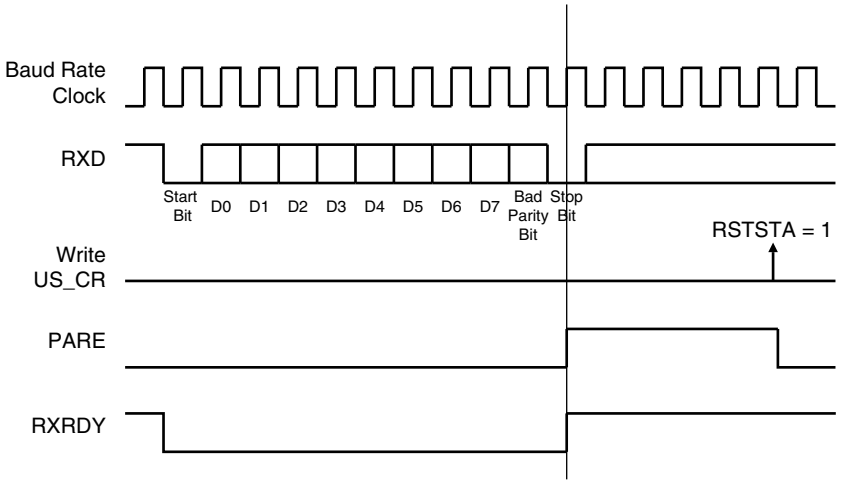
Table 24-6 shows an example of the parity bit for the character 0x41 (character ASCII “A”) depending on the configuration of the USART. Because there are two bits at 1, 1 bit is added when a parity is odd, or 0 is added when a parity is even.

Table 24-6. Parity Bit Examples

Character	Hexa	Binary	Parity Bit	Parity Mode
A	0x41	0100 0001	1	Odd
A	0x41	0100 0001	0	Even
A	0x41	0100 0001	1	Mark
A	0x41	0100 0001	0	Space
A	0x41	0100 0001	None	None

When the receiver detects a parity error, it sets the PARE (Parity Error) bit in the Channel Status Register (CSR). The PARE bit can be cleared by writing the Control Register (CR) with the RSTSTA bit at 1. Figure 24-22 illustrates the parity bit status setting and clearing.

Figure 24-22. Parity Error



24.7.3.10 Multidrop Mode

If the PAR field in the Mode Register (MR) is programmed to the value 0x6 or 0x07, the USART runs in Multidrop Mode. This mode differentiates the data characters and the address characters. Data is transmitted with the parity bit at 0 and addresses are transmitted with the parity bit at 1.

If the USART is configured in multidrop mode, the receiver sets the PARE parity error bit when the parity bit is high and the transmitter is able to send a character with the parity bit high when the Control Register is written with the SENDA bit at 1.

To handle parity error, the PARE bit is cleared when the Control Register is written with the bit RSTSTA at 1.

The transmitter sends an address byte (parity bit set) when SENDA is written to CR. In this case, the next byte written to THR is transmitted as an address. Any character written in THR without having written the command SENDA is transmitted normally with the parity at 0.

24.7.3.11 Transmitter Timeguard

The timeguard feature enables the USART interface with slow remote devices.

The timeguard function enables the transmitter to insert an idle state on the TXD line between two characters. This idle state actually acts as a long stop bit.

The duration of the idle state is programmed in the TG field of the Transmitter Timeguard Register (TTGR). When this field is programmed at zero no timeguard is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted byte during the number of bit periods programmed in TG in addition to the number of stop bits.

As illustrated in Figure 24-23, the behavior of TXRDY and TXEMPTY status bits is modified by the programming of a timeguard. TXRDY rises only when the start bit of the next character is sent, and thus remains at 0 during the timeguard transmission if a character has been written in THR. TXEMPTY remains low until the timeguard transmission is completed as the timeguard is part of the current character being transmitted.

Figure 24-23. Timeguard Operations

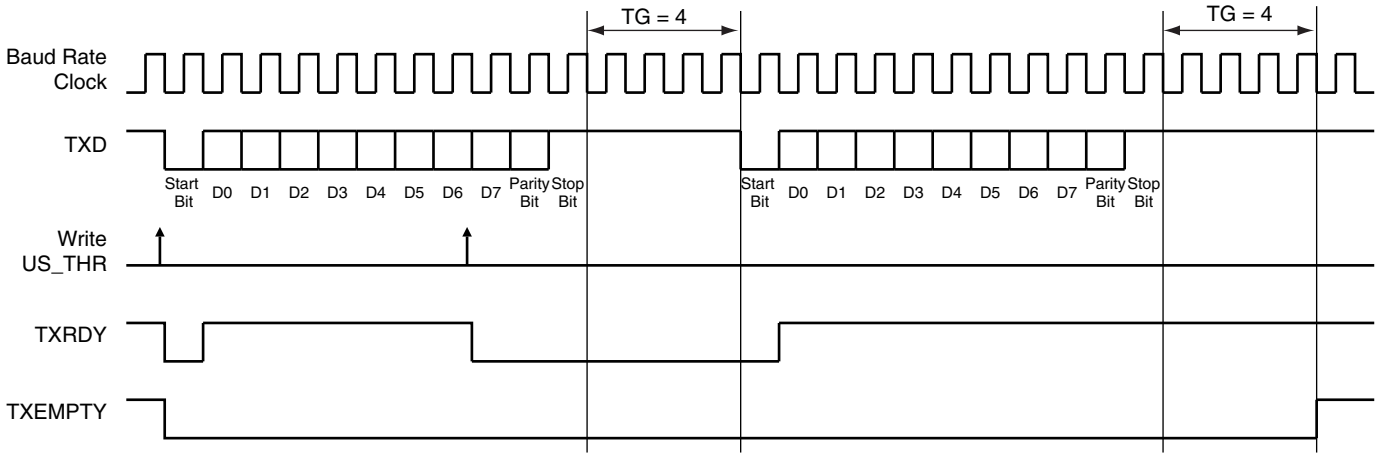


Table 24-7 indicates the maximum length of a timeguard period that the transmitter can handle in relation to the function of the Baud Rate.

Table 24-7. Maximum Timeguard Length Depending on Baud Rate

Baud Rate	Bit time	Timeguard
Bit/sec	µs	ms
1 200	833	212.50
9 600	104	26.56
14400	69.4	17.71
19200	52.1	13.28
28800	34.7	8.85
33400	29.9	7.63
56000	17.9	4.55
57600	17.4	4.43
115200	8.7	2.21

24.7.3.12 Receiver Time-out

The Receiver Time-out provides support in handling variable-length frames. This feature detects an idle condition on the RXD line. When a time-out is detected, the bit TIMEOUT in the Channel Status Register (CSR) rises and can generate an interrupt, thus indicating to the driver an end of frame.

The time-out delay period (during which the receiver waits for a new character) is programmed in the TO field of the Receiver Time-out Register (RTOR). If the TO field is programmed at 0, the Receiver Time-out is disabled and no time-out is detected. The TIMEOUT bit in CSR remains at 0. Otherwise, the receiver loads a 16-bit counter with the value programmed in TO. This counter is decremented at each bit period and reloaded each time a new character is received. If the counter reaches 0, the TIMEOUT bit in the Status Register rises.

The user can either:

•Obtain an interrupt when a time-out is detected after having received at least one character. This is performed by writing the Control Register (CR) with the STTTO (Start Time-out) bit at 1.

•Obtain a periodic interrupt while no character is received. This is performed by writing CR with the RETTO (Reload and Start Time-out) bit at 1.

If STTTO is performed, the counter clock is stopped until a first character is received. The idle state on RXD before the start of the frame does not provide a time-out. This prevents having to obtain a periodic interrupt and enables a wait of the end of frame when the idle state on RXD is detected.

If RETTO is performed, the counter starts counting down immediately from the value TO. This enables generation of a periodic interrupt so that a user time-out can be handled, for example when no key is pressed on a keyboard.

Figure 24-24 shows the block diagram of the Receiver Time-out feature.

Figure 24-24. Receiver Time-out Block Diagram

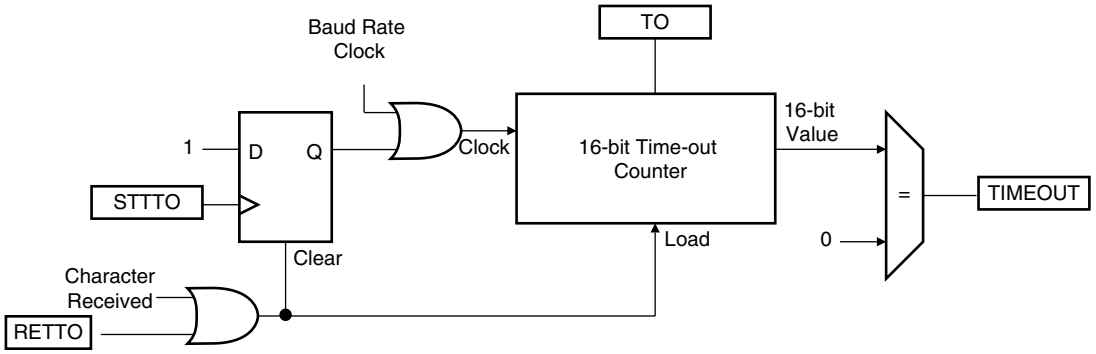


Table 24-8 gives the maximum time-out period for some standard baud rates.

Table 24-8. Maximum Time-out Period

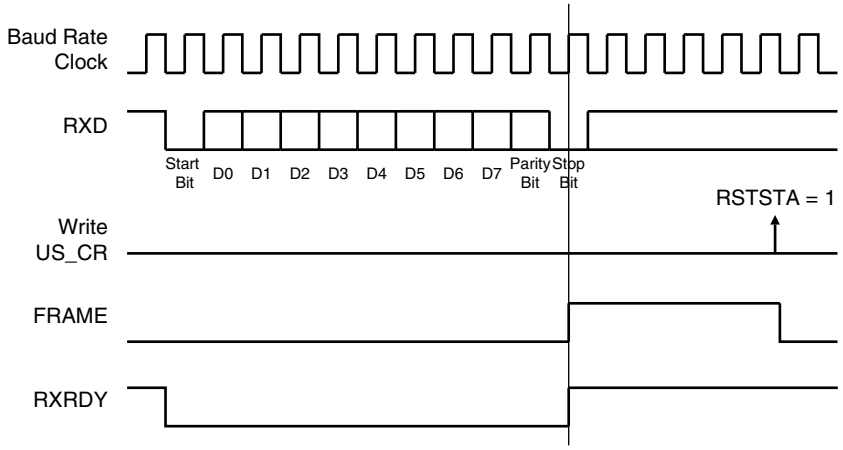
Baud Rate	Bit Time	Time-out
bit/sec	µs	ms
600	1 667	109 225
1 200	833	54 613
2 400	417	27 306
4 800	208	13 653
9 600	104	6 827
14400	69	4 551
19200	52	3 413
28800	35	2 276
33400	30	1 962
56000	18	1 170
57600	17	1 138
200000	5	328

24.7.3.13 Framing Error

The receiver is capable of detecting framing errors. A framing error happens when the stop bit of a received character is detected at level 0. This can occur if the receiver and the transmitter are fully desynchronized.

A framing error is reported on the FRAME bit of the Channel Status Register (CSR). The FRAME bit is asserted in the middle of the stop bit as soon as the framing error is detected. It is cleared by writing the Control Register (CR) with the RSTSTA bit at 1.

Figure 24-25. Framing Error Status



24.7.3.14 Transmit Break

The user can request the transmitter to generate a break condition on the TXD line. A break condition drives the TXD line low during at least one complete character. It appears the same as a 0x00 character sent with the parity and the stop bits at 0. However, the transmitter holds the TXD line at least during one character until the user requests the break condition to be removed.

A break is transmitted by writing the Control Register (CR) with the STTBRK bit at 1. This can be performed at any time, either while the transmitter is empty (no character in either the Shift Register or in THR) or when a character is being transmitted. If a break is requested while a character is being shifted out, the character is first completed before the TXD line is held low.

Once STTBRK command is requested further STTBRK commands are ignored until the end of the break is completed.

The break condition is removed by writing CR with the STPBRK bit at 1. If the STPBRK is requested before the end of the minimum break duration (one character, including start, data, parity and stop bits), the transmitter ensures that the break condition completes.

The transmitter considers the break as though it is a character, i.e. the STTBRK and STPBRK commands are taken into account only if the TXRDY bit in CSR is at 1 and the start of the break condition clears the TXRDY and TXEMPTY bits as if a character is processed.

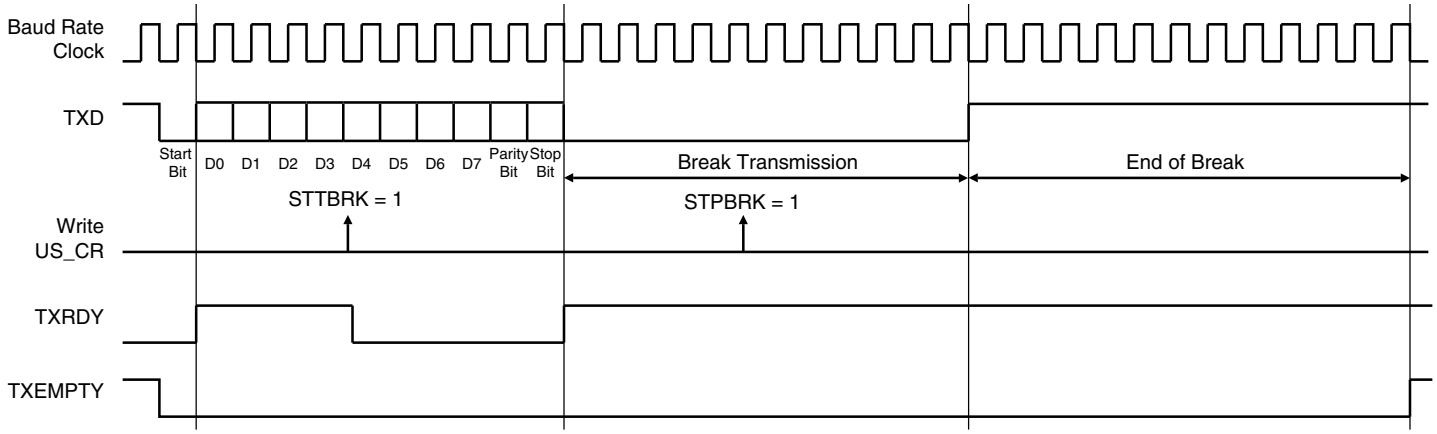
Writing CR with the both STTBRK and STPBRK bits at 1 can lead to an unpredictable result. All STPBRK commands requested without a previous STTBRK command are ignored. A byte written into the Transmit Holding Register while a break is pending, but not started, is ignored.

After the break condition, the transmitter returns the TXD line to 1 for a minimum of 12 bit times. Thus, the transmitter ensures that the remote receiver detects correctly the end of break and the start of the next character. If the timeguard is programmed with a value higher than 12, the TXD line is held high for the timeguard period.

After holding the TXD line for this period, the transmitter resumes normal operations.

Figure 24-26 illustrates the effect of both the Start Break (STTBRK) and Stop Break (STPBRK) commands on the TXD line.

Figure 24-26. Break Transmission



24.7.3.15 Receive Break

The receiver detects a break condition when all data, parity and stop bits are low. This corresponds to detecting a framing error with data at 0x00, but FRAME remains low.

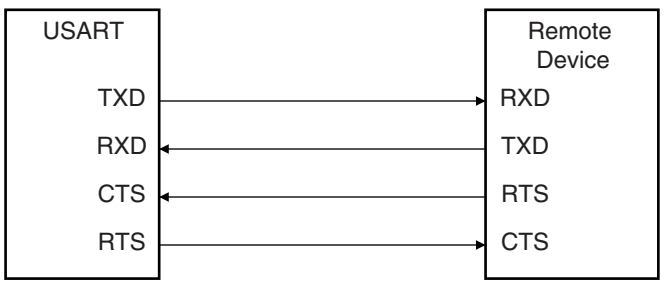
When the low stop bit is detected, the receiver asserts the RXBRK bit in CSR. This bit may be cleared by writing the Control Register (CR) with the bit RSTSTA at 1.

An end of receive break is detected by a high level for at least 2/16 of a bit period in asynchronous operating mode or one sample at high level in synchronous operating mode. The end of break detection also asserts the RXBRK bit.

24.7.3.16 Hardware Handshaking

The USART features a hardware handshaking out-of-band flow control. The RTS and CTS pins are used to connect with the remote device, as shown in Figure 24-27.

Figure 24-27. Connection with a Remote Device for Hardware Handshaking



Setting the USART to operate with hardware handshaking is performed by writing the MODE field in the Mode Register (MR) to the value 0x2.

The USART behavior when hardware handshaking is enabled is the same as the behavior in standard synchronous or asynchronous mode, except that the receiver drives the RTS pin as described below and the level on the CTS pin modifies the behavior of the transmitter as described below. Using this mode requires using the PDC channel for reception. The transmitter can handle hardware handshaking in any case.

Figure 24-28 shows how the receiver operates if hardware handshaking is enabled. The RTS pin is driven high if the receiver is disabled and if the status RXBUFF (Receive Buffer Full) coming from the PDC channel is high. Normally, the remote device does not start transmitting while its CTS pin (driven by RTS) is high. As soon as the Receiver is enabled, the RTS falls, indicating to the remote device that it can start transmitting. Defining a new buffer to the PDC clears the status bit RXBUFF and, as a result, asserts the pin RTS low.

Figure 24-28. Receiver Behavior when Operating with Hardware Handshaking

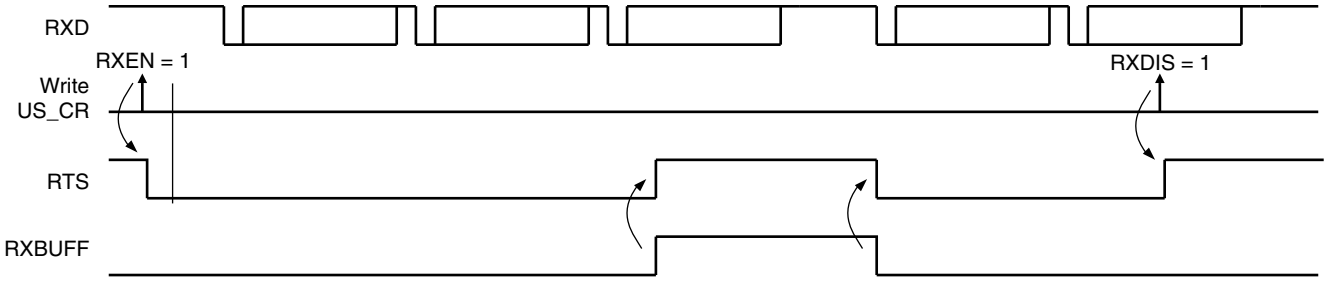
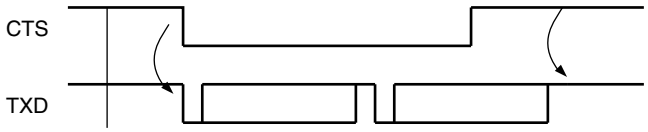


Figure 24-29 shows how the transmitter operates if hardware handshaking is enabled. The CTS pin disables the transmitter. If a character is being processing, the transmitter is disabled only after the completion of the current character and transmission of the next character happens as soon as the pin CTS falls.

Figure 24-29. Transmitter Behavior when Operating with Hardware Handshaking



24.7.4 ISO7816 Mode

The USART features an ISO7816-compatible operating mode. This mode permits interfacing with smart cards and Security Access Modules (SAM) communicating through an ISO7816 link. Both T = 0 and T = 1 protocols defined by the ISO7816 specification are supported.

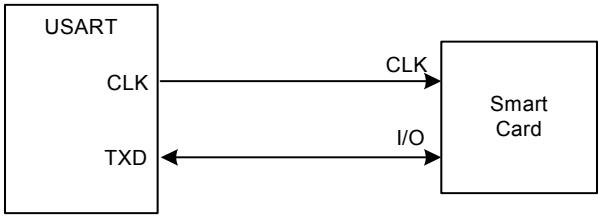
Setting the USART in ISO7816 mode is performed by writing the MODE field in the Mode Register (MR) to the value 0x4 for protocol T = 0 and to the value 0x5 for protocol T = 1.

24.7.4.1 ISO7816 Mode Overview

The ISO7816 is a half duplex communication on only one bidirectional line. The baud rate is determined by a division of the clock provided to the remote device (see "Baud Rate Generator" on page 396).

The USART connects to a smart card as shown in Figure 24-30. The TXD line becomes bidirectional and the Baud Rate Generator feeds the ISO7816 clock on the CLK pin. As the TXD pin becomes bidirectional, its output remains driven by the output of the transmitter but only when the transmitter is active while its input is directed to the input of the receiver. The USART is considered as the master of the communication as it generates the clock.

Figure 24-30. Connection of a Smart Card to the USART



When operating in ISO7816, either in T = 0 or T = 1 modes, the character format is fixed. The configuration is 8 data bits, even parity and 1 or 2 stop bits, regardless of the values programmed in the CHRL, MODE9, PAR and CHMODE fields. MSBF can be used to transmit LSB or MSB first. Parity Bit (PAR) can be used to transmit in normal or inverse mode. Refer to "USART Mode Register" on page 429 and "PAR: Parity Type" on page 430.

The USART cannot operate concurrently in both receiver and transmitter modes as the communication is unidirectional at a time. It has to be configured according to the required mode by enabling or disabling either the receiver or the transmitter as desired. Enabling both the receiver and the transmitter at the same time in ISO7816 mode may lead to unpredictable results.

The ISO7816 specification defines an inverse transmission format. Data bits of the character must be transmitted on the I/O line at their negative value. The USART does not support this format and the user has to perform an exclusive OR on the data before writing it in the Transmit Holding Register (THR) or after reading it in the Receive Holding Register (RHR).

24.7.4.2 Protocol T = 0

In T = 0 protocol, a character is made up of one start bit, eight data bits, one parity bit and one guard time, which lasts two bit times. The transmitter shifts out the bits and does not drive the I/O line during the guard time.

If no parity error is detected, the I/O line remains at 1 during the guard time and the transmitter can continue with the transmission of the next character, as shown in Figure 24-31.

If a parity error is detected by the receiver, it drives the I/O line at 0 during the guard time, as shown in Figure 24-32. This error bit is also named NACK, for Non Acknowledge. In this case, the character lasts 1 bit time more, as the guard time length is the same and is added to the error bit time which lasts 1 bit time.

When the USART is the receiver and it detects an error, it does not load the erroneous character in the Receive Holding Register (RHR). It appropriately sets the PARE bit in the Status Register (SR) so that the software can handle the error.

Figure 24-31. T = 0 Protocol without Parity Error

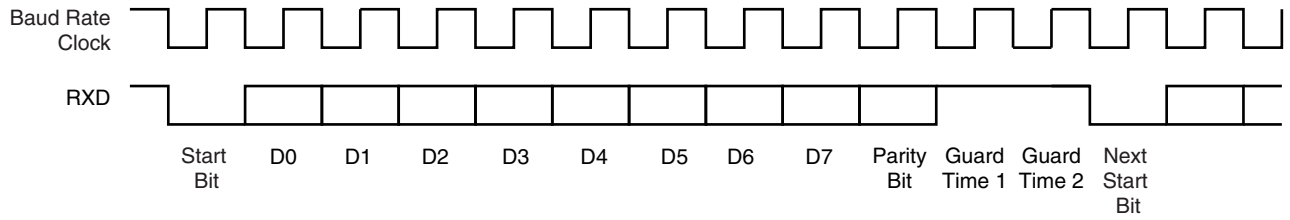
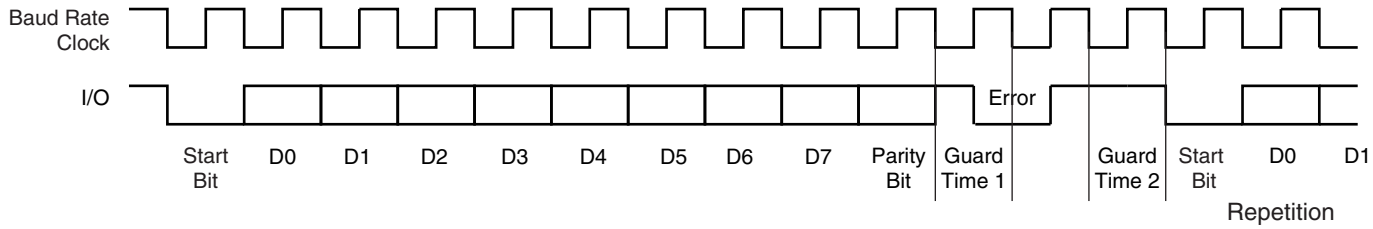


Figure 24-32. T = 0 Protocol with Parity Error



24.7.4.3 Receive Error Counter

The USART receiver also records the total number of errors. This can be read in the Number of Error (NER) register. The NB_ERRORS field can record up to 255 errors. Reading NER automatically clears the NB_ERRORS field.

24.7.4.4 Receive NACK Inhibit

The USART can also be configured to inhibit an error. This can be achieved by setting the INACK bit in the Mode Register (MR). If INACK is at 1, no error signal is driven on the I/O line even if a parity bit is detected, but the INACK bit is set in the Status Register (SR). The INACK bit can be cleared by writing the Control Register (CR) with the RSTNACK bit at 1.

Moreover, if INACK is set, the erroneous received character is stored in the Receive Holding Register, as if no error occurred. However, the RXRDY bit does not raise.

24.7.4.5 Transmit Character Repetition

When the USART is transmitting a character and gets a NACK, it can automatically repeat the character before moving on to the next one. Repetition is enabled by writing the MAX_ITERATION field in the Mode Register (MR) at a value higher than 0. Each character can be transmitted up to eight times; the first transmission plus seven repetitions.

If MAX_ITERATION does not equal zero, the USART repeats the character as many times as the value loaded in MAX_ITERATION.

When the USART repetition number reaches MAX_ITERATION, the ITERATION bit is set in the Channel Status Register (CSR). If the repetition of the character is acknowledged by the receiver, the repetitions are stopped and the iteration counter is cleared.

The ITERATION bit in CSR can be cleared by writing the Control Register with the RSIT bit at 1.

24.7.4.6 Disable Successive Receive NACK

The receiver can limit the number of successive NACKs sent back to the remote transmitter. This is programmed by setting the bit DSNACK in the Mode Register (MR). The maximum number of NACK transmitted is programmed in the MAX_ITERATION field. As soon as

MAX_ITERATION is reached, the character is considered as correct, an acknowledge is sent on the line and the ITERATION bit in the Channel Status Register is set.

24.7.4.7 *Protocol T = 1*

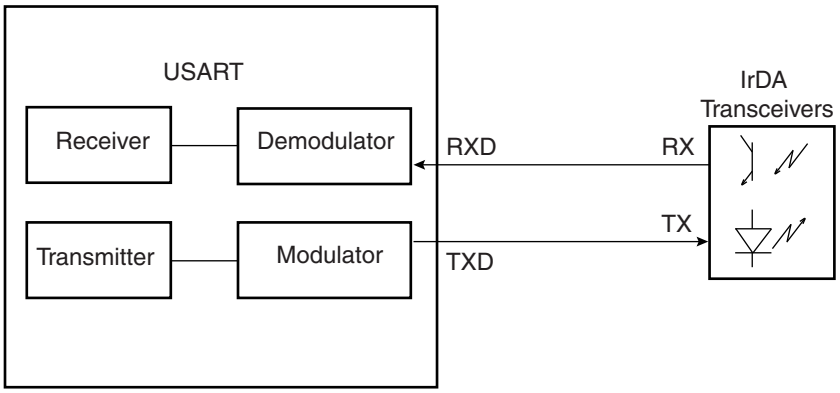
When operating in ISO7816 protocol T = 1, the transmission is similar to an asynchronous format with only one stop bit. The parity is generated when transmitting and checked when receiving. Parity error detection sets the PARE bit in the Channel Status Register (CSR).

24.7.5 IrDA Mode

The USART features an IrDA mode supplying half-duplex point-to-point wireless communication. It embeds the modulator and demodulator which allows a glueless connection to the infrared transceivers, as shown in Figure 24-33. The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 Kb/s to 115.2 Kb/s.

The USART IrDA mode is enabled by setting the MODE field in the Mode Register (MR) to the value 0x8. The IrDA Filter Register (IFR) allows configuring the demodulator filter. The USART transmitter and receiver operate in a normal asynchronous mode and all parameters are accessible. Note that the modulator and the demodulator are activated.

Figure 24-33. Connection to IrDA Transceivers



The receiver and the transmitter must be enabled or disabled according to the direction of the transmission to be managed.

24.7.5.1 *IrDA Modulation*

For baud rates up to and including 115.2 Kbits/sec, the RZI modulation scheme is used. “0” is represented by a light pulse of 3/16th of a bit time. Some examples of signal pulse duration are shown in Table 24-9.

Table 24-9. IrDA Pulse Duration

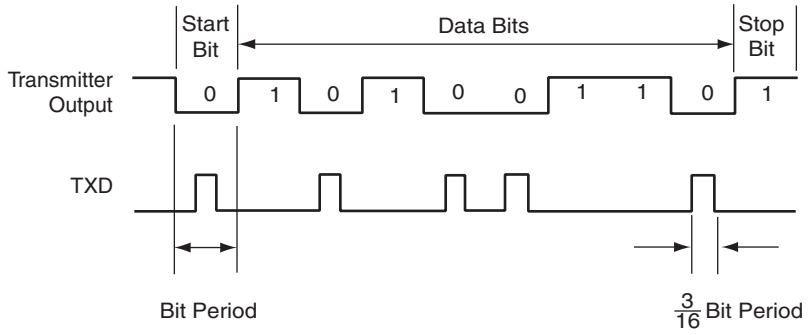
Baud Rate	Pulse Duration (3/16)
2.4 Kb/s	78.13 µs
9.6 Kb/s	19.53 µs
19.2 Kb/s	9.77 µs

Table 24-9. IrDA Pulse Duration

Baud Rate	Pulse Duration (3/16)
38.4 Kb/s	4.88 µs
57.6 Kb/s	3.26 µs
115.2 Kb/s	1.63 µs

Figure 24-34 shows an example of character transmission.

Figure 24-34. IrDA Modulation



24.7.5.2 IrDA Baud Rate

Table 24-10 gives some examples of CD values, baud rate error and pulse duration. Note that the requirement on the maximum acceptable error of ±1.87% must be met.

Table 24-10. IrDA Baud Rate Error

Peripheral Clock	Baud Rate	CD	Baud Rate Error	Pulse Time
3 686 400	115 200	2	0.00%	1.63
20 000 000	115 200	11	1.38%	1.63
32 768 000	115 200	18	1.25%	1.63
40 000 000	115 200	22	1.38%	1.63
3 686 400	57 600	4	0.00%	3.26
20 000 000	57 600	22	1.38%	3.26
32 768 000	57 600	36	1.25%	3.26
40 000 000	57 600	43	0.93%	3.26
3 686 400	38 400	6	0.00%	4.88
20 000 000	38 400	33	1.38%	4.88
32 768 000	38 400	53	0.63%	4.88
40 000 000	38 400	65	0.16%	4.88
3 686 400	19 200	12	0.00%	9.77
20 000 000	19 200	65	0.16%	9.77
32 768 000	19 200	107	0.31%	9.77
40 000 000	19 200	130	0.16%	9.77

Table 24-10. IrDA Baud Rate Error (Continued)

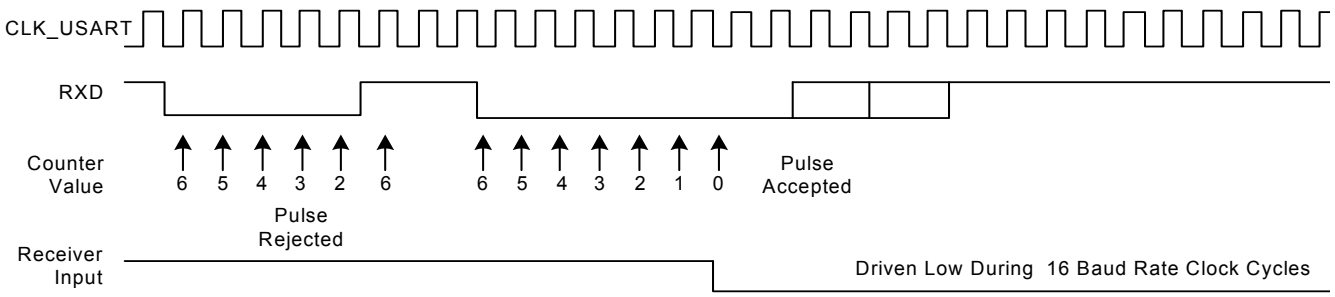
Peripheral Clock	Baud Rate	CD	Baud Rate Error	Pulse Time
3 686 400	9 600	24	0.00%	19.53
20 000 000	9 600	130	0.16%	19.53
32 768 000	9 600	213	0.16%	19.53
40 000 000	9 600	260	0.16%	19.53
3 686 400	2 400	96	0.00%	78.13
20 000 000	2 400	521	0.03%	78.13
32 768 000	2 400	853	0.04%	78.13

24.7.5.3 IrDA Demodulator

The demodulator is based on the IrDA Receive filter comprised of an 8-bit down counter which is loaded with the value programmed in IFR. When a falling edge is detected on the RXD pin, the Filter Counter starts counting down at the CLK_USART speed. If a rising edge is detected on the RXD pin, the counter stops and is reloaded with IFR. If no rising edge is detected when the counter reaches 0, the input of the receiver is driven low during one bit time.

Figure 24-35 illustrates the operations of the IrDA demodulator.

Figure 24-35. IrDA Demodulator Operations

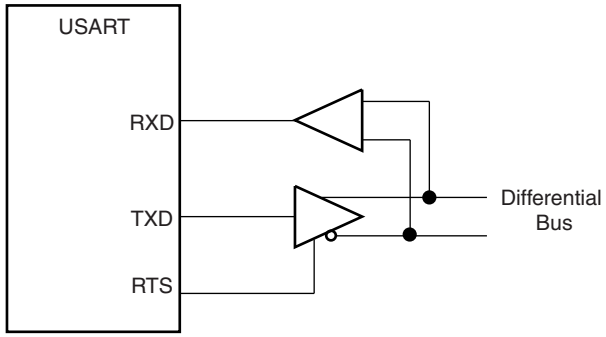


As the IrDA mode uses the same logic as the ISO7816, note that the FI_DI_RATIO field in FIDI must be set to a value higher than 0 in order to assure IrDA communications operate correctly.

24.7.6 RS485 Mode

The USART features the RS485 mode to enable line driver control. While operating in RS485 mode, the USART behaves as though in asynchronous or synchronous mode and configuration of all the parameters is possible. The difference is that the RTS pin is driven high when the transmitter is operating. The behavior of the RTS pin is controlled by the TXEMPTY bit. A typical connection of the USART to a RS485 bus is shown in Figure 24-36.

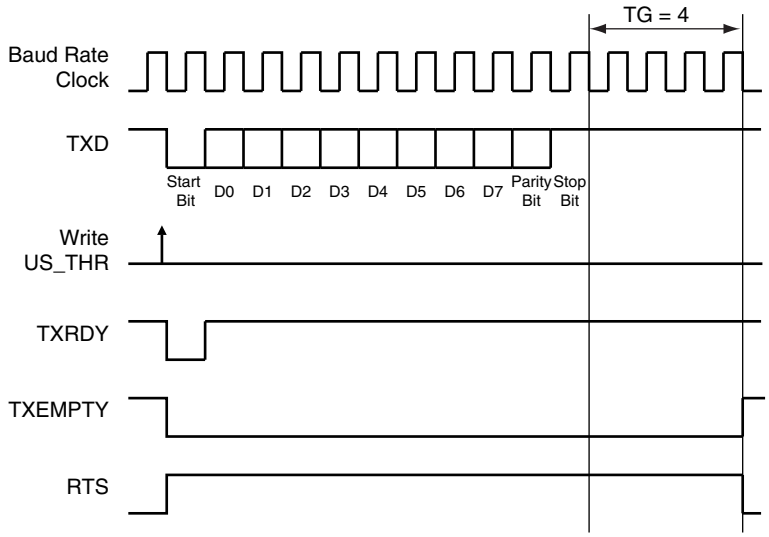
Figure 24-36. Typical Connection to a RS485 Bus



The USART is set in RS485 mode by programming the MODE field in the Mode Register (MR) to the value 0x1.

The RTS pin is at a level inverse to the TXEMPTY bit. Significantly, the RTS pin remains high when a timeguard is programmed so that the line can remain driven after the last character completion. Figure 24-37 gives an example of the RTS waveform during a character transmission when the timeguard is enabled.

Figure 24-37. Example of RTS Drive with Timeguard



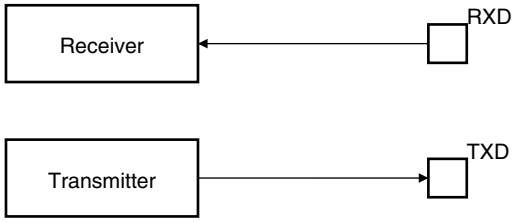
24.7.7 Test Modes

The USART can be programmed to operate in three different test modes. The internal loopback capability allows on-board diagnostics. In the loopback mode the USART interface pins are disconnected or not and reconfigured for loopback internally or externally.

24.7.7.1 Normal Mode

Normal mode connects the RXD pin on the receiver input and the transmitter output on the TXD pin.

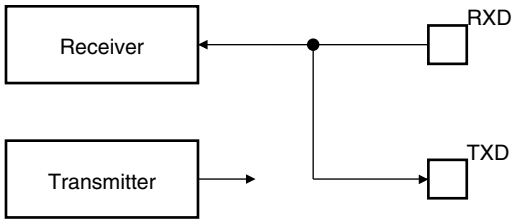
Figure 24-38. Normal Mode Configuration



24.7.7.2 Automatic Echo Mode

Automatic echo mode allows bit-by-bit retransmission. When a bit is received on the RXD pin, it is sent to the TXD pin, as shown in Figure 24-39. Programming the transmitter has no effect on the TXD pin. The RXD pin is still connected to the receiver input, thus the receiver remains active.

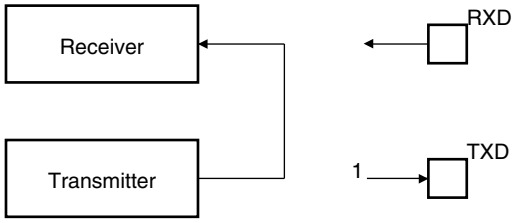
Figure 24-39. Automatic Echo Mode Configuration



24.7.7.3 Local Loopback Mode

Local loopback mode connects the output of the transmitter directly to the input of the receiver, as shown in Figure 24-40. The TXD and RXD pins are not used. The RXD pin has no effect on the receiver and the TXD pin is continuously driven high, as in idle state.

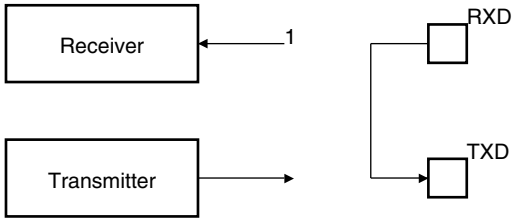
Figure 24-40. Local Loopback Mode Configuration



24.7.7.4 Remote Loopback Mode

Remote loopback mode directly connects the RXD pin to the TXD pin, as shown in Figure 24-41. The transmitter and the receiver are disabled and have no effect. This mode allows bit-by-bit retransmission.

Figure 24-41. Remote Loopback Mode Configuration



24.8 USART User Interface

Table 24-11. USART Memory Map

Offset	Register	Name	Access	Reset State
0x0000	Control Register	CR	Write-only	–
0x0004	Mode Register	MR	Read/Write	–
0x0008	Interrupt Enable Register	IER	Write-only	–
0x000C	Interrupt Disable Register	IDR	Write-only	–
0x0010	Interrupt Mask Register	IMR	Read-only	0x0
0x0014	Channel Status Register	CSR	Read-only	–
0x0018	Receiver Holding Register	RHR	Read-only	0x0
0x001C	Transmitter Holding Register	THR	Write-only	–
0x0020	Baud Rate Generator Register	BRGR	Read/Write	0x0
0x0024	Receiver Time-out Register	RTOR	Read/Write	0x0
0x0028	Transmitter Timeguard Register	TTGR	Read/Write	0x0
0x2C - 0x3C	Reserved	–	–	–
0x0040	FI DI Ratio Register	FIDI	Read/Write	0x174
0x0044	Number of Errors Register	NER	Read-only	–
0x0048	Reserved	-	–	–
0x004C	IrDA Filter Register	IFR	Read/Write	0x0
0x0050	Manchester Encoder Decoder Register	MAN	Read/Write	0x30011004
0x5C - 0xF8	Reserved	–	–	–
0xFC	Version Register	US_VERSION	Read-only	0x–[1]
0x100 - 0x128	Reserved for PDC Registers	–	–	–

Note: 1. Values in the Version Register vary with the version of the IP block implementation.

24.8.1 USART Control Register

Name: CR

Access Type: Write-only

Offset: 0x00

Reset Value: -

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	RTSDIS	RTSEN	–	–
15	14	13	12	11	10	9	8
RETTO	RSTNACK	RSTIT	SENDA	STTTO	STPBRK	STTBRK	RSTSTA
7	6	5	4	3	2	1	0
TXDIS	TXEN	RXDIS	RXEN	RSTTX	RSTRX	–	–

- **RSTRX: Reset Receiver**

0: No effect.

1: Resets the receiver.

- **RSTTX: Reset Transmitter**

0: No effect.

1: Resets the transmitter.

- **RXEN: Receiver Enable**

0: No effect.

1: Enables the receiver, if RXDIS is 0.

- **RXDIS: Receiver Disable**

0: No effect.

1: Disables the receiver.

- **TXEN: Transmitter Enable**

0: No effect.

1: Enables the transmitter if TXDIS is 0.

- **TXDIS: Transmitter Disable**

0: No effect.

1: Disables the transmitter.

- **RSTSTA: Reset Status Bits**

0: No effect.

1: Resets the status bits PARE, FRAME, OVRE, MANERR and RXBRK in CSR.

- **STTBRK: Start Break**

0: No effect.

1: Starts transmission of a break after the characters present in THR and the Transmit Shift Register have been transmitted. No effect if a break is already being transmitted.

- **STPBRK: Stop Break**

0: No effect.

1: Stops transmission of the break after a minimum of one character length and transmits a high level during 12-bit periods. No effect if no break is being transmitted.

- **STTTO: Start Time-out**

0: No effect

1: Starts waiting for a character before clocking the time-out counter.

- **SENDA: Send Address**

0: No effect.

1: In Multidrop Mode only, the next character written to the THR is sent with the address bit set.

- **RSTIT: Reset Iterations**

0: No effect.

1: Resets ITERATION in CSR. No effect if the ISO7816 is not enabled.

- **RSTNACK: Reset Non Acknowledge**

0: No effect

1: Resets NACK in CSR.

- **RETTO: Rearm Time-out**

0: No effect

1: Restart Time-out

- **RTSEN: Request to Send Enable**

0: No effect.

1: Drives the pin RTS to 0.

- **RTSDIS: Request to Send Disable**

0: No effect.

1: Drives the pin RTS to 1.

24.8.2 USART Mode Register

Name: MR

Access Type: Read/Write

31	30	29	28	27	26	25	24
ONEBIT	MODSYNC	MAN	FILTER	–	MAX_ITERATION		

23	22	21	20	19	18	17	16
–	VAR_SYNC	DSNACK	INACK	OVER	CLKO	MODE9	MSBF

15	14	13	12	11	10	9	8
CHMODE		NBSTOP		PAR			SYNC

7	6	5	4	3	2	1	0
CHRL		USCLKS		MODE			

- **MODE**

MODE				Mode of the USART
0	0	0	0	Normal
0	0	0	1	RS485
0	0	1	0	Hardware Handshaking
0	0	1	1	Reserved
0	1	0	0	IS07816 Protocol: T = 0
0	1	0	1	Reserved
0	1	1	0	IS07816 Protocol: T = 1
0	1	1	1	Reserved
1	0	0	0	IrDA
1	1	x	x	Reserved

- **USCLKS: Clock Selection**

USCLKS		Selected Clock
0	0	CLK_USART
0	1	CLK_USART / DIV
1	0	Reserved
1	1	CLK

- **CHRL: Character Length.**

CHRL		Character Length
0	0	5 bits

0	1	6 bits
1	0	7 bits
1	1	8 bits

- **SYNC: Synchronous Mode Select**

0: USART operates in Asynchronous Mode.

1: USART operates in Synchronous Mode.

- **PAR: Parity Type**

PAR			Parity Type
0	0	0	Even parity
0	0	1	Odd parity
0	1	0	Parity forced to 0 (Space)
0	1	1	Parity forced to 1 (Mark)
1	0	x	No parity
1	1	x	Multidrop mode

- **NBSTOP: Number of Stop Bits**

NBSTOP		Asynchronous (SYNC = 0)	Synchronous (SYNC = 1)
0	0	1 stop bit	1 stop bit
0	1	1.5 stop bits	Reserved
1	0	2 stop bits	2 stop bits
1	1	Reserved	Reserved

- **CHMODE: Channel Mode**

CHMODE		Mode Description
0	0	Normal Mode
0	1	Automatic Echo. Receiver input is connected to the TXD pin.
1	0	Local Loopback. Transmitter output is connected to the Receiver Input..
1	1	Remote Loopback. RXD pin is internally connected to the TXD pin.

- **MSBF: Bit Order**

0: Least Significant Bit is sent/received first.

1: Most Significant Bit is sent/received first.

- **MODE9: 9-bit Character Length**

0: CHRL defines character length.

1: 9-bit character length.

- **CLKO: Clock Output Select**

0: The USART does not drive the CLK pin.

1: The USART drives the CLK pin if USCLKS does not select the external clock CLK.

- **OVER: Oversampling Mode**

0: 16x Oversampling.

1: 8x Oversampling.

- **INACK: Inhibit Non Acknowledge**

0: The NACK is generated.

1: The NACK is not generated.

- **DSNACK: Disable Successive NACK**

0: NACK is sent on the ISO line as soon as a parity error occurs in the received character (unless INACK is set).

1: Successive parity errors are counted up to the value specified in the MAX_ITERATION field. These parity errors generate a NACK on the ISO line. As soon as this value is reached, no additional NACK is sent on the ISO line. The flag ITERATION is asserted.

- **VAR_SYNC: Variable synchronization of command/data sync Start Frame Delimiter**

0: User defined configuration of command or data sync field depending on SYNC value.

1: The sync field is updated when a character is written into THR register.

- **MAX_ITERATION**

Defines the maximum number of iterations in mode ISO7816, protocol T= 0.

- **FILTER: Infrared Receive Line Filter**

0: The USART does not filter the receive line.

1: The USART filters the receive line using a three-sample filter (1/16-bit clock) (2 over 3 majority).

- **MAN: Manchester Encoder/Decoder Enable**

0: Manchester Encoder/Decoder are disabled.

1: Manchester Encoder/Decoder are enabled.

- **MODSYNC: Manchester Synchronization mode**

0:The Manchester Start bit is a 0 to 1 transition

1: The Manchester Start bit is a 1 to 0 transition.

- **ONEBIT: Start Frame Delimiter selector**

0: Start Frame delimiter is COMMAND or DATA SYNC.

1: Start Frame delimiter is One Bit.

24.8.3 USART Interrupt Enable Register

Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	MANE	CTSIC	–	–	–

15	14	13	12	11	10	9	8
–	–	NACK	RXBUFF	TXBUFE	ITERATION	TXEMPTY	TIMEOUT

7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: RXRDY Interrupt Enable**
- **TXRDY: TXRDY Interrupt Enable**
- **RXBRK: Receiver Break Interrupt Enable**
- **ENDRX: End of Receive Transfer Interrupt Enable**
- **ENDTX: End of Transmit Interrupt Enable**
- **OVRE: Overrun Error Interrupt Enable**
- **FRAME: Framing Error Interrupt Enable**
- **PARE: Parity Error Interrupt Enable**
- **TIMEOUT: Time-out Interrupt Enable**
- **TXEMPTY: TXEMPTY Interrupt Enable**
- **ITERATION: Iteration Interrupt Enable**
- **TXBUFE: Buffer Empty Interrupt Enable**
- **RXBUFF: Buffer Full Interrupt Enable**
- **NACK: Non Acknowledge Interrupt Enable**
- **CTSIC: Clear to Send Input Change Interrupt Enable**
- **MANE: Manchester Error Interrupt Enable**

0: No effect.

1: Enables the corresponding interrupt.

24.8.4 USART Interrupt Disable Register

Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	MANE	CTSIC	–	–	–

15	14	13	12	11	10	9	8
–	–	NACK	RXBUFF	TXBUFE	ITERATION	TXEMPTY	TIMEOUT

7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: RXRDY Interrupt Disable**
- **TXRDY: TXRDY Interrupt Disable**
- **RXBRK: Receiver Break Interrupt Disable**
- **ENDRX: End of Receive Transfer Interrupt Disable**
- **ENDTX: End of Transmit Interrupt Disable**
- **OVRE: Overrun Error Interrupt Disable**
- **FRAME: Framing Error Interrupt Disable**
- **PARE: Parity Error Interrupt Disable**
- **TIMEOUT: Time-out Interrupt Disable**
- **TXEMPTY: TXEMPTY Interrupt Disable**
- **ITERATION: Iteration Interrupt Disable**
- **TXBUFE: Buffer Empty Interrupt Disable**
- **RXBUFF: Buffer Full Interrupt Disable**
- **NACK: Non Acknowledge Interrupt Disable**
- **CTSIC: Clear to Send Input Change Interrupt Disable**
- **MANE: Manchester Error Interrupt Disable**

0: No effect.

1: Disables the corresponding interrupt.

24.8.5 USART Interrupt Mask Register

Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	MANE	CTSIC	–	–	–
15	14	13	12	11	10	9	8
–	–	NACK	RXBUFF	TXBUFE	ITERATION	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: RXRDY Interrupt Mask**
- **TXRDY: TXRDY Interrupt Mask**
- **RXBRK: Receiver Break Interrupt Mask**
- **ENDRX: End of Receive Transfer Interrupt Mask**
- **ENDTX: End of Transmit Interrupt Mask**
- **OVRE: Overrun Error Interrupt Mask**
- **FRAME: Framing Error Interrupt Mask**
- **PARE: Parity Error Interrupt Mask**
- **TIMEOUT: Time-out Interrupt Mask**
- **TXEMPTY: TXEMPTY Interrupt Mask**
- **ITERATION: Iteration Interrupt Mask**
- **TXBUFE: Buffer Empty Interrupt Mask**
- **RXBUFF: Buffer Full Interrupt Mask**
- **NACK: Non Acknowledge Interrupt Mask**
- **CTSIC: Clear to Send Input Change Interrupt Mask**
- **MANE: Manchester Error Interrupt Mask**

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

24.8.6 USART Channel Status Register

Name: CSR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	MANERR
23	22	21	20	19	18	17	16
CTS	–	–	–	CTSIC	–	–	–
15	14	13	12	11	10	9	8
–	–	NACK	RXBUFF	TXBUFE	ITERATION	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: Receiver Ready**

0: No complete character has been received since the last read of RHR or the receiver is disabled. If characters were being received when the receiver was disabled, RXRDY changes to 1 when the receiver is enabled.

1: At least one complete character has been received and RHR has not yet been read.

- **TXRDY: Transmitter Ready**

0: A character is in the THR waiting to be transferred to the Transmit Shift Register, or an STTBRK command has been requested, or the transmitter is disabled. As soon as the transmitter is enabled, TXRDY becomes 1.

1: There is no character in the THR.

- **RXBRK: Break Received/End of Break**

0: No Break received or End of Break detected since the last RSTSTA.

1: Break Received or End of Break detected since the last RSTSTA.

- **ENDRX: End of Receiver Transfer**

0: The End of Transfer signal from the Receive PDC channel is inactive.

1: The End of Transfer signal from the Receive PDC channel is active.

- **ENDTX: End of Transmitter Transfer**

0: The End of Transfer signal from the Transmit PDC channel is inactive.

1: The End of Transfer signal from the Transmit PDC channel is active.

- **OVRE: Overrun Error**

0: No overrun error has occurred since the last RSTSTA.

1: At least one overrun error has occurred since the last RSTSTA.

- **FRAME: Framing Error**

0: No stop bit has been detected low since the last RSTSTA.

1: At least one stop bit has been detected low since the last RSTSTA.

- **PARE: Parity Error**

0: No parity error has been detected since the last RSTSTA.

1: At least one parity error has been detected since the last RSTSTA.

- **TIMEOUT: Receiver Time-out**

0: There has not been a time-out since the last Start Time-out command or the Time-out Register is 0.

1: There has been a time-out since the last Start Time-out command.

- **TXEMPTY: Transmitter Empty**

0: There are characters in either THR or the Transmit Shift Register, or the transmitter is disabled.

TXEMPTY == 1 means that the transmit shift register is empty and that there is no data in THR.

- **ITERATION: Max number of Repetitions Reached**

0: Maximum number of repetitions has not been reached since the last RSIT.

1: Maximum number of repetitions has been reached since the last RSIT.

- **TXBUFE: Transmission Buffer Empty**

0: The signal Buffer Empty from the Transmit PDC channel is inactive.

1: The signal Buffer Empty from the Transmit PDC channel is active.

- **RXBUFF: Reception Buffer Full**

0: The signal Buffer Full from the Receive PDC channel is inactive.

1: The signal Buffer Full from the Receive PDC channel is active.

- **NACK: Non Acknowledge**

0: No Non Acknowledge has not been detected since the last RSTNACK.

1: At least one Non Acknowledge has been detected since the last RSTNACK.

- **CTSIC: Clear to Send Input Change Flag**

0: No input change has been detected on the CTS pin since the last read of CSR.

1: At least one input change has been detected on the CTS pin since the last read of CSR.

- **CTS: Image of CTS Input**

0: CTS is at 0.

1: CTS is at 1.

- **MANERR: Manchester Error**

0: No Manchester error has been detected since the last RSTSTA.

1: At least one Manchester error has been detected since the last RSTSTA.

24.8.7 USART Receive Holding Register

Name: RHR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
RXSYNH	–	–	–	–	–	–	RXCHR

7	6	5	4	3	2	1	0
RXCHR							

- **RXCHR: Received Character**

Last character received if RXRDY is set.

- **RXSYNH: Received Sync**

0: Last Character received is a Data.

1: Last Character received is a Command.

24.8.8 USART Transmit Holding Register

Name: THR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TXSYNH	–	–	–	–	–	–	TXCHR

7	6	5	4	3	2	1	0
TXCHR							

- **TXCHR: Character to be Transmitted**

Next character to be transmitted after the current character if TXRDY is not set.

- **TXSYNH: Sync Field to be transmitted**

0: The next character sent is encoded as a data. Start Frame Delimiter is DATA SYNC.

1: The next character sent is encoded as a command. Start Frame Delimiter is COMMAND SYNC.

24.8.9 USART Baud Rate Generator Register

Name: BRGR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	FP		

15	14	13	12	11	10	9	8
CD							

7	6	5	4	3	2	1	0
CD							

- **CD: Clock Divider**

CD	**MODE ≠ ISO7816**			MODE = ISO7816
	SYNC = 0		SYNC = 1	
	OVER = 0	**OVER = 1**		
0	Baud Rate Clock Disabled			
1 to 65535	Baud Rate = Selected Clock/16/CD	Baud Rate = Selected Clock/8/CD	Baud Rate = Selected Clock /CD	Baud Rate = Selected Clock/CD/FI_DI_RATIO

- **FP: Fractional Part**

0: Fractional divider is disabled.

1 - 7: Baudrate resolution, defined by FP x 1/8.

24.8.10 USART Receiver Time-out Register

Name: RTOR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TO							

7	6	5	4	3	2	1	0
TO							

- **TO: Time-out Value**

0: The Receiver Time-out is disabled.

1 - 65535: The Receiver Time-out is enabled and the Time-out delay is TO x Bit Period.

24.8.11 USART Transmitter Timeguard Register

Name: TTGR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
TG							

- **TG: Timeguard Value**

0: The Transmitter Timeguard is disabled.

1 - 255: The Transmitter timeguard is enabled and the timeguard delay is TG x Bit Period.

24.8.12 USART FI DI RATIO Register

Name: FIDI

Access Type: Read/Write

Reset Value : 0x174

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	FI_DI_RATIO		
7	6	5	4	3	2	1	0
FI_DI_RATIO							

- **FI_DI_RATIO: FI Over DI Ratio Value**

0: If ISO7816 mode is selected, the Baud Rate Generator generates no signal.

1 - 2047: If ISO7816 mode is selected, the Baud Rate is the clock provided on CLK divided by FI_DI_RATIO.

24.8.13 USART Number of Errors Register

Name: NER

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
NB_ERRORS							

- **NB_ERRORS: Number of Errors**

Total number of errors that occurred during an ISO7816 transfer. This register automatically clears when read.

24.8.14 USART Manchester Configuration Register

Name: MAN

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	DRIFT	–	RX_MPOL	–	–	RX_PP	

23	22	21	20	19	18	17	16
–	–	–	–	RX_PL			

15	14	13	12	11	10	9	8
–	–	–	TX_MPOL	–	–	TX_PP	

7	6	5	4	3	2	1	0
–	–	–	–	TX_PL			

- **TX_PL: Transmitter Preamble Length**

0: The Transmitter Preamble pattern generation is disabled

1 - 15: The Preamble Length is TX_PL x Bit Period

- **TX_PP: Transmitter Preamble Pattern**

TX_PP		Preamble Pattern default polarity assumed (TX_MPOL field not set)
0	0	ALL_ONE
0	1	ALL_ZERO
1	0	ZERO_ONE
1	1	ONE_ZERO

- **TX_MPOL: Transmitter Manchester Polarity**

0: Logic Zero is coded as a zero-to-one transition, Logic One is coded as a one-to-zero transition.

1: Logic Zero is coded as a one-to-zero transition, Logic One is coded as a zero-to-one transition.

- **RX_PL: Receiver Preamble Length**

0: The receiver preamble pattern detection is disabled

1 - 15: The detected preamble length is RX_PL x Bit Period

- **RX_PP: Receiver Preamble Pattern detected**

RX_PP		Preamble Pattern default polarity assumed (RX_MPOL field not set)
0	0	ALL_ONE
0	1	ALL_ZERO
1	0	ZERO_ONE
1	1	ONE_ZERO

- **RX_MPOL: Receiver Manchester Polarity**

0: Logic Zero is coded as a zero-to-one transition, Logic One is coded as a one-to-zero transition.

1: Logic Zero is coded as a one-to-zero transition, Logic One is coded as a zero-to-one transition.

- **DRIFT: Drift compensation**

0: The USART can not recover from an important clock drift

1: The USART can recover from clock drift. The 16X clock mode must be enabled.

24.8.15 USART IrDA FILTER Register

Name: IFR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
IRDA_FILTER							

- **IRDA_FILTER: IrDA Filter**

Sets the filter of the IrDA demodulator.

24.9 USART Version Register

Name: US_VERSION

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	MFN		
15	14	13	12	11	10	9	8
–	–	–	–	VERSION			
7	6	5	4	3	2	1	0
VERSION							

- **VERSION**

Reserved. Value subject to change. No functionality associated. This is the Atmel internal version of the macrocell.

- **MFN**

Reserved. Value subject to change. No functionality associated.

25. AC97 Controller (AC97C)

Rev: 2.1.0.0

25.1 Features

- **Compliant with AC97 2.2 Component Specification**
- **2 independent communication channels**
  - **Codec Channel, dedicated to the AC97 Analog Front End Control and Status Monitoring**
  - **2 channels associated with DMA Controller interface for Isochronous Audio Streaming Transfer**
- **Variable Sampling Rate AC97 Codec Interface Support**
- **One Primary Codec Support**
- **Independent input and Output Slot to Channel Assignment, Several Slots Can Be Assigned to the Same Channel.**
- **Channels Support Mono/Stereo/Multichannel Samples of 10, 16, 18 and 20 Bits.**

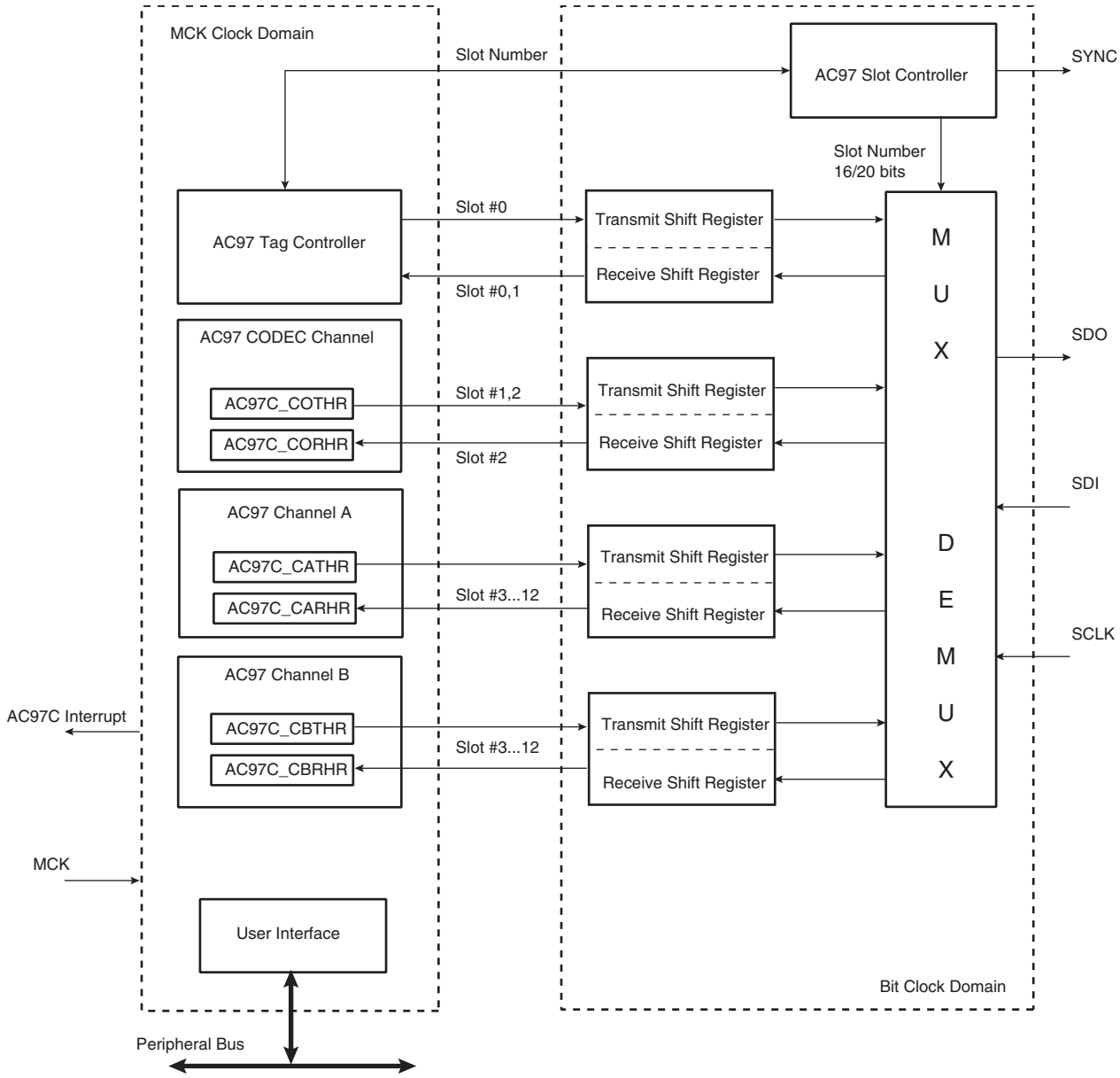
25.2 Description

The AC97 Controller is the hardware implementation of the AC97 digital controller (DC'97) compliant with AC97 Component Specification 2.2. The AC97 Controller communicates with an audio codec (AC97) or a modem codec (MC'97) via the AC-link digital serial interface. All digital audio, modem and handset data streams, as well as control (command/status) informations are transferred in accordance to the AC-link protocol.

The AC97 Controller features a DMA Controller interface for audio streaming transfers. It also supports variable sampling rate and four Pulse Code Modulation (PCM) sample resolutions of 10, 16, 18 and 20 bits.

25.3 Block Diagram

Figure 25-1. Functional Block Diagram



25.4 Pin Name List

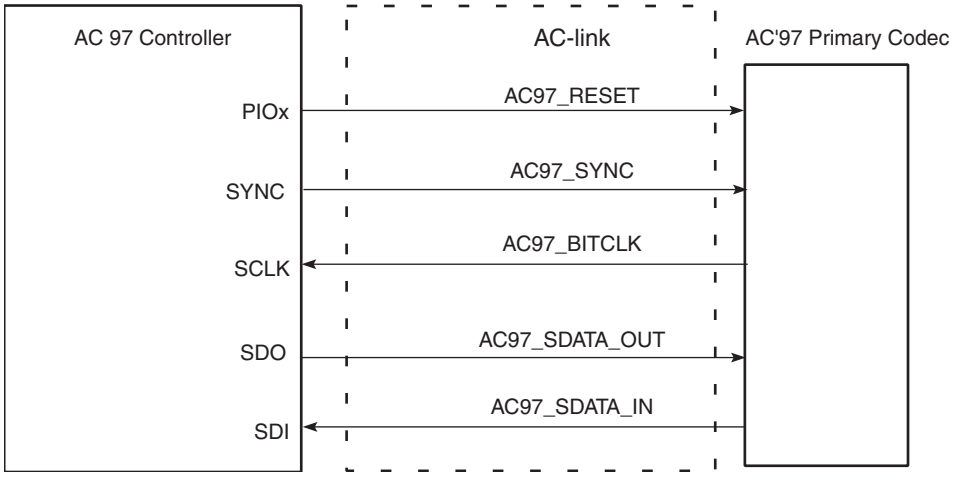
Table 25-1. I/O Lines Description

Pin Name	Pin Description	Type
SCLK	12.288-MHz bit-rate clock (Referred as BITCLK in AC-link spec)	Input
SDI	Receiver Data (Referred as SDATA_IN in AC-link spec)	Input
SYNC	48-KHz frame indicator and synchronizer	Output
SDO	Transmitter Data (Referred as SDATA_OUT in AC-link spec)	Output

The AC97 reset signal provided to the primary codec can be generated by a PIO.

25.5 Application Block Diagram

Figure 25-2. Application Block diagram



25.6 Product Dependencies

25.6.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines.

Before using the AC97 Controller receiver, the PIO controller must be configured in order for the AC97C receiver I/O lines to be in AC97 Controller peripheral mode.

Before using the AC97 Controller transmitter, the PIO controller must be configured in order for the AC97C transmitter I/O lines to be in AC97 Controller peripheral mode.

25.6.2 Power Management

The AC97 clock is generated by the power manager. Before using the AC97, the programmer must ensure that the AC'97 clock is enabled in the power manager.

In the AC97 description, Master Clock (MCK) is the clock of the peripheral bus to which the AC97 is connected. It is important that that the MCK clock frequency is higher than the SCLK (Bit Clock) clock frequancy as signals that cross the two clock domains are re-synchronized.

25.6.3 Interrupt

The AC97 interface has an interrupt line connected to the interrupt controller. In order to handle interrupts, the interrupt controller must be programmed before configuring the AC97.

All AC97 Controller interrupts can be enabled/disabled by writing to the AC97 Controller Interrupt Enable/Disable Registers. Each pending and unmasked AC97 Controller interrupt will assert the interrupt line. The AC97 Controller interrupt service routine can get the interrupt source in two steps:

- Reading and ANDing AC97 Controller Interrupt Mask Register (IMR) and AC97 Controller Status Register (SR).
- Reading AC97 Controller Channel x Status Register (CxSR).)

25.7 Functional Description

25.7.1 Protocol overview

AC-link protocol is a bidirectional, fixed clock rate, serial digital stream. AC-link handles multiple input and output Pulse Code Modulation PCM audio streams, as well as control register accesses employing a Time Division Multiplexed (TDM) scheme that divides each audio frame in 12 outgoing and 12 incoming 20-bit wide data slots.

Figure 25-3. Bidirectional AC-link Frame with Slot Assignment

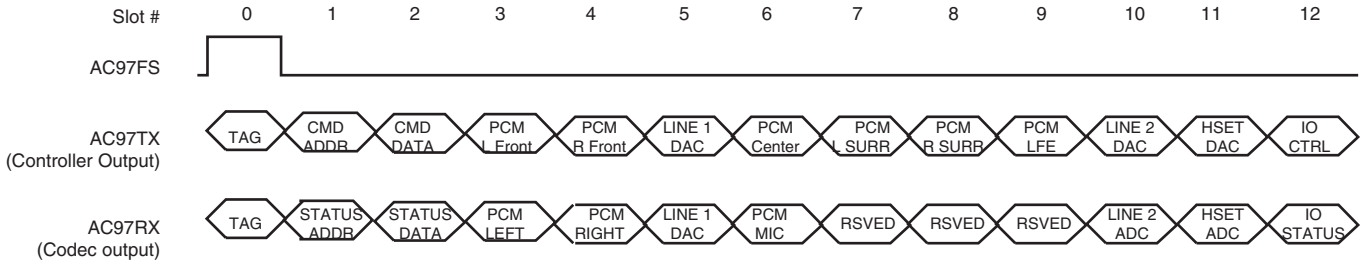


Table 25-2. AC-link Output Slots Transmitted from the AC97C Controller

Slot #	Pin Description
0	TAG
1	Command Address Port
2	Command Data Port
3,4	PCM playback Left/Right Channel
5	Modem Line 1 Output Channel
6, 7, 8	PCM Center/Left Surround/Right Surround
9	PCM LFE DAC
10	Modem Line 2 Output Channel
11	Modem Handset Output Channel
12	Modem GPIO Control Channel

Table 25-3. AC-link Input Slots Transmitted from the AC97C Controller

Slot #	Pin Description
0	TAG
1	Status Address Port
2	Status Data Port
3,4	PCM playback Left/Right Channel
5	Modem Line 1 ADC
6	Dedicated Microphone ADC
7, 8, 9	Vendor Reserved
10	Modem Line 2 ADC
11	Modem Handset Input ADC
12	Modem IO Status

25.7.2 Slot Description

25.7.2.1 Tag Slot

The tag slot, or slot 0, is a 16-bit wide slot that always goes at the beginning of an outgoing or incoming frame. Within tag slot, the first bit is a global bit that flags the entire frame validity. The next 12 bit positions sampled by the AC97 Controller indicate which of the corresponding 12 time slots contain valid data. The slot's last two bits (combined) called Codec ID, are used to distinguish primary and secondary codec.

The 16-bit wide tag slot of the output frame is automatically generated by the AC97 Controller according to the transmit request of each channel and to the SLOTREQ from the previous input frame, sent by the AC97 Codec, in Variable Sample Rate mode.

25.7.2.2 Codec Slot 1

The command/status slot is a 20-bit wide slot used to control features, and monitors status for AC97 Codec functions.

The control interface architecture supports up to sixty-four 16-bit wide read/write registers. Only the even registers are currently defined and addressed.

Slot 1's bitmap is the following:

- Bit 19 is for read/write command, 1= read, 0 = write.
- Bits [18:12] are for control register index.
- Bits [11:0] are reserved.

25.7.2.3 Codec Slot 2

Slot 2 is a 20-bit wide slot used to carry 16-bit wide AC97 Codec control register data. If the current command port operation is a read, the entire slot time is stuffed with zeros. Its bitmap is the following:

- Bits [19:4] are the control register data
- Bits [3:0] are reserved and stuffed with zeros.

25.7.2.4 Data Slots [3:12]

Slots [3:12] are 20-bit wide data slots, they usually carry audio PCM or/and modem I/O data.

25.7.3 AC97 Controller Channel Organization

The AC97 Controller features a Codec channel and 2 logical channels; Channel A and Channel B.

The Codec channel controls AC97 Codec registers, it enables write and read configuration values in order to bring the AC97 Codec to an operating state. The Codec channel always runs slot 1 and slot 2 exclusively, in both input and output directions.

Channel A and Channel B transfer data to/from AC97 codec. All audio samples and modem data must transit by these two channels.

Each slot of the input or the output frame that belongs to this range [3 to 12] can be operated by either Channel A or Channel B. The slot to channel assignment is configured by two registers:

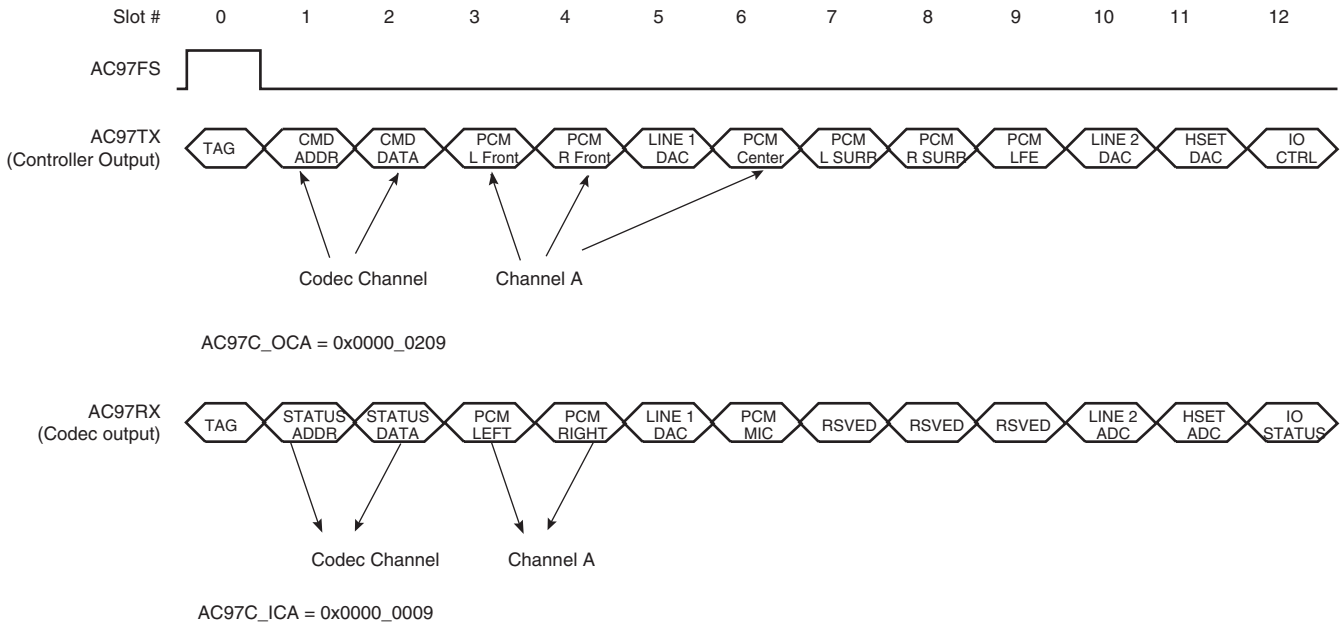
- AC97 Controller Input Channel Assignment Register (ICA)
- AC97 Controller Output Channel Assignment Register (OCA)

The AC97 Controller Input Channel Assignment Register (ICA) configures the input slot to channel assignment. The AC97 Controller Output Channel Assignment Register (OCA) configures the output slot to channel assignment.

A slot can be left unassigned to a channel by the AC97 Controller. Slots 0, 1,and 2 cannot be assigned to Channel A or to Channel B through the OCA and ICA Registers.

The width of sample data, that transit via Channel A and Channel B varies and can take one of these values; 10, 16, 18 or 20 bits.

Figure 25-4. Logical Channel Assignment



25.7.3.1 AC97 Controller Setup

The following operations must be performed in order to bring the AC97 Controller into an operating state:

1. Enable the AC97 Controller clock in the power manager.
2. Turn on AC97 function by enabling the ENA bit in AC97 Controller Mode Register (MR).
3. Configure the input channel assignment by controlling the AC97 Controller Input Assignment Register (ICA).
4. Configure the output channel assignment by controlling the AC97 Controller Input Assignment Register (OCA).
5. Configure sample width for Channel A and Channel B by writing the SIZE bit field in AC97C Channel A Mode Register (CAMR) and AC97C Channel B Mode Register (CBMR). The application can write 10, 16, 18,or 20-bit wide PCM samples through the AC97 interface and they will be transferred into 20-bit wide slots.
6. Configure data Endianness for Channel A and Channel B by writing CEM bit field in CAMR and CBMR registers. Data on the AC-link are shifted MSB first. The application can write little- or big-endian data to the AC97 Controller interface.
7. Configure the PIO controller to drive the RESET signal of the external Codec. The RESET signal must fulfill external AC97 Codec timing requirements.
8. Enable Channel A and/or Channel B by writing CEN bit field in CAMR and CBMR registers.

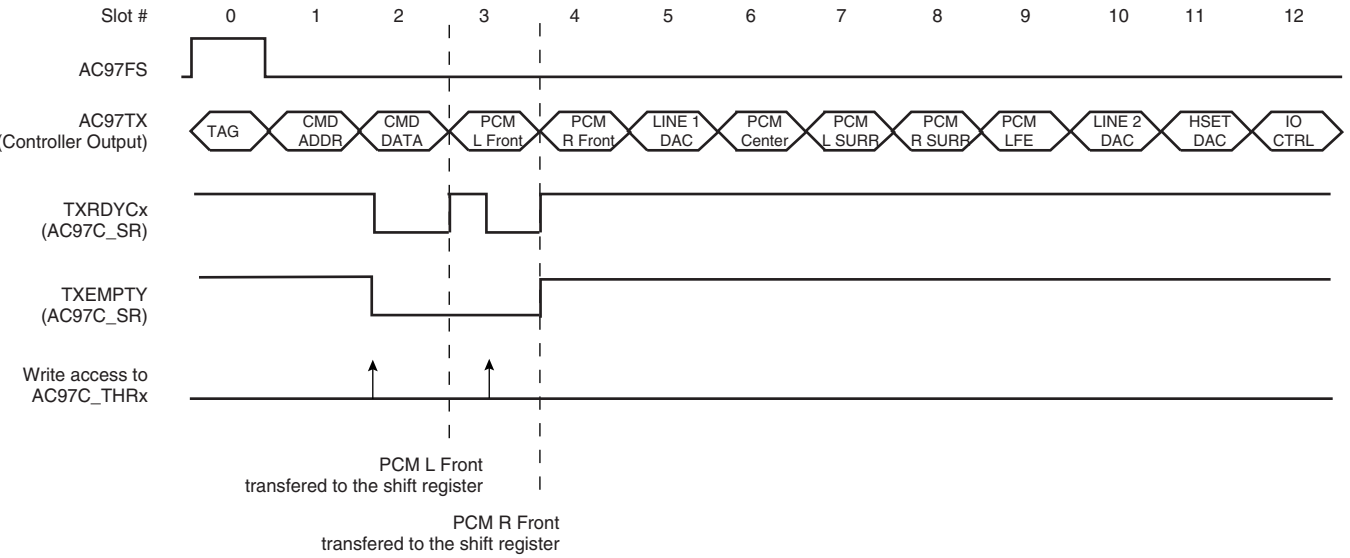
25.7.3.2 Transmit Operation

The application must perform the following steps in order to send data via a channel to the AC97 Codec:

- Check if previous data has been sent by polling TXRDY flag in the AC97C Channel x Status Register (CxSR). x being one of the 2 channels.
- Write data to the AC97 Controller Channel x Transmit Holding Register (CxTHR).

Once data has been transferred to the Channel x Shift Register, the TXRDY flag is automatically set by the AC97 Controller which allows the application to start a new write action. The application can also wait for an interrupt notice associated with TXRDY in order to send data. The interrupt remains active until TXRDY flag is cleared..

Figure 25-5. Audio Transfer (PCM L Front, PCM R Front) on Channel x



The TXEMPTY flag in the AC97 Controller Channel x Status Register (CxSR) is set when all requested transmissions for a channel have been shifted on the AC-link. The application can either poll TXEMPTY flag in CxSR or wait for an interrupt notice associated with the same flag.

In most cases, the AC97 Controller is embedded in chips that target audio player devices. In such cases, the AC97 Controller is exposed to heavy audio transfers. Using the polling technique increases processor overhead and may fail to keep the required pace under an operating system.

In order to avoid these polling drawbacks, the application can perform audio streams by using a DMA controller (DMAC) connected to both channels, which reduces processor overhead and increases performance especially under an operating system.

The DMAC transmit counter values must be equal to the number of PCM samples to be transmitted, each sample goes in one slot.

25.7.3.3 AC97 Output Frame

The AC97 Controller outputs a thirteen-slot frame on the AC-Link. The first slot (tag slot or slot 0) flags the validity of the entire frame and the validity of each slot; whether a slot carries valid data or not. Slots 1 and 2 are used if the application performs control and status monitoring actions on AC97 Codec control/status registers. Slots [3:12] are used according to the content of the AC97 Controller Output Channel Assignment Register (OCA). If the application performs many transmit requests on a channel, some of the slots associated to this channel or all of them will carry valid data.

25.7.3.4 Receive Operation

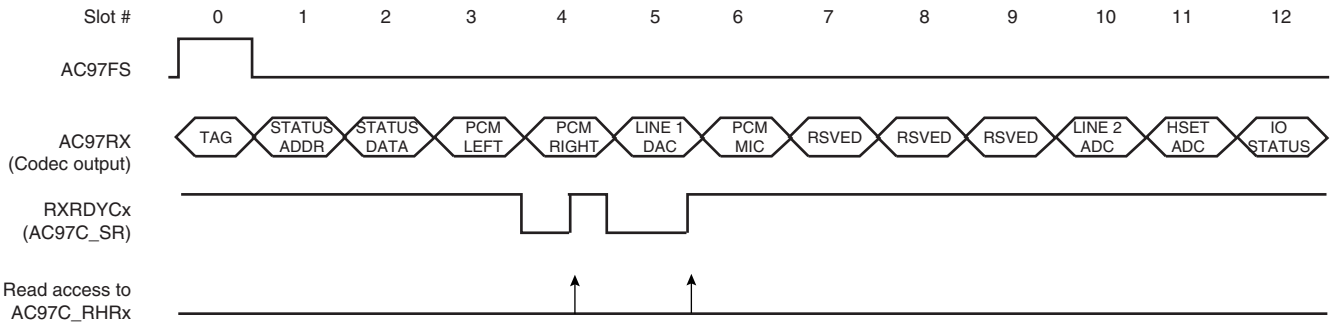
The AC97 Controller can also receive data from AC97 Codec. Data is received in the channel's shift register and then transferred to the AC97 Controller Channel x Read Holding Register. To read the newly received data, the application must perform the following steps:

- Poll RXRDY flag in AC97 Controller Channel x Status Register (CxSR). x being one of the 2 channels.
- Read data from AC97 Controller Channel x Read Holding Register.

The application can also wait for an interrupt notice in order to read data from CxRHR. The interrupt remains active until RXRDY is cleared by reading CxSR.

The RXRDY flag in CxSR is set automatically when data is received in the Channel x shift register. Data is then shifted to CxRHR.

Figure 25-6. Audio Transfer (PCM L Front, PCM R Front) on Channel x



If the previously received data has not been read by the application, the new data overwrites the data already waiting in CxRHR, therefore the OVRUN flag in CxSR is raised. The application can either poll the OVRUN flag in CxSR or wait for an interrupt notice. The interrupt remains active until the OVRUN flag in CxSR is set.

The AC97 Controller can also be used in sound recording devices in association with an AC97 Codec. The AC97 Controller may also be exposed to heavy PCM transfers.

The application can use the DMAC connected to both channels in order to reduce processor overhead and increase performance especially under an operating system.

The DMAC receive counter values must be equal to the number of PCM samples to be received. When more than one timeslot is assigned to a channel using DMA, the different timeslot samples will be interleaved.

25.7.3.5 AC97 Input Frame

The AC97 Controller receives a thirteen slot frame on the AC-Link sent by the AC97 Codec. The first slot (tag slot or slot 0) flags the validity of the entire frame and the validity of each slot; whether a slot carries valid data or not. Slots 1 and 2 are used if the application requires status informations from AC97 Codec. Slots [3:12] are used according to AC97 Controller Output Channel Assignment Register (ICA) content. The AC97 Controller will not receive any data from any slot if ICA is not assigned to a channel in input.

25.7.3.6 Configuring and Using Interrupts

Instead of polling flags in AC97 Controller Global Status Register (SR) and in AC97 Controller Channel x Status Register (CxSR), the application can wait for an interrupt notice. The following steps show how to configure and use interrupts correctly:

- Set the interruptible flag in AC97 Controller Channel x Mode Register (CxMR).
- Set the interruptible event and channel event in AC97 Controller Interrupt Enable Register (IER).

The interrupt handler must read both AC97 Controller Global Status Register (SR) and AC97 Controller Interrupt Mask Register (IMR) and AND them to get the real interrupt source. Furthermore, to get which event was activated, the interrupt handler has to read AC97 Controller Channel x Status Register (CxSR), x being the channel whose event triggers the interrupt.

The application can disable event interrupts by writing in AC97 Controller Interrupt Disable Register (IDR). The AC97 Controller Interrupt Mask Register (IMR) shows which event can trigger an interrupt and which one cannot.

25.7.3.7 Endianness

Endianness can be managed automatically for each channel, except for the Codec channel, by writing to Channel Endianness Mode (CEM) in CxMR. This enables transferring data on AC-link in Little Endian format without any additional operation.

25.7.3.8 To Transmit a Word Stored in Little Endian Format on AC-link

Word to be written in AC97 Controller Channel x Transmit Holding Register (CxTHR) (as it is stored in memory or microprocessor register).

31 – 24	23 – 16	15 – 8	7 – 0
Byte3[7:0]	Byte2[7:0]	Byte1[7:0]	Byte0[7:0]

Word stored in Channel x Transmit Holding Register (AC97C_CxTHR) (data to transmit).

31 – 24	23 – 20	19 – 16	15 – 8	7 – 0
–	–	Byte1[3:0]	Byte2[7:0]	Byte3[7:0]

Data transmitted on appropriate slot: data[19:0] = {Byte1[3:0], Byte2[7:0], Byte3[7:0]}.

25.7.3.9 To Transmit A Halfword Stored in Little Endian Format on AC-link

Halfword to be written in AC97 Controller Channel x Transmit Holding Register (CxTHR).

31 – 24	23 – 16	15 – 8	7 – 0
–	–	Byte0[7:0]	Byte1[7:0]

Halfword stored in AC97 Controller Channel x Transmit Holding Register (CxTHR) (data to transmit).

31 – 24	23 – 16	15 – 8	7 – 0
–	–	Byte1[7:0]	Byte0[7:0]

Data emitted on related slot: data[19:0] = {Byte1[7:0], Byte0[7:0], 0x0}.

25.7.3.10 To Transmit a10-bit Sample Stored in Little Endian Format on AC-link

Halfword to be written in AC97 Controller Channel x Transmit Holding Register (CxTHR).

31 – 24	23 – 16	15 – 8	7 – 0
–	–	Byte0[7:0]	{0x00, Byte1[1:0]}

Halfword stored in AC97 Controller Channel x Transmit Holding Register (CxTHR) (data to transmit).

31 – 24	23 – 16	15 – 10	9 – 8	7 – 0
–	–	–	Byte1 [1:0]	Byte0[7:0]

Data emitted on related slot: data[19:0] = {Byte1[1:0], Byte0[7:0], 0x000}.

25.7.3.11 To Receive Word transfers

Data received on appropriate slot: data[19:0] = {Byte2[3:0], Byte1[7:0], Byte0[7:0]}.

Word stored in AC97 Controller Channel x Receive Holding Register (CxRHR) (Received Data).

31 – 24	23 – 20	19 – 16	15 – 8	7 – 0
–	–	Byte2[3:0]	Byte1[7:0]	Byte0[7:0]

Data is read from AC97 Controller Channel x Receive Holding Register (CxRHR) when Channel x data size is greater than 16 bits and when little endian mode is enabled (data written to memory).

31 – 24	23 – 16	15 – 8	7 – 0
Byte0[7:0]	Byte1[7:0]	{0x0, Byte2[3:0]}	0x00

25.7.3.12 To Receive Halfword Transfers

Data received on appropriate slot: data[19:0] = {Byte1[7:0], Byte0[7:0], 0x0 }.

Halfword stored in AC97 Controller Channel x Receive Holding Register (CxRHR) (Received Data).

31 – 24	23 – 16	15 – 8	7 – 0
–	–	Byte1[7:0]	Byte0[7:0]

Data is read from AC97 Controller Channel x Receive Holding Register (CxRHR) when data size is equal to 16 bits and when little endian mode is enabled.

31 – 24	23 – 16	15 – 8	7 – 0
–	–	Byte0[7:0]	Byte1[7:0]

25.7.3.13 To Receive 10-bit Samples

Data received on appropriate slot: data[19:0] = {Byte1[1:0], Byte0[7:0], 0x000}. Halfword stored in AC97 Controller Channel x Receive Holding Register (CxRHR) (Received Data)

31 – 24	23 – 16	15 – 10	9 – 8	7 – 0
–	–	–	Byte1 [1:0]	Byte0[7:0]

Data read from AC97 Controller Channel x Receive Holding Register (CxRHR) when data size is equal to 10 bits and when little endian mode is enabled.

31 – 24	23 – 16	15 – 8	7 – 3	1 – 0
–	–	Byte0[7:0]	0x00	Byte1 [1:0]

25.7.4 Variable Sample Rate

The problem of variable sample rate can be summarized by a simple example. When passing a 44.1 kHz stream across the AC-link, for every 480 audio output frames that are sent across, 441 of them must contain valid sample data. The new AC97 standard approach calls for the addition of “on-demand” slot request flags. The AC97 Codec examines its sample rate control register, the state of its FIFOs, and the incoming SDATA_OUT tag bits (slot 0) of each output frame and then determines which SLOTREQ bits to set active (low). These bits are passed from the AC97 Codec to the AC97 Controller in slot 1/SLOTREQ in every audio input frame. Each time the AC97 controller sees one or more of the newly defined slot request flags set active (low) in a given audio input frame, it must pass along the next PCM sample for the corresponding slot(s) in the AC-link output frame that immediately follows.

The variable Sample Rate mode is enabled by performing the following steps:

- Setting the VRA bit in the AC97 Controller Mode Register (MR).
- Enable Variable Rate mode in the AC97 Codec by performing a transfer on the Codec channel.

Slot 1 of the input frame is automatically interpreted as SLOTREQ signaling bits. The AC97 Controller will automatically fill the active slots according to both SLOTREQ and OCA register in the next transmitted frame.

25.7.5 Power Management

25.7.5.1 Powering Down the AC-Link

The AC97 Codecs can be placed in low power mode. The application can bring AC97 Codec to a power down state by performing sequential writes to AC97 Codec powerdown register . Both the bit clock (clock delivered by AC97 Codec, SCLK) and the input line (SDI) are held at a logic low voltage level. This puts AC97 Codec in power down state while all its registers are still holding current values. Without the bit clock, the AC-link is completely in a power down state.

The AC97 Controller should not attempt to play or capture audio data until it has awakened AC97 Codec.

To set the AC97 Codec in low power mode, the PR4 bit in the AC97 Codec powerdown register (Codec address 0x26) must be set to 1. Then the primary Codec drives both BITCLK and SDI to a low logic voltage level.

The following operations must be done to put AC97 Codec in low power mode:

- Disable Channel A clearing CEN in the CAMR register.
- Disable Channel B clearing CEN field in the CBMR register.
- Write 0x2680 value in the COTHR register.
- Poll the TXEMPTY flag in CxSR registers for the 2 channels.

At this point AC97 Codec is in low power mode.

25.7.5.2 Waking up the AC-link

There are two methods to bring the AC-link out of low power mode. Regardless of the method, it is always the AC97 Controller that performs the wake-up.

25.7.5.3 Wake-up Tiggered by the AC97 Controller

The AC97 Controller can wake up the AC97 Codec by issuing either a cold or a warm reset.

The AC97 Controller can also wake up the AC97 Codec by asserting SYNC signal, however this action should not be performed for a minimum period of four audio frames following the frame in which the powerdown was issued.

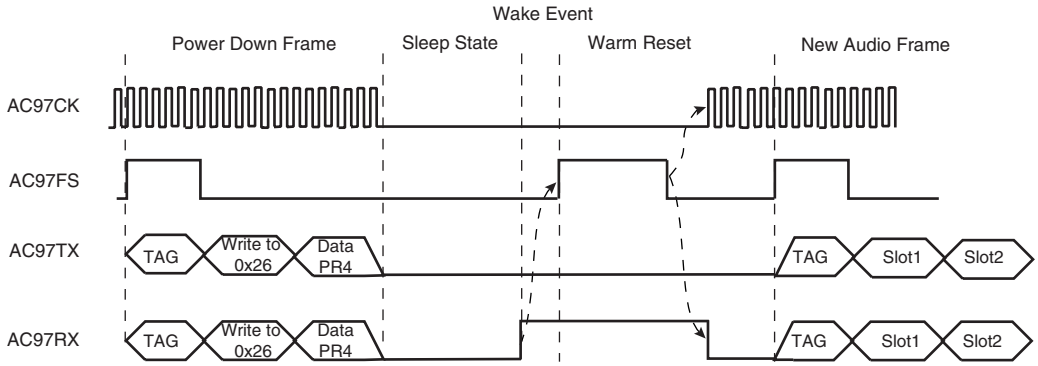
25.7.5.4 Wake-up Triggered by the AC97 Codec

This feature is implemented in AC97 modem codecs that need to report events such as Caller-ID and wake-up on ring.

The AC97 Codec can drive SDI signal from low to high level and holding it high until the controller issues either a cold or a warm reset. The SDI rising edge is asynchronously (regarding SYNC) detected by the AC97 Controller. If WKUP bit is enabled in IMR register, an interrupt is triggered that wakes up the AC97 Controller which should then immediately issue a cold or a warm reset.

If the processor needs to be awakened by an external event, the SDI signal must be externally connected to the WAKEUP entry of the system controller.

Figure 25-7. AC97 Power-Down/Up Sequence



25.7.5.5 AC97 Codec Reset

There are three ways to reset an AC97 Codec.

25.7.5.6 Cold AC97 Reset

A cold reset is generated by asserting the RESET signal low for the minimum specified time (depending on the AC97 Codec) and then by de-asserting RESET high. BITCLK and SYNC is reactivated and all AC97 Codec registers are set to their default power-on values. Transfers on AC-link can resume.

The RESET signal will be controlled via a PIO line. This is how an application should perform a cold reset:

- Clear and set ENA flag in the MR register to reset the AC97 Controller
- Clear PIO line output controlling the AC97 RESET signal
- Wait for the minimum specified time
- Set PIO line output controlling the AC97 RESET signal

BITCLK, the clock provided by AC97 Codec, is detected by the controller.

25.7.5.7 Warm AC97 Reset

A warm reset reactivates the AC-link without altering AC97 Codec registers. A warm reset is signaled by driving AC97FX signal high for a minimum of 1us in the absence of BITCLK. In the absence of BITCLK, AC97FX is treated as an asynchronous (regarding AC97FX) input used to signal a warm reset to AC97 Codec.

This is the right way to perform a warm reset:

- Set WRST in the MR register.
- Wait for at least 1us
- Clear WRST in the MR register.

The application can check that operations have resumed by checking SOF flag in the SR register or wait for an interrupt notice if SOF is enabled in IMR.

25.8 AC97 Controller (AC97C) User Interface

Table 25-4. Register Mapping

Offset	Register	Register Name	Access	Reset
0x0-0x4	Reserved	–	–	–
0x8	Mode Register	MR	Read/Write	0x0
0xC	Reserved	–	–	–
0x10	Input Channel Assignment Register	ICA	Read/Write	0x0
0x14	Output Channel Assignment Register	OCA	Read/Write	0x0
0x18-0x1C	Reserved	–	–	–
0x20	Channel A Receive Holding Register	CARHR	Read	0x0
0x24	Channel A Transmit Holding Register	CATHR	Write	–
0x28	Channel A Status Register	CASR	Read	0x0
0x2C	Channel A Mode Register	CAMR	Read/Write	0x0
0x30	Channel B Receive Holding Register	CBRHR	Read	0x0
0x34	Channel B Transmit Holding Register	CBTHR	Write	–
0x38	Channel B Status Register	CBSR	Read	0x0
0x3C	Channel B Mode Register	CBMR	Read/Write	0x0
0x40	Codec Receive Holding Register	CORHR	Read	0x0
0x44	Codec Transmit Holding Register	COTHR	Write	–
0x48	Codec Status Register	COSR	Read	0x0
0x4C	Codec Mode Register	COMR	Read/Write	0x0
0x50	Status Register	SR	Read	0x0
0x54	Interrupt Enable Register	IER	Write	–
0x58	Interrupt Disable Register	IDR	Write	–
0x5C	Interrupt Mask Register	IMR	Read	0x0
0x60-0xFB	Reserved	–	–	–

25.8.1 AC97 Controller Mode Register

Name: MR

Access Type: Read-Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	VRA	WRST	ENA

- **VRA: Variable Rate (for Data Slots 3-12)**

0: Variable Rate is inactive. (48 KHz only)

1: Variable Rate is active.

- **WRST: Warm Reset**

0: Warm Reset is inactive.

1: Warm Reset is active.

- **ENA: AC97 Controller Global Enable**

0: No effect. AC97 function as well as access to other AC97 Controller registers are disabled.

1: Activates the AC97 function.

25.8.2 AC97 Controller Input Channel Assignment Register

Register Name: ICA

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	CHID12			CHID11		
23	22	21	20	19	18	17	16
CHID10			CHID9			CHID8	
15	14	13	12	11	10	9	8
CHID8	CHID7			CHID6			CHID5
7	6	5	4	3	2	1	0
CHID5		CHID4			CHID3		

- **CHIDx: Channel ID** for the input slot x

CHIDx	Selected Receive Channel
0x0	None. No data will be received during this Slot x
0x1	Channel A data will be received during this slot time.
0x2	Channel B data will be received during this slot time

25.8.3 AC97 Controller Output Channel Assignment Register

Register Name: OCA

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	CHID12			CHID11		
23	22	21	20	19	18	17	16
CHID10			CHID9			CHID8	
15	14	13	12	11	10	9	8
CHID8	CHID7			CHID6			CHID5
7	6	5	4	3	2	1	0
CHID5		CHID4			CHID3		

- **CHIDx: Channel ID** for the output slot x

CHIDx	Selected Transmit Channel
0x0	None. No data will be transmitted during this Slot x
0x1	Channel A data will be transferred during this slot time.
0x2	Channel B data will be transferred during this slot time

25.8.4 AC97 Controller Codec Channel Receive Holding Register

Register Name: CORHR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
SDATA							
7	6	5	4	3	2	1	0
SDATA							

- **SDATA: Status Data**

Data sent by the CODEC in the third AC97 input frame slot (Slot 2).

25.8.5 AC97 Controller Codec Channel Transmit Holding Register

Register Name: COTHR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
READ	CADDR						
15	14	13	12	11	10	9	8
CDATA							
7	6	5	4	3	2	1	0
CDATA							

- **READ: Read/Write command**

0: Write operation to the CODEC register indexed by the CADDR address.

1: Read operation to the CODEC register indexed by the CADDR address.

This flag is sent during the second AC97 frame slot

- **CADDR: CODEC control register index**

Data sent to the CODEC in the second AC97 frame slot.

- **CDATA: Command Data**

Data sent to the CODEC in the third AC97 frame slot (Slot 2).

25.8.6 AC97 Controller Channel A, Channel B Receive Holding Register

Register Name: CARHR, CBRHR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	RDATA			
15	14	13	12	11	10	9	8
RDATA							
7	6	5	4	3	2	1	0
RDATA							

- **RDATA: Receive Data**

Received Data on channel x.

25.8.7 AC97 Controller Channel A, channel B Transmit Holding Register

Register Name: CATHR, CBTHR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	TDATA			
15	14	13	12	11	10	9	8
TDATA							
7	6	5	4	3	2	1	0
TDATA							

- **TDATA: Transmit Data**

Data to be sent on channel x.

25.8.8 AC97 Controller Channel A Status Register

Register Name: CASR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	UNRUN	TXEMPTY	TXRDY

25.8.9 AC97 Controller Channel B Status Register

Register Name: CBSR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	UNRUN	TXEMPTY	TXRDY

25.8.10 AC97 Controller Codec Channel Status Register

Register Name: COSR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	-	TXEMPTY	TXRDY

- **TXRDY: Channel Transmit Ready**

0: Data has been loaded in Channel Transmit Register and is waiting to be loaded in the Channel Transmit Shift Register.

1: Channel Transmit Register is empty.

- **TXEMPTY: Channel Transmit Empty**

0: Data remains in the Channel Transmit Register or is currently transmitted from the Channel Transmit Shift Register.

1: Data in the Channel Transmit Register have been loaded in the Channel Transmit Shift Register and sent to the codec.

- **RXRDY: Channel Receive Ready**

0: Channel Receive Holding Register is empty.

1: Data has been received and loaded in Channel Receive Holding Register.

- **OVRUN: Receive Overrun**

Automatically cleared by a processor read operation.

0: No data has been loaded in the Channel Receive Holding Register while previous data has not been read since the last read of the Status Register.

1: Data has been loaded in the Channel Receive Holding Register while previous data has not yet been read since the last read of the Status Register.

25.8.11 AC97 Controller Channel A Mode Register

Register Name: CAMR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	DMAEN	CEN	–	–	CEM	SIZE	
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	UNRUN	TXEMPTY	TXRDY

- **DMAEN: DMA Enable**

0: Disable DMA transfers for this channel.

1: Enable DMA transfers for this channel using DMAC.

- **CEM: Channel A Endian Mode**

0: Transferring Data through Channel A is straight forward (Big Endian).

1: Transferring Data through Channel A from/to a memory is performed with from/to Little Endian format translation.

- **SIZE: Channel A Data Size**

SIZE Encoding

SIZE	Selected Channel
0x0	20 bits
0x1	18bits
0x2	16 bits
0x3	10 bits

Note: Each time slot in the data phase is 20 bit long. For example, if a 16-bit sample stream is being played to an AC 97 DAC, the first 16 bit positions are presented to the DAC MSB-justified. They are followed by the next four bit positions that the AC97 Controller fills with zeroes. This process ensures that the least significant bits do not introduce any DC biasing, regardless of the implemented DAC's resolution (16-, 18-, or 20-bit).

- **CEN: Channel A Enable**

0: Data transfer is disabled on Channel A.

1: Data transfer is enabled on Channel A.

25.8.12 AC97 Controller Channel B Mode Register

Register Name: CBMR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	DMAEN	CEN	–	–	CEM	SIZE	
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	UNRUN	TXEMPTY	TXRDY

- **DMAEN: DMA Enable**

0: Disable DMA transfers for this channel.

1: Enable DMA transfers for this channel using DMAC.

- **CEM: Channel B Endian Mode**

0: Transferring Data through Channel B is straight forward (Big Endian).

1: Transferring Data through Channel B from/to a memory is performed with from/to Little Endian format translation.

- **SIZE: Channel B Data Size**

SIZE Encoding

SIZE	Selected Channel
0x0	20 bits
0x1	18bits
0x2	16 bits
0x3	10 bits

Note: Each time slot in the data phase is 20 bit long. For example, if a 16-bit sample stream is being played to an AC 97 DAC, the first 16 bit positions are presented to the DAC MSB-justified. They are followed by the next four bit positions that the AC97 Controller fills with zeroes. This process ensures that the least significant bits do not introduce any DC biasing, regardless of the implemented DAC's resolution (16-, 18-, or 20-bit).

- **CEN: Channel B Enable**

0: Data transfer is disabled on Channel B.

1: Data transfer is enabled on Channel B.

25.8.13 AC97 Controller Codec Channel Mode Register

Register Name: COMR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	OVRUN	RXRDY	–	-	TXEMPTY	TXRDY

- **TXRDY: Channel Transmit Ready Interrupt Enable**
- **TXEMPTY: Channel Transmit Empty Interrupt Enable**
- **RXRDY: Channel Receive Ready Interrupt Enable**
- **OVRUN: Receive Overrun Interrupt Enable**

0: Read: the corresponding interrupt is disabled. Write: disables the corresponding interrupt.

1: Read: the corresponding interrupt is enabled. Write: enables the corresponding interrupt.

25.8.14 AC97 Controller Status Register

Register Name: SR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	CBEVT	CAEVT	COEVT	WKUP	SOF

WKUP and SOF flags in SR register are automatically cleared by a processor read operation.

- **SOF: Start Of Frame**

0: No Start of Frame has been detected since the last read of the Status Register.

1: At least one Start of frame has been detected since the last read of the Status Register.

- **WKUP: Wake Up detection**

0: No Wake-up has been detected.

1: At least one rising edge on SDATA_IN has been asynchronously detected. That means AC97 Codec has notified a wake-up.

- **COEVT: CODEC Channel Event**

A Codec channel event occurs when COSR AND COMR is not 0. COEVT flag is automatically cleared when the channel event condition is cleared.

0: No event on the CODEC channel has been detected since the last read of the Status Register.

1: At least one event on the CODEC channel is active.

- **CAEVT: Channel A Event**

A channel A event occurs when CASR AND CAMR is not 0. CAEVT flag is automatically cleared when the channel event condition is cleared.

0: No event on the channel A has been detected since the last read of the Status Register.

1: At least one event on the channel A is active.

- **CBEVT: Channel B Event**

A channel B event occurs when CBSR AND CBMR is not 0. CBEVT flag is automatically cleared when the channel event condition is cleared.

0: No event on the channel B has been detected since the last read of the Status Register.

1: At least one event on the channel B is active.

25.8.15 AC97 Controller Interrupt Enable Register

Register Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	CBEVT	CAEVT	COEVT	WKUP	SOF

- **SOF: Start Of Frame**
- **WKUP: Wake Up**
- **COEVT: Codec Event**
- **CAEVT: Channel A Event**
- **CBEVT: Channel B Event**

0: No Effect.

1: Enables the corresponding interrupt.

25.8.16 AC97 Controller Interrupt Disable Register

Register Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	CBEVT	CAEVT	COEVT	WKUP	SOF

- **SOF: Start Of Frame**
- **WKUP: Wake Up**
- **COEVT: Codec Event**
- **CAEVT: Channel A Event**
- **CBEVT: Channel B Event**

0: No Effect.

1: Disables the corresponding interrupt.

25.8.17 AC97 Controller Interrupt Mask Register

Register Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	CBEVT	CAEVT	COEVT	WKUP	SOF

- **SOF: Start Of Frame**
- **WKUP: Wake Up**
- **COEVT: Codec Event**
- **CAEVT: Channel A Event**
- **CBEVT: Channel B Event**

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

26. Audio Bitstream DAC (ABDAC)

Rev: 1.0.1.1

26.1 Features

- **Digital Stereo DAC**
- **Oversampled D/A conversion architecture**
  - **Oversampling ratio fixed 128x**
  - **FIR equalization filter**
  - **Digital interpolation filter: Comb4**
  - **3rd Order Sigma-Delta D/A converters**
- **Digital bitstream outputs**
- **Parallel interface**
- **Connected to DMA Controller for background transfer without CPU intervention**

26.2 Description

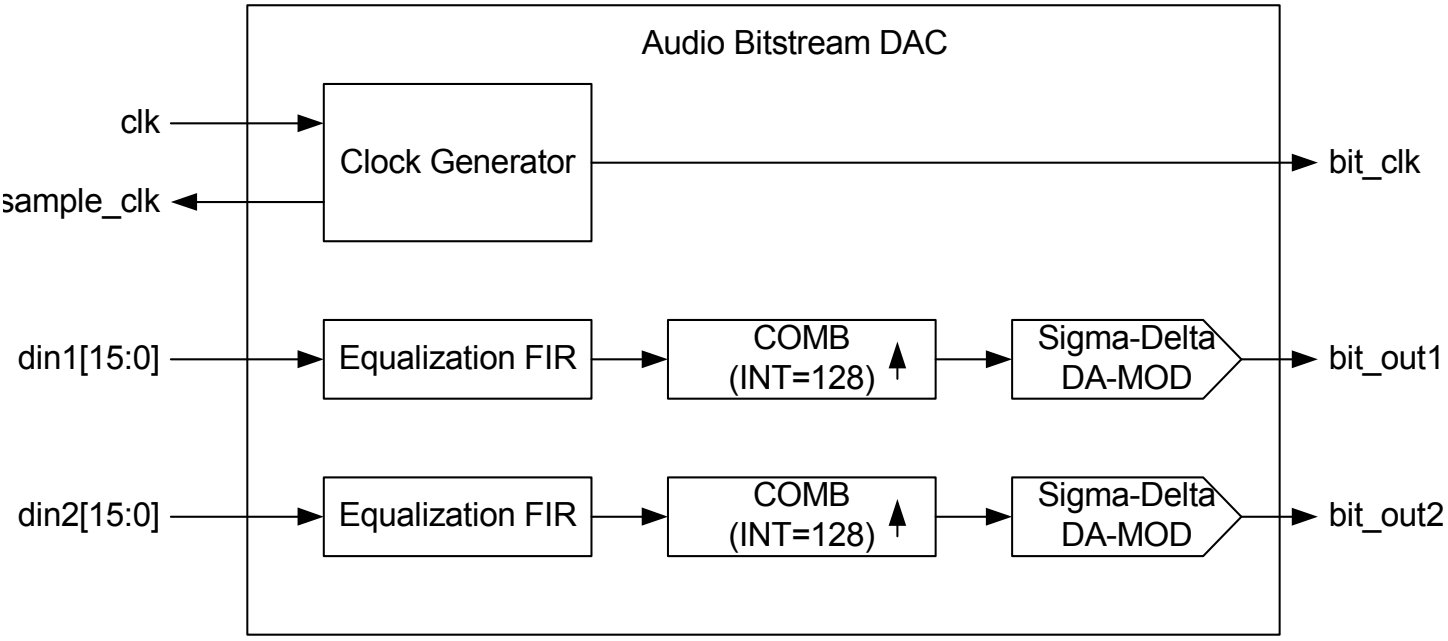
The Audio Bitstream DAC converts a 16-bit sample value to a digital bitstream with an average value proportional to the sample value. Two channels are supported, making the Audio Bitstream DAC particularly suitable for stereo audio. Each channel has a pair of complementary digital outputs, DACn and DACn_N, which can be connected to an external high input impedance amplifier.

The Audio Bitstream DAC is compromised of two 3rd order Sigma Delta D/A converter with an oversampling ratio of 128. The samples are upsampled with a 4th order Sinc interpolation filter (Comb4) before being input to the Sigmal Delta Modulator. In order to compensate for the pass band frequency response of the interpolation filter and flatten the overall frequency response, the input to the interpolation filter is first filtered with a simple 3-tap FIR filter.The total frequency response of the Equalization FIR filter and the interpolation filter is given in Figure 26-2 on page 491. The digital output bitstreams from the Sigma Delta Modulators should be low-pass filtered to remove high frequency noise inserted by the Modulation process.

The output DACn and DACn_N should be as ideal as possible before filtering, to achieve the best SNR quality. The output can be connected to a class D amplifier output stage, or it can be low pass filtered and connected to a high input impedance amplifier. A simple 1st order or higher low pass filter that filters all the frequencies above 50 kHz should be adequate.

26.3 Block Diagram

Figure 26-1. Functional Block Diagram



26.4 Pin Name List

Table 26-1. I/O Lines Description

Pin Name	Pin Description	Type
DATA0	Output from Audio Bitstream DAC Channel 0	Output
DATA1	Output from Audio Bitstream DAC Channel 1	Output
DATAN0	Inverted output from Audio Bitstream DAC Channel 0	Output
DATAN1	Inverted output from Audio Bitstream DAC Channel 1	Output

26.5 Product Dependencies

26.5.1 I/O Lines

The output pins used for the output bitstream from the Audio Bitstream DAC may be multiplexed with PIO lines.

Before using the Audio Bitstream DAC, the PIO controller must be configured in order for the Audio Bitstream DAC I/O lines to be in Audio Bitstream DAC peripheral mode.

26.5.2 Power Management

The PB-bus clock to the Audio Bitstream DAC is generated by the power manager. Before using the Audio Bitstream DAC, the programmer must ensure that the Audio Bitstream DAC clock is enabled in the power manager.

26.5.3 Clock Management

The Audio Bitstream DAC needs a separate clock for the D/A conversion operation. This clock should be set up in the generic clock register in the power manager. The frequency of this clock must be 256 times the frequency of the desired samplerate (f_s). For f_s=48kHz this means that the clock must have a frequency of 12.288MHz.

26.5.4 Interrupts

The Audio Bitstream DAC interface has an interrupt line connected to the interrupt controller. In order to handle interrupts, the interrupt controller must be programmed before configuring the Audio Bitstream DAC.

All Audio Bitstream DAC interrupts can be enabled/disabled by writing to the Audio Bitstream DAC Interrupt Enable/Disable Registers. Each pending and unmasked Audio Bitstream DAC interrupt will assert the interrupt line. The Audio Bitstream DAC interrupt service routine can get the interrupt source by reading the Interrupt Status Register.

26.5.5 DMA

The Audio Bitstream DAC is connected to the DMA controller. The DMA controller can be programmed to automatically transfer samples to the Audio Bitstream DAC Sample Data Register (SDR) when the Audio Bitstream DAC is ready for new samples. This enables the Audio Bitstream DAC to operate without any CPU intervention such as polling the Interrupt Status Register (ISR) or using interrupts. See the DMA controller documentation for details on how to setup DMA transfers.

26.6 Functional Description

In order to use the Audio Bitstream DAC the product dependencies given in Section 26.5 on page 480 must be resolved. Particular attention should be given to the configuration of clocks and I/O lines in order to ensure correct operation of the Audio Bitstream DAC.

The Audio Bitstream DAC is enabled by writing the ENABLE bit in the Audio Bitstream DAC Control Register (CR). The two 16-bit sample values for channel 0 and 1 can then be written to the least and most significant halfword of the Sample Data Register (SDR), respectively. The TX_READY bit in the Interrupt Status Register (ISR) will be set whenever the DAC is ready to receive a new sample. A new sample value should be written to SDR before 256 DAC clock cycles, or an underrun will occur, as indicated by the UNDERRUN status flags in ISR. ISR is cleared when read, or when writing one to the corresponding bits in the Interrupt Clear Register (ICR).

For interrupt-based operation, the relevant interrupts must be enabled by writing one to the corresponding bits in the Interrupt Enable Register (IER). Interrupts can be disabled by the Interrupt Disable Register (IDR), and active interrupts are indicated in the read-only Interrupt Mask Register (IMR).

The Audio Bitstream DAC can also be configured for peripheral DMA access, in which case only the enable bit in the control register needs to be set in the Audio Bitstream DAC module.

26.6.1 Equalization Filter

The equalization filter is a simple 3-tap FIR filter. The purpose of this filter is to compensate for the pass band frequency response of the sinc interpolation filter. The equalization filter makes the pass band response more flat and moves the -3dB corner a little higher.

26.6.2 Interpolation filter

The interpolation filter interpolates from f_s to $128f_s$. This filter is a 4th order Cascaded Integrator-Comb filter, and the basic building blocks of this filter is a comb part and an integrator part.

26.6.3 Sigma Delta Modulator

This part is a 3rd order Sigma Delta Modulator consisting of three differentiators (delta blocks), three integrators (sigma blocks) and a one bit quantizer. The purpose of the integrators is to shape the noise, so that the noise is reduces in the band of interest and increased at the higher frequencies, where it can be filtered.

26.6.4 Data Format

Input data is on two's complement format.

26.7 Audio Bitstream DAC User Interface

Table 26-2. Register Mapping

Offset	Register	Register Name	Access	Reset
0x0	Sample Data Register	SDR	Read/Write	0x0
0x4	Reserved	-	-	-
0x8	Control Register	CR	Read/Write	0x0
0xc	Interrupt Mask Register	IMR	Read	0x0
0x10	Interrupt Enable Register	IER	Write	-
0x14	Interrupt Disable Register	IDR	Write	-
0x18	Interrupt Clear Register	ICR	Write	-
0x1C	Interrupt Status Register	ISR	Read	0x0

26.7.1 Audio Bitstream DAC Sample Data Register

Name: SDR

Access Type: Read-Write

31	30	29	28	27	26	25	24
CHANNEL1							
23	22	21	20	19	18	17	16
CHANNEL1							
15	14	13	12	11	10	9	8
CHANNEL0							
7	6	5	4	3	2	1	0
CHANNEL0							

- **CHANNEL0: Sample Data for Channel 0**

Signed 16-bit Sample Data for channel 0. When the SWAP bit in the DAC Control Register (CR) is set writing to the Sample Data Register (SDR) will cause the values written to CHANNEL0 and CHANNEL1 to be swapped.

- **CHANNEL1: Sample Data for Channel 1**

Signed 16-bit Sample Data for channel 1. When the SWAP bit in the DAC Control Register (CR) is set writing to the Sample Data Register (SDR) will cause the values written to CHANNEL0 and CHANNEL1 to be swapped.

26.7.2 Audio Bitstream DAC Control Register

Name: CR

Access Type: Read-Write

31	30	29	28	27	26	25	24
EN	SWAP	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

- **SWAP: Swap Channels**

0: The CHANNEL0 and CHANNEL1 samples will not be swapped when writing the Audio Bitstream DAC Sample Data Register (SDR).

1: The CHANNEL0 and CHANNEL1 samples will be swapped when writing the Audio Bitstream DAC Sample Data Register (SDR).

- **EN: Enable Audio Bitstream DAC**

0: Audio Bitstream DAC is disabled.

1: Audio Bitstream DAC is enabled.

26.7.3 Audio Bitstream DAC Interrupt Mask Register

Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
-	-	TX_READY	UNDERRUN	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

- **UNDERRUN: Underrun Interrupt Mask**

0: The Audio Bitstream DAC Underrun interrupt is disabled.

1: The Audio Bitstream DAC Underrun interrupt is enabled.

- **TX_READY: TX Ready Interrupt Mask**

0: The Audio Bitstream DAC TX Ready interrupt is disabled.

1: The Audio Bitstream DAC TX Ready interrupt is enabled.

26.7.4 Audio Bitstream DAC Interrupt Enable Register

Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
-	-	TX_READY	UNDERRUN	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

- **UNDERRUN: Underrun Interrupt Enable**

0: No effect.

1: Enables the Audio Bitstream DAC Underrun interrupt.

- **TX_READY: TX Ready Interrupt Enable**

0: No effect.

1: Enables the Audio Bitstream DAC TX Ready interrupt.

26.7.5 Audio Bitstream DAC Interrupt Disable Register

Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
-	-	TX_READY	UNDERRUN	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

- **UNDERRUN: Underrun Interrupt Disable**

0: No effect.

1: Disable the Audio Bitstream DAC Underrun interrupt.

- **TX_READY: TX Ready Interrupt Disable**

0: No effect.

1: Disable the Audio Bitstream DAC TX Ready interrupt.

26.7.6 Audio Bitstream DAC Interrupt Clear Register

Name: ICR

Access Type: Write-only

31	30	29	28	27	26	25	24
-	-	TX_READY	UNDERRUN	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

- **UNDERRUN: Underrun Interrupt Clear**

0: No effect.

1: Clear the Audio Bitstream DAC Underrun interrupt.

- **TX_READY: TX Ready Interrupt Clear**

0: No effect.

1: Clear the Audio Bitstream DAC TX Ready interrupt.

26.7.7 Audio Bitstream DAC Interrupt Status Register

Name: ISR

Access Type: Read-only

31	30	29	28	27	26	25	24
-	-	TX_READY	UNDERRUN	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

- **UNDERRUN: Underrun Interrupt Status**

0: No Audio Bitstream DAC Underrun has occured since the last time ISR was read or since reset.

1: At least one Audio Bitstream DAC Underrun has occured since the last time ISR was read or since reset.

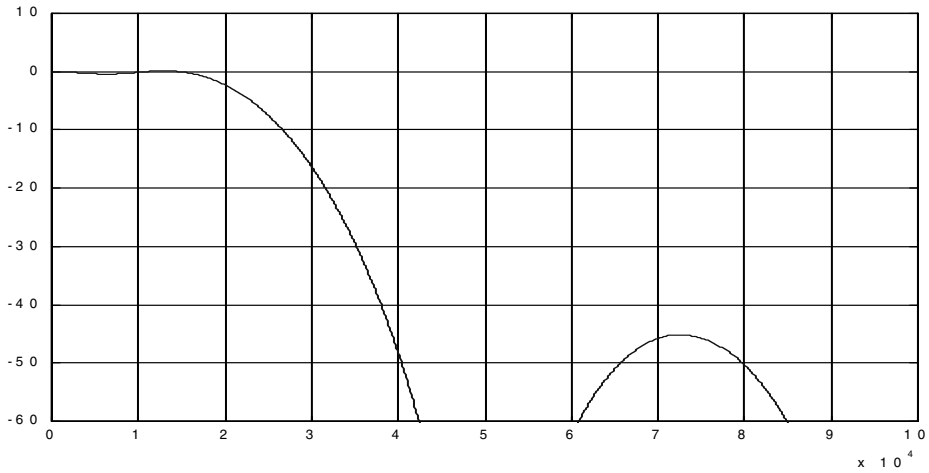
- **TX_READY: TX Ready Interrupt Status**

0: No Audio Bitstream DAC TX Ready has occuredt since the last time ISR was read.

1: At least one Audio Bitstream DAC TX Ready has occuredt since the last time ISR was read.

26.8 Frequency Response

Figure 26-2. Frequecy response, EQ-FIR+COMB[4]



27. Static Memory Controller (SMC)

Rev. 1.0.0.3

27.1 Features

- **6 chip selects available**
- **64-Mbytes address space per chip select**
- **8-, 16- or 32-bit data bus**
- **Word, halfword, byte transfers**
- **Byte write or byte select lines**
- **Programmable setup, pulse and hold time for read signals per chip select**
- **Programmable setup, pulse and hold time for write signals per chip select**
- **Programmable data float time per chip select**
- **Compliant with LCD module**
- **External wait request**
- **Automatic switch to slow clock mode**
- **Asynchronous read in page mode supported: page size ranges from 4 to 32 bytes**

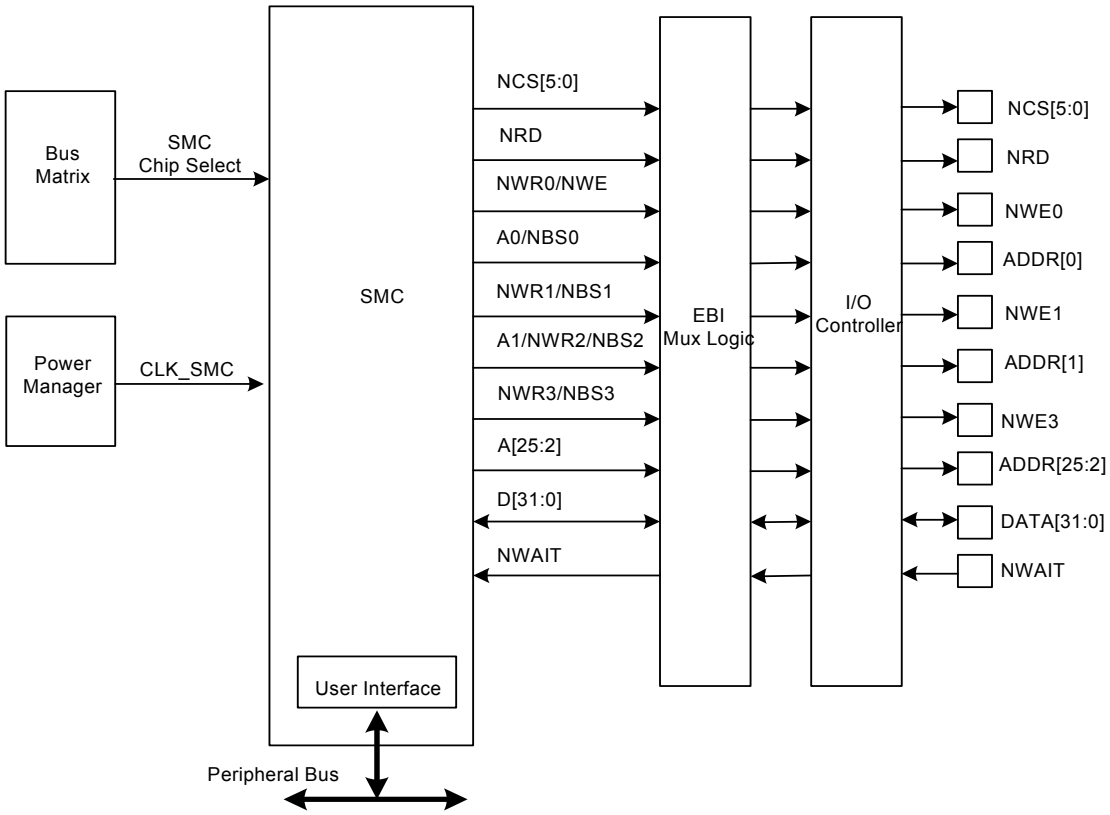
27.2 Overview

The Static Memory Controller (SMC) generates the signals that control the access to the external memory devices or peripheral devices. It has 6 chip selects and a 26-bit address bus. The 32-bit data bus can be configured to interface with 8-, or16-, or 32-bit external devices. Separate read and write control signals allow for direct memory and peripheral interfacing. Read and write signal waveforms are fully parametrizable.

The SMC can manage wait requests from external devices to extend the current access. The SMC is provided with an automatic slow clock mode. In slow clock mode, it switches from user-programmed waveforms to slow-rate specific waveforms on read and write signals. The SMC supports asynchronous burst read in page mode access for page size up to 32 bytes.

27.3 Block Diagram

Figure 27-1. SMC Block Diagram



27.4 I/O Lines Description

Table 27-1. I/O Lines Description

Pin Name	Pin Description	Type	Active Level
NCS[5:0]	Chip Select Lines	Output	Low
NRD	Read Signal	Output	Low
NWR0/NWE	Write 0/Write Enable Signal	Output	Low
A0/NBS0	Address Bit 0/Byte 0 Select Signal	Output	Low
NWR1/NBS1	Write 1/Byte 1 Select Signal	Output	Low
A1/NWR2/NBS2	Address Bit 1/Write 2/Byte 2 Select Signal	Output	Low
NWR3/NBS3	Write 3/Byte 3 Select Signal	Output	Low
A[25:2]	Address Bus	Output	
D[31:0]	Data Bus	Input/Output	
NWAIT	External Wait Signal	Input	Low

27.5 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

27.5.1 I/O Lines

The SMC signals pass through the External Bus Interface (EBI) module where they are multiplexed. The user must first configure the I/O Controller to assign the EBI pins corresponding to SMC signals to their peripheral function. If the I/O lines of the EBI corresponding to SMC signals are not used by the application, they can be used for other purposes by the I/O Controller.

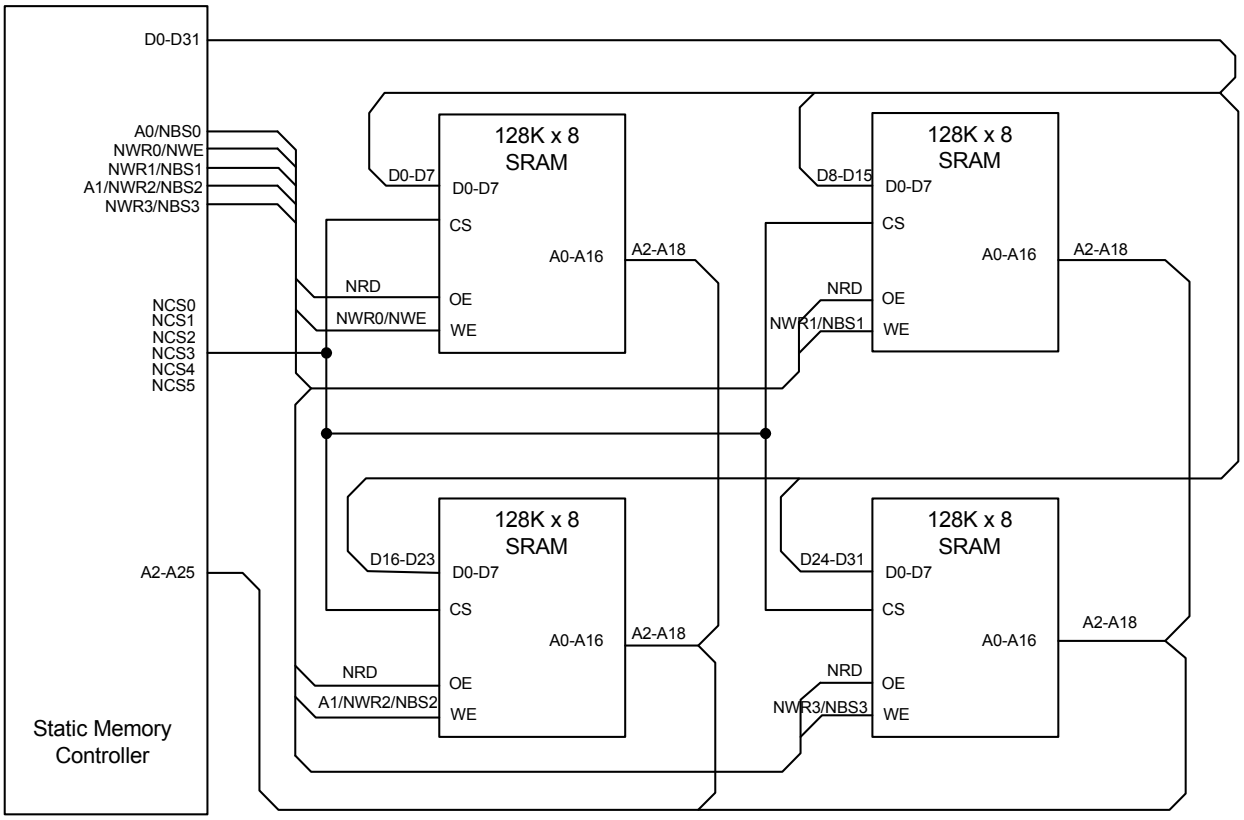
27.5.2 Clocks

The clock for the SMC bus interface (CLK_SMC) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager. It is recommended to disable the SMC before disabling the clock, to avoid freezing the SMC in an undefined state.

27.6 Functional Description

27.6.1 Application Example

Figure 27-2. SMC Connections to Static Memory Devices



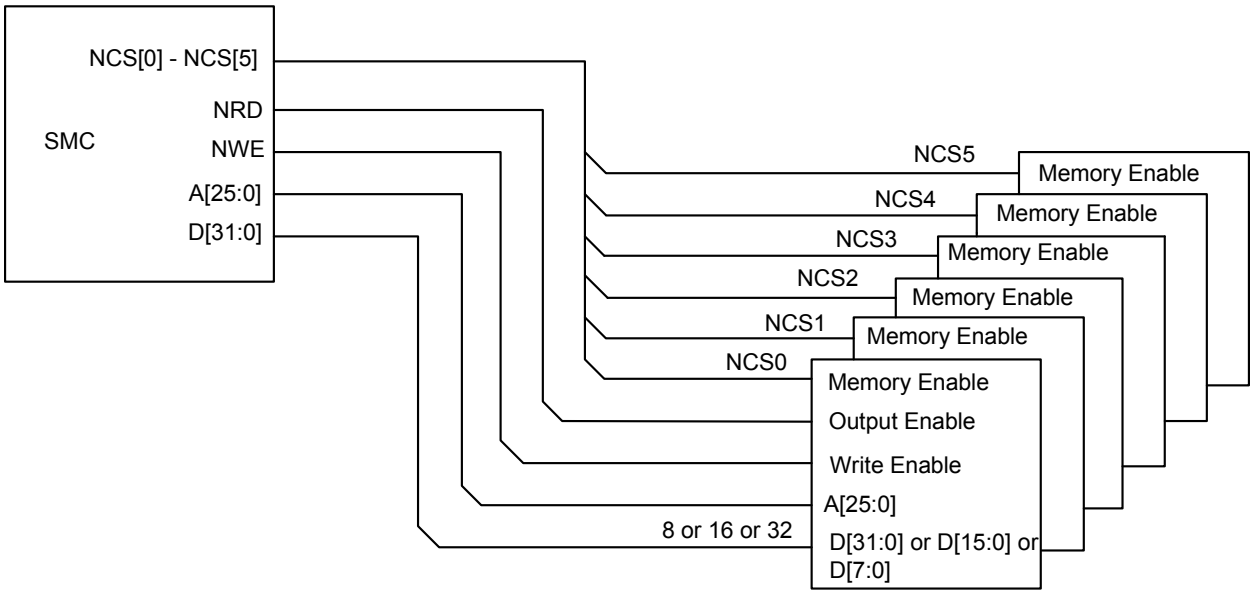
27.6.2 External Memory Mapping

The SMC provides up to 26 address lines, A[25:0]. This allows each chip select line to address up to 64 Mbytes of memory.

If the physical memory device connected on one chip select is smaller than 64Mbytes, it wraps around and appears to be repeated within this space. The SMC correctly handles any valid access to the memory device within the page (see Figure 27-3 on page 495).

A[25:0] is only significant for 8-bit memory, A[25:1] is used for 16-bit memory, A[25:2] is used for 32-bit memory.

Figure 27-3. Memory Connections for Six External Devices



27.6.3 Connection to External Devices

27.6.3.1 Data bus width

A data bus width of 8, 16, or 32 bits can be selected for each chip select. This option is controlled by the Data Bus Width field in the Mode Register (MODE.DBW) for the corresponding chip select.

Figure 27-4 on page 496 shows how to connect a 512K x 8-bit memory on NCS2. Figure 27-5 on page 496 shows how to connect a 512K x 16-bit memory on NCS2. Figure 27-6 shows two 16-bit memories connected as a single 32-bit memory.

27.6.3.2 Byte write or byte select access

Each chip select with a 16-bit or 32-bit data bus can operate with one of two different types of write access: byte write or byte select access. This is controlled by the Byte Access Type bit in the MODE register (MODE.BAT) for the corresponding chip select.

Figure 27-4. Memory Connection for an 8-bit Data Bus

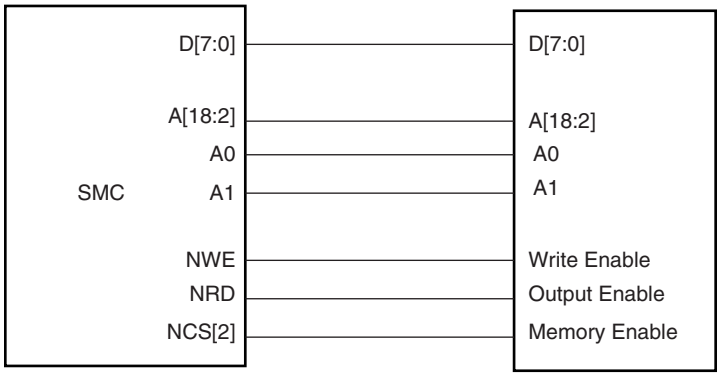


Figure 27-5. Memory Connection for a 16-bit Data Bus

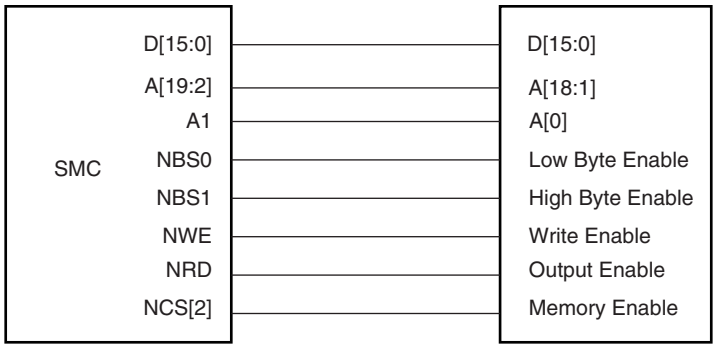
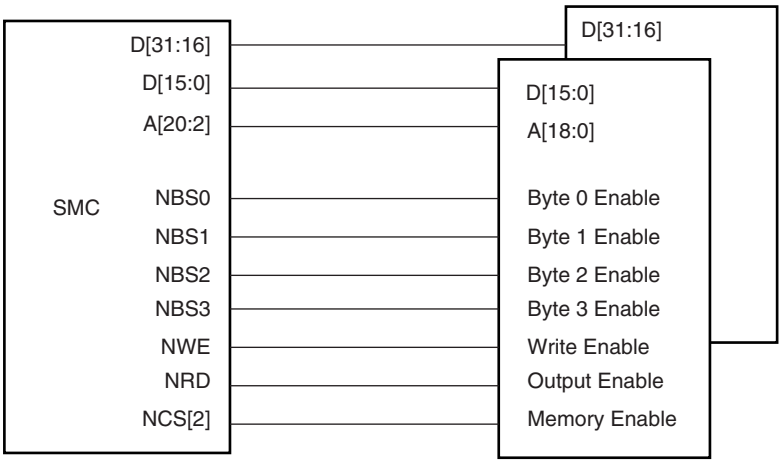


Figure 27-6. Memory Connection for a 32-bit Data Bus



•Byte write access

The byte write access mode supports one byte write signal per byte of the data bus and a single read signal.

Note that the SMC does not allow boot in byte write access mode.

- For 16-bit devices: the SMC provides NWR0 and NWR1 write signals for respectively byte0 (lower byte) and byte1 (upper byte) of a 16-bit bus. One single read signal (NRD) is provided.

The byte write access mode is used to connect two 8-bit devices as a 16-bit memory.

- For 32-bit devices: NWR0, NWR1, NWR2 and NWR3, are the write signals of byte0 (lower byte), byte1, byte2, and byte 3 (upper byte) respectively. One single read signal (NRD) is provided. The byte write access is used to connect four 8-bit devices as a 32-bit memory.

The byte write option is illustrated on Figure 27-7 on page 497.

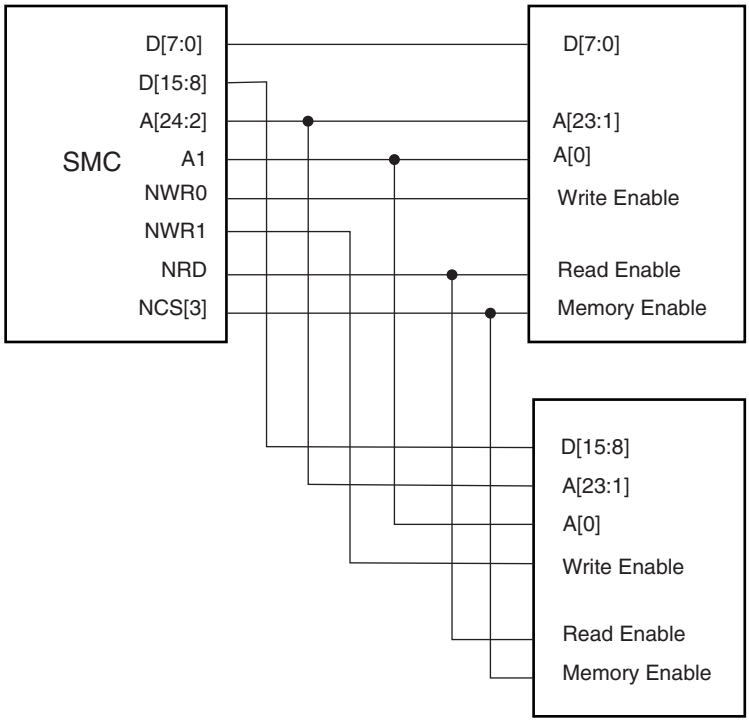
•Byte select access

In this mode, read/write operations can be enabled/disabled at a byte level. One byte select line per byte of the data bus is provided. One NRD and one NWE signal control read and write.

- For 16-bit devices: the SMC provides NBS0 and NBS1 selection signals for respectively byte0 (lower byte) and byte1 (upper byte) of a 16-bit bus. The byte select access is used to connect one 16-bit device.
- For 32-bit devices: NBS0, NBS1, NBS2 and NBS3, are the selection signals of byte0 (lower byte), byte1, byte2, and byte 3 (upper byte) respectively. The byte select access is used to connect two 16-bit devices.

Figure 27-8 on page 498 shows how to connect two 16-bit devices on a 32-bit data bus in byte select access mode, on NCS3.

Figure 27-7. Connection of two 8-bit Devices on a 16-bit Bus: Byte Write Option



•Signal multiplexing

Depending on the MODE.BAT bit, only the write signals or the byte select signals are used. To save I/Os at the external bus interface, control signals at the SMC interface are multiplexed.

For 32-bit devices, bits A0 and A1 are unused. For 16-bit devices, bit A0 of address is unused. When byte select option is selected, NWR1 to NWR3 are unused. When byte write option is selected, NBS0 to NBS3 are unused.

Figure 27-8. Connection of two 16-bit Data Bus on a 32-bit Data Bus: Byte Select Option

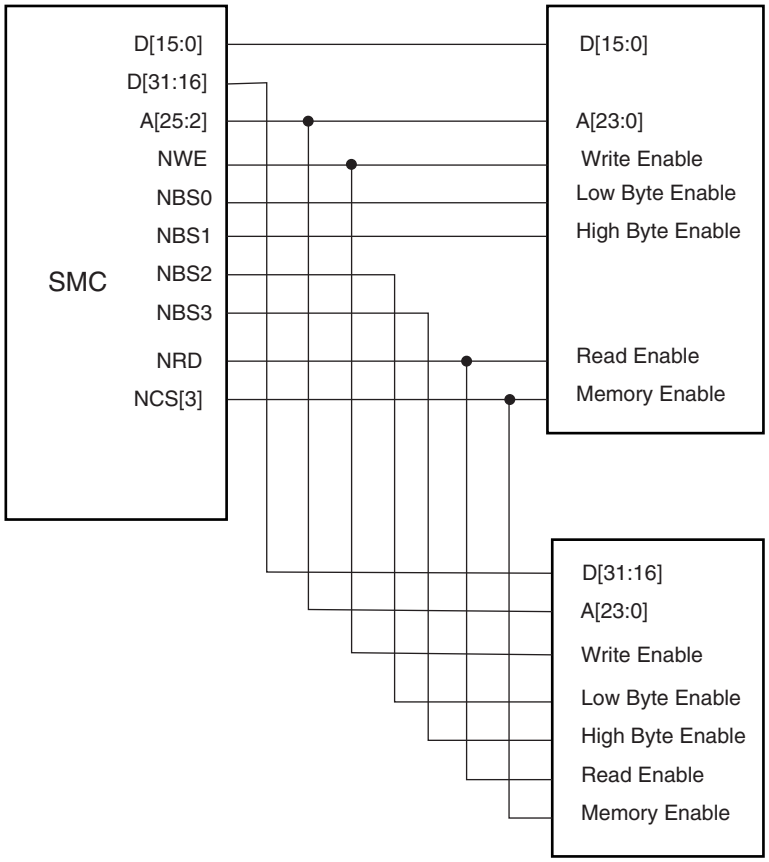


Table 27-2. SMC Multiplexed Signal Translation

Signal Name	32-bit Bus			16-bit Bus		8-bit Bus
Device Type	**1 x 32-bit**	**2 x 16-bit**	**4 x 8-bit**	**1 x 16-bit**	**2 x 8-bit**	**1 x 8-bit**
Byte Access Type (BAT)	Byte Select	Byte Select	Byte Write	Byte Select	Byte Write	
NBS0_A0	NBS0	NBS0		NBS0		A0
NWE_NWR0	NWE	NWE	NWR0	NWE	NWR0	NWE
NBS1_NWR1	NBS1	NBS1	NWR1	NBS1	NWR1	
NBS2_NWR2_A1	NBS2	NBS2	NWR2	A1	A1	A1
NBS3_NWR3	NBS3	NBS3	NWR3			

27.6.4 Standard Read and Write Protocols

In the following sections, the byte access type is not considered. Byte select lines (NBS0 to NBS3) always have the same timing as the address bus (A). NWE represents either the NWE signal in byte select access type or one of the byte write lines (NWR0 to NWR3) in byte write access type. NWR0 to NWR3 have the same timings and protocol as NWE. In the same way, NCS represents one of the NCS[0..5] chip select lines.

27.6.4.1 Read waveforms

The read cycle is shown on Figure 27-9 on page 499.

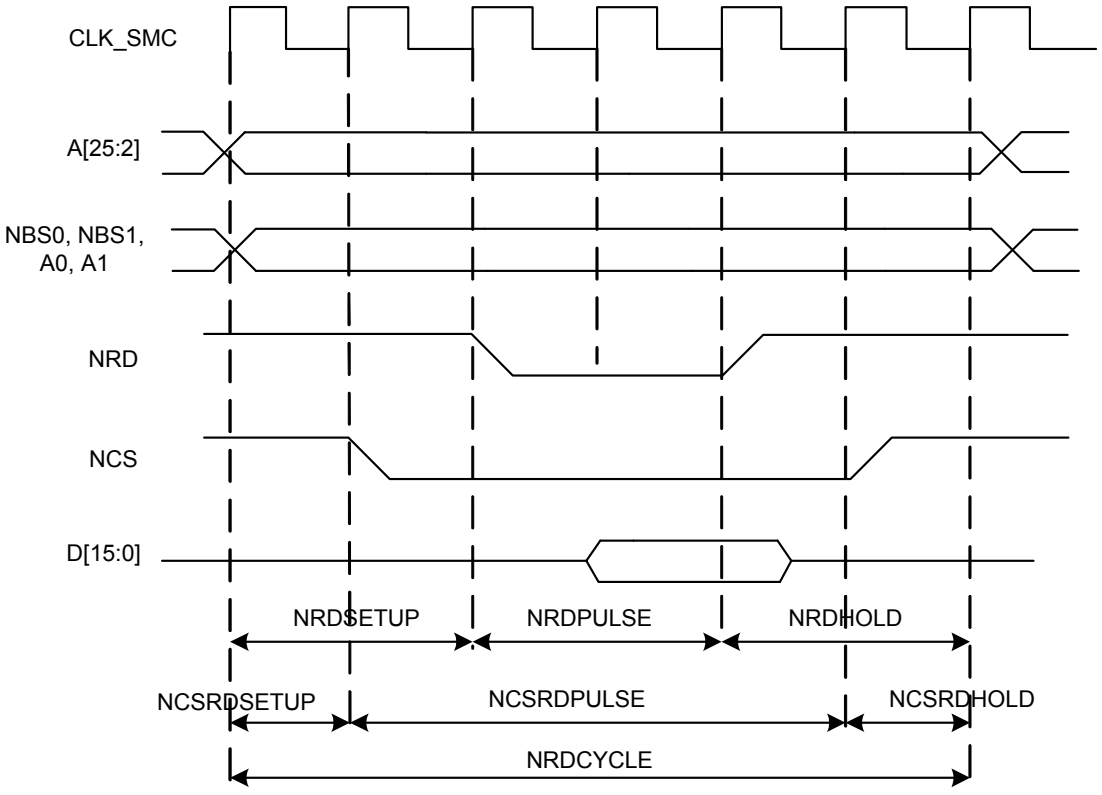
The read cycle starts with the address setting on the memory address bus, i.e.:

{A[25:2], A1, A0} for 8-bit devices

{A[25:2], A1} for 16-bit devices

A[25:2] for 32-bit devices.

Figure 27-9. Standard Read Cycle



•NRD waveform

The NRD signal is characterized by a setup timing, a pulse width, and a hold timing.

1. NRDSETUP: the NRD setup time is defined as the setup of address before the NRD falling edge.
2. NRDPULSE: the NRD pulse length is the time between NRD falling edge and NRD rising edge.

3. NRDHOLD: the NRD hold time is defined as the hold time of address after the NRD rising edge.

•NCS waveform

Similarly, the NCS signal can be divided into a setup time, pulse length and hold time.

1. NCSRDSETUP: the NCS setup time is defined as the setup time of address before the NCS falling edge.
2. NCSRDPULSE: the NCS pulse length is the time between NCS falling edge and NCS rising edge.
3. NCSRDHOLD: the NCS hold time is defined as the hold time of address after the NCS rising edge.

•Read cycle

The NRDCYCLE time is defined as the total duration of the read cycle, i.e., from the time where address is set on the address bus to the point where address may change. The total read cycle time is equal to:

$$NRDCYCLE = NRDSETUP + NRDPULSE + NRDHOLD$$

Similarly,

$$NRDCYCLE = NCSRDSETUP + NCSRDPULSE + NCSRDHOLD$$

All NRD and NCS timings are defined separately for each chip select as an integer number of CLK_SMC cycles. To ensure that the NRD and NCS timings are coherent, the user must define the total read cycle instead of the hold timing. NRDCYCLE implicitly defines the NRD hold time and NCS hold time as:

$$NRDHOLD = NRDCYCLE - NRDSETUP - NRDPULSE$$

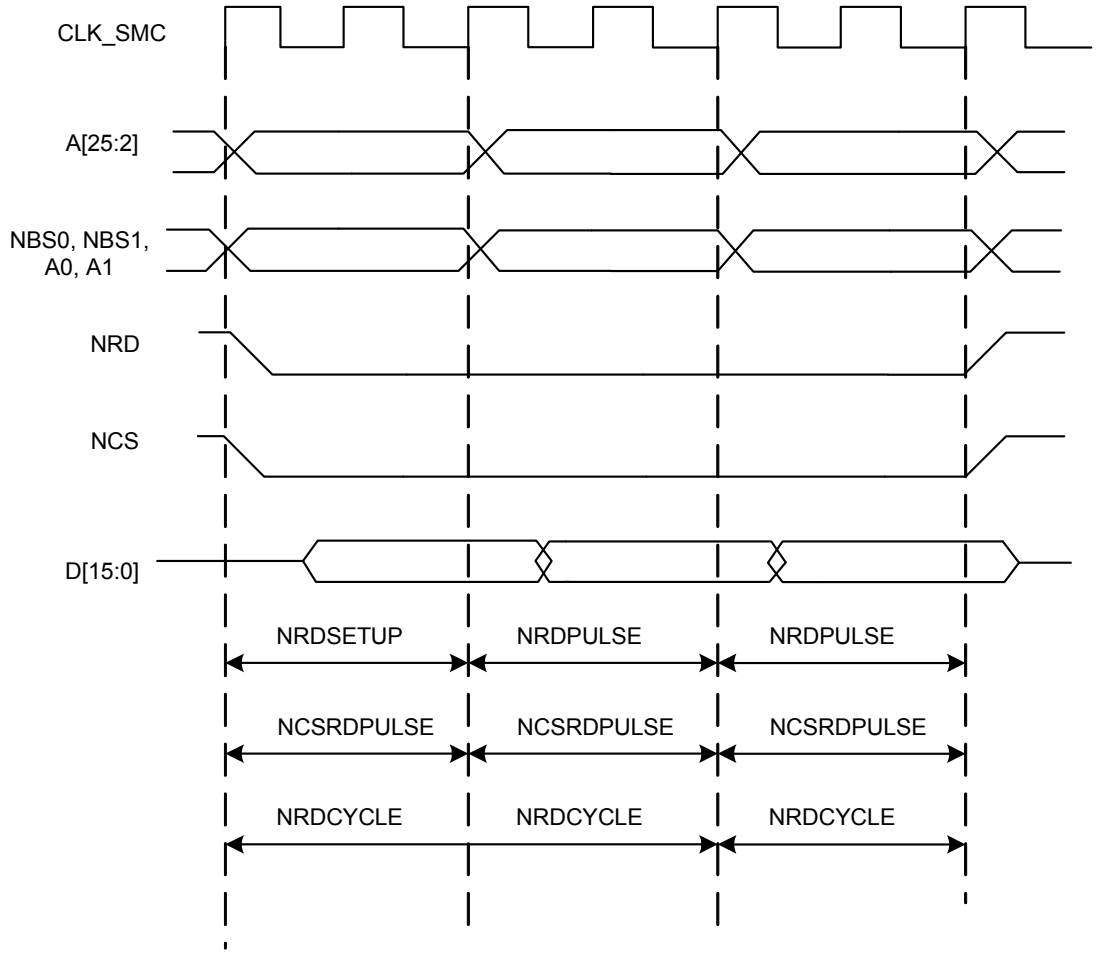
And,

$$NCSRDHOLD = NRDCYCLE - NCSRDSETUP - NCSRDPULSE$$

•Null delay setup and hold

If null setup and hold parameters are programmed for NRD and/or NCS, NRD and NCS remain active continuously in case of consecutive read cycles in the same memory (see Figure 27-10 on page 501).

Figure 27-10. No Setup, No Hold on NRD, and NCS Read Signals



•Null Pulse

Programming null pulse is not permitted. Pulse must be at least written to one. A null value leads to unpredictable behavior.

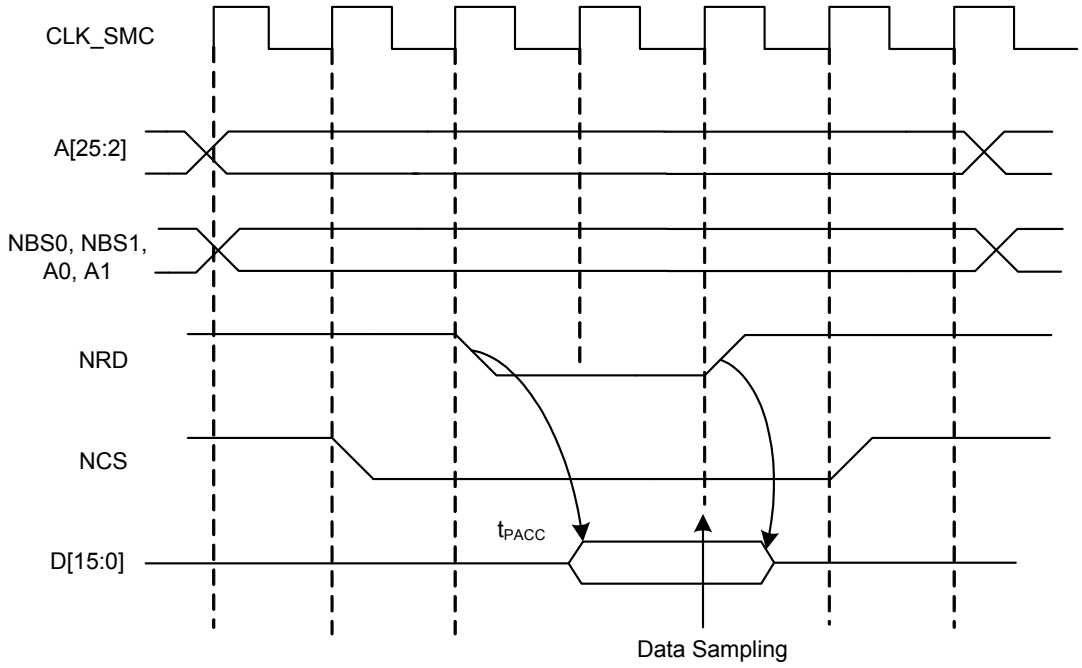
27.6.4.2 Read mode

As NCS and NRD waveforms are defined independently of one other, the SMC needs to know when the read data is available on the data bus. The SMC does not compare NCS and NRD timings to know which signal rises first. The Read Mode bit in the MODE register (MODE.READMODE) of the corresponding chip select indicates which signal of NRD and NCS controls the read operation.

•Read is controlled by NRD (MODE.READMODE = 1)

Figure 27-11 on page 502 shows the waveforms of a read operation of a typical asynchronous RAM. The read data is available t_{PACC} after the falling edge of NRD, and turns to 'Z' after the rising edge of NRD. In this case, the MODE.READMODE bit must be written to one (read is controlled by NRD), to indicate that data is available with the rising edge of NRD. The SMC samples the read data internally on the rising edge of CLK_SMC that generates the rising edge of NRD, whatever the programmed waveform of NCS may be.

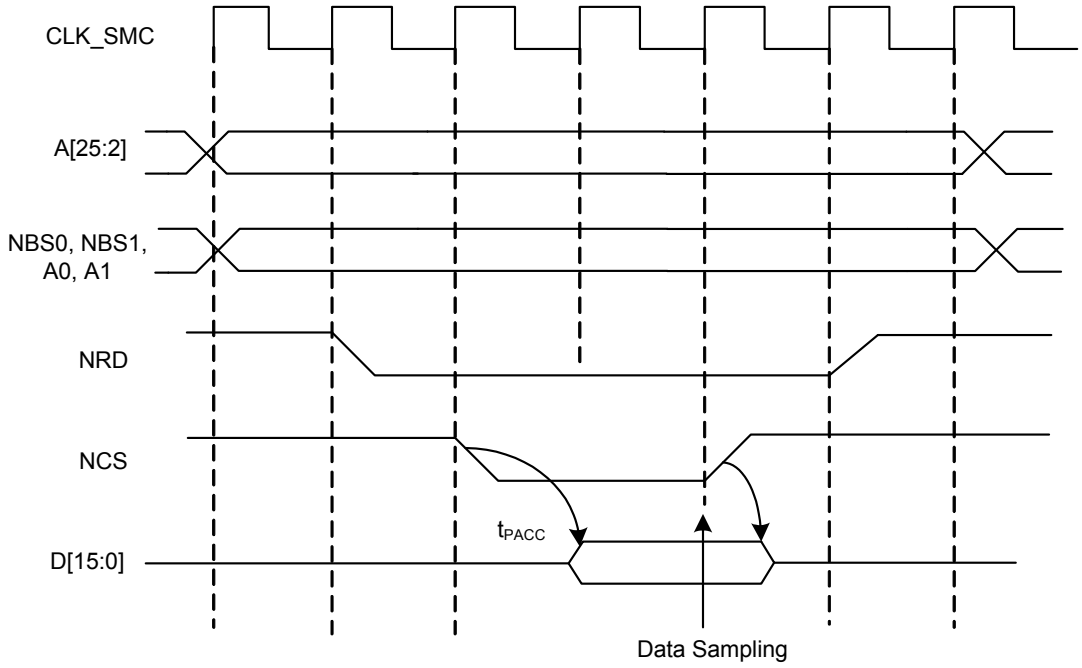
Figure 27-11. READMODE = 1: Data Is Sampled by SMC Before the Rising Edge of NRD



•Read is controlled by NCS (MODE.READMODE = 0)

Figure 27-12 on page 503 shows the typical read cycle of an LCD module. The read data is valid t_{PACC} after the falling edge of the NCS signal and remains valid until the rising edge of NCS. Data must be sampled when NCS is raised. In that case, the MODE.READMODE bit must be written to zero (read is controlled by NCS): the SMC internally samples the data on the rising edge of CML_SMC that generates the rising edge of NCS, whatever the programmed waveform of NRD may be.

Figure 27-12. READMODE = 0: Data Is Sampled by SMC Before the Rising Edge of NCS



27.6.4.3 *Write waveforms*

The write protocol is similar to the read protocol. It is depicted in Figure 27-13 on page 504. The write cycle starts with the address setting on the memory address bus.

•NWE waveforms

The NWE signal is characterized by a setup timing, a pulse width and a hold timing.

1. NWESETUP: the NWE setup time is defined as the setup of address and data before the NWE falling edge.
2. NWEPULSE: the NWE pulse length is the time between NWE falling edge and NWE rising edge.
3. NWEHOLD: the NWE hold time is defined as the hold time of address and data after the NWE rising edge.

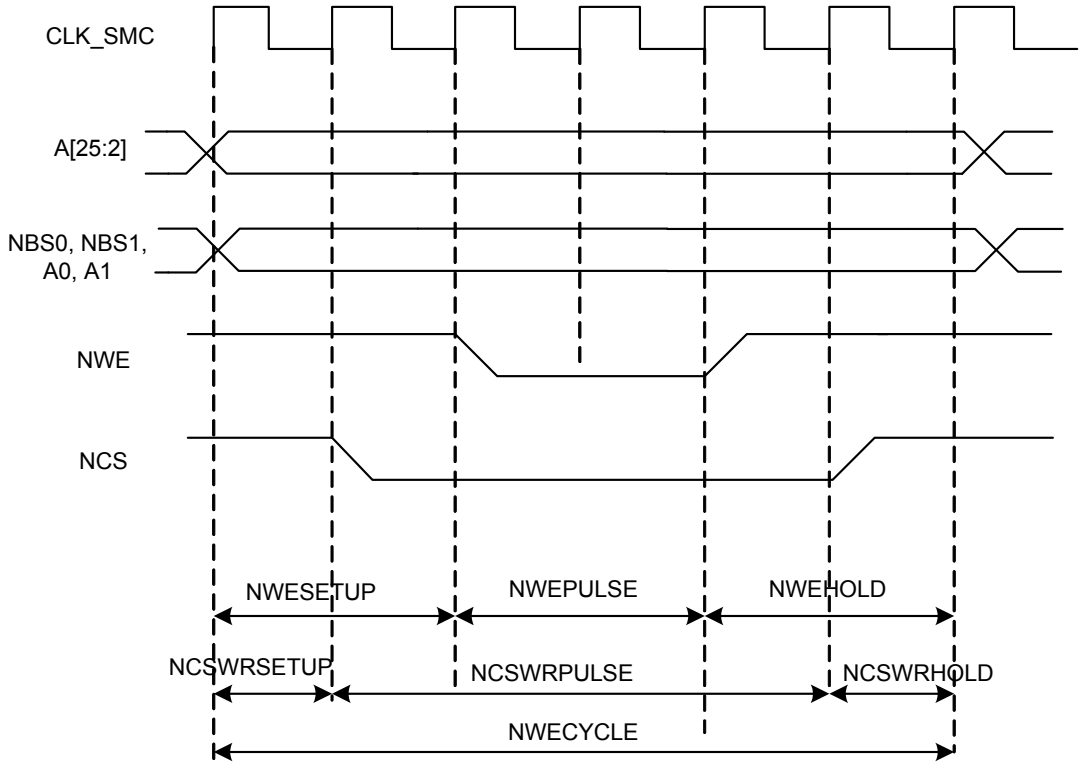
The NWE waveforms apply to all byte-write lines in byte write access mode: NWR0 to NWR3.

27.6.4.4 *NCS waveforms*

The NCS signal waveforms in write operation are not the same that those applied in read operations, but are separately defined.

1. NCSWRSETUP: the NCS setup time is defined as the setup time of address before the NCS falling edge.
2. NCSWRPULSE: the NCS pulse length is the time between NCS falling edge and NCS rising edge;
3. NCSWRHOLD: the NCS hold time is defined as the hold time of address after the NCS rising edge.

Figure 27-13. Write Cycle



•Write cycle

The write cycle time is defined as the total duration of the write cycle, that is, from the time where address is set on the address bus to the point where address may change. The total write cycle time is equal to:

$$NWECYCLE = NWESETUP + NWEPULSE + NWEHOLD$$

Similarly,

$$NWECYCLE = NCSWRSETUP + NCSWRPULSE + NCSWRHOLD$$

All NWE and NCS (write) timings are defined separately for each chip select as an integer number of CLK_SMC cycles. To ensure that the NWE and NCS timings are coherent, the user must define the total write cycle instead of the hold timing. This implicitly defines the NWE hold time and NCS (write) hold times as:

$$NWEHOLD = NWECYCLE - NWESETUP - NWEPULSE$$

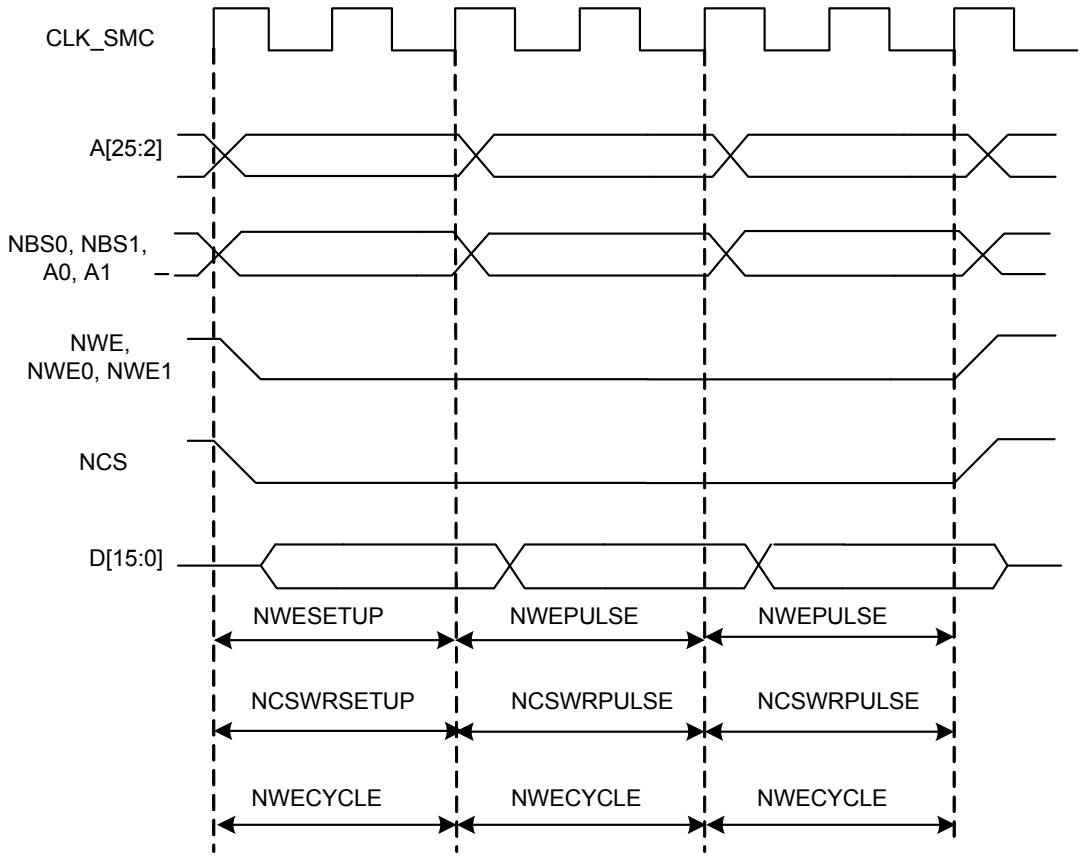
And,

$$NCSWRHOLD = NWECYCLE - NCSWRSETUP - NCSWRPULSE$$

•*Null delay setup and hold*

If null setup parameters are programmed for NWE and/or NCS, NWE and/or NCS remain active continuously in case of consecutive write cycles in the same memory (see Figure 27-14 on page 505). However, for devices that perform write operations on the rising edge of NWE or NCS, such as SRAM, either a setup or a hold must be programmed.

Figure 27-14. Null Setup and Hold Values of NCS and NWE in Write Cycle



•*Null pulse*

Programming null pulse is not permitted. Pulse must be at least written to one. A null value leads to unpredictable behavior.

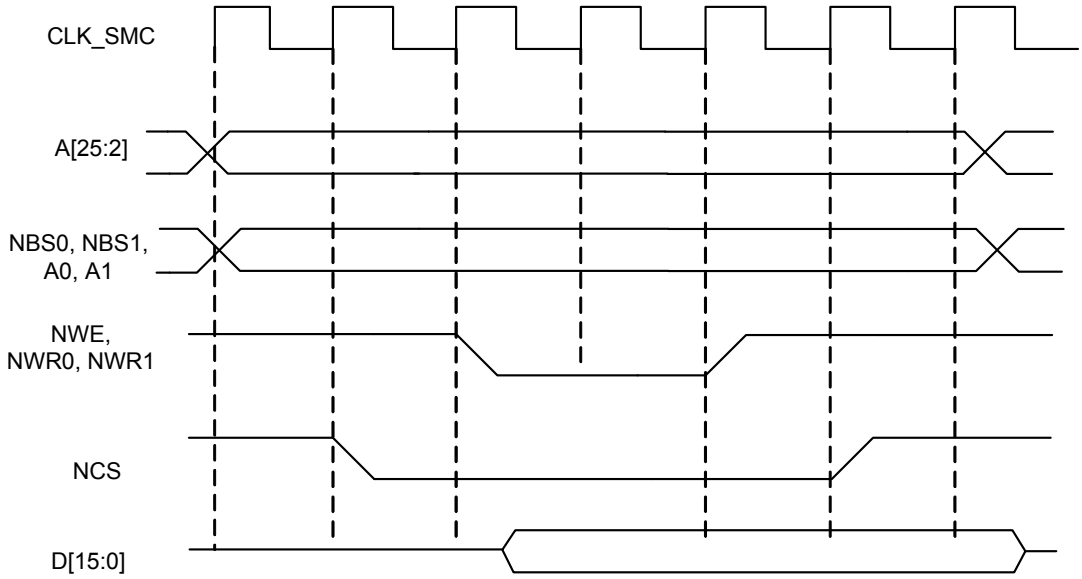
27.6.4.5 Write mode

The Write Mode bit in the MODE register (MODE.WRITEMODE) of the corresponding chip select indicates which signal controls the write operation.

•*Write is controlled by NWE (MODE.WRITEMODE = 1)*

Figure 27-15 on page 506 shows the waveforms of a write operation with MODE.WRITEMODE equal to one. The data is put on the bus during the pulse and hold steps of the NWE signal. The internal data buffers are turned out after the NWESETUP time, and until the end of the write cycle, regardless of the programmed waveform on NCS.

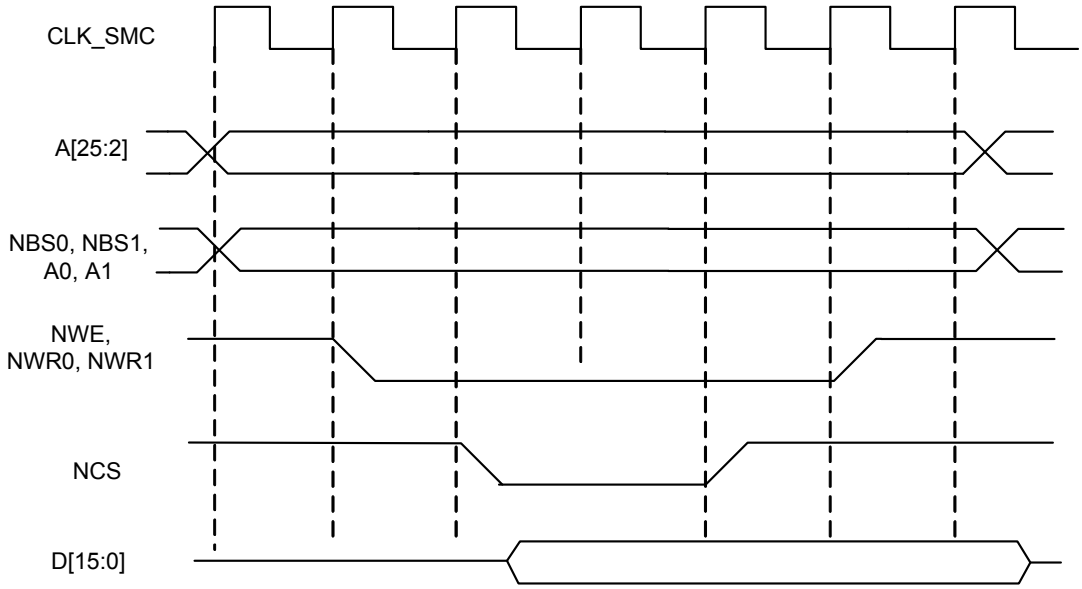
Figure 27-15. WRITEMODE = 1. The Write Operation Is Controlled by NWE



•Write is controlled by NCS (MODE.WRITEMODE = 0)

Figure 27-16 on page 506 shows the waveforms of a write operation with MODE.WRITEMODE written to zero. The data is put on the bus during the pulse and hold steps of the NCS signal. The internal data buffers are turned out after the NCSWRSETUP time, and until the end of the write cycle, regardless of the programmed waveform on NWE.

Figure 27-16. WRITEMODE = 0. The Write Operation Is Controlled by NCS



27.6.4.6 Coding timing parameters

All timing parameters are defined for one chip select and are grouped together in one register according to their type.

The Setup register (SETUP) groups the definition of all setup parameters:

- NRDSETUP, NCSRDSETUP, NWESETUP, and NCSWRSETUP.

The Pulse register (PULSE) groups the definition of all pulse parameters:

- NRDPULSE, NCSRDPULSE, NWEPULSE, and NCSWRPULSE.

The Cycle register (CYCLE) groups the definition of all cycle parameters:

- NRDCYCLE, NWECYCLE.

Table 27-3 on page 507 shows how the timing parameters are coded and their permitted range.

Table 27-3. Coding and Range of Timing Parameters

Coded Value	Number of Bits	Effective Value	Permitted Range	
			Coded Value	Effective Value
setup [5:0]	6	128 x setup[5] + setup[4:0]	0 ≤ value ≤ 31	128 ≤ value ≤ 128+31
pulse [6:0]	7	256 x pulse[6] + pulse[5:0]	0 ≤ value ≤ 63	256 ≤ value ≤ 256+63
cycle [8:0]	9	256 x cycle[8:7] + cycle[6:0]	0 ≤ value ≤ 127	256 ≤ value ≤ 256+127 512 ≤ value ≤ 512+127 768 ≤ value ≤ 768+127

27.6.4.7 Usage restriction

The SMC does not check the validity of the user-programmed parameters. If the sum of SETUP and PULSE parameters is larger than the corresponding CYCLE parameter, this leads to unpredictable behavior of the SMC.

For read operations:

Null but positive setup and hold of address and NRD and/or NCS can not be guaranteed at the memory interface because of the propagation delay of theses signals through external logic and pads. If positive setup and hold values must be verified, then it is strictly recommended to program non-null values so as to cover possible skews between address, NCS and NRD signals.

For write operations:

If a null hold value is programmed on NWE, the SMC can guarantee a positive hold of address, byte select lines, and NCS signal after the rising edge of NWE. This is true if the MODE.WRITEMODE bit is written to one. See Section 27.6.5.2.

For read and write operations: a null value for pulse parameters is forbidden and may lead to unpredictable behavior.

In read and write cycles, the setup and hold time parameters are defined in reference to the address bus. For external devices that require setup and hold time between NCS and NRD signals (read), or between NCS and NWE signals (write), these setup and hold times must be converted into setup and hold times in reference to the address bus.

27.6.5 Automatic Wait States

Under certain circumstances, the SMC automatically inserts idle cycles between accesses to avoid bus contention or operation conflict.

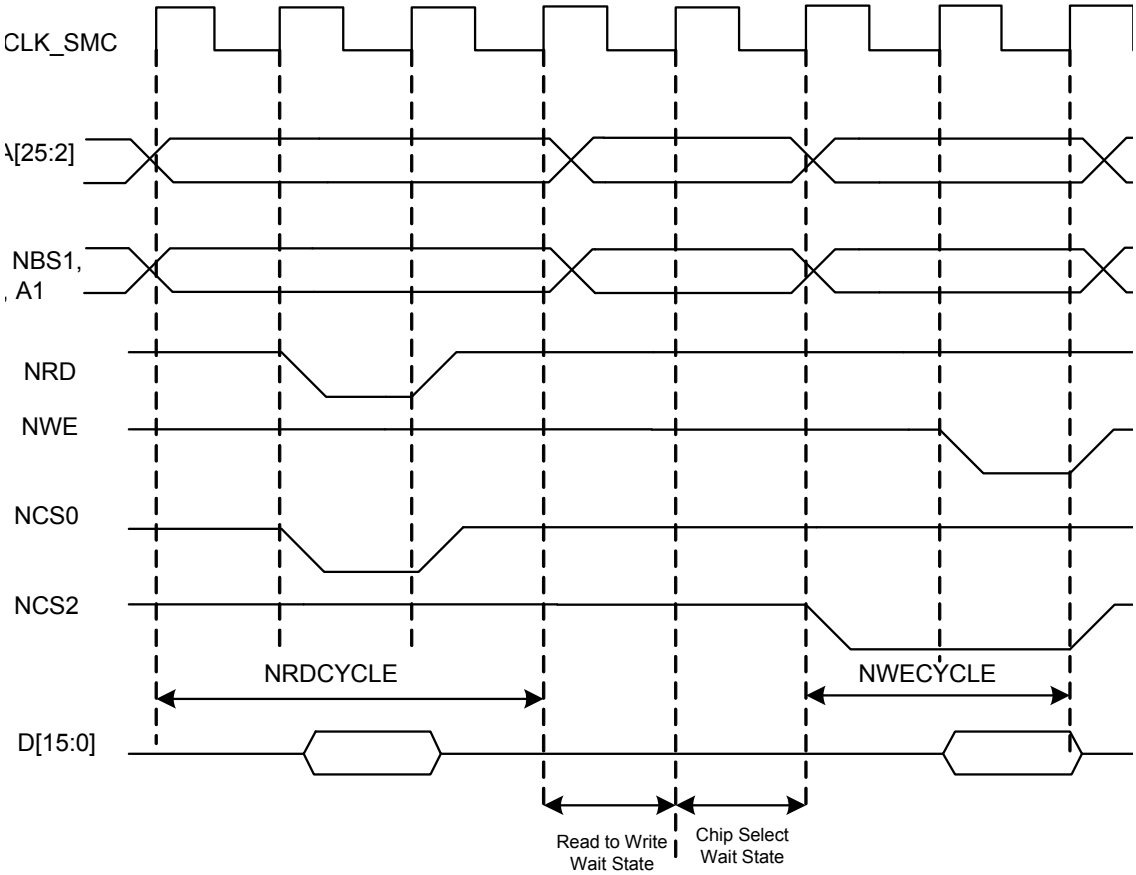
27.6.5.1 Chip select wait states

The SMC always inserts an idle cycle between two transfers on separate chip selects. This idle cycle ensures that there is no bus contention between the deactivation of one device and the activation of the next one.

During chip select wait state, all control lines are turned inactive: NBS0 to NBS3, NWR0 to NWR3, NCS[0..5], NRD lines are all set to high level.

Figure 27-17 on page 508 illustrates a chip select wait state between access on Chip Select 0 (NCS0) and Chip Select 2 (NCS2).

Figure 27-17. Chip Select Wait State Between a Read Access on NCS0 and a Write Access on NCS2



27.6.5.2 Early read wait state

In some cases, the SMC inserts a wait state cycle between a write access and a read access to allow time for the write cycle to end before the subsequent read cycle begins. This wait state is not generated in addition to a chip select wait state. The early read cycle thus only occurs between a write and read access to the same memory device (same chip select).

An early read wait state is automatically inserted if at least one of the following conditions is valid:

- if the write controlling signal has no hold time and the read controlling signal has no setup time (Figure 27-18 on page 509).
- in NCS write controlled mode (MODE.WRITEMODE = 0), if there is no hold timing on the NCS signal and the NCSRDSETUP parameter is set to zero, regardless of the read mode (Figure 27-19 on page 510). The write operation must end with a NCS rising edge. Without an early read wait state, the write operation could not complete properly.
- in NWE controlled mode (MODE.WRITEMODE = 1) and if there is no hold timing (NWEHOLD = 0), the feedback of the write control signal is used to control address, data, chip select, and byte select lines. If the external write control signal is not inactivated as expected due to load capacitances, an early read wait state is inserted and address, data and control signals are maintained one more cycle. See Figure 27-20 on page 511.

Figure 27-18. Early Read Wait State: Write with No Hold Followed by Read with No Setup.

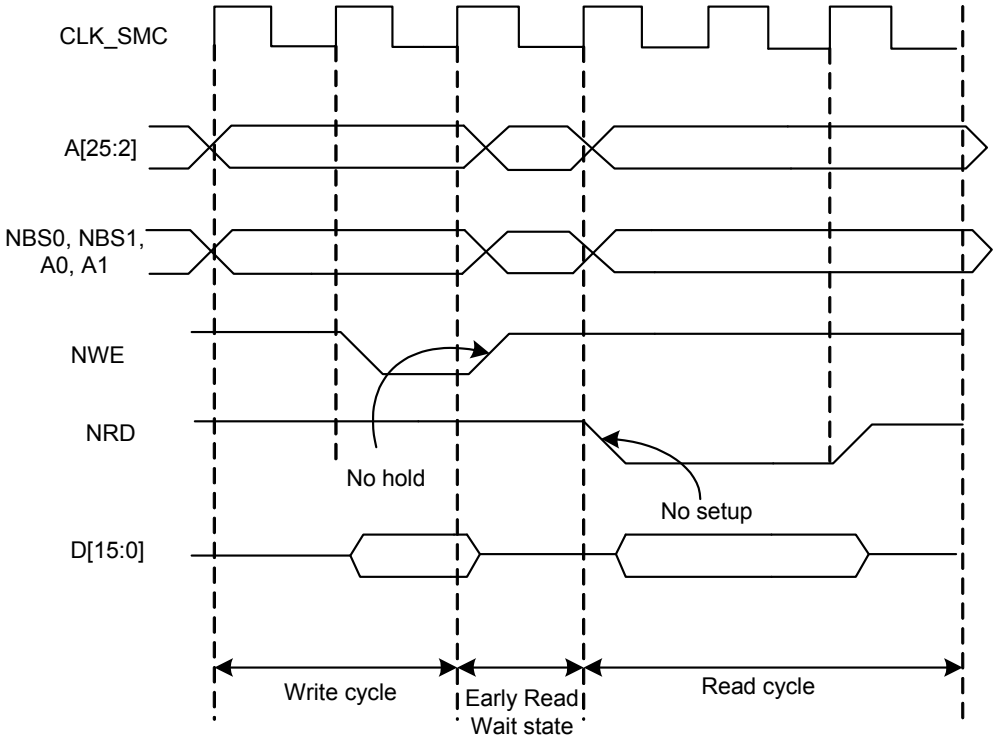


Figure 27-19. Early Read Wait State: NCS Controlled Write with No Hold Followed by a Read with No Setup.

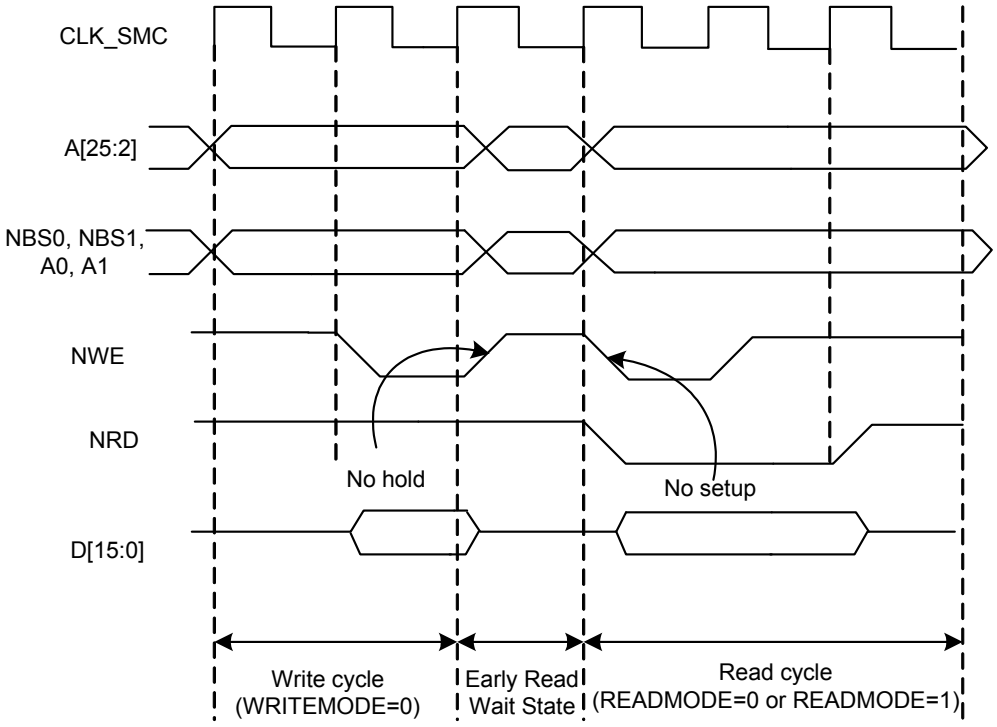
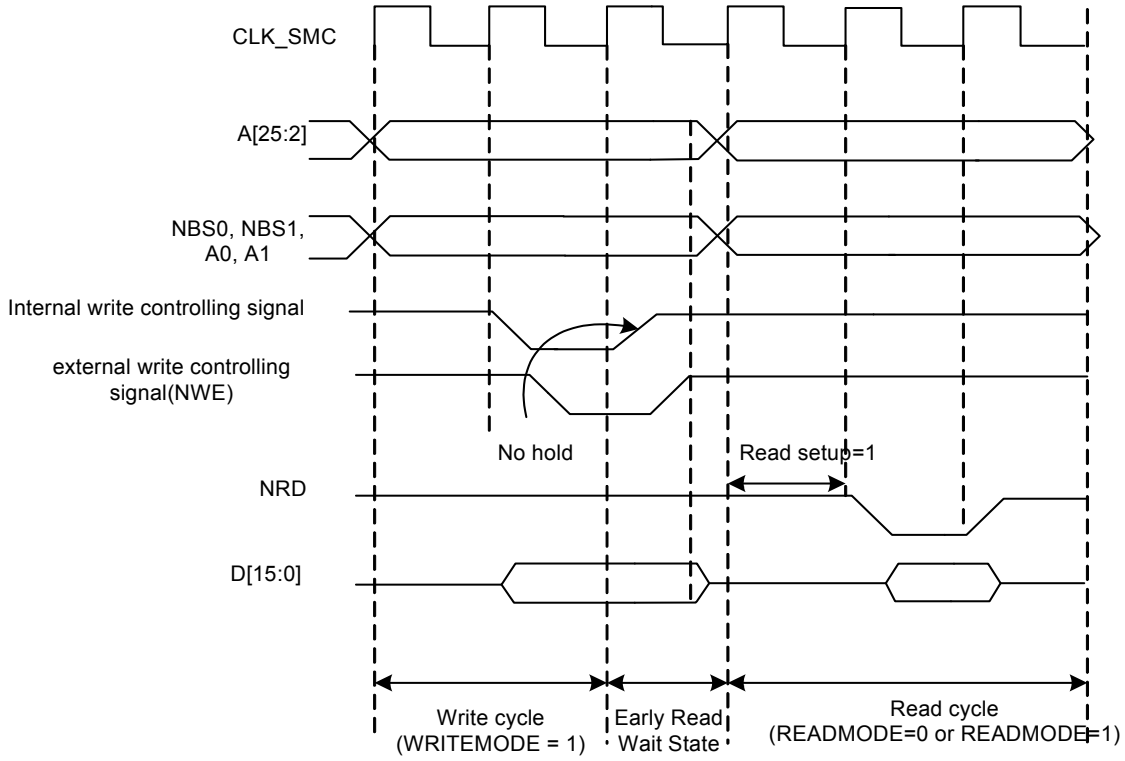


Figure 27-20. Early Read Wait State: NWE-controlled Write with No Hold Followed by a Read with one Set-up Cycle.



27.6.5.3 Reload user configuration wait state

The user may change any of the configuration parameters by writing the SMC user interface.

When detecting that a new user configuration has been written in the user interface, the SMC inserts a wait state before starting the next access. The so called “reload user configuration wait state” is used by the SMC to load the new set of parameters to apply to next accesses.

The reload configuration wait state is not applied in addition to the chip select wait state. If accesses before and after reprogramming the user interface are made to different devices (different chip selects), then one single chip select wait state is applied.

On the other hand, if accesses before and after writing the user interface are made to the same device, a reload configuration wait state is inserted, even if the change does not concern the current chip select.

•User procedure

To insert a reload configuration wait state, the SMC detects a write access to any MODE register of the user interface. If the user only modifies timing registers (SETUP, PULSE, CYCLE registers) in the user interface, he must validate the modification by writing the MODE register, even if no change was made on the mode parameters.

•*Slow clock mode transition*

A reload configuration wait state is also inserted when the slow clock mode is entered or exited, after the end of the current transfer (see Section 27.6.8).

27.6.5.4 Read to write wait state

Due to an internal mechanism, a wait cycle is always inserted between consecutive read and write SMC accesses.

This wait cycle is referred to as a read to write wait state in this document.

This wait cycle is applied in addition to chip select and reload user configuration wait states when they are to be inserted. See Figure 27-17 on page 508.

27.6.6 Data Float Wait States

Some memory devices are slow to release the external bus. For such devices, it is necessary to add wait states (data float wait states) after a read access:

- before starting a read access to a different external memory.
- before starting a write access to the same device or to a different external one.

The Data Float Output Time (t_{DF}) for each external memory device is programmed in the Data Float Time field of the MODE register (MODE.TDFCYCLES) for the corresponding chip select. The value of MODE.TDFCYCLES indicates the number of data float wait cycles (between 0 and 15) before the external device releases the bus, and represents the time allowed for the data output to go to high impedance after the memory is disabled.

Data float wait states do not delay internal memory accesses. Hence, a single access to an external memory with long t_{DF} will not slow down the execution of a program from internal memory.

The data float wait states management depends on the MODE.READMODE bit and the TDF Optimization bit of the MODE register (MODE.TDFMODE) for the corresponding chip select.

27.6.6.1 Read mode

Writing a one to the MODE.READMODE bit indicates to the SMC that the NRD signal is responsible for turning off the tri-state buffers of the external memory device. The data float period then begins after the rising edge of the NRD signal and lasts MODE.TDFCYCLES cycles of the CLK_SMC clock.

When the read operation is controlled by the NCS signal (MODE.READMODE = 0), the MODE.TDFCYCLES field gives the number of CLK_SMC cycles during which the data bus remains busy after the rising edge of NCS.

Figure 27-21 on page 513 illustrates the data float period in NRD-controlled mode (MODE.READMODE =1), assuming a data float period of two cycles (MODE.TDFCYCLES = 2). Figure 27-22 on page 513 shows the read operation when controlled by NCS (MODE.READMODE = 0) and the MODE.TDFCYCLES field equals to three.

Figure 27-21. TDF Period in NRD Controlled Read Access (TDFCYCLES = 2)

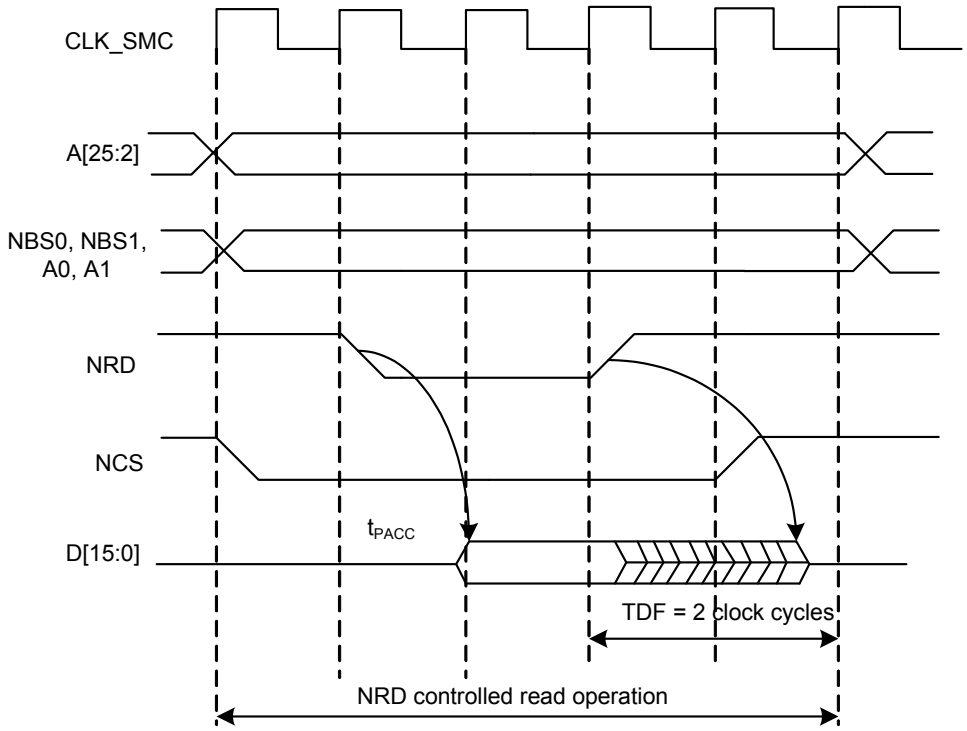
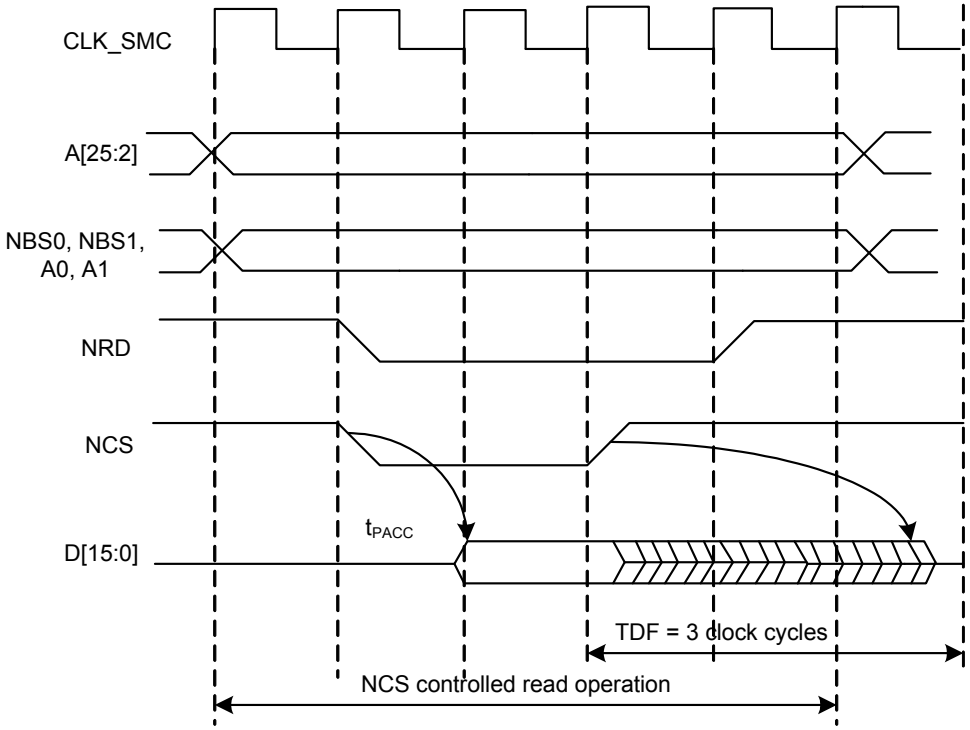


Figure 27-22. TDF Period in NCS Controlled Read Operation (TDFCYCLES = 3)



27.6.6.2 TDF optimization enabled (MODE.TDFMODE = 1)

When the MODE.TDFMODE bit is written to one (TDF optimization is enabled), the SMC takes advantage of the setup period of the next access to optimize the number of wait states cycle to insert.

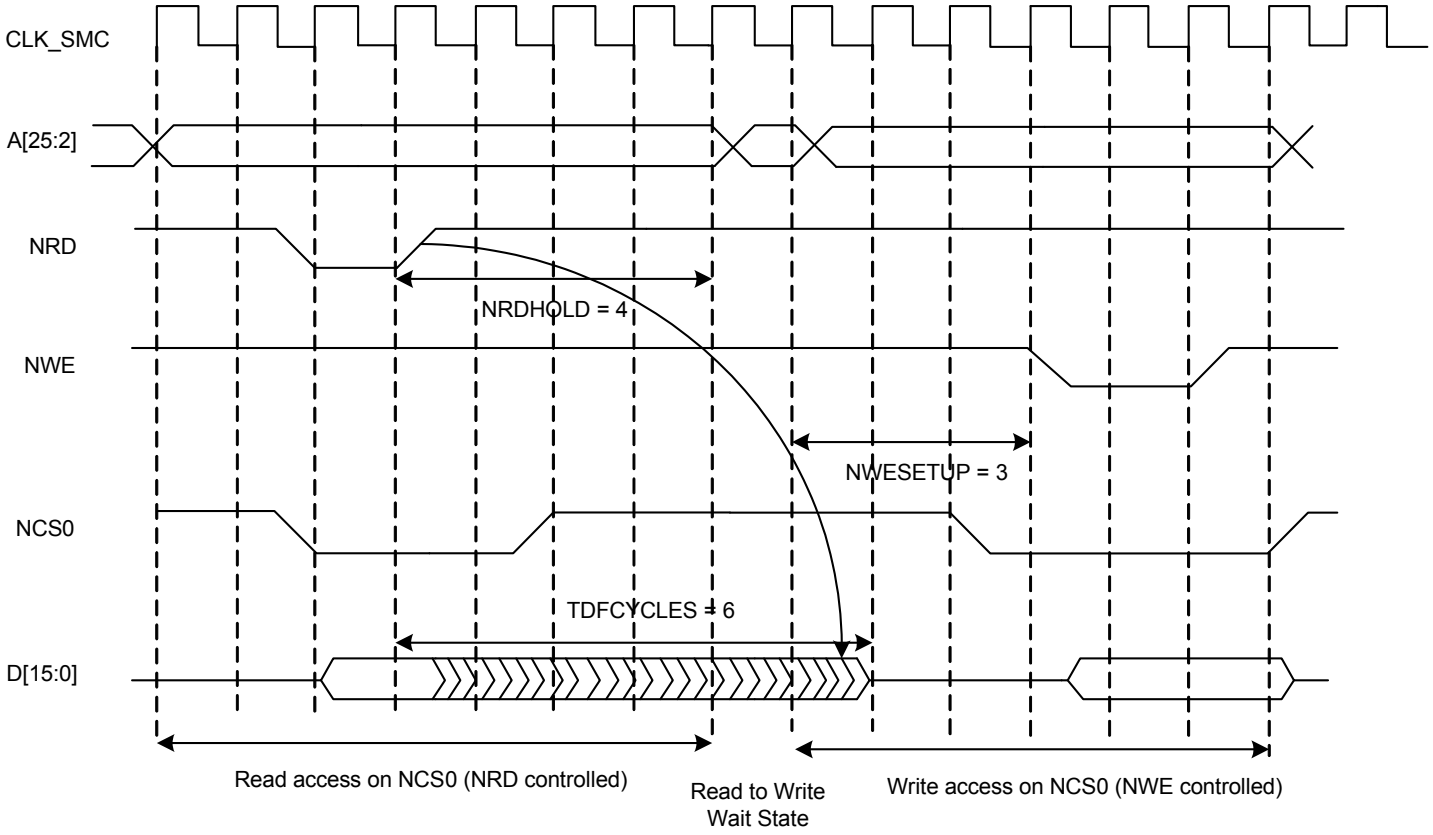
Figure 27-23 on page 514 shows a read access controlled by NRD, followed by a write access controlled by NWE, on Chip Select 0. Chip Select 0 has been programmed with:

NRDHOLD = 4; READMODE = 1 (NRD controlled)

NWESETUP = 3; WRITEMODE = 1 (NWE controlled)

TDFCYCLES = 6; TDFMODE = 1 (optimization enabled).

Figure 27-23. TDF Optimization: No TDF Wait States Are Inserted if the TDF Period Is over when the Next Access Begins



27.6.6.3 TDF optimization disabled (MODE.TDFMODE = 0)

When optimization is disabled, data float wait states are inserted at the end of the read transfer, so that the data float period is ended when the second access begins. If the hold period of the read1 controlling signal overlaps the data float period, no additional data float wait states will be inserted.

Figure 27-24 on page 515, Figure 27-25 on page 515 and Figure 27-26 on page 516 illustrate the cases:

- read access followed by a read access on another chip select.

- read access followed by a write access on another chip select.
- read access followed by a write access on the same chip select.

with no TDF optimization.

Figure 27-24. TDF Optimization Disabled (MODE.TDFMODE = 0). TDF Wait States between Two Read Accesses on Different Chip Selects.

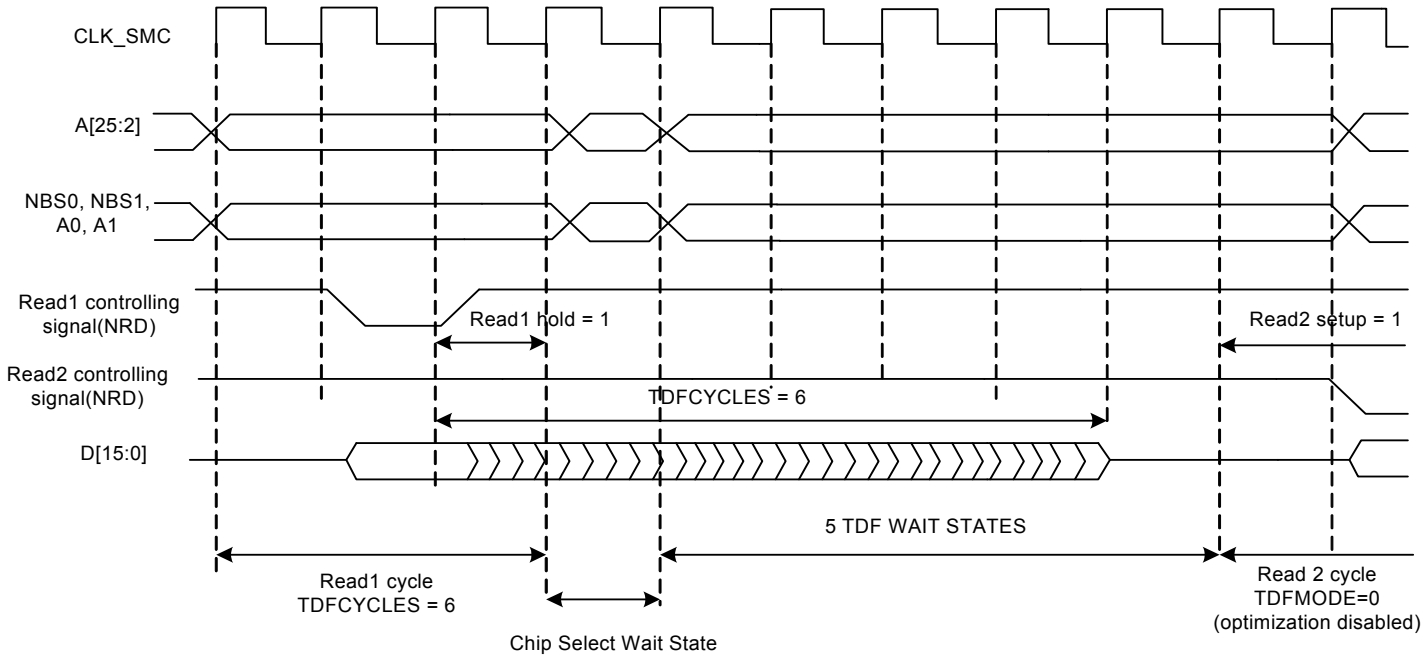


Figure 27-25. TDF Optimization Disabled (MODE.TDFMODE= 0). TDF Wait States between a Read and a Write Access on Different Chip Selects.

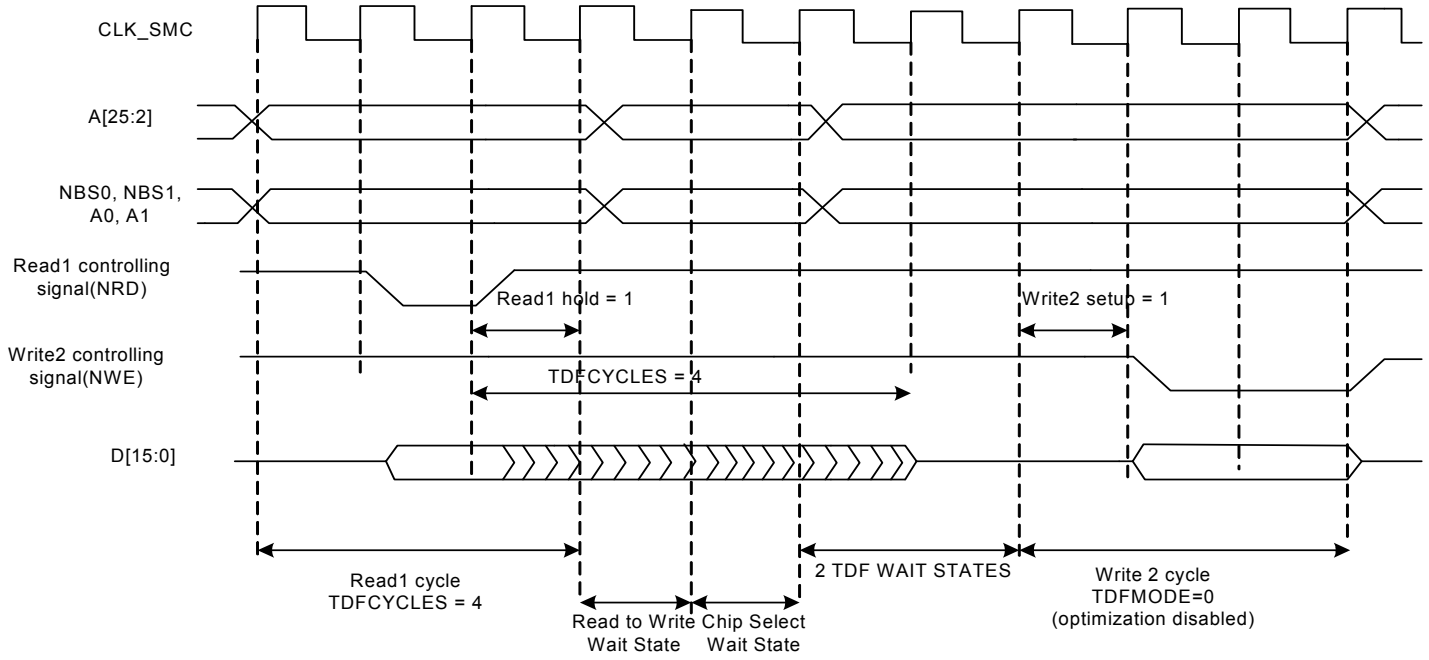
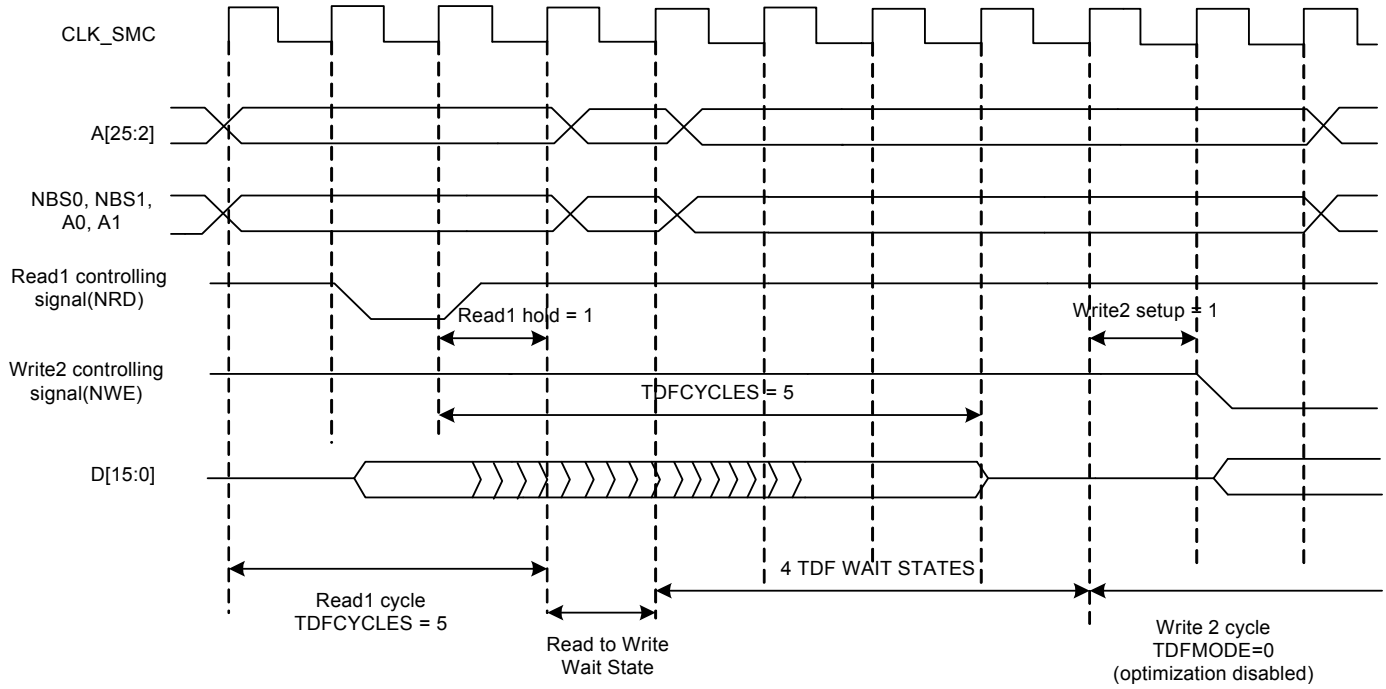


Figure 27-26. TDF Optimization Disabled (MODE.TDFMODE = 0). TDF Wait States between Read and Write accesses on the Same Chip Select.



27.6.7 External Wait

Any access can be extended by an external device using the NWAIT input signal of the SMC. The External Wait Mode field of the MODE register (MODE.EXNWMODE) on the corresponding chip select must be written to either two (frozen mode) or three (ready mode). When the MODE.EXNWMODE field is written to zero (disabled), the NWAIT signal is simply ignored on the corresponding chip select. The NWAIT signal delays the read or write operation in regards to the read or write controlling signal, depending on the read and write modes of the corresponding chip select.

27.6.7.1 Restriction

When one of the MODE.EXNWMODE is enabled, it is mandatory to program at least one hold cycle for the read/write controlling signal. For that reason, the NWAIT signal cannot be used in Page Mode (Section 27.6.9), or in Slow Clock Mode (Section 27.6.8).

The NWAIT signal is assumed to be a response of the external device to the read/write request of the SMC. Then NWAIT is examined by the SMC only in the pulse state of the read or write controlling signal. The assertion of the NWAIT signal outside the expected period has no impact on SMC behavior.

27.6.7.2 Frozen mode

When the external device asserts the NWAIT signal (active low), and after internal synchronization of this signal, the SMC state is frozen, i.e., SMC internal counters are frozen, and all control signals remain unchanged. When the synchronized NWAIT signal is deasserted, the SMC completes the access, resuming the access from the point where it was stopped. See Figure 27-27 on page 517. This mode must be selected when the external device uses the NWAIT signal to delay the access and to freeze the SMC.

The assertion of the NWAIT signal outside the expected period is ignored as illustrated in Figure 27-28 on page 518.

Figure 27-27. Write Access with NWAIT Assertion in Frozen Mode (MODE.EXNWMODE = 2).

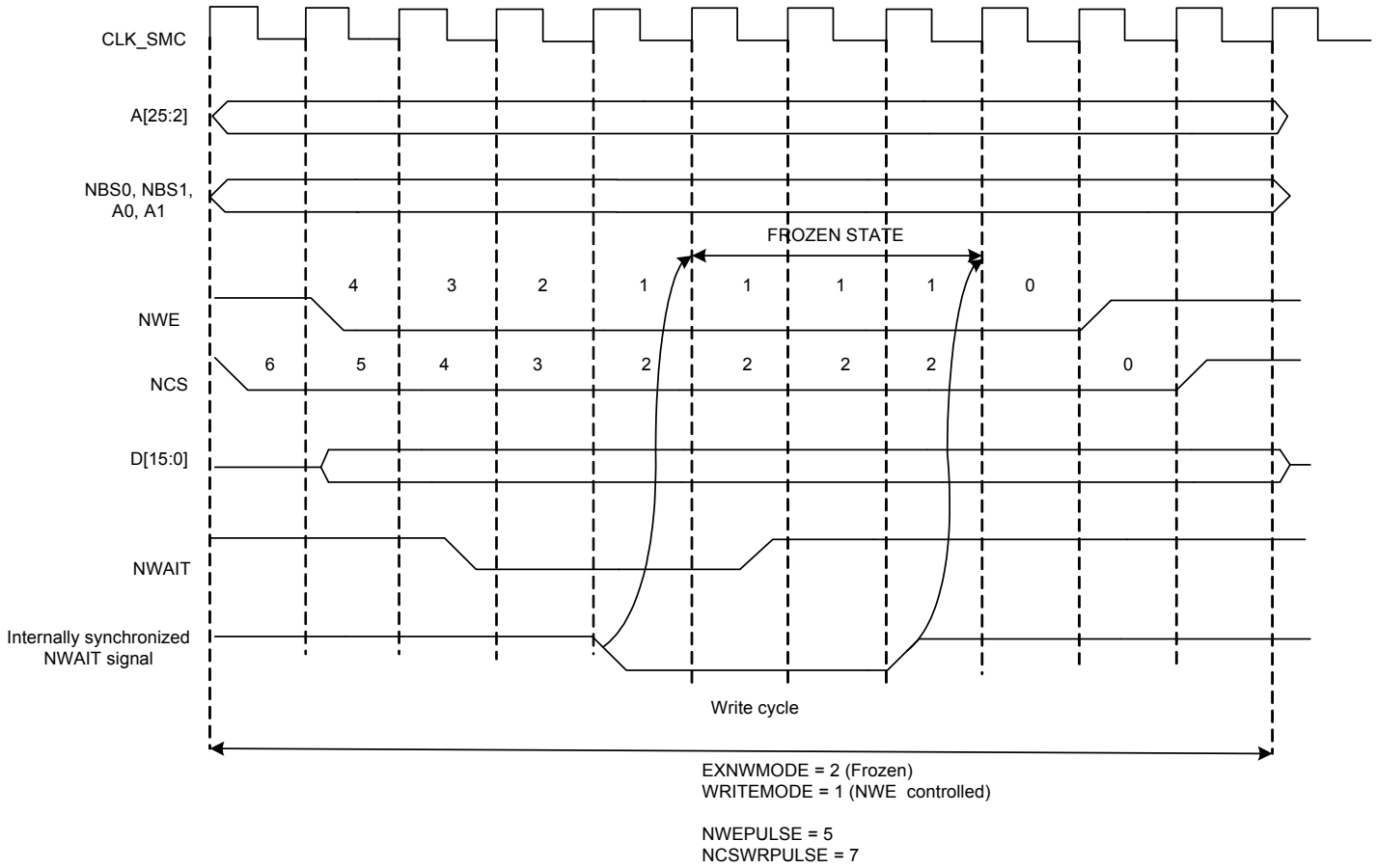
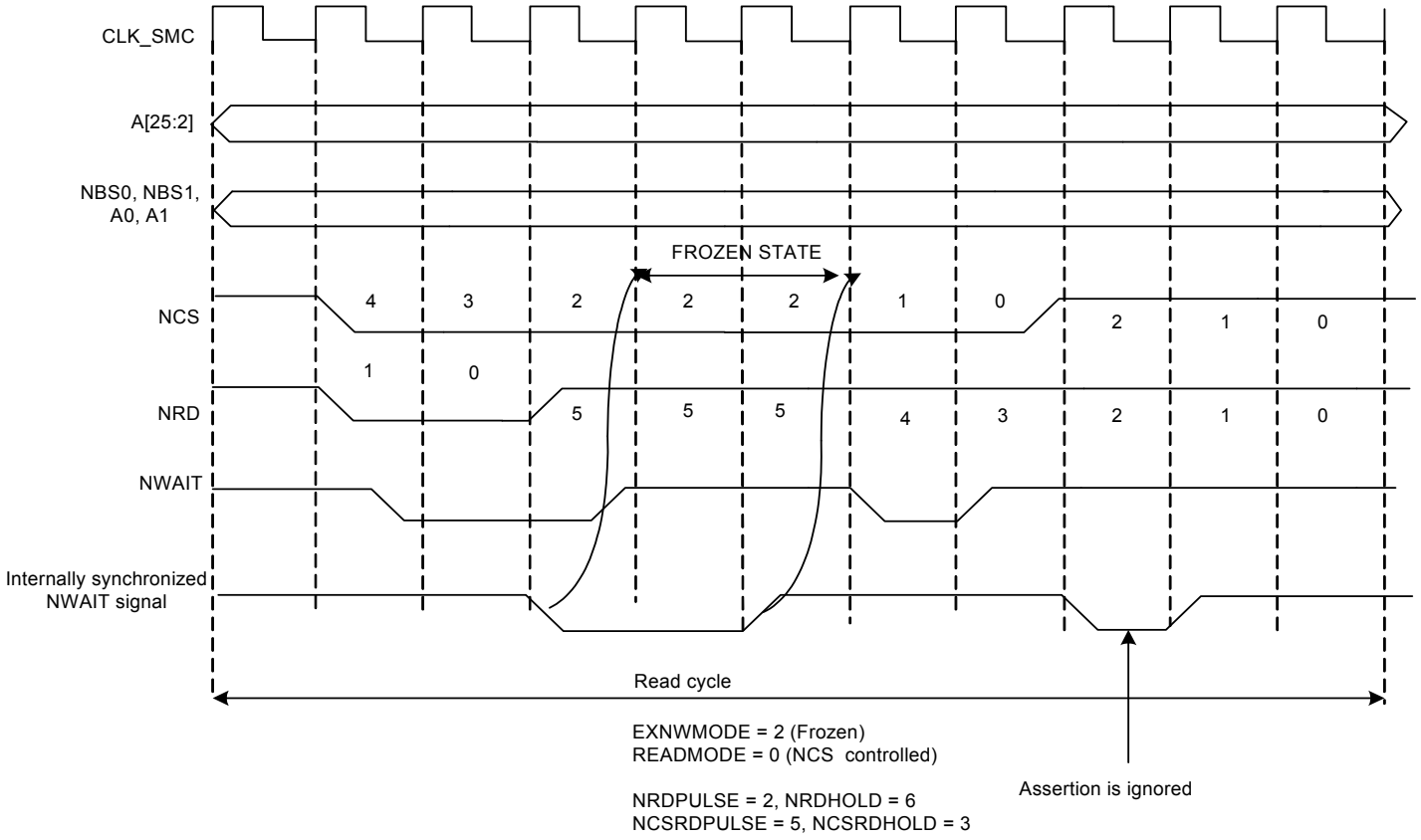


Figure 27-28. Read Access with NWAIT Assertion in Frozen Mode (MODE.EXNWMODE = 2).



27.6.7.3 Ready mode

In Ready mode (MODE.EXNWMODE = 3), the SMC behaves differently. Normally, the SMC begins the access by down counting the setup and pulse counters of the read/write controlling signal. In the last cycle of the pulse phase, the resynchronized NWAIT signal is examined.

If asserted, the SMC suspends the access as shown in Figure 27-29 on page 519 and Figure 27-30 on page 520. After deassertion, the access is completed: the hold step of the access is performed.

This mode must be selected when the external device uses deassertion of the NWAIT signal to indicate its ability to complete the read or write operation.

If the NWAIT signal is deasserted before the end of the pulse, or asserted after the end of the pulse of the controlling read/write signal, it has no impact on the access length as shown in Figure 27-30 on page 520.

Figure 27-29. NWAIT Assertion in Write Access: Ready Mode (MODE.EXNWMODE = 3).

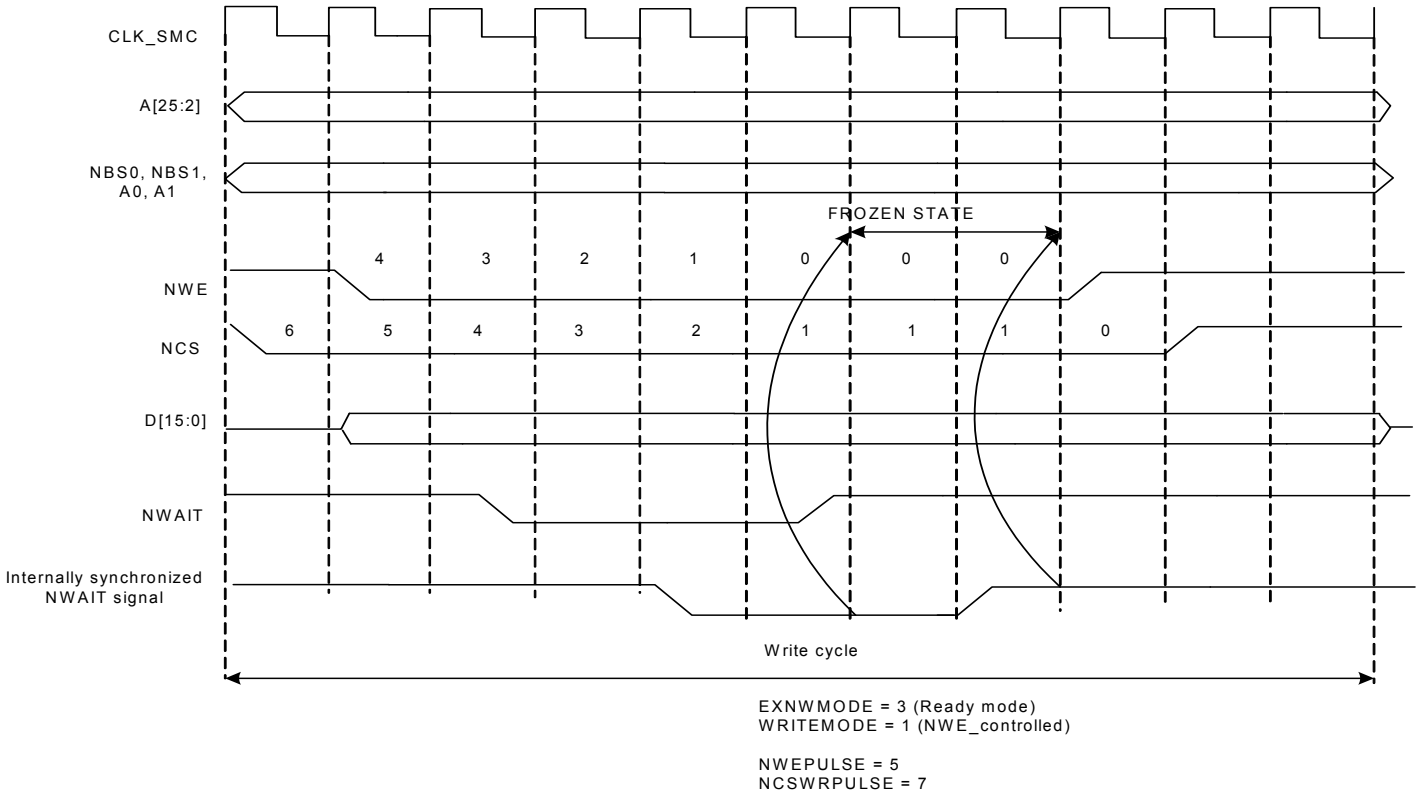
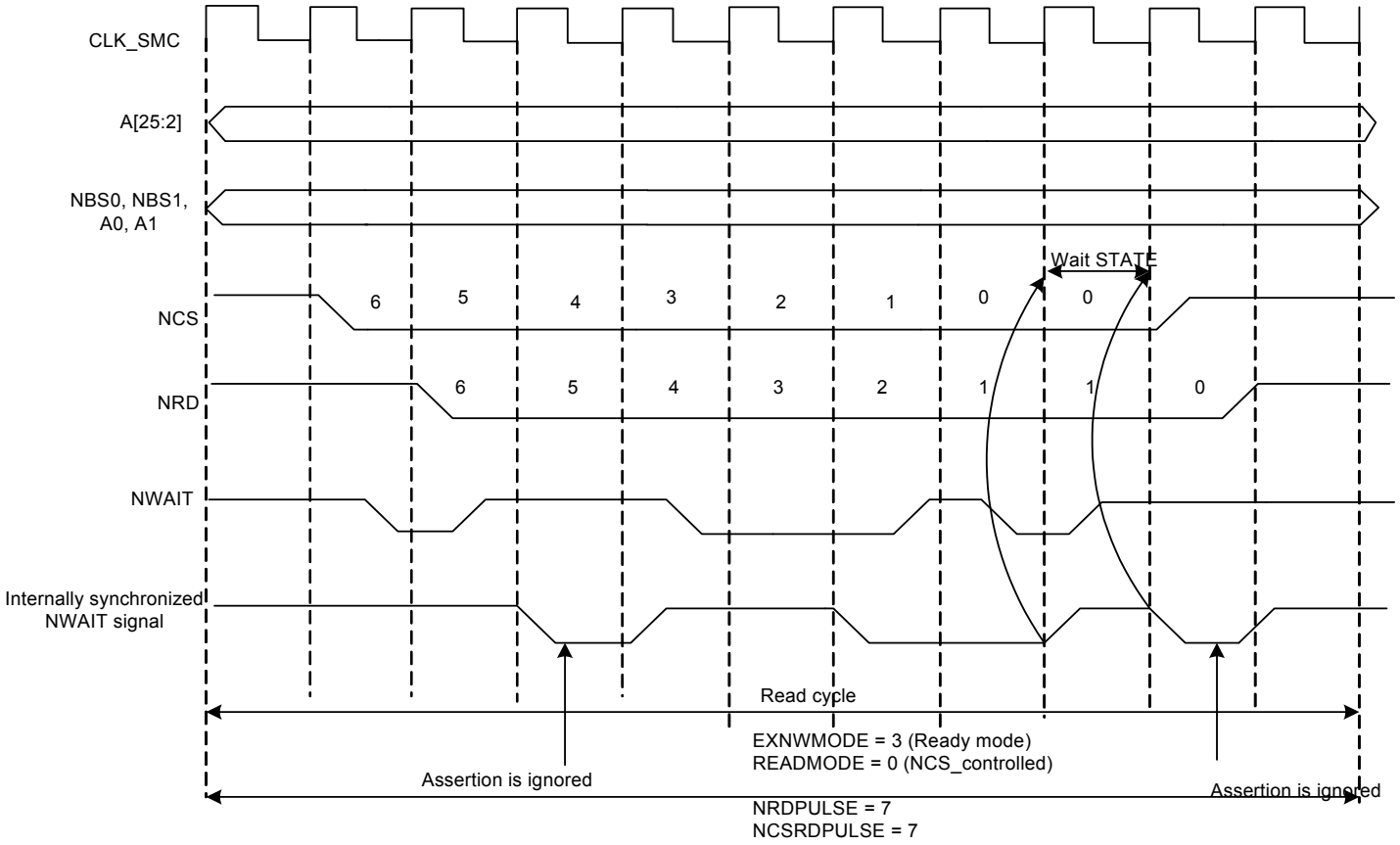


Figure 27-30. NWAIT Assertion in Read Access: Ready Mode (EXNWMODE = 3).



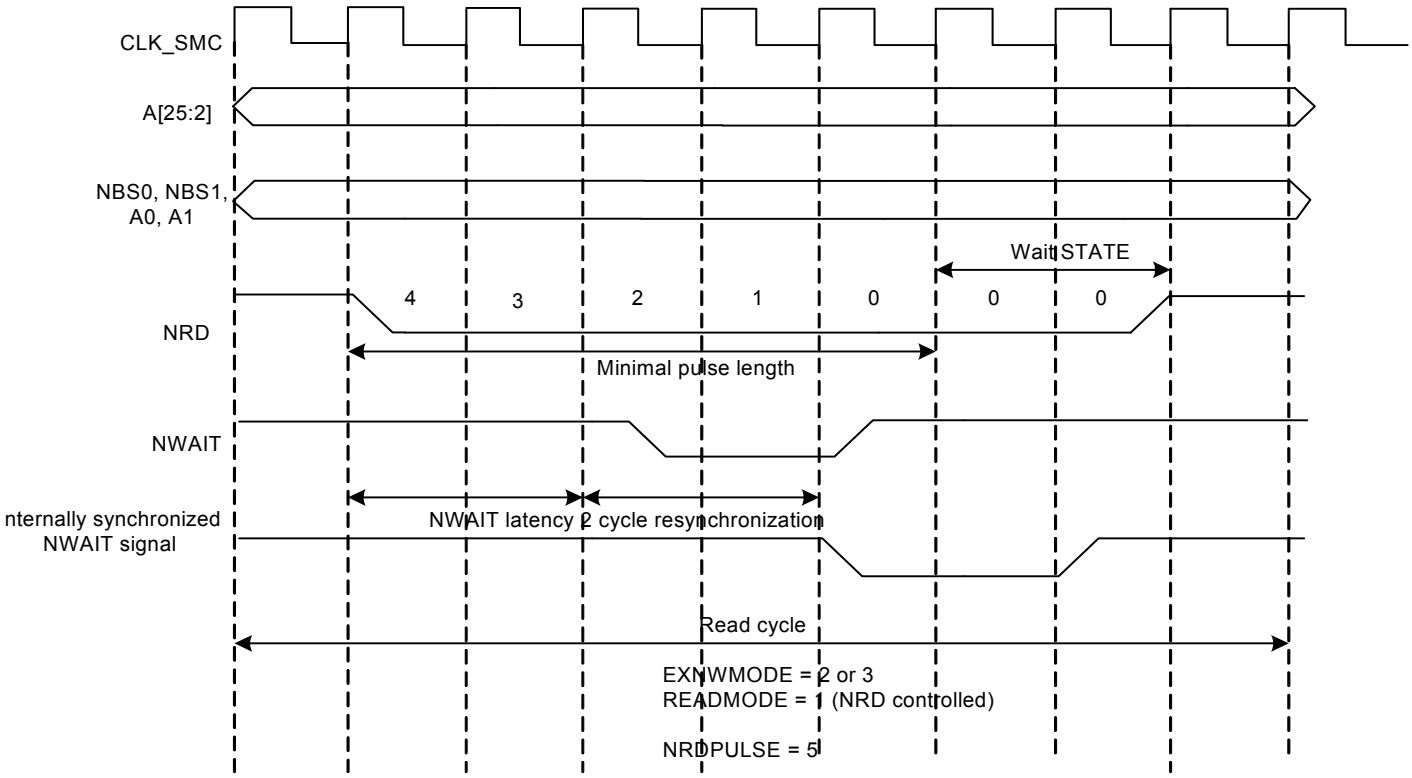
27.6.7.4 NWAIT latency and read/write timings

There may be a latency between the assertion of the read/write controlling signal and the assertion of the NWAIT signal by the device. The programmed pulse length of the read/write controlling signal must be at least equal to this latency plus the two cycles of resynchronization plus one cycle. Otherwise, the SMC may enter the hold state of the access without detecting the NWAIT signal assertion. This is true in frozen mode as well as in ready mode. This is illustrated on Figure 27-31 on page 521.

When the MODE.EXNWMODE field is enabled (ready or frozen), the user must program a pulse length of the read and write controlling signal of at least:

$$\text{minimal pulse length} = \text{NWAIT latency} + 2 \text{ synchronization cycles} + 1 \text{ cycle}$$

Figure 27-31. NWAIT Latency



27.6.8 Slow Clock Mode

The SMC is able to automatically apply a set of “slow clock mode” read/write waveforms when an internal signal driven by the SMC’s Power Management Controller is asserted because CLK_SMC has been turned to a very slow clock rate (typically 32 kHz clock rate). In this mode, the user-programmed waveforms are ignored and the slow clock mode waveforms are applied. This mode is provided so as to avoid reprogramming the User Interface with appropriate waveforms at very slow clock rate. When activated, the slow mode is active on all chip selects.

27.6.8.1 Slow clock mode waveforms

Figure 27-32 on page 522 illustrates the read and write operations in slow clock mode. They are valid on all chip selects. Table 27-4 on page 522 indicates the value of read and write parameters in slow clock mode.

Figure 27-32. Read and Write Cycles in Slow Clock Mode

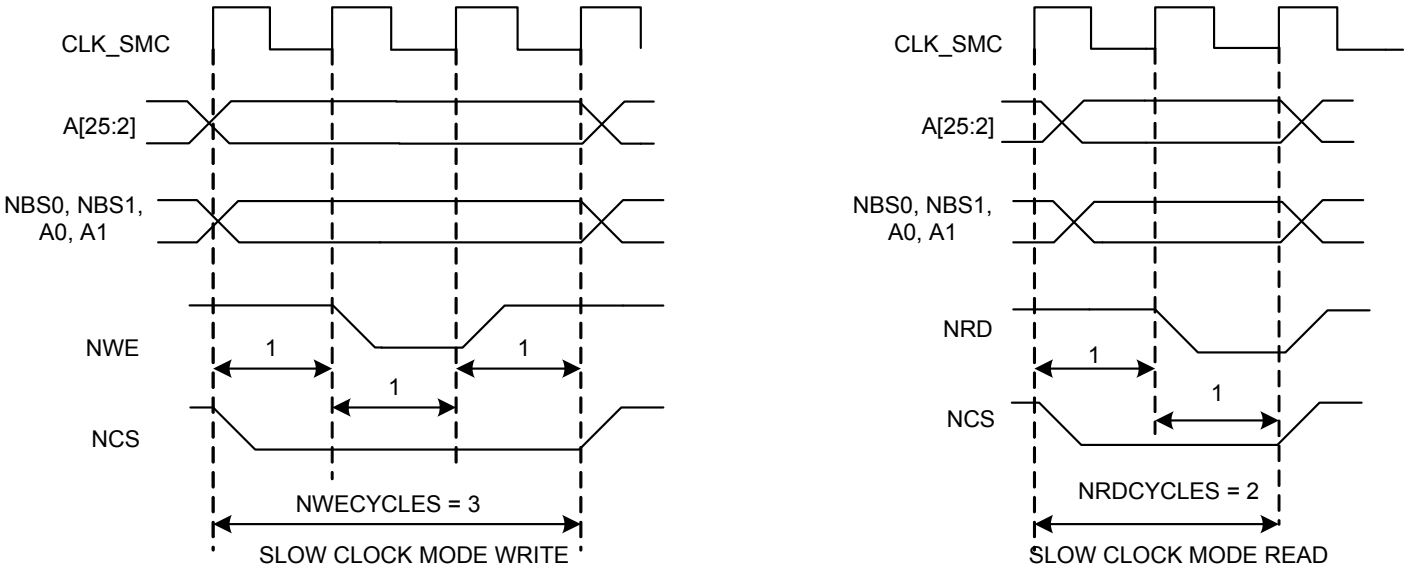


Table 27-4. Read and Write Timing Parameters in Slow Clock Mode

Read Parameters	Duration (cycles)	Write Parameters	Duration (cycles)
NRDSETUP	1	NWESETUP	1
NRDPULSE	1	NWEPULSE	1
NCSRDSETUP	0	NCSWRSETUP	0
NCSRDPULSE	2	NCSWRPULSE	3
NRDCYCLE	2	NWECYCLE	3

27.6.8.2 *Switching from (to) slow clock mode to (from) normal mode*

When switching from slow clock mode to the normal mode, the current slow clock mode transfer is completed at high clock rate, with the set of slow clock mode parameters. See Figure 27-33 on page 523. The external device may not be fast enough to support such timings.

Figure 27-34 on page 524 illustrates the recommended procedure to properly switch from one mode to the other.

Figure 27-33. Clock Rate Transition Occurs while the SMC is Performing a Write Operation

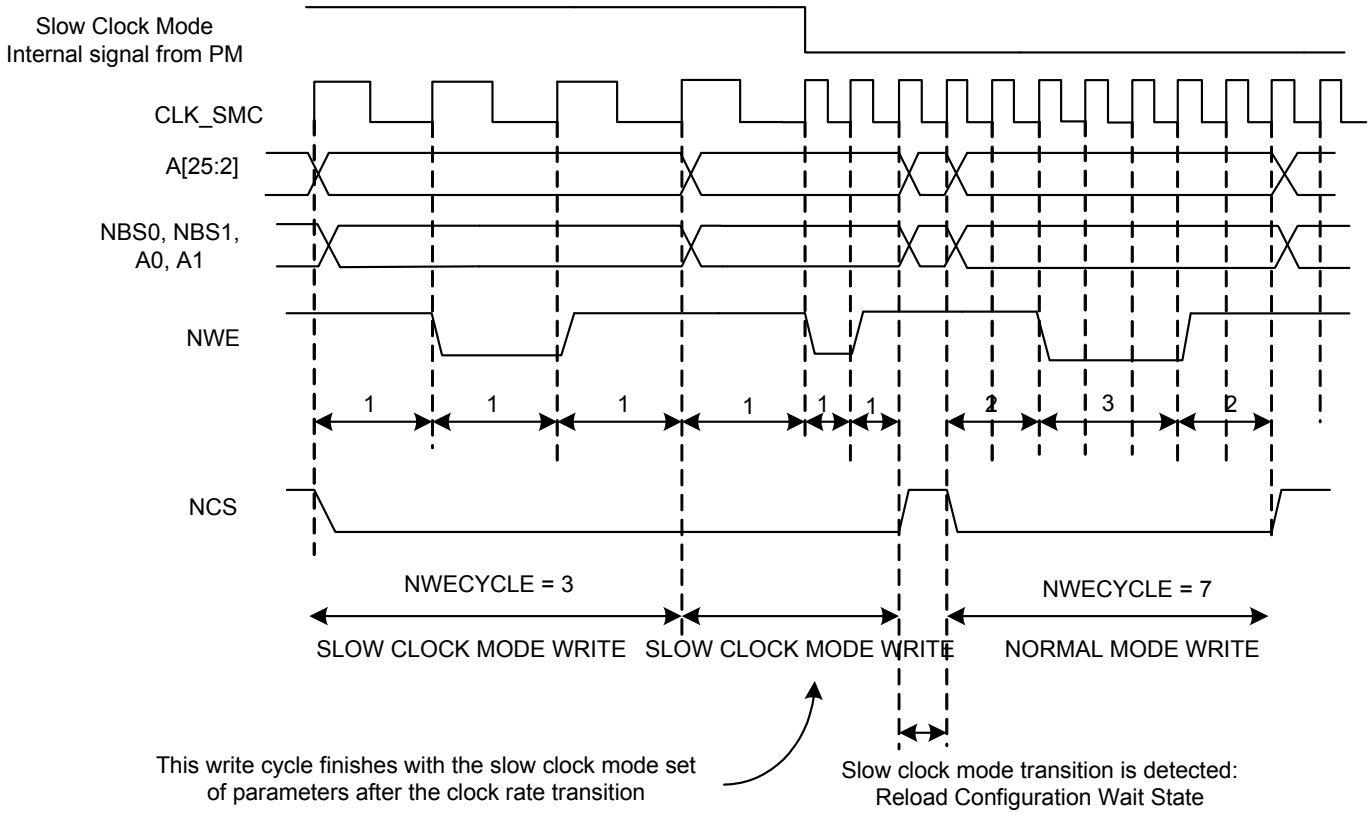
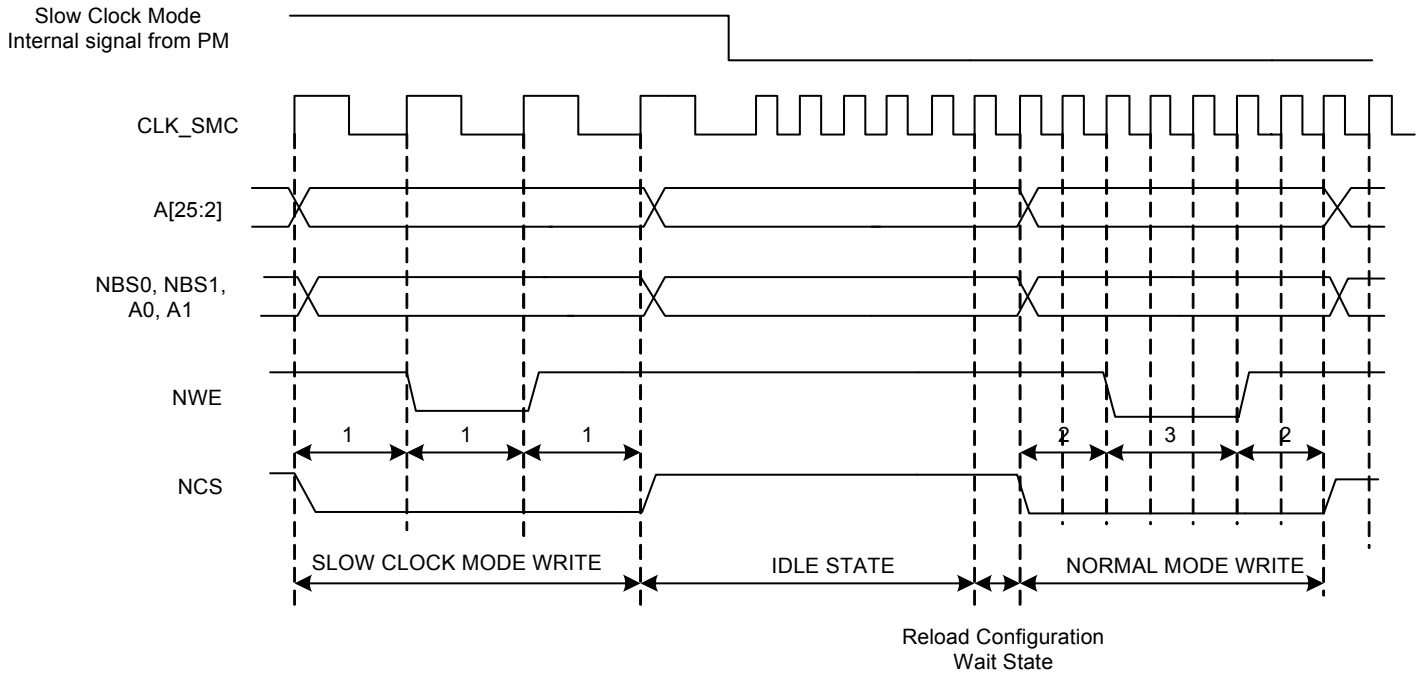


Figure 27-34. Recommended Procedure to Switch from Slow Clock Mode to Normal Mode or from Normal Mode to Slow Clock Mode



27.6.9 Asynchronous Page Mode

The SMC supports asynchronous burst reads in page mode, providing that the Page Mode Enabled bit is written to one in the MODE register (MODE.PMEN). The page size must be configured in the Page Size field in the MODE register (MODE.PS) to 4, 8, 16, or 32 bytes.

The page defines a set of consecutive bytes into memory. A 4-byte page (resp. 8-, 16-, 32-byte page) is always aligned to 4-byte boundaries (resp. 8-, 16-, 32-byte boundaries) of memory. The MSB of data address defines the address of the page in memory, the LSB of address define the address of the data in the page as detailed in Table 27-5 on page 524.

With page mode memory devices, the first access to one page (t_{pa}) takes longer than the subsequent accesses to the page (t_{sa}) as shown in Figure 27-35 on page 525. When in page mode, the SMC enables the user to define different read timings for the first access within one page, and next accesses within the page.

Table 27-5. Page Address and Data Address within a Page

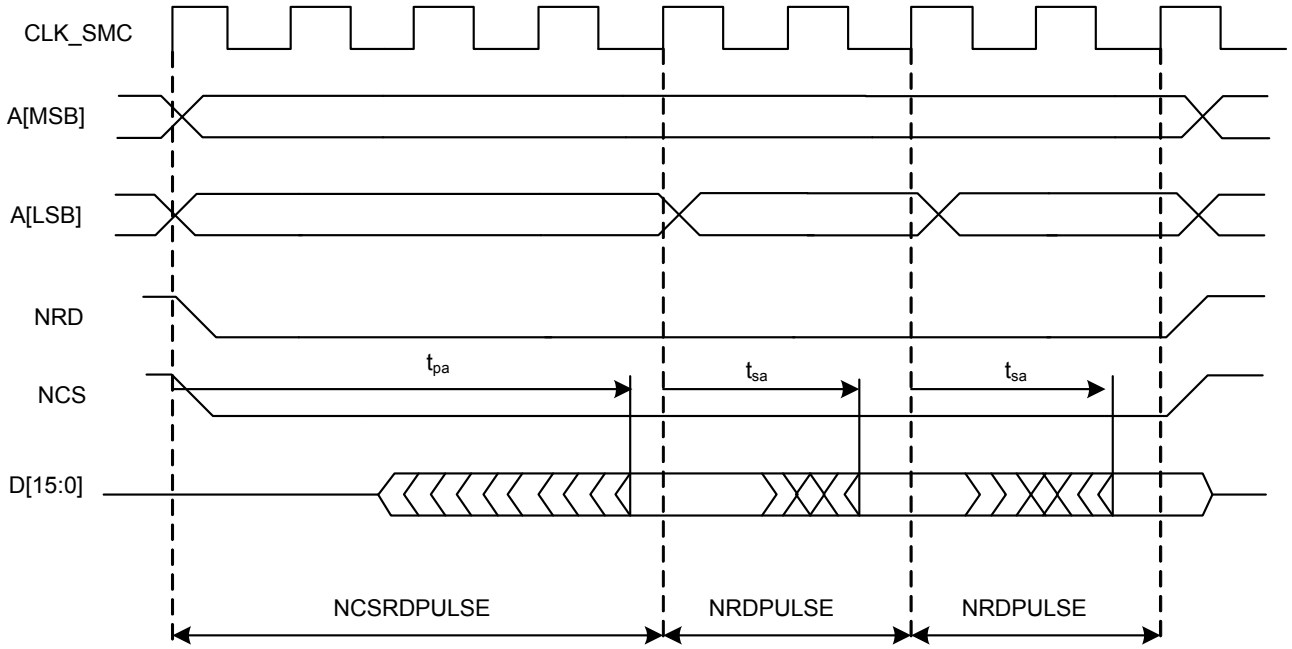
Page Size	Page Address(1)	Data Address in the Page(2)
4 bytes	A[25:2]	A[1:0]
8 bytes	A[25:3]	A[2:0]
16 bytes	A[25:4]	A[3:0]
32 bytes	A[25:5]	A[4:0]

Notes: 1. A denotes the address bus of the memory device
2. For 16-bit devices, the bit 0 of address is ignored. For 32-bit devices, bits [1:0] are ignored.

27.6.9.1 Protocol and timings in page mode

Figure 27-35 on page 525 shows the NRD and NCS timings in page mode access.

Figure 27-35. Page Mode Read Protocol (Address MSB and LSB Are Defined in Table 27-5 on page 524)



The NRD and NCS signals are held low during all read transfers, whatever the programmed values of the setup and hold timings in the User Interface may be. Moreover, the NRD and NCS timings are identical. The pulse length of the first access to the page is defined with the PULSE.NCSRDPULSE field value. The pulse length of subsequent accesses within the page are defined using the PULSE.NRDPULSE field value.

In page mode, the programming of the read timings is described in Table 27-6 on page 525:

Table 27-6. Programming of Read Timings in Page Mode

Parameter	Value	Definition
READMODE	'x'	No impact
NCSRDSETUP	'x'	No impact
NCSRDPULSE	t_{pa}	Access time of first access to the page
NRDSETUP	'x'	No impact
NRDPULSE	t_{sa}	Access time of subsequent accesses in the page
NRDCYCLE	'x'	No impact

The SMC does not check the coherency of timings. It will always apply the NCSRDPULSE timings as page access timing (t_{pa}) and the NRDPULSE for accesses to the page (t_{sa}), even if the programmed value for t_{pa} is shorter than the programmed value for t_{sa}.

27.6.9.2 Byte access type in page mode

The byte access type configuration remains active in page mode. For 16-bit or 32-bit page mode devices that require byte selection signals, configure the MODE.BAT bit to zero (byte select access type).

27.6.9.3 Page mode restriction

The page mode is not compatible with the use of the NWAIT signal. Using the page mode and the NWAIT signal may lead to unpredictable behavior.

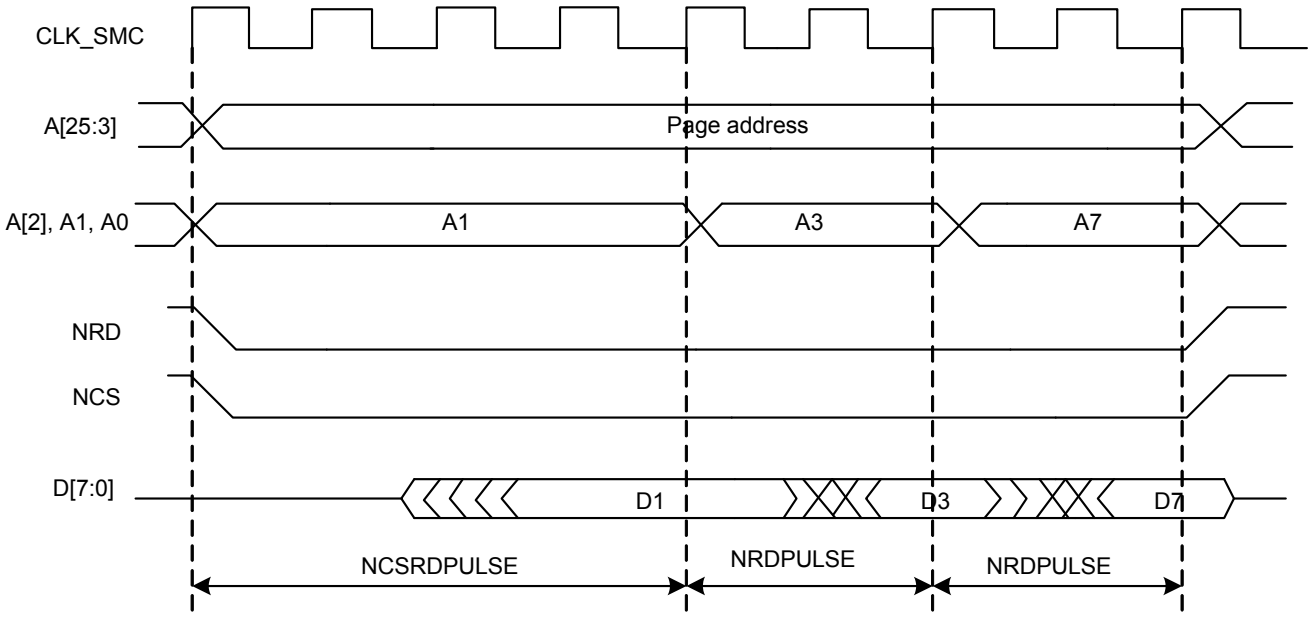
27.6.9.4 Sequential and non-sequential accesses

If the chip select and the MSB of addresses as defined in Table 27-5 on page 524 are identical, then the current access lies in the same page as the previous one, and no page break occurs.

Using this information, all data within the same page, sequential or not sequential, are accessed with a minimum access time (t_{sa}). Figure 27-36 on page 526 illustrates access to an 8-bit memory device in page mode, with 8-byte pages. Access to D1 causes a page access with a long access time (t_{pa}). Accesses to D3 and D7, though they are not sequential accesses, only require a short access time (t_{sa}).

If the MSB of addresses are different, the SMC performs the access of a new page. In the same way, if the chip select is different from the previous access, a page break occurs. If two sequential accesses are made to the page mode memory, but separated by an other internal or external peripheral access, a page break occurs on the second access because the chip select of the device was deasserted between both accesses.

Figure 27-36. Access to Non-sequential Data within the Same Page



27.7 User Interface

The SMC is programmed using the registers listed in Table 27-7 on page 527. For each chip select, a set of four registers is used to program the parameters of the external device connected on it. In Table 27-7 on page 527, “CS_number” denotes the chip select number. Sixteen bytes (0x10) are required per chip select.

The user must complete writing the configuration by writing anyone of the Mode Registers.

Table 27-7. SMC Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00 + CS_number*0x10	Setup Register	SETUP	Read/Write	0x01010101
0x04 + CS_number*0x10	Pulse Register	PULSE	Read/Write	0x01010101
0x08 + CS_number*0x10	Cycle Register	CYCLE	Read/Write	0x00030003
0x0C + CS_number*0x10	Mode Register	MODE	Read/Write	0x10002103

27.7.1 Setup Register

Register Name: SETUP

Access Type: Read/Write

Offset: 0x00 + CS_number*0x10

Reset Value: 0x01010101

31	30	29	28	27	26	25	24
–	–	NCSRDSETUP					

23	22	21	20	19	18	17	16
–	–	NRDSETUP					

15	14	13	12	11	10	9	8
–	–	NCSWRSETUP					

7	6	5	4	3	2	1	0
–	–	NWESETUP					

- **NCSRDSETUP: NCS Setup Length in READ Access**
  In read access, the NCS signal setup length is defined as:

$$\text{NCS Setup Length in read access} = (128 \times NCSRDSETUP[5] + NCSRDSETUP[4:0]) \text{ clock cycles}$$

- **NRDSETUP: NRD Setup Length**
  The NRD signal setup length is defined in clock cycles as:

$$\text{NRD Setup Length} = (128 \times NRDSETUP[5] + NRDSETUP[4:0]) \text{ clock cycles}$$

- **NCSWRSETUP: NCS Setup Length in WRITE Access**
  In write access, the NCS signal setup length is defined as:

$$\text{NCS Setup Length in write access} = (128 \times NCSWRSETUP[5] + NCSWRSETUP[4:0]) \text{ clock cycles}$$

- **NWESETUP: NWE Setup Length**
  The NWE signal setup length is defined as:

$$\text{NWE Setup Length} = (128 \times NWESETUP[5] + NWESETUP[4:0]) \text{ clock cycles}$$

27.7.2 Pulse Register

Register Name: PULSE

Access Type: Read/Write

Offset: 0x04 + CS_number*0x10

Reset Value: 0x01010101

31	30	29	28	27	26	25	24
–	NCSRDPULSE						

23	22	21	20	19	18	17	16
–	NRDPULSE						

15	14	13	12	11	10	9	8
–	NCSWRPULSE						

7	6	5	4	3	2	1	0
–	NWEPULSE						

- **NCSRDPULSE: NCS Pulse Length in READ Access**
  In standard read access, the NCS signal pulse length is defined as:

$$\text{NCS Pulse Length in read access} = (256 \times NCSRDPULSE[6] + NCSRDPULSE[5:0]) \text{ clock cycles}$$

  The NCS pulse length must be at least one clock cycle.
  In page mode read access, the NCSRDPULSE field defines the duration of the first access to one page.
- **NRDPULSE: NRD Pulse Length**
  In standard read access, the NRD signal pulse length is defined in clock cycles as:

$$\text{NRD Pulse Length} = (256 \times NRDPULSE[6] + NRDPULSE[5:0]) \text{ clock cycles}$$

  The NRD pulse length must be at least one clock cycle.
  In page mode read access, the NRDPULSE field defines the duration of the subsequent accesses in the page.
- **NCSWRPULSE: NCS Pulse Length in WRITE Access**
  In write access, the NCS signal pulse length is defined as:

$$\text{NCS Pulse Length in write access} = (256 \times NCSWRPULSE[6] + NCSWRPULSE[5:0]) \text{ clock cycles}$$

  The NCS pulse length must be at least one clock cycle.
- **NWEPULSE: NWE Pulse Length**
  The NWE signal pulse length is defined as:

$$\text{NWE Pulse Length} = (256 \times NWEPULSE[6] + NWEPULSE[5:0]) \text{ clock cycles}$$

  The NWE pulse length must be at least one clock cycle.

27.7.3 Cycle Register

Register Name: CYCLE

Access Type: Read/Write

Offset: 0x08 + CS_number*0x10

Reset Value: 0x00030003

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	NRDCYCLE[8]

23	22	21	20	19	18	17	16
NRDCYCLE[7:0]							

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	NWECYCLE[8]

7	6	5	4	3	2	1	0
NWECYCLE[7:0]							

- **NRDCYCLE[8:0]: Total Read Cycle Length**
  The total read cycle length is the total duration in clock cycles of the read cycle. It is equal to the sum of the setup, pulse and hold steps of the NRD and NCS signals. It is defined as:

$$\text{Read Cycle Length} = (256 \times NRDCYCLE[8:7] + NRDCYCLE[6:0]) \text{ clock cycles}$$

- **NWECYCLE[8:0]: Total Write Cycle Length**
  The total write cycle length is the total duration in clock cycles of the write cycle. It is equal to the sum of the setup, pulse and hold steps of the NWE and NCS signals. It is defined as:

$$\text{Write Cycle Length} = (256 \times NWECYCLE[8:7] + NWECYCLE[6:0]) \text{ clock cycles}$$

27.7.4 Mode Register

Register Name: MODE

Access Type: Read/Write

Offset: 0x0C + CS_number*0x10

Reset Value: 0x10002103

31	30	29	28	27	26	25	24
–	–	PS		–	–	–	PMEN

23	22	21	20	19	18	17	16
–	–	–	TDFMODE	TDFCYCLES			

15	14	13	12	11	10	9	8
–	–	DBW		–	–	–	BAT

7	6	5	4	3	2	1	0
–	–	EXNWMODE		–	–	WRITEMODE	READMODE

- **PS: Page Size**
  If page mode is enabled, this field indicates the size of the page in bytes.

PS	Page Size
0	4-byte page
1	8-byte page
2	16-byte page
3	32-byte page

- **PMEN: Page Mode Enabled**
  1: Asynchronous burst read in page mode is applied on the corresponding chip select.
  0: Standard read is applied.
- **TDFMODE: TDF Optimization**
  1: TDF optimization is enabled. The number of TDF wait states is optimized using the setup period of the next read/write access.
  0: TDF optimization is disabled.The number of TDF wait states is inserted before the next access begins.
- **TDFCYCLES: Data Float Time**
  This field gives the integer number of clock cycles required by the external device to release the data after the rising edge of the read controlling signal. The SMC always provide one full cycle of bus turnaround after the TDFCYCLES period. The external bus cannot be used by another chip select during TDFCYCLES plus one cycles. From 0 up to 15 TDFCYCLES can be set.

- **DBW: Data Bus Width**

DBW	Data Bus Width
0	8-bit bus
1	16-bit bus
2	32-bit bus
3	Reserved

- **BAT: Byte Access Type**

  This field is used only if DBW defines a 16- or 32-bit data bus.

BAT	Byte Access Type
0	Byte select access type: Write operation is controlled using NCS, NWE, NBS0, NBS1, NBS2, and NBS3 Read operation is controlled using NCS, NRD, NBS0, NBS1, NBS2, and NBS3
1	Byte write access type: Write operation is controlled using NCS, NWR0, NWR1, NWR2, and NWR3 Read operation is controlled using NCS and NRD

- **EXNWMODE: External WAIT Mode**

  The NWAIT signal is used to extend the current read or write signal. It is only taken into account during the pulse phase of the read and write controlling signal. When the use of NWAIT is enabled, at least one cycle hold duration must be programmed for the read and write controlling signal.

EXNWMODE	External NWAIT Mode
0	Disabled: the NWAIT input signal is ignored on the corresponding chip select.
1	Reserved
2	Frozen Mode: if asserted, the NWAIT signal freezes the current read or write cycle. after deassertion, the read or write cycle is resumed from the point where it was stopped.
3	Ready Mode: the NWAIT signal indicates the availability of the external device at the end of the pulse of the controlling read or write signal, to complete the access. If high, the access normally completes. If low, the access is extended until NWAIT returns high.

- **WRITEMODE: Write Mode**

  1: The write operation is controlled by the NWE signal. If TDF optimization is enabled (TDFMODE =1), TDF wait states will be inserted after the setup of NWE.

  0: The write operation is controlled by the NCS signal. If TDF optimization is enabled (TDFMODE =1), TDF wait states will be inserted after the setup of NCS.

- **READMODE: Read Mode**

READMODE	Read Access Mode
0	The read operation is controlled by the NCS signal. If TDF are programmed, the external bus is marked busy after the rising edge of NCS. If TDF optimization is enabled (TDFMODE = 1), TDF wait states are inserted after the setup of NCS.
1	The read operation is controlled by the NRD signal. If TDF cycles are programmed, the external bus is marked busy after the rising edge of NRD. If TDF optimization is enabled (TDFMODE =1), TDF wait states are inserted after the setup of NRD.

28. SDRAM Controller (SDRAMC)

Rev: 2.0.0.3

28.1 Features

- 256-Mbytes address space
- Numerous configurations supported
  - 2K, 4K, 8K row address memory parts
  - SDRAM with two or four internal banks
  - SDRAM with 16- or 32-bit data path
- Programming facilities
  - Word, halfword, byte access
  - Automatic page break when memory boundary has been reached
  - Multibank ping-pong access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
  - Automatic update of DS, TCR and PASR parameters (mobile SDRAM devices)
- Energy-saving capabilities
  - Self-refresh, power-down, and deep power-down modes supported
  - Supports mobile SDRAM devices
- Error detection
  - Refresh error interrupt
- SDRAM power-up initialization by software
- CAS latency of one, two, and three supported
- Auto Precharge command not used

28.2 Overview

The SDRAM Controller (SDRAMC) extends the memory capabilities of a chip by providing the interface to an external 16-bit or 32-bit SDRAM device. The page size supports ranges from 2048 to 8192 and the number of columns from 256 to 2048. It supports byte (8-bit), halfword (16-bit) and word (32-bit) accesses.

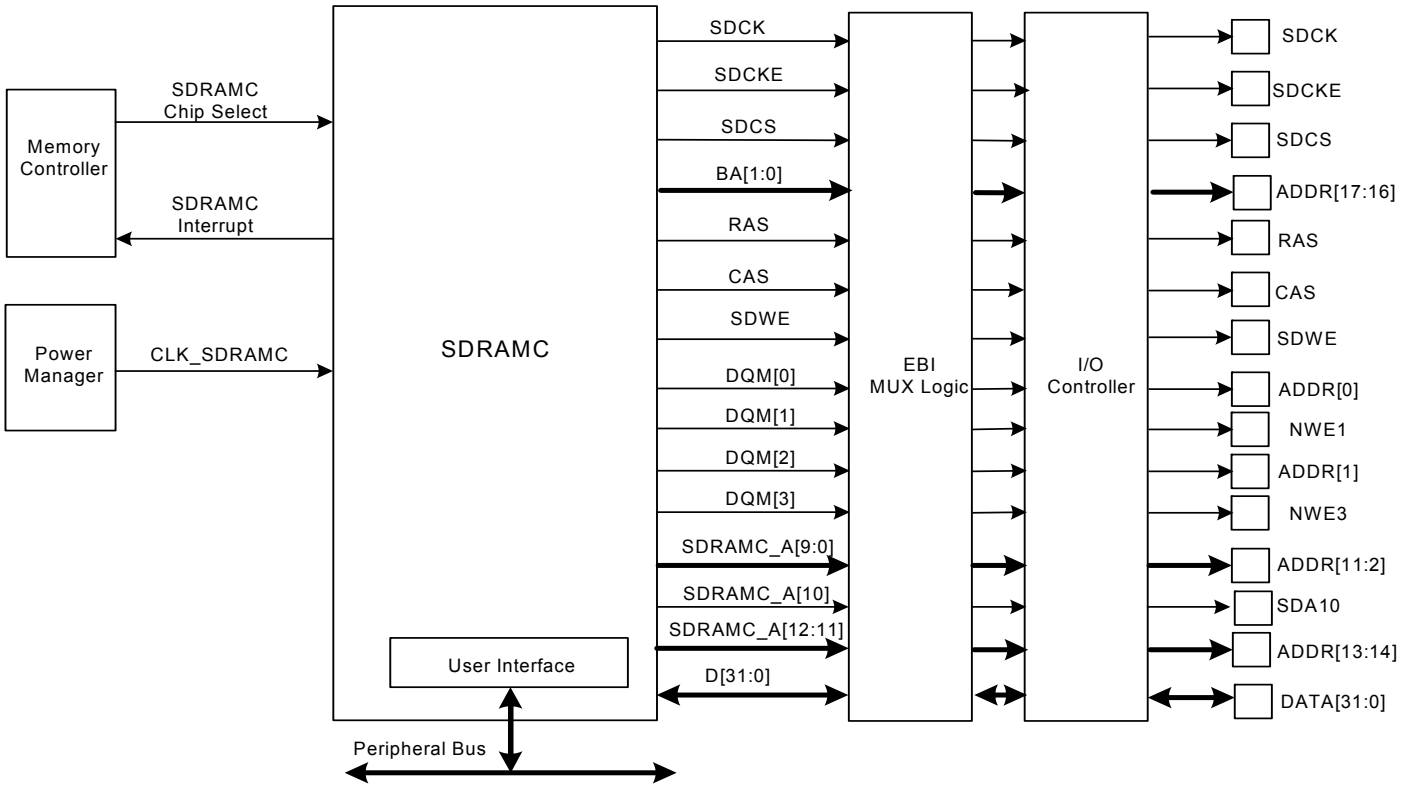
The SDRAMC supports a read or write burst length of one location. It keeps track of the active row in each bank, thus maximizing SDRAM performance, e.g., the application may be placed in one bank and data in the other banks. So as to optimize performance, it is advisable to avoid accessing different rows in the same bank.

The SDRAMC supports a CAS latency of one, two, or three and optimizes the read access depending on the frequency.

The different modes available (self refresh, power-down, and deep power-down modes) minimize power consumption on the SDRAM device.

28.3 Block Diagram

Figure 28-1. SDRAM Controller Block Diagram



28.4 I/O Lines Description

Table 28-1. I/O Lines Description

Name	Description	Type	Active Level
SDCK	SDRAM Clock	Output	
SDCKE	SDRAM Clock Enable	Output	High
SDCS	SDRAM Chip Select	Output	Low
BA[1:0]	Bank Select Signals	Output	
RAS	Row Signal	Output	Low
CAS	Column Signal	Output	Low
SDWE	SDRAM Write Enable	Output	Low
DQM[3:0]	Data Mask Enable Signals	Output	High
SDRAMC_A[12:0]	Address Bus	Output	
D[31:0]	Data Bus	Input/Output	

28.5 Application Example

28.5.1 Hardware Interface

Figure 28-2 on page 536 shows an example of SDRAM device connection to the SDRAMC using a 32-bit data bus width. Figure 28-3 on page 537 shows an example of SDRAM device connection using a 16-bit data bus width. It is important to note that these examples are given for a direct connection of the devices to the SDRAMC, without External Bus Interface or I/O Controller multiplexing.

Figure 28-2. SDRAM Controller Connections to SDRAM Devices: 32-bit Data Bus Width

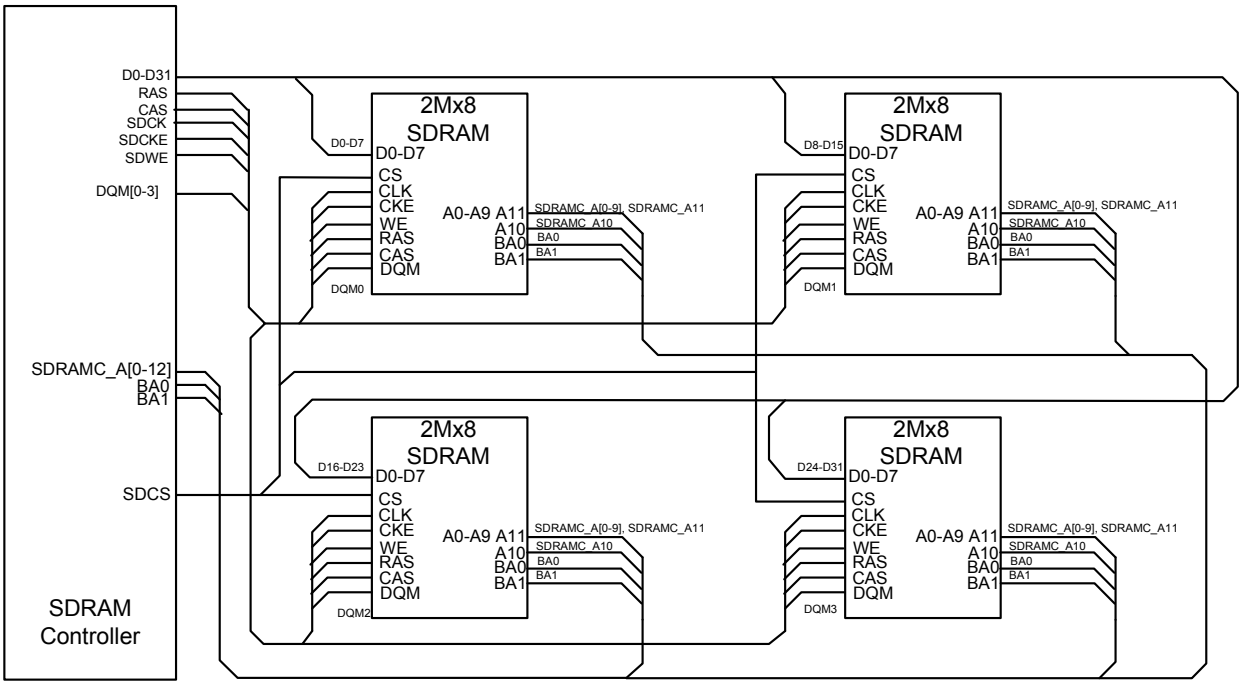
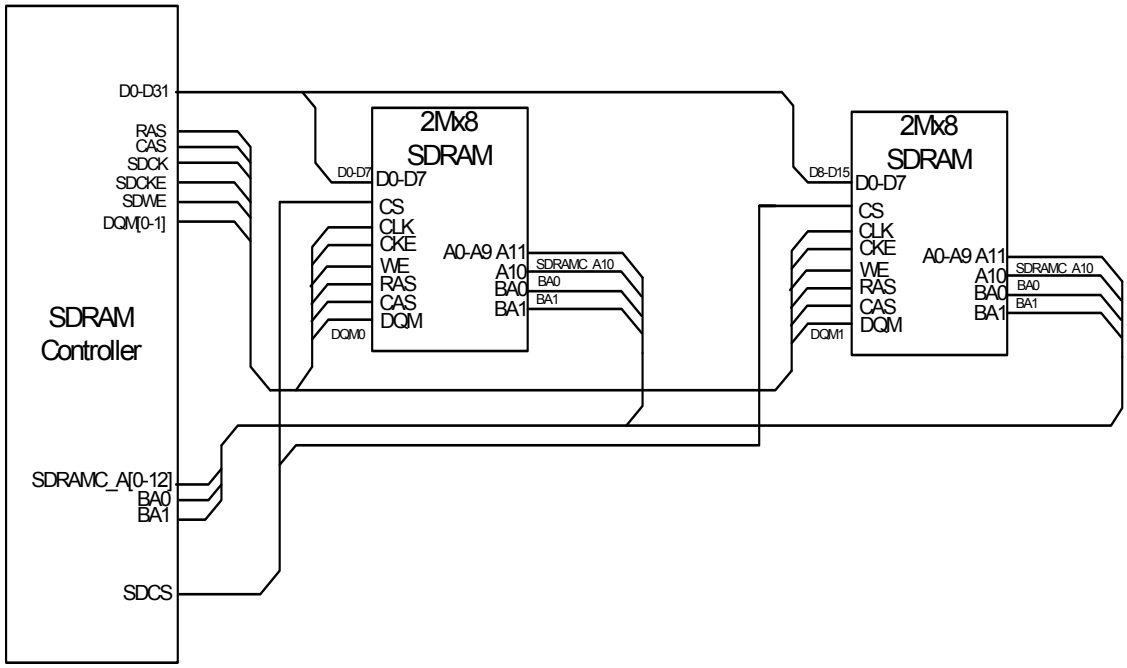


Figure 28-3. SDRAM Controller Connections to SDRAM Devices: 16-bit Data Bus Width



28.5.2 Software Interface

The SDRAM address space is organized into banks, rows, and columns. The SDRAMC allows mapping different memory types according to the values set in the SDRAMC Configuration Register (CR).

The SDRAMC's function is to make the SDRAM device access protocol transparent to the user. Table 28-2 on page 538 to Table 28-7 on page 539 illustrate the SDRAM device memory mapping seen by the user in correlation with the device structure. Various configurations are illustrated.

28.5.2.1 32-bit memory data bus width

Table 28-2. SDRAM Configuration Mapping: 2K Rows, 256/512/1024/2048 Columns

CPU Address Line																											
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					BA[1:0]		Row[10:0]											Column[7:0]								M[1:0]	
				BA[1:0]			Row[10:0]											Column[8:0]								M[1:0]	
			BA[1:0]				Row[10:0]											Column[9:0]								M[1:0]	
		BA[1:0]					Row[10:0]											Column[10:0]								M[1:0]	

Table 28-3. SDRAM Configuration Mapping: 4K Rows, 256/512/1024/2048 Columns

CPU Address Line																											
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				BA[1:0]			Row[11:0]											Column[7:0]								M[1:0]	
			BA[1:0]				Row[11:0]											Column[8:0]								M[1:0]	
		BA[1:0]					Row[11:0]											Column[9:0]								M[1:0]	
	BA[1:0]						Row[11:0]											Column[10:0]								M[1:0]	

Table 28-4. SDRAM Configuration Mapping: 8K Rows, 256/512/1024/2048 Columns

CPU Address Line																											
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			BA[1:0]				Row[12:0]											Column[7:0]								M[1:0]	
		BA[1:0]					Row[12:0]											Column[8:0]								M[1:0]	
	BA[1:0]						Row[12:0]											Column[9:0]								M[1:0]	
BA[1:0]							Row[12:0]											Column[10:0]								M[1:0]	

Notes: 1. M[1:0] is the byte address inside a 32-bit word.

28.5.2.2 16-bit memory data bus width

Table 28-5. SDRAM Configuration Mapping: 2K Rows, 256/512/1024/2048 Columns

CPU Address Line																										
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						BA[1:0]		Row[10:0]										Column[7:0]									M0
					BA[1:0]			Row[10:0]										Column[8:0]									M0
				BA[1:0]				Row[10:0]										Column[9:0]									M0
			BA[1:0]					Row[10:0]										Column[10:0]									M0

Table 28-6. SDRAM Configuration Mapping: 4K Rows, 256/512/1024/2048 Columns

CPU Address Line																										
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					BA[1:0]			Row[11:0]										Column[7:0]									M0
				BA[1:0]				Row[11:0]										Column[8:0]									M0
			BA[1:0]					Row[11:0]										Column[9:0]									M0
		BA[1:0]						Row[11:0]										Column[10:0]									M0

Table 28-7. SDRAM Configuration Mapping: 8K Rows, 256/512/1024/2048 Columns

CPU Address Line																										
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				BA[1:0]				Row[12:0]										Column[7:0]									M0
			BA[1:0]					Row[12:0]										Column[8:0]									M0
		BA[1:0]						Row[12:0]										Column[9:0]									M0
	BA[1:0]							Row[12:0]										Column[10:0]									M0

Notes: 1. M0 is the byte address inside a 16-bit halfword.

28.6 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

28.6.1 I/O Lines

The SDRAMC module signals pass through the External Bus Interface (EBI) module where they are multiplexed. The user must first configure the I/O controller to assign the EBI pins corresponding to SDRAMC signals to their peripheral function. If I/O lines of the EBI corresponding to SDRAMC signals are not used by the application, they can be used for other purposes by the I/O Controller.

28.6.2 Power Management

The SDRAMC must be properly stopped before entering in reset mode, i.e., the user must issue a Deep power mode command in the Mode (MD) register and wait for the command to be completed.

28.6.3 Clocks

The clock for the SDRAMC bus interface (CLK_SDRAMC) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager. It is recommended to disable the SDRAMC before disabling the clock, to avoid freezing the SDRAMC in an undefined state.

28.6.4 Interrupts

The SDRAMC interrupt request line is connected to the interrupt controller. Using the SDRAMC interrupt requires the interrupt controller to be programmed first.

28.7 Functional Description

28.7.1 SDRAM Device Initialization

The initialization sequence is generated by software. The SDRAM devices are initialized by the following sequence:

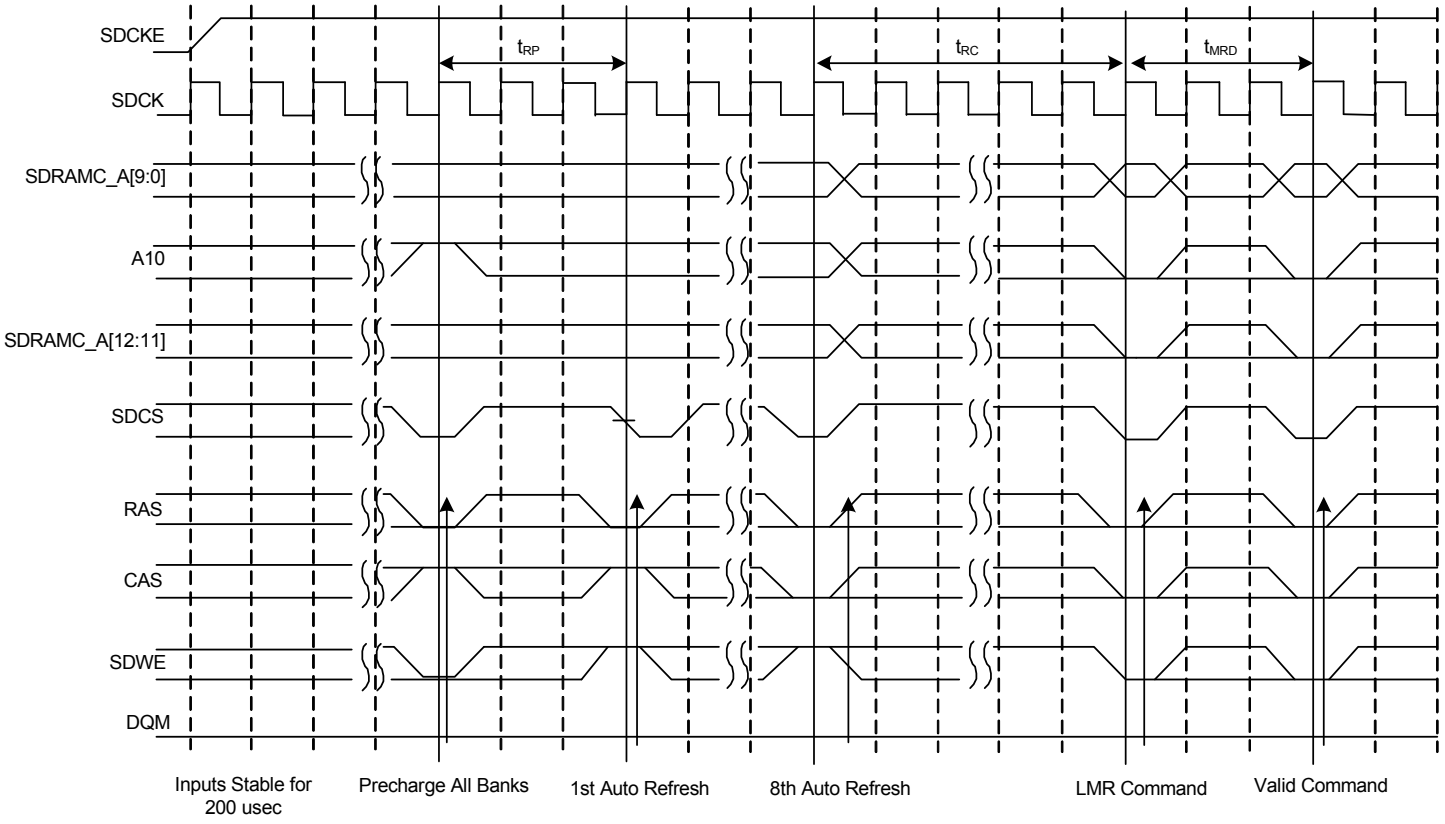
1. SDRAM features must be defined in the CR register by writing the following fields with the desired value: asynchronous timings (TXSR, TRAS, TRCD, TRP, TRC, and TWR), Number of Columns (NC), Number of Rows (NR), Number of Banks (NB), CAS Latency (CAS), and the Data Bus Width (DBW).
2. For mobile SDRAM devices, Temperature Compensated Self Refresh (TCSR), Drive Strength (DS) and Partial Array Self Refresh (PASR) fields must be defined in the Low Power Register (LPR).
3. The Memory Device Type field must be defined in the Memory Device Register (MDR.MD).
4. A No Operation (NOP) command must be issued to the SDRAM devices to start the SDRAM clock. The user must write the value one to the Command Mode field in the SDRAMC Mode Register (MR.MODE) and perform a write access to any SDRAM address.
5. A minimum pause of 200µs is provided to precede any signal toggle.
6. An All Banks Precharge command must be issued to the SDRAM devices. The user must write the value two to the MR.MODE field and perform a write access to any SDRAM address.
7. Eight Auto Refresh commands are provided. The user must write the value four to the MR.MODE field and performs a write access to any SDRAM location eight times.
8. A Load Mode Register command must be issued to program the parameters of the SDRAM devices in its Mode Register, in particular CAS latency, burst type, and burst length. The user must write the value three to the MR.MODE field and perform a write access to the SDRAM. The write address must be chosen so that BA[1:0] are set to zero. See Section 28.8.1 for details about Load Mode Register command.
9. For mobile SDRAM initialization, an Extended Load Mode Register command must be issued to program the SDRAM devices parameters (TCSR, PASR, DS). The user must write the value five to the MR.MODE field and perform a write access to the SDRAM. The

write address must be chosen so that BA[1] or BA[0] are equal to one. See Section 28.8.1 for details about Extended Load Mode Register command.

10. The user must go into Normal Mode, writing the value 0 to the MR.MODE field and performing a write access at any location in the SDRAM.
11. Write the refresh rate into the Refresh Timer Count field in the Refresh Timer Register (TR.COUNT). The refresh rate is the delay between two successive refresh cycles. The SDRAM device requires a refresh every 15.625µs or 7.81µs. With a 100MHz frequency, the TR register must be written with the value 1562 (15.625 µs x 100 MHz) or 781 (7.81 µs x 100 MHz).

After initialization, the SDRAM devices are fully functional.

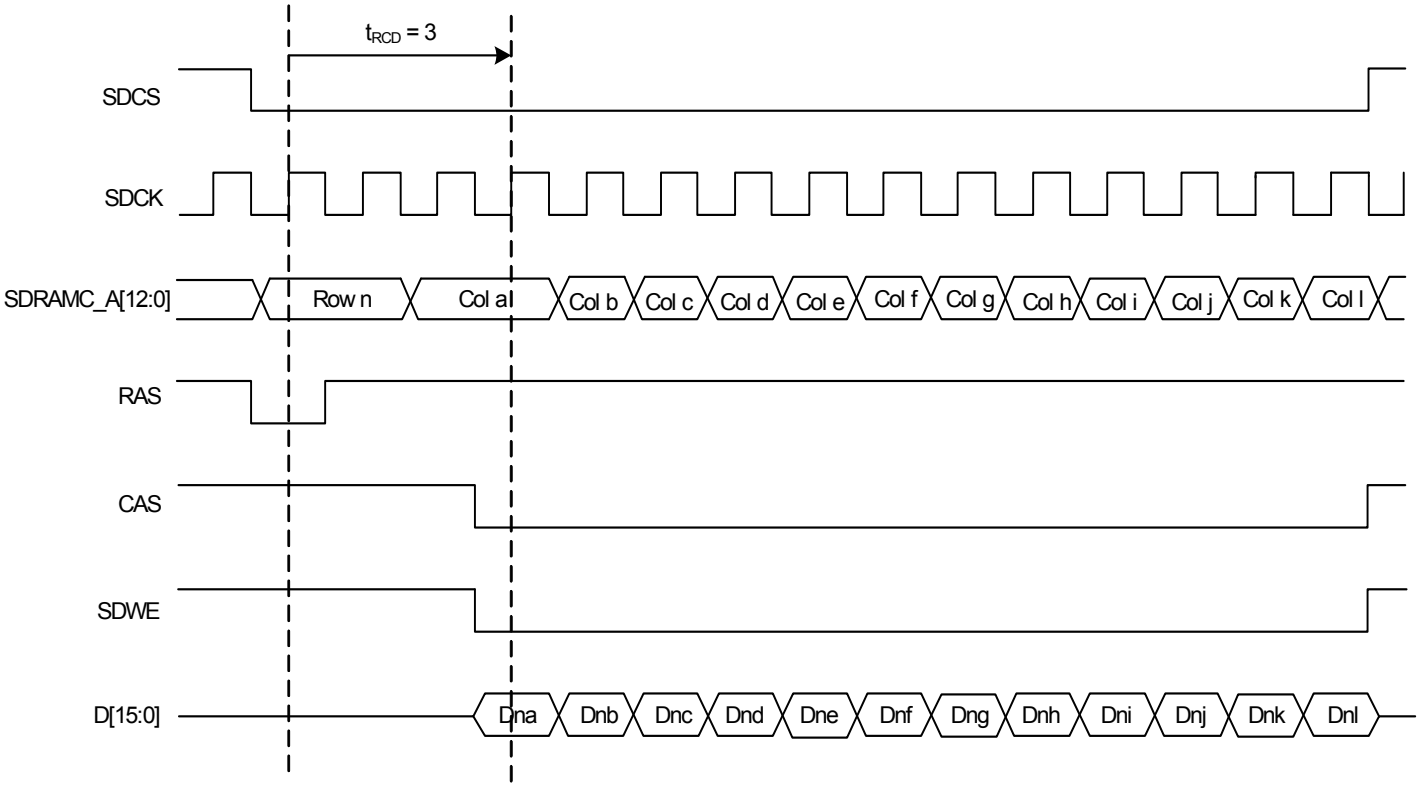
Figure 28-4. SDRAM Device Initialization Sequence



28.7.2 SDRAM Controller Write Cycle

The SDRAMC allows burst access or single access. In both cases, the SDRAMC keeps track of the active row in each bank, thus maximizing performance. To initiate a burst access, the SDRAMC uses the transfer type signal provided by the master requesting the access. If the next access is a sequential write access, writing to the SDRAM device is carried out. If the next access is a write-sequential access, but the current access is to a boundary page, or if the next access is in another row, then the SDRAMC generates a precharge command, activates the new row and initiates a write command. To comply with SDRAM timing parameters, additional clock cycles are inserted between precharge and active (t_{RP}) commands and between active and write (t_{RCD}) commands. For definition of these timing parameters, refer to the Section 28.8.3. This is described in Figure 28-5 on page 542.

Figure 28-5. Write Burst, 16-bit SDRAM Access



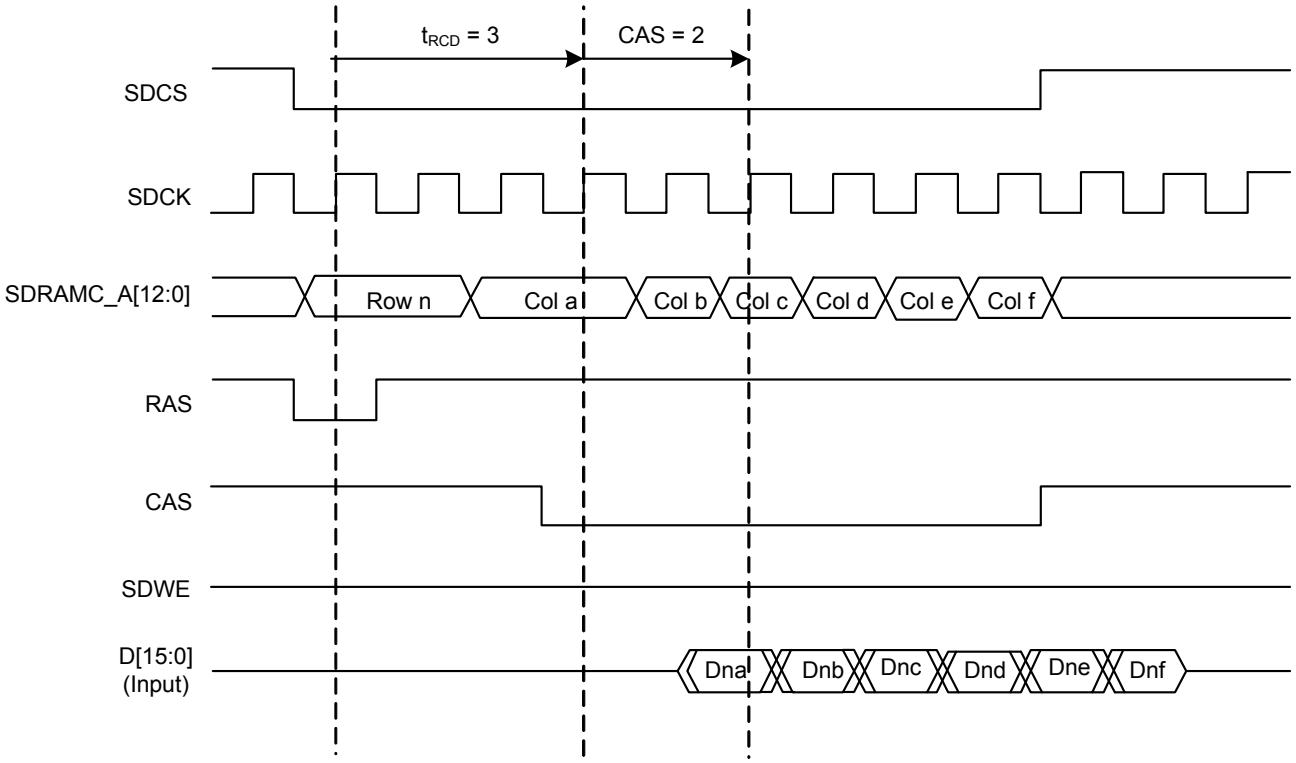
28.7.3 SDRAM Controller Read Cycle

The SDRAMC allows burst access, incremental burst of unspecified length or single access. In all cases, the SDRAMC keeps track of the active row in each bank, thus maximizing performance of the SDRAM. If row and bank addresses do not match the previous row/bank address, then the SDRAMC automatically generates a precharge command, activates the new row and starts the read command. To comply with the SDRAM timing parameters, additional clock cycles on SDCK are inserted between precharge and active (t_{RP}) commands and between active and read (t_{RCD}) commands. These two parameters are set in the CR register of the SDRAMC. After a read command, additional wait states are generated to comply with the CAS latency (one, two, or three clock delays specified in the CR register).

For a single access or an incremented burst of unspecified length, the SDRAMC anticipates the next access. While the last value of the column is returned by the SDRAMC on the bus, the SDRAMC anticipates the read to the next column and thus anticipates the CAS latency. This reduces the effect of the CAS latency on the internal bus.

For burst access of specified length (4, 8, 16 words), access is not anticipated. This case leads to the best performance. If the burst is broken (border, busy mode, etc.), the next access is handled as an incrementing burst of unspecified length.

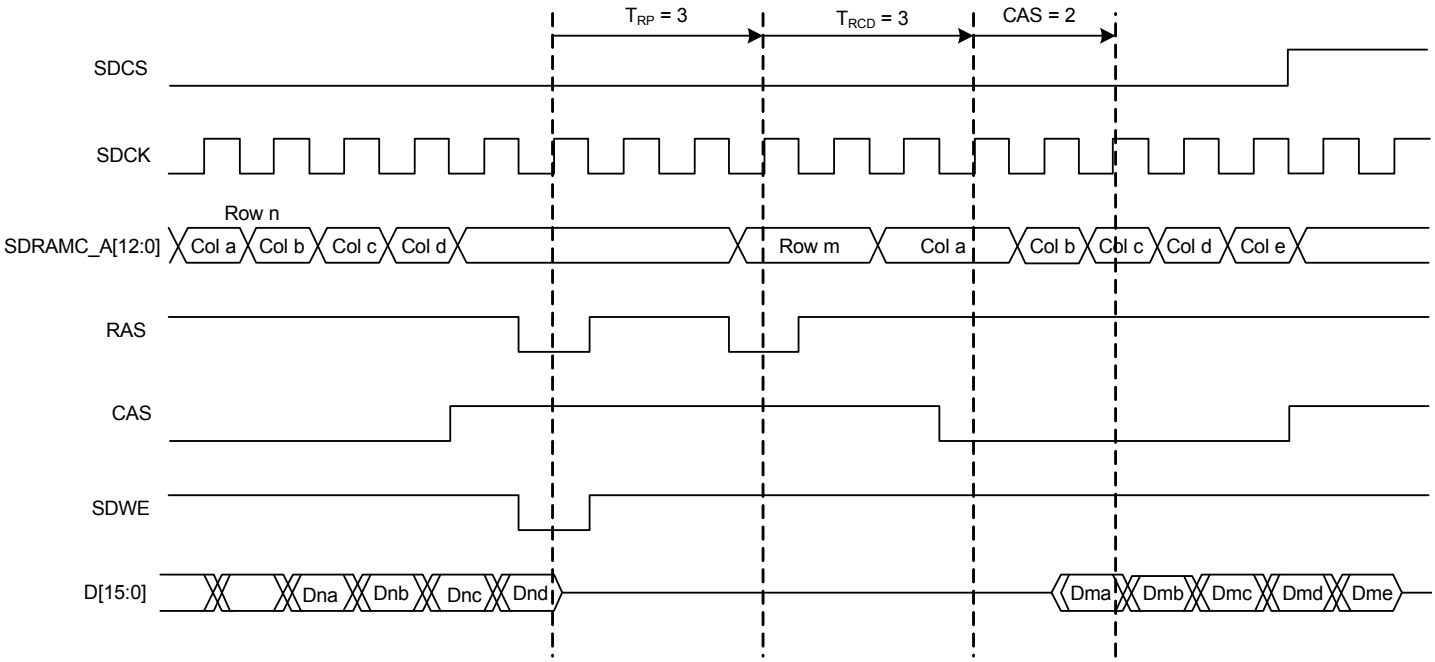
Figure 28-6. Read Burst, 16-bit SDRAM Access



28.7.4 Border Management

When the memory row boundary has been reached, an automatic page break is inserted. In this case, the SDRAMC generates a precharge command, activates the new row and initiates a read or write command. To comply with SDRAM timing parameters, an additional clock cycle is inserted between the precharge and active (t_{RP}) commands and between the active and read (t_{RCD}) commands. This is described in Figure 28-7 on page 544.

Figure 28-7. Read Burst with Boundary Row Access



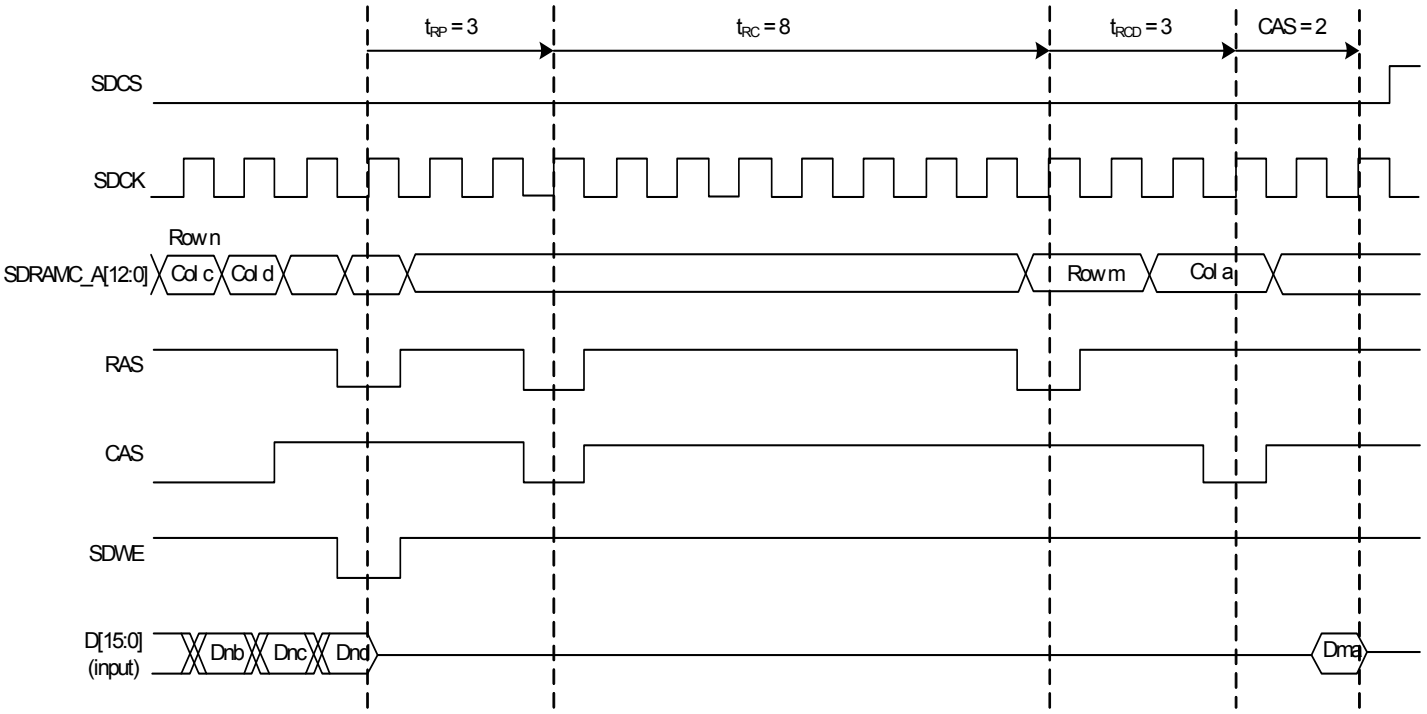
28.7.5 SDRAM Controller Refresh Cycles

An auto refresh command is used to refresh the SDRAM device. Refresh addresses are generated internally by the SDRAM device and incremented after each auto refresh automatically. The SDRAMC generates these auto refresh commands periodically. An internal timer is loaded with the value in the Refresh Timer Register (TR) that indicates the number of clock cycles between successive refresh cycles.

A refresh error interrupt is generated when the previous auto refresh command did not perform. In this case a Refresh Error Status bit is set in the Interrupt Status Register (ISR.RES). It is cleared by reading the ISR register.

When the SDRAMC initiates a refresh of the SDRAM device, internal memory accesses are not delayed. However, if the CPU tries to access the SDRAM, the slave indicates that the device is busy and the master is held by a wait signal. See Figure 28-8 on page 545.

Figure 28-8. Refresh Cycle Followed by a Read Access



28.7.6 Power Management

Three low power modes are available:

- Self refresh mode: the SDRAM executes its own auto refresh cycles without control of the SDRAMC. Current drained by the SDRAM is very low.
- Power-down mode: auto refresh cycles are controlled by the SDRAMC. Between auto refresh cycles, the SDRAM is in power-down. Current drained in power-down mode is higher than in self refresh mode.
- Deep power-down mode (only available with mobile SDRAM): the SDRAM contents are lost, but the SDRAM does not drain any current.

The SDRAMC activates one low power mode as soon as the SDRAM device is not selected. It is possible to delay the entry in self refresh and power-down mode after the last access by configuring the Timeout field in the Low Power Register (LPR.TIMEOUT).

28.7.6.1 Self refresh mode

This mode is selected by writing the value one to the Low Power Configuration Bits field in the SDRAMC Low Power Register (LPR.LPCB). In self refresh mode, the SDRAM device retains data without external clocking and provides its own internal clocking, thus performing its own auto refresh cycles. All the inputs to the SDRAM device become “don’t care” except SDCKE, which remains low. As soon as the SDRAM device is selected, the SDRAMC provides a sequence of commands and exits self refresh mode.

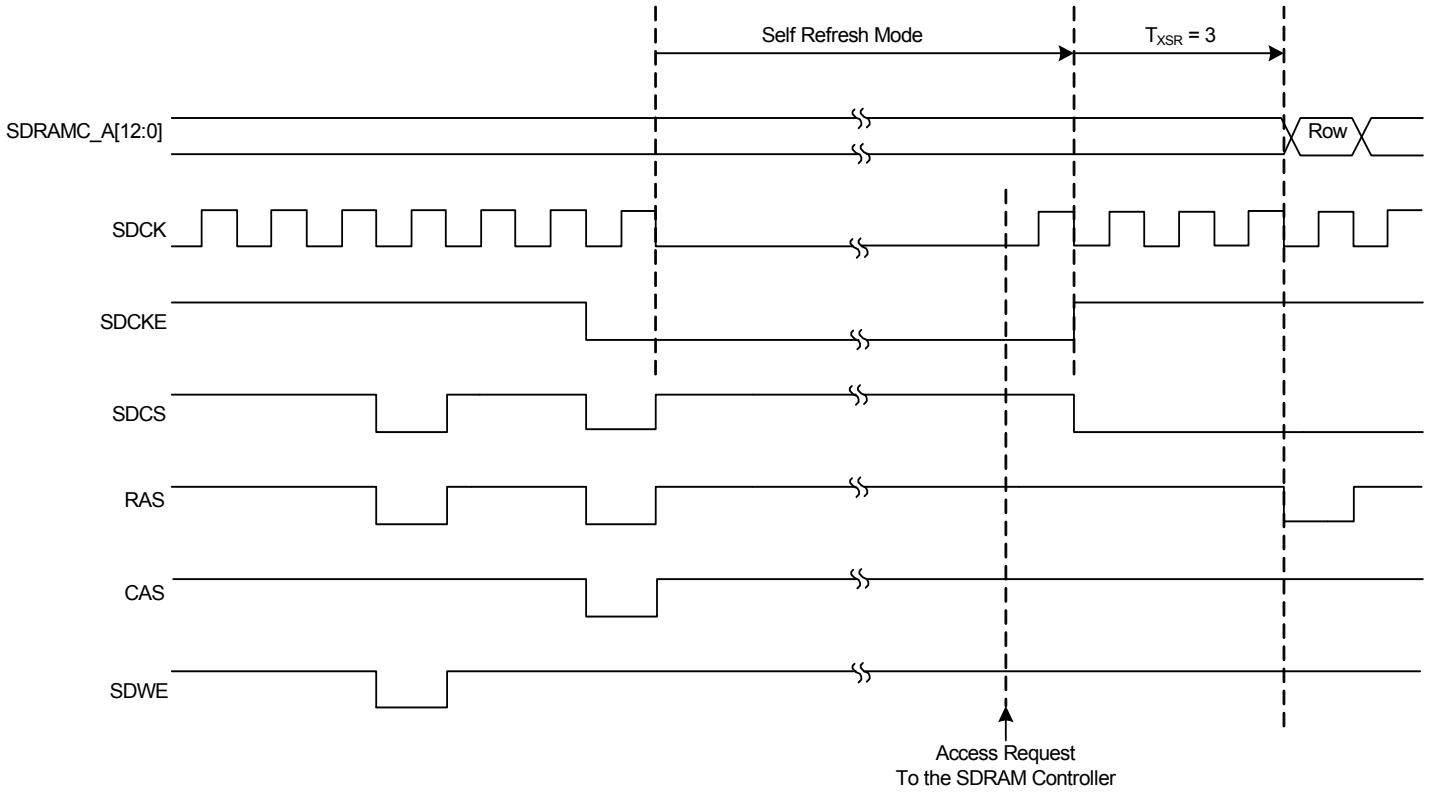
Some low power SDRAMs (e.g., mobile SDRAM) can refresh only one quarter or a half quarter or all banks of the SDRAM array. This feature reduces the self refresh current. To configure this feature, Temperature Compensated Self Refresh (TCSR), Partial Array Self Refresh (PASR)

and Drive Strength (DS) parameters must be set by writing the corresponding fields in the LPR register, and transmitted to the low power SDRAM device during initialization.

After initialization, as soon as the LPR.PASR, LPR.DS, or LPR.TCSR fields are modified and self refresh mode is activated, the SDRAMC issues an Extended Load Mode Register command to the SDRAM and the Extended Mode Register of the SDRAM device is accessed automatically. The PASR/DS/TCSR parameters values are therefore updated before entry into self refresh mode.

The SDRAM device must remain in self refresh mode for a minimum period of t_{RAS} and may remain in self refresh mode for an indefinite period. This is described in Figure 28-9 on page 546.

Figure 28-9. Self Refresh Mode Behavior

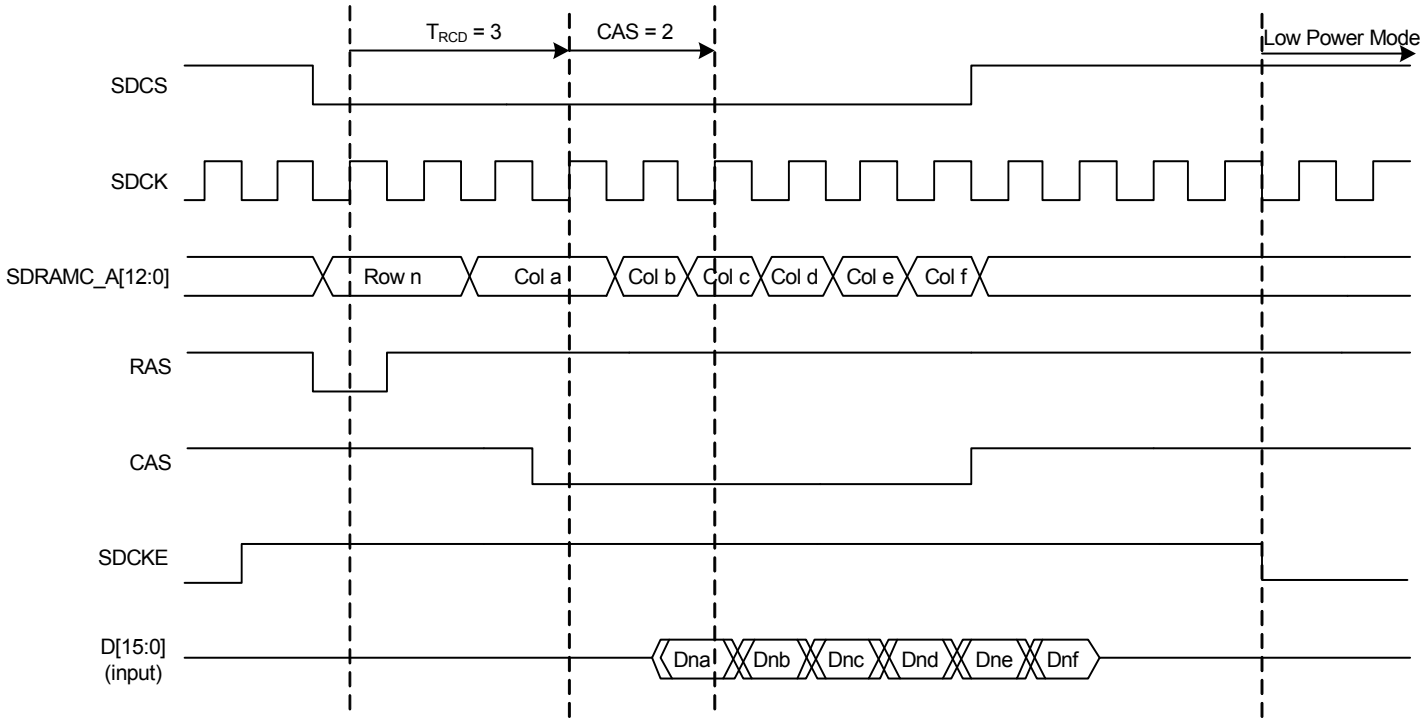


28.7.6.2 Low power mode

This mode is selected by writing the value two to the LPR.LPCB field. Power consumption is greater than in self refresh mode. All the input and output buffers of the SDRAM device are deactivated except SDCKE, which remains low. In contrast to self refresh mode, the SDRAM device cannot remain in low power mode longer than the refresh period (64ms for a whole device refresh operation). As no auto refresh operations are performed by the SDRAM itself, the SDRAMC carries out the refresh operation. The exit procedure is faster than in self refresh mode.

This is described in Figure 28-10 on page 547.

Figure 28-10. Low Power Mode Behavior



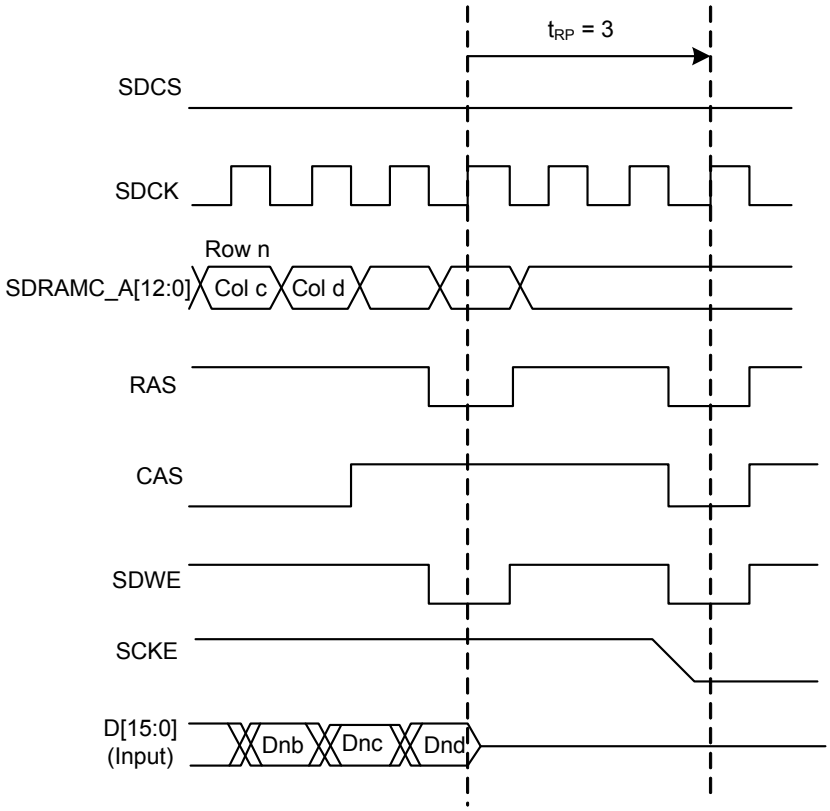
28.7.6.3 Deep power-down mode

This mode is selected by writing the value three to the LPR.LPCB field. When this mode is activated, all internal voltage generators inside the SDRAM are stopped and all data is lost.

When this mode is enabled, the user must not access to the SDRAM until a new initialization sequence is done (See Section 28.7.1).

This is described in Figure 28-11 on page 548.

Figure 28-11. Deep Power-down Mode Behavior



28.8 User Interface

Table 28-8. SDRAMC Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00	Mode Register	MR	Read/Write	0x00000000
0x04	Refresh Timer Register	TR	Read/Write	0x00000000
0x08	Configuration Register	CR	Read/Write	0x852372C0
0x0C	High Speed Register	HSR	Read/Write	0x00000000
0x10	Low Power Register	LPR	Read/Write	0x00000000
0x14	Interrupt Enable Register	IER	Write-only	0x00000000
0x18	Interrupt Disable Register	IDR	Write-only	0x00000000
0x1C	Interrupt Mask Register	IMR	Read-only	0x00000000
0x20	Interrupt Status Register	ISR	Read-only	0x00000000
0x24	Memory Device Register	MDR	Read/Write	0x00000000

28.8.1 Mode Register

Register Name: MR

Access Type: Read/Write

Offset: 0x00

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	MODE		

- **MODE: Command Mode**
  This field defines the command issued by the SDRAMC when the SDRAM device is accessed.

MODE	Description
0	Normal mode. Any access to the SDRAM is decoded normally.
1	The SDRAMC issues a “NOP” command when the SDRAM device is accessed regardless of the cycle.
2	The SDRAMC issues an “All Banks Precharge” command when the SDRAM device is accessed regardless of the cycle.
3	The SDRAMC issues a “Load Mode Register” command when the SDRAM device is accessed regardless of the cycle. This command will load the CR.CAS field into the SDRAM device Mode Register. All the other parameters of the SDRAM device Mode Register will be set to zero (burst length, burst type, operating mode, write burst mode...).
4	The SDRAMC issues an “Auto Refresh” command when the SDRAM device is accessed regardless of the cycle. Previously, an “All Banks Precharge” command must be issued.
5	The SDRAMC issues an “Extended Load Mode Register” command when the SDRAM device is accessed regardless of the cycle. This command will load the LPR.PASR, LPR.DS, and LPR.TCR fields into the SDRAM device Extended Mode Register. All the other bits of the SDRAM device Extended Mode Register will be set to zero.
6	Deep power-down mode. Enters deep power-down mode.

28.8.2 Refresh Timer Register

Register Name: TR

Access Type: Read/Write

Offset: 0x04

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	COUNT[11:8]			

7	6	5	4	3	2	1	0
COUNT[7:0]							

- **COUNT[11:0]: Refresh Timer Count**

  This 12-bit field is loaded into a timer that generates the refresh pulse. Each time the refresh pulse is generated, a refresh burst is initiated.

  The value to be loaded depends on the SDRAMC clock frequency (CLK_SDRAMC), the refresh rate of the SDRAM device and the refresh burst length where 15.6µs per row is a typical value for a burst of length one.

  To refresh the SDRAM device, this 12-bit field must be written. If this condition is not satisfied, no refresh command is issued and no refresh of the SDRAM device is carried out.

28.8.3 Configuration Register

Register Name: CR

Access Type: Read/Write

Offset: 0x08

Reset Value: 0x852372C0

31	30	29	28	27	26	25	24
TXSR				TRAS			
23	22	21	20	19	18	17	16
TRCD				TRP			
15	14	13	12	11	10	9	8
TRC				TWR			
7	6	5	4	3	2	1	0
DBW	CAS		NB	NR		NC	

- **TXSR: Exit Self Refresh to Active Delay**
  Reset value is eight cycles.
  This field defines the delay between SCKE set high and an Activate command in number of cycles. Number of cycles is between 0 and 15.
- **TRAS: Active to Precharge Delay**
  Reset value is five cycles.
  This field defines the delay between an Activate command and a Precharge command in number of cycles. Number of cycles is between 0 and 15.
- **TRCD: Row to Column Delay**
  Reset value is two cycles.
  This field defines the delay between an Activate command and a Read/Write command in number of cycles. Number of cycles is between 0 and 15.
- **TRP: Row Precharge Delay**
  Reset value is three cycles.
  This field defines the delay between a Precharge command and another command in number of cycles. Number of cycles is between 0 and 15.
- **TRC: Row Cycle Delay**
  Reset value is seven cycles.
  This field defines the delay between a Refresh and an Activate Command in number of cycles. Number of cycles is between 0 and 15.
- **TWR: Write Recovery Delay**
  Reset value is two cycles.
  This field defines the Write Recovery Time in number of cycles. Number of cycles is between 0 and 15.
- **DBW: Data Bus Width**
  Reset value is 16 bits.
  0: Data bus width is 32 bits.
  1: Data bus width is 16 bits.

- **CAS: CAS Latency**
  Reset value is two cycles.
  In the SDRAMC, only a CAS latency of one, two and three cycles is managed.

CAS	CAS Latency (Cycles)
0	Reserved
1	1
2	2
3	3

- **NB: Number of Banks**
  Reset value is two banks.

NB	Number of Banks
0	2
1	4

- **NR: Number of Row Bits**
  Reset value is 11 row bits.

NR	Row Bits
0	11
1	12
2	13
3	Reserved

- **NC: Number of Column Bits**
  Reset value is 8 column bits.

NC	Column Bits
0	8
1	9
2	10
3	11

28.8.4 High Speed Register

Register Name: HSR

Access Type: Read/Write

Offset: 0x0C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DA

- **DA: Decode Cycle Enable**

  A decode cycle can be added on the addresses as soon as a non-sequential access is performed on the HSB bus.

  The addition of the decode cycle allows the SDRAMC to gain time to access the SDRAM memory.

  1: Decode cycle is enabled.

  0: Decode cycle is disabled.

28.8.5 Low Power Register

Register Name: LPR

Access Type: Read/Write

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	TIMEOUT		DS		TCSR	

7	6	5	4	3	2	1	0
-	PASR			-	-	LPCB	

- **TIMEOUT: Time to Define when Low Power Mode Is Enabled**

TIMEOUT	Time to Define when Low Power Mode Is Enabled
0	The SDRAMC activates the SDRAM low power mode immediately after the end of the last transfer.
1	The SDRAMC activates the SDRAM low power mode 64 clock cycles after the end of the last transfer.
2	The SDRAMC activates the SDRAM low power mode 128 clock cycles after the end of the last transfer.
3	Reserved.

- **DS: Drive Strength (only for low power SDRAM)**
  This field is transmitted to the SDRAM during initialization to select the SDRAM strength of data output. This parameter must be set according to the SDRAM device specification.
  After initialization, as soon as this field is modified and self refresh mode is activated, the Extended Mode Register of the SDRAM device is accessed automatically and its DS parameter value is updated before entry in self refresh mode.
- **TCSR: Temperature Compensated Self Refresh (only for low power SDRAM)**
  This field is transmitted to the SDRAM during initialization to set the refresh interval during self refresh mode depending on the temperature of the low power SDRAM. This parameter must be set according to the SDRAM device specification.
  After initialization, as soon as this field is modified and self refresh mode is activated, the Extended Mode Register of the SDRAM device is accessed automatically and its TCSR parameter value is updated before entry in self refresh mode.
- **PASR: Partial Array Self Refresh (only for low power SDRAM)**
  This field is transmitted to the SDRAM during initialization to specify whether only one quarter, one half or all banks of the SDRAM array are enabled. Disabled banks are not refreshed in self refresh mode. This parameter must be set according to the SDRAM device specification.
  After initialization, as soon as this field is modified and self refresh mode is activated, the Extended Mode Register of the SDRAM device is accessed automatically and its PASR parameter value is updated before entry in self refresh mode.

- **LPCB: Low Power Configuration Bits**

LPCB	Low Power Configuration
0	Low power feature is inhibited: no power-down, self refresh or deep power-down command is issued to the SDRAM device.
1	The SDRAMC issues a self refresh command to the SDRAM device, the SDCLK clock is deactivated and the SDCKE signal is set low. The SDRAM device leaves the self refresh mode when accessed and enters it after the access.
2	The SDRAMC issues a power-down command to the SDRAM device after each access, the SDCKE signal is set to low. The SDRAM device leaves the power-down mode when accessed and enters it after the access.
3	The SDRAMC issues a deep power-down command to the SDRAM device. This mode is unique to low-power SDRAM.

28.8.6 Interrupt Enable Register

Register Name: IER

Access Type: Write-only

Offset: 0x14

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	RES

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will set the corresponding bit in IMR.

28.8.7 Interrupt Disable Register

Register Name: IDR

Access Type: Write-only

Offset: 0x18

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	RES

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in IMR.

28.8.8 Interrupt Mask Register

Register Name: IMR

Access Type: Read-only

Offset: 0x1C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	RES

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

A bit in this register is cleared when the corresponding bit in IDR is written to one.

A bit in this register is set when the corresponding bit in IER is written to one.

28.8.9 Interrupt Status Register

Register Name: ISR

Access Type: Read-only

Offset: 0x20

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	RES

- **RES: Refresh Error Status**
  This bit is set when a refresh error is detected.
  This bit is cleared when the register is read.

28.8.10 Memory Device Register

Register Name: MDR

Access Type: Read/Write

Offset: 0x24

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	MD	

- **MD: Memory Device Type**

MD	Device Type
0	SDRAM
1	Low power SDRAM
Other	Reserved

29. Error Corrected Code (ECC) Controller

Rev: 1.0.0.0

29.1 Features

- **Hardware Error Corrected Code (ECC) Generation**
  - **Detection and Correction by Software**
- **Supports NAND Flash and SmartMedia™ Devices with 8- or 16-bit Data Path.**
- **Supports NAND Flash/SmartMedia with Page Sizes of 528, 1056, 2112 and 4224 Bytes, Specified by Software**

29.2 Description

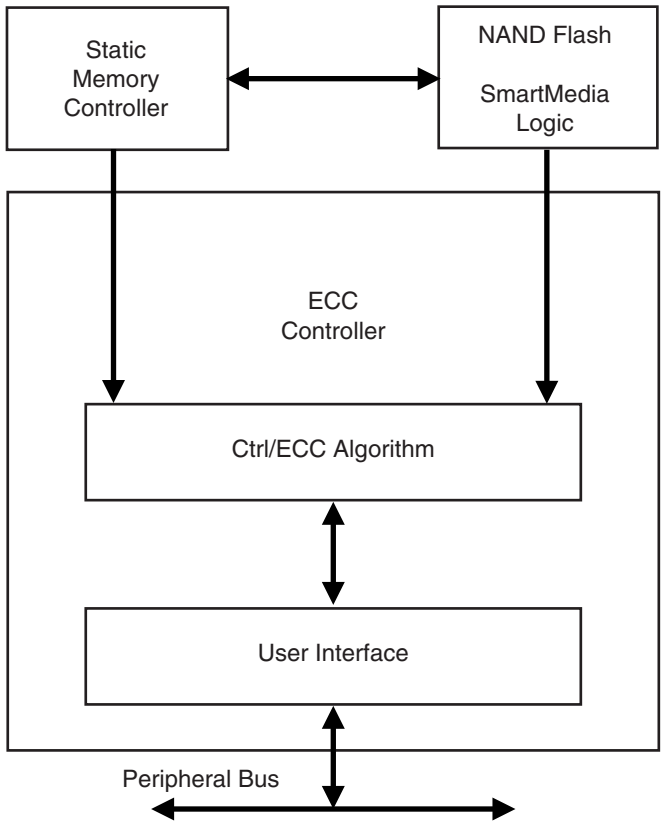
NAND Flash/SmartMedia devices contain by default invalid blocks which have one or more invalid bits. Over the NAND Flash/SmartMedia lifetime, additional invalid blocks may occur which can be detected/corrected by ECC code.

The ECC Controller is a mechanism that encodes data in a manner that makes possible the identification and correction of certain errors in data. The ECC controller is capable of single bit error correction and 2-bit random detection. When NAND Flash/SmartMedia have more than 2 bits of errors, the data cannot be corrected.

The ECC user interface is accesible through the peripheral bus.

29.3 Block Diagram

Figure 29-1. Block Diagram



29.4 Functional Description

A page in NAND Flash and SmartMedia memories contains an area for main data and an additional area used for redundancy (ECC). The page is organized in 8-bit or 16-bit words. The page size corresponds to the number of words in the main data plus the number of words in the extra area used for redundancy.

The only configuration required for ECC is the NAND Flash or the SmartMedia page size (528/1056/2112/4224). Page size is configured setting the PAGESIZE field in the ECC Mode Register (MR).

ECC is automatically computed as soon as a read (00h)/write (80h) command to the NAND Flash or the SmartMedia is detected. Read and write access must start at a page boundary.

ECC is computed as soon as the counter reaches the page size. Values in the ECC Parity Register (PR) and ECC NParity Register (NPR) are then valid and locked until a new start condition (read/write command followed by five access address cycles).

29.4.1 Write Access

Once the flash memory page is written, the computed ECC code is available in the ECC Parity Error (PR) and ECC_NParity Error (NPR) registers. The ECC code value must be written by the software application at the end of the page, in the extra area used for redundancy.

29.4.2 Read Access

After reading main data in the page area, the application can perform read access to the extra area used for redundancy. Error detection is automatically performed by the ECC controller. The application can check the ECC Status Register (SR) for any detected errors.

It is up to the application to correct any detected error. ECC computation can detect four different circumstances:

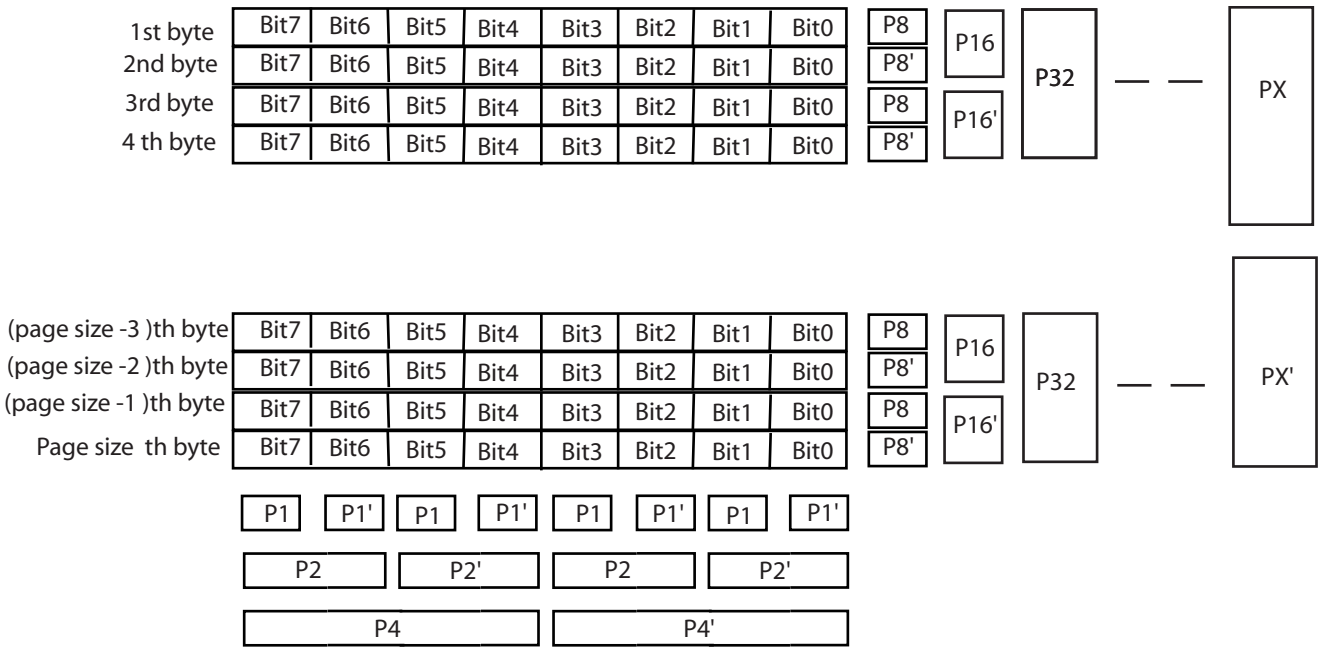
- No error: XOR between the ECC computation and the ECC code stored at the end of the NAND Flash or SmartMedia page is equal to 0. No error flags in the ECC Status Register (SR).
- Recoverable error: Only the RECERR flag in the ECC Status register (SR) is set. The corrupted word offset in the read page is defined by the WORDADDR field in the ECC Parity Register (PR). The corrupted bit position in the concerned word is defined in the BITADDR field in the ECC Parity Register (PR).
- ECC error: The ECCERR flag in the ECC Status Register is set. An error has been detected in the ECC code stored in the Flash memory. The position of the corrupted bit can be found by the application performing an XOR between the Parity and the NParity contained in the ECC code stored in the flash memory.
- Non correctable error: The MULERR flag in the ECC Status Register is set. Several unrecoverable errors have been detected in the flash memory page.

ECC Status Register, ECC Parity Register and ECC NParity Register are cleared when a read/write command is detected or a software register is enabled.

For single bit Error Correction and double bit Error Detection (SEC-DED) hsiao code is used. 32-bit ECC is generated in order to perform one bit correction per 512/1024/2048/4096 8- or 16-bit

words. Of the 32 ECC bits, 26 bits are for line parity and 6 bits are for column parity. They are generated according to the schemes shown in Figure 29-2 and Figure 29-3.

Figure 29-2. Parity Generation for 512/1024/2048/4096 8-bit Words1



Page size = 512 Px = 2048
Page size = 1024 Px = 4096
Page size = 2048 Px = 8192
Page size = 4096 Px = 16384

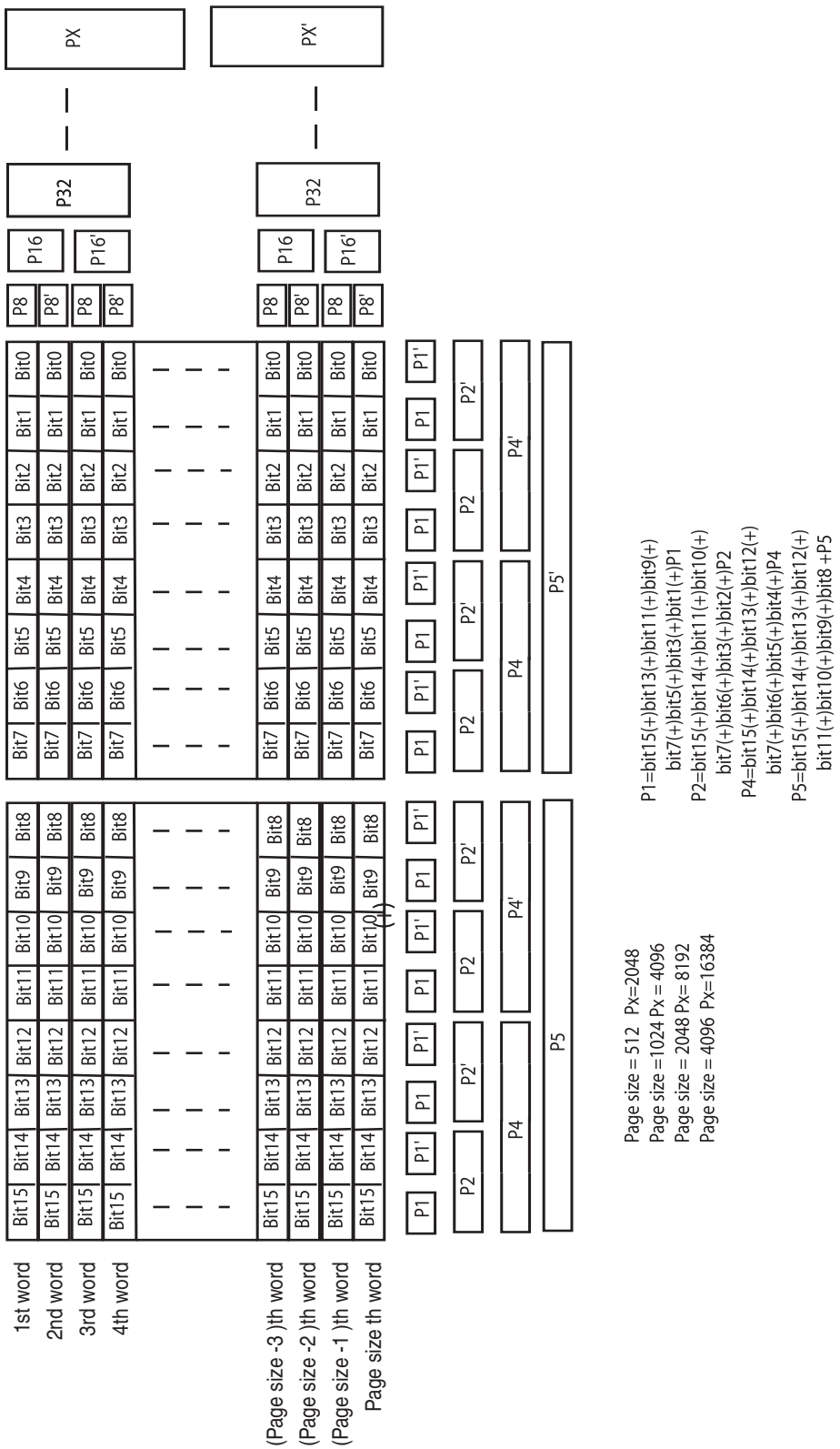
P1=bit7(+)bit5(+)bit3(+)bit1(+)P1
P2=bit7(+)bit6(+)bit3(+)bit2(+)P2
P4=bit7(+)bit6(+)bit5(+)bit4(+)P4
P1'=bit6(+)bit4(+)bit2(+)bit0(+)P1'
P2'=bit5(+)bit4(+)bit1(+)bit0(+)P2'
P4'=bit7(+)bit6(+)bit5(+)bit4(+)P4'

To calculate P8' to PX' and P8 to PX, apply the algorithm that follows.

Page size = 2^n

```
for i =0 to n
begin
 for (j = 0 to page_size_byte)
 begin
  if(j[i] ==1)
   P[2^(i+3)]=bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
              bit2(+)bit1(+)bit0(+)P[2^(i+3)]
  else
   P[2^(i+3)]'=bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
               bit2(+)bit1(+)bit0(+)P[2^(i+3)]'
  end
end
```

Figure 29-3. Parity Generation for 512/1024/2048/4096 16-bit Words



To calculate P8' to PX' and P8 to PX, apply the algorithm that follows.

```
Page size = 2^n

   for i =0 to n
   begin
    for (j = 0 to page_size_word)
    begin
     if(j[i] ==1)
      P[2^(i+3)]= bit15(+)bit14(+)bit13(+)bit12(+)
                  bit11(+)bit10(+)bit9(+)bit8(+)
                  bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
                  bit2(+)bit1(+)bit0(+)P[2^(n+3)]
     else
      P[2^(i+3)]'=bit15(+)bit14(+)bit13(+)bit12(+)
                  bit11(+)bit10(+)bit9(+)bit8(+)
                  bit7(+)bit6(+)bit5(+)bit4(+)bit3(+)
                  bit2(+)bit1(+)bit0(+)P[2^(i+3)]'
     end
   end
```

29.5 ECC User Interface

Table 29-1. ECC Register Mapping

Offset	Register	Register Name	Access	Reset
0x00	ECC Control Register	CR	Write-only	0x0
0x04	ECC Mode Register	MR	Read/Write	0x0
0x8	ECC Status Register	SR	Read-only	0x0
0x0C	ECC Parity Register	PR	Read-only	0x0
0x10	ECC NParity Register	NPR	Read-only	0x0
0x14-0xF8	Reserved	–	–	–
0x14 - 0xFC	Reserved	–	–	–

29.5.1 ECC Control Register

Name: CR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	RST

- **RST: RESET Parity**

Provides reset to current ECC by software.

0: No effect

1: Reset sECC Parity and ECC NParity register

29.5.2 ECC Mode Register

Register Name: MR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	PAGESIZE	

- **PAGESIZE: Page Size**

This field defines the page size of the NAND Flash device.

Page Size	Description
00	528 words
01	1056 words
10	2112 words
11	4224 words

A word has a value of 8 bits or 16 bits, depending on the NAND Flash or Smartmedia memory organization.

29.5.3 ECC Status Register

Register Name: SR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	MULERR	ECCERR	RECERR

- **RECERR: Recoverable Error**

0: No Errors Detected

1: Errors Detected. If MULERR is 0, a single correctable error was detected. Otherwise multiple uncorrected errors were detected

- **ECCERR: ECC Error**

0: No Errors Detected

1: A single bit error occurred in the ECC bytes.

Read both ECC Parity and ECC Parityn register, the error occurred at the location which contains a 1 in the least significant 16 bits.

- **MULERR: Multiple Error**

0: No Multiple Errors Detected

1: Multiple Errors Detected

29.5.4 ECC Parity Register

Register Name: PR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
WORDADDR							
7	6	5	4	3	2	1	0
WORDADDR				BITADDR			

During a page write, the value of the entire register must be written in the extra area used for redundancy (for a 512-byte page size: address 512-513)

- **BITADDR**

During a page read, this value contains the corrupted bit offset where an error occurred, if a single error was detected. If multiple errors were detected, this value is meaningless.

- **WORDADDR**

During a page read, this value contains the word address (8-bit or 16-bit word depending on the memory plane organization) where an error occurred, if a single error was detected. If multiple errors were detected, this value is meaningless.

29.5.5 ECC NParity Register

Register Name: NPR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
NPARITY							
7	6	5	4	3	2	1	0
NPARITY							

- **NPARITY:**

During a write, the value of this register must be written in the extra area used for redundancy (for a 512-byte page size: address 514-515)

30. MultiMedia Card Interface (MCI)

Rev: 2.0.0.3

30.1 Features

- **Compatible with MultiMedia Card Specification Version 2.2**
- **Compatible with SD Memory Card Specification Version 1.0**
- **Compatible with MultiMedia Card Specification Version 3.31**
- **Compatible with SDIO Specification Version 1.1**
- **Cards Clock Rate Up to Master Clock Divided by 2**
- **Embedded Power Management to Slow Down Clock Rate When Not Used**
- **Supports 2 Slots**
  - **Each Slot for either a MultiMediaCard Bus (Up to 30 Cards) or an SD Memory Card**
- **Support for Stream, Block and Multi-block Data Read and Write**
- **Supports Connection to DMA Controller**
  - **Minimizes Processor Intervention for Large Buffer Transfers**

30.2 Overview

The MCI includes a command register, response registers, data registers, timeout counters and error detection logic that automatically handle the transmission of commands and, when required, the reception of the associated responses and data with a limited processor overhead.

The MCI supports stream, block and multi-block data read and write, and is compatible with a DMA Controller, minimizing processor intervention for large buffer transfers.

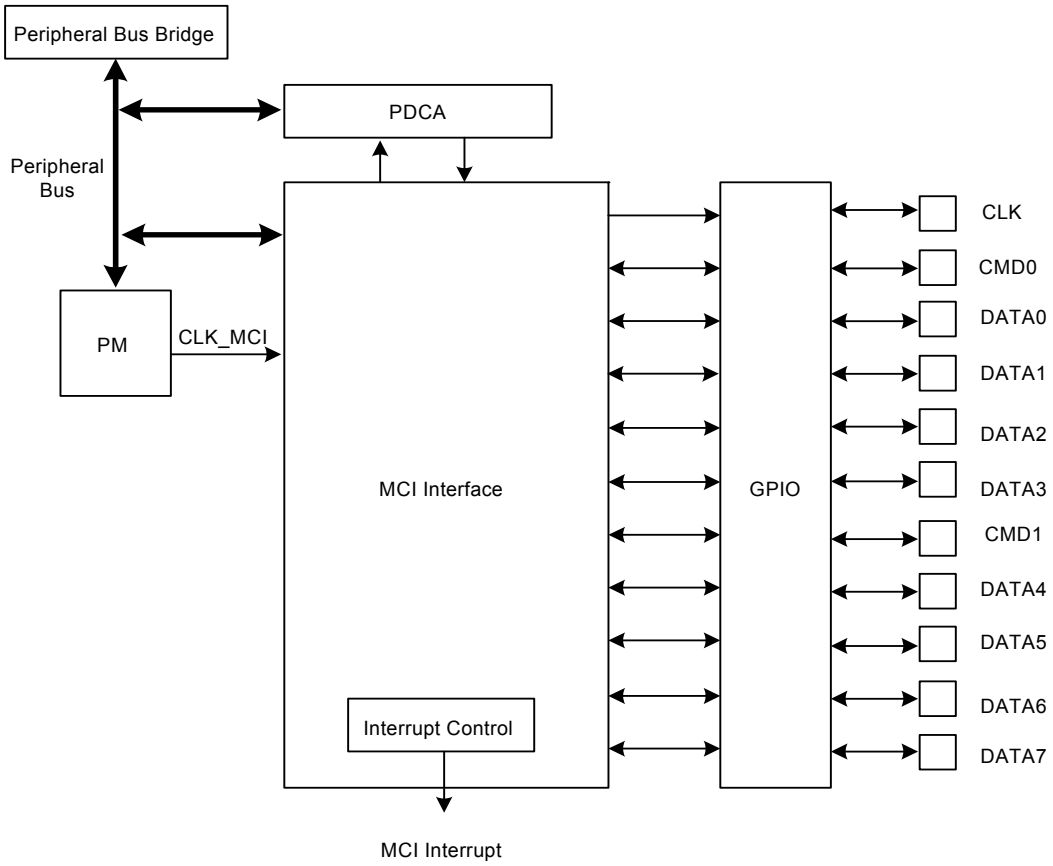
The MCI operates at a rate of up to Master Clock divided by 2 and supports the interfacing of 2 Slots . Each slot may be used to interface with a MultiMedia Card bus (up to 30 Cards) or with a SD Memory Card. Only one slot can be selected at a time (slots are multiplexed). A bit field in the SD Card Register performs this selection.

The SD Memory Card communication is based on a 9-pin interface (clock, command, four data and three power lines) and the MultiMediaCard on a 7-pin interface (clock, command, one data, three power lines and one reserved for future use).

The SD Memory Card interface also supports MultiMedia Card operations. The main differences between SD and MultiMedia Cards are the initialization process and the bus topology.

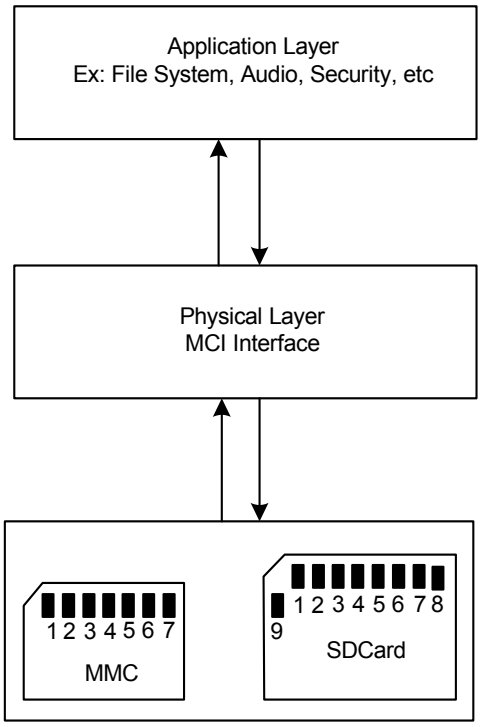
30.3 Block Diagram

Figure 30-1. Block Diagram



30.4 Application Block Diagram

Figure 30-2. Application Block Diagram



30.5 I/O Lines Description

Table 30-1. I/O Lines Description

Pin Name	Pin Description	Type[1]	Comments
CMD[1:0]	Command/response	I/O/PP/OD	CMD of an MMC or SD Card
CLK	Clock	I/O	CLK of an MMC or SD Card
DATA[3..0]	Data 0..3 of Slot A	I/O/PP	DAT0 of an MMC DAT[0..3] of an SD Card
DATA[7...4]	Data 0..3 of Slot B	I/O/PP	DAT0 of an MMC DAT[0..3] of an SD Card

Note: 1. I: Input, O: Output, PP: Push/Pull, OD: Open Drain.

30.6 Product Dependencies

30.6.1 GPIO

The pins used for interfacing the MultiMedia Cards or SD Cards may be multiplexed with GPIO lines. The programmer must first program the GPIO controller to assign the peripheral functions to MCI pins.

30.6.2 Power Manager

The MCI may receive a clock from the Power Manager (PM), so the programmer must first configure the PM to enable the MCI clock(CLK_MCI).

30.6.3 Interrupt Controller

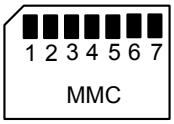
The MCI interface has an interrupt line connected to the Interrupt Controller (INTC).

Handling the MCI interrupt requires programming the INTC before configuring the MCI.

30.7 Functional Description

30.7.1 Bus Topology

Figure 30-3. MultiMedia Memory Card Bus Topology



The MultiMedia Card communication is based on a 7-pin serial bus interface. It has three communication lines and four supply lines.

Table 30-2. Bus Topology

Pin Number	Name	Type[1]	Description	MCI Pin Name (Slot x)
1	RSV	NC	Not connected	
2	CMD	I/O/PP/OD	Command/response	CMDx
3	VSS1	S	Supply voltage ground	VSS
4	VDD	S	Supply voltage	VDD
5	CLK	I/O	Clock	CLK
6	VSS2	S	Supply voltage ground	VSS
7	DAT[0]	I/O/PP	Data 0	DATAx0

Note: 1. I: Input, O: Output, PP: Push/Pull, OD: Open Drain.

Figure 30-4. MMC Bus Connections (One Slot)

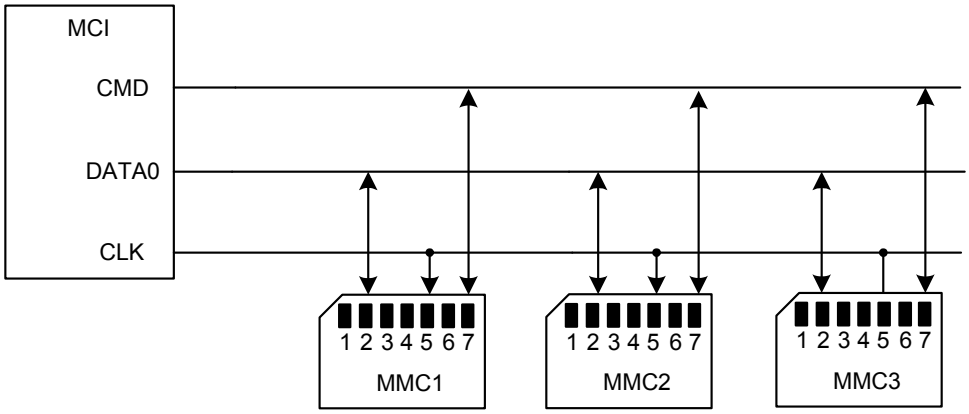
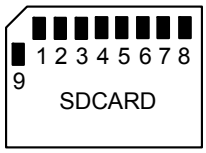


Figure 30-5. SD Memory Card Bus Topology



The SD Memory Card bus includes the signals listed in Table 30-3 on page 577.

Table 30-3. SD Memory Card Bus Signals

Pin Number	Name	Type[1]	Description	MCI Pin Name (Slot x)
1	CD/DAT[3]	I/O/PP	Card detect/ Data line Bit 3	DATAx3
2	CMD	PP	Command/response	CMDx
3	VSS1	S	Supply voltage ground	VSS
4	VDD	S	Supply voltage	VDD
5	CLK	I/O	Clock	CLK
6	VSS2	S	Supply voltage ground	VSS
7	DAT[0]	I/O/PP	Data line Bit 0	DATAx0
8	DAT[1]	I/O/PP	Data line Bit 1 or Interrupt	DATAx1
9	DAT[2]	I/O/PP	Data line Bit 2	DATAx2

Note: 1. I: input, O: output, PP: Push Pull, OD: Open Drain

Figure 30-6. SD Card Bus Connections with Two Slots

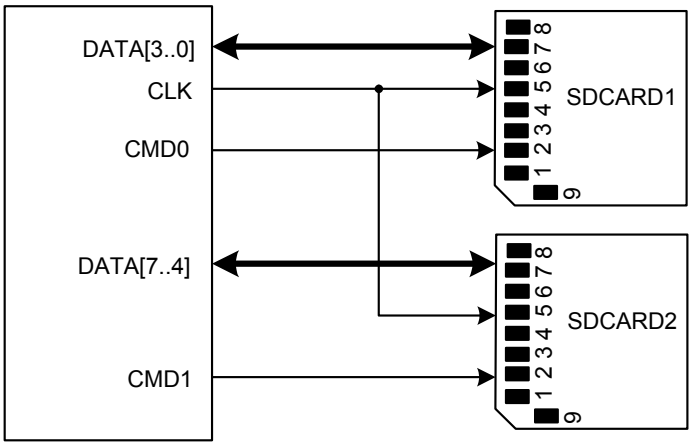
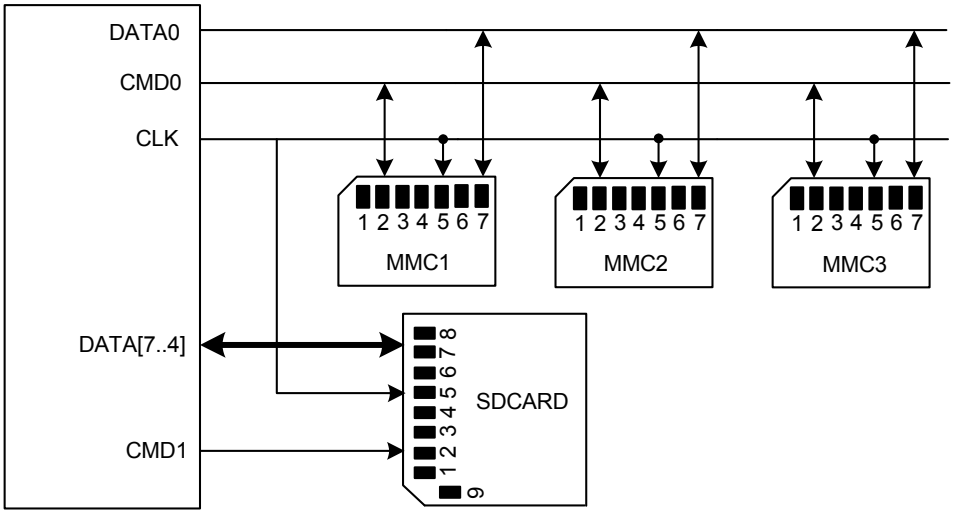


Figure 30-7. Mixing MultiMedia and SD Memory Cards with Two Slots



When the MCI is configured to operate with SD memory cards, the width of the data bus can be selected in the SDCR register. Clearing the SDCBUS bit in this register means that the width is one bit; setting it means that the width is four bits. In the case of multimedia cards, only the data line 0 is used. The other data lines can be used as independent GPIOs.

30.7.2 MultiMedia Card Operations

After a power-on reset, the cards are initialized by a special message-based MultiMedia Card bus protocol. Each message is represented by one of the following tokens:

- Command: A command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: A response is a token which is sent from an addressed card or (synchronously) from all connected cards to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: Data can be transferred from the card to the host or vice versa. Data is transferred via the data line.

Card addressing is implemented using a session address assigned during the initialization phase by the bus controller to all currently connected cards. Their unique CID number identifies individual cards.

The structure of commands, responses and data blocks is described in the MultiMedia-Card System Specification. See also Table 30-4 on page 580.

MultiMediaCard bus data transfers are composed of these tokens.

There are different types of operations. Addressed operations always contain a command and a response token. In addition, some operations have a data token; the others transfer their information directly within the command or response structure. In this case, no data token is present in an operation. The bits on the DAT and the CMD lines are transferred synchronous to the MCI Clock.

Two types of data transfer commands are defined:

- Sequential commands: These commands initiate a continuous data stream. They are terminated only when a stop command follows on the CMD line. This mode reduces the command overhead to an absolute minimum.
- Block-oriented commands: These commands send a data block succeeded by CRC bits.

Both read and write operations allow either single or multiple block transmission. A multiple block transmission is terminated when a stop command follows on the CMD line similarly to the sequential read or when a multiple block transmission has a predefined block count (See ”Data Transfer Operation” on page 581.).

The MCI provides a set of registers to perform the entire range of MultiMedia Card operations.

30.7.2.1 Command - Response Operation

After reset, the MCI is disabled and becomes valid after setting the MCIEN bit in the Control Register(CR).

The two bits RDPROOF and WRPROOF in the Mode Register (MR) allow stopping the MCI Clock during read or write access if the internal FIFO is full. This will guarantee data integrity, not bandwidth.

The command and the response of the card are clocked out with the rising edge of the MCI Clock.

All the timings for MultiMedia Card are defined in the MultiMediaCard System Specification.

The two bus modes (open drain and push/pull) needed to process all the operations are defined in the MCI command register. The CMDR allows a command to be carried out.

For example, to perform an ALL_SEND_CID command:

	Host Command					N_{ID} Cycles					CID			
CMD	S	T	Content	CRC	E	Z	******	Z	S	T	Content	Z	Z	Z

The command ALL_SEND_CID and the fields and values for the CMDR Control Register are described in Table 30-4 and Table 30-5.

Table 30-4. ALL_SEND_CID Command Description

CMD Index	Type	Argument	Resp	Abbreviation	Command Description
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks all cards to send their CID numbers on the CMD line

Note: bcr means broadcast command with response.

Table 30-5. Fields and Values for CMDR Command Register

Field	Value
CMDNB (command number)	2 (CMD2)
RSPTYP (response type)	2 (R2: 136 bits response)
SPCMD (special command)	0 (not a special command)
OPCMD (open drain command)	1
MAXLAT (max latency for command to response)	0 (NID cycles ==> 5 cycles)
TRCMD (transfer command)	0 (No transfer)
TRDIR (transfer direction)	X (available only in transfer command)
TRTYP (transfer type)	X (available only in transfer command)

The ARGR contains the argument field of the command.

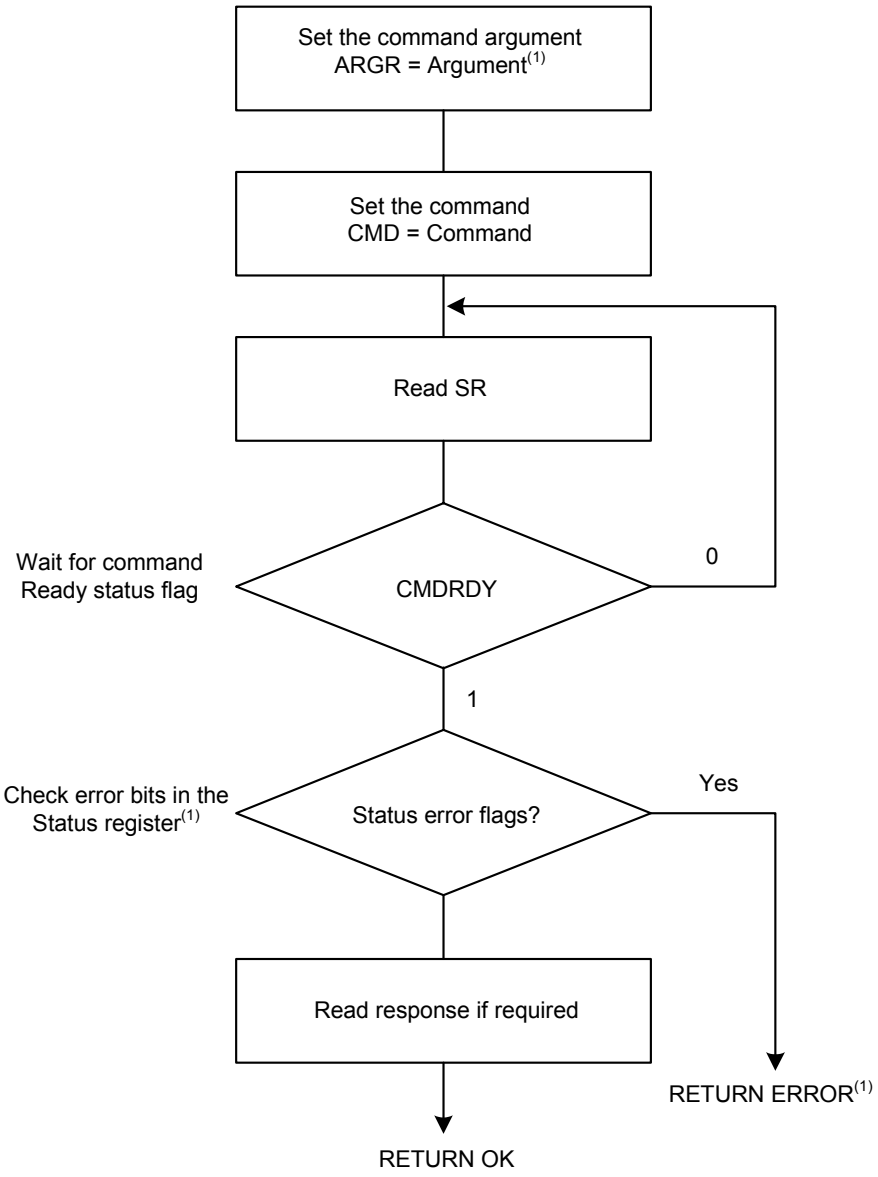
To send a command, the user must perform the following steps:

- Fill the argument register (ARGR) with the command argument.
- Set the command register (CMDR) (see Table 30-5).

The command is sent immediately after writing the command register. The status bit CMDRDY in the Status Register (SR) is asserted when the command is completed. If the command requires a response, it can be read in the Response Register (RSPR). The response size can be from 48 bits up to 136 bits depending on the command. The MCI embeds an error detection to prevent any corrupted data during the transfer.

The following flowchart shows how to send a command to the card and read the response if needed. In this example, the status register bits are polled but setting the appropriate bits in the Interrupt Enable Register (IER) allows using an interrupt method.

Figure 30-8. Command/Response Functional Flow Diagram



Note: 1. If the command is SEND_OP_COND, the CRC error flag is always present (refer to R3 response in the MultiMedia Card specification).

30.7.2.2 Data Transfer Operation

The MultiMedia Card allows several read/write operations (single block, multiple blocks, stream, etc). These kind of transfers can be selected setting the Transfer Type (TRTYP) field in the I Command Register (CMDR).

These operations can be done using the a DMA Controller.

In all cases, the block length (BLKLEN field) must be defined either in the MR register, or in the Block Register(BLKR). This field determines the size of the data block.

Enabling PDC Force Byte Transfer (PDCFBYTE in the MR) allows the PDC to manage with internal byte transfers, so that transfers of blocks with a size different from modulo 4 can be sup-

ported. When PDC Force Byte Transfer is disabled, the PDC type of transfers are in words, otherwise the type of transfers are in bytes.

Consequent to MMC Specification 3.1, two types of multiple block read (or write) transactions are defined (the host can use either one at any time):

- Open-ended/Infinite Multiple block read (or write):

  The number of blocks for the read (or write) multiple block operation is not defined. The card will continuously transfer (or program) data blocks until a stop transmission command is received.

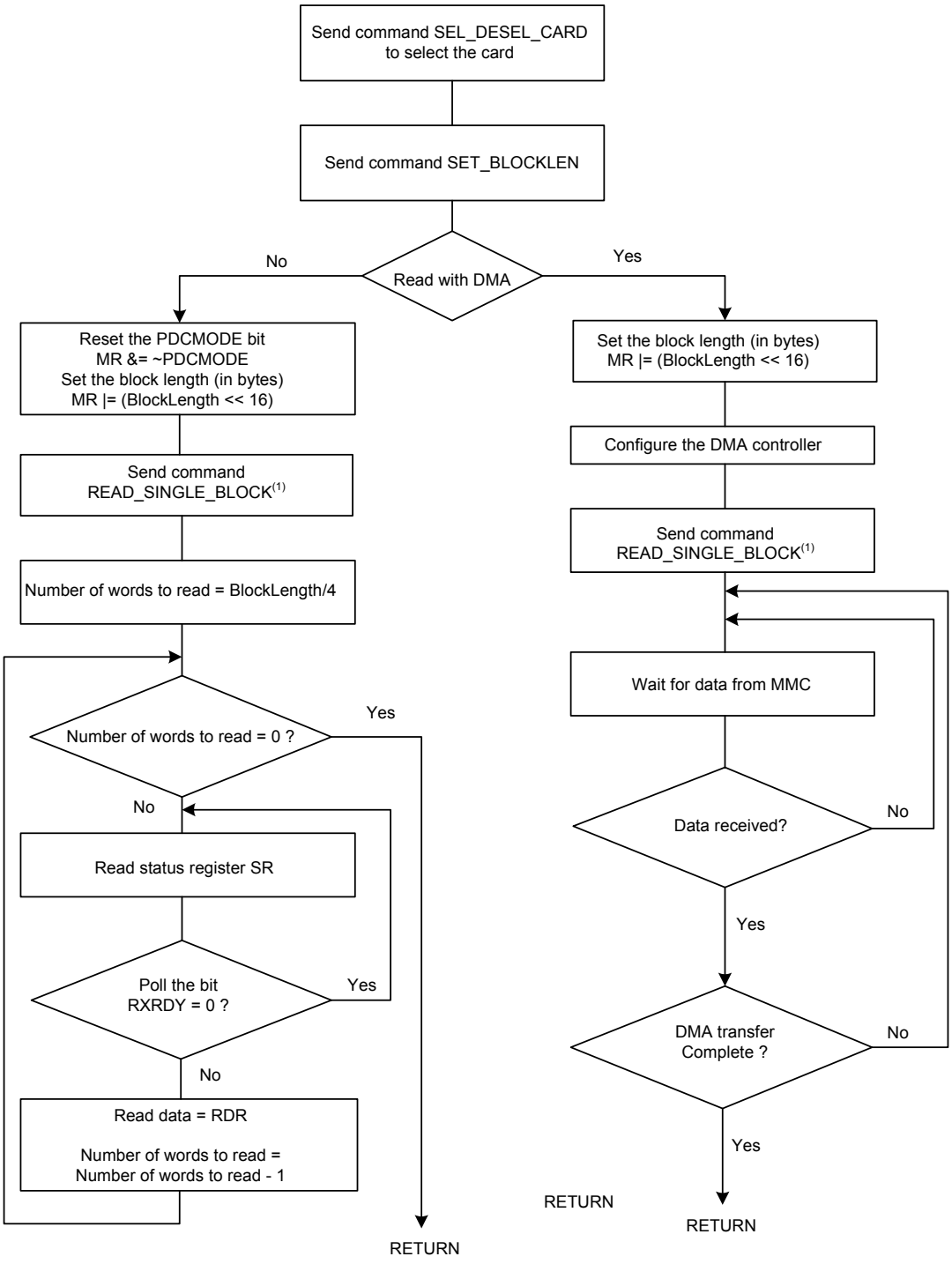
- Multiple block read (or write) with pre-defined block count (since version 3.1 and higher):

  The card will transfer (or program) the requested number of data blocks and terminate the transaction. The stop command is not required at the end of this type of multiple block read (or write), unless terminated with an error. In order to start a multiple block read (or write) with pre-defined block count, the host must correctly program the Block Register (BLKR). Otherwise the card will start an open-ended multiple block read. The BCNT field of the Block Register defines the number of blocks to transfer (from 1 to 65535 blocks). Programming the value 0 in the BCNT field corresponds to an infinite block transfer.

30.7.2.3 Read Operation

The following flowchart shows how to read a single block with or without use of DMA facilities. In this example, a polling method is used to wait for the end of read. Similarly, the user can configure the IER regsiter to trigger an interrupt at the end of read.

Figure 30-9. Read Functional Flow Diagram



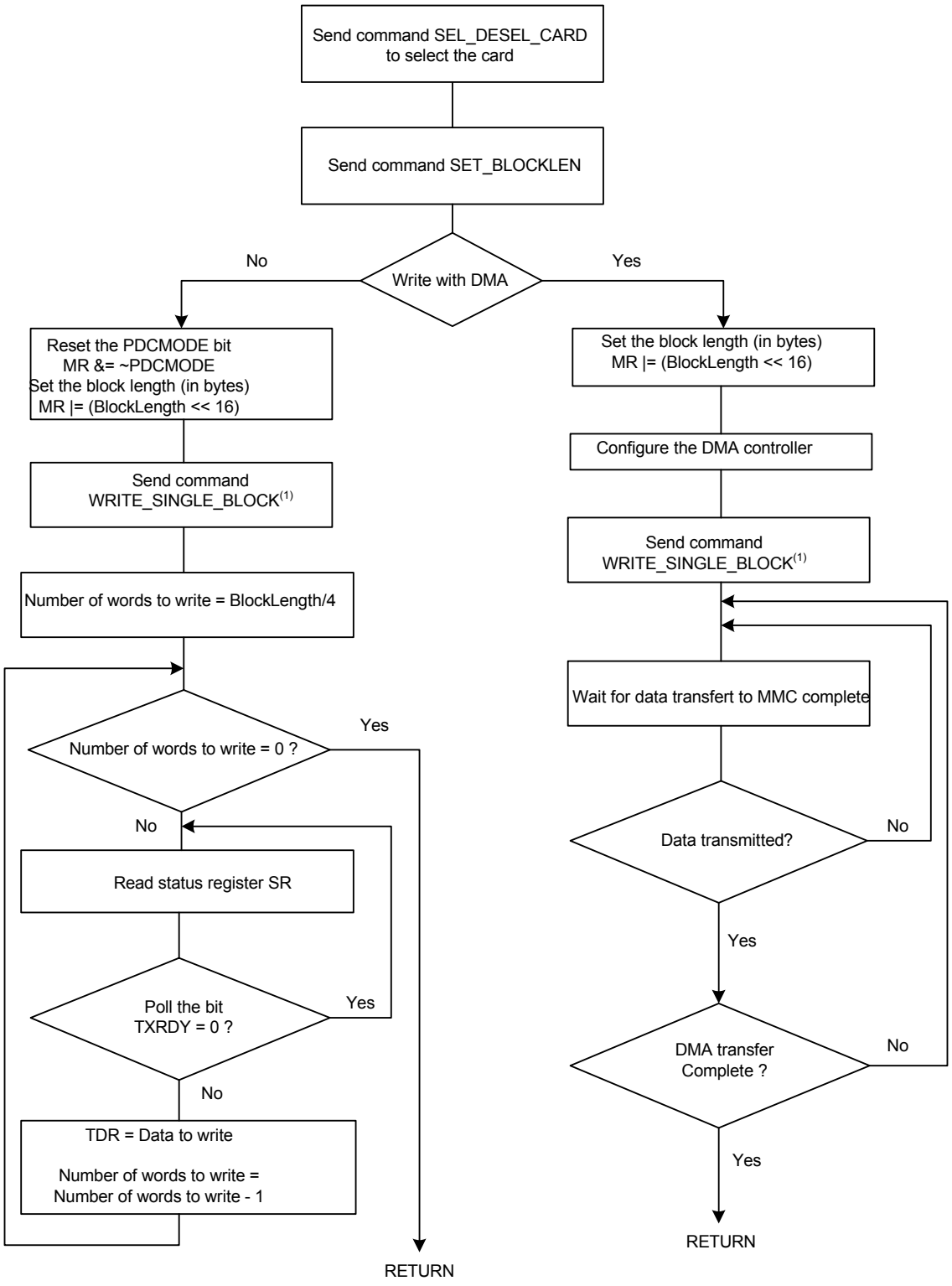
Note: 1. This command is supposed to have been correctly sent (see Figure 30-8).

30.7.2.4 Write Operation

In write operation, the MR register is used to define the padding value when writing non-multiple block size. If the bit DMAPADV is 0, then 0x00 value is used when padding data, otherwise 0xFF is used.

The following flowchart shows how to write a single block with or without use of DMA facilities. Polling or interrupt method can be used to wait for the end of write according to the contents of the Interrupt Mask Register (IMR).

Figure 30-10. Write Functional Flow Diagram



Note: 1. It is assumed that this command has been correctly sent (see Figure 30-8).

30.7.3 SD Card Operations

The MultiMedia Card Interface allows processing of SD Memory (Secure Digital Memory Card) and SDIO (SD Input Output) Card commands.

SD/SDIO cards are based on the MultiMedia Card (MMC) format, but are physically slightly thicker and feature higher data transfer rates, a lock switch on the side to prevent accidental overwriting and security features. The physical form factor, pin assignment and data transfer protocol are forward-compatible with the MMC with some additions. SD slots can actually be used for more than flash memory cards. Devices that support SDIO can use small devices designed for the SD form factor, such as GPS receivers, Wi-Fi or Bluetooth adapters, modems, barcode readers, IrDA adapters, FM radio tuners, RFID readers, digital cameras and more.

SD/SDIO is covered by numerous patents and trademarks, and licensing is only available through the Secure Digital Card Association.

The SD/SDIO Card communication is based on a 9-pin interface (Clock, Command, 4 x Data and 3 x Power lines). The communication protocol is defined as a part of this specification. The main difference between the SD/SDIO Card and the MMC is the initialization process.

The SD/SDIO Card Register (SDCR) allows selection of the Card Slot and the data bus width.

The SD/SDIO Card bus allows dynamic configuration of the number of data lines. After power up, by default, the SD/SDIO Card uses only DAT0 for data transfer. After initialization, the host can change the bus width (number of active data lines).

30.7.3.1 SDIO Data Transfer Type

SDIO cards may transfer data in either a multi-byte (1 to 512 bytes) or an optional block format (1 to 511 blocks), while the SD memory cards are fixed in the block transfer mode. The TRTYP field in the Command Register (CMDR) allows to choose between SDIO Byte or SDIO Block transfer.

The number of bytes/blocks to transfer is set through the BCNT field in the Block Register (BLKR). In SDIO Block mode, the field BLKLEN must be set to the data block size while this field is not used in SDIO Byte mode.

An SDIO Card can have multiple I/O or combined I/O and memory (called Combo Card). Within a multi-function SDIO or a Combo card, there are multiple devices (I/O and memory) that share access to the SD bus. In order to allow the sharing of access to the host among multiple devices, SDIO and combo cards can implement the optional concept of suspend/resume (Refer to the SDIO Specification for more details). To send a suspend or a resume command, the host must set the SDIO Special Command field (IOSPCMD) in the Command Register.

30.7.3.2 SDIO Interrupts

Each function within an SDIO or Combo card may implement interrupts (Refer to the SDIO Specification for more details). In order to allow the SDIO card to interrupt the host, an interrupt function is added to a pin on the DAT[1] line to signal the card's interrupt to the host. An SDIO interrupt on each slot can be enabled through the MCI Interrupt Enable Register. The SDIO interrupt is sampled regardless of the currently selected slot.

30.8 User Interface

Table 30-6. Register Mapping

Offset	Register	Register Name	Read/Write	Reset
0x00	Control Register	CR	Write	–
0x04	Mode Register	MR	Read/write	0x0
0x08	Data Timeout Register	DTOR	Read/write	0x0
0x0C	SD/SDIO Card Register	SDCR	Read/write	0x0
0x10	Argument Register	ARGR	Read/write	0x0
0x14	Command Register	CMDR	Write	–
0x18	Block Register	BLKR	Read/write	–
0x1C	Reserved	–	–	–
0x20	Response Register(1)	RSPR	Read	0x0
0x24	Response Register(1)	RSPR	Read	0x0
0x28	Response Register(1)	RSPR	Read	0x0
0x2C	Response Register(1)	RSPR	Read	0x0
0x30	Receive Data Register	RDR	Read	0x0
0x34	Transmit Data Register	TDR	Write	–
0x38 - 0x3C	Reserved	–	–	–
0x40	Status Register	SR	Read	0x25
0x44	Interrupt Enable Register	IER	Write	–
0x48	Interrupt Disable Register	IDR	Write	–
0x4C	Interrupt Mask Register	IMR	Read	0x0
0x50-0xF8	Reserved	–	–	–
0xFC	Version Register	VERSION	Read-only	–
0x50-0xFC	Reserved	–	–	–

Note: 1. The response register can be read by N accesses at the same RSPR or at consecutive addresses (0x20 to 0x2C). N depends on the size of the response.

30.8.1 Control Register

Name: CR

Access Type: Write-only

Offset: 0x00

Reset Value: –

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	–		MCIDIS	MCIEN

- **SWRST: Software Reset**

0 = No effect.

1 = Resets the MCI. A software triggered hardware reset of the MCI interface is performed.

- **MCIDIS: Multi-Media Interface Disable**

0 = No effect.

1 = Disables the Multi-Media Interface.

- **MCIEN: Multi-Media Interface Enable**

0 = No effect.

1 = Enables the Multi-Media Interface if MCDIS is 0.

30.8.2 Mode Register

Name: MR

Access Type: Read/write

Offset: 0x04

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
BLKLEN							
23	22	21	20	19	18	17	16
BLKLEN							
15	14	13	12	11	10	9	8
-	DMAPADV	PDCFBYTE	WRPROOF	RDPROOF			
7	6	5	4	3	2	1	0
CLKDIV							

- **BLKLEN: Data Block Length**

This field determines the size of the data block.

This field is also accessible in the MCI Block Register (BLKR).

Bits 16 and 17 must be written to 0 if PDCFBYTE is disabled.

Note: In SDIO Byte mode, BLKLEN field is not used.

- **DMAPADV: DMA Padding Value**

0 = 0x00 value is used when padding data in write transfer.

1 = 0xFF value is used when padding data in write transfer.

- **PDCFBYTE: PDC Force Byte Transfer**

Enabling PDC Force Byte Transfer allows the PDC to manage with internal byte transfers, so that transfer of blocks with a size different from modulo 4 can be supported. This applies to both PDC and non-PDC transfers.

Warning: BLKLEN value depends on PDCFBYTE.

0 = Disables PDC Force Byte Transfer. PDC type of transfer are in words.

1 = Enables PDC Force Byte Transfer. PDC type of transfer are in bytes.

- **WRPROOF Write Proof Enable**

Enabling Write Proof allows to stop the MCI Clock during write access if the internal FIFO is full. This will guarantee data integrity, not bandwidth.

0 = Disables Write Proof.

1 = Enables Write Proof.

- **RDPROOF Read Proof Enable**

Enabling Read Proof allows to stop the MCI Clock during read access if the internal FIFO is full. This will guarantee data integrity, not bandwidth.

0 = Disables Read Proof.

1 = Enables Read Proof.

- **CLKDIV: Clock Divider**

Multimedia Card Interface clock (MCCK) is Master Clock (CLK_MCI) divided by (2*(CLKDIV+1)).

30.8.3 Data Timeout Register

Name: DTOR

Access Type: Read/write

Offset: 0x08

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	DTOMUL			DTOCYC			

- **DTOMUL: Data Timeout Multiplier**

These fields determine the maximum number of Master Clock cycles that the MCI waits between two data block transfers. It equals (DTOCYC x Multiplier).

Multiplier is defined by DTOMUL as shown in the following table:

DTOMUL			Multiplier
0	0	0	1
0	0	1	16
0	1	0	128
0	1	1	256
1	0	0	1024
1	0	1	4096
1	1	0	65536
1	1	1	1048576

If the data time-out set by DTOCYC and DTOMUL has been exceeded, the Data Time-out Error flag (DTOE) in the MCI Status Register (SR) raises.

- **DTOCYC: Data Timeout Cycle Number**

30.8.4 SD Card/SDIO Register

Name: SDCR

Access Type: Read/write

Offset: 0x0C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SDCBUS	–	–	–	–	–	SDCSEL	

- **SDCBUS: SD Card/SDIO Bus Width**

0 = 1-bit data bus

1 = 4-bit data bus

- **SDCSEL: SD Card Selector**

0 = SDCARD Slot A selected.

1= SDCARD Slot B selected.

30.8.5 Argument Register

Name: ARGR

Access Type: Read/write

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
ARG							

23	22	21	20	19	18	17	16
ARG							

15	14	13	12	11	10	9	8
ARG							

7	6	5	4	3	2	1	0
ARG							

- **ARG: Command Argument**

30.8.6 Command Register

Name: CMDR

Access Type: Write-only

Offset: 0x14

Reset Value: –

31	30	29	28	27	26	25	24
–	–	–	–	–	–	IOSPCMD	
23	22	21	20	19	18	17	16
–	–	TRTYP			TRDIR	TRCMD	
15	14	13	12	11	10	9	8
–	–	–	MAXLAT	OPDCMD	SPCMD		
7	6	5	4	3	2	1	0
RSPTYP		CMDNB					

This register is write-protected while CMDRDY is 0 in SR. If an Interrupt command is sent, this register is only writeable by an interrupt response (field SPCMD). This means that the current command execution cannot be interrupted or modified.

- **IOSPCMD: SDIO Special Command**

IOSPCMD		SDIO Special Command Type
0	0	Not a SDIO Special Command
0	1	SDIO Suspend Command
1	0	SDIO Resume Command
1	1	Reserved

- **TRTYP: Transfer Type**

TRTYP			Transfer Type
0	0	0	MMC/SDCard Single Block
0	0	1	MMC/SDCard Multiple Block
0	1	0	MMC Stream
0	1	1	Reserved
1	0	0	SDIO Byte
1	0	1	SDIO Block
1	1	0	Reserved
1	1	1	Reserved

- **TRDIR: Transfer Direction**

0 = Write

1 = Read

- **TRCMD: Transfer Command**

TRCMD		Transfer Type
0	0	No data transfer
0	1	Start data transfer
1	0	Stop data transfer
1	1	Reserved

- **MAXLAT: Max Latency for Command to Response**

0 = 5-cycle max latency

1 = 64-cycle max latency

- **OPDCMD: Open Drain Command**

0 = Push pull command

1 = Open drain command

- **SPCMD: Special Command**

SPCMD			Command
0	0	0	Not a special CMD.
0	0	1	Initialization CMD: 74 clock cycles for initialization sequence.
0	1	0	Synchronized CMD: Wait for the end of the current data block transfer before sending the pending command.
0	1	1	Reserved.
1	0	0	Interrupt command: Corresponds to the Interrupt Mode (CMD40).
1	0	1	Interrupt response: Corresponds to the Interrupt Mode (CMD40).

- **RSPTYP: Response Type**

RSP		Response Type
0	0	No response.
0	1	48-bit response.
1	0	136-bit response.
1	1	Reserved.

- **CMDNB: Command Number**

30.8.7 Block Register

Name: BLKR

Access Type: Read/write

Offset: 0x00

Reset Value: –

31	30	29	28	27	26	25	24
BLKLEN							
23	22	21	20	19	18	17	16
BLKLEN							
15	14	13	12	11	10	9	8
BCNT							
7	6	5	4	3	2	1	0
BCNT							

- **BLKLEN: Data Block Length**

This field determines the size of the data block.

This field is also accessible in the MCI Mode Register (MR).

Bits 16 and 17 must be set to 0 if PDCFBYTE is disabled.

Note: In SDIO Byte mode, BLKLEN field is not used.

- **BCNT: MMC/SDIO Block Count - SDIO Byte Count**

This field determines the number of data byte(s) or block(s) to transfer.

The transfer data type and the authorized values for BCNT field are determined by the TRTYP field in the MCI Command Register (CMDR):

TRTYP			Type of Transfer	BCNT Authorized Values
0	0	1	MMC/SDCard Multiple Block	From 1 to MCI_MAXNUM_BLK: Value 0 corresponds to an infinite block transfer.
1	0	0	SDIO Byte	From 1 to 512 bytes: Value 0 corresponds to a 512-byte transfer. Values from 0x200 to 0xFFFF are forbidden.
1	0	1	SDIO Block	From 1 to 511 blocks: Value 0 corresponds to an infinite block transfer. Values from 0x200 to 0xFFFF are forbidden.
Other values			-	Reserved.

Warning: In SDIO Byte and Block modes, writing to the 7 last bits of BCNT field, is forbidden and may lead to unpredictable results.

30.8.8 Response Register

Name: RSPR

Access Type: Read-only

Offset: 0x20 - 0x2C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
RSP							
23	22	21	20	19	18	17	16
RSP							
15	14	13	12	11	10	9	8
RSP							
7	6	5	4	3	2	1	0
RSP							

- **RSP: Response**

Note: 1. The response register can be read by N accesses at the same RSPR or at consecutive addresses (0x20 to 0x2C). N depends on the size of the response.

30.8.9 Receive Data Register

Name: RDR

Access Type: Read-only

Offset: 0x30

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DATA							

23	22	21	20	19	18	17	16
DATA							

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA: Data to Read**

30.8.10 Transmit Data Register

Name: TDR

Access Type: Write-only

Offset: 0x34

Reset Value: –

31	30	29	28	27	26	25	24
DATA							

23	22	21	20	19	18	17	16
DATA							

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA: Data to Write**

30.8.11 Status Register

Name: SR

Access Type: Read-only

Offset: 0x40

Reset Value: 0x00000025

31	30	29	28	27	26	25	24
UNRE	OVRE	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
15	14	13	12	11	10	9	8
–	–	–	–	–	–	SDIOIRQB	SDIOIRQA
7	6	5	4	3	2	1	0
–	–	NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY

- **UNRE: Underrun**

0 = No error.

1 = At least one 8-bit data has been sent without valid information (not written). Cleared when sending a new data transfer command.

- **OVRE: Overrun**

0 = No error.

1 = At least one 8-bit received data has been lost (not read). Cleared when sending a new data transfer command.

- **DTOE: Data Time-out Error**

0 = No error.

1 = The data time-out set by DTOCYC and DTOMUL in DTOR has been exceeded. Cleared when reading SR.

- **DCRCE: Data CRC Error**

0 = No error.

1 = A CRC16 error has been detected in the last data block. Cleared when reading SR.

- **RTOE: Response Time-out Error**

0 = No error.

1 = The response time-out set by MAXLAT in the CMDR has been exceeded. Cleared when writing in the CMDR.

- **RENDE: Response End Bit Error**

0 = No error.

1 = The end bit of the response has not been detected. Cleared when writing in the CMDR.

- **RCRCE: Response CRC Error**

0 = No error.

1 = A CRC7 error has been detected in the response. Cleared when writing in the CMDR.

- **RDIRE: Response Direction Error**

0 = No error.

1 = The direction bit from card to host in the response has not been detected.

- **RINDE: Response Index Error**

0 = No error.

1 = A mismatch is detected between the command index sent and the response index received. Cleared when writing in the CMDR.

- **SDIOIRQB: SDIO Interrupt for Slot B**

0 = No interrupt detected on SDIO Slot B.

1 = A SDIO Interrupt on Slot B has reached. Cleared when reading the SR.

- **SDIOIRQA: SDIO Interrupt for Slot A**

0 = No interrupt detected on SDIO Slot A.

1 = A SDIO Interrupt on Slot A has reached. Cleared when reading the SR.

- **NOTBUSY: Data Not Busy**

This flag must be used only for Write Operations.

A block write operation uses a simple busy signalling of the write operation duration on the data (DAT0) line: during a data transfer block, if the card does not have a free data receive buffer, the card indicates this condition by pulling down the data line (DAT0) to LOW. The card stops pulling down the data line as soon as at least one receive buffer for the defined data transfer block length becomes free.

The NOTBUSY flag allows to deal with these different states.

0 = The MCI is not ready for new data transfer. Cleared at the end of the card response.

1 = The MCI is ready for new data transfer. Set when the busy state on the data line has ended. This corresponds to a free internal data receive buffer of the card.

Refer to the MMC or SD Specification for more details concerning the busy behavior.

- **DTIP: Data Transfer in Progress**

0 = No data transfer in progress.

1 = The current data transfer is still in progress, including CRC16 calculation. Cleared at the end of the CRC16 calculation.

- **BLKE: Data Block Ended**

This flag must be used only for Write Operations.

0 = A data block transfer is not yet finished. Cleared when reading the SR.

1 = A data block transfer has ended, including the CRC16 Status transmission.
The flag is set for each transmitted CRC Status.

Refer to the MMC or SD Specification for more details concerning the CRC Status.

- **TXRDY: Transmit Ready**

0= The last data written in TDR has not yet been transferred in the Shift Register.

1= The last data written in TDR has been transferred in the Shift Register.

- **RXRDY: Receiver Ready**

0 = No data has been received since the last read of RDR.

1 = Data has been received since the last read of RDR.

- **CMDRDY: Command Ready**

0 = A command is in progress.

1 = The last command has been sent. Cleared when writing in the CMDR.

30.8.12 Interrupt Enable Register

Name: IER

Access Type: Write-only

Offset: 0x44

Reset Value: –

31	30	29	28	27	26	25	24
UNRE	OVRE	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
15	14	13	12	11	10	9	8
–	–	–	–	–	–	SDIOIRQB	SDIOIRQA
7	6	5	4	3	2	1	0
–	–	NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY

- **UNRE: UnderRun Interrupt Enable**
- **OVRE: Overrun Interrupt Enable**
- **DTOE: Data Time-out Error Interrupt Enable**
- **DCRCE: Data CRC Error Interrupt Enable**
- **RTOE: Response Time-out Error Interrupt Enable**
- **RENDE: Response End Bit Error Interrupt Enable**
- **RCRCE: Response CRC Error Interrupt Enable**
- **RDIRE: Response Direction Error Interrupt Enable**
- **RINDE: Response Index Error Interrupt Enable**
- **SDIOIRQB: SDIO Interrupt for Slot B Interrupt Enable**
- **SDIOIRQA: SDIO Interrupt for Slot A Interrupt Enable**
- **NOTBUSY: Data Not Busy Interrupt Enable**
- **DTIP: Data Transfer in Progress Interrupt Enable**
- **BLKE: Data Block Ended Interrupt Enable**
- **TXRDY: Transmit Ready Interrupt Enable**
- **RXRDY: Receiver Ready Interrupt Enable**
- **CMDRDY: Command Ready Interrupt Enable**

0 = No effect.

1 = Enables the corresponding interrupt.

30.8.13 Interrupt Disable Register

Name: IDR

Access Type: Write-only

Offset: 0x48

Reset Value: –

31	30	29	28	27	26	25	24
UNRE	OVRE	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
15	14	13	12	11	10	9	8
–	–	–	–	–	–	SDIOIRQB	SDIOIRQA
7	6	5	4	3	2	1	0
–	–	NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY

- **UNRE: UnderRun Interrupt Disable**
- **OVRE: Overrun Interrupt Disable**
- **DTOE: Data Time-out Error Interrupt Disable**
- **DCRCE: Data CRC Error Interrupt Disable**
- **RTOE: Response Time-out Error Interrupt Disable**
- **RENDE: Response End Bit Error Interrupt Disable**
- **RCRCE: Response CRC Error Interrupt Disable**
- **RDIRE: Response Direction Error Interrupt Disable**
- **RINDE: Response Index Error Interrupt Disable**
- **SDIOIRQB: SDIO Interrupt for Slot B Interrupt Enable**
- **SDIOIRQA: SDIO Interrupt for Slot A Interrupt Enable**
- **NOTBUSY: Data Not Busy Interrupt Disable**
- **DTIP: Data Transfer in Progress Interrupt Disable**
- **BLKE: Data Block Ended Interrupt Disable**
- **TXRDY: Transmit Ready Interrupt Disable**
- **RXRDY: Receiver Ready Interrupt Disable**
- **CMDRDY: Command Ready Interrupt Disable**

0 = No effect.

1 = Disables the corresponding interrupt.

30.8.14 Interrupt Mask Register

Name: IMR

Access Type: Read-only

Offset: 0x4C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
UNRE	OVRE	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
15	14	13	12	11	10	9	8
–	–	–	–	–	–	SDIOIRQB	SDIOIRQA
7	6	5	4	3	2	1	0
–	–	NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY

- **UNRE: UnderRun Interrupt Mask**
- **OVRE: Overrun Interrupt Mask**
- **DTOE: Data Time-out Error Interrupt Mask**
- **DCRCE: Data CRC Error Interrupt Mask**
- **RTOE: Response Time-out Error Interrupt Mask**
- **RENDE: Response End Bit Error Interrupt Mask**
- **RCRCE: Response CRC Error Interrupt Mask**
- **RDIRE: Response Direction Error Interrupt Mask**
- **RINDE: Response Index Error Interrupt Mask**
- **SDIOIRQB: SDIO Interrupt for Slot B Interrupt Enable**
- **SDIOIRQA: SDIO Interrupt for Slot A Interrupt Enable**
- **NOTBUSY: Data Not Busy Interrupt Mask**
- **DTIP: Data Transfer in Progress Interrupt Mask**
- **BLKE: Data Block Ended Interrupt Mask**
- **TXRDY: Transmit Ready Interrupt Mask**
- **RXRDY: Receiver Ready Interrupt Mask**
- **CMDRDY: Command Ready Interrupt Mask**

0 = The corresponding interrupt is not enabled.

1 = The corresponding interrupt is enabled.

31. Ethernet MAC (MACB)

Rev: 1.1.2.5

31.1 Features

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s Operation
- Full- and Half-duplex Operation
- Statistics Counter Registers
- MII/RMII Interface to the Physical Layer
- Interrupt Generation to Signal Receive and Transmit Completion
- DMA Master on Receive and Transmit Channels
- Transmit and Receive FIFOs
- Automatic Pad and CRC Generation on Transmitted Frames
- Automatic Discard of Frames Received with Errors
- Address Checking Logic Supports Up to Four Specific 48-bit Addresses
- Supports Promiscuous Mode Where All Valid Received Frames are Copied to Memory
- Hash Matching of Unicast and Multicast Destination Addresses
- External Address Matching of Received Frames
- Physical Layer Management through MDIO Interface
- Half-duplex Flow Control by Forcing Collisions on Incoming Frames
- Full-duplex Flow Control with Recognition of Incoming Pause Frames and Hardware Generation of Transmitted Pause Frames
- Support for 802.1Q VLAN Tagging with Recognition of Incoming VLAN and Priority Tagged Frames
- Multiple Buffers per Receive and Transmit Frame
- Wake-on-LAN Support
- Jumbo Frames Up to 10240 bytes Supported

31.2 Description

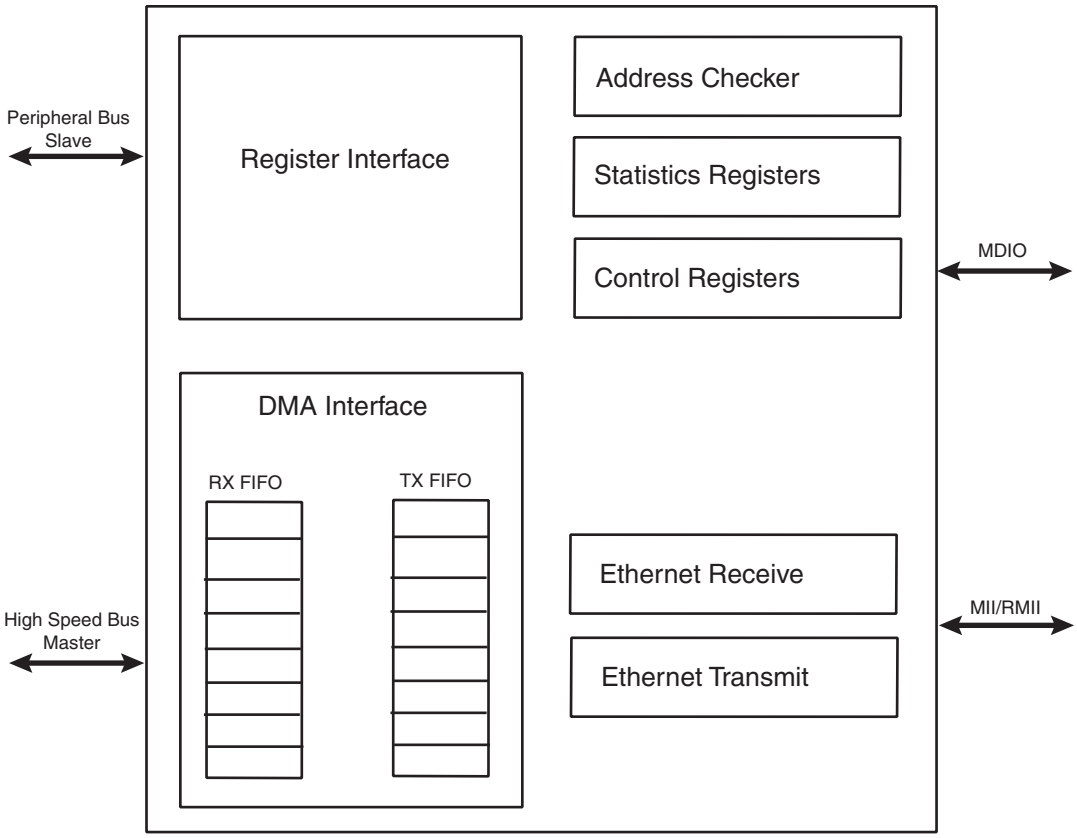
The MACB module implements a 10/100 Ethernet MAC compatible with the IEEE 802.3 standard using an address checker, statistics and control registers, receive and transmit blocks, and a DMA interface.

The address checker recognizes four specific 48-bit addresses and contains a 64-bit hash register for matching multicast and unicast addresses. It can recognize the broadcast address of all ones, copy all frames, and act on an external address match signal.

The statistics register block contains registers for counting various types of events associated with transmit and receive operations. These registers, along with the status words stored in the receive buffer list, enable software to generate network management statistics compatible with IEEE 802.3.

31.3 Block Diagram

Figure 31-1. MACB Block Diagram



31.4 Product Dependencies

31.4.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the MACB pins to their peripheral functions.

31.4.2 Power Management

The MACB clock is generated by the Power Manager. Before using the MACB, the programmer must ensure that the MACB clock is enabled in the Power Manager.

In the MACB description, Master Clock (MCK) is the clock of the peripheral bus to which the MACB is connected.

The synchronization module in the MACB requires that the bus clock (hclk) runs on at least the speed of the macb_tx/rx_clk, which is 25MHz in 100Mbps, and 2.5MHZ in 10Mbps in MII mode and 50MHz in 100Mbps, and 5MHZ in 10Mbps in RMII mode.

To prevent bus errors the MACB operation must be terminated before entering sleep mode.

31.4.3 Interrupt

The MACB interface has an interrupt line connected to the Interrupt Controller. Handling the MACB interrupt requires programming the interrupt controller before configuring the MACB.

31.5 Functional Description

Figure 31-1 on page 607 illustrates the different blocks of the MACB module.

The control registers drive the MDIO interface, setup DMA activity, start frame transmission and select modes of operation such as full- or half-duplex.

The receive block checks for valid preamble, FCS, alignment and length, and presents received frames to the address checking block and DMA interface.

The transmit block takes data from the DMA interface, adds preamble and, if necessary, pad and FCS, and transmits data according to the CSMA/CD (carrier sense multiple access with collision detect) protocol. The start of transmission is deferred if CRS (carrier sense) is active.

If COL (collision) becomes active during transmission, a jam sequence is asserted and the transmission is retried after a random back off. CRS and COL have no effect in full duplex mode.

The DMA block connects to external memory through its high speed bus (HSB) interface. It contains receive and transmit FIFOs for buffering frame data. It loads the transmit FIFO and empties the receive FIFO using HSB bus master operations. Receive data is not sent to memory until the address checking logic has determined that the frame should be copied. Receive or transmit frames are stored in one or more buffers. Receive buffers have a fixed length of 128 bytes. Transmit buffers range in length between 0 and 2047 bytes, and up to 128 buffers are permitted per frame. The DMA block manages the transmit and receive framebuffer queues. These queues can hold multiple frames.

31.5.1 Memory Interface

Frame data is transferred to and from the MACB through the DMA interface. All transfers are 32-bit words and may be single accesses or bursts of 2, 3 or 4 words. Burst accesses do not cross sixteen-byte boundaries. Bursts of 4 words are the default data transfer; single accesses or bursts of less than four words may be used to transfer data at the beginning or the end of a buffer.

The DMA controller performs six types of operation on the bus. In order of priority, these are:

1. Receive buffer manager write
2. Receive buffer manager read
3. Transmit data DMA read
4. Receive data DMA write
5. Transmit buffer manager read
6. Transmit buffer manager write

31.5.1.1 FIFO

The FIFO depths are 124 bytes.

Data is typically transferred into and out of the FIFOs in bursts of four words. For receive, a bus request is asserted when the FIFO contains four words and has space for three more. For transmit, a bus request is generated when there is space for four words, or when there is space for two words if the next transfer is to be only one or two words.

Thus the bus latency must be less than the time it takes to load the FIFO and transmit or receive three words (12 bytes) of data.

At 100 Mbit/s, it takes 960 ns to transmit or receive 12 bytes of data. In addition, six master clock cycles should be allowed for data to be loaded from the bus and to propagate through the FIFOs. For a 60 MHz master clock this takes 100 ns, making the bus latency requirement 860 ns.

31.5.1.2 Receive Buffers

Received frames, optionally including CRC/FCS, are written to receive buffers stored in memory. Each receive buffer is 128 bytes long. The start location for each receive buffer is stored in memory in a list of receive buffer descriptors at a location pointed to by the receive buffer queue pointer register. The receive buffer start location is a word address. For the first buffer of a frame, the start location can be offset by up to three bytes depending on the value written to bits 14 and 15 of the network configuration register. If the start location of the buffer is offset the available length of the first buffer of a frame is reduced by the corresponding number of bytes.

Each list entry consists of two words, the first being the address of the receive buffer and the second being the receive status. If the length of a receive frame exceeds the buffer length, the status word for the used buffer is written with zeroes except for the “start of frame” bit and the offset bits, if appropriate. Bit zero of the address field is written to one to show the buffer has been used. The receive buffer manager then reads the location of the next receive buffer and fills that with receive frame data. The final buffer descriptor status word contains the complete frame status. Refer to Table 31-1 for details of the receive buffer descriptor list.

Table 31-1. Receive Buffer Descriptor Entry

Bit	Function
Word 0	
31:2	Address of beginning of buffer
1	Wrap - marks last descriptor in receive buffer descriptor list.
0	Ownership - needs to be zero for the MACB to write data to the receive buffer. The MACB sets this to one once it has successfully written a frame to memory. Software has to clear this bit before the buffer can be used again.
Word 1	
31	Global all ones broadcast address detected
30	Multicast hash match
29	Unicast hash match
28	External address match
27	Reserved for future use
26	Specific address register 1 match
25	Specific address register 2 match
24	Specific address register 3 match
23	Specific address register 4 match
22	Type ID match
21	VLAN tag detected (i.e., type id of 0x8100)

Table 31-1. Receive Buffer Descriptor Entry (Continued)

Bit	Function
20	Priority tag detected (i.e., type id of 0x8100 and null VLAN identifier)
19:17	VLAN priority (only valid if bit 21 is set)
16	Concatenation format indicator (CFI) bit (only valid if bit 21 is set)
15	End of frame - when set the buffer contains the end of a frame. If end of frame is not set, then the only other valid status are bits 12, 13 and 14.
14	Start of frame - when set the buffer contains the start of a frame. If both bits 15 and 14 are set, then the buffer contains a whole frame.
13:12	Receive buffer offset - indicates the number of bytes by which the data in the first buffer is offset from the word address. Updated with the current values of the network configuration register. If jumbo frame mode is enabled through bit 3 of the network configuration register, then bits 13:12 of the receive buffer descriptor entry are used to indicate bits 13:12 of the frame length.
11:0	Length of frame including FCS (if selected). Bits 13:12 are also used if jumbo frame mode is selected.

To receive frames, the buffer descriptors must be initialized by writing an appropriate address to bits 31 to 2 in the first word of each list entry. Bit zero must be written with zero. Bit one is the wrap bit and indicates the last entry in the list.

The start location of the receive buffer descriptor list must be written to the receive buffer queue pointer register before setting the receive enable bit in the network control register to enable receive. As soon as the receive block starts writing received frame data to the receive FIFO, the receive buffer manager reads the first receive buffer location pointed to by the receive buffer queue pointer register.

If the filter block then indicates that the frame should be copied to memory, the receive data DMA operation starts writing data into the receive buffer. If an error occurs, the buffer is recovered. If the current buffer pointer has its wrap bit set or is the 1024th descriptor, the next receive buffer location is read from the beginning of the receive descriptor list. Otherwise, the next receive buffer location is read from the next word in memory.

There is an 11-bit counter to count out the 2048 word locations of a maximum length, receive buffer descriptor list. This is added with the value originally written to the receive buffer queue pointer register to produce a pointer into the list. A read of the receive buffer queue pointer register returns the pointer value, which is the queue entry currently being accessed. The counter is reset after receive status is written to a descriptor that has its wrap bit set or rolls over to zero after 1024 descriptors have been accessed. The value written to the receive buffer pointer register may be any word-aligned address, provided that there are at least 2048 word locations available between the pointer and the top of the memory.

The System Bus specification states that bursts should not cross 1K boundaries. As receive buffer manager writes are bursts of two words, to ensure that this does not occur, it is best to write the pointer register with the least three significant bits set to zero. As receive buffers are used, the receive buffer manager sets bit zero of the first word of the descriptor to indicate *used*. If a receive error is detected the receive buffer currently being written is recovered. Previous buffers are not recovered. Software should search through the *used* bits in the buffer descriptors to find out how many frames have been received. It should be checking the start-of-frame and end-of-frame bits, and not rely on the value returned by the receive buffer queue pointer register which changes continuously as more buffers are used.

For CRC errored frames, excessive length frames or length field mismatched frames, all of which are counted in the statistics registers, it is possible that a frame fragment might be stored in a sequence of receive buffers. Software can detect this by looking for start of frame bit set in a buffer following a buffer with no end of frame bit set.

For a properly working Ethernet system, there should be no excessively long frames or frames greater than 128 bytes with CRC/FCS errors. Collision fragments are less than 128 bytes long. Therefore, it is a rare occurrence to find a frame fragment in a receive buffer.

If bit zero is set when the receive buffer manager reads the location of the receive buffer, then the buffer has already been used and cannot be used again until software has processed the frame and cleared bit zero. In this case, the DMA block sets the buffer not available bit in the receive status register and triggers an interrupt.

If bit zero is set when the receive buffer manager reads the location of the receive buffer and a frame is being received, the frame is discarded and the receive resource error statistics register is incremented.

A receive overrun condition occurs when bus was not granted in time or because HRESP was not OK (bus error). In a receive overrun condition, the receive overrun interrupt is asserted and the buffer currently being written is recovered. The next frame received with an address that is recognized reuses the buffer.

If bit 17 of the network configuration register is set, the FCS of received frames shall not be copied to memory. The frame length indicated in the receive status field shall be reduced by four bytes in this case.

31.5.1.3 Transmit Buffer

Frames to be transmitted are stored in one or more transmit buffers. Transmit buffers can be between 0 and 2047 bytes long, so it is possible to transmit frames longer than the maximum length specified in IEEE Standard 802.3. Zero length buffers are allowed. The maximum number of buffers permitted for each transmit frame is 128.

The start location for each transmit buffer is stored in memory in a list of transmit buffer descriptors at a location pointed to by the transmit buffer queue pointer register. Each list entry consists of two words, the first being the byte address of the transmit buffer and the second containing the transmit control and status. Frames can be transmitted with or without automatic CRC generation. If CRC is automatically generated, padding is also automatically generated to take frames to a minimum length of 64 bytes. Table 31-2 on page 612 defines an entry in the transmit buffer descriptor list. To transmit frames, the buffer descriptors must be initialized by writing an appropriate byte address to bits 31 to 0 in the first word of each list entry. The second transmit buffer descriptor is initialized with control information that indicates the length of the buffer, whether or not it is to be transmitted with CRC and whether the buffer is the last buffer in the frame.

After transmission, the control bits are written back to the second word of the first buffer along with the “used” bit and other status information. Before a transmission, bit 31 is the “used” bit which must be zero when the control word is read. It is written to one when a frame has been transmitted. Bits 27, 28 and 29 indicate various transmit error conditions. Bit 30 is the “wrap” bit which can be set for any buffer within a frame. If no wrap bit is encountered after 1024 descriptors, the queue pointer rolls over to the start.

The transmit buffer queue pointer register must not be written while transmit is active. If a new value is written to the transmit buffer queue pointer register, the queue pointer resets itself to

point to the beginning of the new queue. If transmit is disabled by writing to bit 3 of the network control, the transmit buffer queue pointer register resets to point to the beginning of the transmit queue. Note that disabling receive does not have the same effect on the receive queue pointer.

Once the transmit queue is initialized, transmit is activated by writing to bit 9, the *Transmit Start* bit of the network control register. Transmit is halted when a buffer descriptor with its *used* bit set is read, or if a transmit error occurs, or by writing to the transmit halt bit of the network control register. (Transmission is suspended if a pause frame is received while the pause enable bit is set in the network configuration register.) Rewriting the start bit while transmission is active is allowed.

Transmission control is implemented with a Tx_go variable which is readable in the transmit status register at bit location 3. The Tx_go variable is reset when:

–transmit is disabled

–a buffer descriptor with its ownership bit set is read

–a new value is written to the transmit buffer queue pointer register

–bit 10, tx_halt, of the network control register is written

–there is a transmit error such as too many retries or a transmit underrun.

To set tx_go, write to bit 9, tx_start, of the network control register. Transmit halt does not take effect until any ongoing transmit finishes. If a collision occurs during transmission of a multi-buffer frame, transmission automatically restarts from the first buffer of the frame. If a “used” bit is read midway through transmission of a multi-buffer frame, this is treated as a transmit error. Transmission stops, tx_er is asserted and the FCS is bad.

If transmission stops due to a transmit error, the transmit queue pointer resets to point to the beginning of the transmit queue. Software needs to re-initialize the transmit queue after a transmit error.

If transmission stops due to a “used” bit being read at the start of the frame, the transmission queue pointer is not reset and transmit starts from the same transmit buffer descriptor when the transmit start bit is written

Table 31-2. Transmit Buffer Descriptor Entry

Bit	Function
	Word 0
31:0	**Byte Address of buffer**
	Word 1
31	Used. Needs to be zero for the MACB to read data from the transmit buffer. The MACB sets this to one for the first buffer of a frame once it has been successfully transmitted. Software has to clear this bit before the buffer can be used again. Note: This bit is only set for the first buffer in a frame unlike receive where all buffers have the Used bit set once used.
30	Wrap. Marks last descriptor in transmit buffer descriptor list.
29	Retry limit exceeded, transmit error detected
28	Transmit underrun, occurs either when hresp is not OK (bus error) or the transmit data could not be fetched in time or when buffers are exhausted in mid frame.
27	Buffers exhausted in mid frame
26:17	Reserved

Table 31-2. Transmit Buffer Descriptor Entry (Continued)

Bit	Function
16	No CRC. When set, no CRC is appended to the current frame. This bit only needs to be set for the last buffer of a frame.
15	Last buffer. When set, this bit indicates the last buffer in the current frame has been reached.
14:11	Reserved
10:0	Length of buffer

31.5.2 Transmit Block

This block transmits frames in accordance with the Ethernet IEEE 802.3 CSMA/CD protocol. Frame assembly starts by adding preamble and the start frame delimiter. Data is taken from the transmit FIFO a word at a time. Data is transmitted least significant nibble first. If necessary, padding is added to increase the frame length to 60 bytes. CRC is calculated as a 32-bit polynomial. This is inverted and appended to the end of the frame, taking the frame length to a minimum of 64 bytes. If the No CRC bit is set in the second word of the last buffer descriptor of a transmit frame, neither pad nor CRC are appended.

In full-duplex mode, frames are transmitted immediately. Back-to-back frames are transmitted at least 96 bit times apart to guarantee the interframe gap.

In half-duplex mode, the transmitter checks carrier sense. If asserted, it waits for it to de-assert and then starts transmission after the interframe gap of 96 bit times. If the collision signal is asserted during transmission, the transmitter transmits a jam sequence of 32 bits taken from the data register and retries transmission after the back off time has elapsed.

The back-off time is based on an XOR of the 10 least significant bits of the data coming from the transmit FIFO and a 10-bit pseudo random number. The number of bits used depends on the number of collisions seen. After the first collision, 1 bit is used, after the second 2, and so on up to 10. Above 10, all 10 bits are used. An error is indicated and no further attempts are made if 16 attempts cause collisions.

If transmit DMA underruns, bad CRC is automatically appended using the same mechanism as jam insertion and the TX_ER signal is asserted. In a properly configured system, this should never happen.

If the back pressure bit is set in the network control register in half duplex mode, the transmit block transmits 64 bits of data, which can consist of 16 nibbles of 1011 or in bit-rate mode 64 1s, whenever it sees an incoming frame to force a collision. This provides a way of implementing flow control in half-duplex mode.

31.5.3 Pause Frame Support

The start of an 802.3 pause frame is as follows:

Table 31-3. Start of an 802.3 Pause Frame

Destination Address	Source Address	Type (Mac Control Frame)	Pause Opcode	Pause Time
0x0180C2000001	6 bytes	0x8808	0x0001	2 bytes

The network configuration register contains a receive pause enable bit (13). If a valid pause frame is received, the pause time register is updated with the frame's pause time, regardless of

its current contents and regardless of the state of the configuration register bit 13. An interrupt (12) is triggered when a pause frame is received, assuming it is enabled in the interrupt mask register. If bit 13 is set in the network configuration register and the value of the pause time register is non-zero, no new frame is transmitted until the pause time register has decremented to zero.

The loading of a new pause time, and hence the pausing of transmission, only occurs when the MACB is configured for full-duplex operation. If the MACB is configured for half-duplex, there is no transmission pause, but the pause frame received interrupt is still triggered.

A valid pause frame is defined as having a destination address that matches either the address stored in specific address register 1 or matches 0x0180C2000001 and has the MAC control frame type ID of 0x8808 and the pause opcode of 0x0001. Pause frames that have FCS or other errors are treated as invalid and are discarded. Valid pause frames received increment the Pause Frame Received statistic register.

The pause time register decrements every 512 bit times (i.e., 128 `rx_clks` in nibble mode) once transmission has stopped. For test purposes, the register decrements every `rx_clk` cycle once transmission has stopped if bit 12 (retry test) is set in the network configuration register. If the pause enable bit (13) is not set in the network configuration register, then the decrementing occurs regardless of whether transmission has stopped or not.

An interrupt (13) is asserted whenever the pause time register decrements to zero (assuming it is enabled in the interrupt mask register). Automatic transmission of pause frames is supported through the transmit pause frame bits of the network control register and the `tx_pause` and `tx_pause_zero` inputs. If either bit 11 or bit 12 of the network control register is written to with a 1, or if the input signal `tx_pause` is toggled, a pause frame is transmitted only if full duplex is selected in the network configuration register and transmit is enabled in the network control register.

Pause frame transmission occurs immediately if transmit is inactive or if transmit is active between the current frame and the next frame due to be transmitted. The transmitted pause frame is comprised of the items in the following list:

- a destination address of 01-80-C2-00-00-01
- a source address taken from the specific address 1 register
- a type ID of 88-08 (MAC control frame)
- a pause opcode of 00-01
- a pause quantum
- fill of 00 to take the frame to minimum frame length
- valid FCS

The pause quantum used in the generated frame depends on the trigger source for the frame as follows:

1. If bit 11 is written with a one, the pause quantum comes from the transmit pause quantum register. The Transmit Pause Quantum register resets to a value of 0xFFFF giving a maximum pause quantum as a default.
2. If bit 12 is written with a one, the pause quantum is zero.
3. If the `tx_pause` input is toggled and the `tx_pause_zero` input is held low until the next toggle, the pause quantum comes from the transmit pause quantum register.
4. If the `tx_pause` input is toggled and the `tx_pause_zero` input is held high until the next toggle, the pause quantum is zero.

After transmission, no interrupts are generated and the only statistics register that is incremented is the pause frames transmitted register.

31.5.4 Receive Block

The receive block checks for valid preamble, FCS, alignment and length, presents received frames to the DMA block and stores the frames destination address for use by the address checking block. If, during frame reception, the frame is found to be too long or rx_er is asserted, a bad frame indication is sent to the DMA block. The DMA block then ceases sending data to memory. At the end of frame reception, the receive block indicates to the DMA block whether the frame is good or bad. The DMA block recovers the current receive buffer if the frame was bad. The receive block signals the register block to increment the alignment error, the CRC (FCS) error, the short frame, long frame, jabber error, the receive symbol error statistics and the length field mismatch statistics.

The enable bit for jumbo frames in the network configuration register allows the MACB to receive jumbo frames of up to 10240 bytes in size. This operation does not form part of the IEEE802.3 specification and is disabled by default. When jumbo frames are enabled, frames received with a frame size greater than 10240 bytes are discarded.

31.5.5 Address Checking Block

The address checking (or filter) block indicates to the DMA block which receive frames should be copied to memory. Whether a frame is copied depends on what is enabled in the network configuration register, the state of the external match pin, the contents of the specific address and hash registers and the frame's destination address. In this implementation of the MACB, the frame's source address is not checked. Provided that bit 18 of the Network Configuration register is not set, a frame is not copied to memory if the MACB is transmitting in half duplex mode at the time a destination address is received. If bit 18 of the Network Configuration register is set, frames can be received while transmitting in half-duplex mode.

Ethernet frames are transmitted a byte at a time, least significant bit first. The first six bytes (48 bits) of an Ethernet frame make up the destination address. The first bit of the destination address, the LSB of the first byte of the frame, is the group/individual bit: this is *One* for multicast addresses and *Zero* for unicast. The *All Ones* address is the broadcast address, and a special case of multicast.

The MACB supports recognition of four specific addresses. Each specific address requires two registers, specific address register bottom and specific address register top. Specific address register bottom stores the first four bytes of the destination address and specific address register top contains the last two bytes. The addresses stored can be specific, group, local or universal.

The destination address of received frames is compared against the data stored in the specific address registers once they have been activated. The addresses are deactivated at reset or when their corresponding specific address register bottom is written. They are activated when specific address register top is written. If a receive frame address matches an active address, the frame is copied to memory.

The following example illustrates the use of the address match registers for a MAC address of 21:43:65:87:A9:CB.

Preamble 55

SFD D5

DA (Octet0 - LSB) 21

DA(Octet 1) 43

DA(Octet 2) 65

DA(Octet 3) 87

DA(Octet 4) A9

DA (Octet5 - MSB) CB

SA (LSB) 00

SA 00

SA 00

SA 00

SA 00

SA (MSB) 43

SA (LSB) 21

The sequence above shows the beginning of an Ethernet frame. Byte order of transmission is from top to bottom as shown. For a successful match to specific address 1, the following address matching registers must be set up:

- Base address + 0x98 0x87654321 (Bottom)
- Base address + 0x9C 0x0000CBA9 (Top)

And for a successful match to the Type ID register, the following should be set up:

- Base address + 0xB8 0x00004321

31.5.6 Broadcast Address

The broadcast address of 0xFFFFFFFFFFFF is recognized unless the 'no broadcast' bit in the network configuration register is set.

31.5.7 Hash Addressing

The hash address register is 64 bits long and takes up two locations in the memory map. The least significant bits are stored in hash register bottom and the most significant bits in hash register top.

The unicast hash enable and the multicast hash enable bits in the network configuration register enable the reception of hash matched frames. The destination address is reduced to a 6-bit index into the 64-bit hash register using the following hash function. The hash function is an *exclusive or* of every sixth bit of the destination address.

hash_index[5] = da[5] ^ da[11] ^ da[17] ^ da[23] ^ da[29] ^ da[35] ^ da[41] ^ da[47]

hash_index[4] = da[4] ^ da[10] ^ da[16] ^ da[22] ^ da[28] ^ da[34] ^ da[40] ^ da[46]

hash_index[3] = da[3] ^ da[09] ^ da[15] ^ da[21] ^ da[27] ^ da[33] ^ da[39] ^ da[45]

hash_index[2] = da[2] ^ da[08] ^ da[14] ^ da[20] ^ da[26] ^ da[32] ^ da[38] ^ da[44]

hash_index[1] = da[1] ^ da[07] ^ da[13] ^ da[19] ^ da[25] ^ da[31] ^ da[37] ^ da[43]

hash_index[0] = da[0] ^ da[06] ^ da[12] ^ da[18] ^ da[24] ^ da[30] ^ da[36] ^ da[42]

`da[0]` represents the least significant bit of the first byte received, that is, the multicast/unicast indicator, and `da[47]` represents the most significant bit of the last byte received.

If the hash index points to a bit that is set in the hash register, then the frame is matched according to whether the frame is multicast or unicast.

A multicast match is signalled if the multicast hash enable bit is set. da[0] is 1 and the hash index points to a bit set in the hash register.

A unicast match is signalled if the unicast hash enable bit is set. da[0] is 0 and the hash index points to a bit set in the hash register.

To receive all multicast frames, the hash register should be set with all ones and the multicast hash enable bit should be set in the network configuration register.

31.5.8 External Address Matching

The external address signal (eam) is enabled by bit 9 in the network configuration register. When enabled, the filter block sends the store frame and the external address match status signal to the DMA block if the external address match signal is asserted (from a source external to the MACB) and the destination address has been received and the frame has not completed.

For the DMA block to be able to copy the frame to memory, the external address signal must be asserted before four words have been loaded into the receive FIFO.

31.5.9 Copy All Frames (or Promiscuous Mode)

If the copy all frames bit is set in the network configuration register, then all non-errored frames are copied to memory. For example, frames that are too long, too short, or have FCS errors or rx_er asserted during reception are discarded and all others are received. Frames with FCS errors are copied to memory if bit 19 in the network configuration register is set.

31.5.10 Type ID Checking

The contents of the type_id register are compared against the length/type ID of received frames (i.e., bytes 13 and 14). Bit 22 in the receive buffer descriptor status is set if there is a match. The reset state of this register is zero which is unlikely to match the length/type ID of any valid Ethernet frame.

Note: A type ID match does not affect whether a frame is copied to memory.

31.5.11 VLAN Support

An Ethernet encoded 802.1Q VLAN tag looks like this:

Table 31-4. 802.1Q VLAN Tag

TPID (Tag Protocol Identifier) 16 bits	TCI (Tag Control Information) 16 bits
0x8100	First 3 bits priority, then CFI bit, last 12 bits VID

The VLAN tag is inserted at the 13th byte of the frame, adding an extra four bytes to the frame. If the VID (VLAN identifier) is null (0x000), this indicates a priority-tagged frame. The MAC can support frame lengths up to 1536 bytes, 18 bytes more than the original Ethernet maximum frame length of 1518 bytes. This is achieved by setting bit 8 in the network configuration register.

The following bits in the receive buffer descriptor status word give information about VLAN tagged frames:

- Bit 21 set if receive frame is VLAN tagged (i.e. type id of 0x8100)
- Bit 20 set if receive frame is priority tagged (i.e. type id of 0x8100 and null VID). (If bit 20 is set bit 21 is set also.)
- Bit 19, 18 and 17 set to priority if bit 21 is set
- Bit 16 set to CFI if bit 21 is set

31.5.12 PHY Maintenance

The register MAN enables the MACB to communicate with a PHY by means of the MDIO interface. It is used during auto-negotiation to ensure that the MACB and the PHY are configured for the same speed and duplex configuration.

The PHY maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit two is set in the network status register (about 2000 MCK cycles later when bit ten is set to zero, and bit eleven is set to one in the network configuration register). An interrupt is generated as this bit is set. During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each MDC cycle. This causes transmission of a PHY management frame on MDIO.

Reading during the shift operation returns the current contents of the shift register. At the end of management operation, the bits have shifted back to their original locations. For a read operation, the data bits are updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced.

The MDIO interface can read IEEE 802.3 clause 45 PHYs as well as clause 22 PHYs. To read clause 45 PHYs, bits[31:28] should be written as 0x0011. For a description of MDC generation, see the network configuration register in the ”Network Control Register” on page 625.

31.5.13 Media Independent Interface

The Ethernet MAC is capable of interfacing to both RMII and MII Interfaces. The RMII bit in the USRIO register controls the interface that is selected. When this bit is set, the RMII interface is selected, else the MII interface is selected.

The MII and RMII interface are capable of both 10Mb/s and 100Mb/s data rates as described in the IEEE 802.3u standard. The signals used by the MII and RMII interfaces are described in Table 31-5.

Table 31-5. Pin Configuration

Pin Name	MII	RMII
ETXCK_EREFCK	ETXCK: Transmit Clock	EREFCK: Reference Clock
ECRS	ECRS: Carrier Sense	
ECOL	ECOL: Collision Detect	
ERXDV	ERXDV: Data Valid	ECRSDV: Carrier Sense/Data Valid
ERX0 - ERX3	ERX0 - ERX3: 4-bit Receive Data	ERX0 - ERX1: 2-bit Receive Data
ERXER	ERXER: Receive Error	ERXER: Receive Error
ERXCK	ERXCK: Receive Clock	
ETXEN	ETXEN: Transmit Enable	ETXEN: Transmit Enable
ETX0-ETX3	ETX0 - ETX3: 4-bit Transmit Data	ETX0 - ETX1: 2-bit Transmit Data
ETXER	ETXER: Transmit Error	

The intent of the RMII is to provide a reduced pin count alternative to the IEEE 802.3u MII. It uses 2 bits for transmit (ETX0 and ETX1) and two bits for receive (ERX0 and ERX1). There is a Transmit Enable (ETXEN), a Receive Error (ERXER), a Carrier Sense (ECRS_DV), and a 50 MHz Reference Clock (ETXCK_EREFCK) for 100Mb/s data rate.

31.5.13.1 RMII Transmit and Receive Operation

The same signals are used internally for both the RMII and the MII operations. The RMII maps these signals in a more pin-efficient manner. The transmit and receive bits are converted from a 4-bit parallel format to a 2-bit parallel scheme that is clocked at twice the rate. The carrier sense and data valid signals are combined into the ECRSDV signal. This signal contains information on carrier sense, FIFO status, and validity of the data. Transmit error bit (ETXER) and collision detect (ECOL) are not used in RMII mode.

31.6 Programming Interface

31.6.1 Initialization

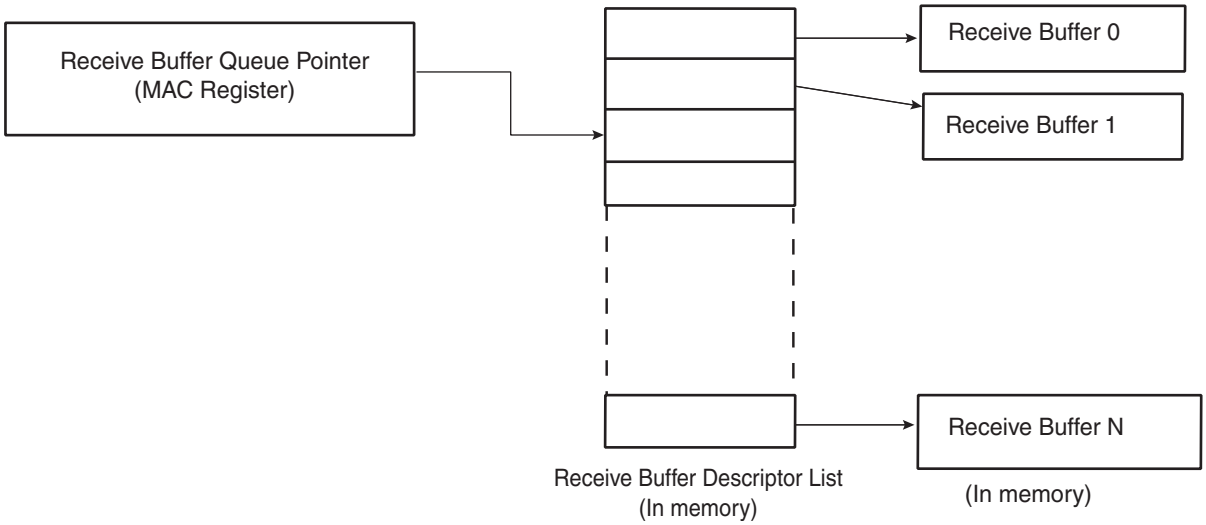
31.6.1.1 Configuration

Initialization of the MACB configuration (e.g. frequency ratios) must be done while the transmit and receive circuits are disabled. See the description of the network control register and network configuration register later in this document.

31.6.1.2 Receive Buffer List

Receive data is written to areas of data (i.e., buffers) in system memory. These buffers are listed in another data structure that also resides in main memory. This data structure (receive buffer queue) is a sequence of descriptor entries as defined in ”Receive Buffer Descriptor Entry” on page 609. It points to this data structure.

Figure 31-2. Receive Buffer List



To create the list of buffers:

1. Allocate a number (*n*) of buffers of 128 bytes in system memory.
2. Allocate an area 2*n* words for the receive buffer descriptor entry in system memory and create *n* entries in this list. Mark all entries in this list as owned by MACB, i.e., bit 0 of word 0 set to 0.
3. If less than 1024 buffers are defined, the last descriptor must be marked with the wrap bit (bit 1 in word 0 set to 1).
4. Write address of receive buffer descriptor entry to MACB register receive_buffer queue pointer.
5. The receive circuits can then be enabled by writing to the address recognition registers and then to the network control register.

31.6.1.3 Transmit Buffer List

Transmit data is read from the system memory These buffers are listed in another data structure that also resides in main memory. This data structure (Transmit Buffer Queue) is a sequence of descriptor entries (as defined in Table 31-2 on page 612) that points to this data structure.

To create this list of buffers:

1. Allocate a number (*n*) of buffers of between 1 and 2047 bytes of data to be transmitted in system memory. Up to 128 buffers per frame are allowed.
2. Allocate an area 2*n* words for the transmit buffer descriptor entry in system memory and create N entries in this list. Mark all entries in this list as owned by MACB, i.e. bit 31 of word 1 set to 0.
3. If fewer than 1024 buffers are defined, the last descriptor must be marked with the wrap bit — bit 30 in word 1 set to 1.
4. Write address of transmit buffer descriptor entry to MACB register transmit_buffer queue pointer.
5. The transmit circuits can then be enabled by writing to the network control register.

31.6.1.4 Address Matching

The MACB register-pair hash address and the four specific address register-pairs must be written with the required values. Each register-pair comprises a bottom register and top register, with the bottom register being written first. The address matching is disabled for a particular register-pair after the bottom-register has been written and re-enabled when the top register is written. See Section “31.5.5” on page 615. for details of address matching. Each register-pair may be written at any time, regardless of whether the receive circuits are enabled or disabled.

31.6.1.5 Interrupts

There are 14 interrupt conditions that are detected within the MACB. These are ORed to make a single interrupt. This interrupt is passed to the interrupt controller. On receipt of the interrupt signal, the CPU enters the interrupt handler. To ascertain which interrupt has been generated, read the interrupt status register. Note that this register clears itself when read. At reset, all interrupts are disabled. To enable an interrupt, write to interrupt enable register with the pertinent interrupt bit set to 1. To disable an interrupt, write to interrupt disable register with the pertinent interrupt bit set to 1. To check whether an interrupt is enabled or disabled, read interrupt mask register: if the bit is set to 1, the interrupt is disabled.

31.6.1.6 Transmitting Frames

To set up a frame for transmission:

1. Enable transmit in the network control register.
2. Allocate an area of system memory for transmit data. This does not have to be contiguous, varying byte lengths can be used as long as they conclude on byte borders.
3. Set-up the transmit buffer list.
4. Set the network control register to enable transmission and enable interrupts.
5. Write data for transmission into these buffers.
6. Write the address to transmit buffer descriptor queue pointer.
7. Write control and length to word one of the transmit buffer descriptor entry.
8. Write to the transmit start bit in the network control register.

31.6.1.7 Receiving Frames

When a frame is received and the receive circuits are enabled, the MACB checks the address and, in the following cases, the frame is written to system memory:

- if it matches one of the four specific address registers.
- if it matches the hash address function.
- if it is a broadcast address (0xFFFFFFFFFFFF) and broadcasts are allowed.
- if the MACB is configured to copy all frames.
- if the EAM is asserted before four words have been loaded into the receive FIFO.

The register receive buffer queue pointer points to the next entry (see Table 31-1 on page 609) and the MACB uses this as the address in system memory to write the frame to. Once the frame has been completely and successfully received and written to system memory, the MACB then updates the receive buffer descriptor entry with the reason for the address match and marks the area as being owned by software. Once this is complete an interrupt receive complete is set. Software is then responsible for handling the data in the buffer and then releasing the buffer by writing the ownership bit back to 0.

If the MACB is unable to write the data at a rate to match the incoming frame, then an interrupt receive overrun is set. If there is no receive buffer available, i.e., the next buffer is still owned by software, the interrupt receive buffer not available is set. If the frame is not successfully received, a statistic register is incremented and the frame is discarded without informing software.

31.7 Ethernet MAC (MACB) User Interface

Table 31-6. Ethernet MAC (MACB) Register Mapping

Offset	Register	Name	Access	Reset Value
0x00	Network Control Register	NCR	Read/Write	0
0x04	Network Configuration Register	NCFG	Read/Write	0x800
0x08	Network Status Register	NSR	Read-only	-
0x0C	Reserved			
0x10	Reserved			
0x14	Transmit Status Register	TSR	Read/Write	0x0000_0000
0x18	Receive Buffer Queue Pointer Register	RBQP	Read/Write	0x0000_0000
0x1C	Transmit Buffer Queue Pointer Register	TBQP	Read/Write	0x0000_0000
0x20	Receive Status Register	RSR	Read/Write	0x0000_0000
0x24	Interrupt Status Register	ISR	Read/Write	0x0000_0000
0x28	Interrupt Enable Register	IER	Write-only	-
0x2C	Interrupt Disable Register	IDR	Write-only	-
0x30	Interrupt Mask Register	IMR	Read-only	0x0000_3FFF
0x34	Phy Maintenance Register	MAN	Read/Write	0x0000_0000
0x38	Pause Time Register	PTR	Read/Write	0x0000_0000
0x3C	Pause Frames Received Register	PFR	Read/Write	0x0000_0000
0x40	Frames Transmitted Ok Register	FTO	Read/Write	0x0000_0000
0x44	Single Collision Frames Register	SCF	Read/Write	0x0000_0000
0x48	Multiple Collision Frames Register	MCF	Read/Write	0x0000_0000
0x4C	Frames Received Ok Register	FRO	Read/Write	0x0000_0000
0x50	Frame Check Sequence Errors Register	FCSE	Read/Write	0x0000_0000
0x54	Alignment Errors Register	ALE	Read/Write	0x0000_0000
0x58	Deferred Transmission Frames Register	DTF	Read/Write	0x0000_0000
0x5C	Late Collisions Register	LCOL	Read/Write	0x0000_0000
0x60	Excessive Collisions Register	EXCOL	Read/Write	0x0000_0000
0x64	Transmit Underrun Errors Register	TUND	Read/Write	0x0000_0000
0x68	Carrier Sense Errors Register	CSE	Read/Write	0x0000_0000
0x6C	Receive Resource Errors Register	RRE	Read/Write	0x0000_0000
0x70	Receive Overrun Errors Register	ROV	Read/Write	0x0000_0000
0x74	Receive Symbol Errors Register	RSE	Read/Write	0x0000_0000
0x78	Excessive Length Errors Register	ELE	Read/Write	0x0000_0000
0x7C	Receive Jabbers Register	RJA	Read/Write	0x0000_0000
0x80	Undersize Frames Register	USF	Read/Write	0x0000_0000
0x84	SQE Test Errors Register	STE	Read/Write	0x0000_0000
0x88	Received Length Field Mismatch Register	RLE	Read/Write	0x0000_0000

Table 31-6. Ethernet MAC (MACB) Register Mapping (Continued)

Offset	Register	Name	Access	Reset Value
0x8C	Transmitted Pause Frames Register	TPF	Read/Write	0x0000_0000
0x90	Hash Register Bottom [31:0] Register	HRB	Read/Write	0x0000_0000
0x94	Hash Register Top [63:32] Register	HRT	Read/Write	0x0000_0000
0x98	Specific Address 1 Bottom Register	SA1B	Read/Write	0x0000_0000
0x9C	Specific Address 1 Top Register	SA1T	Read/Write	0x0000_0000
0xA0	Specific Address 2 Bottom Register	SA2B	Read/Write	0x0000_0000
0xA4	Specific Address 2 Top Register	SA2T	Read/Write	0x0000_0000
0xA8	Specific Address 3 Bottom Register	SA3B	Read/Write	0x0000_0000
0xAC	Specific Address 3 Top Register	SA3T	Read/Write	0x0000_0000
0xB0	Specific Address 4 Bottom Register	SA4B	Read/Write	0x0000_0000
0xB4	Specific Address 4 Top Register	SA4T	Read/Write	0x0000_0000
0xB8	Type ID Checking Register	TID	Read/Write	0x0000_0000
0xBC	Transmit Pause Quantum Register	TPQ	Read/Write	0x0000_FFFF
0xC0	User Input/output Register	USRIO	Read/Write	0x0000_0000
0xC4	Wake on LAN Register	WOL	Read/Write	0x0000_0000
0xC8 - 0xFC	Reserved	–	–	–

31.7.1 Network Control Register

Register Name: NCR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	TZQ	TPF	THALT	TSTART	BP
7	6	5	4	3	2	1	0
WESTAT	INCSTAT	CLRSTAT	MPE	TE	RE	LLB	LB

- **LB: LoopBack**

Asserts the loopback signal to the PHY.

- **LLB: LoopBack Local**

connects txd to rxd, tx_en to rx_dv, forces full duplex and drives rx_clk and tx_clk with pclk divided by 4. rx_clk and tx_clk may glitch as the MACB is switched into and out of internal loop back. It is important that receive and transmit circuits have already been disabled when making the switch into and out of internal loop back. This function may not be supported by some instantiations of the MACB.

- **RE: Receive enable**

When set, enables the MACB to receive data. When reset, frame reception stops immediately and the receive FIFO is cleared. The receive queue pointer register is unaffected.

- **TE: Transmit enable**

When set, enables the Ethernet transmitter to send data. When reset, transmission stops immediately, the transmit FIFO and control registers are cleared and the transmit queue pointer register resets to point to the start of the transmit descriptor list.

- **MPE: Management port enable**

Set to one to enable the management port. When zero, forces MDIO to high impedance state and MDC low.

- **CLRSTAT: Clear statistics registers**

This bit is write only. Writing a one clears the statistics registers.

- **INCSTAT: Increment statistics registers**

This bit is write only. Writing a one increments all the statistics registers by one for test purposes.

- **WESTAT: Write enable for statistics registers**

Setting this bit to one makes the statistics registers writable for functional test purposes.

- **BP: Back pressure**

If set in half duplex mode, forces collisions on all received frames.

- **TSTART: Start transmission**

Writing one to this bit starts transmission.

- **THALT: Transmit halt**

Writing one to this bit halts transmission as soon as any ongoing frame transmission ends.

- **TPF: Transmit pause frame**

Writing one to this bit transmits a pause frame with the pause quantum from the transmit pause quantum register at the next available transmitter idle time.

- **TZQ: Transmit zero quantum pause frame**

Writing a one to this bit transmits a pause frame with zero pause quantum at the next available transmitter idle time.

31.7.2 Network Configuration Register

Register Name: NCFGR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	IRXFCS	EFRHD	DRFCS	RLCE

15	14	13	12	11	10	9	8
RBOF		PAE	RTY	CLK		EAE	BIG

7	6	5	4	3	2	1	0
UNI	MTI	NBC	CAF	JFRAME	Bit rate	FD	SPD

- **SPD: Speed**

Set to 1 to indicate 100 Mbit/s operation, 0 for 10 Mbit/s. The value of this pin is reflected on the `speed` pin.

- **FD: Full Duplex**

If set to 1, the transmit block ignores the state of collision and carrier sense and allows receive while transmitting. Also controls the `half_duplex` pin.

- **Bit rate:**

If set to 1 to configure the interface for serial operation. Must be set before receive and transmit enable in the network control register. If set a serial interface is configured with transmit and receive data being driven out on txd[0] and received on rxd[0] serially. Also the crs and rx_dv are logically ORed together so either may be used as the data valid signal.

- **CAF: Copy All Frames**

When set to 1, all valid frames are received.

- **JFRAME: Jumbo Frames**

Set to one to enable jumbo frames of up to 10240 bytes to be accepted.

- **NBC: No Broadcast**

When set to 1, frames addressed to the broadcast address of all ones are not received.

- **MTI: Multicast Hash Enable**

When set, multicast frames are received when the 6-bit hash function of the destination address points to a bit that is set in the hash register.

- **UNI: Unicast Hash Enable**

When set, unicast frames are received when the 6-bit hash function of the destination address points to a bit that is set in the hash register.

- **BIG: Receive 1536 bytes frames**

Setting this bit means the MACB receives frames up to 1536 bytes in length. Normally, the MACB would reject any frame above 1518 bytes.

- **EAE: External address match enable**

When set, the `eam` pin can be used to copy frames to memory.

- **CLK: MDC clock divider**

Set according to `system clock` speed. This determines by what number `system clock` is divided to generate MDC. For conformance with 802.3, MDC must not exceed 2.5MHz (MDC is only active during MDIO read and write operations).

CLK	MDC
00	**MCK divided by 8 (MCK up to 20 MHz)**
01	**MCK divided by 16 (MCK up to 40 MHz)**
10	**MCK divided by 32 (MCK up to 80 MHz)**
11	**MCK divided by 64 (MCK up to 160 MHz)**

- **RTY: Retry test**

Must be set to zero for normal operation. If set to one, the back off between collisions is always one slot time. Setting this bit to one helps testing the too many retries condition. Also used in the pause frame tests to reduce the pause counters decrement time from 512 bit times, to every `rx_clk` cycle.

- **PAE: Pause Enable**

When set, transmission pauses when a valid pause frame is received.

- **RBOF: Receive Buffer Offset**

Indicates the number of bytes by which the received data is offset from the start of the first receive buffer.

RBOF	Offset
00	No offset from start of receive buffer
01	One-byte offset from start of receive buffer
10	Two-byte offset from start of receive buffer
11	Three-byte offset from start of receive buffer

- **RLCE: Receive Length field Checking Enable**

When set, frames with measured lengths shorter than their length fields are discarded. Frames containing a type ID in bytes 13 and 14 — length/type ID = 0600 — are not be counted as length errors.

- **DRFCS: Discard Receive FCS**

When set, the FCS field of received frames will not be copied to memory.

- **EFRHD:**

Enable Frames to be received in half-duplex mode while transmitting.

- **IRXFCS: Ignore RX FCS**

When set, frames with FCS/CRC errors are not rejected and no FCS error statistics are counted. For normal operation, this bit must be set to 0.

31.7.3 Network Status Register

Register Name: NSR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	IDLE	MDIO	-

- **MDIO**

Returns status of the mdio_in pin. Use the PHY maintenance register for reading managed frames rather than this bit.

- **IDLE**

0 = The PHY logic is running.

1 = The PHY management logic is idle (i.e., has completed).

31.7.4 Transmit Status Register

Register Name: TSR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	UND	COMP	BEX	TGO	RLE	COL	UBR

This register, when read, provides details of the status of a transmit. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.

- **UBR: Used Bit Read**

Set when a transmit buffer descriptor is read with its used bit set. Cleared by writing a one to this bit.

- **COL: Collision Occurred**

Set by the assertion of collision. Cleared by writing a one to this bit.

- **RLE: Retry Limit exceeded**

Cleared by writing a one to this bit.

- **TGO: Transmit Go**

If high transmit is active.

- **BEX: Buffers exhausted mid frame**

If the buffers run out during transmission of a frame, then transmission stops, FCS shall be bad and tx_er asserted. Cleared by writing a one to this bit.

- **COMP: Transmit Complete**

Set when a frame has been transmitted. Cleared by writing a one to this bit.

- **UND: Transmit Underrun**

Set when transmit DMA was not able to read data from memory, either because the bus was not granted in time, because a not OK `hresp(bus error)` was returned or because a used bit was read midway through frame transmission. If this occurs, the transmitter forces `bad` CRC. Cleared by writing a one to this bit.

31.7.5 Receive Buffer Queue Pointer Register

Register Name: RBQP

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR						–	–

This register points to the entry in the receive buffer queue (descriptor list) currently being used. It is written with the start location of the receive buffer descriptor list. The lower order bits increment as buffers are used up and wrap to their original values after either 1024 buffers or when the wrap bit of the entry is set.

Reading this register returns the location of the descriptor currently being accessed. This value increments as buffers are used. Software should not use this register for determining where to remove received frames from the queue as it constantly changes as new frames are received. Software should instead work its way through the buffer descriptor queue checking the used bits.

Receive buffer writes also comprise bursts of two words and, as with transmit buffer reads, it is recommended that bit 2 is always written with zero to prevent a burst crossing a 1K boundary, in violation of the System Bus specification.

- **ADDR: Receive buffer queue pointer address**

Written with the address of the start of the receive queue, reads as a pointer to the current buffer being used.

31.7.6 Transmit Buffer Queue Pointer Register

Register Name: TBQP

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR						–	–

This register points to the entry in the transmit buffer queue (descriptor list) currently being used. It is written with the start location of the transmit buffer descriptor list. The lower order bits increment as buffers are used up and wrap to their original values after either 1024 buffers or when the wrap bit of the entry is set. This register can only be written when bit 3 in the transmit status register is low.

As transmit buffer reads consist of bursts of two words, it is recommended that bit 2 is always written with zero to prevent a burst crossing a 1K boundary, in violation of the System Bus specification.

- **ADDR: Transmit buffer queue pointer address**

Written with the address of the start of the transmit queue, reads as a pointer to the first buffer of the frame being transmitted or about to be transmitted.

31.7.7 Receive Status Register

Register Name: RSR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	OVR	REC	BNA

This register, when read, provides details of the status of a receive. Once read, individual bits may be cleared by writing 1 to them. It is not possible to set a bit to 1 by writing to the register.

- **BNA: Buffer Not Available**

An attempt was made to get a new buffer and the pointer indicated that it was owned by the processor. The DMA rereads the pointer each time a new frame starts until a valid pointer is found. This bit is set at each attempt that fails even if it has not had a successful pointer read since it has been cleared.

Cleared by writing a one to this bit.

- **REC: Frame Received**

One or more frames have been received and placed in memory. Cleared by writing a one to this bit.

- **OVR: Receive Overrun**

The DMA block was unable to store the receive frame to memory, either because the bus was not granted in time or because a not OK `hresp(bus error)` was returned. The buffer is recovered if this happens.

Cleared by writing a one to this bit.

31.7.8 Interrupt Status Register

Register Name: ISR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	PTZ	PFR	HRESP	ROVR	-	–
7	6	5	4	3	2	1	0
TCOMP	TXERR	RLE	TUND	TXUBR	RXUBR	RCOMP	MFD

- **MFD: Management Frame Done**

The PHY maintenance register has completed its operation. Cleared on read.

- **RCOMP: Receive Complete**

A frame has been stored in memory. Cleared on read.

- **RXUBR: Receive Used Bit Read**

Set when a receive buffer descriptor is read with its used bit set. Cleared on read.

- **TXUBR: Transmit Used Bit Read**

Set when a transmit buffer descriptor is read with its used bit set. Cleared on read.

- **TUND: Ethernet Transmit Buffer Underrun**

The transmit DMA did not fetch frame data in time for it to be transmitted or `hresp` returned not OK. Also set if a used bit is read mid-frame or when a new transmit queue pointer is written. Cleared on read.

- **RLE: Retry Limit Exceeded**

Cleared on read.

- **TXERR: Transmit Error**

Transmit buffers exhausted in mid-frame - transmit error. Cleared on read.

- **TCOMP: Transmit Complete**

Set when a frame has been transmitted. Cleared on read.

- **ROVR: Receive Overrun**

Set when the receive overrun status bit gets set. Cleared on read.

- **HRESP: Hresp not OK**

Set when the DMA block sees `a bus error`. Cleared on read.

- **PFR: Pause Frame Received**

Indicates a valid pause has been received. Cleared on a read.

- **PTZ: Pause Time Zero**

Set when the pause time register, 0x38 decrements to zero. Cleared on a read.

31.7.9 Interrupt Enable Register

Register Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	PTZ	PFR	HRESP	ROVR		–

7	6	5	4	3	2	1	0
TCOMP	TXERR	RLE	TUND	TXUBR	RXUBR	RCOMP	MFD

- **MFD: Management Frame sent**

Enable management done interrupt.

- **RCOMP: Receive Complete**

Enable receive complete interrupt.

- **RXUBR: Receive Used Bit Read**

Enable receive used bit read interrupt.

- **TXUBR: Transmit Used Bit Read**

Enable transmit used bit read interrupt.

- **TUND: Ethernet Transmit Buffer Underrun**

Enable transmit underrun interrupt.

- **RLE: Retry Limit Exceeded**

Enable retry limit exceeded interrupt.

- **TXERR: Transmit Error**

Enable transmit buffers exhausted in mid-frame interrupt.

- **TCOMP: Transmit Complete**

Enable transmit complete interrupt.

- **ROVR: Receive Overrun**

Enable receive overrun interrupt.

- **HRESP: Hresp not OK**

Enable Hresp not OK interrupt.

- **PFR: Pause Frame Received**

Enable pause frame received interrupt.

- **PTZ: Pause Time Zero**

Enable pause time zero interrupt.

31.7.10 Interrupt Disable Register

Register Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	PTZ	PFR	HRESP	ROVR	-	–
7	6	5	4	3	2	1	0
TCOMP	TXERR	RLE	TUND	TXUBR	RXUBR	RCOMP	MFD

- **MFD: Management Frame sent**

Disable management done interrupt.

- **RCOMP: Receive Complete**

Disable receive complete interrupt.

- **RXUBR: Receive Used Bit Read**

Disable receive used bit read interrupt.

- **TXUBR: Transmit Used Bit Read**

Disable transmit used bit read interrupt.

- **TUND: Ethernet Transmit Buffer Underrun**

Disable transmit underrun interrupt.

- **RLE: Retry Limit Exceeded**

Disable retry limit exceeded interrupt.

- **TXERR: Transmit Error**

Disable transmit buffers exhausted in mid-frame interrupt.

- **TCOMP: Transmit Complete**

Disable transmit complete interrupt.

- **ROVR: Receive Overrun**

Disable receive overrun interrupt.

- **HRESP: Hresp not OK**

Disable Hresp not OK interrupt.

- **PFR: Pause Frame Received**

Disable pause frame received interrupt.

- **PTZ: Pause Time Zero**

Disable pause time zero interrupt.

31.7.11 Interrupt Mask Register

Register Name: IMR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	PTZ	PFR	HRESP	ROVR	-	–
7	6	5	4	3	2	1	0
TCOMP	TXERR	RLE	TUND	TXUBR	RXUBR	RCOMP	MFD

- **MFD: Management Frame sent**

Management done interrupt masked.

- **RCOMP: Receive Complete**

Receive complete interrupt masked.

- **RXUBR: Receive Used Bit Read**

Receive used bit read interrupt masked.

- **TXUBR: Transmit Used Bit Read**

Transmit used bit read interrupt masked.

- **TUND: Ethernet Transmit Buffer Underrun**

Transmit underrun interrupt masked.

- **RLE: Retry Limit Exceeded**

Retry limit exceeded interrupt masked.

- **TXERR: Transmit Error**

Transmit buffers exhausted in mid-frame interrupt masked.

- **TCOMP: Transmit Complete**

Transmit complete interrupt masked.

- **ROVR: Receive Overrun**

Receive overrun interrupt masked.

- **HRESP: Hresp not OK**

Hresp not OK interrupt masked.

- **PFR: Pause Frame Received**

Pause frame received interrupt masked.

- **PTZ: Pause Time Zero**

Pause time zero interrupt masked.

31.7.12 PHY Maintenance Register

Register Name: MAN

Access Type: Read/Write

31	30	29	28	27	26	25	24
SOF		RW		PHYA			

23	22	21	20	19	18	17	16
PHYA		REGA				CODE	

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA**

For a write operation this is written with the data to be written to the PHY.

After a read operation this contains the data read from the PHY.

- **CODE:**

Must be written to 10. Reads as written.

- **REGA: Register Address**

Specifies the register in the PHY to access.

- **PHYA: PHY Address**

- **RW: Read/Write**

10 is read; 01 is write. Any other value is an invalid PHY management frame

- **SOF: Start of frame**

Must be written 01 for a valid frame.

31.7.13 Pause Time Register

Register Name: PTR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
PTIME							

7	6	5	4	3	2	1	0
PTIME							

- **PTIME: Pause Time**

Stores the current value of the pause time register which is decremented every 512 bit times.

31.7.14 Hash Register Bottom

Register Name: HRB

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

- **ADDR:**

Bits 31:0 of the hash address register. See ”Hash Addressing” on page 616.

31.7.15 Hash Register Top

Register Name: HRT

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

- **ADDR:**

Bits 63:32 of the hash address register. See ”Hash Addressing” on page 616.

31.7.16 Specific Address 1 Bottom Register

Register Name: SA1B

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

Least significant bits of the destination address. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

31.7.17 Specific Address 1 Top Register

Register Name: SA1T

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

The most significant bits of the destination address, that is bits 47 to 32.

31.7.18 Specific Address 2 Bottom Register

Register Name: SA2B

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

Least significant bits of the destination address. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

31.7.19 Specific Address 2 Top Register

Register Name: SA2T

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

The most significant bits of the destination address, that is bits 47 to 32.

31.7.20 Specific Address 3 Bottom Register

Register Name: SA3B

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

Least significant bits of the destination address. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

31.7.21 Specific Address 3 Top Register

Register Name: SA3T

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

The most significant bits of the destination address, that is bits 47 to 32.

31.7.22 Specific Address 4 Bottom Register

Register Name: SA4B

Access Type: Read/Write

31	30	29	28	27	26	25	24
ADDR							
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

Least significant bits of the destination address. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

31.7.23 Specific Address 4 Top Register

Register Name: SA4T

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

- **ADDR**

The most significant bits of the destination address, that is bits 47 to 32.

31.7.24 Type ID Checking Register

Register Name: TID

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TID							

7	6	5	4	3	2	1	0
TID							

- **TID: Type ID checking**

For use in comparisons with received frames TypeID/Length field.

31.7.25 Transmit Pause Quantum Register

Register Name: TPQ

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
TPQ							
7	6	5	4	3	2	1	0
TPQ							

- **TPQ: Transmit Pause Quantum**

Used in hardware generation of transmitted pause frames as value for pause quantum.

31.7.26 User Input/Output Register

Register Name: USRIO

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	TX_PAUSE_ ZERO	TX_PAUSE	EAM	RMII

- **RMII**

When set, this bit enables the MII operation mode. When reset, it selects the RMII mode.

- **EAM**

When set, this bit causes a frame to be copied to memory, if this feature is enabled by the EAE bit in NCFGR. Otherwise, no frame is copied.

- **TX_PAUSE**

Toggling this bit causes a PAUSE frame to be transmitted.

- **TX_PAUSE_ZERO**

Selects either zero or the transmit quantum register as the transmitted pause frame quantum.

31.7.27 Wake-on-LAN Register

Register Name: WOL

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	MTI	SA1	ARP	MAG

15	14	13	12	11	10	9	8
IP							

7	6	5	4	3	2	1	0
IP							

- **IP: ARP request IP address**

Written to define the least significant 16 bits of the target IP address that is matched to generate a Wake-on-LAN event. A value of zero does not generate an event, even if this is matched by the received frame.

- **MAG: Magic packet event enable**

When set, magic packet events causes the `wol` output to be asserted.

- **ARP: ARP request event enable**

When set, ARP request events causes the `wol` output to be asserted.

- **SA1: Specific address register 1 event enable**

When set, specific address 1 events causes the `wol` output to be asserted.

- **MTI: Multicast hash event enable**

When set, multicast hash events causes the `wol` output to be asserted.

31.7.28 MACB Statistic Registers

These registers reset to zero on a read and stick at all ones when they count to their maximum value. They should be read frequently enough to prevent loss of data. The receive statistics registers are only incremented when the receive enable bit is set in the network control register. To write to these registers, bit 7, WESTAT, in the network control register, NCR, must be set. The statistics register block contains the following registers.

31.7.28.1 Pause Frames Received Register

Register Name: PFR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
FROK							
7	6	5	4	3	2	1	0
FROK							

- **FROK: Pause Frames received OK**

A 16-bit register counting the number of good pause frames received. A good frame has a length of 64 to 1518 (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set) and has no FCS, alignment or receive symbol errors.

31.7.28.2 Frames Transmitted OK Register

Register Name: FTO

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
FTOK							
15	14	13	12	11	10	9	8
FTOK							
7	6	5	4	3	2	1	0
FTOK							

- **FTOK: Frames Transmitted OK**

A 24-bit register counting the number of frames successfully transmitted, i.e., no underrun and not too many retries.

31.7.28.3 Single Collision Frames Register

Register Name: SCF

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
SCF							
7	6	5	4	3	2	1	0
SCF							

- **SCF: Single Collision Frames**

A 16-bit register counting the number of frames experiencing a single collision before being successfully transmitted, i.e., no underrun.

31.7.28.4 Multicollision Frames Register

Register Name: MCF

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
MCF							
7	6	5	4	3	2	1	0
MCF							

- **MCF: Multicollision Frames**

A 16-bit register counting the number of frames experiencing between two and fifteen collisions prior to being successfully transmitted, i.e., no underrun and not too many retries.

31.7.28.5 Frames Received OK Register

Register Name: FRO

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
FROK							
15	14	13	12	11	10	9	8
FROK							
7	6	5	4	3	2	1	0
FROK							

- **FROK: Frames Received OK**

A 24-bit register counting the number of good frames received, i.e., address recognized and successfully copied to memory. A good frame is of length 64 to 1518 bytes (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set) and has no FCS, alignment or receive symbol errors.

31.7.28.6 Frames Check Sequence Errors Register

Register Name: FCSE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
FCSE							

- **FCSE: Frame Check Sequence Errors**

An 8-bit register counting frames that are an integral number of bytes, have bad CRC and are between 64 and 1518 bytes in length (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set). This register is also incremented if a symbol error is detected and the frame is of valid length and has an integral number of bytes.

31.7.28.7 Alignment Errors Register

Register Name: ALE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
ALE							

- **ALE: Alignment Errors**

An 8-bit register counting frames that are not an integral number of bytes long and have bad CRC when their length is truncated to an integral number of bytes and are between 64 and 1518 bytes in length (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set). This register is also incremented if a symbol error is detected and the frame is of valid length and does not have an integral number of bytes.

31.7.28.8 Deferred Transmission Frames Register

Register Name: DTF

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
DTF							
7	6	5	4	3	2	1	0
DTF							

- **DTF: Deferred Transmission Frames**

A 16-bit register counting the number of frames experiencing deferral due to carrier sense being active on their first attempt at transmission. Frames involved in any collision are not counted nor are frames that experienced a transmit underrun.

31.7.28.9 Late Collisions Register

Register Name: LCOL

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
LCOL							

- **LCOL: Late Collisions**

An 8-bit register counting the number of frames that experience a collision after the slot time (512 bits) has expired. A late collision is counted twice; i.e., both as a collision and a late collision.

31.7.28.10 Excessive Collisions Register

Register Name: EXCOL

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
EXCOL							

- **EXCOL: Excessive Collisions**

An 8-bit register counting the number of frames that failed to be transmitted because they experienced 16 collisions.

31.7.28.11 Transmit Underrun Errors Register

Register Name: TUND

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
TUND							

- **TUND: Transmit Underruns**

An 8-bit register counting the number of frames not transmitted due to a transmit DMA underrun. If this register is incremented, then no other statistics register is incremented.

31.7.28.12 Carrier Sense Errors Register

Register Name: CSE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
CSE							

- **CSE: Carrier Sense Errors**

An 8-bit register counting the number of frames transmitted where carrier sense was not seen during transmission or where carrier sense was deasserted after being asserted in a transmit frame without collision (no underrun). Only incremented in half-duplex mode. The only effect of a carrier sense error is to increment this register. The behavior of the other statistics registers is unaffected by the detection of a carrier sense error.

31.7.28.13 Receive Resource Errors Register

Register Name: RRE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
RRE							
7	6	5	4	3	2	1	0
RRE							

- **RRE: Receive Resource Errors**

A 16-bit register counting the number of frames that were address matched but could not be copied to memory because no receive buffer was available.

31.7.28.14 Receive Overrun Errors Register

Register Name: ROVR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
ROVR							

- **ROVR: Receive Overrun**

An 8-bit register counting the number of frames that are address recognized but were not copied to memory due to a receive DMA overrun.

31.7.28.15 Receive Symbol Errors Register

Register Name: RSE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RSE							

- **RSE: Receive Symbol Errors**

An 8-bit register counting the number of frames that had `rx_er` asserted during reception. Receive symbol errors are also counted as an FCS or alignment error if the frame is between 64 and 1518 bytes in length (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set). If the frame is larger, it is recorded as a jabber error.

31.7.28.16 Excessive Length Errors Register

Register Name: ELE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
EXL							

- **EXL: Excessive Length Errors**

An 8-bit register counting the number of frames received exceeding 1518 bytes (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set) in length but do not have either a CRC error, an alignment error nor a receive symbol error.

31.7.28.17 Receive Jabbers Register

Register Name: RJA

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RJB							

- **RJB: Receive Jabbers**

An 8-bit register counting the number of frames received exceeding 1518 bytes (1536 if bit 8, BIG, in network configuration register, NCFGR, is set, 10240 if bit 3, JFRAME in network configuration register, NCFGR, is set) in length and have either a CRC error, an alignment error or a receive symbol error.

31.7.28.18 Undersize Frames Register

Register Name: USF

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
USF							

- **USF: Undersize frames**

An 8-bit register counting the number of frames received less than 64 bytes in length but do not have either a CRC error, an alignment error or a receive symbol error.

31.7.28.19 SQE Test Errors Register

Register Name: STE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SQER							

- **SQER: SQE test errors**

An 8-bit register counting the number of frames where `col` was not asserted within 96 bit times (an interframe gap) of `tx_en` being deasserted in half duplex mode.

31.7.28.20 Received Length Field Mismatch Register

Register Name: RLE

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RLFM							

- **RLFM: Receive Length Field Mismatch**

An 8-bit register counting the number of frames received that have a measured length shorter than that extracted from its length field. Checking is enabled through bit 16 of the network configuration register. Frames containing a type ID in bytes 13 and 14 (i.e., length/type ID □ 0x0600) are not counted as length field errors, neither are excessive length frames.

31.7.28.21 Transmitted Pause Frames Register

Register Name: TPF

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TPF							

7	6	5	4	3	2	1	0
TPF							

- **TPF: Transmitted Pause Frames**

A 16-bit register counting the number of pause frames transmitted.

32. Hi-Speed USB Interface (USBA)

Rev: 1.4.0.2

32.1 Features

- **Supports Hi (480Mbps) and Full (12Mbps) speed communication**
- **Compatible with the USB 2.0 specification**
- **UTMI Compliant**
- **7 Endpoints**
- **Embedded Dual-port RAM for Endpoints**
- **Suspend/Resume Logic (Command of UTMI)**
- **Up to Three Memory Banks for Endpoints (Not for Control Endpoint)**
- **4 KBytes of DPRAM**

32.2 Description

The USB High Speed Device (USBA) is compliant with the Universal Serial Bus (USB), rev 2.0 High Speed device specification.

Each endpoint can be configured in one of several USB transfer types. It can be associated with one, two or three banks of a dual-port RAM used to store the current data payload. If two or three banks are used, one DPR bank is read or written by the processor, while the other is read or written by the USB device peripheral. This feature is mandatory for isochronous endpoints.

Table 32-1. USBA Endpoint Description

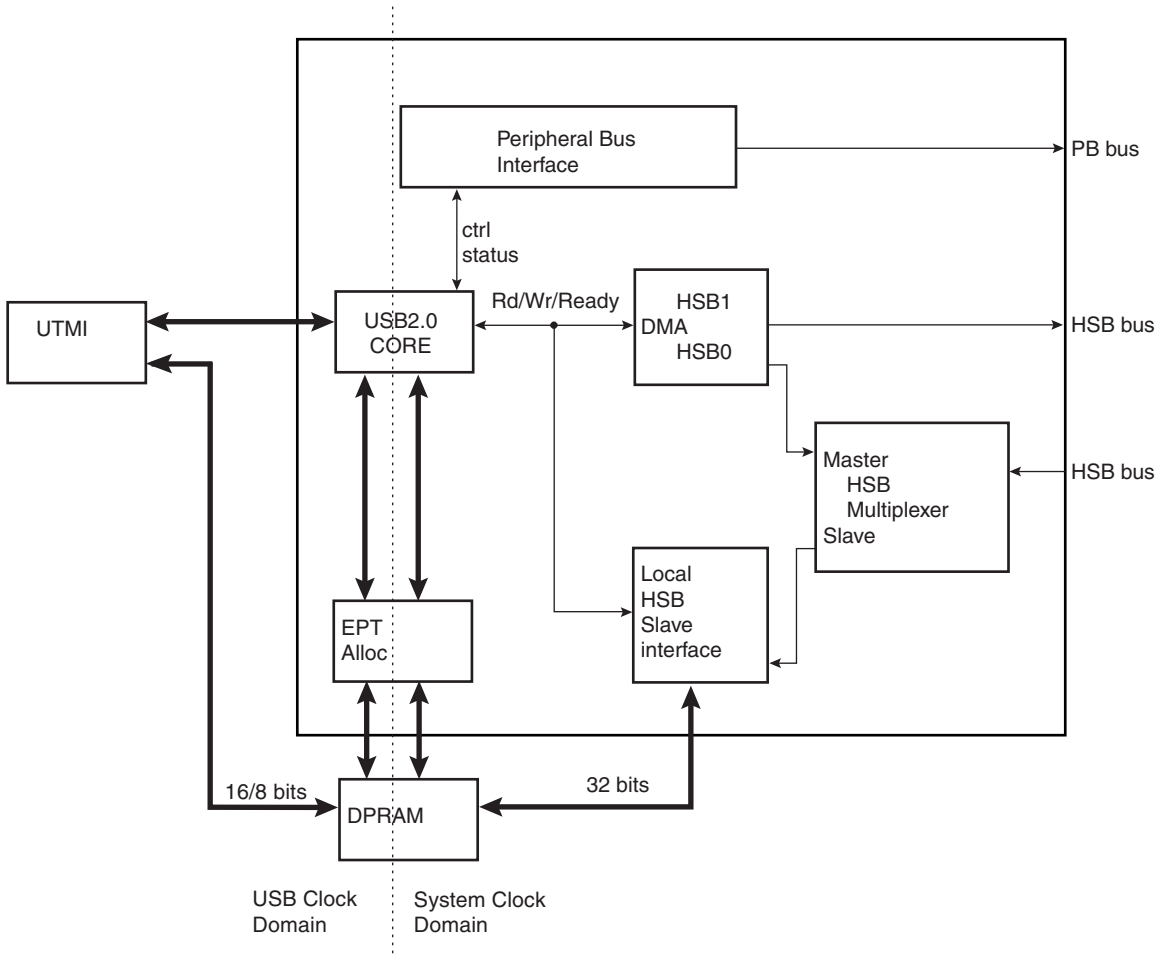
Endpoint #	Mnemonic	Nb Bank	DMA	High Band Width	Max. Endpoint Size	Endpoint Type	Offset
0	EP0	1	N	N	64	Control	0x00000
1	EP1	2	Y	Y	512	Ctrl/Bulk/Iso/Interrupt	0x10000
2	EP2	2	Y	Y	512	Ctrl/Bulk/Iso/Interrupt	0x20000
3	EP3	3	Y	N	64	Ctrl/Bulk/Interrupt	0x30000
4	EP4	3	Y	N	64	Ctrl/Bulk/Interrupt	0x40000
5	EP5	3	Y	Y	1024	Ctrl/Bulk/Iso/Interrupt	0x50000
6	EP6	3	Y	Y	1024	Ctrl/Bulk/Iso/Interrupt	0x60000

The default size of the DPRAM is 4 KB.

Suspend and resume are automatically detected by the USBA device, which notifies the processor by raising an interrupt.

32.3 Block Diagram

Figure 32-1. Block diagram:



32.4 Product Dependencies

32.4.1 Power Management

The USBA clock is generated by the Power Manager. Before using the USBA, the programmer must ensure that the USBA clock is enabled in the Power Manager.

To prevent bus errors the USBA operation must be terminated before entering sleep mode.

The USB HS PHY clock has to be enabled before using the USBA. The description of this clock can be found in the Peripherals chapter under Clock Connections.

32.4.2 Interrupt

The USBA interface has an interrupt line connected to the Interrupt Controller. Handling the USBA interrupt requires programming the interrupt controller before configuring the USBA.

32.5 Typical Connection

Figure 32-2. Board Schematic

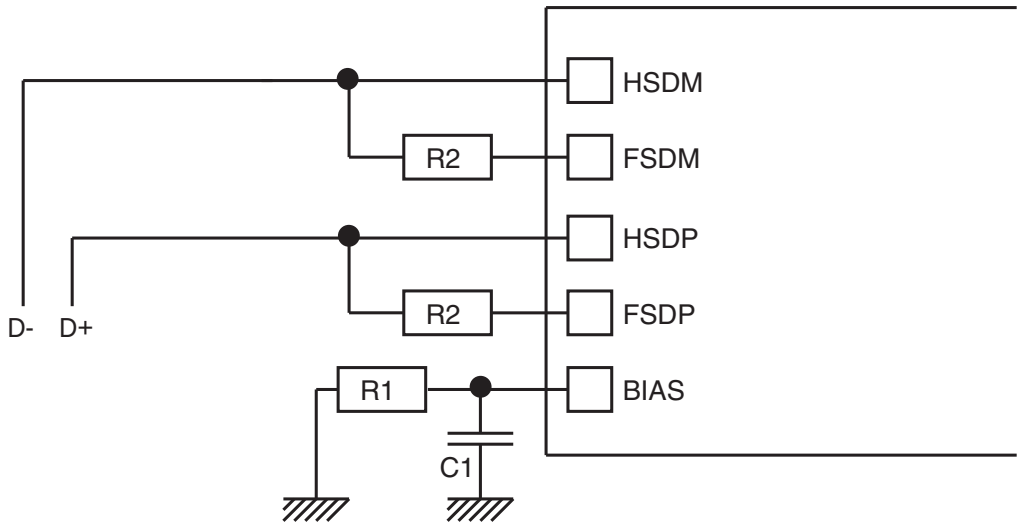


Table 32-2. Components Typical Values

Symbol	Value	Unit
R1	6.8 ± 1%	kΩ
R2	39 ± 1%	Ω
C1	10	pF

32.6 USB V2.0 High Speed Device Introduction

The USB V2.0 High Speed Device provides communication services to/from host when attached. Each device is offered with a collection of communication flows (pipes) associated with each endpoint. Software on the host communicates with a USB Device through a set of communication flows.

32.6.1 USB V2.0 High Speed Transfer Types

A communication flow is carried over one of four transfer types defined by the USB device.

A device provides several logical communication pipes with the host. To each logical pipe is associated an endpoint. Transfer through a pipe belongs to one of the four transfer types:

- Control Transfers: Used to configure a device at attach time and can be used for other device-specific purposes, including control of other pipes on the device.
- Bulk Data Transfers: Generated or consumed in relatively large burst quantities and have wide dynamic latitude in transmission constraints.
- Interrupt Data Transfers: Used for timely but reliable delivery of data, for example, characters or coordinates with human-perceptible echo or feedback response characteristics.
- Isochronous Data Transfers: Occupy a prenegotiated amount of USB bandwidth with a prenegotiated delivery latency. (Also called streaming real time transfers.)

As indicated below, transfers are sequential events carried out on the USB bus.

Endpoints must be configured according to the transfer type they handle.

Table 32-3. USB Communication Flow

Transfer	Direction	Bandwidth	Endpoint Size	Error Detection	Retrying
Control	Bidirectional	Not guaranteed	8,16,32,64	Yes	Automatic
Isochronous	Unidirectional	Guaranteed	8-1024	Yes	No
Interrupt	Unidirectional	Not guaranteed	8-1024	Yes	Yes
Bulk	Unidirectional	Not guaranteed	8-512	Yes	Yes

32.6.2 USB Transfer Event Definitions

A transfer is composed of one or several transactions;

Table 32-4. USB Transfer Events

CONTROL (bidirectional)	Control Transfers [1]	• Setup transaction > Data IN transactions > Status OUT transaction • Setup transaction > Data OUT transactions > Status IN transaction • Setup transaction > Status IN transaction
IN (device toward host)	Bulk IN Transfer	• Data IN transaction > Data IN transaction
	Interrupt IN Transfer	• Data IN transaction > Data IN transaction
	Isochronous IN Transfer [2]	• Data IN transaction > Data IN transaction
OUT (host toward device)	Bulk OUT Transfer	• Data OUT transaction > Data OUT transaction
	Interrupt OUT Transfer	• Data OUT transaction > Data OUT transaction
	Isochronous OUT Transfer [2]	• Data OUT transaction > Data OUT transaction

Notes: 1. Control transfer must use endpoints with one bank and can be aborted using a stall handshake.
2. Isochronous transfers must use endpoints configured with two or three banks.

An endpoint handles all transactions related to the type of transfer for which it has been configured.

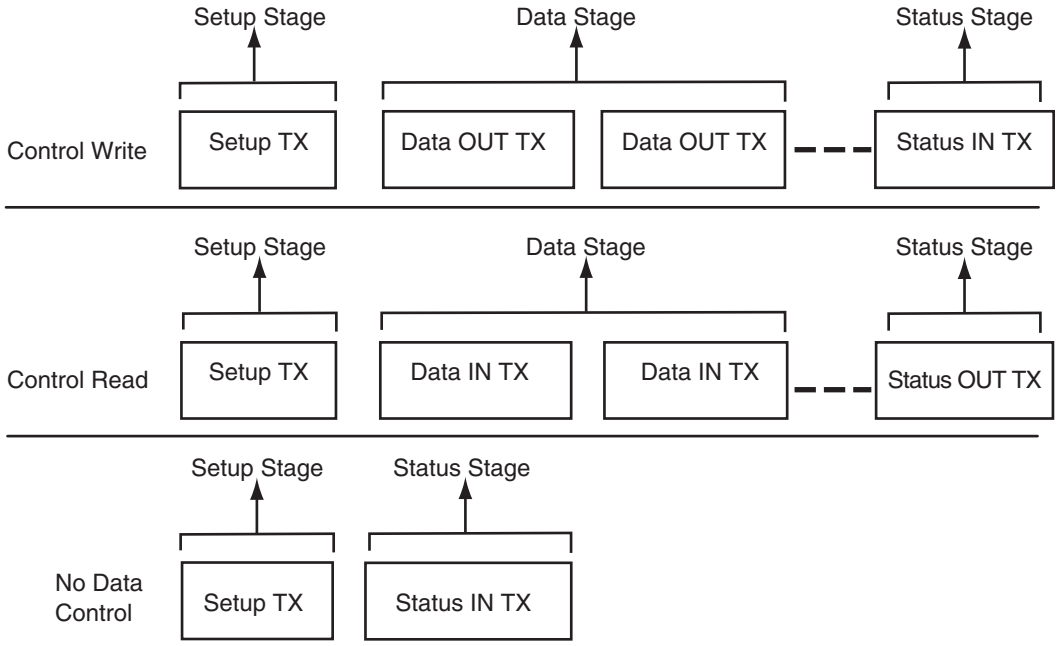
32.6.3 USB V2.0 High Speed BUS Transactions

Each transfer results in one or more transactions over the USB bus.

There are five kinds of transactions flowing across the bus in packets:

1. Setup Transaction
2. Data IN Transaction
3. Data OUT Transaction
4. Status IN Transaction
5. Status OUT Transaction

Figure 32-3. Control Read and Write Sequences



A status IN or OUT transaction is identical to a data IN or OUT transaction.

32.6.4 Endpoint Configuration

The endpoint 0 is always a control endpoint, it must be programmed and active in order to be enabled when the End Of Reset interrupt occurs.

To configure the endpoints:

- Fill the configuration register (EPTCFG) with the endpoint size, direction (IN or OUT), type (CTRL, Bulk, IT, ISO) and the number of banks.
- Fill the number of transactions (NB_TRANS) for isochronous endpoints.

Note: For control endpoints the direction has no effect.

- Verify that the EPT_MAPD flag is set. This flag is set if the endpoint size and the number of banks are correct compared to the FIFO maximum capacity and the maximum number of allowed banks.
- Configure control flags of the endpoint and enable it in EPTCTLENBx according to "USBA Endpoint Control Register" on page 722.

Control endpoints can generate interrupts and use only 1 bank.

All endpoints (except endpoint 0) can be configured either as Bulk, Interrupt or Isochronous. See Table 32-1. USBA Endpoint Description.

The maximum packet size they can accept corresponds to the maximum endpoint size.

Note: The endpoint size of 1024 is reserved for isochronous endpoints.

The size of the DPRAM is 4 KB. The DPR is shared by all active endpoints. The memory size required by the active endpoints must not exceed the size of the DPRAM.

SIZE_DPRAM = SIZE _EPT0

+ NB_BANK_EPT1 x SIZE_EPT1

+ NB_BANK_EPT2 x SIZE_EPT2

+ NB_BANK_EPT3 x SIZE_EPT3

+ NB_BANK_EPT4 x SIZE_EPT4

+ NB_BANK_EPT5 x SIZE_EPT5

+ NB_BANK_EPT6 x SIZE_EPT6

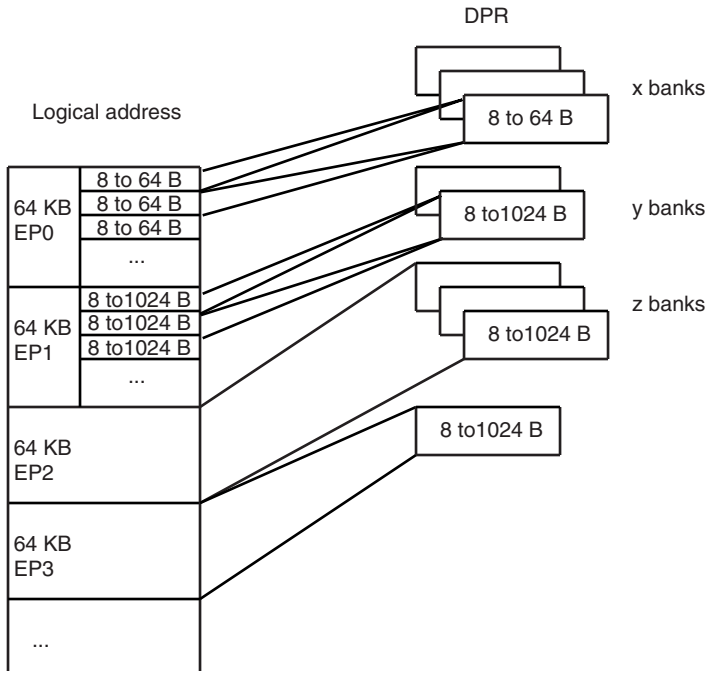
+... (refer to 32.7.17 USBA Endpoint Configuration Register)

If a user tries to configure endpoints with a size the sum of which is greater than the DPRAM, then the EPT_MAPD is not set.

The application has access to the physical block of DPR reserved for the endpoint through a 64 KB logical address space.

The physical block of DPR allocated for the endpoint is remapped all along the 64 KB logical address space. The application can write a 64 KB buffer linearly.

Figure 32-4. Logical Address Space for DPR Access:



Configuration examples of EPTCTLx (USBA Endpoint Control Register) for Bulk IN endpoint type follow below.

- With DMA
  - AUTO_VALID: Automatically validate the packet and switch to the next bank.
  - EPT_ENABL: Enable endpoint.
- Without DMA:
  - TX_BK_RDY: An interrupt is generated after each transmission.
  - EPT_ENABL: Enable endpoint.

Configuration examples of Bulk OUT endpoint type follow below.

- With DMA
  - AUTO_VALID: Automatically validate the packet and switch to the next bank.
  - EPT_ENABL: Enable endpoint.
- Without DMA
  - RX_BK_RDY: An interrupt is sent after a new packet has been stored in the endpoint FIFO.
  - EPT_ENABL: Enable endpoint.

32.6.5 DMA

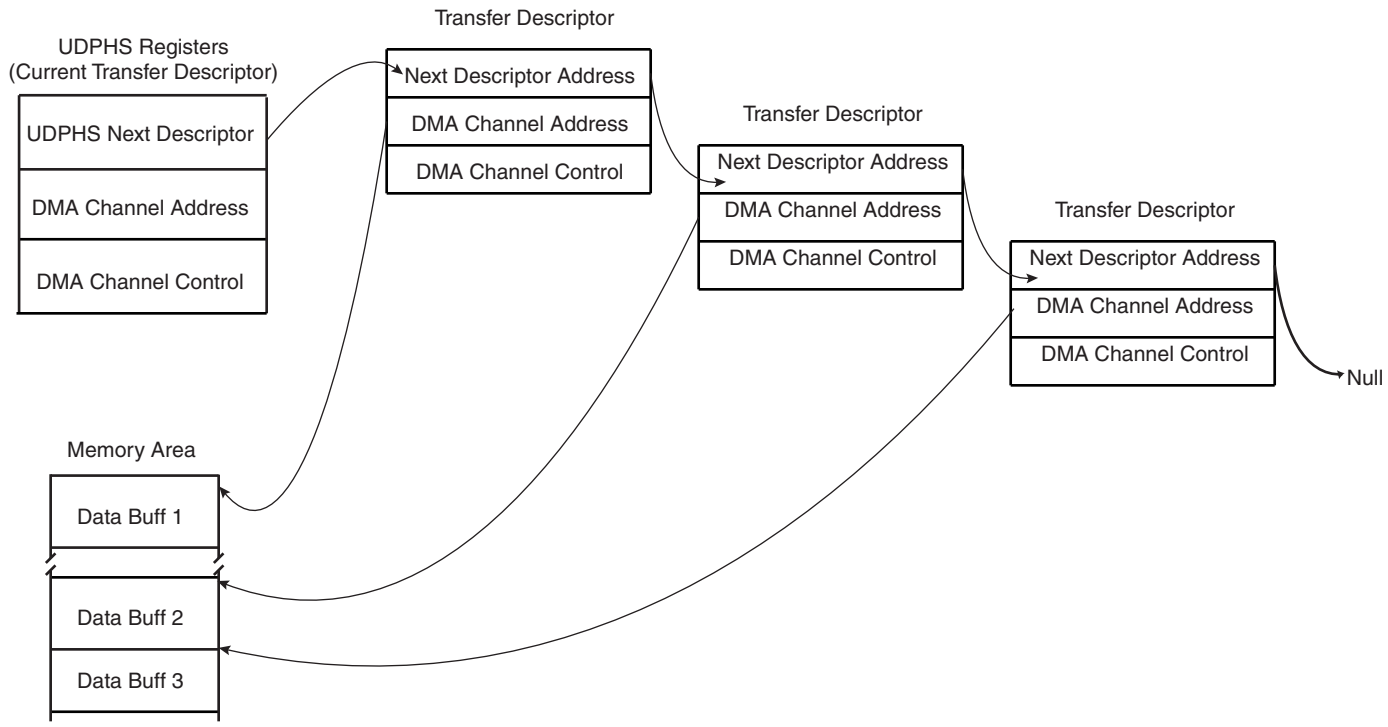
USB packets of any length may be transferred when required by the USBA Device. These transfers always feature sequential addressing.

Packet data HSB bursts may be locked on a DMA buffer basis for drastic overall HSB bus bandwidth performance boost with paged memories. These clock-cycle consuming memory row (or bank) changes will then likely not occur, or occur only once instead of dozens times, during a single big USB packet DMA transfer in case another HSB master addresses the memory. This means up to 128-word single-cycle unbroken HSB bursts for Bulk endpoints and 256-word single-cycle unbroken bursts for isochronous endpoints. This maximum burst length is then controlled by the lowest programmed USB endpoint size (EPT_SIZE bit in the EPTCFGx register) and DMA Size (BUFF_LENGTH bit in the DMACONTROLx register).

The USBA device average throughput may be up to nearly 60 MBytes. Its internal slave average access latency decreases as burst length increases due to the 0 wait-state side effect of unchanged endpoints. If at least 0 wait-state word burst capability is also provided by the external DMA HSB bus slaves, each of both DMA HSB busses need less than 50% bandwidth allocation for full USBA bandwidth usage at 30 MHz, and less than 25% at 60 MHz.

The USBA DMA Channel Transfer Descriptor is described in "USBA DMA Channel Transfer Descriptor" on page 733

Figure 32-5. Example of DMA Chained List:



32.6.6 Handling Transactions with USB V2.0 Device Peripheral

32.6.6.1 Setup Transaction

The setup packet is valid in the DPR while RX_SETUP is set. Once RX_SETUP is cleared by the application, the USBA accepts the next packets sent over the device endpoint.

When a valid setup packet is accepted by the USBA:

- the USBA device automatically acknowledges the setup packet (sends an ACK response)
- payload data is written in the endpoint
- sets the RX_SETUP interrupt
- the BYTE_COUNT field in the EPTSTAx register is updated

An endpoint interrupt is generated while RX_SETUP in the EPTSTAx register is not cleared. This interrupt is carried out to the microcontroller if interrupts are enabled for this endpoint.

Thus, firmware must detect RX_SETUP polling EPTSTAx or catching an interrupt, read the setup packet in the FIFO, then clear the RX_SETUP bit in the EPTCLRSTA register to acknowledge the setup stage.

If STALL_SNT was set to 1, then this bit is automatically reset when a setup token is detected by the device. Then, the device still accepts the setup stage. (See Section 32.6.6.15 ”STALL” on page 686).

32.6.6.2 NYET

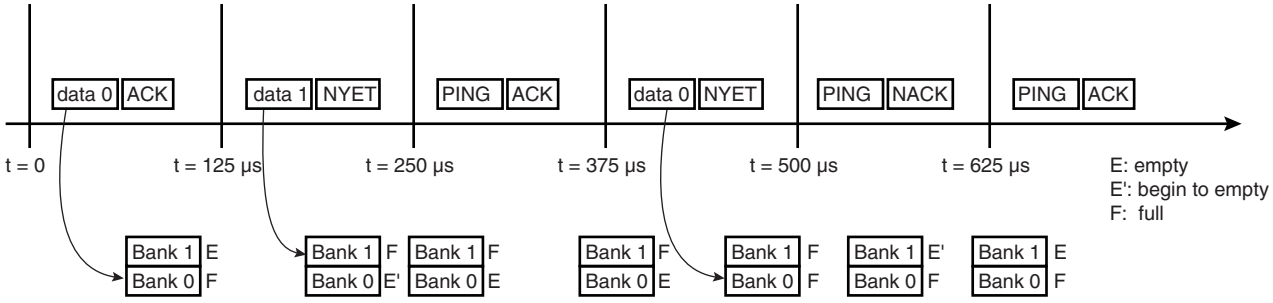
NYET is a High Speed only handshake. It is returned by a High Speed endpoint as part of the PING protocol.

High Speed devices must support an improved NAK mechanism for Bulk OUT and control endpoints (except setup stage). This mechanism allows the device to tell the host whether it has sufficient endpoint space for the next OUT transfer (see USB 2.0 spec 8.5.1 NAK Limiting via Ping Flow Control).

The NYET/ACK response to a High Speed Bulk OUT transfer and the PING response are automatically handled by hardware in the EPTCTLx register (except when the user wants to force a NAK response by using the NYET_DIS bit).

If the endpoint responds instead to the OUT/DATA transaction with an NYET handshake, this means that the endpoint accepted the data but does not have room for another data payload. The host controller must return to using a PING token until the endpoint indicates it has space available.

Figure 32-6. NYET Example with Two Endpoint Banks



32.6.6.3 Data IN

32.6.6.4 Bulk IN or Interrupt IN

Data IN packets are sent by the device during the data or the status stage of a control transfer or during an (interrupt/bulk/isochronous) IN transfer. Data buffers are sent packet by packet under the control of the application or under the control of the DMA channel.

There are three ways for an application to transfer a buffer in several packets over the USB:

- packet by packet (see 32.6.6.5 below)
- 64 KB (see 32.6.6.5 below)
- DMA (see 32.6.6.6 below)

32.6.6.5 Bulk IN or Interrupt IN: Sending a Packet Under Application Control (Device to Host)

The application can write one or several banks.

A simple algorithm can be used by the application to send packets regardless of the number of banks associated to the endpoint.

Algorithm Description for Each Packet:

- The application waits for TX_PK_RDY flag to be cleared in the EPTSTAx register before it can perform a write access to the DPR.
- The application writes one USB packet of data in the DPR through the 64 KB endpoint logical memory window.
- The application sets TX_PK_RDY flag in the EPTSETSTAx register.

The application is notified that it is possible to write a new packet to the DPR by the TX_PK_RDY interrupt. This interrupt can be enabled or masked by setting the TX_PK_RDY bit in the EPTCTLENB/EPTCTLDIS register.

Algorithm Description to Fill Several Packets:

Using the previous algorithm, the application is interrupted for each packet. It is possible to reduce the application overhead by writing linearly several banks at the same time. The AUTO_VALID bit in the EPTCTLx must be set by writing the AUTO_VALID bit in the EPTCTLENBx register.

The auto-valid-bank mechanism allows the transfer of data (IN and OUT) without the intervention of the CPU. This means that bank validation (set TX_PK_RDY or clear the RX_BK_RDY bit) is done by hardware.

- The application checks the BUSY_BANK_STA field in the EPTSTAx register. The application must wait that at least one bank is free.
- The application writes a number of bytes inferior to the number of free DPR banks for the endpoint. Each time the application writes the last byte of a bank, the TX_PK_RDY signal is automatically set by the USBA.
- If the last packet is incomplete (i.e., the last byte of the bank has not been written) the application must set the TX_PK_RDY bit in the EPTSETSTAx register.

The application is notified that all banks are free, so that it is possible to write another burst of packets by the BUSY_BANK interrupt. This interrupt can be enabled or masked by setting the BUSY_BANK flag in the EPTCTLENB and EPTCTLDIS registers.

This algorithm must not be used for isochronous transfer. In this case, the ping-pong mechanism does not operate.

A Zero Length Packet can be sent by setting just the TX_PKTRDY flag in the EPTSETSTAx register.

32.6.6.6 *Bulk IN or Interrupt IN: Sending a Buffer Using DMA (Device to Host)*

The USBA integrates a DMA host controller. This DMA controller can be used to transfer a buffer from the memory to the DPR or from the DPR to the processor memory under the USBA control. The DMA can be used for all transfer types except control transfer.

Example DMA configuration:

1. Program DMAADDRESSx with the address of the buffer that should be transfer.
2. Enable the interrupt of the DMA in IEN
3. Program DMACONTROLx:
   - Size of buffer to send: size of the buffer to be sent to the host.
   - END_B_EN: The endpoint can validate the packet (according to the values programmed in the AUTO_VALID and SHRT_PCKT fields of EPTCTLx.) (See "USBA Endpoint Control Register" on page 722 and Figure 32-11. Autovalid with DMA)
   - END_BUFFIT: generate an interrupt when the BUFF_COUNT in DMASTATUSx reaches 0.
   - CHANN_ENB: Run and stop at end of buffer

The auto-valid-bank mechanism allows the transfer of data (IN & OUT) without the intervention of the CPU. This means that bank validation (set TX_PK_RDY or clear the RX_BK_RDY bit) is done by hardware.

A transfer descriptor can be used. Instead of programming the register directly, a descriptor should be programmed and the address of this descriptor is then given to DMANXTDSC to be processed after setting the LDNXT_DSC field (Load Next Descriptor Now) in DMACONTROLx register.

The structure that defines this transfer descriptor must be aligned.

Each buffer to be transferred must be described by a DMA Transfer descriptor (see "USBA DMA Channel Transfer Descriptor" on page 733). Transfer descriptors are chained. Before executing transfer of the buffer, the USBA may fetch a new transfer descriptor from the memory address pointed by the DMANXTDSCx register. Once the transfer is complete, the transfer status is updated in the DMASTATUSx register.

To chain a new transfer descriptor with the current DMA transfer, the DMA channel must be stopped. To do so, INTDIS_DMA and TX_BK_RDY may be set in the EPTCTLENBx register. It is also possible for the application to wait for the completion of all transfers. In this case the LDNXT_DSC field in the last transfer descriptor DMACONTROLx register must be set to 0 and CHANN_ENB set to 1.

Then the application can chain a new transfer descriptor.

The INTDIS_DMA can be used to stop the current DMA transfer if an enabled interrupt is triggered. This can be used to stop DMA transfers in case of errors.

The application can be notified at the end of any buffer transfer (ENB_BUFFIT bit in the DMACONTROLx register).

Figure 32-7. Data IN Transfer for Endpoint with One Bank

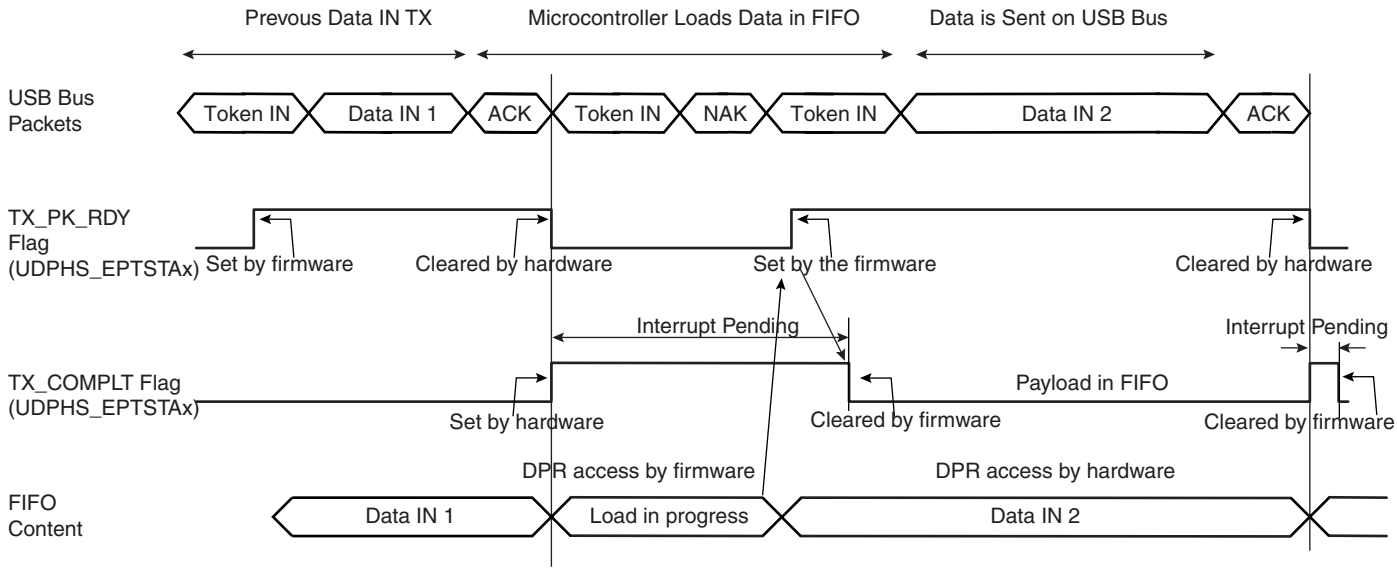


Figure 32-8. Data IN Transfer for Endpoint with Two Banks

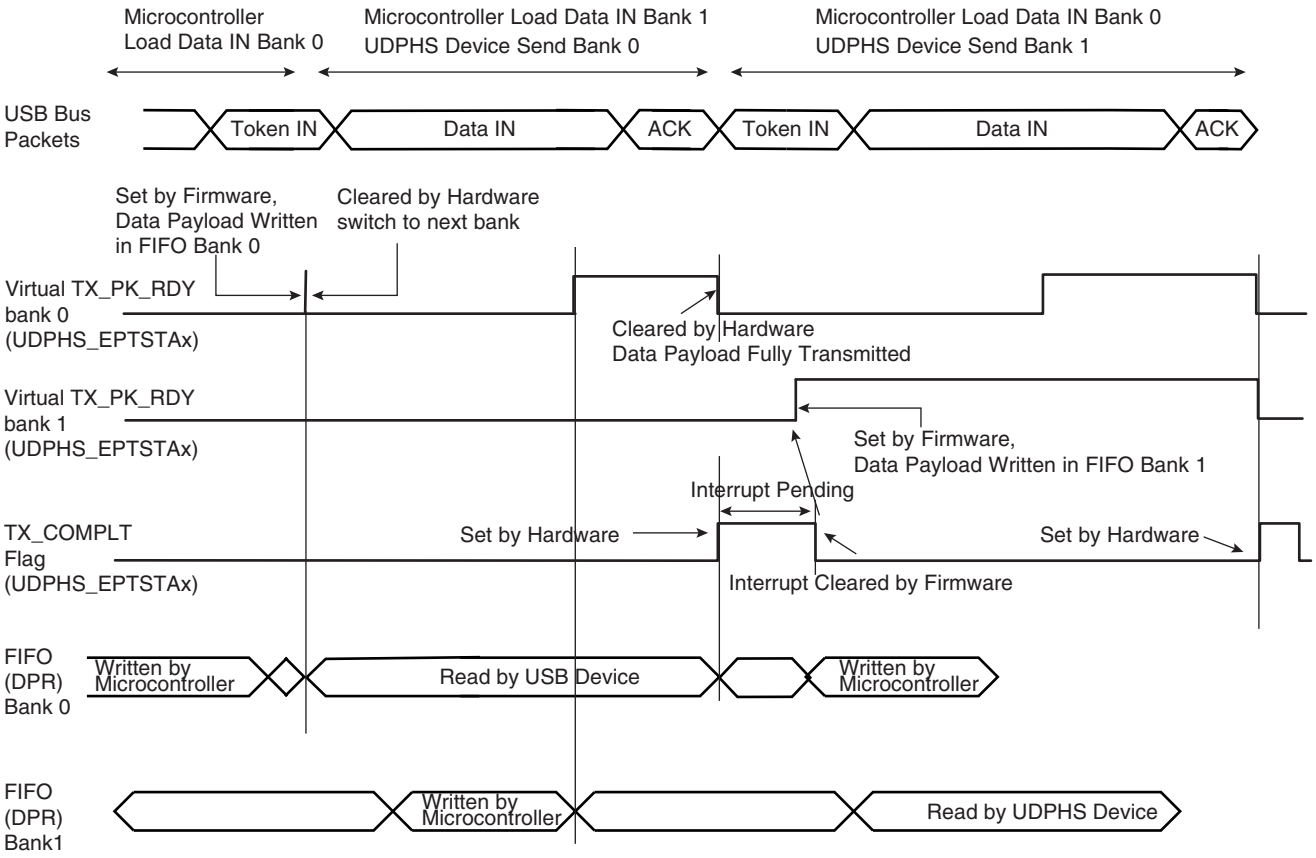
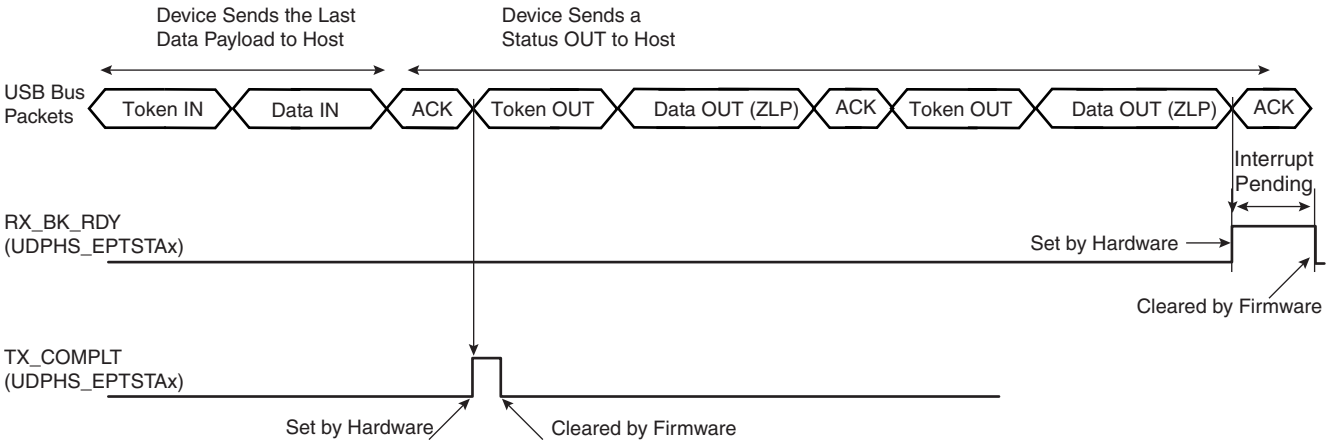
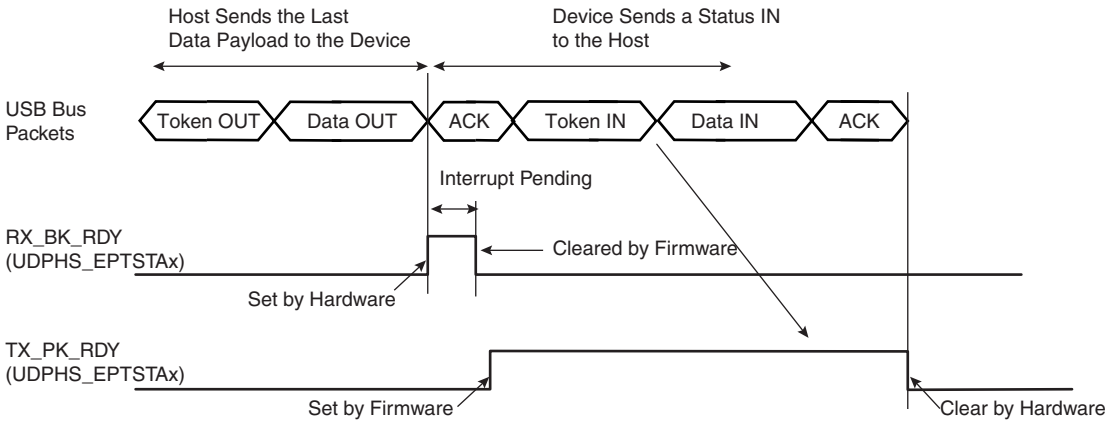


Figure 32-9. Data IN Followed By Status OUT Transfer at the End of a Control Transfer



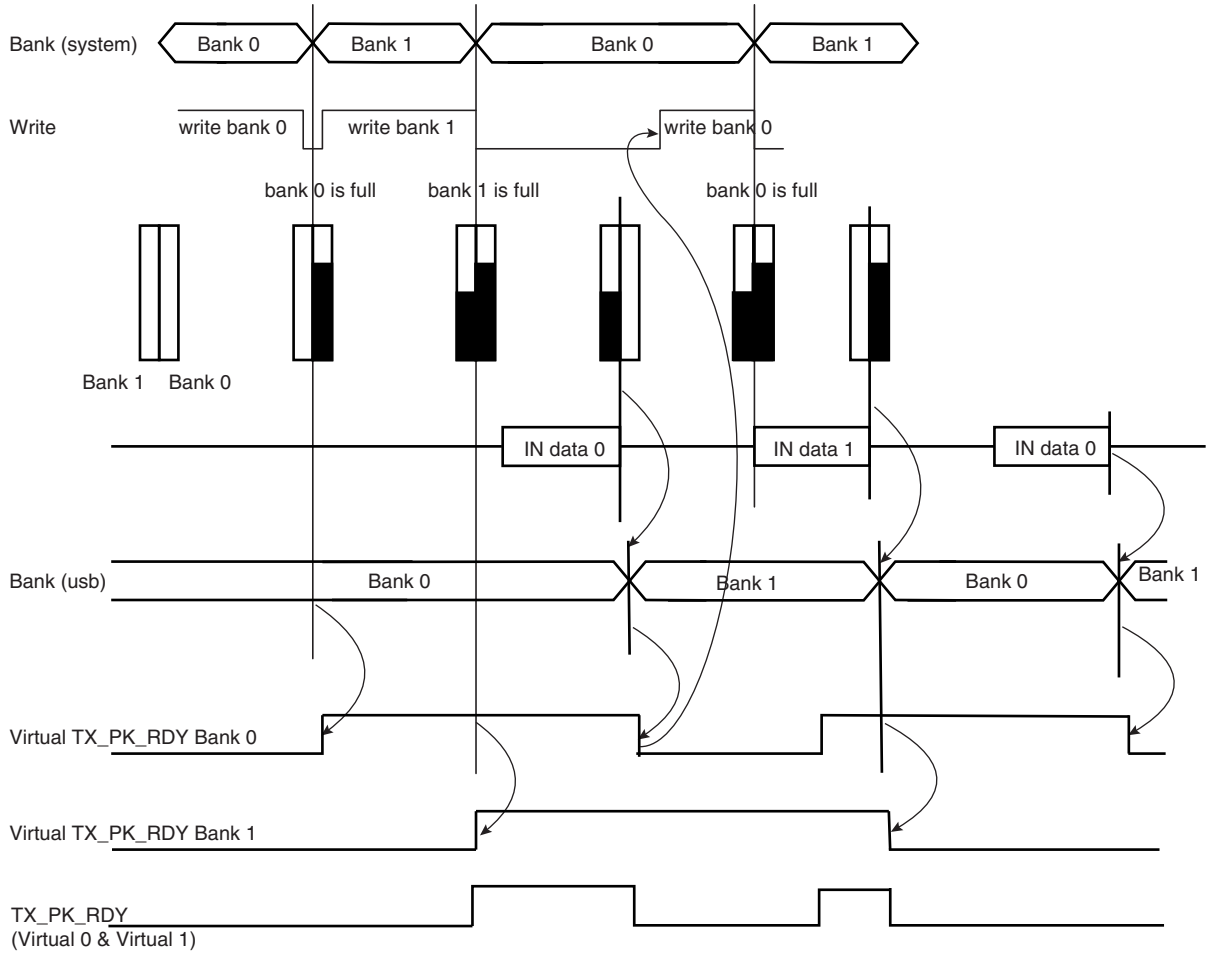
Note: A NAK handshake is always generated at the first status stage token.

Figure 32-10. Data OUT Followed by Status IN Transfer



Note: Before proceeding to the status stage, the software should determine that there is no risk of extra data from the host (data stage). If not certain (non-predictable data stage length), then the software should wait for a NAK-IN interrupt before proceeding to the status stage. This precaution should be taken to avoid collision in the FIFO.

Figure 32-11. Autovalid with DMA



Note: In the illustration above Autovalid validates a bank as full, although this might not be the case, in order to continue processing data and to send to DMA.

32.6.6.7 Isochronous IN

Isochronous-IN is used to transmit a stream of data whose timing is implied by the delivery rate. Isochronous transfer provides periodic, continuous communication between host and device.

It guarantees bandwidth and low latencies appropriate for telephony, audio, video, etc.

If the endpoint is not available (TX_PK_RDY = 0), then the device does not answer to the host. An ERR_FL_ISO interrupt is generated in the EPTSTAx register and once enabled, then sent to the CPU.

The STALL_SNT command bit is not used for an ISO-IN endpoint.

32.6.6.8 High Bandwidth Isochronous Endpoint Handling: IN Example

For high bandwidth isochronous endpoints, the DMA can be programmed with the number of transactions (BUFF_LENGTH field in DMACONTROLx) and the system should provide the required number of packets per microframe, otherwise, the host will notice a sequencing problem.

A response should be made to the first token IN recognized inside a microframe under the following conditions:

- If at least one bank has been validated, the correct DATAx corresponding to the programmed Number Of Transactions per Microframe (NB_TRANS) should be answered. In case of a subsequent missed or corrupted token IN inside the microframe, the USBA Core available data bank(s) that should normally have been transmitted during that microframe shall be flushed at its end. If this flush occurs, an error condition is flagged (ERR_FLUSH is set in EPTSTAx).
- If no bank is validated yet, the default DATA0 ZLP is answered and underflow is flagged (ERR_FL_ISO is set in EPTSTAx). Then, no data bank is flushed at microframe end.
- If no data bank has been validated at the time when a response should be made for the second transaction of NB_TRANS = 3 transactions microframe, a DATA1 ZLP is answered and underflow is flagged (ERR_FL_ISO is set in EPTSTAx). If and only if remaining untransmitted banks for that microframe are available at its end, they are flushed and an error condition is flagged (ERR_FLUSH is set in EPTSTAx).
- If no data bank has been validated at the time when a response should be made for the last programmed transaction of a microframe, a DATA0 ZLP is answered and underflow is flagged (ERR_FL_ISO is set in EPTSTAx). If and only if the remaining untransmitted data bank for that microframe is available at its end, it is flushed and an error condition is flagged (ERR_FLUSH is set in EPTSTAx).
- If at the end of a microframe no valid token IN has been recognized, no data bank is flushed and no error condition is reported.

At the end of a microframe in which at least one data bank has been transmitted, if less than NB_TRANS banks have been validated for that microframe, an error condition is flagged (ERR_TRANS is set in EPTSTAx).

Cases of Error (in EPTSTAx)

- ERR_FL_ISO: There was no data to transmit inside a microframe, so a ZLP is answered by default.
- ERR_FLUSH: At least one packet has been sent inside the microframe, but the number of token IN received is lesser than the number of transactions actually validated (TX_BK_RDY) and likewise with the NB_TRANS programmed.
- ERR_TRANS: At least one packet has been sent inside the microframe, but the number of token IN received is lesser than the number of programmed NB_TRANS transactions and the packets not requested were not validated.
- ERR_FL_ISO + ERR_FLUSH: At least one packet has been sent inside the microframe, but the data has not been validated in time to answer one of the following token IN.
- ERR_FL_ISO + ERR_TRANS: At least one packet has been sent inside the microframe, but the data has not been validated in time to answer one of the following token IN and the data can be discarded at the microframe end.

- ERR_FLUSH + ERR_TRANS: The first token IN has been answered and it was the only one received, a second bank has been validated but not the third, whereas NB_TRANS was waiting for three transactions.
- ERR_FL_ISO + ERR_FLUSH + ERR_TRANS: The first token IN has been treated, the data for the second Token IN was not available in time, but the second bank has been validated before the end of the microframe. The third bank has not been validated, but three transactions have been set in NB_TRANS.

32.6.6.9 Data OUT

32.6.6.10 Bulk OUT or Interrupt OUT

Like data IN, data OUT packets are sent by the host during the data or the status stage of control transfer or during an interrupt/bulk/isochronous OUT transfer. Data buffers are sent packet by packet under the control of the application or under the control of the DMA channel.

32.6.6.11 Bulk OUT or Interrupt OUT: Receiving a Packet Under Application Control (Host to Device)

Algorithm Description for Each Packet:

- The application enables an interrupt on RX_BK_RDY.
- When an interrupt on RX_BK_RDY is received, the application knows that EPTSTAx register BYTE_COUNT bytes have been received.
- The application reads the BYTE_COUNT bytes from the endpoint.
- The application clears RX_BK_RDY.

Note: If the application does not know the size of the transfer, it may **not** be a good option to use AUTO_VALID. Because if a zero-length-packet is received, the RX_BK_RDY is automatically cleared by the AUTO_VALID hardware and if the endpoint interrupt is triggered, the software will not find its originating flag when reading the EPTSTAx register.

Algorithm to Fill Several Packets:

- The application enables the interrupts of BUSY_BANK and AUTO_VALID.
- When a BUSY_BANK interrupt is received, the application knows that all banks available for the endpoint have been filled. Thus, the application can read all banks available.

If the application doesn't know the size of the receive buffer, instead of using the BUSY_BANK interrupt, the application must use RX_BK_RDY.

32.6.6.12 Bulk OUT or Interrupt OUT: Sending a Buffer Using DMA (Host To Device)

To use the DMA setting, the AUTO_VALID field is mandatory.

See 32.6.6.6 Bulk IN or Interrupt IN: Sending a Buffer Using DMA (Device to Host) for more information.

DMA Configuration Example:

1. First program DMAADDRESSx with the address of the buffer that should be transferred.
2. Enable the interrupt of the DMA in IEN
3. Program the DMA Channelx Control Register:
   - Size of buffer to be sent.
   - END_B_EN: Can be used for OUT packet truncation (discarding of unbuffered packet data) at the end of DMA buffer.

– END_BUFFIT: Generate an interrupt when BUFF_COUNT in the DMASTATUSx register reaches 0.
– END_TR_EN: End of transfer enable, the USBA device can put an end to the current DMA transfer, in case of a short packet.
– END_TR_IT: End of transfer interrupt enable, an interrupt is sent after the last USB packet has been transferred by the DMA, if the USB transfer ended with a short packet. (Beneficial when the receive size is unknown.)
– CHANN_ENB: Run and stop at end of buffer.

For OUT transfer, the bank will be automatically cleared by hardware when the application has read all the bytes in the bank (the bank is empty).

Note: When a zero-length-packet is received, RX_BK_RDY bit in EPTSTAx is cleared automatically by AUTO_VALID, and the application knows of the end of buffer by the presence of the END_TR_IT.

Note: If the host sends a zero-length packet, and the endpoint is free, then the device sends an ACK. No data is written in the endpoint, the RX_BY_RDY interrupt is generated, and the BYTE_COUNT field in EPTSTAx is null.

Figure 32-12. Data OUT Transfer for Endpoint with One Bank

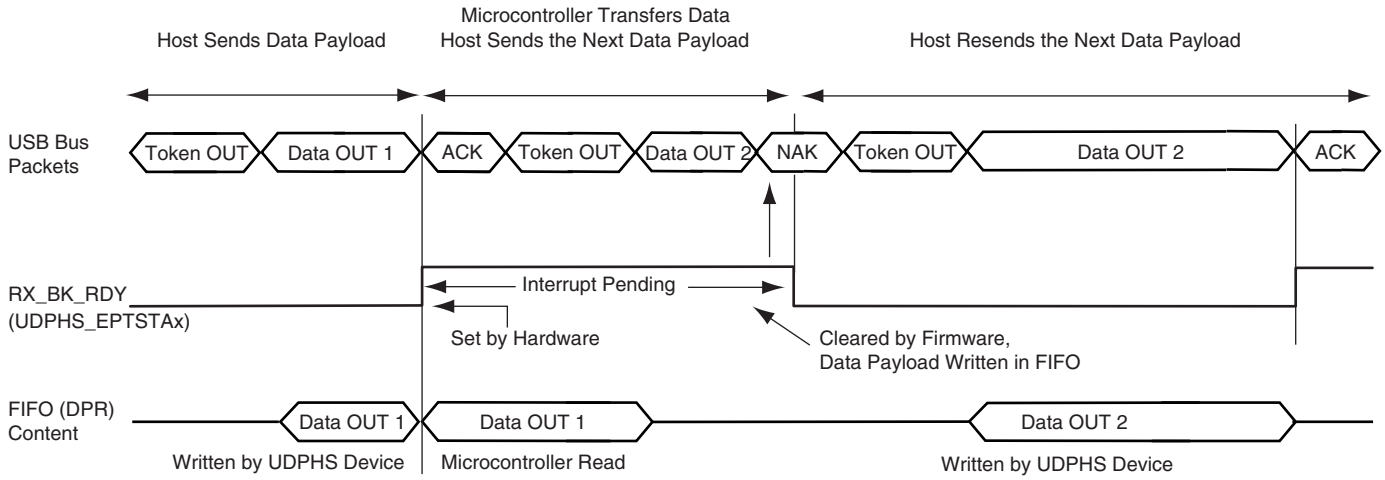
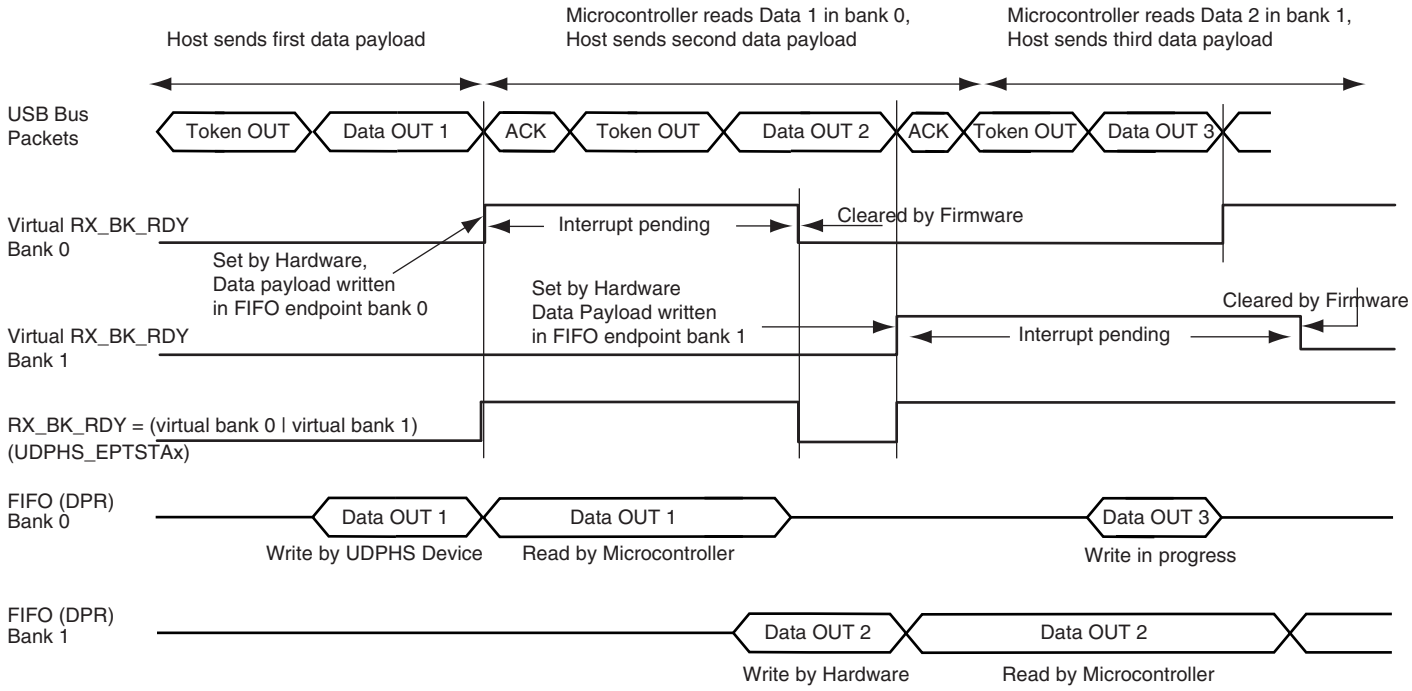
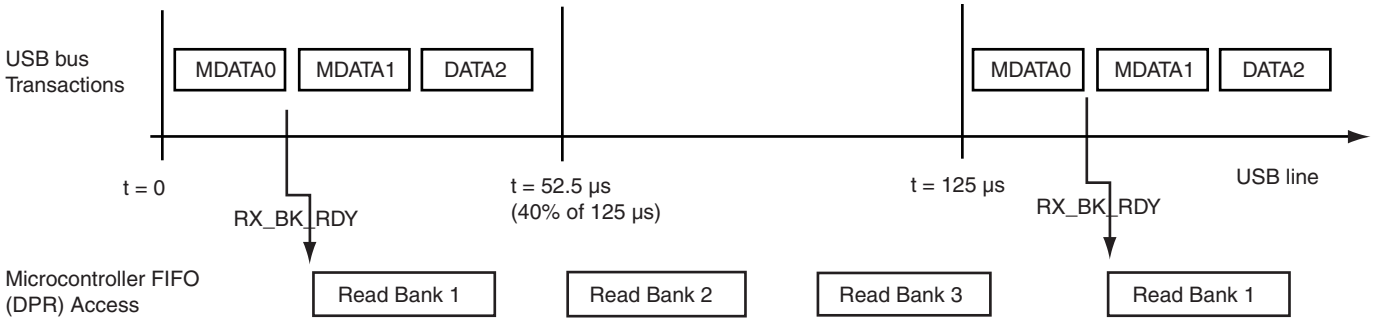


Figure 32-13. Data OUT Transfer for an Endpoint with Two Banks



32.6.6.13 High Bandwidth Isochronous Endpoint OUT

Figure 32-14. Bank Management, Example of Three Transactions per Microframe



USB 2.0 supports individual High Speed isochronous endpoints that require data rates up to 192 Mb/s (24 MB/s): 3x1024 data bytes per microframe.

To support such a rate, two or three banks may be used to buffer the three consecutive data packets. The microcontroller (or the DMA) should be able to empty the banks very rapidly (at least 24 MB/s on average).

NB_TRANS field in EPTCFGx register = Number Of Transactions per Microframe.

If NB_TRANS > 1 then it is High Bandwidth.

Example:

- If NB_TRANS = 3, the sequence should be either
  - MData0
  - MData0/Data1
  - MData0/Data1/Data2
- If NB_TRANS = 2, the sequence should be either
  - MData0
  - MData0/Data1
- If NB_TRANS = 1, the sequence should be
  - Data0

32.6.6.14 Isochronous Endpoint Handling: OUT Example

The user can ascertain the bank status (free or busy), and the toggle sequencing of the data packet for each bank with the EPTSTAx register in the three bit fields as follows:

- TOGGLESQ_STA: PID of the data stored in the current bank
- CURRENT_BANK: Number of the bank currently being accessed by the microcontroller.
- BUSY_BANK_STA: Number of busy bank

This is particularly useful in case of a missing data packet.

If the inter-packet delay between the OUT token and the Data is greater than the USB standard, then the ISO-OUT transaction is ignored. (Payload data is not written, no interrupt is generated to the CPU.)

If there is a data CRC (Cyclic Redundancy Check) error, the payload is, none the less, written in the endpoint. The ERR_CRISO flag is set in EPTSTAx register.

If the endpoint is already full, the packet is not written in the DPRAM. The ERR_FL_ISO flag is set in EPTSTAx.

If the payload data is greater than the maximum size of the endpoint, then the ERR_OVFLW flag is set. It is the task of the CPU to manage this error. The data packet is written in the endpoint (except the extra data).

If the host sends a Zero Length Packet, and the endpoint is free, no data is written in the endpoint, the RX_BK_RDY flag is set, and the BYTE_COUNT field in EPTSTAx register is null.

The FRCESTALL command bit is unused for an isochonous endpoint.

Otherwise, payload data is written in the endpoint, the RX_BK_RDY interrupt is generated and the BYTE_COUNT in EPTSTAx register is updated.

32.6.6.15 STALL

STALL is returned by a function in response to an IN token or after the data phase of an OUT or in response to a PING transaction. STALL indicates that a function is unable to transmit or receive data, or that a control pipe request is not supported.

• OUT

To stall an endpoint, set the FRCESTALL bit in EPTSETSTAx register and after the STALL_SNT flag has been set, set the TOGGLE_SEG bit in the EPTCLRSTAx register.

• IN

Set the FRCESTALL bit in EPTSETSTAx register.

Figure 32-15. Stall Handshake Data OUT Transfer

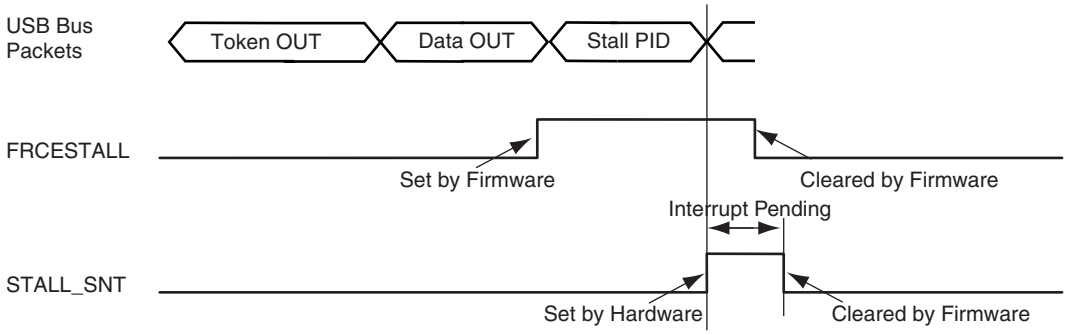
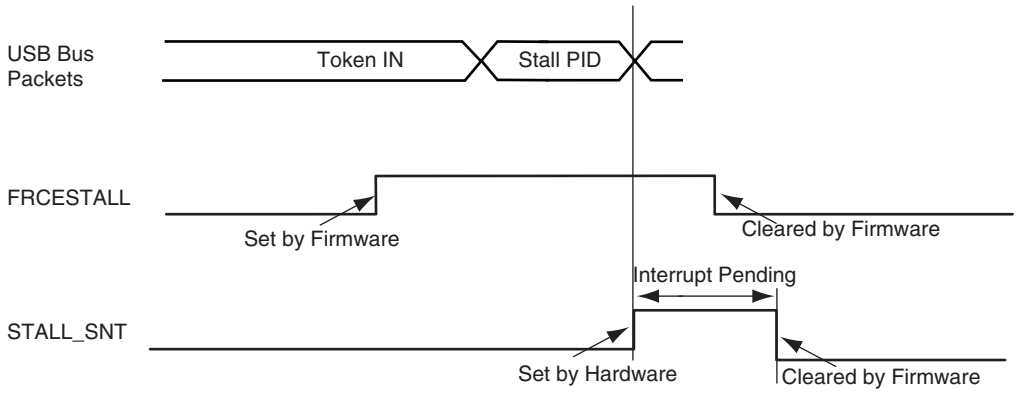


Figure 32-16. Stall Handshake Data IN Transfer



32.6.7 Speed Identification

The high speed reset is managed by the hardware.

At the connection, the host makes a reset which could be a classic reset (full speed) or a high speed reset.

At the end of the reset process (full or high), the ENDRESET interrupt is generated.

Then the CPU should read the SPEED bit in INTSTAx to ascertain the speed mode of the device.

32.6.8 USB V2.0 High Speed Global Interrupt

Interrupts are defined in Section 32.7.3 ”USBA Interrupt Enable Register” (IEN) and in Section 32.7.4 ”USBA Interrupt Status Register” (INTSTA).

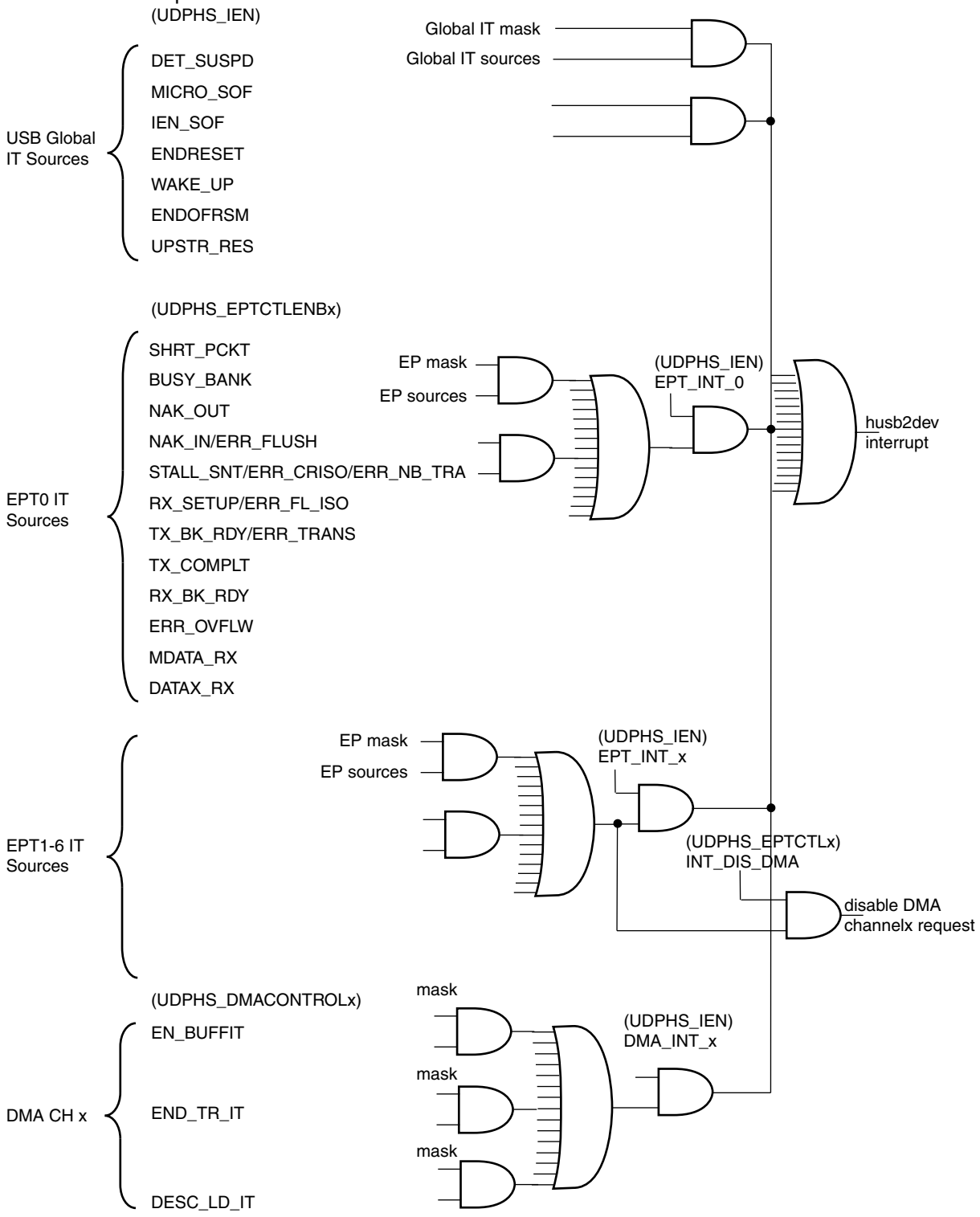
32.6.9 Endpoint Interrupts

Interrupts are enabled in IEN (see Section 32.7.3 ”USBA Interrupt Enable Register”) and individually masked in EPTCTLENBx (see Section 32.7.18 ”USBA Endpoint Control Enable Register”).

Table 32-5. Endpoint Interrupt Source Masks

SHRT_PCKT	Short Packet Interrupt
BUSY_BANK	Busy Bank Interrupt
NAK_OUT	NAKOUT Interrupt
NAK_IN/ERR_FLUSH	NAKIN/Error Flush Interrupt
STALL_SNT/ERR_CRISO/ERR_NB_TRA	Stall Sent/CRC error/Number of Transaction Error Interrupt
RX_SETUP/ERR_FL_ISO	Received SETUP/Error Flow Interrupt
TX_PK_RD /ERR_TRANS	TX Packet Read/Transaction Error Interrupt
TX_COMPLT	Transmitted IN Data Complete Interrupt
RX_BK_RDY	Received OUT Data Interrupt
ERR_OVFLW	Overflow Error Interrupt
MDATA_RX	MDATA Interrupt
DATAX_RX	DATAx Interrupt

Figure 32-17. USBA Interrupt Control Interface

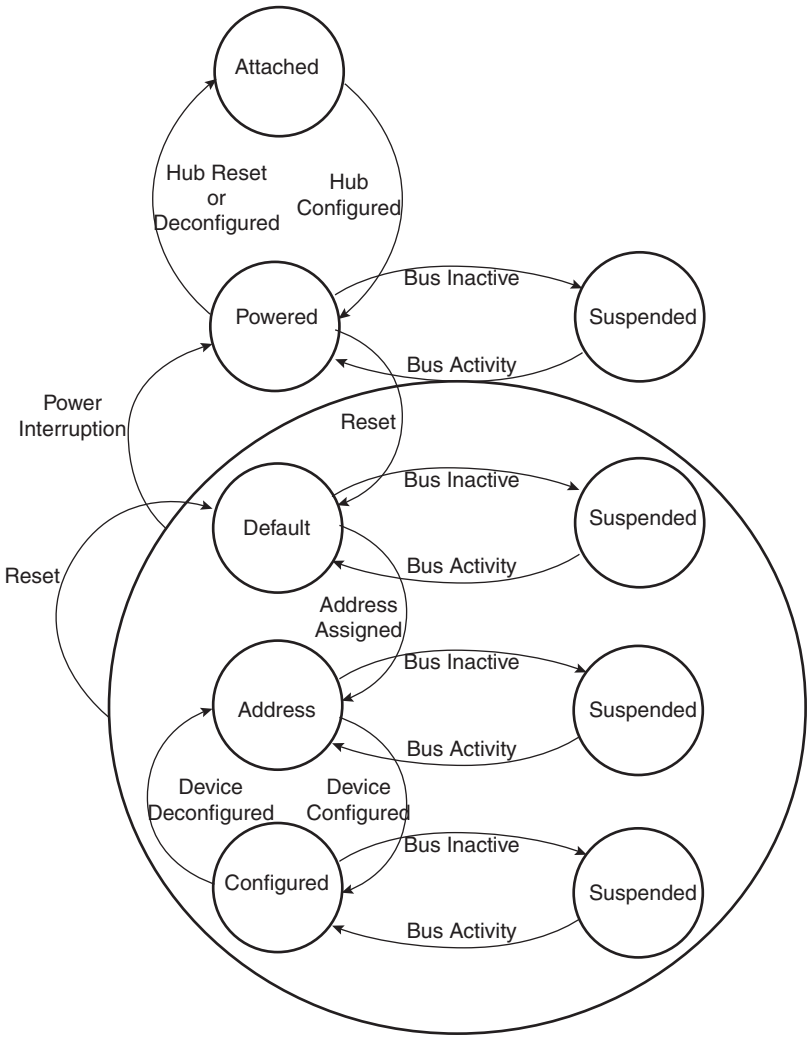


32.6.10 Power Modes

32.6.10.1 Controlling Device States

A USB device has several possible states. Refer to Chapter 9 (USB Device Framework) of the Universal Serial Bus Specification, Rev 2.0.

Figure 32-18. USBADevice State Diagram



Movement from one state to another depends on the USB bus state or on standard requests sent through control transactions via the default endpoint (endpoint 0).

After a period of bus inactivity, the USB device enters Suspend Mode. Accepting Suspend/Resume requests from the USB host is mandatory. Constraints in Suspend Mode are very strict for bus-powered applications; devices may not consume more than 500 µA on the USB bus.

While in Suspend Mode, the host may wake up a device by sending a resume signal (bus activity) or a USB device may send a wake-up request to the host, e.g., waking up a PC by moving a USB mouse.

The wake-up feature is not mandatory for all devices and must be negotiated with the host.

32.6.10.2 *From Powered State to Default State (Reset)*

After its connection to a USB host, the USB device waits for an end-of-bus reset. The unmasked flag ENDRESET is set in the IEN register and an interrupt is triggered.

Once the ENDRESET interrupt has been triggered, the device enters Default State. In this state, the USBA software must:

- Enable the default endpoint, setting the EPT_ENABL flag in the EPTCTLENB[0] register and, optionally, enabling the interrupt for endpoint 0 by writing 1 in EPT_INT_0 of the IEN register. The enumeration then begins by a control transfer.
- Configure the Interrupt Mask Register which has been reset by the USB reset detection
- Enable the transceiver.

In this state, the EN_USBA bit in CTRL register must be enabled.

32.6.10.3 *From Default State to Address State (Address Assigned)*

After a Set Address standard device request, the USB host peripheral enters the address state.

Warning: before the device enters address state, it must achieve the Status IN transaction of the control transfer, i.e., the USBA device sets its new address once the TX_COMPLT flag in the EPTCTL[0] register has been received and cleared.

To move to address state, the driver software sets the DEV_ADDR field and the FADDR_EN flag in the CTRL register.

32.6.10.4 *From Address State to Configured State (Device Configured)*

Once a valid Set Configuration standard request has been received and acknowledged, the device enables endpoints corresponding to the current configuration. This is done by setting the BK_NUMBER, EPT_TYPE, EPT_DIR and EPT_SIZE fields in the EPTCFGx registers and enabling them by setting the EPT_ENABL flag in the EPTCTLENBx registers, and, optionally, enabling corresponding interrupts in the IEN register.

32.6.10.5 *Entering Suspend State (Bus Activity)*

When a Suspend (no bus activity on the USB bus) is detected, the DET_SUSPD signal in the INTSTA register is set. This triggers an interrupt if the corresponding bit is set in the IEN register. This flag is cleared by writing to the CLRINT register. Then the device enters Suspend Mode.

In this state bus powered devices must drain less than 500 µA from the 5V VBUS. As an example, the microcontroller switches to slow clock, disables the PLL and main oscillator, and goes into Idle Mode. It may also switch off other devices on the board.

The USBAUSBA device peripheral clocks can be switched off. Resume event is asynchronously detected.

32.6.10.6 *Receiving a Host Resume*

In Suspend mode, a resume event on the USB bus line is detected asynchronously, transceiver and clocks disabled (however the pull-up should not be removed).

Once the resume is detected on the bus, the signal WAKE_UP in the INTSTA is set. It may generate an interrupt if the corresponding bit in the IEN register is set. This interrupt may be used to wake-up the core, enable PLL and main oscillators and configure clocks.

32.6.10.7 Sending an External Resume

In Suspend State it is possible to wake-up the host by sending an external resume.

The device waits at least 5 ms after being entered in Suspend State before sending an external resume.

The device must force a K state from 1 to 15 ms to resume the host.

32.6.11 Test Mode

A device must support the TEST_MODE feature when in the Default, Address or Configured High Speed device states.

TEST_MODE can be:

- Test_J
- Test_K
- Test_Packet
- Test_SEO_NAK

(See Section 32.7.11 ”USBA Test Register” on page 708 for definitions of each test mode.)

```
const char test_packet_buffer[] = {
  // JKJKJKJK * 9
  0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,0x00,
  // JJKKJJKK * 8
  0xAA,0xAA,0xAA,0xAA,0xAA,0xAA,0xAA,0xAA,
  // JJKKJJKK * 8
  0xEE,0xEE,0xEE,0xEE,0xEE,0xEE,0xEE,0xEE,
  // JJJJJJJKKKKKKK * 8
  0xFE,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,0xFF,
  // JJJJJJJK * 8
  0x7F,0xBF,0xDF,0xEF,0xF7,0xFB,0xFD,
  // {JKKKKKKK * 10}, JK
  0xFC,0x7E,0xBF,0xDF,0xEF,0xF7,0xFB,0xFD,0x7E
};
```

32.7 USB High Speed Device (USBA) User Interface

Table 32-6. Register Mapping

Offset	Register	Name	Access	Reset
0x00	USBA Control Register	CTRL	Read/Write	0x0000_0200
0x04	USBA Frame Number Register	FNUM	Read	0x0000_0000
0x08 - 0x0C	Reserved	–	–	–
0x10	USBA Interrupt Enable Register	IEN	Read/Write	0x0000_0010
0x14	USBA Interrupt Status Register	INTSTA	Read	0x0000_0000
0x18	USBA Clear Interrupt Register	CLRINT	Write	–
0x1C	USBA Endpoints Reset Register	EPTRST	Write	–
0x20 - 0xCC	Reserved	–	–	–
0xD0	USBA Test SOF Counter Register	TSTSOFCNT	Read/Write	0x0000_0000
0xD4	USBA Test A Counter Register	TSTCNTA	Read/Write	0x0000_0000
0xD8	USBA Test B Counter Register	TSTCNTB	Read/Write	0x0000_0000
0xDC	USBA Test Mode Register	TSTMODEREG	Read/Write	0x0000_0000
0xE0	USBA Test Register	TST	Read/Write	0x0000_0000
0xE4 - 0xE8	Reserved	–	–	–
0xEC	USBA PADDRSIZE Register	IPPADDRSIZE	Read	0x0000_4000
0xF0	USBA Name1 Register	IPNAME1	Read	0x4855_5342
0xF4	USBA Name2 Register	IPNAME2	Read	0x3244_4556
0xF8	USBA Features Register	IPFEATURES	Read	
0xFC	USBA IP Version Register	IPVERSION	Read	
0x100	USBA Endpoint Configuration Register	EPTCFGx	Read/Write	0x0000_0000
0x104	USBA Endpoint Control Enable Register	EPTCTLENBx	Write	–
0x108	USBA Endpoint Control Disable Register	EPTCTLDISx	Write	–
0x10C	USBA Endpoint Control Register	EPTCTLx	Read	0x0000_0000(1)
0x110	Reserved	–	–	–
0x114	USBA Endpoint Set Status Register	EPTSETSTAx	Write	–
0x118	USBA Endpoint Clear Status Register	EPTCLRSTAx	Write	–
0x11C	USBA Endpoint Status Register	EPTSTA	Read	0x0000_0040
0x120 - 0x1FC	Endpoints 1 to 7			
0x200 - 0x2FC	Endpoints 8 to 15			
0x200 - 0x30C	Reserved	–	–	–
0x300 - 0x30C	Reserved	–	–	–
0x310	USBA DMA Next Descriptor Address Register	DMANXTDSCx	Read/Write	0x0000_0000
0x314	USBA DMA Channelx Address Register	DMAADDRESSx	Read/Write	0x0000_0000

Table 32-6. Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x318	USBA DMA Channelx Control Register	DMACONTROLx	Read/Write	0x0000_0000
0x31C	USBA DMA Channelx Status Register	DMASTATUSx	Read/Write	0x0000_0000
0x320 - 0x37C	DMA Channel 2 to 7			

Note: 1. The reset value for EPTCTL0 is 0x0000_0001

32.7.1 USBA Control Register

Name: CTRL

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	REWAKEUP	DETACH	EN_USBA

7	6	5	4	3	2	1	0
FADDR_EN	DEV_ADDR						

- **DEV_ADDR: USBA Address**

Read:

This field contains the default address (0) after power-up or USBA bus reset.

Write:

This field is written with the value set by a SET_ADDRESS request received by the device firmware.

- **FADDR_EN: Function Address Enable**

Read:

0 = Device is not in address state.

1 = Device is in address state.

Write:

0 = only the default function address is used (0).

1 = this bit is set by the device firmware after a successful status phase of a SET_ADDRESS transaction. When set, the only address accepted by the USBA controller is the one stored in the USBA Address field. It will not be cleared afterwards by the device firmware. It is cleared by hardware on hardware reset, or when USBA bus reset is received (see above).

- **EN_USBA: USBA Enable**

Read:

0 = USBA is disabled.

1 = USBA is enabled.

Write:

0 = disable and reset the USBA controller, disable the USBA transceiver.

1 = enables the USBA controller.

- **DETACH: Detach Command**

Read:

0 = USBA is attached.

1 = USBA is detached, UTMI transceiver is suspended.

Write:

0 = pull up the DP line (attach command).

1 = simulate a detach on the USBA line and force the UTMI transceiver into suspend state (Suspend M = 0).

- **REWAKEUP: Send Remote Wake Up**

Read:

0 = Remote Wake Up is disabled.

1 = Remote Wake Up is enabled.

Write:

0 = no effect.

1 = force an external interrupt on the USBA controller for Remote Wake UP purposes.

An Upstream Resume is sent only after the USBA bus has been in SUSPEND state for at least 5 ms.

This bit is automatically cleared by hardware at the end of the Upstream Resume.

32.7.2 USBA Frame Number Register

Name: FNUM

Access Type: Read

31	30	29	28	27	26	25	24
FNUM_ERR	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	FRAME_NUMBER					

7	6	5	4	3	2	1	0
FRAME_NUMBER					MICRO_FRAME_NUM		

- **MICRO_FRAME_NUM: Microframe Number**

Number of the received microframe (0 to 7) in one frame.This field is reset at the beginning of each new frame (1 ms).

One microframe is received each 125 microseconds (1 ms/8).

- **FRAME_NUMBER: Frame Number as defined in the Packet Field Formats**

This field is provided in the last received SOF packet (see INT_SOF in the USBA Interrupt Status Register).

- **FNUM_ERR: Frame Number CRC Error**

This bit is set by hardware when a corrupted Frame Number in Start of Frame packet (or Micro SOF) is received.

This bit and the INT_SOF (or MICRO_SOF) interrupt are updated at the same time.

32.7.3 USBA Interrupt Enable Register

Name: IEN

Access Type: Read/Write

31	30	29	28	27	26	25	24
	DMA_INT_6	DMA_INT_5	DMA_INT_4	DMA_INT_3	DMA_INT_2	DMA_INT_1	–
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
EPT_INT_7	EPT_INT_6	EPT_INT_5	EPT_INT_4	EPT_INT_3	EPT_INT_2	EPT_INT_1	EPT_INT_0
7	6	5	4	3	2	1	0
UPSTR_RES	ENDOFRSM	WAKE_UP	ENDRESET	INT_SOF	MICRO_SOF	DET_SUSPD	–

- **DET_SUSPD: Suspend Interrupt Enable**

Read:

0 = Suspend Interrupt is disabled.

1 = Suspend Interrupt is enabled.

Write

0 = disable Suspend Interrupt.

1 = enable Suspend Interrupt.

- **MICRO_SOF: Micro-SOF Interrupt Enable**

Read:

0 = Micro-SOF Interrupt is disabled.

1 = Micro-SOF Interrupt is enabled.

Write

0 = disable Micro-SOF Interrupt.

1 = enable Micro-SOF Interrupt.

- **INT_SOF: SOF Interrupt Enable**

Read:

0 = SOF Interrupt is disabled.

1 = SOF Interrupt is enabled.

Write

0 = disable SOF Interrupt.

1 = enable SOF Interrupt.

- **ENDRESET: End Of Reset Interrupt Enable**

Read:

0 = End Of Reset Interrupt is disabled.

1 = End Of Reset Interrupt is enabled.

Write

0 = disable End Of Reset Interrupt.

1 = enable End Of Reset Interrupt.

- **WAKE_UP: Wake Up CPU Interrupt Enable**

Read:

0 = Wake Up CPU Interrupt is disabled.

1 = Wake Up CPU Interrupt is enabled.

Write

0 = disable Wake Up CPU Interrupt.

1 = enable Wake Up CPU Interrupt.

- **ENDOFRSM: End Of Resume Interrupt Enable**

Read:

0 = Resume Interrupt is disabled.

1 = Resume Interrupt is enabled.

Write

0 = disable Resume Interrupt.

1 = enable Resume Interrupt.

- **UPSTR_RES: Upstream Resume Interrupt Enable**

Read:

0 = Upstream Resume Interrupt is disabled.

1 = Upstream Resume Interrupt is enabled.

Write

0 = disable Upstream Resume Interrupt.

1 = enable Upstream Resume Interrupt.

- **EPT_INT_x: Endpointx Interrupt Enable**

Read:

0 = the interrupts for this endpoint are disabled.

1 = the interrupts for this endpoint are enabled.

Write

0 = disable the interrupts for this endpoint.

1 = enable the interrupts for this endpoint.

- **DMA_INT_x: DMA Channelx Interrupt Enable**

Read:

0 = the interrupts for this channel are disabled.

1 = the interrupts for this channel are enabled.

Write

0 = disable the interrupts for this channel.

1 = enable the interrupts for this channel.

32.7.4 USBA Interrupt Status Register

Name: INTSTA

Access Type: Read-only

31	30	29	28	27	26	25	24
	DMA_INT_6	DMA_INT_5	DMA_INT_4	DMA_INT_3	DMA_INT_2	DMA_INT_1	–
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
EPT_INT_7	EPT_INT_6	EPT_INT_5	EPT_INT_4	EPT_INT_3	EPT_INT_2	EPT_INT_1	EPT_INT_0
7	6	5	4	3	2	1	0
UPSTR_RES	ENDOFRSM	WAKE_UP	ENDRESET	INT_SOF	MICRO_SOF	DET_SUSPD	SPEED

- **SPEED: Speed Status**

0 = reset by hardware when the hardware is in Full Speed mode.

1 = set by hardware when the hardware is in High Speed mode

- **DET_SUSPD: Suspend Interrupt**

0 = cleared by setting the DET_SUSPD bit in CLRINT register

1 = set by hardware when a USBA Suspend (Idle bus for three frame periods, a J state for 3 ms) is detected. This triggers a USBA interrupt when the DET_SUSPD bit is set in IEN register.

- **MICRO_SOF: Micro Start Of Frame Interrupt**

0 = cleared by setting the MICRO_SOF bit in CLRINT register.

1 = set by hardware when an USBA micro start of frame PID (SOF) has been detected (every 125 us) or synthesized by the macro. This triggers a USBA interrupt when the MICRO_SOF bit is set in IEN. In case of detected SOF, the MICRO_FRAME_NUM field in FNUM register is incremented and the FRAME_NUMBER field doesn't change.

Note: The Micro Start Of Frame Interrupt (MICRO_SOF), and the Start Of Frame Interrupt (INT_SOF) are not generated at the same time.

- **INT_SOF: Start Of Frame Interrupt**

0 = cleared by setting the INT_SOF bit in CLRINT.

1 = set by hardware when an USBA Start Of Frame PID (SOF) has been detected (every 1 ms) or synthesized by the macro. This triggers a USBA interrupt when the INT_SOF bit is set in IEN register. In case of detected SOF, in High Speed mode, the MICRO_FRAME_NUMBER field is cleared in FNUM register and the FRAME_NUMBER field is updated.

- **ENDRESET: End Of Reset Interrupt**

0 = cleared by setting the ENDRESET bit in CLRINT.

1 = set by hardware when an End Of Reset has been detected by the USBA controller. This triggers a USBA interrupt when the ENDRESET bit is set in IEN.

- **WAKE_UP: Wake Up CPU Interrupt**

0 = cleared by setting the WAKE_UP bit in CLRINT.

1 = set by hardware when the USBA controller is in SUSPEND state and is re-activated by a filtered non-idle signal from the USBA line (not by an upstream resume). This triggers a USBA interrupt when the WAKE_UP bit is set in IEN register. When receiving this interrupt, the user has to enable the device controller clock prior to operation.

Note: this interrupt is generated even if the device controller clock is disabled.

- **ENDOFRSM: End Of Resume Interrupt**

0 = cleared by setting the ENDOFRSM bit in CLRINT.

1 = set by hardware when the USBA controller detects a good end of resume signal initiated by the host. This triggers a USBA interrupt when the ENDOFRSM bit is set in IEN.

- **UPSTR_RES: Upstream Resume Interrupt**

0 = cleared by setting the UPSTR_RES bit in CLRINT.

1 = set by hardware when the USBA controller is sending a resume signal called “upstream resume”. This triggers a USBA interrupt when the UPSTR_RES bit is set in IEN.

- **EPT_INT_x: Endpointx Interrupt**

0 = reset when the EPTSTAx interrupt source is cleared.

1 = set by hardware when an interrupt is triggered by the EPTSTAx register and this endpoint interrupt is enabled by the EPT_INT_x bit in IEN.

- **DMA_INT_x: DMA Channelx Interrupt**

0 = reset when the DMASTATUSx interrupt source is cleared.

1 = set by hardware when an interrupt is triggered by the DMA Channelx and this endpoint interrupt is enabled by the DMA_INT_x bit in IEN.

32.7.5 USBA Clear Interrupt Register

Name: CLRINT

Access Type: Write only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
UPSTR_RES	ENDOFRSM	WAKE_UP	ENDRESET	INT_SOF	MICRO_SOF	DET_SUSPD	–

- **DET_SUSPD: Suspend Interrupt Clear**

0 = no effect.

1 = clear the DET_SUSPD bit in INTSTA.

- **MICRO_SOF: Micro Start Of Frame Interrupt Clear**

0 = no effect.

1 = clear the MICRO_SOF bit in INTSTA.

- **INT_SOF: Start Of Frame Interrupt Clear**

0 = no effect.

1 = clear the INT_SOF bit in INTSTA.

- **ENDRESET: End Of Reset Interrupt Clear**

0 = no effect.

1 = clear the ENDRESET bit in INTSTA.

- **WAKE_UP: Wake Up CPU Interrupt Clear**

0 = no effect.

1 = clear the WAKE_UP bit in INTSTA.

- **ENDOFRSM: End Of Resume Interrupt Clear**

0 = no effect.

1 = clear the ENDOFRSM bit in INTSTA.

- **UPSTR_RES: Upstream Resume Interrupt Clear**

0 = no effect.

1 = clear the UPSTR_RES bit in INTSTA.

32.7.6 USBA Endpoints Reset Register

Name: EPTRST

Access Type: Write only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RST_EPT_7	RST_EPT_6	RST_EPT_5	RST_EPT_4	RST_EPT_3	RST_EPT_2	RST_EPT_1	RST_EPT_0

- **RST_EPT_x: Endpointx Reset**

0 = no effect.

1 = reset the Endpointx state.

Setting this bit clears the Endpoint status EPTSTAx register, except for the TOGGLESQ_STA field.

32.7.7 USBA Test SOF Counter Register

Name: TSTSOFCNT

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
SOFCTLOAD	SOFCNTMAX						

- **SOFCNTMAX: SOF Counter Max Value**
- **SOFCTLOAD: SOF Counter Load**

32.7.8 USBA Test A Counter Register

Name: TSTCNTA

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
CNTALOAD	CNTAMAX						

7	6	5	4	3	2	1	0
CNTAMAX							

- **CNTALOAD: A Counter Load**
- **CNTAMAX: A Counter Max Value**

32.7.9 USBA Test B Counter Register

Name: TSTCNTB

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
CNTBLOAD	–	CNTBMAX					

- **CNTBLOAD: B Counter Load**
- **CNTBMAX: B Counter Max Value**

32.7.10 USBA Test Mode Register

Name: TSTMODEREG

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	TSTMODE					

- **TSTMODE: USBA Core TestModeReg**

32.7.11 USBA Test Register

Name: TST

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	OPMODE2	TST_PKT	TST_K	TST_J	SPEED_CFG	

- **SPEED_CFG: Speed Configuration**

Read/Write:

Speed Configuration:

00	Normal Mode: The macro is in Full Speed mode, ready to make a High Speed identification, if the host supports it and then to automatically switch to High Speed mode
01	Reserved
10	Force High Speed: Set this value to force the hardware to work in High Speed mode. Only for debug or test purpose.
11	Force Full Speed: Set this value to force the hardware to work only in Full Speed mode. In this configuration, the macro will not respond to a High Speed reset handshake

- **TST_J: Test J Mode**

Read and write:

0 = no effect.

1 = set to send the J state on the USBA line. This enables the testing of the high output drive level on the D+ line.

- **TST_K: Test K Mode**

Read and write:

0 = no effect.

1 = set to send the K state on the USBA line. This enables the testing of the high output drive level on the D- line.

- **TST_PKT: Test Packet Mode**

Read and write:

0 = no effect.

1 = set to repetitively transmit the packet stored in the current bank. This enables the testing of rise and fall times, eye patterns, jitter, and any other dynamic waveform specifications.

- **OPMODE2: OpMode2**

Read and write:

0 = no effect.

1 = set to force the OpMode signal (UTMI interface) to “10”, to disable the bit-stuffing and the NRZI encoding.

Note: For the Test mode, Test_SE0_NAK (see Universal Serial Bus Specification, Revision 2.0: 7.1.20, Test Mode Support). Force the device in High Speed mode, and configure a bulk-type endpoint. Do not fill this endpoint for sending NAK to the host.

Upon command, a port’s transceiver must enter the High Speed receive mode and remain in that mode until the exit action is taken. This enables the testing of output impedance, low level output voltage and loading characteristics. In addition, while in this mode, upstream facing ports (and only upstream facing ports) must respond to any IN token packet with a NAK handshake (only if the packet CRC is determined to be correct) within the normal allowed device response time. This enables testing of the device squelch level circuitry and, additionally, provides a general purpose stimulus/response test for basic functional testing.

32.7.12 USBA PADDRSIZE Register

Name: IPPADDRSIZE

Access Type: Read-only

31	30	29	28	27	26	25	24
IP_PADDRSIZE							

23	22	21	20	19	18	17	16
IP_PADDRSIZE							

15	14	13	12	11	10	9	8
IP_PADDRSIZE							

7	6	5	4	3	2	1	0
IP_PADDRSIZE							

- **IP_PADDRSIZE**

2^PADDR_SIZE

PB address bus aperture of the USBA

32.7.13 USBA Name1 Register

Name: IPNAME1

Access Type: Read-only

31	30	29	28	27	26	25	24
IP_NAME1							

23	22	21	20	19	18	17	16
IP_NAME1							

15	14	13	12	11	10	9	8
IP_NAME1							

7	6	5	4	3	2	1	0
IP_NAME1							

- **IP_NAME1**

ASCII string “HUSB”

32.7.14 USBA Name2 Register

Name: IPNAME2

Access Type: Read-only

31	30	29	28	27	26	25	24
IP_NAME2							

23	22	21	20	19	18	17	16
IP_NAME2							

15	14	13	12	11	10	9	8
IP_NAME2							

7	6	5	4	3	2	1	0
IP_NAME2							

- **IP_NAME2**

ASCII string “2DEV”

32.7.15 USBA Features Register

Name: IPFEATURES

Access Type: Read-only

31	30	29	28	27	26	25	24

23	22	21	20	19	18	17	16
ISO_EPT_7	ISO_EPT_6	ISO_EPT_5	ISO_EPT_4	ISO_EPT_3	ISO_EPT_2	ISO_EPT_1	DATAB16_8

15	14	13	12	11	10	9	8
BW_DPRAM	FIFO_MAX_SIZE			DMA_FIFO_WORD_DEPTH			

7	6	5	4	3	2	1	0
DMA_B_SIZ	DMA_CHANNEL_NBR			EPT_NBR_MAX			

- **EPT_NBR_MAX: Max Number of Endpoints**

Give the max number of endpoints.

0 = if 16 endpoints are hardware implemented.

1 = if 1 endpoint is hardware implemented.

2 = if 2 endpoints are hardware implemented.

...

15 = if 15 endpoints are hardware implemented.

- **DMA_CHANNEL_NBR: Number of DMA Channels**

Give the number of DMA channels.

1 = if 1 DMA channel is hardware implemented.

2 = if 2 DMA channels are hardware implemented.

...

7 = if 7 DMA channels are hardware implemented.

- **DMA_B_SIZ: DMA Buffer Size**

0 = if the DMA Buffer size is 16 bits.

1 = if the DMA Buffer size is 24 bits.

- **DMA_FIFO_WORD_DEPTH: DMA FIFO Depth in Words**

0 = if FIFO is 16 words deep.

1 = if FIFO is 1 word deep.

2 = if FIFO is 2 words deep.

...

15 = if FIFO is 15 words deep.

- **FIFO_MAX_SIZE: DPRAM Size**

0 = if DPRAM is 128 bytes deep.

1 = if DPRAM is 256 bytes deep.

2 = if DPRAM is 512 bytes deep.

3 = if DPRAM is 1024 bytes deep.

4 = if DPRAM is 2048 bytes deep.

5 = if DPRAM is 4096 bytes deep.

6 = if DPRAM is 8192 bytes deep.

7 = if DPRAM is 16384 bytes deep.

- **BW_DPRAM: DPRAM Byte Write Capability**

0 = if DPRAM Write Data Shadow logic is implemented.

1 = if DPRAM is byte write capable.

- **DATAB16_8: UTMI DataBus16_8**

0 = if the UTMI uses an 8-bit parallel data interface (60 MHz, unidirectional).

1 = if the UTMI uses a 16-bit parallel data interface (30 MHz, bidirectional).

- **ISO_EPT_x: Endpointx High Bandwidth Isochronous Capability**

0 = if the endpoint does not have isochronous High Bandwidth Capability.

1 = if the endpoint has isochronous High Bandwidth Capability.

32.7.16 USBA IP Version Register

Name: IPVERSION

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	METAL_FIX_NUM		

15	14	13	12	11	10	9	8
VERSION_NUM							

7	6	5	4	3	2	1	0
VERSION_NUM							

- **VERSION_NUM: IP Version**

Give the IP version.

- **METAL_FIX_NUM: Number of metal fixes**

Give the number of metal fixes.

32.7.17 USBA Endpoint Configuration Register

Name: EPTCFGx

Access Type: Read/Write

31	30	29	28	27	26	25	24
EPT_MAPD	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	NB_TRANS	
7	6	5	4	3	2	1	0
BK_NUMBER		EPT_TYPE		EPT_DIR	EPT_SIZE		

- **EPT_SIZE: Endpoint Size**

Read and write:

Set this field according to the endpoint size in bytes (see Section 32.6.4 ”Endpoint Configuration”).

Endpoint Size

000	8 bytes
001	16 bytes
010	32 bytes
011	64 bytes
100	128 bytes
101	256 bytes
110	512 bytes
111	1024 bytes(1)

Note: 1. 1024 bytes is only for isochronous endpoint.

- **EPT_DIR: Endpoint Direction**

Read and write:

0 = Clear this bit to configure OUT direction for Bulk, Interrupt and Isochronous endpoints.

1 = set this bit to configure IN direction for Bulk, Interrupt and Isochronous endpoints.

For Control endpoints this bit has no effect and should be left at zero.

- **EPT_TYPE: Endpoint Type**

Read and write:

Set this field according to the endpoint type (see Section 32.6.4 ”Endpoint Configuration”).

(Endpoint 0 should always be configured as control)

Endpoint Type:

00	Control endpoint
01	Isochronous endpoint
10	Bulk endpoint
11	Interrupt endpoint

- **BK_NUMBER: Number of Banks**

Read and write:

Set this field according to the endpoint's number of banks (see Section 32.6.4 "Endpoint Configuration").

Number of Banks

00	Zero bank, the endpoint is not mapped in memory
01	One bank (bank 0)
10	Double bank (Ping-Pong: bank 0/bank 1)
11	Triple bank (bank 0/bank 1/bank 2)

- **NB_TRANS: Number Of Transaction per Microframe**

Read and Write:

The Number of transactions per microframe is set by software.

Note: Meaningful for high bandwidth isochronous endpoint only.

- **EPT_MAPD: Endpoint Mapped**

Read-only:

0 = the user should reprogram the register with correct values.

1 = set by hardware when the endpoint size (EPT_SIZE) and the number of banks (BK_NUMBER) are correct regarding:

- the fifo max capacity (FIFO_MAX_SIZE in IPFEATURES register)
- the number of endpoints/banks already allocated
- the number of allowed banks for this endpoint

32.7.18 USBA Endpoint Control Enable Register

Name: EPTCTLENBx

Access Type: Write-only

31	30	29	28	27	26	25	24
SHRT_PCKT	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	BUSY_BANK	–	–

15	14	13	12	11	10	9	8
NAK_OUT	NAK_IN/ ERR_FLUSH	STALL_SNT/ ERR_CRISO/ ERR_NBTRA	RX_SETUP/ ERR_FL_ISO	TX_PK_RDY/ ERR_TRANS	TX_COMPLT	RX_BK_RDY	ERR_OVFLW

7	6	5	4	3	2	1	0
MDATA_RX	DATAX_RX	–	NYET_DIS	INTDIS_DMA	–	AUTO_VALID	EPT_ENABL

For additional Information, see ”USBA Endpoint Control Register” on page 722.

- **EPT_ENABL: Endpoint Enable**

0 = no effect.

1 = enable endpoint according to the device configuration.

- **AUTO_VALID: Packet Auto-Valid Enable**

0 = no effect.

1 = enable this bit to automatically validate the current packet and switch to the next bank for both IN and OUT transfers.

- **INTDIS_DMA: Interrupts Disable DMA**

0 = no effect.

1 = If set, when an enabled endpoint-originated interrupt is triggered, the DMA request is disabled.

- **NYET_DIS: NYET Disable (Only for High Speed Bulk OUT endpoints)**

0 = no effect.

1 = forces an ACK response to the next High Speed Bulk OUT transfer instead of a NYET response.

- **DATAX_RX: DATAx Interrupt Enable (Only for high bandwidth Isochronous OUT endpoints)**

0 = no effect.

1 = enable DATAx Interrupt.

- **MDATA_RX: MDATA Interrupt Enable (Only for high bandwidth Isochronous OUT endpoints)**

0 = no effect.

1 = enable MDATA Interrupt.

- **ERR_OVFLW: Overflow Error Interrupt Enable**

0 = no effect.

1 = enable Overflow Error Interrupt.

- **RX_BK_RDY: Received OUT Data Interrupt Enable**

0 = no effect.

1 = enable Received OUT Data Interrupt.

- **TX_COMPLT: Transmitted IN Data Complete Interrupt Enable**

0 = no effect.

1 = enable Transmitted IN Data Complete Interrupt.

- **TX_PK_RDY/ERR_TRANS: TX Packet Ready/Transaction Error Interrupt Enable**

0 = no effect.

1 = enable TX Packet Ready/Transaction Error Interrupt.

- **RX_SETUP/ERR_FL_ISO: Received SETUP/Error Flow Interrupt Enable**

0 = no effect.

1 = enable RX_SETUP/Error Flow ISO Interrupt.

- **STALL_SNT/ERR_CRISO/ERR_NBTRA: Stall Sent /ISO CRC Error/Number of Transaction Error Interrupt Enable**

0 = no effect.

1 = enable Stall Sent/Error CRC ISO/Error Number of Transaction Interrupt.

- **NAK_IN/ERR_FLUSH: NAKIN/Bank Flush Error Interrupt Enable**

0 = no effect.

1 = enable NAKIN/Bank Flush Error Interrupt.

- **NAK_OUT: NAKOUT Interrupt Enable**

0 = no effect.

1 = enable NAKOUT Interrupt.

- **BUSY_BANK: Busy Bank Interrupt Enable**

0 = no effect.

1 = enable Busy Bank Interrupt.

- **SHRT_PCKT: Short Packet Send/Short Packet Interrupt Enable**

For OUT endpoints:

0 = no effect.

1 = enable Short Packet Interrupt.

For IN endpoints:

Guarantees short packet at end of DMA Transfer if the DMACONTROLx register END_B_EN and EPTCTLx register AUTOVALID bits are also set.

32.7.19 USBA Endpoint Control Disable Register

Name: EPTCTLDISx

Access Type: Write-only

31	30	29	28	27	26	25	24
SHRT_PCKT	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	BUSY_BANK	–	–
15	14	13	12	11	10	9	8
NAK_OUT	NAK_IN/ ERR_FLUSH	STALL_SNT/ ERR_CRISO/ ERR_NBTRA	RX_SETUP/ ERR_FL_ISO	TX_PK_RDY/ ERR_TRANS	TX_COMPLT	RX_BK_RDY	ERR_OVFLW
7	6	5	4	3	2	1	0
MDATA_RX	DATAX_RX	–	NYET_DIS	INTDIS_DMA	–	AUTO_VALID	EPT_DISABL

For additional Information, see ”USBA Endpoint Control Register” on page 722.

- **EPT_DISABL: Endpoint Disable**

0 = no effect.

1 = disable endpoint.

- **AUTO_VALID: Packet Auto-Valid Disable**

0 = no effect.

1 = disable this bit to not automatically validate the current packet.

- **INTDIS_DMA: Interrupts Disable DMA**

0 = no effect.

1 = disable the “Interrupts Disable DMA”.

- **NYET_DIS: NYET Enable (Only for High Speed Bulk OUT endpoints)**

0 = no effect.

1 = let the hardware handle the handshake response for the High Speed Bulk OUT transfer.

- **DATAX_RX: DATAx Interrupt Disable (Only for High Bandwidth Isochronous OUT endpoints)**

0 = no effect.

1 = disable DATAx Interrupt.

- **MDATA_RX: MDATA Interrupt Disable (Only for High Bandwidth Isochronous OUT endpoints)**

0 = no effect.

1 = disable MDATA Interrupt.

- **ERR_OVFLW: Overflow Error Interrupt Disable**

0 = no effect.

1 = disable Overflow Error Interrupt.

- **RX_BK_RDY: Received OUT Data Interrupt Disable**

0 = no effect.

1 = disable Received OUT Data Interrupt.

- **TX_COMPLT: Transmitted IN Data Complete Interrupt Disable**

0 = no effect.

1 = disable Transmitted IN Data Complete Interrupt.

- **TX_PK_RDY/ERR_TRANS: TX Packet Ready/Transaction Error Interrupt Disable**

0 = no effect.

1 = disable TX Packet Ready/Transaction Error Interrupt.

- **RX_SETUP/ERR_FL_ISO: Received SETUP/Error Flow Interrupt Disable**

0 = no effect.

1 = disable RX_SETUP/Error Flow ISO Interrupt.

- **STALL_SNT/ERR_CRISO/ERR_NBTRA: Stall Sent/ISO CRC Error/Number of Transaction Error Interrupt Disable**

0 = no effect.

1 = disable Stall Sent/Error CRC ISO/Error Number of Transaction Interrupt.

- **NAK_IN/ERR_FLUSH: NAKIN/bank flush error Interrupt Disable**

0 = no effect.

1 = disable NAKIN/ Bank Flush Error Interrupt.

- **NAK_OUT: NAKOUT Interrupt Disable**

0 = no effect.

1 = disable NAKOUT Interrupt.

- **BUSY_BANK: Busy Bank Interrupt Disable**

0 = no effect.

1 = disable Busy Bank Interrupt.

- **SHRT_PCKT: Short Packet Interrupt Disable**

For OUT endpoints:

0 = no effect.

1 = disable Short Packet Interrupt.

For IN endpoints:

Never automatically add a zero length packet at end of DMA transfer.

.

32.7.20 USBA Endpoint Control Register

Name: EPTCTLx

Access Type: Read-only

31	30	29	28	27	26	25	24
SHRT_PCKT	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	BUSY_BANK	–	–

15	14	13	12	11	10	9	8
NAK_OUT	NAK_IN/ ERR_FLUSH	STALL_SNT/ ERR_CRISO/ ERR_NBTRA	RX_SETUP/ ERR_FL_ISO	TX_PK_RDY/ ERR_TRANS	TX_COMPLT	RX_BK_RDY	ERR_OVFLW

7	6	5	4	3	2	1	0
MDATA_RX	DATAX_RX	–	NYET_DIS	INTDIS_DMA	–	AUTO_VALID	EPT_ENABL

- **EPT_ENABL: Endpoint Enable**

0 = If cleared, the endpoint is disabled according to the device configuration. Endpoint 0 should always be enabled after a hardware or USBA bus reset and participate in the device configuration.

1 = If set, the endpoint is enabled according to the device configuration.

- **AUTO_VALID: Packet Auto-Valid Enabled (Not for CONTROL Endpoints)**

Set this bit to automatically validate the current packet and switch to the next bank for both IN and OUT endpoints.

For IN Transfer:

If this bit is set, then the EPTSTAx register TX_PK_RDY bit is set automatically when the current bank is full and at the end of DMA buffer if the DMACONTROLx register END_B_EN bit is set.

The user may still set the EPTSTAx register TX_PK_RDY bit if the current bank is not full, unless the user wants to send a Zero Length Packet by software.

For OUT Transfer:

If this bit is set, then the EPTSTAx register RX_BK_RDY bit is automatically reset for the current bank when the last packet byte has been read from the bank FIFO or at the end of DMA buffer if the DMACONTROLx register END_B_EN bit is set. For example, to truncate a padded data packet when the actual data transfer size is reached.

The user may still clear the EPTSTAx register RX_BK_RDY bit, for example, after completing a DMA buffer by software if DMACONTROLx register END_B_EN bit was disabled or in order to cancel the read of the remaining data bank(s).

- **INTDIS_DMA: Interrupt Disables DMA**

If set, when an enabled endpoint-originated interrupt is triggered, the DMA request is disabled regardless of the IEN register EPT_INT_x bit for this endpoint. Then, the firmware will have to clear or disable the interrupt source or clear this bit if transfer completion is needed.

If the exception raised is associated with the new system bank packet, then the previous DMA packet transfer is normally completed, but the new DMA packet transfer is not started (not requested).

If the exception raised is not associated to a new system bank packet (NAK_IN, NAK_OUT, ERR_FL_ISO...), then the request cancellation may happen at any time and may immediately stop the current DMA transfer.

This may be used, for example, to identify or prevent an erroneous packet to be transferred into a buffer or to complete a DMA buffer by software after reception of a short packet, or to perform buffer truncation on ERR_FL_ISO interrupt for adaptive rate.

- **NYET_DIS: NYET Disable (Only for High Speed Bulk OUT endpoints)**

0 = If clear, this bit lets the hardware handle the handshake response for the High Speed Bulk OUT transfer.

1 = If set, this bit forces an ACK response to the next High Speed Bulk OUT transfer instead of a NYET response.

Note: According to the *Universal Serial Bus Specification, Rev 2.0* (8.5.1.1 NAK Responses to OUT/DATA During PING Protocol), a NAK response to an HS Bulk OUT transfer is expected to be an unusual occurrence.

- **DATAX_RX: DATAx Interrupt Enabled (Only for High Bandwidth Isochronous OUT endpoints)**

0 = no effect.

1 = send an interrupt when a DATA2, DATA1 or DATA0 packet has been received meaning the whole microframe data payload has been received.

- **MDATA_RX: MDATA Interrupt Enabled (Only for High Bandwidth Isochronous OUT endpoints)**

0 = no effect.

1 = send an interrupt when an MDATA packet has been received and so at least one packet of the microframe data payload has been received.

- **ERR_OVFLW: Overflow Error Interrupt Enabled**

0 = Overflow Error Interrupt is masked.

1 = Overflow Error Interrupt is enabled.

- **RX_BK_RDY: Received OUT Data Interrupt Enabled**

0 = Received OUT Data Interrupt is masked.

1 = Received OUT Data Interrupt is enabled.

- **TX_COMPLT: Transmitted IN Data Complete Interrupt Enabled**

0 = Transmitted IN Data Complete Interrupt is masked.

1 = Transmitted IN Data Complete Interrupt is enabled.

- **TX_PK_RDY/ERR_TRANS: TX Packet Ready/Transaction Error Interrupt Enabled**

0 = TX Packet Ready/Transaction Error Interrupt is masked.

1 = TX Packet Ready/Transaction Error Interrupt is enabled.

Caution: Interrupt source is active as long as the corresponding EPTSTAx register TX_PK_RDY flag remains low. If there are no more banks available for transmitting after the software has set EPTSTAx/TX_PK_RDY for the last transmit packet, then the interrupt source remains inactive until the first bank becomes free again to transmit at EPTSTAx/TX_PK_RDY hardware clear.

- **RX_SETUP/ERR_FL_ISO: Received SETUP/Error Flow Interrupt Enabled**

0 = Received SETUP/Error Flow Interrupt is masked.

1 = Received SETUP/Error Flow Interrupt is enabled.

- **STALL_SNT/ERR_CRISO/ERR_NBTRA: Stall Sent/ISO CRC Error/Number of Transaction Error Interrupt Enabled**

0 = Stall Sent/ISO CRC error/number of Transaction Error Interrupt is masked.

1 = Stall Sent /ISO CRC error/number of Transaction Error Interrupt is enabled.

- **NAK_IN/ERR_FLUSH: NAKIN/Bank Flush Error Interrupt Enabled**

0 = NAKIN Interrupt is masked.

1 = NAKIN/Bank Flush Error Interrupt is enabled.

- **NAK_OUT: NAKOUT Interrupt Enabled**

0 = NAKOUT Interrupt is masked.

1 = NAKOUT Interrupt is enabled.

- **BUSY_BANK: Busy Bank Interrupt Enabled**

0 = BUSY_BANK Interrupt is masked.

1 = BUSY_BANK Interrupt is enabled.

For OUT endpoints: an interrupt is sent when all banks are busy.

For IN endpoints: an interrupt is sent when all banks are free**.**

- **SHRT_PCKT: Short Packet Interrupt Enabled**

For OUT endpoints: send an Interrupt when a Short Packet has been received.

0 = Short Packet Interrupt is masked.

1 = Short Packet Interrupt is enabled.

For IN endpoints: a Short Packet transmission is guaranteed upon end of the DMA Transfer, thus signaling a BULK or INTERRUPT end of transfer or an end of isochronous (micro-)frame data, but only if the DMACONTROLx register END_B_EN and EPTCTLx register AUTO_VALID bits are also set.

32.7.21 USBA Endpoint Set Status Register

Name: EPTSETSTAx

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	TX_PK_RDY	–	KILL_BANK	–
7	6	5	4	3	2	1	0
–	–	FRCESTALL	–	–	–	–	–

- **FRCESTALL: Stall Handshake Request Set**

0 = no effect.

1 = set this bit to request a STALL answer to the host for the next handshake

Refer to chapters 8.4.5 (Handshake Packets) and 9.4.5 (Get Status) of the *Universal Serial Bus Specification, Rev 2.0* for more information on the STALL handshake.

- **KILL_BANK: KILL Bank Set (for IN Endpoint)**

0 = no effect.

1 = kill the last written bank.

- **TX_PK_RDY: TX Packet Ready Set**

0 = no effect.

1 = set this bit after a packet has been written into the endpoint FIFO for IN data transfers

  – This flag is used to generate a Data IN transaction (device to host).
  – Device firmware checks that it can write a data payload in the FIFO, checking that TX_PK_RDY is cleared.
  – Transfer to the FIFO is done by writing in the “Buffer Address” register.
  – Once the data payload has been transferred to the FIFO, the firmware notifies the USBA device setting TX_PK_RDY to one.
  – USBA bus transactions can start.
  – TXCOMP is set once the data payload has been received by the host.
  – Data should be written into the endpoint FIFO only after this bit has been cleared.
  – Set this bit without writing data to the endpoint FIFO to send a Zero Length Packet.

32.7.22 USBA Endpoint Clear Status Register

Name: EPTCLRSTAx

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
NAK_OUT	NAK_IN/ ERR_FLUSH	STALL_SNT/ ERR_NBTRA	RX_SETUP/ ERR_FL_ISO	–	TX_COMPLT	RX_BK_RDY	–

7	6	5	4	3	2	1	0
–	TOGGLESQ	FRCESTALL	–	–	–	–	–

- **FRCESTALL: Stall Handshake Request Clear**

0 = no effect.

1 = clear the STALL request. The next packets from host will not be STALLed.

- **TOGGLESQ: Data Toggle Clear**

0 = no effect.

1 = clear the PID data of the current bank

For OUT endpoints, the next received packet should be a DATA0.

For IN endpoints, the next packet will be sent with a DATA0 PID.

- **RX_BK_RDY: Received OUT Data Clear**

0 = no effect.

1 = clear the RX_BK_RDY flag of EPTSTAx.

- **TX_COMPLT: Transmitted IN Data Complete Clear**

0 = no effect.

1 = clear the TX_COMPLT flag of EPTSTAx.

- **RX_SETUP/ERR_FL_ISO: Received SETUP/Error Flow Clear**

0 = no effect.

1 = clear the RX_SETUP/ERR_FL_ISO flags of EPTSTAx.

- **STALL_SNT/ERR_NBTRA: Stall Sent/Number of Transaction Error Clear**

0 = no effect.

1 = clear the STALL_SNT/ERR_NBTRA flags of EPTSTAx.

- **NAK_IN/ERR_FLUSH: NAKIN/Bank Flush Error Clear**

0 = no effect.

1 = clear the NAK_IN/ERR_FLUSH flags of EPTSTAx.

- **NAK_OUT: NAKOUT Clear**

0 = no effect.

1 = clear the NAK_OUT flag of EPTSTAx.

32.7.23 USBA Endpoint Status Register

Name: EPTSTAx

Access Type: Read-only

31	30	29	28	27	26	25	24
SHRT_PCKT	BYTE_COUNT						

23	22	21	20	19	18	17	16
BYTE_COUNT				BUSY_BANK_STA		CURRENT_BANK/ CONTROL_DIR	

15	14	13	12	11	10	9	8
NAK_OUT	NAK_IN/ ERR_FLUSH	STALL_SNT/ ERR_CRISO/ ERR_NBTRA	RX_SETUP/ ERR_FL_ISO	TX_PK_RDY/ ERR_TRANS	TX_COMPLT	RX_BK_RDY/ KILL_BANK	ERR_OVFLW

7	6	5	4	3	2	1	0
TOGGLESQ_STA		FRCESTALL	–	–	–	–	–

- **FRCESTALL: Stall Handshake Request**

0 = no effect.

1= If set a STALL answer will be done to the host for the next handshake.

This bit is reset by hardware upon received SETUP.

- **TOGGLESQ_STA: Toggle Sequencing**

Toggle Sequencing:

IN endpoint: it indicates the PID Data Toggle that will be used for the next packet sent. This is not relative to the current bank.

CONTROL and OUT endpoint:

These bits are set by hardware to indicate the PID data of the current bank:

00	Data0
01	Data1
10	Data2 (only for High Bandwidth Isochronous Endpoint)
11	MData (only for High Bandwidth Isochronous Endpoint)

Note 1: In OUT transfer, the Toggle information is meaningful only when the current bank is busy (Received OUT Data = 1).

Note 2: These bits are updated for OUT transfer:

– a new data has been written into the current bank.

– the user has just cleared the Received OUT Data bit to switch to the next bank.

Note 3: For High Bandwidth Isochronous Out endpoint, it is recommended to check the EPTSTAx/ERR_TRANS bit to know if the toggle sequencing is correct or not.

Note 4: This field is reset to DATA1 by the EPTCLRSTAx register TOGGLESQ bit, and by EPTCTLDISx (disable endpoint).

- **ERR_OVFLW: Overflow Error**

This bit is set by hardware when a new too-long packet is received.

Example: If the user programs an endpoint 64 bytes wide and the host sends 128 bytes in an OUT transfer, then the Overflow Error bit is set.

This bit is updated at the same time as the BYTE_COUNT field.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPTCTLDISx (disable endpoint).

- **RX_BK_RDY/KILL_BANK: Received OUT Data/KILL Bank**

Received OUT Data: (For OUT endpoint or Control endpoint)

This bit is set by hardware after a new packet has been stored in the endpoint FIFO.

This bit is cleared by the device firmware after reading the OUT data from the endpoint.

For multi-bank endpoints, this bit may remain active even when cleared by the device firmware, this if an other packet has been received meanwhile.

Hardware assertion of this bit may generate an interrupt if enabled by the EPTCTLx register RX_BK_RDY bit.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPTCTLDISx (disable endpoint).

KILL Bank: (For IN endpoint)

  – the bank is really cleared or the bank is sent, BUSY_BANK_STA is decremented.
  – the bank is not cleared but sent on the IN transfer, TX_COMPLT
  – the bank is not cleared because it was empty. The user should wait that this bit is cleared before trying to clear another packet.

Note: “Kill a packet” may be refused if at the same time, an IN token is coming and the current packet is sent on the USBA line. In this case, the TX_COMPLT bit is set. Take notice however, that if at least two banks are ready to be sent, there is no problem to kill a packet even if an IN token is coming. In fact, in that case, the current bank is sent (IN transfer) and the last bank is killed.

- **TX_COMPLT: Transmitted IN Data Complete**

This bit is set by hardware after an IN packet has been transmitted for isochronous endpoints and after it has been accepted (ACK’ed) by the host for Control, Bulk and Interrupt endpoints.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint), and by EPTCTLDISx (disable endpoint).

- **TX_PK_RDY/ERR_TRANS: TX Packet Ready/Transaction Error**

TX Packet Ready:

This bit is cleared by hardware, as soon as the packet has been sent for isochronous endpoints, or after the host has acknowledged the packet for Control, Bulk and Interrupt endpoints.

For Multi-bank endpoints, this bit may remain clear even after software is set if another bank is available to transmit.

Hardware clear of this bit may generate an interrupt if enabled by the EPTCTLx register TX_PK_RDY bit.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint), and by EPTCTLDISx (disable endpoint).

Transaction Error: (For high bandwidth isochronous OUT endpoints) (Read-Only)

This bit is set by hardware when a transaction error occurs inside one microframe.

If one toggle sequencing problem occurs among the n-transactions (n = 1, 2 or 3) inside a microframe, then this bit is still set as long as the current bank contains one “bad” n-transaction. (see ”CURRENT_BANK/CONTROL_DIR: Current

Bank/Control Direction" on page 731) As soon as the current bank is relative to a new "good" n-transactions, then this bit is reset.

Note1: A transaction error occurs when the toggle sequencing does not respect the *Universal Serial Bus Specification, Rev 2.0* (5.9.2 High Bandwidth Isochronous endpoints) (Bad PID, missing data....)

Note2: When a transaction error occurs, the user may empty all the "bad" transactions by clearing the Received OUT Data flag (RX_BK_RDY).

If this bit is reset, then the user should consider that a new n-transaction is coming.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint), and by EPTCTLDISx (disable endpoint).

- **RX_SETUP/ERR_FL_ISO: Received SETUP/Error Flow**

Received SETUP: (for Control endpoint only)

This bit is set by hardware when a valid SETUP packet has been received from the host.

It is cleared by the device firmware after reading the SETUP data from the endpoint FIFO.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint), and by EPTCTLDISx (disable endpoint).

Error Flow: (for isochronous endpoint only)

This bit is set by hardware when a transaction error occurs.

- Isochronous IN transaction is missed, the micro has no time to fill the endpoint (underflow).
- Isochronous OUT data is dropped because the bank is busy (overflow).

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPTCTLDISx (disable endpoint).

- **STALL_SNT/ERR_CRISO/ERR_NBTRA: Stall Sent/CRC ISO Error/Number of Transaction Error**

STALL_SNT: (for Control, Bulk and Interrupt endpoints)

This bit is set by hardware after a STALL handshake has been sent as requested by the EPTSTAx register FRCESTALL bit.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPTCTLDISx (disable endpoint).

ERR_CRISO: (for Isochronous OUT endpoints) (Read-only)

This bit is set by hardware if the last received data is corrupted (CRC error on data).

This bit is updated by hardware when new data is received (Received OUT Data bit).

ERR_NBTRA: (for High Bandwidth Isochronous IN endpoints)

This bit is set at the end of a microframe in which at least one data bank has been transmitted, if less than the number of transactions per micro-frame banks (EPTCFGx register NB_TRANS) have been validated for transmission inside this microframe.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPTCTLDISx (disable endpoint).

- **NAK_IN/ERR_FLUSH: NAK IN/Bank Flush Error**

NAK_IN:

This bit is set by hardware when a NAK handshake has been sent in response to an IN request from the Host.

This bit is cleared by software.

ERR_FLUSH: (for High Bandwidth Isochronous IN endpoints)

This bit is set when flushing unsent banks at the end of a microframe.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPT_CTL_DISx (disable endpoint).

- **NAK_OUT: NAK OUT**

This bit is set by hardware when a NAK handshake has been sent in response to an OUT or PING request from the Host.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPT_CTL_DISx (disable endpoint).

- **CURRENT_BANK/CONTROL_DIR: Current Bank/Control Direction**

Current Bank: (all endpoints except Control endpoint)

These bits are set by hardware to indicate the number of the current bank.

00	Bank 0 (or single bank)
01	Bank 1
10	Bank 2
11	Invalid

Note: the current bank is updated each time the user:

– Sets the TX Packet Ready bit to prepare the next IN transfer and to switch to the next bank.

– Clears the received OUT data bit to access the next bank.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPTCTLDISx (disable endpoint).

Control Direction: (for Control endpoint only)

0 = a Control Write is requested by the Host.

1 = a Control Read is requested by the Host.

Note1: This bit corresponds with the 7th bit of the bmRequestType (Byte 0 of the Setup Data).

Note2: This bit is updated after receiving new setup data.

- **BUSY_BANK_STA: Busy Bank Number**

These bits are set by hardware to indicate the number of busy banks.

IN endpoint: it indicates the number of busy banks filled by the user, ready for IN transfer.

OUT endpoint: it indicates the number of busy banks filled by OUT transaction from the Host.

00	All banks are free
01	1 busy bank
10	2 busy banks
11	3 busy banks

- **BYTE_COUNT: USBA Byte Count**

Byte count of a received data packet.

This field is incremented after each write into the endpoint (to prepare an IN transfer).

This field is decremented after each reading into the endpoint (OUT transfer).

This field is also updated at RX_BK_RDY flag clear with the next bank.

This field is also updated at TX_PK_RDY flag set with the next bank.

This field is reset by RST_EPT_x of EPTRST register.

- **SHRT_PCKT: Short Packet**

An OUT Short Packet is detected when the receive byte count is less than the configured EPTCFGx register EPT_Size.

This bit is updated at the same time as the BYTE_COUNT field.

This bit is reset by EPTRST register RST_EPT_x (reset endpoint) and by EPTCTLDISx (disable endpoint).

32.7.24 USBA DMA Channel Transfer Descriptor

The DMA channel transfer descriptor is loaded from the memory.

Be careful with the alignment of this buffer.

The structure of the DMA channel transfer descriptor is defined by three parameters as described below:

Offset 0:

The address must be aligned: 0xXXXX0

Next Descriptor Address Register: DMANXTDSCx

Offset 4:

The address must be aligned: 0xXXXX4

DMA Channelx Address Register: DMAADDRESSx

Offset 8:

The address must be aligned: 0xXXXX8

DMA Channelx Control Register: DMACONTROLx

To use the DMA channel transfer descriptor, fill the structures with the correct value (as described in the following pages).

Then write directly in DMANXTDSCx the address of the descriptor to be used first.

Then write 1 in the LDNXT_DSC bit of DMACONTROLx (load next channel transfer descriptor). The descriptor is automatically loaded upon Endpointx request for packet transfer.

32.7.25 USBA DMA Next Descriptor Address Register

Name: DMANXTDSCx

Access Type: Read/Write

31	30	29	28	27	26	25	24
NXT_DSC_ADD							

23	22	21	20	19	18	17	16
NXT_DSC_ADD							

15	14	13	12	11	10	9	8
NXT_DSC_ADD							

7	6	5	4	3	2	1	0
NXT_DSC_ADD							

- **NXT_DSC_ADD**

This field points to the next channel descriptor to be processed. This channel descriptor must be aligned, so bits 0 to 3 of the address must be equal to zero.

32.7.26 USBA DMA Channelx Address Register

Name: DMAADDRESSx

Access Type: Read/Write

31	30	29	28	27	26	25	24
BUFF_ADD							

23	22	21	20	19	18	17	16
BUFF_ADD							

15	14	13	12	11	10	9	8
BUFF_ADD							

7	6	5	4	3	2	1	0
BUFF_ADD							

- **BUFF_ADD**

This field determines the HSB bus starting address of a DMA channel transfer.

Channel start and end addresses may be aligned on any byte boundary.

The firmware may write this field only when the DMASTATUS register CHANN_ENB bit is clear.

This field is updated at the end of the address phase of the current access to the HSB bus. It is incrementing of the access byte width. The access width is 4 bytes (or less) at packet start or end, if the start or end address is not aligned on a word boundary.

The packet start address is either the channel start address or the next channel address to be accessed in the channel buffer.

The packet end address is either the channel end address or the latest channel address accessed in the channel buffer.

The channel start address is written by software or loaded from the descriptor, whereas the channel end address is either determined by the end of buffer or the USBA device, USB end of transfer if the DMACONTROLx register END_TR_EN bit is set.

32.7.27 USBA DMA Channelx Control Register

Name: DMACONTROLx

Access Type: Read/Write

31	30	29	28	27	26	25	24
BUFF_LENGTH							
23	22	21	20	19	18	17	16
BUFF_LENGTH							
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB

- **CHANN_ENB (Channel Enable Command)**

0 = DMA channel is disabled at and no transfer will occur upon request. This bit is also cleared by hardware when the channel source bus is disabled at end of buffer.

If the DMACONTROL register LDNXT_DSC bit has been cleared by descriptor loading, the firmware will have to set the corresponding CHANN_ENB bit to start the described transfer, if needed.

If the DMACONTROL register LDNXT_DSC bit is cleared, the channel is frozen and the channel registers may then be read and/or written reliably as soon as both DMASTATUS register CHANN_ENB and CHANN_ACT flags read as 0.

If a channel request is currently serviced when this bit is cleared, the DMA FIFO buffer is drained until it is empty, then the DMASTATUS register CHANN_ENB bit is cleared.

If the LDNXT_DSC bit is set at or after this bit clearing, then the currently loaded descriptor is skipped (no data transfer occurs) and the next descriptor is immediately loaded.

1 = DMASTATUS register CHANN_ENB bit will be set, thus enabling DMA channel data transfer. Then any pending request will start the transfer. This may be used to start or resume any requested transfer.

- **LDNXT_DSC: Load Next Channel Transfer Descriptor Enable (Command)**

0 = no channel register is loaded after the end of the channel transfer.

1 = the channel controller loads the next descriptor after the end of the current transfer, i.e. when the DMASTATUS/CHANN_ENB bit is reset.

If the DMA CONTROL/CHANN_ENB bit is cleared, the next descriptor is immediately loaded upon transfer request.

DMA Channel Control Command Summary

LDNXT_DSC	CHANN_ENB	Description
0	0	Stop now
0	1	Run and stop at end of buffer
1	0	Load next descriptor now
1	1	Run and link at end of buffer

- **END_TR_EN: End of Transfer Enable (Control)**

Used for OUT transfers only.

0 = USB end of transfer is ignored.

1 = USBA device can put an end to the current buffer transfer.

When set, a BULK or INTERRUPT short packet or the last packet of an ISOCHRONOUS (micro) frame (DATAX) will close the current buffer and the DMASTATUSx register END_TR_ST flag will be raised.

This is intended for USBA non-prenegotiated end of transfer (BULK or INTERRUPT) or ISOCHRONOUS microframe data buffer closure.

- **END_B_EN: End of Buffer Enable (Control)**

0 = DMA Buffer End has no impact on USB packet transfer.

1 = endpoint can validate the packet (according to the values programmed in the EPTCTLx register AUTO_VALID and SHRT_PCKT fields) at DMA Buffer End, i.e. when the DMASTATUS register BUFF_COUNT reaches 0.

This is mainly for short packet IN validation initiated by the DMA reaching end of buffer, but could be used for OUT packet truncation (discarding of unwanted packet data) at the end of DMA buffer.

- **END_TR_IT: End of Transfer Interrupt Enable**

0 = USBA device initiated buffer transfer completion will not trigger any interrupt at STATUSx/END_TR_ST rising.

1 = an interrupt is sent after the buffer transfer is complete, if the USBA device has ended the buffer transfer.

Use when the receive size is unknown.

- **END_BUFFIT: End of Buffer Interrupt Enable**

0 = DMA_STATUSx/END_BF_ST rising will not trigger any interrupt.

1 = an interrupt is generated when the DMASTATUSx register BUFF_COUNT reaches zero.

- **DESC_LD_IT: Descriptor Loaded Interrupt Enable**

0 = DMASTATUSx/DESC_LDST rising will not trigger any interrupt.

1 = an interrupt is generated when a descriptor has been loaded from the bus.

- **BURST_LCK: Burst Lock Enable**

0 = the DMA never locks bus access.

1 = USB packets HSB data bursts are locked for maximum optimization of the bus bandwidth usage and maximization of fly-by HSB burst duration.

- **BUFF_LENGTH: Buffer Byte Length (Write-only)**

This field determines the number of bytes to be transferred until end of buffer. The maximum channel transfer size (64 KB) is reached when this field is 0 (default value). If the transfer size is unknown, this field should be set to 0, but the transfer end may occur earlier under USBA device control.

When this field is written, The DMASTATUSx register BUFF_COUNT field is updated with the write value.

Note: Bits [31:2] are only writable when issuing a channel Control Command other than “Stop Now”.

Note: For reliability it is highly recommended to wait for both DMASTATUSx register CHAN_ACT and CHAN_ENB flags are at 0, thus ensuring the channel has been stopped before issuing a command other than “Stop Now”.

32.7.28 USBA DMA Channelx Status Register

Name: DMASTATUSx

Access Type: Read/Write

31	30	29	28	27	26	25	24
BUFF_COUNT							

23	22	21	20	19	18	17	16
BUFF_COUNT							

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	DESC_LDST	END_BF_ST	END_TR_ST	–	–	CHANN_ACT	CHANN_ENB

- **CHANN_ENB: Channel Enable Status**

0 = if cleared, the DMA channel no longer transfers data, and may load the next descriptor if the DMACONTROLx register LDNXT_DSC bit is set.

When any transfer is ended either due to an elapsed byte count or a USBA device initiated transfer end, this bit is automatically reset.

1 = if set, the DMA channel is currently enabled and transfers data upon request.

This bit is normally set or cleared by writing into the DMACONTROLx register CHANN_ENB bit field either by software or descriptor loading.

If a channel request is currently serviced when the DMACONTROLx register CHANN_ENB bit is cleared, the DMA FIFO buffer is drained until it is empty, then this status bit is cleared.

- **CHANN_ACT: Channel Active Status**

0 = the DMA channel is no longer trying to source the packet data.

When a packet transfer is ended this bit is automatically reset.

1 = the DMA channel is currently trying to source packet data, i.e. selected as the highest-priority requesting channel.

When a packet transfer cannot be completed due to an END_BF_ST, this flag stays set during the next channel descriptor load (if any) and potentially until USBA packet transfer completion, if allowed by the new descriptor.

- **END_TR_ST: End of Channel Transfer Status**

0 = cleared automatically when read by software.

1 = set by hardware when the last packet transfer is complete, if the USBA device has ended the transfer.

Valid until the CHANN_ENB flag is cleared at the end of the next buffer transfer.

- **END_BF_ST: End of Channel Buffer Status**

0 = cleared automatically when read by software.

1 = set by hardware when the BUFF_COUNT downcount reach zero.

Valid until the CHANN_ENB flag is cleared at the end of the next buffer transfer.

- **DESC_LDST: Descriptor Loaded Status**

0 = cleared automatically when read by software.

1 = set by hardware when a descriptor has been loaded from the system bus.

Valid until the CHANN_ENB flag is cleared at the end of the next buffer transfer.

- **BUFF_COUNT: Buffer Byte Count**

This field determines the current number of bytes still to be transferred for this buffer.

This field is decremented from the HSB source bus access byte width at the end of this bus address phase.

The access byte width is 4 by default, or less, at DMA start or end, if the start or end address is not aligned on a word boundary.

At the end of buffer, the DMA accesses the USBA device only for the number of bytes needed to complete it.

This field value is reliable (stable) only if the channel has been stopped or frozen (EPTCTLx register NT_DIS_DMA bit is used to disable the channel request) and the channel is no longer active CHANN_ACT flag is 0.

Note: For OUT endpoints, if the receive buffer byte length (BUFF_LENGTH) has been defaulted to zero because the USB transfer length is unknown, the actual buffer byte length received will be 0x10000-BUFF_COUNT.

33. Timer/Counter (TC)

Rev: 2.0.0.1

33.1 Features

- **Three 16-bit Timer Counter channels**
- **A wide range of functions including:**
  - **Frequency measurement**
  - **Event counting**
  - **Interval measurement**
  - **Pulse generation**
  - **Delay timing**
  - **Pulse width modulation**
  - **Up/down capabilities**
- **Each channel is user-configurable and contains:**
  - **Three external clock inputs**
  - **Five internal clock inputs**
  - **Two multi-purpose input/output signals**
- **Internal interrupt signal**
- **Two global registers that act on all three TC channels**
- **Peripheral event input on all A lines in capture mode**

33.2 Overview

The Timer Counter (TC) includes three identical 16-bit Timer Counter channels.

Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing, and pulse width modulation.

Each channel has three external clock inputs, five internal clock inputs, and two multi-purpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts.

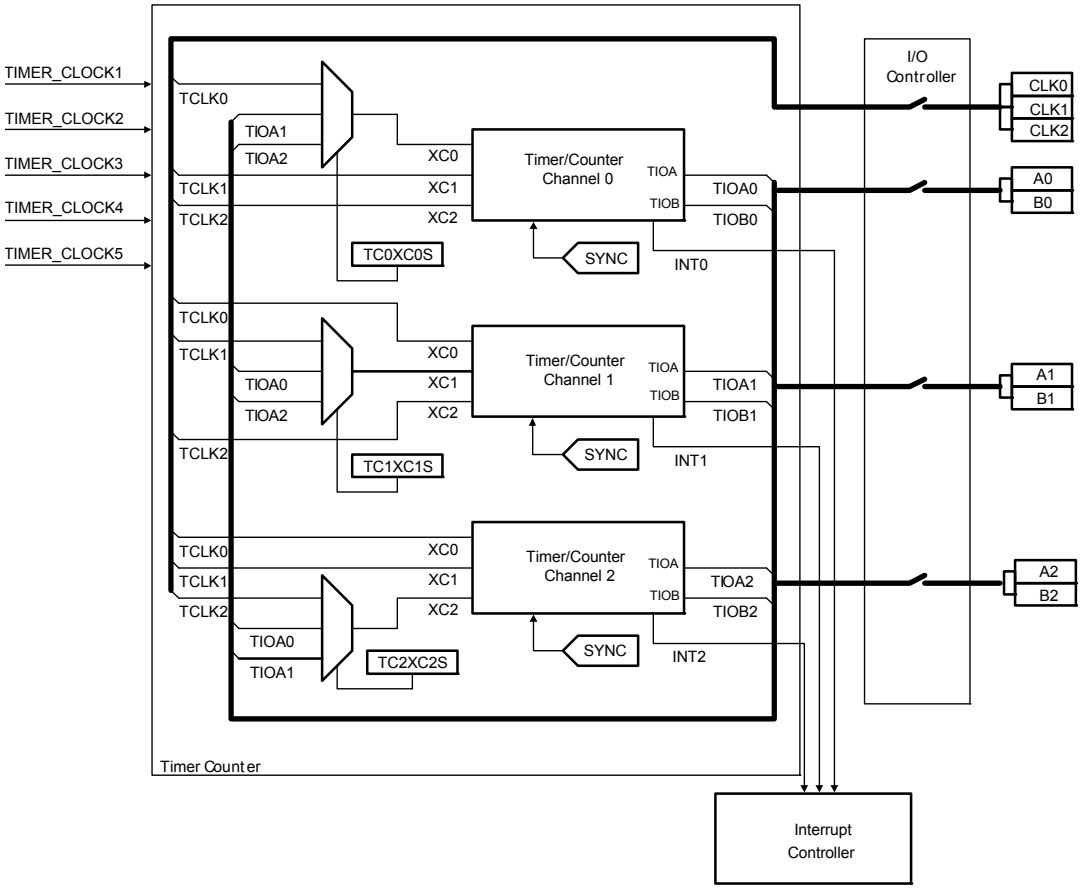
The TC block has two global registers which act upon all three TC channels.

The Block Control Register (BCR) allows the three channels to be started simultaneously with the same instruction.

The Block Mode Register (BMR) defines the external clock inputs for each channel, allowing them to be chained.

33.3 Block Diagram

Figure 33-1. TC Block Diagram



33.4 I/O Lines Description

Table 33-1. I/O Lines Description

Pin Name	Description	Type
CLK0-CLK2	External Clock Input	Input
A0-A2	I/O Line A	Input/Output
B0-B2	I/O Line B	Input/Output

33.5 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

33.5.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with I/O lines. The user must first program the I/O Controller to assign the TC pins to their peripheral functions.

When using the TIOA lines as inputs the user must make sure that no peripheral events are generated on the line. Refer to the Peripheral Event System chapter for details.

33.5.2 Power Management

If the CPU enters a sleep mode that disables clocks used by the TC, the TC will stop functioning and resume operation after the system wakes up from sleep mode.

33.5.3 Clocks

The clock for the TC bus interface (CLK_TC) is generated by the Power Manager. This clock is enabled at reset, and can be disabled in the Power Manager. It is recommended to disable the TC before disabling the clock, to avoid freezing the TC in an undefined state.

33.5.4 Interrupts

The TC interrupt request line is connected to the interrupt controller. Using the TC interrupt requires the interrupt controller to be programmed first.

33.5.5 Peripheral Events

The TC peripheral events are connected via the Peripheral Event System. Refer to the Peripheral Event System chapter for details.

33.5.6 Debug Operation

The Timer Counter clocks are frozen during debug operation, unless the OCD system keeps peripherals running in debug operation.

33.6 Functional Description

33.6.1 TC Description

The three channels of the Timer Counter are independent and identical in operation. The registers for channel programming are listed in Figure 33-3 on page 757.

33.6.1.1 Channel I/O Signals

As described in Figure 33-1 on page 741, each Channel has the following I/O signals.

Table 33-2. Channel I/O Signals Description

Block/Channel	Signal Name	Description
Channel Signal	XC0, XC1, XC2	External Clock Inputs
	TIOA	Capture mode: Timer Counter Input Waveform mode: Timer Counter Output
	TIOB	Capture mode: Timer Counter Input Waveform mode: Timer Counter Input/Output
	INT	Interrupt Signal Output
	SYNC	Synchronization Input Signal

33.6.1.2 16-bit counter

Each channel is organized around a 16-bit counter. The value of the counter is incremented at each positive edge of the selected clock. When the counter has reached the value 0xFFFF and passes to 0x0000, an overflow occurs and the Counter Overflow Status bit in the Channel n Status Register (SRn.COVFS) is set.

The current value of the counter is accessible in real time by reading the Channel n Counter Value Register (CVn). The counter can be reset by a trigger. In this case, the counter value passes to 0x0000 on the next valid edge of the selected clock.

33.6.1.3 *Clock selection*

At block level, input clock signals of each channel can either be connected to the external inputs TCLK0, TCLK1 or TCLK2, or be connected to the configurable I/O signals A0, A1 or A2 for chaining by writing to the BMR register. See Figure 33-2 on page 743.

Each channel can independently select an internal or external clock source for its counter:

- Internal clock signals: TIMER_CLOCK1, TIMER_CLOCK2, TIMER_CLOCK3, TIMER_CLOCK4, TIMER_CLOCK5. See the Module Configuration Chapter for details about the connection of these clock sources.
- External clock signals: XC0, XC1 or XC2. See the Module Configuration Chapter for details about the connection of these clock sources.

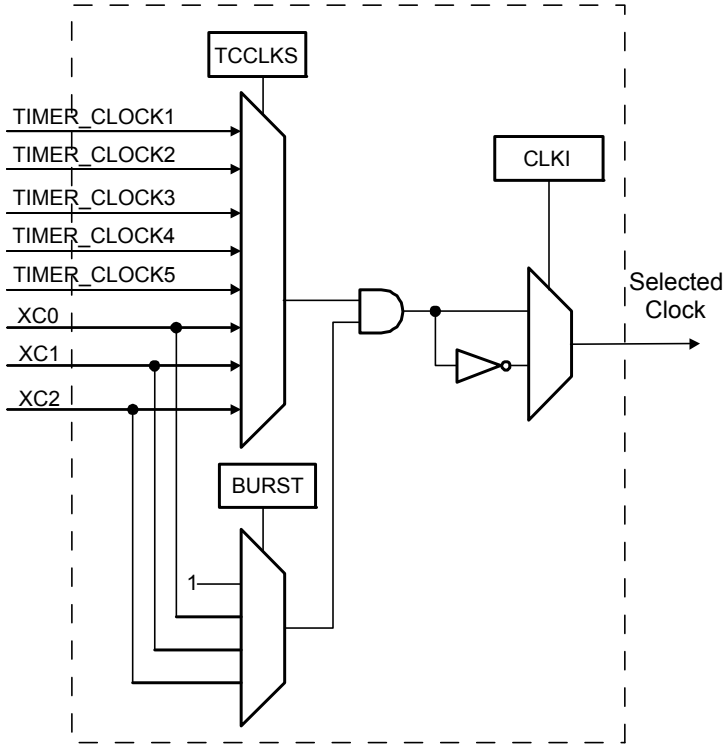
This selection is made by the Clock Selection field in the Channel n Mode Register (CMRn.TCCLKS).

The selected clock can be inverted with the Clock Invert bit in CMRn (CMRn.CLKI). This allows counting on the opposite edges of the clock.

The burst function allows the clock to be validated when an external signal is high. The Burst Signal Selection field in the CMRn register (CMRn.BURST) defines this signal.

Note: In all cases, if an external clock is used, the duration of each of its levels must be longer than the CLK_TC period. The external clock frequency must be at least 2.5 times lower than the CLK_TC.

Figure 33-2. Clock Selection

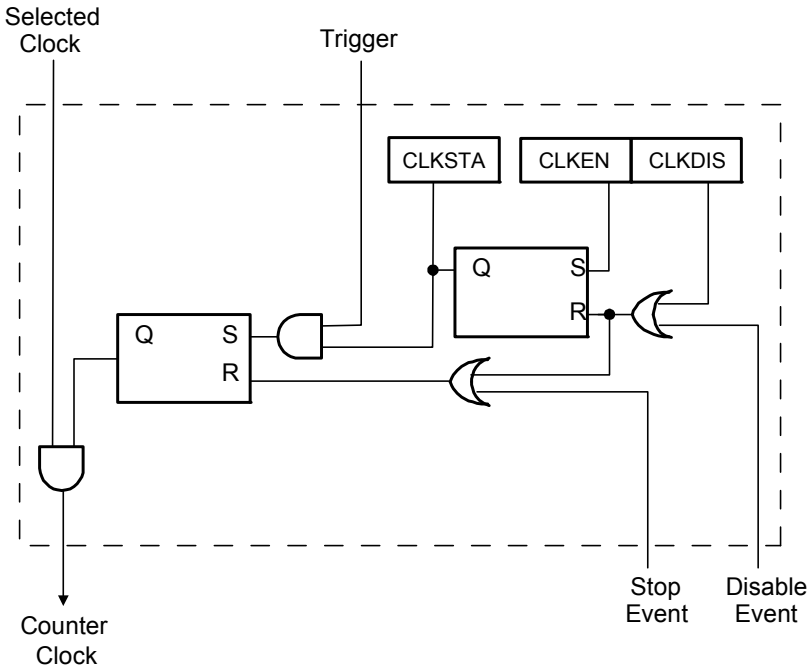


33.6.1.4 Clock control

The clock of each counter can be controlled in two different ways: it can be enabled/disabled and started/stopped. See Figure 33-3 on page 744.

- The clock can be enabled or disabled by the user by writing to the Counter Clock Enable/Disable Command bits in the Channel n Clock Control Register (CCRn.CLKEN and CCRn.CLKDIS). In Capture mode it can be disabled by an RB load event if the Counter Clock Disable with RB Loading bit in CMRn is written to one (CMRn.LDBDIS). In Waveform mode, it can be disabled by an RC Compare event if the Counter Clock Disable with RC Compare bit in CMRn is written to one (CMRn.CPCDIS). When disabled, the start or the stop actions have no effect: only a CLKEN command in CCRn can re-enable the clock. When the clock is enabled, the Clock Enabling Status bit is set in SRn (SRn.CLKSTA).
- The clock can also be started or stopped: a trigger (software, synchro, external or compare) always starts the clock. In Capture mode the clock can be stopped by an RB load event if the Counter Clock Stopped with RB Loading bit in CMRn is written to one (CMRn.LDBSTOP). In Waveform mode it can be stopped by an RC compare event if the Counter Clock Stopped with RC Compare bit in CMRn is written to one (CMRn.CPCSTOP). The start and the stop commands have effect only if the clock is enabled.

Figure 33-3. Clock Control



33.6.1.5 TC operating modes

Each channel can independently operate in two different modes:

- Capture mode provides measurement on signals.
- Waveform mode provides wave generation.

The TC operating mode selection is done by writing to the Wave bit in the CCRn register (CCRn.WAVE).

In Capture mode, TIOA and TIOB are configured as inputs.

In Waveform mode, TIOA is always configured to be an output and TIOB is an output if it is not selected to be the external trigger.

33.6.1.6 Trigger

A trigger resets the counter and starts the counter clock. Three types of triggers are common to both modes, and a fourth external trigger is available to each mode.

The following triggers are common to both modes:

- Software Trigger: each channel has a software trigger, available by writing a one to the Software Trigger Command bit in CCRn (CCRn.SWTRG).
- SYNC: each channel has a synchronization signal SYNC. When asserted, this signal has the same effect as a software trigger. The SYNC signals of all channels are asserted simultaneously by writing a one to the Synchro Command bit in the BCR register (BCR.SYNC).
- Compare RC Trigger: RC is implemented in each channel and can provide a trigger when the counter value matches the RC value if the RC Compare Trigger Enable bit in CMRn (CMRn.CPCTRG) is written to one.

The channel can also be configured to have an external trigger. In Capture mode, the external trigger signal can be selected between TIOA and TIOB. In Waveform mode, an external event can be programmed to be one of the following signals: TIOB, XC0, XC1, or XC2. This external event can then be programmed to perform a trigger by writing a one to the External Event Trigger Enable bit in CMRn (CMRn.ENETRG).

If an external trigger is used, the duration of the pulses must be longer than the CLK_TC period in order to be detected.

Regardless of the trigger used, it will be taken into account at the following active edge of the selected clock. This means that the counter value can be read differently from zero just after a trigger, especially when a low frequency signal is selected as the clock.

33.6.1.7 Peripheral events on TIOA inputs

The TIOA input lines are ored internally with peripheral events from the Peripheral Event System. To capture using events the user must ensure that the corresponding pin functions for the TIOA line are disabled. When capturing on the external TIOA pin the user must ensure that no peripheral events are generated on this pin.

33.6.2 Capture Operating Mode

This mode is entered by writing a zero to the CMRn.WAVE bit.

Capture mode allows the TC channel to perform measurements such as pulse timing, frequency, period, duty cycle and phase on TIOA and TIOB signals which are considered as inputs.

Figure 33-4 on page 747 shows the configuration of the TC channel when programmed in Capture mode.

33.6.2.1 Capture registers A and B

Registers A and B (RA and RB) are used as capture registers. This means that they can be loaded with the counter value when a programmable event occurs on the signal TIOA.

The RA Loading Selection field in CMRn (CMRn.LDRA) defines the TIOA edge for the loading of the RA register, and the RB Loading Selection field in CMRn (CMRn.LDRB) defines the TIOA edge for the loading of the RB register.

RA is loaded only if it has not been loaded since the last trigger or if RB has been loaded since the last loading of RA.

RB is loaded only if RA has been loaded since the last trigger or the last loading of RB.

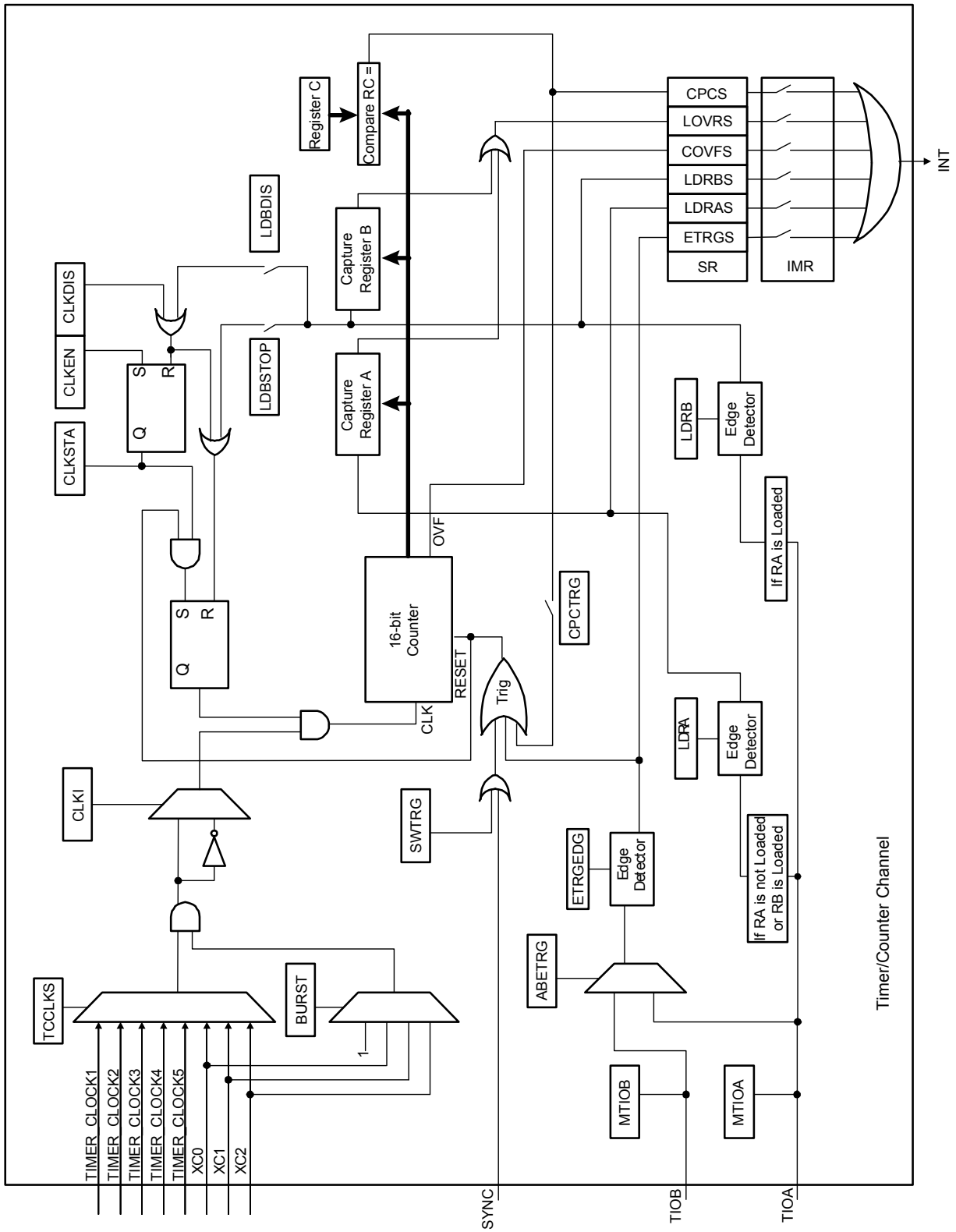
Loading RA or RB before the read of the last value loaded sets the Load Overrun Status bit in SRn (SRn.LOVRS). In this case, the old value is overwritten.

33.6.2.2 Trigger conditions

In addition to the SYNC signal, the software trigger and the RC compare trigger, an external trigger can be defined.

The TIOA or TIOB External Trigger Selection bit in CMRn (CMRn.ABETRG) selects TIOA or TIOB input signal as an external trigger. The External Trigger Edge Selection bit in CMRn (CMRn.ETREDG) defines the edge (rising, falling or both) detected to generate an external trigger. If CMRn.ETRGEDG is zero (none), the external trigger is disabled.

Figure 33-4. Capture Mode



33.6.3 Waveform Operating Mode

Waveform operating mode is entered by writing a one to the CMRn.WAVE bit.

In Waveform operating mode the TC channel generates one or two PWM signals with the same frequency and independently programmable duty cycles, or generates different types of one-shot or repetitive pulses.

In this mode, TIOA is configured as an output and TIOB is defined as an output if it is not used as an external event.

Figure 33-5 on page 749 shows the configuration of the TC channel when programmed in Waveform operating mode.

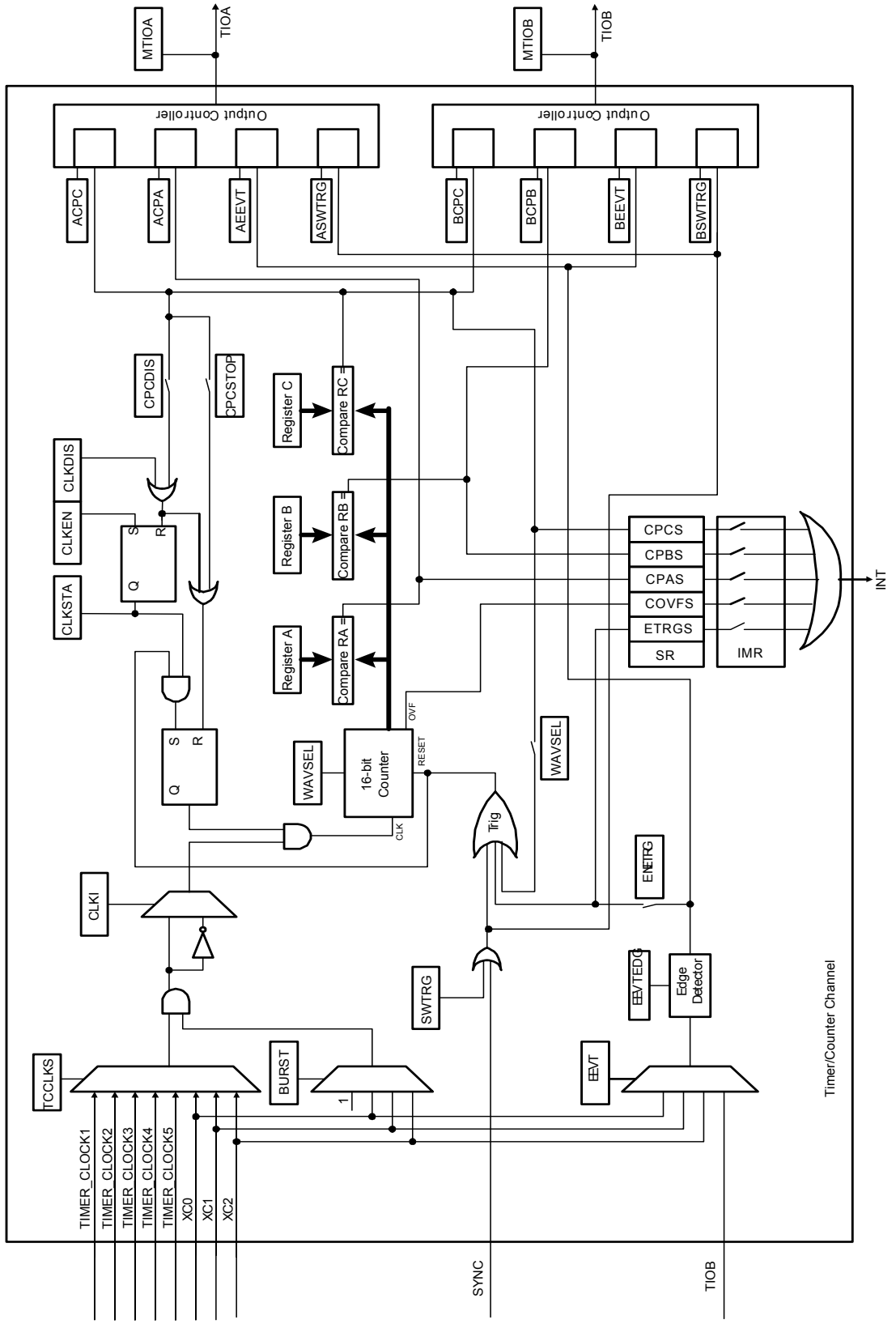
33.6.3.1 Waveform selection

Depending on the Waveform Selection field in CMRn (CMRn.WAVSEL), the behavior of CVn varies.

With any selection, RA, RB and RC can all be used as compare registers.

RA Compare is used to control the TIOA output, RB Compare is used to control the TIOB output (if correctly configured) and RC Compare is used to control TIOA and/or TIOB outputs.

Figure 33-5. Waveform Mode



33.6.3.2 WAVSEL = 0

When CMRn.WAVSEL is zero, the value of CVn is incremented from 0 to 0xFFFF. Once 0xFFFF has been reached, the value of CVn is reset. Incrementation of CVn starts again and the cycle continues. See Figure 33-6 on page 750.

An external event trigger or a software trigger can reset the value of CVn. It is important to note that the trigger may occur at any time. See Figure 33-7 on page 751.

RC Compare cannot be programmed to generate a trigger in this configuration. At the same time, RC Compare can stop the counter clock (CMRn.CPCSTOP = 1) and/or disable the counter clock (CMRn.CPCDIS = 1).

Figure 33-6. WAVSEL= 0 Without Trigger

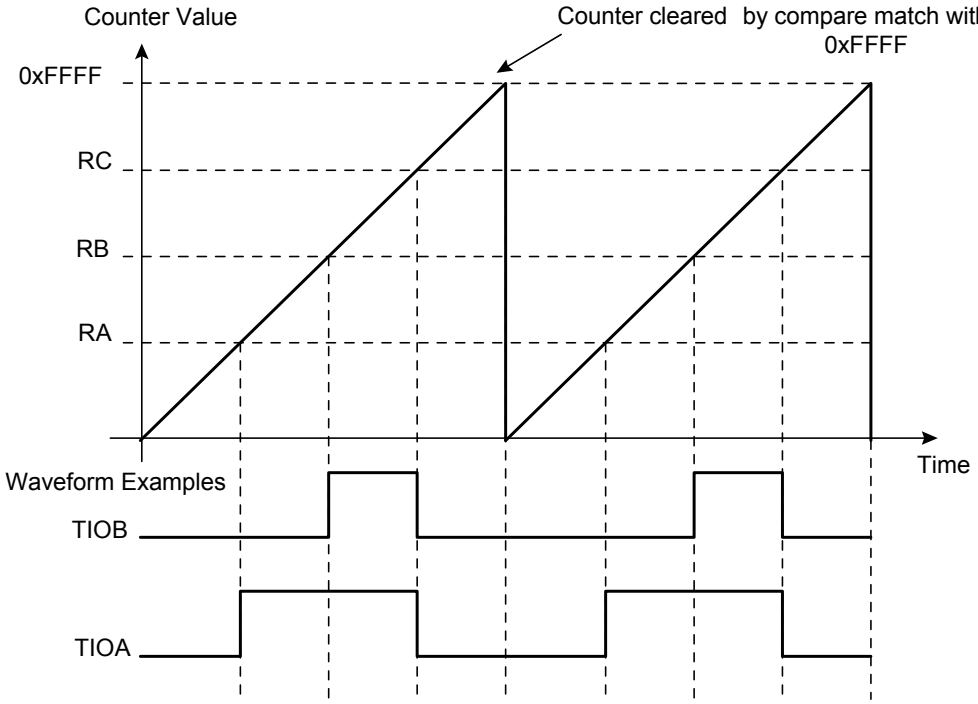
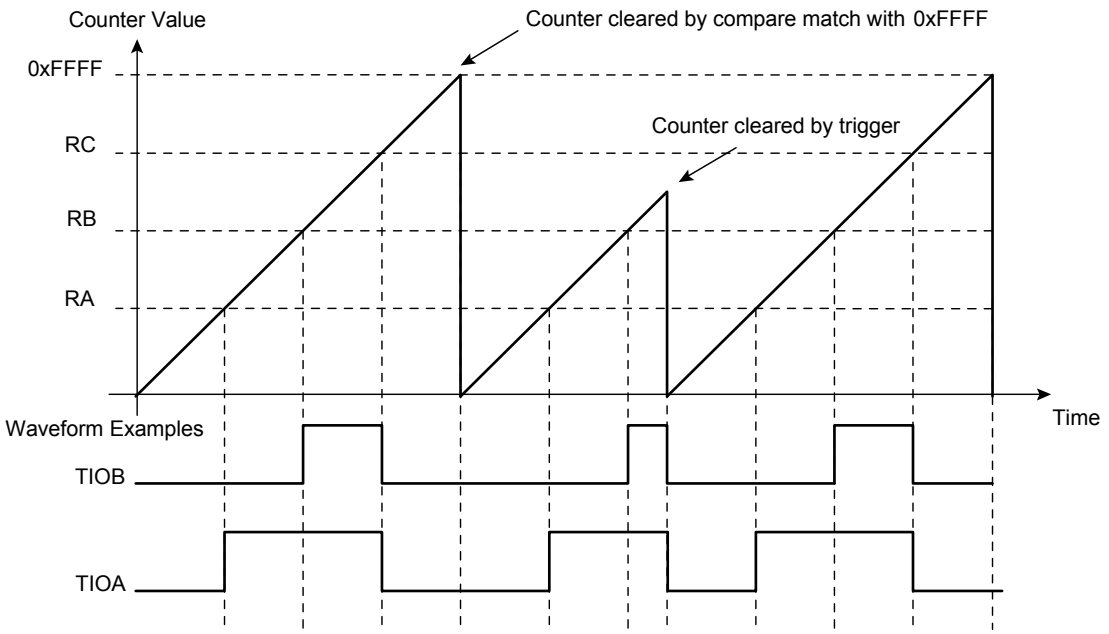


Figure 33-7. WAVSEL= 0 With Trigger



33.6.3.3 *WAVSEL = 2*

When CMRn.WAVSEL is two, the value of CVn is incremented from zero to the value of RC, then automatically reset on a RC Compare. Once the value of CVn has been reset, it is then incremented and so on. See Figure 33-8 on page 752.

It is important to note that CVn can be reset at any time by an external event or a software trigger if both are programmed correctly. See Figure 33-9 on page 752.

In addition, RC Compare can stop the counter clock (CMRn.CPCSTOP) and/or disable the counter clock (CMRn.CPCDIS = 1).

Figure 33-8. WAVSEL = 2 Without Trigger

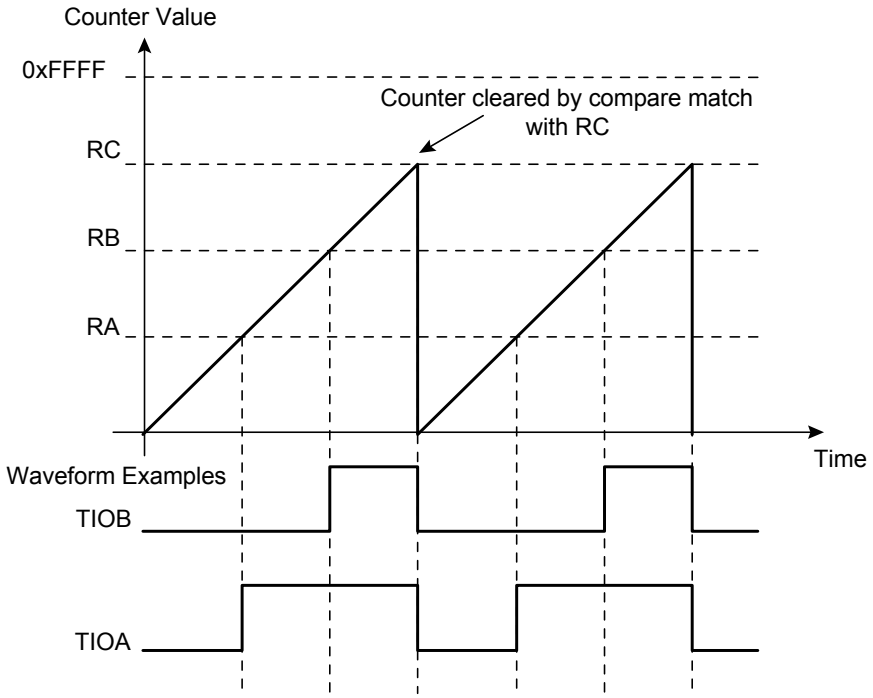
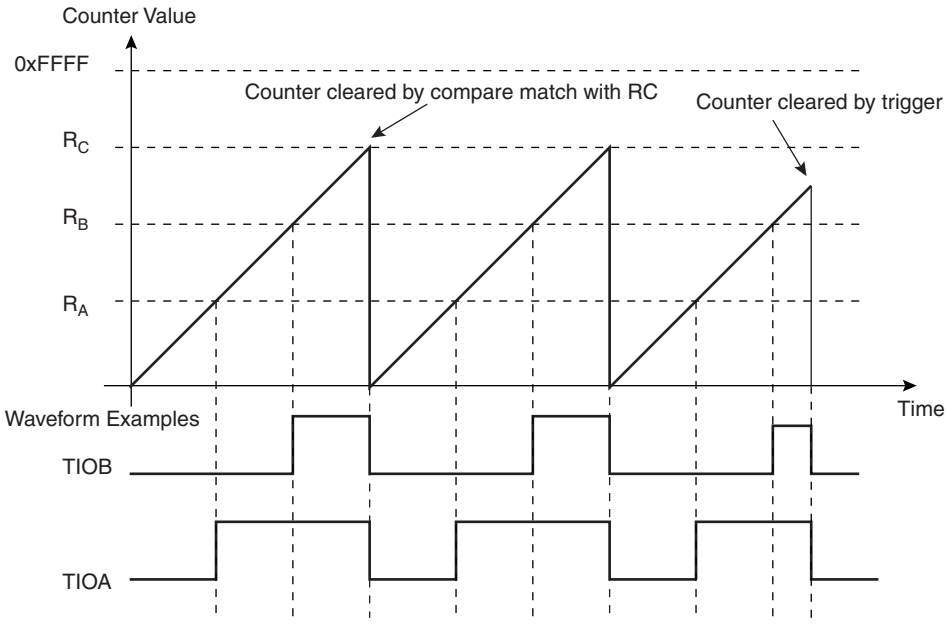


Figure 33-9. WAVSEL = 2 With Trigger



33.6.3.4 WAVSEL = 1

When CMRn.WAVSEL is one, the value of CVn is incremented from 0 to 0xFFFF. Once 0xFFFF is reached, the value of CVn is decremented to 0, then re-incremented to 0xFFFF and so on. See Figure 33-10 on page 753.

A trigger such as an external event or a software trigger can modify CVn at any time. If a trigger occurs while CVn is incrementing, CVn then decrements. If a trigger is received while CVn is decrementing, CVn then increments. See Figure 33-11 on page 753.

RC Compare cannot be programmed to generate a trigger in this configuration.

At the same time, RC Compare can stop the counter clock (CMRn.CPCSTOP = 1) and/or disable the counter clock (CMRn.CPCDIS = 1).

Figure 33-10. WAVSEL = 1 Without Trigger

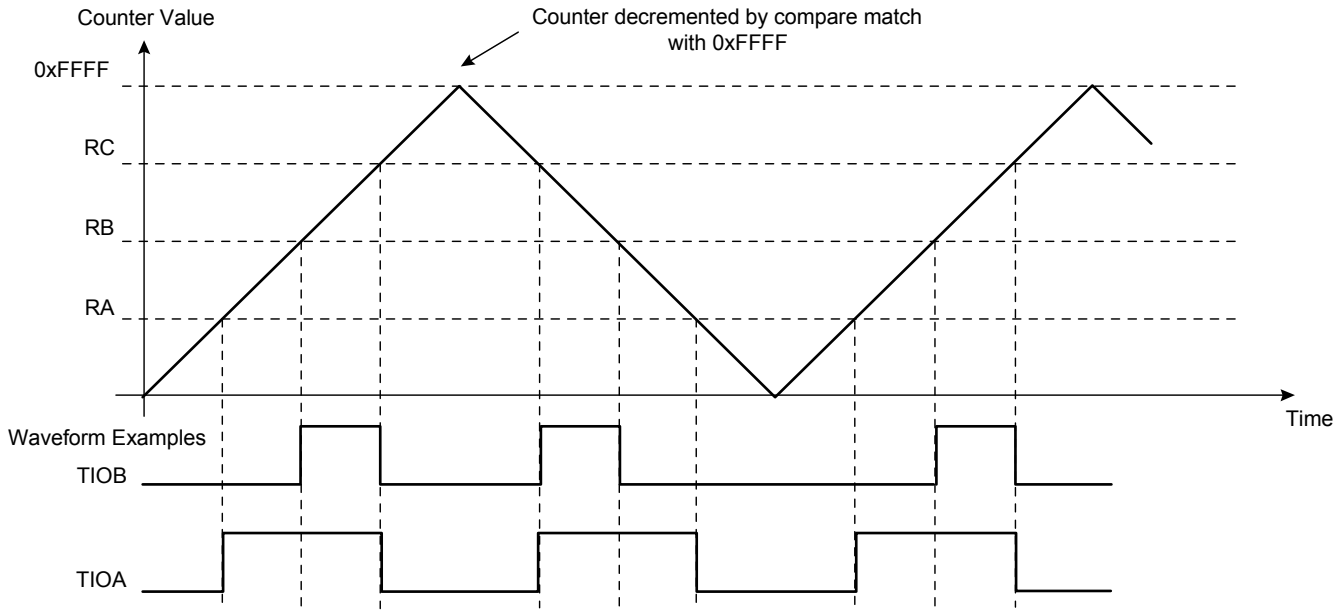
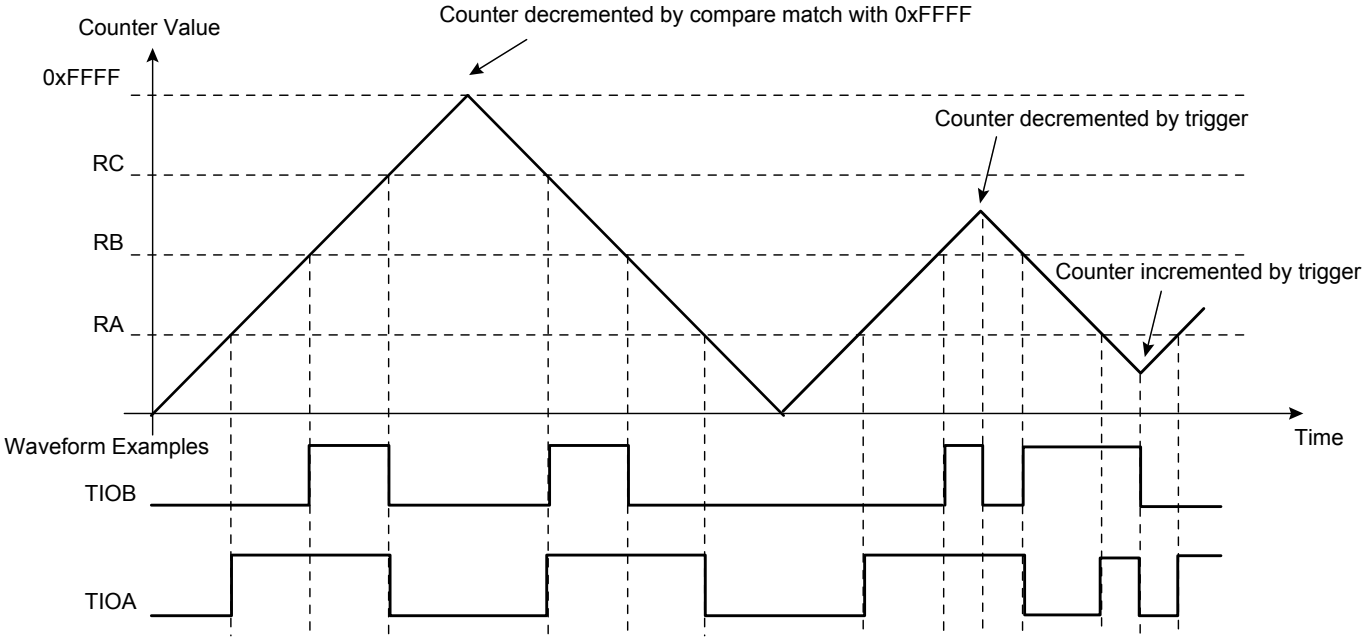


Figure 33-11. WAVSEL = 1 With Trigger



33.6.3.5 WAVSEL = 3

When CMRn.WAVSEL is three, the value of CVn is incremented from zero to RC. Once RC is reached, the value of CVn is decremented to zero, then re-incremented to RC and so on. See Figure 33-12 on page 754.

A trigger such as an external event or a software trigger can modify CVn at any time. If a trigger occurs while CVn is incrementing, CVn then decrements. If a trigger is received while CVn is decrementing, CVn then increments. See Figure 33-13 on page 755.

RC Compare can stop the counter clock (CMRn.CPCSTOP = 1) and/or disable the counter clock (CMRn.CPCDIS = 1).

Figure 33-12. WAVSEL = 3 Without Trigger

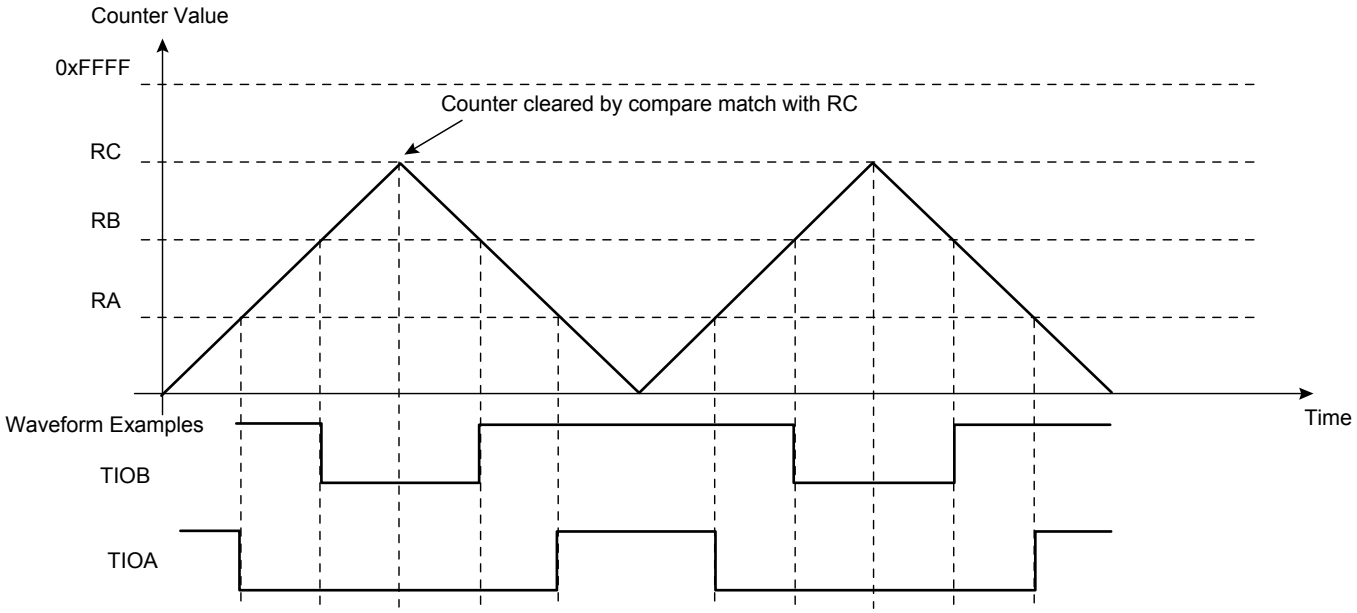
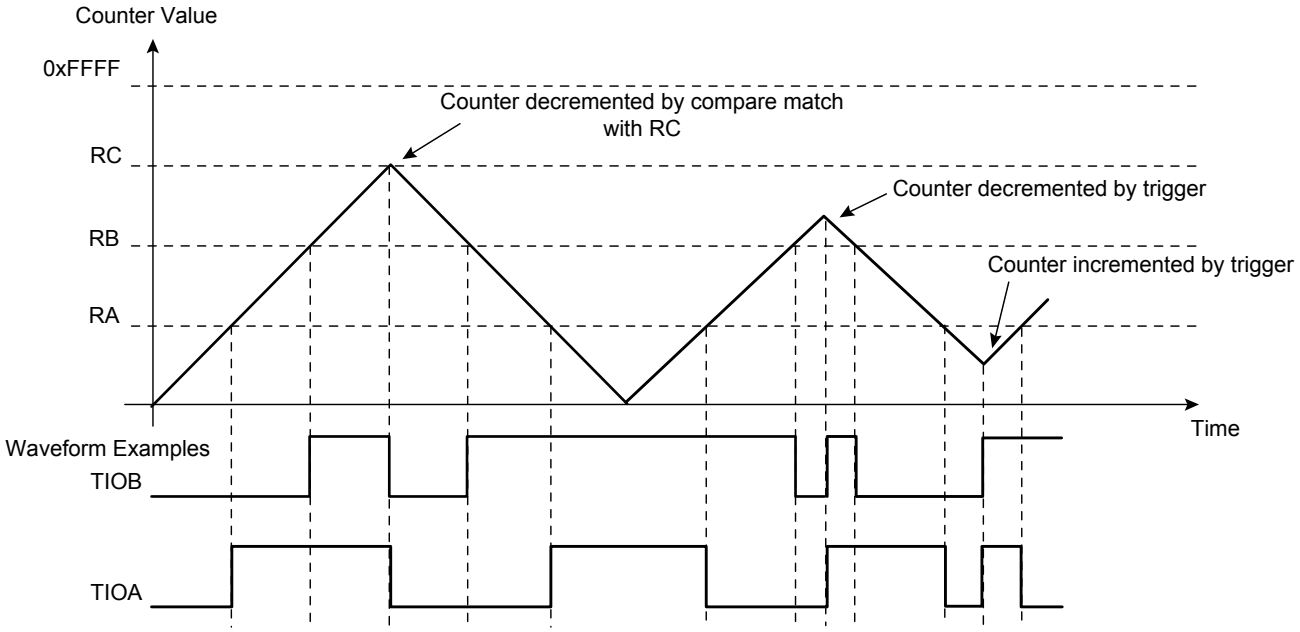


Figure 33-13. WAVSEL = 3 With Trigger



33.6.3.6 External event/trigger conditions

An external event can be programmed to be detected on one of the clock sources (XC0, XC1, XC2) or TIOB. The external event selected can then be used as a trigger.

The External Event Selection field in CMRn (CMRn.EEVT) selects the external trigger. The External Event Edge Selection field in CMRn (CMRn.EEVTEDG) defines the trigger edge for each of the possible external triggers (rising, falling or both). If CMRn.EEVTEDG is written to zero, no external event is defined.

If TIOB is defined as an external event signal (CMRn.EEVT = 0), TIOB is no longer used as an output and the compare register B is not used to generate waveforms and subsequently no IRQs. In this case the TC channel can only generate a waveform on TIOA.

When an external event is defined, it can be used as a trigger by writing a one to the CMRn.ENETRG bit.

As in Capture mode, the SYNC signal and the software trigger are also available as triggers. RC Compare can also be used as a trigger depending on the CMRn.WAVSEL field.

33.6.3.7 Output controller

The output controller defines the output level changes on TIOA and TIOB following an event. TIOB control is used only if TIOB is defined as output (not as an external event).

The following events control TIOA and TIOB:

- software trigger
- external event
- RC compare

RA compare controls TIOA and RB compare controls TIOB. Each of these events can be programmed to set, clear or toggle the output as defined in the following fields in CMRn:

- RC Compare Effect on TIOB (CMRn.BCPC)
- RB Compare Effect on TIOB (CMRn.BCPB)
- RC Compare Effect on TIOA (CMRn.ACPC)
- RA Compare Effect on TIOA (CMRn.ACPA)

33.7 User Interface

Table 33-3. TC Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00	Channel 0 Control Register	CCR0	Write-only	0x00000000
0x04	Channel 0 Mode Register	CMR0	Read/Write	0x00000000
0x10	Channel 0 Counter Value	CV0	Read-only	0x00000000
0x14	Channel 0 Register A	RA0	Read/Write(1)	0x00000000
0x18	Channel 0 Register B	RB0	Read/Write(1)	0x00000000
0x1C	Channel 0 Register C	RC0	Read/Write	0x00000000
0x20	Channel 0 Status Register	SR0	Read-only	00x00000000
0x24	Interrupt Enable Register	IER0	Write-only	0x00000000
0x28	Channel 0 Interrupt Disable Register	IDR0	Write-only	0x00000000
0x2C	Channel 0 Interrupt Mask Register	IMR0	Read-only	0x00000000
0x40	Channel 1 Control Register	CCR1	Write-only	0x00000000
0x44	Channel 1 Mode Register	CMR1	Read/Write	0x00000000
0x50	Channel 1 Counter Value	CV1	Read-only	0x00000000
0x54	Channel 1 Register A	RA1	Read/Write(1)	0x00000000
0x58	Channel 1 Register B	RB1	Read/Write(1)	0x00000000
0x5C	Channel 1 Register C	RC1	Read/Write	0x00000000
0x60	Channel 1 Status Register	SR1	Read-only	0x00000000
0x64	Channel 1 Interrupt Enable Register	IER1	Write-only	0x00000000
0x68	Channel 1 Interrupt Disable Register	IDR1	Write-only	0x00000000
0x6C	Channel 1 Interrupt Mask Register	IMR1	Read-only	0x00000000
0x80	Channel 2 Control Register	CCR2	Write-only	0x00000000
0x84	Channel 2 Mode Register	CMR2	Read/Write	0x00000000
0x90	Channel 2 Counter Value	CV2	Read-only	0x00000000
0x94	Channel 2 Register A	RA2	Read/Write(1)	0x00000000
0x98	Channel 2 Register B	RB2	Read/Write(1)	0x00000000
0x9C	Channel 2 Register C	RC2	Read/Write	0x00000000
0xA0	Channel 2 Status Register	SR2	Read-only	0x00000000
0xA4	Channel 2 Interrupt Enable Register	IER2	Write-only	0x00000000
0xA8	Channel 2 Interrupt Disable Register	IDR2	Write-only	0x00000000
0xAC	Channel 2 Interrupt Mask Register	IMR2	Read-only	0x00000000
0xC0	Block Control Register	BCR	Write-only	0x00000000
0xC4	Block Mode Register	BMR	Read/Write	0x00000000

Notes: 1. Read-only if CMRn.WAVE is zero

33.7.1 Channel Control Register

Name: CCR

Access Type: Write-only

Offset: 0x00 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	SWTRG	CLKDIS	CLKEN

- **SWTRG: Software Trigger Command**
  1: Writing a one to this bit will perform a software trigger: the counter is reset and the clock is started.
  0: Writing a zero to this bit has no effect.
- **CLKDIS: Counter Clock Disable Command**
  1: Writing a one to this bit will disable the clock.
  0: Writing a zero to this bit has no effect.
- **CLKEN: Counter Clock Enable Command**
  1: Writing a one to this bit will enable the clock if CLKDIS is not one.
  0: Writing a zero to this bit has no effect.

33.7.2 Channel Mode Register: Capture Mode

Name: CMR

Access Type: Read/Write

Offset: 0x04 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	LDRB		LDRA	

15	14	13	12	11	10	9	8
WAVE	CPCTRG	-	-	-	ABETRG	ETRGEDG	

7	6	5	4	3	2	1	0
LDBDIS	LDBSTOP	BURST		CLKI	TCCLKS		

- **LDRB: RB Loading Selection**

LDRB	Edge
0	none
1	rising edge of TIOA
2	falling edge of TIOA
3	each edge of TIOA

- **LDRA: RA Loading Selection**

LDRA	Edge
0	none
1	rising edge of TIOA
2	falling edge of TIOA
3	each edge of TIOA

- **WAVE**
  1: Capture mode is disabled (Waveform mode is enabled).
  0: Capture mode is enabled.
- **CPCTRG: RC Compare Trigger Enable**
  1: RC Compare resets the counter and starts the counter clock.
  0: RC Compare has no effect on the counter and its clock.
- **ABETRG: TIOA or TIOB External Trigger Selection**
  1: TIOA is used as an external trigger.

0: TIOB is used as an external trigger.

- **ETRGEDG: External Trigger Edge Selection**

ETRGEDG	Edge
0	none
1	rising edge
2	falling edge
3	each edge

- **LDBDIS: Counter Clock Disable with RB Loading**
  1: Counter clock is disabled when RB loading occurs.
  0: Counter clock is not disabled when RB loading occurs.
- **LDBSTOP: Counter Clock Stopped with RB Loading**
  1: Counter clock is stopped when RB loading occurs.
  0: Counter clock is not stopped when RB loading occurs.
- **BURST: Burst Signal Selection**

BURST	Burst Signal Selection
0	The clock is not gated by an external signal
1	XC0 is ANDed with the selected clock
2	XC1 is ANDed with the selected clock
3	XC2 is ANDed with the selected clock

- **CLKI: Clock Invert**
  1: The counter is incremented on falling edge of the clock.
  0: The counter is incremented on rising edge of the clock.
- **TCCLKS: Clock Selection**

TCCLKS	Clock Selected
0	TIMER_CLOCK1
1	TIMER_CLOCK2
2	TIMER_CLOCK3
3	TIMER_CLOCK4
4	TIMER_CLOCK5
5	XC0
6	XC1
7	XC2

33.7.3 Channel Mode Register: Waveform Mode

Name: CMR

Access Type: Read/Write

Offset: 0x04 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
BSWTRG		BEEVT		BCPC		BCPB	

23	22	21	20	19	18	17	16
ASWTRG		AEEVT		ACPC		ACPA	

15	14	13	12	11	10	9	8
WAVE	WAVSEL		ENETRG	EEVT		EEVTEDG	

7	6	5	4	3	2	1	0
CPCDIS	CPCSTOP	BURST		CLKI	TCCLKS		

- **BSWTRG: Software Trigger Effect on TIOB**

BSWTRG	Effect
0	none
1	set
2	clear
3	toggle

- **BEEVT: External Event Effect on TIOB**

BEEVT	Effect
0	none
1	set
2	clear
3	toggle

- **BCPC: RC Compare Effect on TIOB**

BCPC	Effect
0	none
1	set
2	clear
3	toggle

- **BCPB: RB Compare Effect on TIOB**

BCPB	Effect
0	none
1	set
2	clear
3	toggle

- **ASWTRG: Software Trigger Effect on TIOA**

ASWTRG	Effect
0	none
1	set
2	clear
3	toggle

- **AEEVT: External Event Effect on TIOA**

AEEVT	Effect
0	none
1	set
2	clear
3	toggle

- **ACPC: RC Compare Effect on TIOA**

ACPC	Effect
0	none
1	set
2	clear
3	toggle

- **ACPA: RA Compare Effect on TIOA**

ACPA	Effect
0	none
1	set
2	clear
3	toggle

- **WAVE**
  1: Waveform mode is enabled.
  0: Waveform mode is disabled (Capture mode is enabled).
- **WAVSEL: Waveform Selection**

WAVSEL	Effect
0	UP mode without automatic trigger on RC Compare
1	UPDOWN mode without automatic trigger on RC Compare
2	UP mode with automatic trigger on RC Compare
3	UPDOWN mode with automatic trigger on RC Compare

- **ENETRG: External Event Trigger Enable**
  1: The external event resets the counter and starts the counter clock.
  0: The external event has no effect on the counter and its clock. In this case, the selected external event only controls the TIOA output.
- **EEVT: External Event Selection**

EEVT	Signal selected as external event	TIOB Direction
0	TIOB	input(1)
1	XC0	output
2	XC1	output
3	XC2	output

Note: 1. *If TIOB is chosen as the external event signal, it is configured as an input and no longer generates waveforms and subsequently no IRQs.*

- **EEVTEDG: External Event Edge Selection**

EEVTEDG	Edge
0	none
1	rising edge
2	falling edge
3	each edge

- **CPCDIS: Counter Clock Disable with RC Compare**
  1: Counter clock is disabled when counter reaches RC.
  0: Counter clock is not disabled when counter reaches RC.
- **CPCSTOP: Counter Clock Stopped with RC Compare**
  1: Counter clock is stopped when counter reaches RC.

0: Counter clock is not stopped when counter reaches RC.

- **BURST: Burst Signal Selection**

BURST	Burst Signal Selection
0	The clock is not gated by an external signal.
1	XC0 is ANDed with the selected clock.
2	XC1 is ANDed with the selected clock.
3	XC2 is ANDed with the selected clock.

- **CLKI: Clock Invert**

1: Counter is incremented on falling edge of the clock.

0: Counter is incremented on rising edge of the clock.

- **TCCLKS: Clock Selection**

TCCLKS	Clock Selected
0	TIMER_CLOCK1
1	TIMER_CLOCK2
2	TIMER_CLOCK3
3	TIMER_CLOCK4
4	TIMER_CLOCK5
5	XC0
6	XC1
7	XC2

33.7.4 Channel Counter Value Register

Name: CV

Access Type: Read-only

Offset: 0x10 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
CV[15:8]							

7	6	5	4	3	2	1	0
CV[7:0]							

- **CV: Counter Value**
  CV contains the counter value in real time.

33.7.5 Channel Register A

Name: RA

Access Type: Read-only if CMRn.WAVE = 0, Read/Write if CMRn.WAVE = 1

Offset: 0x14 + n * 0X40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
RA[15:8]							

7	6	5	4	3	2	1	0
RA[7:0]							

- **RA: Register A**
  RA contains the Register A value in real time.

33.7.6 Channel Register B

Name: RB

Access Type: Read-only if CMRn.WAVE = 0, Read/Write if CMRn.WAVE = 1

Offset: 0x18 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
RB[15:8]							

7	6	5	4	3	2	1	0
RB[7:0]							

- **RB: Register B**
  RB contains the Register B value in real time.

33.7.7 Channel Register C

Name: RC

Access Type: Read/Write

Offset: 0x1C + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
RC[15:8]							

7	6	5	4	3	2	1	0
RC[7:0]							

- **RC: Register C**
  RC contains the Register C value in real time.

33.7.8 Channel Status Register

Name: SR

Access Type: Read-only

Offset: 0x20 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	MTIOB	MTIOA	CLKSTA
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

Note: Reading the Status Register will also clear the interrupt bit for the corresponding interrupts.

- **MTIOB: TIOB Mirror**
  1: TIOB is high. If CMRn.WAVE is zero, this means that TIOB pin is high. If CMRn.WAVE is one, this means that TIOB is driven high.
  0: TIOB is low. If CMRn.WAVE is zero, this means that TIOB pin is low. If CMRn.WAVE is one, this means that TIOB is driven low.
- **MTIOA: TIOA Mirror**
  1: TIOA is high. If CMRn.WAVE is zero, this means that TIOA pin is high. If CMRn.WAVE is one, this means that TIOA is driven high.
  0: TIOA is low. If CMRn.WAVE is zero, this means that TIOA pin is low. If CMRn.WAVE is one, this means that TIOA is driven low.
- **CLKSTA: Clock Enabling Status**
  1: This bit is set when the clock is enabled.
  0: This bit is cleared when the clock is disabled.
- **ETRGS: External Trigger Status**
  1: This bit is set when an external trigger has occurred.
  0: This bit is cleared when the SR register is read.
- **LDRBS: RB Loading Status**
  1: This bit is set when an RB Load has occurred and CMRn.WAVE is zero.
  0: This bit is cleared when the SR register is read.
- **LDRAS: RA Loading Status**
  1: This bit is set when an RA Load has occurred and CMRn.WAVE is zero.
  0: This bit is cleared when the SR register is read.
- **CPCS: RC Compare Status**
  1: This bit is set when an RC Compare has occurred.
  0: This bit is cleared when the SR register is read.

- **CPBS: RB Compare Status**
  1: This bit is set when an RB Compare has occurred and CMRn.WAVE is one.
  0: This bit is cleared when the SR register is read.
- **CPAS: RA Compare Status**
  1: This bit is set when an RA Compare has occurred and CMRn.WAVE is one.
  0: This bit is cleared when the SR register is read.
- **LOVRS: Load Overrun Status**
  1: This bit is set when RA or RB have been loaded at least twice without any read of the corresponding register and CMRn.WAVE is zero.
  0: This bit is cleared when the SR register is read.
- **COVFS: Counter Overflow Status**
  1: This bit is set when a counter overflow has occurred.
  0: This bit is cleared when the SR register is read.

33.7.9 Channel Interrupt Enable Register

Name: IER

Access Type: Write-only

Offset: 0x24 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will set the corresponding bit in IMR.

33.7.10 Channel Interrupt Disable Register

Name: IDR

Access Type: Write-only

Offset: 0x28 + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in IMR.

33.7.11 Channel Interrupt Mask Register

Name: IMR

Access Type: Read-only

Offset: 0x2C + n * 0x40

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

A bit in this register is cleared when the corresponding bit in IDR is written to one.

A bit in this register is set when the corresponding bit in IER is written to one.

33.7.12 Block Control Register

Name: BCR

Access Type: Write-only

Offset: 0xC0

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SYNC

- **SYNC: Synchro Command**
  1: Writing a one to this bit asserts the SYNC signal which generates a software trigger simultaneously for each of the channels.
  0: Writing a zero to this bit has no effect.

33.7.13 Block Mode Register

Name: BMR

Access Type: Read/Write

Offset: 0xC4

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	TC2XC2S		TC1XC1S		TC0XC0S	

- **TC2XC2S: External Clock Signal 2 Selection**

TC2XC2S	Signal Connected to XC2
0	TCLK2
1	none
2	TIOA0
3	TIOA1

- **TC1XC1S: External Clock Signal 1 Selection**

TC1XC1S	Signal Connected to XC1
0	TCLK1
1	none
2	TIOA0
3	TIOA2

- **TC0XC0S: External Clock Signal 0 Selection**

TC0XC0S	Signal Connected to XC0
0	TCLK0

1	none
2	TIOA1
3	TIOA2

34. Pulse Width Modulation Controller (PWM)

Rev: 1.2.0.2

34.1 Features

- 4 Channels
- One 20-bit Counter Per Channel
- Common Clock Generator Providing Thirteen Different Clocks
  - A Modulo n Counter Providing Eleven Clocks
  - Two Independent Linear Dividers Working on Modulo n Counter Outputs
- Independent Channels
  - Independent Enable Disable Command for Each Channel
  - Independent Clock Selection for Each Channel
  - Independent Period and Duty Cycle for Each Channel
  - Double Buffering of Period or Duty Cycle for Each Channel
  - Programmable Selection of The Output Waveform Polarity for Each Channel
  - Programmable Center or Left Aligned Output Waveform for Each Channel

34.2 Description

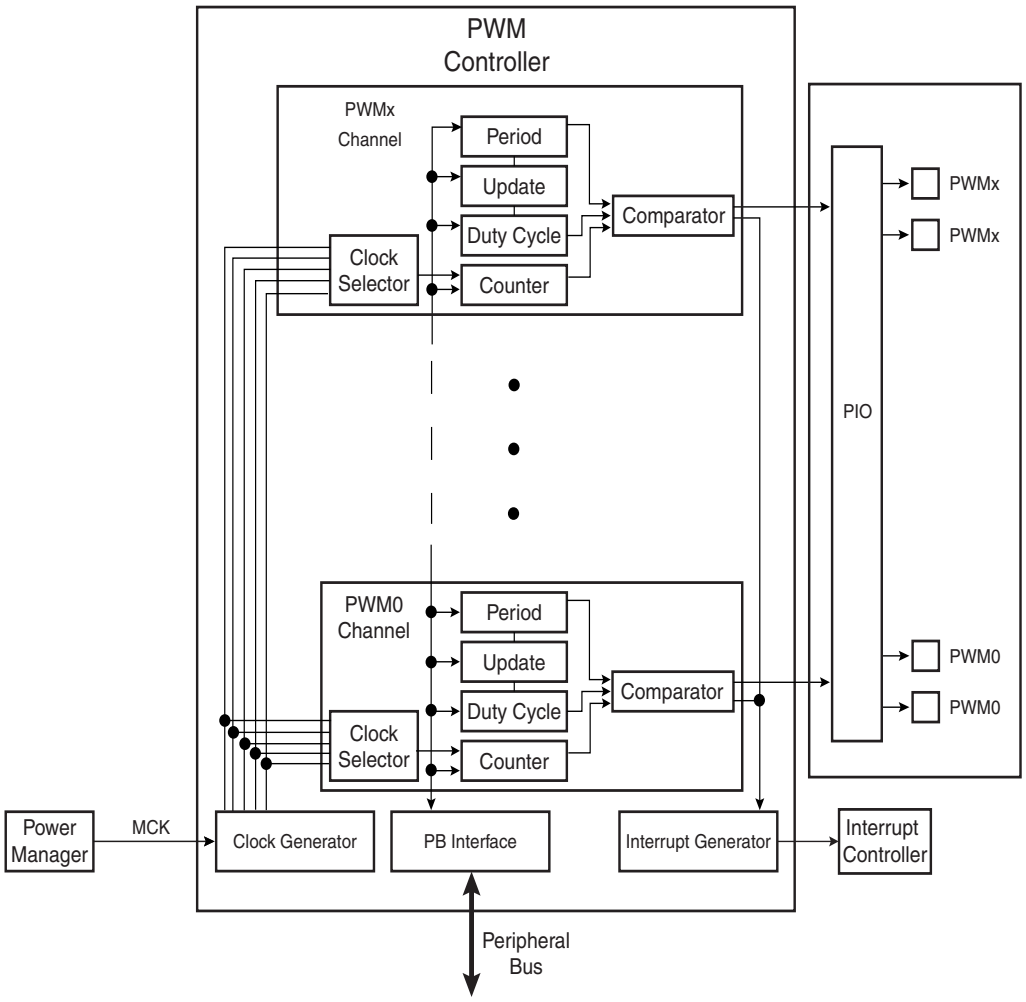
The PWM macrocell controls several channels independently. Each channel controls one square output waveform. Characteristics of the output waveform such as period, duty-cycle and polarity are configurable through the user interface. Each channel selects and uses one of the clocks provided by the clock generator. The clock generator provides several clocks resulting from the division of the PWM macrocell master clock.

All PWM macrocell accesses are made through registers mapped on the peripheral bus.

Channels can be synchronized, to generate non overlapped waveforms. All channels integrate a double buffering system in order to prevent an unexpected output waveform while modifying the period or the duty-cycle.

34.3 Block Diagram

Figure 34-1. Pulse Width Modulation Controller Block Diagram



34.4 I/O Lines Description

Each channel outputs one waveform on one external I/O line.

Table 34-1. I/O Line Description

Name	Description	Type
PWMx	PWM Waveform Output for channel x	Output

34.5 Product Dependencies

34.5.1 I/O Lines

The pins used for interfacing the PWM may be multiplexed with PIO lines. The programmer must first program the PIO controller to assign the desired PWM pins to their peripheral function. If I/O lines of the PWM are not used by the application, they can be used for other purposes by the PIO controller.

Not all PWM outputs may be enabled. If an application requires only four channels, then only four PIO lines will be assigned to PWM outputs.

34.5.2 Debug operation

The PWM clock is running during debug operation.

34.5.3 Power Management

The PWM clock is generated by the Power Manager. Before using the PWM, the programmer must ensure that the PWM clock is enabled in the Power Manager. However, if the application does not require PWM operations, the PWM clock can be stopped when not needed and be restarted later. In this case, the PWM will resume its operations where it left off.

In the PWM description, Master Clock (MCK) is the clock of the peripheral bus to which the PWM is connected.

34.5.4 Interrupt Sources

The PWM interrupt line is connected to the interrupt controller. Using the PWM interrupt requires the interrupt controller to be programmed first.

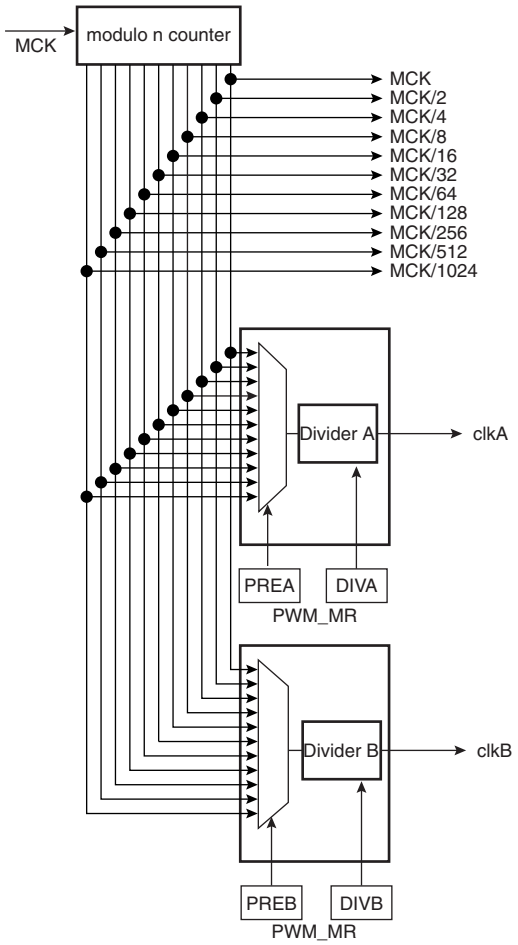
34.6 Functional Description

The PWM macrocell is primarily composed of a clock generator module and 4 channels.

- Clocked by the system clock, MCK, the clock generator module provides 13 clocks.
- Each channel can independently choose one of the clock generator outputs.
- Each channel generates an output waveform with attributes that can be defined independently for each channel through the user interface registers.

34.6.1 PWM Clock Generator

Figure 34-2. Functional View of the Clock Generator Block Diagram



Caution: Before using the PWM macrocell, the programmer must ensure that the PWM clock in the Power Manager is enabled.

The PWM macrocell master clock, MCK, is divided in the clock generator module to provide different clocks available for all channels. Each channel can independently select one of the divided clocks.

The clock generator is divided in three blocks:

– a modulo n counter which provides 11 clocks: F_{MCK}, $F_{MCK}/2$, $F_{MCK}/4$, $F_{MCK}/8$, $F_{MCK}/16$, $F_{MCK}/32$, $F_{MCK}/64$, $F_{MCK}/128$, $F_{MCK}/256$, $F_{MCK}/512$, $F_{MCK}/1024$

– two linear dividers (1, 1/2, 1/3, ... 1/255) that provide two separate clocks: clkA and clkB

Each linear divider can independently divide one of the clocks of the modulo n counter. The selection of the clock to be divided is made according to the PREA (PREB) field of the PWM Mode register (MR). The resulting clock clkA (clkB) is the clock selected divided by DIVA (DIVB) field value in the PWM Mode register (MR).

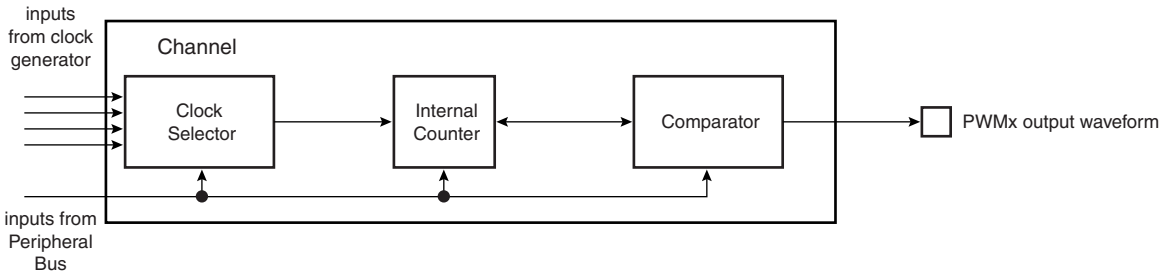
After a reset of the PWM controller, DIVA (DIVB) and PREA (PREB) in the PWM Mode register are set to 0. This implies that after reset clkA (clkB) are turned off.

At reset, all clocks provided by the modulo n counter are turned off except clock “clk”. This situation is also true when the PWM master clock is turned off through the Power Management Controller.

34.6.2 PWM Channel

34.6.2.1 Block Diagram

Figure 34-3. Functional View of the Channel Block Diagram



Each of the 4 channels is composed of three blocks:

- A clock selector which selects one of the clocks provided by the clock generator described in Section 34.6.1 ”PWM Clock Generator” on page 780.
- An internal counter clocked by the output of the clock selector. This internal counter is incremented or decremented according to the channel configuration and comparators events. The size of the internal counter is 20 bits.
- A comparator used to generate events according to the internal counter value. It also computes the PWMx output waveform according to the configuration.

34.6.2.2 Waveform Properties

The different properties of output waveforms are:

- the ***internal clock selection***. The internal channel counter is clocked by one of the clocks provided by the clock generator described in the previous section. This channel parameter is defined in the CPRE field of the CMRx register. This field is reset at 0.
- the ***waveform period***. This channel parameter is defined in the CPRD field of the CPRDx register.

- If the waveform is left aligned, then the output waveform period depends on the counter source clock and can be calculated:
By using the Master Clock (MCK) divided by an X given prescaler value
(with X being 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024), the resulting period formula will be:

$$\frac{(X \times CPRD)}{MCK}$$

By using a Master Clock divided by one of both DIVA or DIVB divider, the formula becomes, respectively:

$$\frac{(CRPD \times DIVA)}{MCK} \text{ or } \frac{(CRPD \times DIVAB)}{MCK}$$

If the waveform is center aligned then the output waveform period depends on the counter source clock and can be calculated:
By using the Master Clock (MCK) divided by an X given prescaler value
(with X being 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula will be:

$$\frac{(2 \times X \times CPRD)}{MCK}$$

By using a Master Clock divided by one of both DIVA or DIVB divider, the formula becomes, respectively:

$$\frac{(2 \times CPRD \times DIVA)}{MCK} \text{ or } \frac{(2 \times CPRD \times DIVB)}{MCK}$$

- the ***waveform duty cycle***. This channel parameter is defined in the CDTY field of the CDTYx register.
If the waveform is left aligned then:

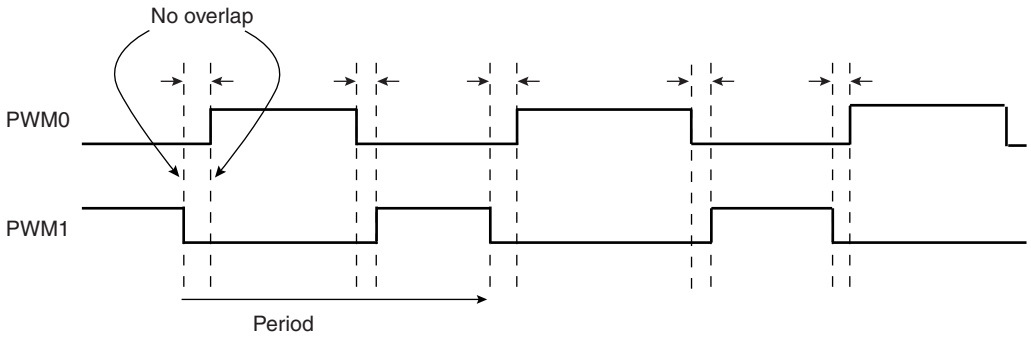
$$\text{duty cycle} = \frac{(period - 1/\text{fchannel_x_clock} \times CDTY)}{period}$$

If the waveform is center aligned, then:

$$\text{duty cycle} = \frac{((period/2) - 1/\text{fchannel_x_clock} \times CDTY))}{(period/2)}$$

- the ***waveform polarity.*** At the beginning of the period, the signal can be at high or low level. This property is defined in the CPOL field of the CMRx register. By default the signal starts by a low level.
- the ***waveform alignment***. The output waveform can be left or center aligned. Center aligned waveforms can be used to generate non overlapped waveforms. This property is defined in the CALG field of the CMRx register. The default mode is left aligned.

Figure 34-4. Non Overlapped Center Aligned Waveforms



Note: 1. See Figure 34-5 on page 784 for a detailed description of center aligned waveforms.

When center aligned, the internal channel counter increases up to CPRD and.decreases down to 0. This ends the period.

When left aligned, the internal channel counter increases up to CPRD and is reset. This ends the period.

Thus, for the same CPRD value, the period for a center aligned channel is twice the period for a left aligned channel.

Waveforms are fixed at 0 when:

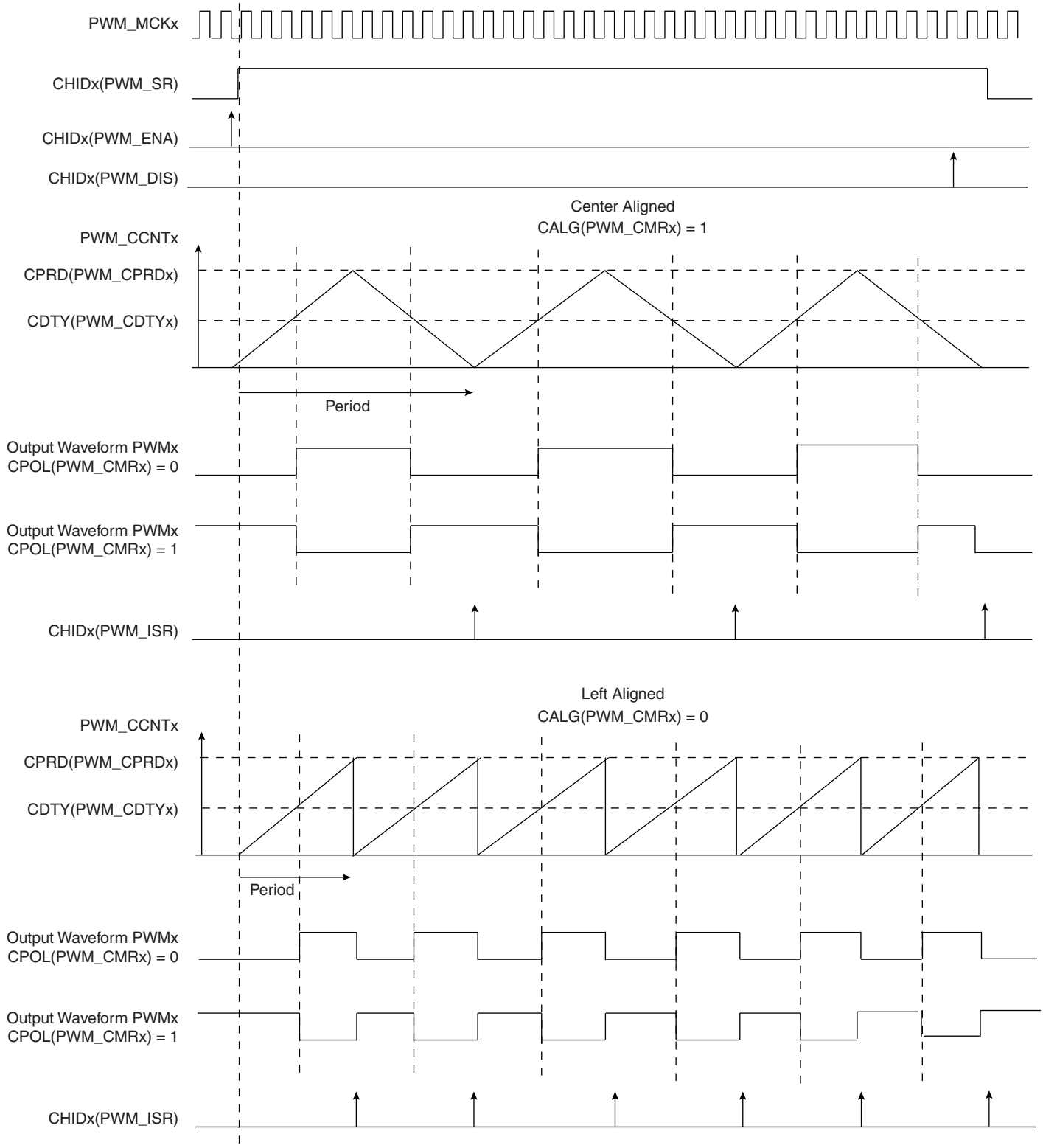
- CDTY = CPRD and CPOL = 0
- CDTY = 0 and CPOL = 1

Waveforms are fixed at 1 (once the channel is enabled) when:

- CDTY = 0 and CPOL = 0
- CDTY = CPRD and CPOL = 1

The waveform polarity must be set before enabling the channel. This immediately affects the channel output level. Changes on channel polarity are not taken into account while the channel is enabled.

Figure 34-5. Waveform Properties



34.6.3 PWM Controller Operations

34.6.3.1 Initialization

Before enabling the output channel, this channel must have been configured by the software application:

- Configuration of the clock generator if DIVA and DIVB are required
- Selection of the clock for each channel (CPRE field in the CMRx register)
- Configuration of the waveform alignment for each channel (CALG field in the CMRx register)
- Configuration of the period for each channel (CPRD in the CPRDx register). Writing in CPRDx Register is possible while the channel is disabled. After validation of the channel, the user must use CUPDx Register to update CPRDx as explained below.
- Configuration of the duty cycle for each channel (CDTY in the CDTYx register). Writing in CDTYx Register is possible while the channel is disabled. After validation of the channel, the user must use CUPDx Register to update CDTYx as explained below.
- Configuration of the output waveform polarity for each channel (CPOL in the CMRx register)
- Enable Interrupts (Writing CHIDx in the IER register)
- Enable the PWM channel (Writing CHIDx in the ENA register)

It is possible to synchronize different channels by enabling them at the same time by means of writing simultaneously several CHIDx bits in the ENA register.

In such a situation, all channels may have the same clock selector configuration and the same period specified.

34.6.3.2 Source Clock Selection Criteria

The large number of source clocks can make selection difficult. The relationship between the value in the Period Register (CPRDx) and the Duty Cycle Register (CDTYx) can help the user in choosing. The event number written in the Period Register gives the PWM accuracy. The Duty Cycle quantum cannot be lower than *1/CPRDx* value. The higher the value of CPRDx, the greater the PWM accuracy.

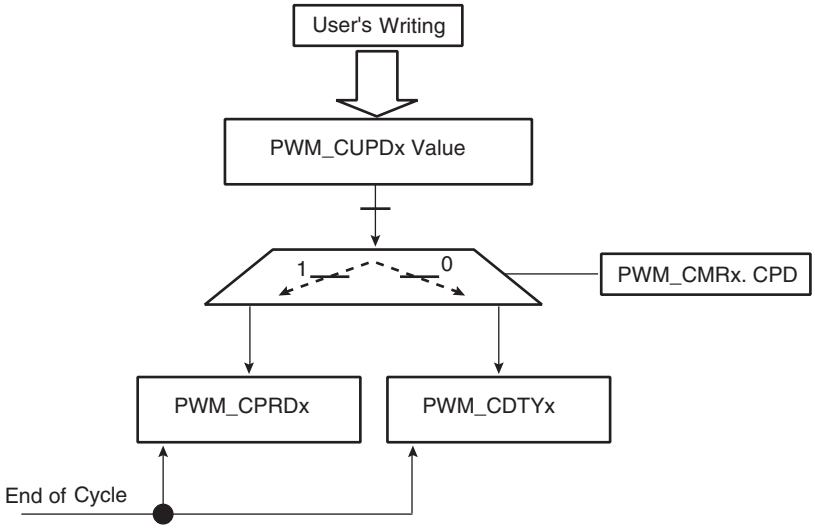
For example, if the user sets 15 (in decimal) in CPRDx, the user is able to set a value between 1 up to 14 in CDTYx Register. The resulting duty cycle quantum cannot be lower than 1/15 of the PWM period.

34.6.3.3 Changing the Duty Cycle or the Period

It is possible to modulate the output waveform duty cycle or period.

To prevent unexpected output waveform, the user must use the update register (PWM_CUPDx) to change waveform parameters while the channel is still enabled. The user can write a new period value or duty cycle value in the update register (CUPDx). This register holds the new value until the end of the current cycle and updates the value for the next cycle. Depending on the CPD field in the CMRx register, CUPDx either updates CPRDx or CDTYx. Note that even if the update register is used, the period must not be smaller than the duty cycle.

Figure 34-6. Synchronized Period or Duty Cycle Update



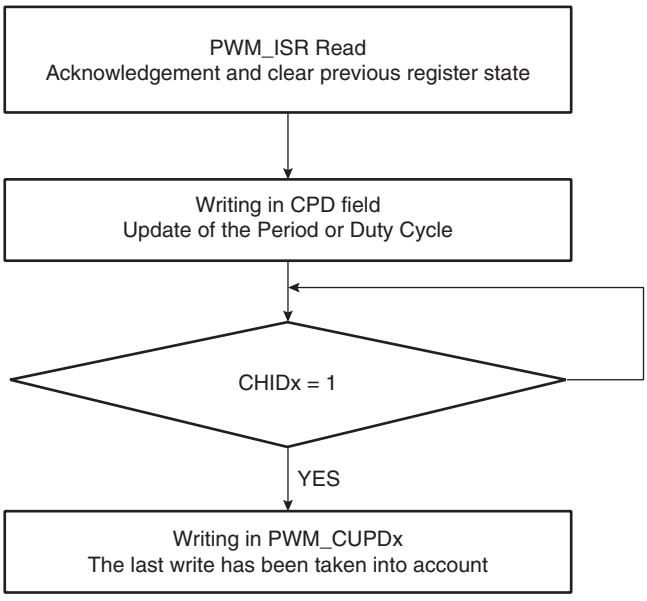
To prevent overwriting the CUPDx by software, the user can use status events in order to synchronize his software. Two methods are possible. In both, the user must enable the dedicated interrupt in IER at PWM Controller level.

The first method (polling method) consists of reading the relevant status bit in ISR Register according to the enabled channel(s). See Figure 34-7.

The second method uses an Interrupt Service Routine associated with the PWM channel.

Note: Reading the ISR register automatically clears CHIDx flags.

Figure 34-7. Polling Method



Note: Polarity and alignment can be modified only when the channel is disabled.

34.6.3.4 Interrupts

Depending on the interrupt mask in the IMR register, an interrupt is generated at the end of the corresponding channel period. The interrupt remains active until a read operation in the ISR register occurs.

A channel interrupt is enabled by setting the corresponding bit in the IER register. A channel interrupt is disabled by setting the corresponding bit in the IDR register.

34.7 Pulse Width Modulation (PWM) Controller User Interface

34.7.1 Register Mapping

Table 34-2. PWM Controller Registers

Offset	Register	Name	Access	Peripheral Reset Value
0x00	PWM Mode Register	MR	Read/Write	0
0x04	PWM Enable Register	ENA	Write-only	-
0x08	PWM Disable Register	DIS	Write-only	-
0x0C	PWM Status Register	SR	Read-only	0
0x10	PWM Interrupt Enable Register	IER	Write-only	-
0x14	PWM Interrupt Disable Register	IDR	Write-only	-
0x18	PWM Interrupt Mask Register	IMR	Read-only	0
0x1C	PWM Interrupt Status Register	ISR	Read-only	0
0x4C - 0xF8	Reserved	–	–	–
0x4C - 0xFC	Reserved	–	–	–
0x100 - 0x1FC	Reserved			
0x200	Channel 0 Mode Register	CMR0	Read/Write	0x0
0x204	Channel 0 Duty Cycle Register	CDTY0	Read/Write	0x0
0x208	Channel 0 Period Register	CPRD0	Read/Write	0x0
0x20C	Channel 0 Counter Register	CCNT0	Read-only	0x0
0x210	Channel 0 Update Register	CUPD0	Write-only	-
...	Reserved			
0x220	Channel 1 Mode Register	CMR1	Read/Write	0x0
0x224	Channel 1 Duty Cycle Register	CDTY1	Read/Write	0x0
0x228	Channel 1 Period Register	CPRD1	Read/Write	0x0
0x22C	Channel 1 Counter Register	CCNT1	Read-only	0x0
0x230	Channel 1 Update Register	CUPD1	Write-only	-
...	...	...	...	...

34.7.2 PWM Mode Register

Register Name: MR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	PREB			

23	22	21	20	19	18	17	16
DIVB							

15	14	13	12	11	10	9	8
–	–	–	–	PREA			

7	6	5	4	3	2	1	0
DIVA							

- **DIVA, DIVB: CLKA, CLKB Divide Factor**

DIVA, DIVB	CLKA, CLKB
0	CLKA, CLKB clock is turned off
1	CLKA, CLKB clock is clock selected by PREA, PREB
2-255	CLKA, CLKB clock is clock selected by PREA, PREB divided by DIVA, DIVB factor.

- **PREA, PREB**

PREA, PREB				Divider Input Clock
0	0	0	0	MCK.
0	0	0	1	MCK/2
0	0	1	0	MCK/4
0	0	1	1	MCK/8
0	1	0	0	MCK/16
0	1	0	1	MCK/32
0	1	1	0	MCK/64
0	1	1	1	MCK/128
1	0	0	0	MCK/256
1	0	0	1	MCK/512
1	0	1	0	MCK/1024
Other				Reserved

34.7.3 PWM Enable Register

Register Name: ENA

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID**

0 = No effect.

1 = Enable PWM output for channel x.

34.7.4 PWM Disable Register

Register Name: DIS

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID**

0 = No effect.

1 = Disable PWM output for channel x.

34.7.5 PWM Status Register

Register Name: SR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID**

0 = PWM output for channel x is disabled.

1 = PWM output for channel x is enabled.

34.7.6 PWM Interrupt Enable Register

Register Name: IER

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID.**

0 = No effect.

1 = Enable interrupt for PWM channel x.

34.7.7 PWM Interrupt Disable Register

Register Name: IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID.**

0 = No effect.

1 = Disable interrupt for PWM channel x.

34.7.8 PWM Interrupt Mask Register

Register Name: IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID.**

0 = Interrupt for PWM channel x is disabled.

1 = Interrupt for PWM channel x is enabled.

34.7.9 PWM Interrupt Status Register

Register Name: ISR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CHID3	CHID2	CHID1	CHID0

- **CHIDx: Channel ID**

0 = No new channel period since the last read of the ISR register.

1 = At least one new channel period since the last read of the ISR register.

Note: Reading ISR automatically clears CHIDx flags.

34.7.10 PWM Channel Mode Register

Register Name: CMRx

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	CPD	CPOL	CALG

7	6	5	4	3	2	1	0
–	–	–	–	CPRE			

- **CPRE: Channel Pre-scaler**

CPRE				Channel Pre-scaler
0	0	0	0	MCK
0	0	0	1	MCK/2
0	0	1	0	MCK/4
0	0	1	1	MCK/8
0	1	0	0	MCK/16
0	1	0	1	MCK/32
0	1	1	0	MCK/64
0	1	1	1	MCK/128
1	0	0	0	MCK/256
1	0	0	1	MCK/512
1	0	1	0	MCK/1024
1	0	1	1	CLKA
1	1	0	0	CLKB
Other				Reserved

- **CALG: Channel Alignment**

0 = The period is left aligned.

1 = The period is center aligned.

- **CPOL: Channel Polarity**

0 = The output waveform starts at a low level.

1 = The output waveform starts at a high level.

- **CPD: Channel Update Period**

0 = Writing to the CUPDx will modify the duty cycle at the next period start event.

1 = Writing to the CUPDx will modify the period at the next period start event.

34.7.11 PWM Channel Duty Cycle Register

Register Name: CDTYx

Access Type: Read/Write

31	30	29	28	27	26	25	24
CDTY							

23	22	21	20	19	18	17	16
CDTY							

15	14	13	12	11	10	9	8
CDTY							

7	6	5	4	3	2	1	0
CDTY							

Only the first 20 bits (internal channel counter size) are significant.

- **CDTY: Channel Duty Cycle**

Defines the waveform duty cycle. This value must be defined between 0 and CPRD (CPRx).

34.7.12 PWM Channel Period Register

Register Name: CPRDx

Access Type: Read/Write

31	30	29	28	27	26	25	24
CPRD							
23	22	21	20	19	18	17	16
CPRD							
15	14	13	12	11	10	9	8
CPRD							
7	6	5	4	3	2	1	0
CPRD							

Only the first 20 bits (internal channel counter size) are significant.

- **CPRD: Channel Period**

If the waveform is left-aligned, then the output waveform period depends on the counter source clock and can be calculated:

– By using the Master Clock (MCK) divided by an X given prescaler value (with X being 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula will be:

$$\frac{(X \times CPRD)}{MCK}$$

– By using a Master Clock divided by one of both DIVA or DIVB divider, the formula becomes, respectively:

$$\frac{(CRPD \times DIVA)}{MCK} \text{ or } \frac{(CRPD \times DIVAB)}{MCK}$$

If the waveform is center-aligned, then the output waveform period depends on the counter source clock and can be calculated:

– By using the Master Clock (MCK) divided by an X given prescaler value (with X being 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula will be:

$$\frac{(2 \times X \times CPRD)}{MCK}$$

– By using a Master Clock divided by one of both DIVA or DIVB divider, the formula becomes, respectively:

$$\frac{(2 \times CPRD \times DIVA)}{MCK} \text{ or } \frac{(2 \times CPRD \times DIVB)}{MCK}$$

34.7.13 PWM Channel Counter Register

Register Name: CCNTx

Access Type: Read-only

31	30	29	28	27	26	25	24
CNT							

23	22	21	20	19	18	17	16
CNT							

15	14	13	12	11	10	9	8
CNT							

7	6	5	4	3	2	1	0
CNT							

- **CNT: Channel Counter Register**

Internal counter value. This register is reset when:

- the channel is enabled (writing CHIDx in the ENA register).
- the counter reaches CPRD value defined in the CPRDx register if the waveform is left aligned.

34.7.14 PWM Channel Update Register

Register Name: CUPDx

Access Type: Write-only

31	30	29	28	27	26	25	24
CUPD							

23	22	21	20	19	18	17	16
CUPD							

15	14	13	12	11	10	9	8
CUPD							

7	6	5	4	3	2	1	0
CUPD							

This register acts as a double buffer for the period or the duty cycle. This prevents an unexpected waveform when modifying the waveform period or duty-cycle.

Only the first 20 bits (internal channel counter size) are significant.

CPD (CMRx Register)	
0	The duty-cycle (CDTY in the CDTYx register) is updated with the CUPD value at the beginning of the next period.
1	The period (CPRD in the CPRDx register) is updated with the CUPD value at the beginning of the next period.

35. LCD Controller (LCDC)

Rev: 1.7.0.3

35.1 Features

- **STN Panel Features**
  - **Single and Dual Scan Color and Monochrome LCD Panels**
  - **4-bit Single Scan, 8-bit Single or Dual Scan, 16-bit Dual Scan Interfaces**
  - **Up to 16 Gray Levels for Monochrome and Up to 4096 Colors for Color Panel**
  - **1 or 2 Bits per Pixel (Palletized), 4 Bits per Pixel (Non-palletized) for Monochrome**
  - **1, 2, 4 or 8 bits per Pixel (Palletized), 16 Bits per Pixel (Non-palletized) for Color STN Display**
- **TFT Panel Features**
  - **Single Scan Active TFT LCD Panel**
  - **Up to 24-bit Single Scan Interfaces**
  - **1, 2, 4 or 8 Bits per Pixel (Palletized), 16 or 24 Bits per Pixel (Non-palletized)**
- **Common Features**
  - **Configurable Screen Size Up to 2048 x 2048**
  - **DMA Controller for Reading the Display Data from an External Memory**
  - **2K bytes Input FIFO**
  - **2D Frame Buffer Addressing Allowing Movement in an Image Larger Than the Screen Size**

35.2 Description

The LCD Controller consists of logic for transferring LCD image data from an external display buffer to an LCD module with integrated common and segment drivers.

The LCD Controller supports single and double scan monochrome and color passive STN LCD modules and single scan active TFT LCD modules. On monochrome STN displays, up to 16 gray shades are supported using a time-based dithering algorithm and Frame Rate Control (FRC) method. This method is also used in color STN displays to generate up to 4096 colors.

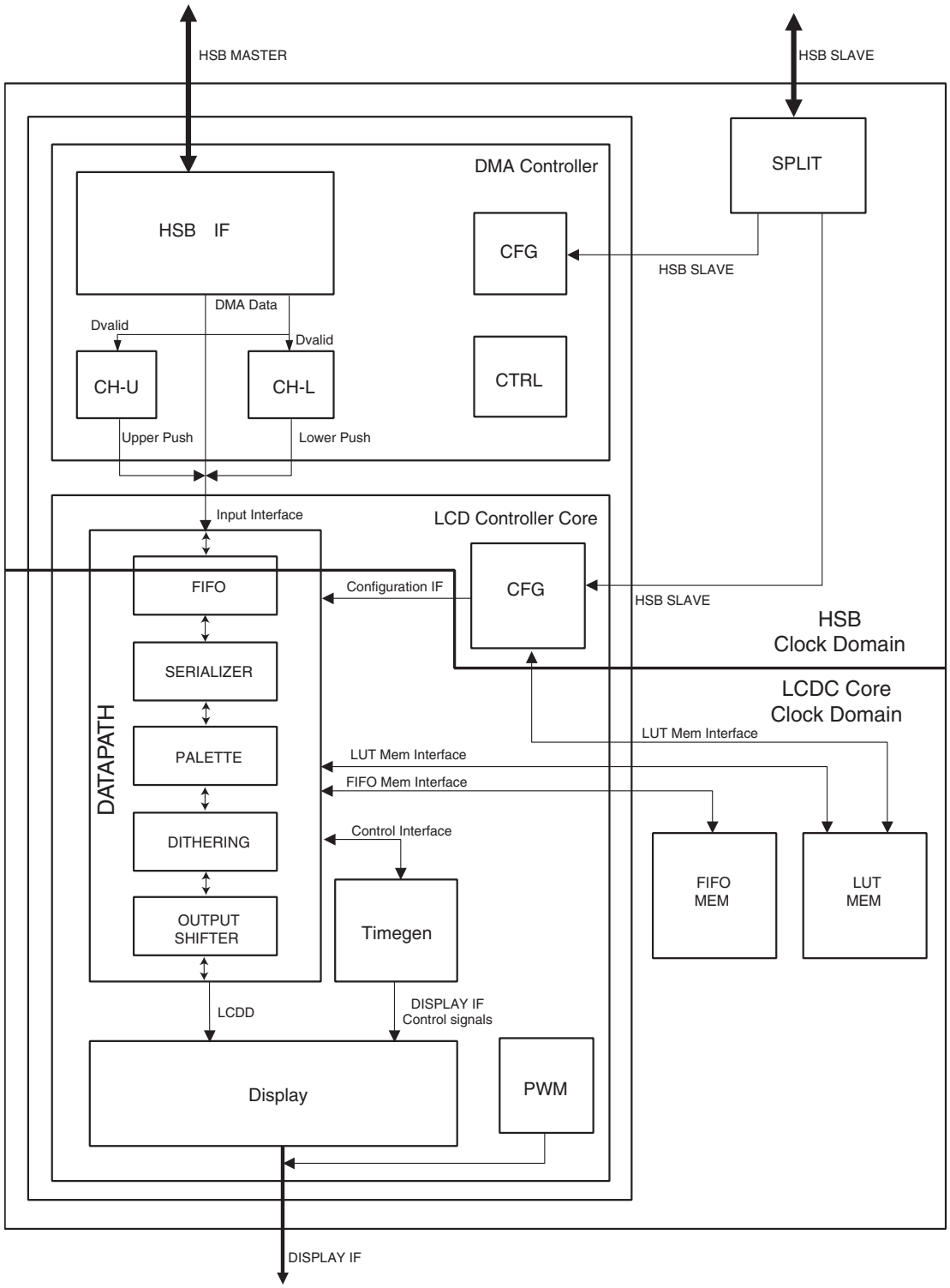
The LCD Controller has a display input buffer (FIFO) to allow a flexible connection of the external high speed bus master interface, and a lookup table to allow palletized display configurations.

The LCD Controller is programmable in order to support many different requirements such as resolutions up to 2048 x 2048; pixel depth (1, 2, 4, 8, 16, 24 bits per pixel); data line width (4, 8, 16 or 24 bits) and interface timing.

The LCD Controller is connected to the High Speed Bus (HSB) as a master for reading pixel data. However, the LCD Controller interfaces with the HSB as a slave in order to configure its registers.

35.3 Block Diagram

Figure 35-1. LCD Macrocell Block Diagram



35.4 I/O Lines Description

Table 35-1. I/O Lines Description

Name	Description	Type
CC	Contrast control signal	Output
HSYNC	Line synchronous signal (STN) or Horizontal synchronous signal (TFT)	Output
PCLK	LCD pixel clock signal (STN/TFT)	Output
VSYNC	Frame synchronous signal (STN) or Vertical synchronization signal (TFT)	Output
DVAL	STN AC bias signal for the driver or Data enable signal (TFT)	Output
MOD	LCD Modulation signal	Output
PWR	LCD panel Power enable control signal	Output
GP[7:0]	LCD General purpose lines	Output
LCDD[23:0]	LCD Data Bus output	Output

35.5 Product Dependencies

35.5.1 I/O Lines

The pins used for interfacing the LCD Controller may be multiplexed with PIO lines. The programmer must first program the PIO Controller to assign the pins to their peripheral function. If I/O lines of the LCD Controller are not used by the application, they can be used for other purposes by the PIO Controller.

35.5.2 Power Management

The LCDC Core Clock, which is used to generate the PCLK output and the other LCD synchronization signals, is driven by a generic clock output in the Power Manager. Before using the LCDC, the programmer must ensure that the correct generic clock is enabled in the Power Manager. The generic clock number used for the LCDC is listed in the Power Manager chapter.

35.5.3 Interrupt Sources

The LCD interface has an interrupt line connected to the interrupt controller. In order to handle interrupts, the interrupt controller must be programmed before configuring the LCD.

35.5.4 Clock Management

When the LCDC is being used in a system with SDRAM, the SDRAM clock frequency must be greater than the frequency of the LCDC Core Clock.

35.6 Functional Description

The LCD Controller consists of two main blocks (Figure 35-1 on page 804), the DMA controller and the LCD controller core (LCDC core). The DMA controller reads the display data from an external memory through a HSB master interface. The LCD controller core formats the display data. The LCD controller core continuously pumps the pixel data into the LCD module via the LCD data bus (LCDD[23:0]); this bus is timed by the PCLK, DVAL, HSYNC, and VSYNC signals.

35.6.1 DMA Controller

35.6.1.1 Configuration Block

The configuration block is a set of programmable registers that are used to configure the DMA controller operation. These registers are written via the HSB slave interface. Only word access is allowed.

For details on the configuration registers, see "LCD Controller (LCDC) User Interface" on page 835.

35.6.1.2 HSB Interface

This block generates the HSB transactions. It generates undefined-length incrementing bursts as well as 4- ,8- or 16-beat incrementing bursts. The size of the transfer can be configured in the BRSTLEN field of the DMAFRMCFG register. For details on this register, see "DMA Frame Configuration Register" on page 843.

35.6.1.3 Channel-U

This block stores the base address and the number of words transferred for this channel (frame in single scan mode and Upper Panel in dual scan mode) since the beginning of the frame. It also generates the end of frame signal.

It has two pointers, the base address and the number of words to transfer. When the module receives a new_frame signal, it reloads the number of words to transfer pointer with the size of the frame/panel. When the module receives the new_frame signal, it also reloads the base address with the base address programmed by the host.

The size of the frame/panel can be programmed in the FRMSIZE field of the DMAFRMCFG Register. This size is calculated as follows:

- In TFT mode:

$$\text{Frame_size} = \left\lceil \frac{\text{Display_size} \times \text{Bpp}}{32} \right\rceil$$

- In STN Monochrome mode:

$$\text{Frame_size} = \left\lceil \frac{(\text{LINEVAL} + 1) \times (\text{HOZVAL} + 1) \times \text{E_ifwidth} \times \text{Bpp}}{32} \right\rceil$$

- In STN Color mode:

$$\text{Frame_size} = \left\lceil \frac{(\text{LINEVAL} + 1)\left(\frac{(\text{HOZVAL} + 1) \times \text{E_ifwidth}}{3}\right)\text{Bpp}}{32} \right\rceil$$

where:

- LINEVAL is the value of the LINEVAL field of the LCDFRMCFG register of LCD Controller
- HOZVAL is the value of the HOZVAL field of the LCDFRMCFG register of the LCD Controller
- E_ifwidth is the number of data bits in the LCD interface for each panel
- Bpp is the bits per pixel configuration

$$\text{Frame_size} = \left\lceil \frac{\text{X_size*Y_size}}{32} \right\rceil$$

X_size = ((LINESIZE+1)*Bpp+PIXELOFF)/32

Y_size = (LINEVAL+1)

- LINESIZE is the horizontal size of the display in pixels, minus 1, as programmed in the LINESIZE field of the LCDFRMCFG register of the LCD Controller.
- Bpp is the number of bits per pixel configured.
- PIXELOFF is the pixel offset for 2D addressing, as programmed in the DMA2DCFG register. Applicable only if 2D addressing is being used.
- LINEVAL is the vertical size of the display in pixels, minus 1, as programmed in the LINEVAL field of the LCDFRMCFG register of the LCD Controller.

Note: X_size is calculated as an up-rounding of a division by 32. (This can also be done adding 31 to the dividend before using an integer division by 32). When using the 2D-addressing mode (see "2D Memory Addressing" on page 829), it is important to note that the above calculation must be executed and the FRMSIZE field programmed with every movement of the displaying window, since a change in the PIXELOFF field can change the resulting FRMSIZE value.

35.6.1.4 Channel-L

This block has the same functionality as Channel-U, but for the Lower Panel in dual scan mode only.

35.6.1.5 Control

This block receives the request signals from the LCDC core and generates the requests for the channels.

35.6.2 LCD Controller Core

35.6.2.1 Configuration Block

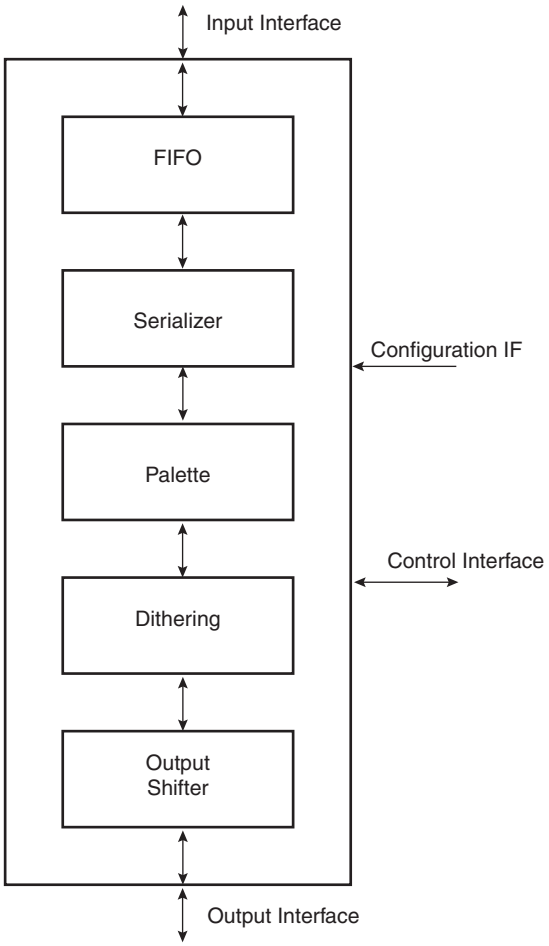
The configuration block is a set of programmable registers that are used to configure the LCDC core operation. These registers are written via the HSB slave interface. Only word access is allowed.

The description of the configuration registers can be found in "LCD Controller (LCDC) User Interface" on page 835.

35.6.2.2 Datapath

The datapath block contains five submodules: FIFO, Serializer, Palette, Dithering and Shifter. The structure of the datapath is shown in Figure 35-2.

Figure 35-2. Datapath Structure



This module transforms the data read from the memory into a format according to the LCD module used. It has four different interfaces: the input interface, the output interface, the configuration interface and the control interface.

- The input interface connects the datapath with the DMA controller. It is a dual FIFO interface with a data bus and two push lines that are used by the DMA controller to fill the FIFOs.
- The output interface is a 24-bit data bus. The configuration of this interface depends on the type of LCD used (TFT or STN, Single or Dual Scan, 4-bit, 8-bit, 16-bit or 24-bit interface).
- The configuration interface connects the datapath with the configuration block. It is used to select between the different datapath configurations.
- The control interface connects the datapath with the timing generation block. The main control signal is the data-request signal, used by the timing generation module to request new data from the datapath.

The datapath can be characterized by two parameters: initial_latency and cycles_per_data. The parameter initial_latency is defined as the number of LCDC Core Clock cycles until the first data is available at the output of the datapath. The parameter cycles_per_data is the minimum number of LCDC Core Clock cycles between two consecutive data at the output interface.

These parameters are different for the different configurations of the LCD Controller and are shown in Table 35-2.

Table 35-2. Datapath Parameters

Configuration				
DISTYPE	**SCAN**	**IFWIDTH**	**initial_latency**	**cycles_per_data**
TFT			9	1
STN Mono	Single	4	13	4
STN Mono	Single	8	17	8
STN Mono	Dual	8	17	8
STN Mono	Dual	16	25	16
STN Color	Single	4	11	2
STN Color	Single	8	12	3
STN Color	Dual	8	14	4
STN Color	Dual	16	15	6

35.6.2.3 FIFO

The FIFO block buffers the input data read by the DMA module. It contains two input FIFOs to be used in Dual Scan configuration that are configured as a single FIFO when used in single scan configuration.

The size of the FIFOs allows a wide range of architectures to be supported.

The upper threshold of the FIFOs can be configured in the FIFOTH field of the LCDFIFO register. The LCDC core will request a DMA transfer when the number of words in each FIFO is less than FIFOTH words. To avoid overwriting in the FIFO and to maximize the FIFO utilization, the FIFOTH should be programmed with:

FIFOTH = LCD_FIFO_SIZE - (2 x DMA_burst_length + 3)

where:

- LCD_FIFO_SIZE is the effective size of the FIFO. It is the total FIFO memory size in single scan mode and half that size in dual scan mode.
- DMA_burst_length is the burst length of the transfers made by the DMA

35.6.2.4 Serializer

This block serializes the data read from memory. It reads words from the FIFO and outputs pixels (1 bit, 2 bits, 4 bits, 8 bits, 16 bits or 24 bits wide) depending on the format specified in the PIXELSIZE field of the LCDCON2 register. It also adapts the memory-ordering format. Both big-endian and little-endian formats are supported. They are configured in the MEMOR field of the LCDCON2 register.

The organization of the pixel data in the memory depends on the configuration and is shown in Table 35-3 and Table 35-4.

Note: For a color depth of 24 bits per pixel there are two different formats supported: packed and unpacked. The packed format needs less memory but has some limitations when working in 2D addressing mode (See Section “35.10” on page 829.).

Table 35-3. Little Endian Memory Organization

Mem Addr	0x3								0x2								0x1								0x0							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 1bpp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 2bpp	15		14		13		12		11		10		9		8		7		6		5		4		3		2		1		0	
Pixel 4bpp	7				6				5				4				3				2				1				0	
Pixel 8bpp	3								2								1								0							
Pixel 16bpp	1																0															
Pixel 24bpp	1								0																							
Pixel 24bpp	2																1															
Pixel 24bpp	3																								2							
Pixel 24bpp	5								4																							

Table 35-4. Big Endian Memory Organization

Mem Addr	0x3								0x2								0x1								0x0							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 1bpp	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Pixel 2bpp	0		1		2		3		4		5		6		7		8		9		10		11		12		13		14		15	
Pixel 4bpp	0				1				2				3				4				5				6				7			
Pixel 8bpp	0								1								2								3							
Pixel 16bpp	0																1															
Pixel 24bpp packed	0																								1							
Pixel 24bpp packed	1																2															

Table 35-4. Big Endian Memory Organization

Mem Addr	0x3	0x2	0x1	0x0
Pixel 24bpp packed	2	3		
Pixel 24bpp packed	4			5
Pixel 24bpp unpacked	not used	0		

Table 35-5. WinCE Pixel Memory Organization

Mem Addr	0x3								0x2								0x1								0x0							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pixel 1bpp	24	25	26	27	28	29	30	31	16	17	18	19	20	21	22	23	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
Pixel 2bpp	12		13		14		15		8		9		10		11		4		5		6		7		0		1		2		3	
Pixel 4bpp	6				7				4				5				2				3				0				1			
Pixel 8bpp	3								2								1								0							
Pixel 16bpp	1																0															
Pixel 24bpp packed	1								0																							
Pixel 24bpp packed	2																1															
Pixel 24bpp packed	3																								2							
Pixel 24bpp unpacked	not used								0																							

35.6.2.5 Palette

This block is used to generate the pixel gray or color information in palletized configurations. The different modes with the palletized/non-palletized configuration can be found in Table 35-6. In

these modes, 1, 2, 4 or 8 input bits index an entry in the lookup table. The corresponding entry in the lookup table contains the color or gray shade information for the pixel.

Table 35-6. Palette Configurations

Configuration		
DISTYPE	**PIXELSIZE**	**Palette**
TFT	1, 2, 4, 8	Palletized
TFT	16, 24	Non-palletized
STN Mono	1, 2	Palletized
STN Mono	4	Non-palletized
STN Color	1, 2, 4, 8	Palletized
STN Color	16	Non-palletized

The lookup table can be accessed by the host in R/W mode to allow the host to program and check the values stored in the palette. It is mapped in the LCD controller configuration memory map. The LUT is mapped as 16-bit half-words aligned at word boundaries, only word write access is allowed (the 16 MSB of the bus are not used). For the detailed memory map, see Table 35-13 on page 835.

The lookup table contains 256 16-bit wide entries. The 256 entries are chosen by the programmer from the 2^{16} possible combinations.

For the structure of each LUT entry, see Table 35-7.

Table 35-7. Lookup Table Structure in the Memory

Address	Data Output [15:0]			
00	Intensity_bit_0	Blue_value_0[4:0]	Green_value_0[4:0]	Red_value_0[4:0]
01	Intensity_bit_1	Blue_value_1[4:0]	Green_value_1[4:0]	Red_value_1[4:0]
...				
FE	Intensity_bit_254	Blue_value_254[4:0]	Green_value_254[4:0]	Red_value_254[4:0]
FF	Intensity_bit_255	Blue_value_255[4:0]	Green_value_255[4:0]	Red_value_255[4:0]

In STN Monochrome, only the four most significant bits of the red value are used (16 gray shades). In STN Color, only the four most significant bits of the blue, green and red value are used (4096 colors).

In TFT mode, all the bits in the blue, green and red values are used (32768 colors). In this mode, there is also a common intensity bit that can be used to double the possible colors. This bit is the least significant bit of each color component in the LCDD interface (LCDD[18], LCDD[10], LCDD[2]). The LCDD unused bits are tied to 0 when TFT palletized configurations are used (LCDD[17:16], LCDD[9:8], LCDD[1:0]).

35.6.2.6 Dithering

The dithering block is used to generate the shades of gray or color when the LCD Controller is used with an STN LCD Module. It uses a time-based dithering algorithm and Frame Rate Control method.

The Frame Rate Control varies the duty cycle for which a given pixel is turned on, giving the display an appearance of multiple shades. In order to reduce the flicker noise caused by turning on and off adjacent pixels at the same time, a time-based dithering algorithm is used to vary the pattern of adjacent pixels every frame. This algorithm is expressed in terms of Dithering Pattern registers (DP_i) and considers not only the pixel gray level number, but also its horizontal coordinate.

Table 35-8 shows the correspondences between the gray levels and the duty cycle.

Table 35-8. Dithering Duty Cycle

Gray Level	Duty Cycle	Pattern Register
15	1	-
14	6/7	DP6_7
13	4/5	DP4_5
12	3/4	DP3_4
11	5/7	DP5_7
10	2/3	DP2_3
9	3/5	DP3_5
8	4/7	DP4_7
7	1/2	~DP1_2
6	3/7	~DP4_7
5	2/5	~DP3_5
4	1/3	~DP2_3
3	1/4	~DP3_4
2	1/5	~DP4_5
1	1/7	~DP6_7
0	0	-

The duty cycles for gray levels 0 and 15 are 0 and 1, respectively.

The same DP_i register can be used for the pairs for which the sum of duty cycles is 1 (e.g., 1/7 and 6/7). The dithering pattern for the first pair member is the inversion of the one for the second.

The DP_i registers contain a series of 4-bit patterns. The $(3\text{-}m)^{th}$ bit of the pattern determines if a pixel with horizontal coordinate x = 4n + m (n is an integer and m ranges from 0 to 3) should be turned on or off in the current frame. The operation is shown by the examples below.

Consider the pixels a, b, c and d with the horizontal coordinates 4*n+0, 4*n+1, 4*n+2 and 4*n+3, respectively. The four pixels should be displayed in gray level 9 (duty cycle 3/5) so the register used is DP3_5 =”1010 0101 1010 0101 1111”.

The output sequence obtained in the data output for monochrome mode is shown in Table 35-9.

Table 35-9. Dithering Algorithm for Monochrome Mode

Frame Number	Pattern	Pixel a	Pixel b	Pixel c	Pixel d
N	1010	ON	OFF	ON	OFF
N+1	0101	OFF	ON	OFF	ON
N+2	1010	ON	OFF	ON	OFF
N+3	0101	OFF	ON	OFF	ON
N+4	1111	ON	ON	ON	ON
N+5	1010	ON	OFF	ON	OFF
N+6	0101	OFF	ON	OFF	ON
N+7	1010	ON	OFF	ON	OFF
...	...	...	...	...	...

Consider now color display mode and two pixels p0 and p1 with the horizontal coordinates 4*n+0, and 4*n+1. A color pixel is composed of three components: {R, G, B}. Pixel p0 will be displayed sending the color components {R0, G0, B0} to the display. Pixel p1 will be displayed sending the color components {R1, G1, B1}. Suppose that the data read from memory and mapped to the lookup tables corresponds to shade level 10 for the three color components of both pixels, with the dithering pattern to apply to all of them being DP2_3 = “1101 1011 0110”. Table 35-10 shows the output sequence in the data output bus for single scan configurations. (In Dual Scan Configuration, each panel data bus acts like in the equivalent single scan configuration.)

Table 35-10. Dithering Algorithm for Color Mode

Frame	Signal	Shadow Level	Bit used	Dithering Pattern	4-bit LCDD	8-bit LCDD	Output
N	red_data_0	1010	3	1101	LCDD[3]	LCDD[7]	R0
N	green_data_0	1010	2	1101	LCDD[2]	LCDD[6]	G0
N	blue_data_0	1010	1	1101	LCDD[1]	LCDD[5]	b0
N	red_data_1	1010	0	1101	LCDD[0]	LCDD[4]	R1
N	green_data_1	1010	3	1101	LCDD[3]	LCDD[3]	G1
N	blue_data_1	1010	2	1101	LCDD[2]	LCDD[2]	B1
…	…	…	…	…	…	…	…
N+1	red_data_0	1010	3	1011	LCDD[3]	LCDD[7]	R0
N+1	green_data_0	1010	2	1011	LCDD[2]	LCDD[6]	g0
N+1	blue_data_0	1010	1	1011	LCDD[1]	LCDD[5]	B0
N+1	red_data_1	1010	0	1011	LCDD[0]	LCDD[4]	R1
N+1	green_data_1	1010	3	1011	LCDD[3]	LCDD[3]	G1
N+1	blue_data_1	1010	2	1011	LCDD[2]	LCDD[2]	b1
…	…	…	…	…	…	…	…
N+2	red_data_0	1010	3	0110	LCDD[3]	LCDD[7]	r0

Table 35-10. Dithering Algorithm for Color Mode (Continued)

Frame	Signal	Shadow Level	Bit used	Dithering Pattern	4-bit LCDD	8-bit LCDD	Output
N+2	green_data_0	1010	2	0110	LCDD[2]	LCDD[6]	G0
N+2	blue_data_0	1010	1	0110	LCDD[1]	LCDD[5]	B0
N+2	red_data_1	1010	0	0110	LCDD[0]	LCDD[4]	r1
N+2	green_data_1	1010	3	0110	LCDD[3]	LCDD[3]	g1
N+2	blue_data_1	1010	2	0110	LCDD[2]	LCDD[2]	B1
…	…	…	…	…	…	…	…

Note: Ri = red pixel component ON. Gi = green pixel component ON. Bi = blue pixel component ON. ri = red pixel component OFF. gi = green pixel component OFF. bi = blue pixel component OFF.

35.6.2.7 Shifter

The FIFO, Serializer, Palette and Dithering modules process one pixel at a time in monochrome mode and three sub-pixels at a time in color mode (R,G,B components). This module packs the data according to the output interface. This interface can be programmed in the DISTYPE, SCANMOD, and IFWIDTH fields of the LCDCON2 register.

The DISTYPE field selects between TFT, STN monochrome and STN color display. The SCANMODE field selects between single and dual scan modes; in TFT mode, only single scan is supported. The IFWIDTH field configures the width of the interface in STN mode: 4-bit (in single scan mode only), 8-bit and 16-bit (in dual scan mode only).

For a more detailed description of the fields, see ”LCD Controller (LCDC) User Interface” on page 835.

For a more detailed description of the LCD Interface, see ”LCD Interface” on page 821.

35.6.2.8 Timegen

The time generator block generates the control signals PCLK, HSYNC, VSYNC, DVAL, and MODE, used by the LCD module. This block is programmable in order to support different types of LCD modules and obtain the output clock signals, which are derived from the LCDC Core Clock.

The MODE signal provides an AC signal for the display. It is used by the LCD to alternate the polarity of the row and column voltages used to turn the pixels on and off. This prevents the liquid crystal from degradation. It can be configured to toggle every frame (bit MMODE = 0 in LCDMVAL register) or to toggle every programmable number of HSYNC pulses (bit MMODE = 1, number of pulses defined in MVAL field of LCDMVAL register).

$$f_{LCD_MODE} = \frac{f_{LCD_HSYNC}}{2 \times (MVAL + 1)}$$

Figure 35-3 and Figure 35-4 on page 816 show the timing of MODE in both configurations.

Figure 35-3. Full Frame Timing, MMODE=1, MVAL=1

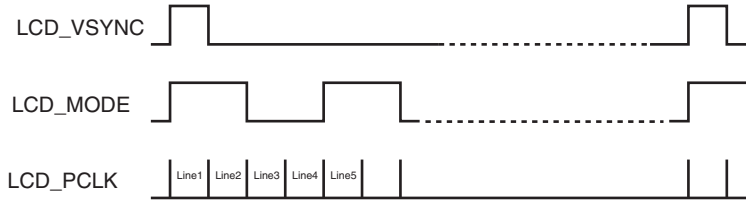
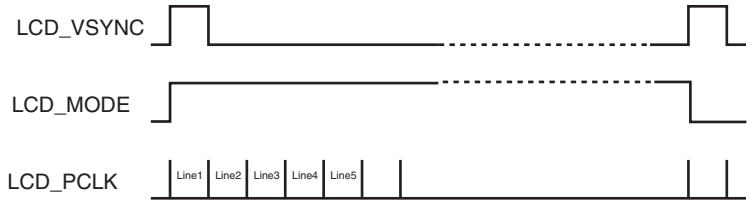


Figure 35-4. Full Frame Timing, MMODE=0



The PCLK signal is used to clock the data into the LCD drivers' shift register. The data is sent through LCDD[23:0] synchronized by default with the PCLK falling edge (rising edge can be selected). The CLKVAL field of LCDCON1 register controls the rate of this signal. The divisor can also be bypassed with the BYPASS bit in the LCDCON1 register. In this case, the rate of PCLK is equal to the frequency of the LCDC Core Clock. The minimum period of the PCLK signal depends on the configuration. This information can be found in Table 35-11.

$$f_{LCD_PCLK} = \frac{f_{LCDC_clock}}{2 \times CLKVAL}$$

The PCLK signal has two different timings that are selected with the CLKMOD field of the LCDCON2 register:

- Always Active (used with TFT LCD Modules)
- Active only when data is available (used with STN LCD Modules)

Table 35-11. Minimum PCLK Period in LCDC Core Clock Cycles

Configuration			
DISTYPE	**SCAN**	**IFWIDTH**	**PCLK Period**
TFT			1
STN Mono	Single	4	4
STN Mono	Single	8	8
STN Mono	Dual	8	8
STN Mono	Dual	16	16
STN Color	Single	4	2

Table 35-11. Minimum PCLK Period in LCDC Core Clock Cycles

Configuration			PCLK Period
DISTYPE	**SCAN**	**IFWIDTH**	
STN Color	Single	8	2
STN Color	Dual	8	4
STN Color	Dual	16	6

The DVAL signal indicates valid data in the LCD Interface.

After each horizontal line of data has been shifted into the LCD, the HSYNC is asserted to cause the line to be displayed on the panel.

The following timing parameters can be configured:

- Vertical to Horizontal Delay (VHDLY): The delay between begin_of_line and the generation of HSYNC is configurable in the VHDLY field of the LCDTIM1 register. The delay is equal to (VHDLY+1) PCLK cycles.
- Horizontal Pulse Width (HPW): The HSYNC pulse width is configurable in HPW field of LCDTIM2 register. The width is equal to (HPW + 1) PCLK cycles.
- Horizontal Back Porch (HBP): The delay between the HSYNC falling edge and the first PCLK rising edge with valid data at the LCD Interface is configurable in the HBP field of the LCDTIM2 register. The delay is equal to (HBP+1) PCLK cycles.
- Horizontal Front Porch (HFP): The delay between end of valid data and the end of the line is configurable in the HFP field of the LCDTIM2 register. The delay is equal to (HFP+1) PCLK cycles.

There is a limitation in the minimum values of VHDLY, HPW and HBP parameters imposed by the initial latency of the datapath. The total delay in LCDC Core Clock cycles must be higher than or equal to the latency column in Table 35-2 on page 809. This limitation is given by the following formula:

35.6.2.9 Equation 1

$$(\mathrm{VHDLY} + \mathrm{HPW} + \mathrm{HBP} + 3) \times \mathrm{PCLK_PERIOD} \geq \mathrm{DPATH_LATENCY}$$

where:

- VHDLY, HPW, HBP are the value of the fields of LCDTIM1 and LCDTIM2 registers
- PCLK_PERIOD is the period of PCLK signal measured in LCDC Core Clock cycles
- DPATH_LATENCY is the datapath latency of the configuration, given in Table 35-2 on page 809

The VSYNC is asserted once per frame. This signal is asserted to cause the LCD's line pointer to start over at the top of the display. The timing of this signal depends on the type of LCD: STN or TFT LCD.

In STN mode, the high phase corresponds to the complete first line of the frame. In STN mode, this signal is synchronized with the first active PCLK rising edge in a line.

In TFT mode, the high phase of this signal starts at the beginning of the first line. The following timing parameters can be selected:

- Vertical Pulse Width (VPW): VSYNC pulse width is configurable in VPW field of the LCDTIM1 register. The pulse width is equal to (VPW+1) lines.

- Vertical Back Porch: Number of inactive lines at the beginning of the frame is configurable in VBP field of LCDTIM1 register. The number of inactive lines is equal to VBP. This field should be programmed with 0 in STN Mode.
- Vertical Front Porch: Number of inactive lines at the end of the frame is configurable in VFP field of LCDTIM2 register. The number of inactive lines is equal to VFP. This field should be programmed with 0 in STN mode.

There are two other parameters to configure in this module, the HOZVAL and the LINEVAL fields of the LCDFRMCFG:

- HOZVAL configures the number of active PCLK cycles in each line. The number of active cycles in each line is equal to (HOZVAL+1) cycles. The minimum value of this parameter is 1.
- LINEVAL configures the number of active lines per frame. This number is equal to (LINEVAL+1) lines. The minimum value of this parameter is 1.

Figure 35-5, Figure 35-6 and Figure 35-7 show the timing of MODE, PCLK, DVAL, HSYNC and VSYNC signals:

Figure 35-5. STN Panel Timing, CLKMOD 0

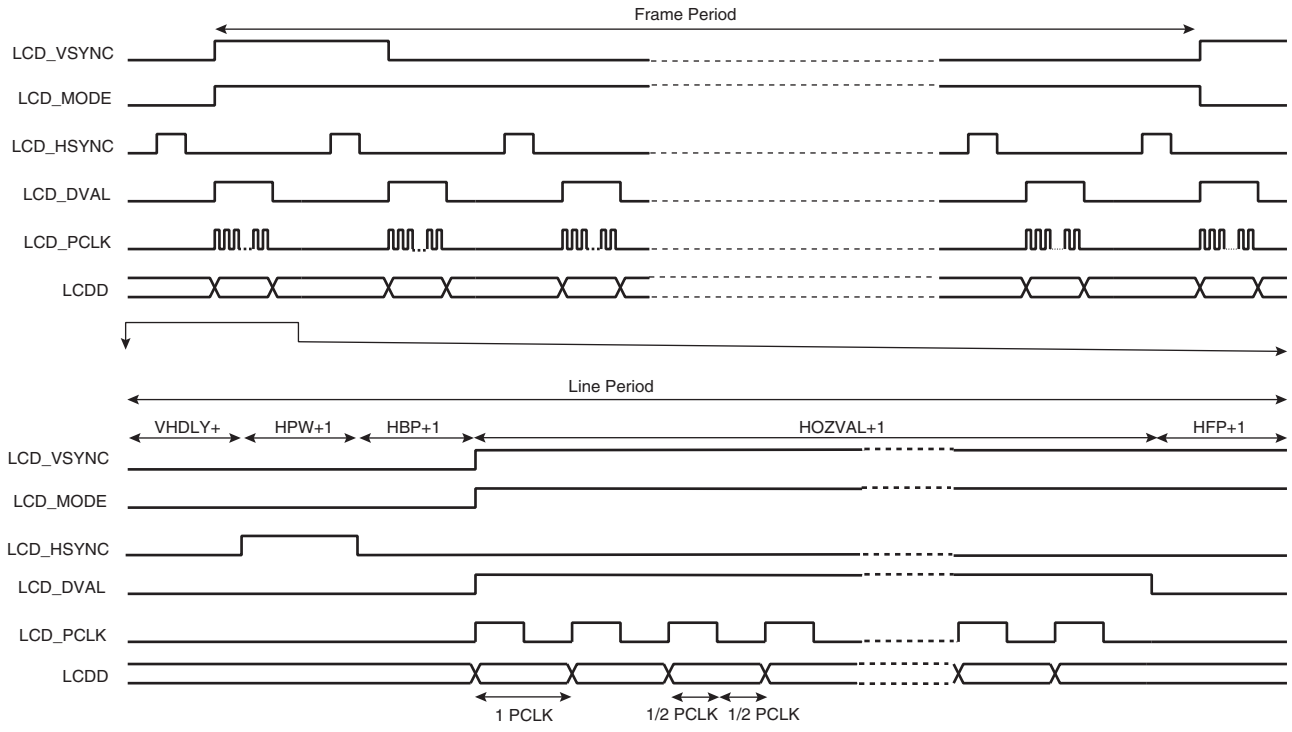


Figure 35-6. TFT Panel Timing, CLKMOD = 0, VPW = 2, VBP = 2, VFP = 1

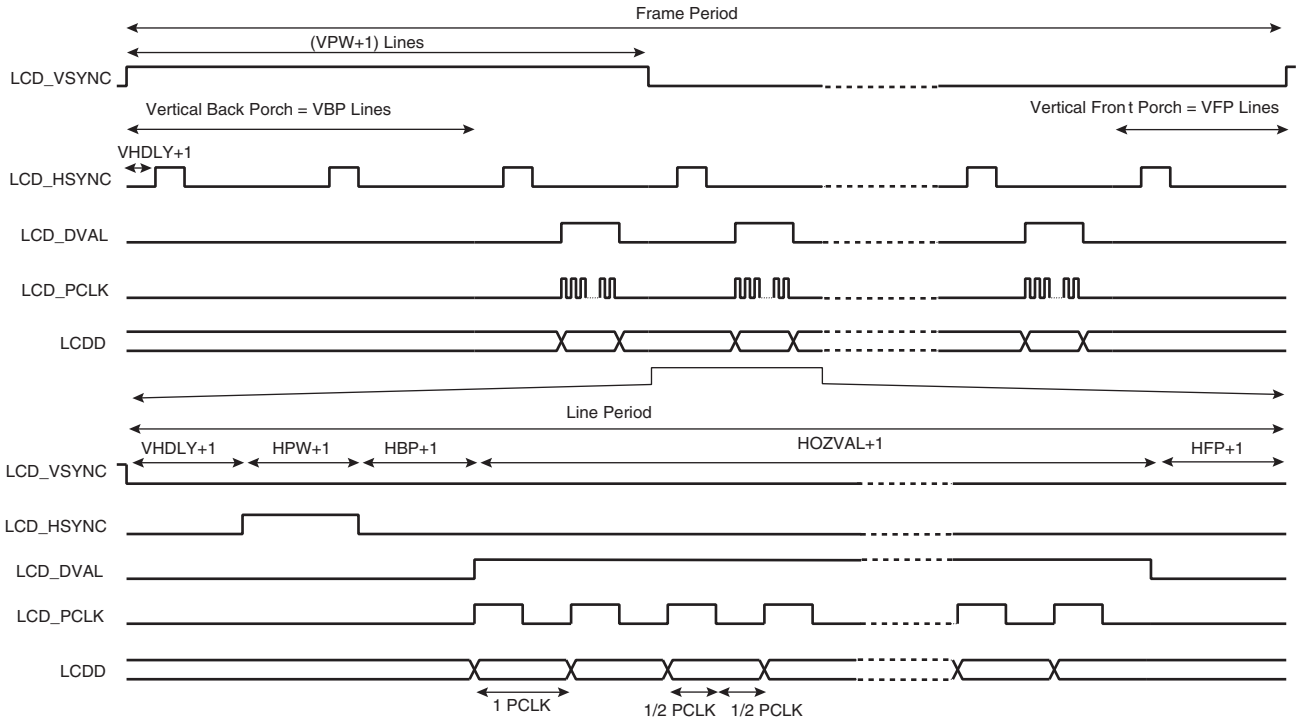
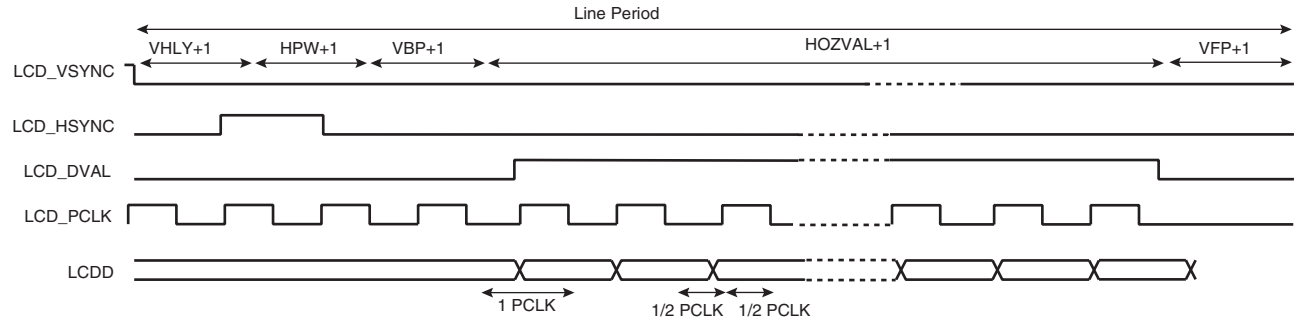


Figure 35-7. TFT Panel Timing (Line Expanded View), CLKMOD=1



Usually the FRM rate is about 70 Hz to 75 Hz. It is given by the following equation:

$$\frac{1}{f_{lcd_vsync}} = \left(\frac{VHDLY + HPW + HBP + HOZVAL + HFP + 5}{f_{lcd_pclk}}\right)(VBP + LINEVAL + VFP + 1)$$

where:

- HOZVAL determines de number of PCLK cycles per line
- LINEVAL determines the number of hsync cycles per frame, according to the expressions shown below:

In STN Mode:

$$HOZVAL = \frac{Horizontal_display_size}{Number_data_lines} - 1$$

$$LINEVAL = Vertical_display_size - 1$$

In monochrome mode, Horizontal_display_size is equal to the number of horizontal pixels. The number_data_lines is equal to the number of bits of the interface in single scan mode; number_data_lines is equal to half the bits of the interface in dual scan mode.

In color mode, Horizontal_display_size equals three times the number of horizontal pixels.

In TFT Mode:

$$HOZVAL = Horizontal_display_size - 1$$

$$LINEVAL = Vertical_display_size - 1$$

The frame rate equation is used first without considering the clock periods added at the end beginning or at the end of each line to determine, approximately, the PCLK rate:

$$f_{lcd_pclk} = (HOZVAL + 5) \times (f_{lcd_vsync} \times (LINEVAL + 1))$$

With this value, the CLKVAL is fixed, as well as the corresponding PCLK rate.

Then select VHDLY, HPW and HBP according to the type of LCD used and "Equation 1" on page 817.

Finally, the frame rate is adjusted to 70 Hz - 75 Hz with the HFP value:

$$HFP = f_{pclk} \times \left[\frac{1}{f_{lcd_vsync} \times (LINEVAL + VBP + VFP + 1)}\right] - (VHDLY + VPW + VBP + HOZVAL + 5)$$

The line counting is controlled by the read-only field LINECNT of LCDCON1 register. The LINECNT field decreases by one unit at each falling edge of hsync.

35.6.2.10 Display

This block is used to configure the polarity of the data and control signals. The polarity of all clock signals can be configured by LCDCON2[12:8] register setting.

The block also generates the LCD_PWR output that can be used to turn the LCD module on and off by software. This signal is controlled by the PWRCON register and respects the number of frames configured in the GUARD_TIME field of PWRCON register (PWRCON[7:1]) between the write access to LCD_PWR field (PWRCON[0]) and the activation/deactivation of LCD_PWR output signal. The minimum value for the GUARD_TIME field is one frame. This gives the DMA Controller enough time to fill the FIFOs before the start of data transfer to the LCD.

35.6.2.11 PWM

This block generates the LCD contrast control signal (CC) to make possible the control of the display's contrast by software. This is an 8-bit PWM (Pulse Width Modulation) signal that can be converted to an analog voltage with a simple passive filter.

The PWM module has a free-running counter whose value is compared against a compare register (CONTRAST_VAL register). If the value in the counter is less than that in the register, the output brings the value of the polarity (POL) bit in the PWM control register: CONTRAST_CTR. Otherwise, the opposite value is output. Thus, a periodic waveform with a pulse width proportional to the value in the compare register is generated.

Due to the comparison mechanism, the output pulse has a width between zero and 255 PWM counter cycles. Thus by adding a simple passive filter outside the chip, an analog voltage between 0 and (255/256) × VDD can be obtained (for the positive polarity case, or between (1/256) × VDD and VDD for the negative polarity case). Other voltage values can be obtained by adding active external circuitry.

For PWM mode, the frequency of the counter can be adjusted to four different values using field PS of CONTRAST_CTR register.

35.6.3 LCD Interface

The LCD Controller interfaces with the LCD Module through the LCD Interface (Table 35-12 on page 826). The Controller supports the following interface configurations: 24-bit TFT single scan, 16-bit STN Dual Scan Mono (Color), 8-bit STN Dual (Single) Scan Mono (Color), 4-bit single scan Mono (Color).

A 4-bit single scan STN display uses 4 parallel data lines to shift data to successive single horizontal lines one at a time until the entire frame has been shifted and transferred. The 4 LSB pins of LCD Data Bus (LCDD [3:0]) can be directly connected to the LCD driver; the 20 MSB pins (LCDD [23:4]) are not used.

An 8-bit single scan STN display uses 8 parallel data lines to shift data to successive single horizontal lines one at a time until the entire frame has been shifted and transferred. The 8 LSB pins of LCD Data Bus (LCDD [7:0]) can be directly connected to the LCD driver; the 16 MSB pins (LCDD [23:8]) are not used.

An 8-bit Dual Scan STN display uses two sets of 4 parallel data lines to shift data to successive upper and lower panel horizontal lines one at a time until the entire frame has been shifted and transferred. The bus LCDD[3:0] is connected to the upper panel data lines and the bus LCDD[7:4] is connected to the lower panel data lines. The rest of the LCD Data Bus lines (LCDD[23:8]) are not used.

A 16-bit Dual Scan STN display uses two sets of 8 parallel data lines to shift data to successive upper and lower panel horizontal lines one at a time until the entire frame has been shifted and transferred. The bus LCDD[7:0] is connected to the upper panel data lines and the bus LCDD[15:8] is connected to the lower panel data lines. The rest of the LCD Data Bus lines (LCDD[23:16]) are not used.

STN Mono displays require one bit of image data per pixel. STN Color displays require three bits (Red, Green and Blue) of image data per pixel, resulting in a horizontal shift register of length three times the number of pixels per horizontal line. This RGB or Monochrome data is shifted to the LCD driver as consecutive bits via the parallel data lines.

A TFT single scan display uses up to 24 parallel data lines to shift data to successive horizontal lines one at a time until the entire frame has been shifted and transferred. The 24 data lines are divided in three bytes that define the color shade of each color component of each pixel. The LCDD bus is split as LCDD[23:16] for the blue component, LCDD[15:8] for the green component and LCDD[7:0] for the red component. If the LCD Module has lower color resolution (fewer bits per color component), only the most significant bits of each component are used.

All these interfaces are shown in Figure 35-8 to Figure 35-12. Figure 35-8 on page 822 shows the 24-bit single scan TFT display timing; Figure 35-9 on page 822 shows the 4-bit single scan STN display timing for monochrome and color modes; Figure 35-10 on page 823 shows the 8-bit single scan STN display timing for monochrome and color modes; Figure 35-11 on page 824

shows the 8-bit Dual Scan STN display timing for monochrome and color modes; Figure 35-12 on page 825 shows the 16-bit Dual Scan STN display timing for monochrome and color modes.

Figure 35-8. TFT Timing (First Line Expanded View)

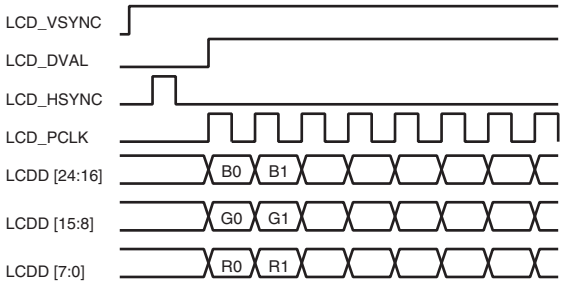


Figure 35-9. Single Scan Monochrome and Color 4-bit Panel Timing (First Line Expanded View)

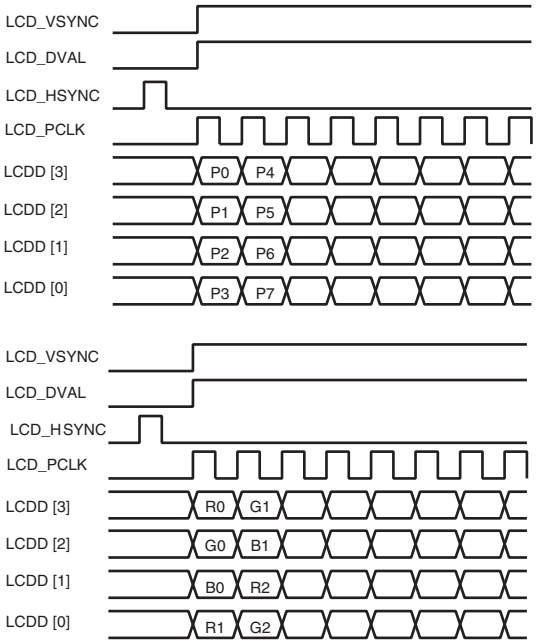


Figure 35-10. Single Scan Monochrome and Color 8-bit Panel Timing (First Line Expanded View)

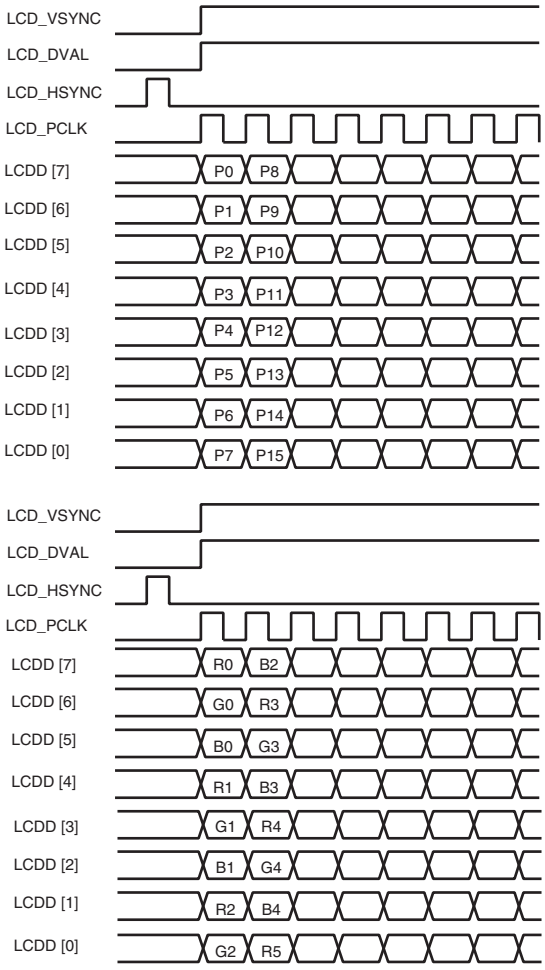


Figure 35-11. Dual Scan Monochrome and Color 8-bit Panel Timing (First Line Expanded View)

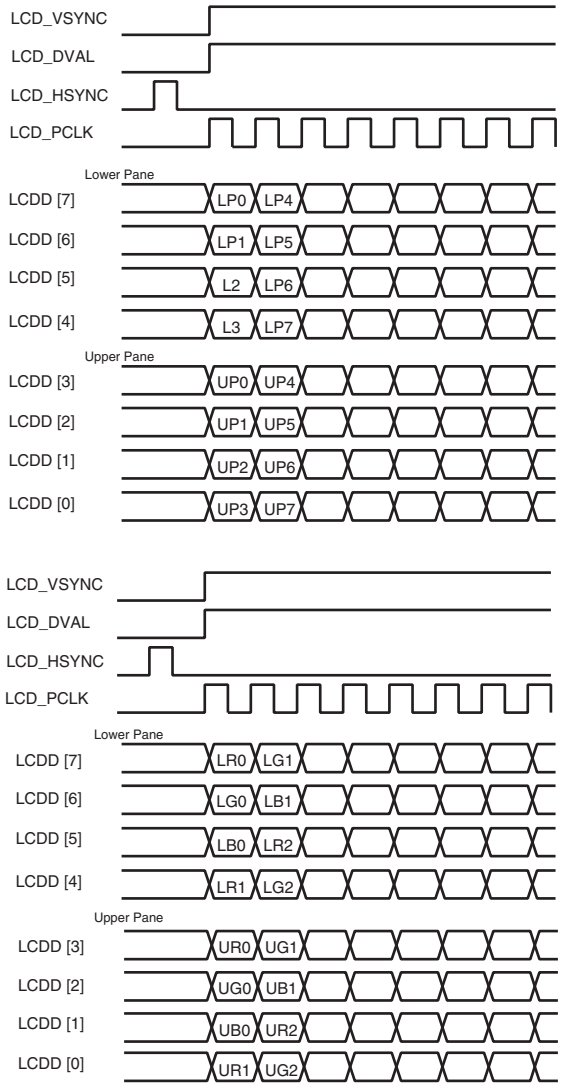


Figure 35-12. Dual Scan Monochrome and Color 16-bit Panel Timing (First Line Expanded View)

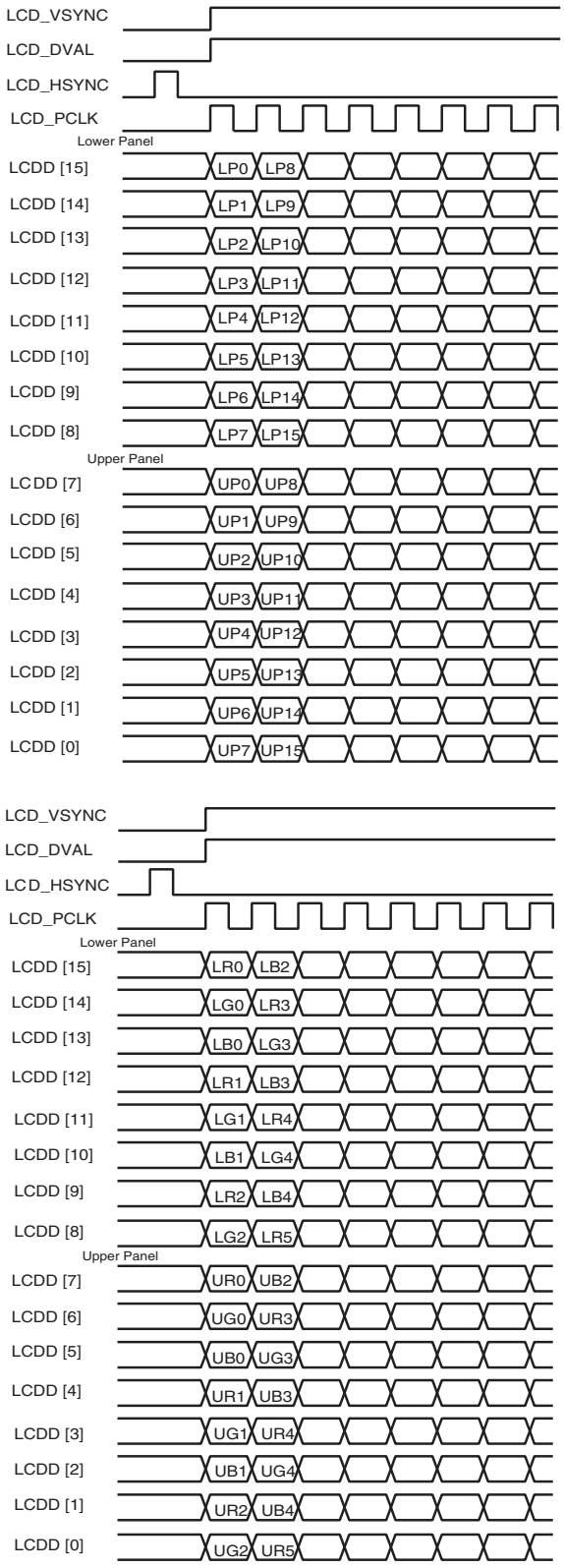


Table 35-12. LCD Signal Multiplexing

LCD Data Bus	4-bit STN Single Scan (mono, color)	8-bit STN Single Scan (mono, color)	8-bit STN Dual Scan (mono, color)	16-bit STN Dual Scan (mono, color)	24-bit TFT	16-bit TFT
LCDD[23]					BLUE7	BLUE4
LCDD[22]					BLUE6	BLUE3
LCDD[21]					BLUE5	BLUE2
LCDD[20]					BLUE4	BLUE1
LCDD[19]					BLUE3	BLUE0
LCDD[18]					BLUE2	Intensity Bit
LCDD[17]					BLUE1	
LCDD[16]					BLUE0	
LCDD[15]				LCDLP7	GREEN7	GREEN4
LCDD[14]				LCDLP6	GREEN6	GREEN3
LCDD[13]				LCDLP5	GREEN5	GREEN2
LCDD[12]				LCDLP4	GREEN4	GREEN1
LCDD[11]				LCDLP3	GREEN3	GREEN0
LCDD[10]				LCDLP2	GREEN2	Intensity Bit
LCDD[9]				LCDLP1	GREEN1	
LCDD[8]				LCDLP0	GREEN0	
LCDD[7]		LCD7	LCDLP3	LCDUP7	RED7	RED4
LCDD[6]		LCD6	LCDLP2	LCDUP6	RED6	RED3
LCDD[5]		LCD5	LCDLP1	LCDUP5	RED5	RED2
LCDD[4]		LCD4	LCDLP0	LCDUP4	RED4	RED1
LCDD[3]	LCD3	LCD3	LCDUP3	LCDUP3	RED3	RED0
LCDD[2]	LCD2	LCD2	LCDUP2	LCDUP2	RED2	Intensity Bit
LCDD[1]	LCD1	LCD1	LCDUP1	LCDUP1	RED1	
LCDD[0]	LCD0	LCD0	LCDUP0	LCDUP0	RED0	

35.7 Interrupts

The LCD Controller generates six different IRQs. All the IRQs are synchronized with the internal LCDC Core Clock. The IRQs are:

- DMA Memory error IRQ. Generated when the DMA receives an error response from an HSB slave while it is doing a data transfer.
- FIFO underflow IRQ. Generated when the Serializer tries to read a word from the FIFO when the FIFO is empty.
- FIFO overwrite IRQ. Generated when the DMA Controller tries to write a word in the FIFO while the FIFO is full.
- DMA end of frame IRQ. Generated when the DMA controller updates the Frame Base Address pointers. This IRQ can be used to implement a double-buffer technique. For more information, see ”Double-buffer Technique” on page 829.
- End of Line IRQ. This IRQ is generated when the LINEBLANK period of each line is reached and the DMA Controller is in inactive state.
- End of Last Line IRQ. This IRQ is generated when the LINEBLANK period of the last line of the current frame is reached and the DMA Controller is in inactive state.

Each IRQ can be individually enabled, disabled or cleared, in the IER (Interrupt Enable Register), IDR (Interrupt Disable Register) and ICR (Interrupt Clear Register) registers. The IMR register contains the mask value for each IRQ source and the LDC_ISR contains the status of each IRQ source. A more detailed description of these registers can be found in ”LCD Controller (LCDC) User Interface” on page 835.

35.8 Configuration Sequence

The DMA Controller starts to transfer image data when the LCDC Core is activated (Write to PWR field of PWRCON register). Thus, the user should configure the LCDC Core and configure and enable the DMA Controller prior to activation of the LCD Controller. In addition, the image data to be shows should be available when the LCDC Core is activated, regardless of the value programmed in the GUARD_TIME field of the PWRCON register.

To disable the LCD Controller, the user should disable the LCDC Core and then disable the DMA Controller. The user should not enable the LCDC again until the LCDC Core is in IDLE state. This is checked by reading the BUSY bit in the PWRCON register.

The initialization sequence that the user should follow to make the LCDC work is:

- Create or copy the first image to show in the display buffer memory.
- If a palletized mode is used, create and store a palette in the internal LCD Palette memory(See Section “35.6.2.5” on page 811.
- Configure the LCD Controller Core without enabling it:
  - LCDCON1 register: Program the CLKVAL and BYPASS fields: these fields control the pixel clock divisor that is used to generate the pixel clock PCLK. The value to program depends on the LCDC Core Clock and on the type and size of the LCD Module used. There is a minimum value of the PCLK clock period that depends on the LCD Controller Configuration, this minimum value can be found in Table 35-11 on page 816. The equations that are used to calculate the value of the pixel clock divisor can be found at the end of the section ”Timegen” on page 815

- –LCDCON2 register: Program its fields following their descriptions in the LCD Controller User Interface section below and considering the type of LCD module used and the desired working mode. Consider that not all combinations are possible.
- –LCDTIM1 and LCDTIM2 registers: Program their fields according to the datasheet of the LCD module used and with the help of the Timegen section in page 10. Note that some fields are not applicable to STN modules and must be programmed with 0 values. Note also that there is a limitation on the minimum value of VHDLY, HPW, HBP that depends on the configuration of the LCDC.
- –LCDFRMCFG register: program the dimensions of the LCD module used.
- –LCDFIFO register: To program it, use the formula in section "FIFO" on page 809
- –LCDMVAL register: Its configuration depends on the LCD Module used and should be tuned to improve the image quality in the display (See Section "35.6.2.8" on page 815.)
- –DP1_2 to DP6_7 registers: they are only used for STN displays. They contain the dithering patterns used to generate gray shades or colors in these modules. They are loaded with recommended patterns at reset, so it is not necessary to write anything on them. They can be used to improve the image quality in the display by tuning the patterns in each application.
- –PWRCON Register: this register controls the power-up sequence of the LCD, so take care to use it properly. Do not enable the LCD (writing a 1 in PWR field) until the previous steps and the configuration of the DMA have been finished.
- –CONTRAST_CTR and CONTRAST_VAL: use this registers to adjust the contrast of the display, when the *cc* line is used.

•Configure the DMA Controller. The user should configure the base address of the display buffer memory, the size of the HSB transaction and the size of the display image in memory. When the DMA is configured the user should enable the DMA. To do so the user should configure the following registers:

- –DMABADDR1 and DMABADDR2 registers: In single scan mode only DMABADDR1 register must be configured with the base address of the display buffer in memory. In dual scan mode DMABADDR1 should be configured with the base address of the Upper Panel display buffer and DMABADDR2 should be configured with the base address of the Lower Panel display buffer.
- –DMAFRMCFG register: Program the FRMSIZE field. Note that in dual scan mode the vertical size to use in the calculation is that of each panel. Respect to the BRSTLEN field, a recommended value is a 4-word burst.
- –DMACON register: Once both the LCD Controller Core and the DMA Controller have been configured, enable the DMA Controller by writing a "1" to the DMAEN field of this register. If using a dual scan module or the 2D addressing feature, do not forget to write the DMAUPDT bit after every change to the set of DMA configuration values.
- –DMA2DCFG register: Required only in 2D memory addressing mode (see "2D Memory Addressing" on page 829).

•Finally, enable the LCD Controller Core by writing a "1" in the PWR field of the PWRCON register and do any other action that may be required to turn the LCD module on.

35.9 Double-buffer Technique

The double-buffer technique is used to avoid flickering while the frame being displayed is updated. Instead of using a single buffer, there are two different buffers, the backbuffer (background buffer) and the primary buffer (the buffer being displayed).

The host updates the backbuffer while the LCD Controller is displaying the primary buffer. When the backbuffer has been updated the host updates the DMA Base Address registers.

When using a Dual Panel LCD Module, both base address pointers should be updated in the same frame. There are two possibilities:

- Check the DMAFRMPTx register to ensure that there is enough time to update the DMA Base Address registers before the end of frame.
- Update the Frame Base Address Registers when the End Of Frame IRQ is generated.

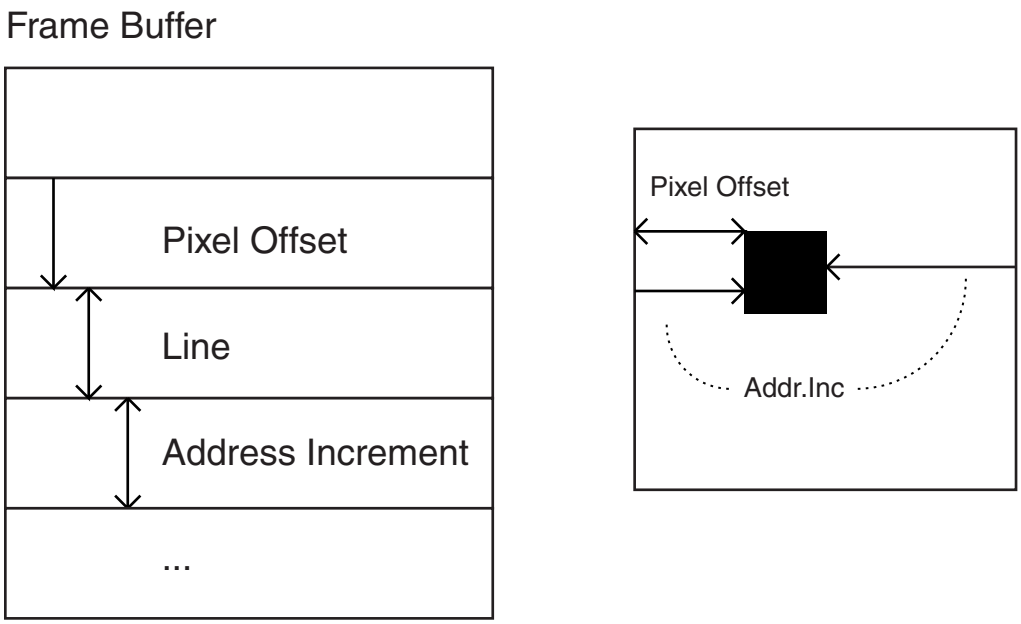
Once the host has updated the Frame Base Address Registers and the next DMA end of frame IRQ arrives, the backbuffer and the primary buffer are swapped and the host can work with the new backbuffer.

When using a dual-panel LCD module, both base address pointers should be updated in the same frame. In order to achieve this, the DMAUPDT bit in DMACON register must be used to validate the new base address.

35.10 2D Memory Addressing

The LCDC can be configured to work on a frame buffer larger than the actual screen size. By changing the values in a few registers, it is easy to move the displayed area along the frame buffer width and height.

Figure 35-13. .Frame Buffer Addressing



In order to locate the displayed window within a larger frame buffer, the software must:

- Program the DMABADDR1 (DMABADDR2) register(s) to make them point to the word containing the first pixel of the area of interest.
- Program the PIXELOFF field of DMA2DCFG register to specify the offset of this first pixel within the 32-bit memory word that contains it.
- Define the width of the complete frame buffer by programming in the field ADDRINC of DMA2DCFG register the address increment between the last word of a line and the first word of the next line (in number of 32-bit words).
- Enable the 2D addressing mode by writing the DMA2DEN bit in DMACON register. If this bit is not activated, the values in the DMA2DCFG register are not considered and the controller assumes that the displayed area occupies a continuous portion of the memory.

The above configuration can be changed frame to frame, so the displayed window can be moved rapidly. Note that the FRMSIZE field of DMAFRMCFG register must be updated with any movement of the displaying window. Note also that the software must write bit DMAUPDT in DMACON register after each configuration for it to be accepted by LCDC.

Note: In 24 bpp packed mode, the DMA base address must point to a word containing a complete pixel (possible values of PIXELOFF are 0 and 8). This means that the horizontal origin of the displaying window must be a multiple of 4 pixels or a multiple of 4 pixels minus 1 ($x = 4n$ or $x = 4n-1$, valid origins are pixel 0,3,4,7,8,11,12, etc.).

35.11 General-purpose Register

The LCD Controller has eight general-purpose output lines that are controlled by a general-purpose register (LCDGPR). The use of these lines is not fixed; they can be used in a wide range of applications. Some applications examples are:

- Palette swapping: In this application, the size of the palette memory is doubled. The two extra bits in the addresses (one extra bit in the low-priority address and one extra bit in the high-priority address) are connected to two general-purpose lines. One line is used to select the palette being updated through the HSB slave interface and the other line is used to select the working palette.
- Common intensity control in TFT mode: In this application, the most significant bit of each LCD component of the TFT interface is logically OR-ed with a general-purpose line. If the most significant bit of each color component in the palette is 0, the intensity can be controlled with the single general-purpose line.
- Control of signals of LCD modules not included in the LCD Interface, such as a standard/reverse scanning configuration pin, backlight on/off pin or user LEDs of the LCD module.

35.12 Register Configuration Examples

35.12.1 STN LCD Example

This example is for an STN color (RGB) 320*240 display, 8-bit single scan, running at 70 frames/s with a LCDC Core Clock of 60 MHz. First, the pixel rate required to drive the display should be determined by multiplying the total number of pixels on the display (320*240) by the frame rate:

Pixel rate: (320*240 pixels/frame)*(70 frames/s) = 5,376,000 pixels/s

Next, the bit rate required to drive the display should be determined. Since the display is STN color, each pixel consists of 3 bits (R,G,B), so the bit rate is just 3 times the pixel rate:

Bit rate: (5,376,000 pixels/s)*(3 bits/pixel) = 16,128,000 bits/s

Since the interface to the display is 8 bits wide, each PCLK cycle will transfer 8 bits to the display (neglecting front porch and back porch PCLK cycles which do not transfer data). Thus, the approximate PCLK frequency should be determined by dividing the bit rate by 8:

PCLK rate: (16,128,000 bits/s)/(8 bits/PCLKcycle) = 2,016,000 PCLKcycles/s = 2.016 MHz

Now that the desired PCLK rate is known, it is necessary to determine the value of the CLKVAL field in LCD Control Register 1 (LDCCON1) and write to this register:

CLKVAL = ((60 MHz)/(2*2.016 MHz)) - 1 = 14 (rounded to nearest integer)

LDCCON1 = CLKVAL << 12;

Note that because CLKVAL had to be rounded to the nearest integer, the actual PCLK rate will be (60 MHz)/((14+1)*2) = 2.000 MHz.

The next register that must be configured is LCD Control Register 2 (LDCCON2). This register contains eleven fields which should be configured as follows:

DISTYPE = 1; // Display Type: STN Color

SCANMOD = 0; // Scan Mode: Single Scan

IFWIDTH = 1; //Interface Width: 8-bit

PIXELSIZE = 3; // Pixel size: 8 bits per pixel

INVVD = 0; // LCDD polarity: Normal

INVFRAME = 0; //Vsync polarity: Normal

INVLINE = 0; //Hsync polarity: Normal

INVCLK = 0; //PCLK polarity: Normal

INVDVAL = 0; //Dval polarity: Normal

CLKMOD = 0; //PCLK mode: PCLK only active during active display period for STN display

MEMOR = 2; // Memory Ordering Format: Little Endian

LCDCON2 can then be written as follows:

LDCCON2 = (MEMOR<<30) | (CLKMOD<<15) | (INVDVAL<<12) | (INVCLK<<11) | (INVLINE<<10) | (INVFRAME<<9) | (INVVD << 8) | (PIXELSIZE<<5) | (IFWIDTH<<3) | (SCANMOD<<2) | (DISTYPE<<0);

For an STN display, all bits of the LCD Timing Configuration Register 1 must be written with 0:

LCDTIM1 = 0; // In STN mode, all bits must be zero

LCD Timing Configuration Register 2 contains 3 fields that control the horizontal back porch, sync pulse, and front porch widths. This example will assume that a sync pulse width of 1 PCLK cycle is desired and that front and back porch widths of 11 PCLK cycles are desired:

HBP = 11 - 1; // horizontal back porch of 11 PCLK cycles

HPW = 1 - 1; // horizontal pulse width of 1 PCLK cycle

HFP = 11 - 1; // horizontal front porch of 11 PCLK cycles

LCDTIM2 can then be written as follows:

LCDTIM2 = (HFP<<21) | (HPW<<8) | (HBP<<0);

The LCD Frame Configuration Register contains two fields, LINEVAL and HOZVAL. LINEVAL is computed by subtracting 1 from the vertical display size (in pixels):

LINEVAL = 240 - 1;

For an STN display, HOZVAL is determined by dividing the horizontal display size (in bits) by the number of data lines and then subtracting one. Because the STN display is color, the horizontal display size in bits is 3 times the horizontal display size in pixels:

HOZVAL= ((3*320)/8) - 1;

If the value calculated for HOZVAL is not an integer, it must be rounded up to the next integer value. LCDFRMCFG can then be written as follows:

LCDFRMCFG = (HOZVAL << 21) | (LINEVAL<<0);

The MODE Toggle Rate Value Register contains two fields, MVAL and MMODE, that determine the MODE toggle rate. For this example it will be assumed that the desired mode toggle rate is 5 line periods:

MVAL = 5 - 1;

MMODE = 1; // Allow MVAL to determine the toggle rate

LCDMVAL can then be written as follows:

LCDMVAL = (MMODE<<31) | (MVAL<<0);

Finally, the BRSTLEN (Burst Length) and FRMSIZE (Frame Size) fields of the DMA Frame Configuration Register must be determined. A desired burst length of 8 will be assumed:

BRSTLEN = 8 - 1;

The Frame Size is in units of 32-bit words, so it is determined by multiplying the number of pixels in the display by the number of bits used for representing a pixel in memory and then dividing by 32:

FRMSIZE = ((320*240)*8) / 32;

DMAFRMCFG can then be written as follows:

DMAFRMCFG = (BRSTLEN<<24) | (FRMSIZE<<0);

35.12.2 TFT LCD Example

This example is based on the NEC TFT color LCD module NL6448BC20-08. This module is a 640*480 display, 16-bit single scan, running at 60 frames/s. First, the pixel rate required to drive the display should be determined by multiplying the total number of pixels on the display (640*480) by the frame rate:

Pixel rate: (640*480 pixels/frame)*(60 frames/s) = 18,432,000 pixels/s

Next, the bit rate required to drive the display should be determined. Since the display is TFT color, each pixel consists of 16 bits (5 red bits, 5 green bits, 5 blue bits, and an intensity bit), so the bit rate is 16 times the pixel rate:

Bit rate: (18,432,000 pixels/s)*(16 bits/pixel) = 294,912,000 bits/s

Since the interface to the display is 16 bits wide, each PCLK cycle will transfer 16 bits to the display (neglecting front porch and back porch PCLK cycles which do not transfer data). Thus, the approximate PCLK frequency should be determined by dividing the bit rate by 16:

PCLK rate: (294,912,000 bits/s)/(16 bits/PCLKcycle) = 18,432,000 PCLKcycles/s = 18.432 MHz

Now that the desired PCLK rate is known, and assuming a LCDC Core Clock of 50 MHz, it is necessary to determine the value of the CLKVAL field in LCDCON1 and write to LDCCON1:

CLKVAL = ((50 MHz)/(2*18.432 MHz)) - 1 = 0 (rounded to nearest integer)

LDCCON1 = CLKVAL << 12;

Note that because it was necessary to round CLKVAL to the nearest integer, the actual PCLK rate will be (50 MHz)/((0+1)*2) = 25.000 MHz.

The next register that must be configured is LDCCON2. This register contains eleven fields which should be configured as follows:

DISTYPE = 2; // Display Type: TFT

SCANMOD = 0; // Scan Mode: Single Scan

IFWIDTH = 0; // Interface Width: 0 -- does not apply to TFT displays

PIXELSIZE = 4; // Pixel Size: 16 bits per pixel

INVVD = 0; // LCDD polarity: Normal

INVFRAME = 1; //Vsync polarity: Inverted

INVLINE = 1; //Hsync polarity: Inverted

INVCLK = 1; //PCLK polarity: Inverted

INVDVAL = 0; //Dval polarity: Normal

CLKMOD = 1; //PCLK mode: PCLK always active for TFT displays

MEMOR = 2; // Memory Ordering Format: Little Endian

LDCCON2 can then be written as follows:

LDCCON2 = (MEMOR<<30) | (CLKMOD<<15) | (INVDVAL<<12) | (INVCLK<<11) | (INVLINE<<10) | (INVFRAME<<9) | (INVVD << 8) | (PIXELSIZE<<5) | (IFWIDTH<<3) | (SCANMOD<<2) | (DISTYPE<<0);

LCDTIM1 contains four fields which determine the vertical front porch, back porch, and pulse width, as well as the vertical to horizontal delay. Assuming desired values for these four parameters of 12, 31, 2, and 2, respectively, these fields should be determined as follows:

VFP = (12); VBP = (31); VPW = (2 - 1); VHDLY= (2 - 1);

LCDTIM1 can then be written as follows:

LCDTIM1 = (VHDLY<<24) | (VPW<<16) | (VBP<<8) | (VFP<<0);

LCDTIM2 contains three fields which determine the horizontal front porch, pulse width, and back porch. Assuming desired values of 16, 96, and 48, respectively, these fields should be determined as follows:

HFP = (16 - 1); HPW= (96 - 1); HBP = (48 - 1);

However, there is a problem with the calculated value of HPW (95) because the width of the HPW field in LCDTIM2 is only 6 bits, which implies that the largest allowed value of HPW is 63. Fortunately, the horizontal pulse width value of 96 specified in the LCD module data sheet is just a typical value. The minimum allowed horizontal pulse width is specified as 10 in the LCD module data sheet, so HPW can be recomputed using a horizontal pulse width of 10:

HPW = (10 - 1);

LCDTIM2 can then be written:

LCDTIM2 = (HFP << 21) | (HPW<<8) | (HBP<<0);

The LCD Frame Configuration Register contains two fields, LINEVAL and HOZVAL. LINEVAL is computed by subtracting 1 from the vertical display size (in pixels):

LINEVAL = 480 - 1;

For a TFT display, HOZVAL is determined by subtracting 1 from the horizontal display size:

HOZVAL = 640 - 1;

LCDFRMCFG is then written as:

LCDFRMCFG = (HOZVAL<<21) | (LINEVAL<<0);

LCDMVAL determines the MODE toggle rate. For this display, MODE should toggle every frame, so all bits written to LCDMVAL should be zero:

LCDMVAL = 0; // MODE toggle each frame

Finally, the BRSTLEN (Burst Length) and FRMSIZE (Frame Size) fields of the DMA Frame Configuration Register must be determined. A desired burst length of 8 will be assumed:

BRSTLEN = 8 - 1;

The Frame Size is in units of 32-bit words, so it is determined by multiplying the number of pixels in the display by the number of bits used for representing a pixel in memory and then dividing by 32:

FRMSIZE = ((640*480)*16) / 32;

DMAFRMCFG can then be written as follows:

DMAFRMCFG = (BRSTLEN<<24) | (FRMSIZE<<0);

35.13 LCD Controller (LCDC) User Interface

Table 35-13. LCD Controller (LCDC) User Interface

Offset	Register	Register Name	Access	Reset Value
0x0	DMA Base Address Register 1	DMABADDR1	R/W	0x00000000
0x4	DMA Base Address Register 2	DMABADDR2	R/W	0x00000000
0x8	DMA Frame Pointer Register 1	DMAFRMPT1	Read-only	0x00000000
0xC	DMA Frame Pointer Register 2	DMAFRMPT2	Read-only	0x00000000
0x10	DMA Frame Address Register 1	DMAFRMADD1	Read-only	0x00000000
0x14	DMA Frame Address Register 2	DMAFRMADD2	Read-only	0x00000000
0x18	DMA Frame Configuration Register	DMAFRMCFG	R/W	0x00000000
0x1C	DMA Control Register	DMACON	R/W	0x00000000
0x20	DMA 2D Addressing Register	DMA2DCFG	R/W	0x00000000
0x800	LCD Control Register 1	LCDCON1	R/W	0x00002000
0x804	LCD Control Register 2	LCDCON2	R/W	0x00000000
0x808	LCD Timing Register 1	LCDTIM1	R/W	0x00000000
0x80C	LCD Timing Register 2	LCDTIM2	R/W	0x00000000
0x810	LCD Frame Configuration Register	LCDFRMCFG	R/W	0x00000000
0x814	LCD FIFO Register	LCDFIFO	R/W	0x00000000
0x818	MODE Toggle Rate Value Register	LCDMVAL	R/W	0x00000000
0x81C	Dithering Pattern DP1_2	DP1_2	R/W	0xA5
0x820	Dithering Pattern DP4_7	DP4_7	R/W	0x5AF0FA5
0x824	Dithering Pattern DP3_5	DP3_5	R/W	0xA5A5F
0x828	Dithering Pattern DP2_3	DP2_3	R/W	0xA5F
0x82C	Dithering Pattern DP5_7	DP5_7	R/W	0xFAF5FA5
0x830	Dithering Pattern DP3_4	DP3_4	R/W	0xFAF5
0x834	Dithering Pattern DP4_5	DP4_5	R/W	0xFAF5F
0x838	Dithering Pattern DP6_7	DP6_7	R/W	0xF5FFAFF
0x83C	Power Control Register	PWRCON	R/W	0x0000000e
0x840	Contrast Control Register	CONTRAST_CTR	R/W	0x00000000
0x844	Contrast Value Register	CONTRAST_VAL	R/W	0x00000000
0x848	LCD Interrupt Enable Register	IER	Write-only	0x0
0x84C	LCD Interrupt Disable Register	IDR	Write-only	0x0
0x850	LCD Interrupt Mask Register	IMR	Read-only	0x0
0x854	LCD Interrupt Status Register	ISR	Read-only	0x0
0x858	LCD Interrupt Clear Register	ICR	Write-only	0x0
0x85C	LCD General-purpose Register	GPR	R/W	0x0
0x860	LCD Interrupt Test Register	ITR	Write-only	0
0x864	LCD Interrupt Raw Status Register	IRR	Read-only	0

Table 35-13. LCD Controller (LCDC) User Interface (Continued)

Offset	Register	Register Name	Access	Reset Value
0xC00	Palette entry 0	LUT ENTRY 0	R/W	
0xC04	Palette entry 1	LUT ENTRY 1	R/W	
0xC08	Palette entry 2	LUT ENTRY 2	R/W	
0xC0C	Palette entry 3	LUT ENTRY 3	R/W	
…		…		
0xFFC	Palette entry 255	LUT ENTRY 255	R/W	

35.13.1 DMA Base Address Register 1

Name: DMABADDR1

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
BADDR-U							
23	22	21	20	19	18	17	16
BADDR-U							
15	14	13	12	11	10	9	8
BADDR-U							
7	6	5	4	3	2	1	0
BADDR-U							

- **BADDR-U**

Base Address for the upper panel in dual scan mode. Base Address for the complete frame in single scan mode.

If a dual scan configuration is selected in LCDCON2 register or bit DMA2DEN in register DMACON is set, the bit DMAUPDT in that same register must be written after writing any new value to this field in order to make the DMA controller use this new value.

Note: DMA Base Address is aligned as word address. This means the last two bits of this register value are always zero.

35.13.2 DMA Base Address Register 2

Name: DMABADDR2

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
BADDR-L							
23	22	21	20	19	18	17	16
BADDR-L							
15	14	13	12	11	10	9	8
BADDR-L							
7	6	5	4	3	2	1	0
BADDR-L							

- **BADDR-L**

Base Address for the lower panel in dual scan mode only.

If a dual scan configuration is selected in LCDCON2 register or bit DMA2DEN in register DMACON is set, the bit DMAUPDT in that same register must be written after writing any new value to this field in order to make the DMA controller use this new value.

Note: DMA Base Address is aligned as word address. This means the last two bits of this register value are always zero.

35.13.3 DMA Frame Pointer Register 1

Name: DMAFRMPT1

Access: Read-only

Reset value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	FRMPT-U						
15	14	13	12	11	10	9	8
FRMPT-U							
7	6	5	4	3	2	1	0
FRMPT-U							

- **FRMPT-U**

Current value of frame pointer for the upper panel in dual scan mode. Current value of frame pointer for the complete frame in single scan mode. Down count from FRMSIZE to 0.

Note: This register is read-only and contains the current value of the frame pointer (number of words to the end of the frame). It can be used as an estimation of the number of words transferred from memory for the current frame.

35.13.4 DMA Frame Pointer Register 2

Name: DMAFRMPT2

Access: Read-only

Reset value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	FRMPT-L					
15	14	13	12	11	10	9	8
FRMPT-L							
7	6	5	4	3	2	1	0
FRMPT-L							

- **FRMPT-L**

Current value of frame pointer for the Lower panel in dual scan mode only. Down count from FRMSIZE to 0.

Note: This register is read-only and contains the current value of the frame pointer (number of words to the end of the frame). It can be used as an estimation of the number of words transferred from memory for the current frame.

35.13.5 DMA Frame Address Register 1

Name: DMAFRMADD1

Access: Read-only

Reset value: 0x00000000

31	30	29	28	27	26	25	24
FRMADD-U							
23	22	21	20	19	18	17	16
FRMADD-U							
15	14	13	12	11	10	9	8
FRMADD-U							
7	6	5	4	3	2	1	0
FRMADD-U							

- **FRMADD-U**

Current value of frame address for the upper panel in dual scan mode. Current value of frame address for the complete frame in single scan.

Note: This register is read-only and contains the current value of the last DMA transaction in the bus for the panel/frame.

Note: DMA Frame Address is aligned as word address. This means the last two bits of this register value are always zero.

35.13.6 DMA Frame Address Register 2

Name: DMAFRMADD2

Access: Read-only

Reset value: 0x00000000

31	30	29	28	27	26	25	24
FRMADD-L							
23	22	21	20	19	18	17	16
FRMADD-L							
15	14	13	12	11	10	9	8
FRMADD-L							
7	6	5	4	3	2	1	0
FRMADD-L							

- **FRMADD-L**

Current value of frame address for the lower panel in dual scan mode only.

Note: This register is read-only and contains the current value of the last DMA transaction in the bus for the panel.

Note: DMA Frame Address is aligned as word address. This means the last two bits of this register value are always zero

35.13.7 DMA Frame Configuration Register

Name: DMAFRMCFG

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	BRSTLEN			
23	22	21	20	19	18	17	16
-	FRMSIZE						
15	14	13	12	11	10	9	8
FRMSIZE							
7	6	5	4	3	2	1	0
FRMSIZE							

- **FRMSIZE: Frame Size**

In single scan mode, this is the frame size in words. In dual scan mode, this is the size of each panel.

If a dual scan configuration is selected in LCDCON2 register or bit DMA2DEN in register DMACON is set, the bit DMAUPDT in that same register must be written after writing any new value to this field in order to make the DMA controller use this new value.

- **BRSTLEN: Burst Length**

Program with the desired burst length - 1

35.13.8 DMA Control Register

Name: DMACON

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
			DMA2DEN	DMAUPDT	DMABUSY	DMARST	DMAEN

- **DMAEN: DMA Enable**

0: DMA is disabled.

1: DMA is enabled.

- **DMARST: DMA Reset (Write-only)**

0: No effect.

1: Reset DMA module. DMA Module should be reset only when disabled and in idle state.

- **DMABUSY: DMA Busy**

0: DMA module is idle.

1: DMA module is busy (doing a transaction on the HSB bus).

- **DMAUPDT: DMA Configuration Update**

0: No effect

1: Update DMA Configuration. Used for simultaneous updating of DMA parameters in dual scan mode or when using 2D addressing. The values written in the registers DMABADDR1, DMABADDR2 and DMA2DCFG, and in the field FRMSIZE of register DMAFRMCFG, are accepted by the DMA controller and are applied at the next frame. This bit is used only if a dual scan configuration is selected (bit SCANMOD of LCDCON2 register) or 2D addressing is enabled (bit DMA2DEN in this register). Otherwise, the LCD controller accepts immediately the values written in the registers referred to above.

- **DMA2DEN: DMA 2D Addressing Enable**

0: 2D addressing is disabled (values in register DMA2DCFG are “don’t care”).

1: 2D addressing is enabled.

35.13.9 LCD DMA 2D Addressing Register

Name: DMA2DCFG

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
			PIXELOFF				
23	22	21	20	19	18	17	16
-							
15	14	13	12	11	10	9	8
ADDRINC							
7	6	5	4	3	2	1	0
ADDRINC							

- **ADDRINC: DMA 2D Addressing Increment**

When 2-D DMA addressing is enabled (bit DMA2DEN is set in register DMACON), this field specifies the number of bytes that the DMA controller must jump between screen lines. It must be programmed as: [({address of first 32-bit word in a screen line} - {address of last 32-bit word in previous line})]. In other words, it is equal to 4*[number of 32-bit words occupied by each line in the complete frame buffer minus the number of 32-bit words occupied by each displayed line]. Bit DMAUPDT in register DMACON must be written after writing any new value to this field in order to make the DMA controller use this new value.

- **PIXELOFF: DAM2D Addressing Pixel offset**

When 2D DMA addressing is enabled (bit DMA2DEN is set in register DMACON), this field specifies the offset of the first pixel in each line within the memory word that contains this pixel. The offset is specified in number of bits in the range 0-31, so for example a value of 4 indicates that the first pixel in the screen starts at bit 4 of the 32-bit word pointed by register DMABADDR1. Bits 0 to 3 of that word are not used. This example is valid for little endian memory organization. When using big endian memory organization, this offset is considered from bit 31 downwards, or equivalently, a given value of this field always selects the pixel in the same relative position within the word, independently of the memory ordering configuration. Bit DMAUPDT in register DMACON must be written after writing any new value to this field in order to make the DMA controller use this new value.

35.13.10 LCD Control Register 1

Name: LCDCON1

Access: Read/Write, except LINECNT: Read-only

Reset value: 0x00002000

31	30	29	28	27	26	25	24
LINECNT							
23	22	21	20	19	18	17	16
LINECNT			CLKVAL				
15	14	13	12	11	10	9	8
CLKVAL				-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	BYPASS

- **BYPASS: Bypass PCLK divider**

0: The divider is not bypassed. PCLK frequency defined by the CLKVAL field.

1: The PCLK divider is bypassed. PCLK frequency is equal to the LCDC Core Clock frequency.

- **CLKVAL: Clock divider**

9-bit divider for pixel clock (PCLK) frequency.

$$Pixel_clock = LCDC_Core_Clock / ((CLKVAL + 1) \times 2)$$

- **LINECNT: Line Counter (Read-only)**

Current value of 11-bit line counter. Down count from LINEVAL to 0.

35.13.11 LCD Control Register 2

Name: LCDCON2

Access: Read/Write

Reset value: 0x0000000

31	30	29	28	27	26	25	24
MEMOR		-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
CLKMOD	-	-	INVDVAL	INVCLK	INVLINE	INVFRAME	INVVD
7	6	5	4	3	2	1	0
PIXELSIZE			IFWIDTH		SCANMOD	DISTYPE	

- **DISTYPE: Display Type**

DISTYPE		
0	0	STN Monochrome
0	1	STN Color
1	0	TFT
1	1	Reserved

- **SCANMOD: Scan Mode**

0: Single Scan

1: Dual Scan

- **IFWIDTH: Interface width (STN)**

IFWIDTH		
0	0	4-bit (Only valid in single scan STN mono or color)
0	1	8-bit (Only valid in STN mono or Color)
1	0	16-bit (Only valid in dual scan STN mono or color)
1	1	Reserved

- **PIXELSIZE: Bits per pixel**

PIXELSIZE			
0	0	0	1 bit per pixel
0	0	1	2 bits per pixel
0	1	0	4 bits per pixel
0	1	1	8 bits per pixel
1	0	0	16 bits per pixel
1	0	1	24 bits per pixel packed (Only valid in TFT mode)
1	1	0	24 bits per pixel unpacked (Only valid in TFT mode)
1	1	1	Reserved

- **INVVD: LCDD polarity**

0: Normal

1: Inverted

- **INVFRAME: vsync polarity**

0: Normal (active high)

1: Inverted (active low)

- **INVLINE: hsync polarity**

0: Normal (active high)

1: Inverted (active low)

- **INVCLK: PCLK polarity**

0: Normal (LCDD fetched at PCLK falling edge)

1: Inverted (LCDD fetched at PCLK rising edge)

- **INVDVAL: dval polarity**

0: Normal (active high)

1: Inverted (active low)

- **CLKMOD: PCLK mode**

0: PCLK only active during active display period

1: PCLK always active

- **MEMOR: Memory Ordering Format**

00: Big Endian

10: Little Endian

11: WinCE format

35.13.12 LCD Timing Configuration Register 1

Name: LCDTIM1

Access: Read/Write

Reset value: 0x0000000

31	30	29	28	27	26	25	24
-	-	-	-	VHDLY			
23	22	21	20	19	18	17	16
-	-	VPW					
15	14	13	12	11	10	9	8
VBP							
7	6	5	4	3	2	1	0
VFP							

- **VFP: Vertical Front Porch**

In TFT mode, these bits equal the number of idle lines at the end of the frame.

In STN mode, these bits should be set to 0.

- **VBP: Vertical Back Porch**

In TFT mode, these bits equal the number of idle lines at the beginning of the frame.

In STN mode, these bits should be set to 0.

- **VPW: Vertical Synchronization pulse width**

In TFT mode, these bits determine the vertical synchronization pulse width. VSYNC width is equal to (VPW+1) lines.

In STN mode, these bits should be set to 0.

- **VHDLY: Vertical to horizontal delay**

In TFT mode, this value determines the delay between VSYNC rising or falling edge and HSYNC rising edge. Delay is (VHDLY+1) PCLK cycles.

In STN mode, these bits should be set to 0.

35.13.13 LCD Timing Configuration Register 2

Name: LCDTIM2

Access: Read/Write

Reset value: 0x0000000

31	30	29	28	27	26	25	24
HFP							
23	22	21	20	19	18	17	16
HFP			-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	HPW					
7	6	5	4	3	2	1	0
HBP							

- **HBP: Horizontal Back Porch**

Determines the number of idle PCLK cycles at the beginning of the line. Idle period is (HBP+1) PCLK cycles.

- **HPW: Horizontal synchronization pulse width**

Determines the width of the HSYNC pulse, given in PCLK cycles. Width is (HPW+1) PCLK cycles.

- **HFP: Horizontal Front Porch**

Determines the number of idle PCLK cycles at the end of the line. Idle period is (HFP+1) PCLK cycles.

35.13.14 LCD Frame Configuration Register

Name: LCDFRMCFG

Access: Read/Write

Reset value: 0x0000000

31	30	29	28	27	26	25	24
HOZVAL							
23	22	21	20	19	18	17	16
HOZVAL			-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	LINEVAL		
7	6	5	4	3	2	1	0
LINEVAL							

- **LINEVAL: Vertical size of LCD module**

LINEVAL = (Vertical display size) - 1

In dual scan mode, vertical display size refers to the size of each panel.

- **HOZVAL: Horizontal size of LCD module**

In STN Mode:

  – HOZVAL = (Horizontal display size)/ Number of valid LCDD data line) - 1
  – In STN monochrome mode, Horizontal display size = Number of horizontal pixels
  – In STN color mode, Horizontal display size = 3*Number of horizontal pixels
  – In 4-bit single scan or 8-bit dual scan STN display mode, number of valid LCDD data lines = 4
  – In 8-bit single scan or 16-bit dual scan STN display mode, number of valid LCDD data lines = 8
  – If the value calculated for HOZVAL with the above formula is not an integer, it must be rounded up to the next integer value.

In TFT mode:

  – HOZVAL = Horizontal display size - 1

35.13.15 LCD FIFO Register

Name: LCDFIFO

Access: Read/Write

Reset value: 0x0000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
FIFOTH							
7	6	5	4	3	2	1	0
FIFOTH							

- **FIFOTH: FIFO Threshold**

Must be programmed with:

$$FIFOTH = LCD_FIFO_SIZE - (2 \times DMA_burst_length + 3)$$

where:

- LCD_FIFO_SIZE is the effective size of the FIFO. It is the total FIFO memory size in single scan mode and half that size in dual scan mode.
- DMA_burst_length is the burst length of the transfers made by the DMA.

35.13.16 MODE Toggle Rate Value Register

Name: LCDMVAL

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
MMODE	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
MVAL							

- **MVAL: MODE toggle rate value**

MODE toggle rate if MMODE = 1. Toggle rate is MVAL + 1 line periods.

- **MMODE: MODE toggle rate select**

0: Each Frame

1: Rate defined by MVAL

35.13.17 Dithering Pattern DP1_2 Register

Name: DP1_2

Access: Read/Write

Reset value: 0xA5

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
DP1_2							

- **DP1_2: Pattern value for ½ duty cycle**

35.13.18 Dithering Pattern DP4_7 Register

Name: DP4_7

Access: Read/Write

Reset value: 0x5AF0FA5

31	30	29	28	27	26	25	24
-	-	-	-	DP4_7			
23	22	21	20	19	18	17	16
DP4_7							
15	14	13	12	11	10	9	8
DP4_7							
7	6	5	4	3	2	1	0
DP4_7							

- **DP4_7: Pattern value for 4/7 duty cycle**

35.13.19 Dithering Pattern DP3_5 Register

Name: DP3_5

Access: Read/Write

Reset value: 0xA5A5F

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	DP3_5			
15	14	13	12	11	10	9	8
DP3_5							
7	6	5	4	3	2	1	0
DP3_5							

- **DP3_5: Pattern value for 3/5 duty cycle**

35.13.20 Dithering Pattern DP2_3 Register

Name: DP2_3: Dithering Pattern DP2_3 Register

Access: Read/Write

Reset value: 0xA5F

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	DP2_3			
7	6	5	4	3	2	1	0
DP2_3							

- **DP2_3: Pattern value for 2/3 duty cycle**

35.13.21 Dithering Pattern DP5_7 Register

Name: DP5_7:

Access: Read/Write

Reset value: 0xFAF5FA5

31	30	29	28	27	26	25	24
-	-	-	-	DP5_7			
23	22	21	20	19	18	17	16
DP5_7							
15	14	13	12	11	10	9	8
DP5_7							
7	6	5	4	3	2	1	0
DP5_7							

- **DP5_7: Pattern value for 5/7 duty cycle**

35.13.22 Dithering Pattern DP3_4 Register

Name: DP3_4

Access: Read/Write

Reset value: 0xFAF5

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
DP3_4							
7	6	5	4	3	2	1	0
DP3_4							

- **DP3_4: Pattern value for 3/4 duty cycle**

35.13.23 Dithering Pattern DP4_5 Register

Name: DP4_5

Access: Read/Write

Reset value: 0xFAF5F

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	DP4_5			
15	14	13	12	11	10	9	8
DP4_5							
7	6	5	4	3	2	1	0
DP4_5							

- **DP4_5: Pattern value for 4/5 duty cycle**

35.13.24 Dithering Pattern DP6_7 Register

Name: DP6_7

Access: Read/Write

Reset value: 0xF5FFAFF

31	30	29	28	27	26	25	24
-	-	-	-	DP6_7			
23	22	21	20	19	18	17	16
DP6_7							
15	14	13	12	11	10	9	8
DP6_7							
7	6	5	4	3	2	1	0
DP6_7							

- **DP6_7: Pattern value for 6/7 duty cycle**

35.13.25 Power Control Register

Name: PWRCON

Access: Read/Write

Reset value: 0x0000000e

31	30	29	28	27	26	25	24
BUSY	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
GUARD_TIME							PWR

- **PWR: LCD module power control**

0 = pwr pin is low, other * pins are low.

0->1 = * pins activated, pwr are set high with the delay of GUARD_TIME frame periods.

1 = pwr pin is high, other * pins are active

1->0 = pwr pin is low, other * pins are active, but are set low after GUARD_TIME frame periods.

- **GUARD_TIME**

Delay in frame periods between applying control signals to the LCD module and setting PWR high, and between setting PWR low and removing control signals from LCD module

- **BUSY**

Read-only field. If 1, it indicates that the LCD is busy (active and displaying data, in power on sequence or in power off sequence).

35.13.26 Contrast Control Register

Name: CONTRAST_CTR

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	ENA	POL	PS	

- **PS**

This 2-bit value selects the configuration of a counter prescaler. The meaning of each combination is as follows:

PS		
0	0	The counter advances at a rate of fCOUNTER = fLCDC_CLOCK.
0	1	The counter advances at a rate of fCOUNTER = fLCDC_CLOCK/2.
1	0	The counter advances at a rate of fCOUNTER = fLCDC_CLOCK/4.
1	1	The counter advances at a rate of fCOUNTER = fLCDC_CLOCK/8.

- **POL**

This bit defines the polarity of the output. If 1, the output pulses are high level (the output will be high whenever the value in the counter is less than the value in the compare register CONTRAST_VAL). If 0, the output pulses are low level.

- **ENA**

When 1, this bit enables the operation of the PWM generator. When 0, the PWM counter is stopped.

35.13.27 Contrast Value Register

Name: CONTRAST_VAL

Access: Read/Write

Reset value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
CVAL							

- **CVAL**

PWM compare value. Used to adjust the analog value obtained after an external filter to control the contrast of the display.

35.13.28 LCD Interrupt Enable Register

Name: IER

Access: Write-only

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MERIE	OWRIE	UFLWIE	-	EOFIE	LSTLNIE	LNIE

- **LNIE: Line interrupt enable**

0: No effect

1: Enable each line interrupt

- **LSTLNIE: Last line interrupt enable**

0: No effect

1: Enable last line interrupt

- **EOFIE: DMA End of frame interrupt enable**

0: No effect

1: Enable End Of Frame interrupt

- **UFLWIE: FIFO underflow interrupt enable**

0: No effect

1: Enable FIFO underflow interrupt

- **OWRIE: FIFO overwrite interrupt enable**

0: No effect

1: Enable FIFO overwrite interrupt

- **MERIE: DMA memory error interrupt enable**

0: No effect

1: Enable DMA memory error interrupt

35.13.29 LCD Interrupt Disable Register

Name: IDR

Access: Write-only

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MERID	OWRID	UFLWID	-	EOFID	LSTLNID	LNID

- **LNID: Line interrupt disable**

0: No effect

1: Disable each line interrupt

- **LSTLNID: Last line interrupt disable**

0: No effect

1: Disable last line interrupt

- **EOFID: DMA End of frame interrupt disable**

0: No effect

1: Disable End Of Frame interrupt

- **UFLWID: FIFO underflow interrupt disable**

0: No effect

1: Disable FIFO underflow interrupt

- **OWRID: FIFO overwrite interrupt disable**

0: No effect

1: Disable FIFO overwrite interrupt

- **MERID: DMA Memory error interrupt disable**

0: No effect

1: Disable DMA Memory error interrupt

35.13.30 LCD Interrupt Mask Register

Name: IMR

Access: Read-only

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MERIM	OWRIM	UFLWIM	-	EOFIM	LSTLNIM	LNIM

- **LNIM: Line interrupt mask**

0: Line Interrupt disabled

1: Line interrupt enabled

- **LSTLNIM: Last line interrupt mask**

0: Last Line Interrupt disabled

1: Last Line Interrupt enabled

- **EOFIM: DMA End of frame interrupt mask**

0: End Of Frame interrupt disabled

1: End Of Frame interrupt enabled

- **UFLWIM: FIFO underflow interrupt mask**

0: FIFO underflow interrupt disabled

1: FIFO underflow interrupt enabled

- **OWRIM: FIFO overwrite interrupt mask**

0: FIFO overwrite interrupt disabled

1: FIFO overwrite interrupt enabled

- **MERIM: DMA Memory error interrupt mask**

0: DMA Memory error interrupt disabled

1: DMA Memory error interrupt enabled

35.13.31 LCD Interrupt Status Register

Name: ISR

Access: Read-only

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MERIS	OWRIS	UFLWIS	-	EOFIS	LSTLNIS	LNIS

- **LNIS: Line interrupt status**

0: Line Interrupt not active

1: Line Interrupt active

- **LSTLNIS: Last line interrupt status**

0: Last Line Interrupt not active

1: Last Line Interrupt active

- **EOFIS: DMA End of frame interrupt status**

0: End Of Frame interrupt not active

1: End Of Frame interrupt active

- **UFLWIS: FIFO underflow interrupt status**

0: FIFO underflow interrupt not active

1: FIFO underflow interrupt active

- **OWRIS: FIFO overwrite interrupt status**

0: FIFO overwrite interrupt not active

1: FIFO overwrite interrupt active

- **MERIS: DMA Memory error interrupt status**

0: DMA Memory error interrupt not active

1: DMA Memory error interrupt active

35.13.32 LCD Interrupt Clear Register

Name: ICR

Access: Write-only

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MERIC	OWRIC	UFLWIC	-	EOFIC	LSTLNIC	LNIC

- **LNIC: Line interrupt clear**

0: No effect

1: Clear each line interrupt

- **LSTLNIC: Last line interrupt clear**

0: No effect

1: Clear Last line Interrupt

- **EOFIC: DMA End of frame interrupt clear**

0: No effect

1: Clear End Of Frame interrupt

- **UFLWIC: FIFO underflow interrupt clear**

0: No effect

1: Clear FIFO underflow interrupt

- **OWRIC: FIFO overwrite interrupt clear**

0: No effect

1: Clear FIFO overwrite interrupt

- **MERIC: DMA Memory error interrupt clear**

0: No effect

1: Clear DMA Memory error interrupt

35.13.33 LCD General-purpose Register

Name: GPR

Access: Read/Write

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
GPRB7	GPRB6	GPRB5	GPRB4	GPRB3	GPRB2	GPRB1	GPRB0

- **GPRBx: General-purpose bit**

Controls the general-purpose line x.

35.13.34 LCD Interrupt Test Register

Name: ITR

Access: Write-only

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MERIT	OWRIT	UFLWIT	-	EOFIT	LSTLNIT	LNIT

- **LNIT: Line interrupt test**

0: No effect

1: Set each line interrupt

- **LSTLNIT: Last line interrupt test**

0: No effect

1: Set Last line interrupt

- **EOFIT: DMA End of frame interrupt test**

0: No effect

1: Set End Of Frame interrupt

- **UFLWIT: FIFO underflow interrupt test**

0: No effect

1: Set FIFO underflow interrupt

- **OWRIT: FIFO overwrite interrupt test**

0: No effect

1: Set FIFO overwrite interrupt

- **MERIT: DMA Memory error interrupt test**

0: No effect

1: Set DMA Memory error interrupt

35.13.35 LCD Interrupt Raw Status Register

Name: IRR

Access: Write-only

Reset value: 0x0

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	MERIR	OWRIR	UFLWIR	-	EOFIR	LSTLNIR	LNIR

- **LNIR: Line interrupt raw status**

0: No effect

1: Line interrupt condition present

- **LSTLNIR: Last line interrupt raw status**

0: No effect

1: Last line Interrupt condition present

- **EOFIR: DMA End of frame interrupt raw status**

0: No effect

1: End Of Frame interrupt condition present

- **UFLWIR: FIFO underflow interrupt raw status**

0: No effect

1: FIFO underflow interrupt condition present

- **OWRIR: FIFO overwrite interrupt raw status**

0: No effect

1: FIFO overwrite interrupt condition present

- **MERIR: DMA Memory error interrupt raw status**

0: No effect

1: DMA Memory error interrupt condition present

36. Image Sensor Interface (ISI)

Rev: 0.0.5.2

36.1 Features

- **ITU-R BT. 601/656 8-bit Mode External Interface Support**
- **Supports up to 12-bit Grayscale CMOS Sensors**
- **Support for ITU-R BT.656-4 SAV and EAV Synchronization**
- **Vertical and Horizontal Resolutions up to 2048 x 2048**
- **Preview Path up to 640*480**
- **128 Bytes FIFO on Codec Path**
- **128 Bytes FIFO on Preview Path**
- **Support for Packed Data Formatting for YCbCr 4:2:2 Formats**
- **Preview Scaler to Generate Smaller Size image**
- **Programmable Frame Capture Rate**
- **VGA, QVGA, CIF, QCIF supported for LCD Preview**
- **Custom Formats with Horizontal and Vertical Preview Size as Multiples of 16 Also Supported for LCD Preview**

36.2 Overview

The Image Sensor Interface (ISI) connects a CMOS-type image sensor to the processor and provides image capture in various formats. It does data conversion, if necessary, before the storage in memory through DMA.

The ISI supports color CMOS image sensor and grayscale image sensors with a reduced set of functionalities.

In grayscale mode, the data stream is stored in memory without any processing and so is not compatible with the LCD controller.

Internal FIFOs on the preview and codec paths are used to store the incoming data. The RGB output on the preview path is compatible with the LCD controller. This module outputs the data in RGB format (LCD compatible) and has scaling capabilities to make it compliant to the LCD display resolution (See Table 36-3 on page 876).

Several input formats such as preprocessed RGB or YCbCr are supported through the data bus interface.

It supports two modes of synchronization:

1. The hardware with VSYNC and HSYNC signals
2. The International Telecommunication Union Recommendation *ITU-R BT.656-4* Start-of-Active-Video (SAV) and End-of-Active-Video (EAV) synchronization sequence.

Using EAV/SAV for synchronization reduces the pin count (VSYNC, HSYNC not used). The polarity of the synchronization pulse is programmable to comply with the sensor signals.

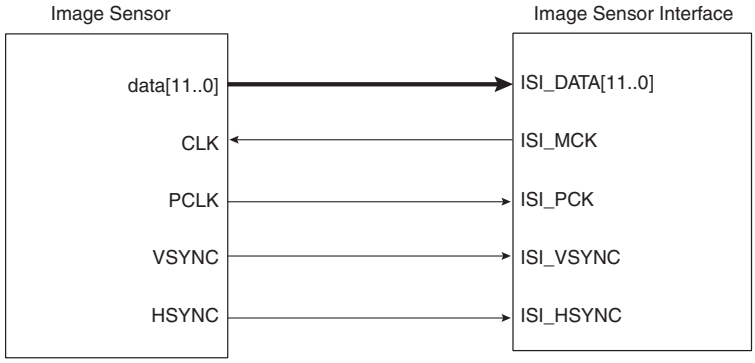
Table 36-1. I/O Description

Signal	Dir	Description
VSYNC	IN	Vertical Synchronization
HSYNC	IN	Horizontal Synchronization

Table 36-1. I/O Description

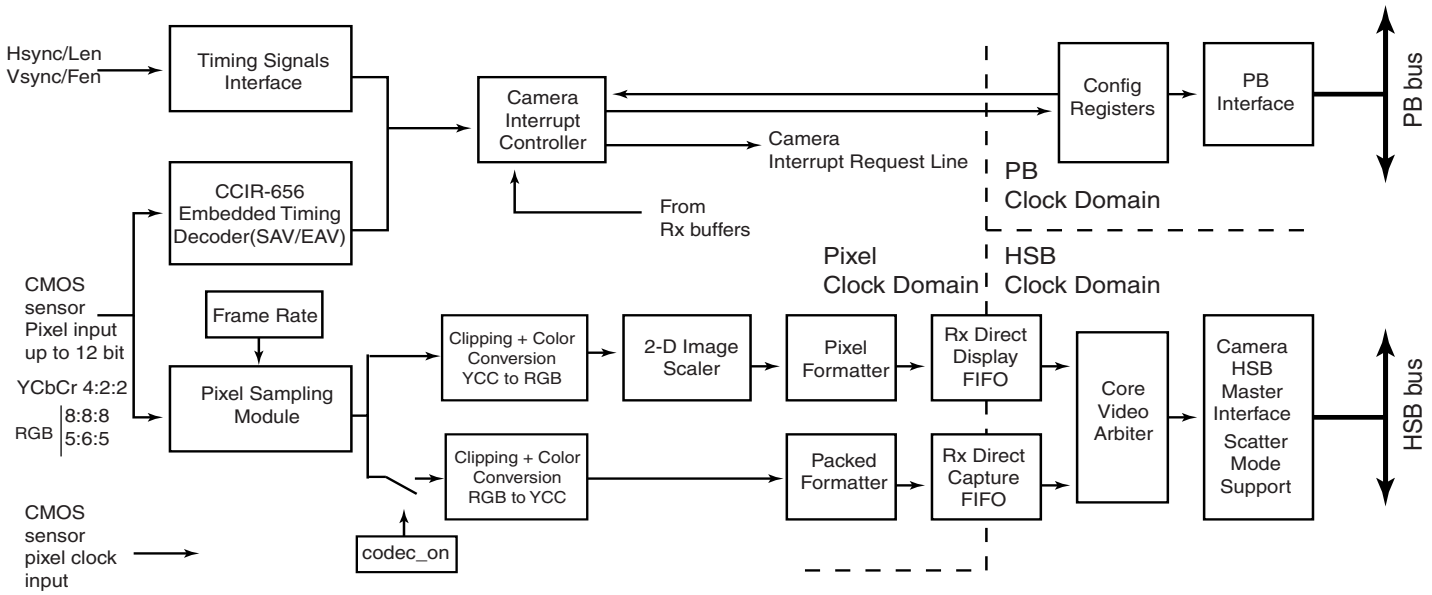
DATA[11..0]	IN	Sensor Pixel Data
MCK	OUT	Master Clock Provided to the Image Sensor
PCK	IN	Pixel Clock Provided by the Image Sensor

Figure 36-1. ISI Connection Example



36.3 Block Diagram

Figure 36-2. Image Sensor Interface Block Diagram



36.4 Product Dependencies

36.4.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the ISI pins to their peripheral functions.

36.4.2 Power Management

The ISI clock is generated by the Power Manager. Before using the ISI, the programmer must ensure that the ISIclock is enabled in the Power Manager.

In the ISI description, Master Clock (MCK) is the clock of the peripheral bus to which the ISI is connected.

To prevent bus errors the ISI operation must be terminated before entering sleep mode

36.4.3 Interrupt

The ISI interface has an interrupt line connected to the Interrupt Controller. Handling the ISI interrupt requires programming the interrupt controller before configuring the ISI.

36.5 Functional Description

The Image Sensor Interface (ISI) supports direct connection to the International Telecommunication Union Recommendation ITU-R BT. 601/656 8-bit mode compliant sensors and up to 12-bit grayscale sensors. It receives the image data stream from the image sensor on the 12-bit data bus.

This module receives up to 12 bits for data, the horizontal and vertical synchronizations and the pixel clock. The reduced pin count alternative for synchronization is supported for sensors that embed SAV (start of active video) and EAV (end of active video) delimiters in the data stream.

The Image Sensor Interface interrupt line is generally connected to the Interrupt Controller and can trigger an interrupt at the beginning of each frame and at the end of a DMA frame transfer. If the SAV/EAV synchronization is used, an interrupt can be triggered on each delimiter event.

For 8-bit color sensors, the data stream received can be in several possible formats: YCbCr 4:2:2, RGB 8:8:8, RGB 5:6:5 and may be processed before the storage in memory. The data stream may be sent on both preview path and codec path if the bit CODEC_ON in the CR1 is one. To optimize the bandwidth, the codec path should be enabled only when a capture is required.

In grayscale mode, the input data stream is stored in memory without any processing. The 12-bit data, which represent the grayscale level for the pixel, is stored in memory one or two pixels per word, depending on the GS_MODE bit in the CR2 register. The codec datapath is not available when grayscale image is selected.

A frame rate counter allows users to capture all frames or 1 out of every 2 to 8 frames.

36.5.1 Data Timing

The two data timings using horizontal and vertical synchronization and EAV/SAV sequence synchronization are shown in Figure 36-3 and Figure 36-4.

In the VSYNC/HSYNC synchronization, the valid data is captured with the active edge of the pixel clock (PCK), after SFD lines of vertical blanking and SLD pixel clock periods delay programmed in the control register.

The ITU-RBT.656-4 defines the functional timing for an 8-bit wide interface.

There are two timing reference signals, one at the beginning of each video data block SAV (0xFF000080) and one at the end of each video data block EAV(0xFF00009D). Only data sent between EAV and SAV is captured. Horizontal blanking and vertical blanking are ignored. Use of the SAV and EAV synchronization eliminates the VSYNC and HSYNC signals from the inter-

face, thereby reducing the pin count. In order to retrieve both frame and line synchronization properly, at least one line of vertical blanking is mandatory.

Figure 36-3. HSYNC and VSYNC Synchronization

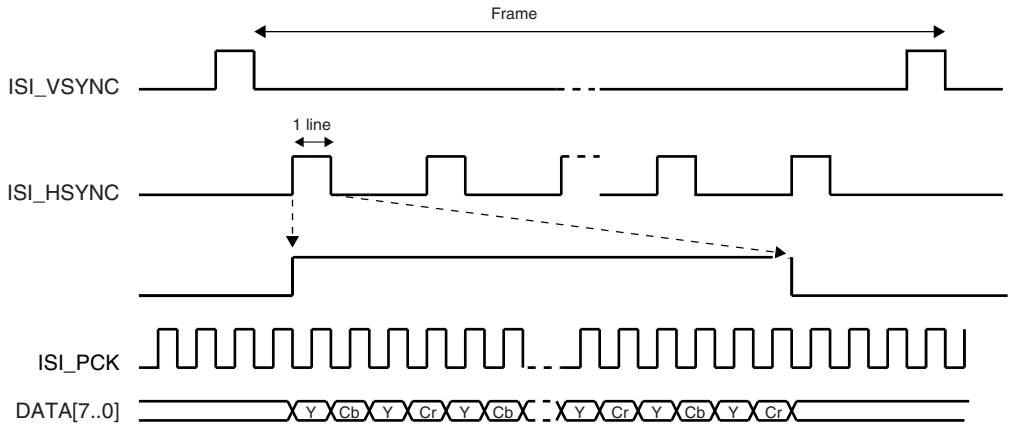
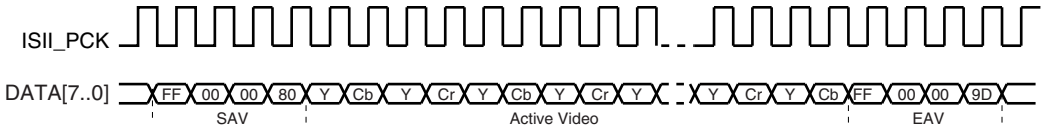


Figure 36-4. SAV and EAV Sequence Synchronization



36.5.2 Data Ordering

The RGB color space format is required for viewing images on a display screen preview, and the YCbCr color space format is required for encoding.

All the sensors do not output the YCbCr or RGB components in the same order. The ISI allows the user to program the same component order as the sensor, reducing software treatments to restore the right format.

Table 36-2. Data Ordering in YCbCr Mode

Mode	Byte 0	Byte 1	Byte 2	Byte 3
Default	Cb(i)	Y(i)	Cr(i)	Y(i+1)
Mode1	Cr(i)	Y(i)	Cb(i)	Y(i+1)
Mode2	Y(i)	Cb(i)	Y(i+1)	Cr(i)
Mode3	Y(i)	Cr(i)	Y(i+1)	Cb(i)

Table 36-3. RGB Format in Default Mode, RGB_CFG = 00, No Swap

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0

Table 36-3. RGB Format in Default Mode, RGB_CFG = 00, No Swap

	Byte 0	R7(i)	R6(i)	R5(i)	R4(i)	R3(i)	R2(i)	R1(i)	R0(i)
	Byte 1	G7(i)	G6(i)	G5(i)	G4(i)	G3(i)	G2(i)	G1(i)	G0(i)
	Byte 2	B7(i)	B6(i)	B5(i)	B4(i)	B3(i)	B2(i)	B1(i)	B0(i)
RGB 8:8:8	Byte 3	R7(i+1)	R6(i+1)	R5(i+1)	R4(i+1)	R3(i+1)	R2(i+1)	R1(i+1)	R0(i+1)
	Byte 0	R4(i)	R3(i)	R2(i)	R1(i)	R0(i)	G5(i)	G4(i)	G3(i)
	Byte 1	G2(i)	G1(i)	G0(i)	B4(i)	B3(i)	B2(i)	B1(i)	B0(i)
	Byte 2	R4(i+1)	R3(i+1)	R2(i+1)	R1(i+1)	R0(i+1)	G5(i+1)	G4(i+1)	G3(i+1)
RGB 5:6:5	Byte 3	G2(i+1)	G1(i+1)	G0(i+1)	B4(i+1)	B3i+1)	B2(i+1)	B1(i+1)	B0(i+1)

Table 36-4. RGB Format, RGB_CFG = 10 (Mode 2), No Swap

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	Byte 0	G2(i)	G1(i)	G0(i)	R4(i)	R3(i)	R2(i)	R1(i)	R0(i)
	Byte 1	B4(i)	B3(i)	B2(i)	B1(i)	B0(i)	G5(i)	G4(i)	G3(i)
	Byte 2	G2(i+1)	G1(i+1)	G0(i+1)	R4(i+1)	R3(i+1)	R2(i+1)	R1(i+1)	R0(i+1)
RGB 5:6:5	Byte 3	B4(i+1)	B3(i+1)	B2(i+1)	B1(i+1)	B0(i+1)	G5(i+1)	G4(i+1)	G3(i+1)

Table 36-5. RGB Format in Default Mode, RGB_CFG = 00, Swap Activated

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
	Byte 0	R0(i)	R1(i)	R2(i)	R3(i)	R4(i)	R5(i)	R6(i)	R7(i)
	Byte 1	G0(i)	G1(i)	G2(i)	G3(i)	G4(i)	G5(i)	G6(i)	G7(i)
RGB 8:8:8	Byte 2	B0(i)	B1(i)	B2(i)	B3(i)	B4(i)	B5(i)	B6(i)	B7(i)
	Byte 3	R0(i+1)	R1(i+1)	R2(i+1)	R3(i+1)	R4(i+1)	R5(i+1)	R6(i+1)	R7(i+1)
	Byte 0	G3(i)	G4(i)	G5(i)	R0(i)	R1(i)	R2(i)	R3(i)	R4(i)
	Byte 1	B0(i)	B1(i)	B2(i)	B3(i)	B4(i)	G0(i)	G1(i)	G2(i)
RGB 5:6:5	Byte 2	G3(i+1)	G4(i+1)	G5(i+1)	R0(i+1)	R1(i+1)	R2(i+1)	R3(i+1)	R4(i+1)
	Byte 3	B0(i+1)	B1(i+1)	B2(i+1)	B3(i+1)	B4(i+1)	G0(i+1)	G1(i+1)	G2(i+1)

The RGB 5:6:5 input format is processed to be displayed as RGB 5:5:5 format. The RGB 5:5:5 format is compliant with the 16-bit mode of the LCD controller.

36.5.3 Clocks

The sensor master clock (MCK) can be generated either by the power manager through a programmable clock output or by an external oscillator connected to the sensor.

None of the sensors embeds a power management controller, so providing the clock by the power manager is a simple and efficient way to control power consumption of the system.

Care must be taken when programming the system clock. The ISI has two clock domains, the system bus clock and the pixel clock provided by sensor. The two clock domains are not synchronized, but the system clock must be faster than pixel clock.

36.5.4 Preview Path

36.5.4.1 Scaling, Decimation (Subsampling)

This module resizes captured 8-bit color sensor images to fit the LCD display format. The resize module performs only downscaling. The same ratio is applied for both horizontal and vertical resize, then a fractional decimation algorithm is applied.

The decimation factor is a multiple of 1/16 and values 0 to 15 are forbidden.

Table 36-6. Decimation Factor

Dec value	0->15	16	17	18	19	...	124	125	126	127
Dec Factor	X	1	1.063	1.125	1.188	...	7.750	7.813	7.875	7.938

Table 36-7. Decimation and Scaler Offset Values

INPUT OUTPUT		352*288	640*480	800*600	1280*1024	1600*1200	2048*1536
VGA 640*480	F	NA	16	20	32	40	51
QVGA 320*240	F	16	32	40	64	80	102
CIF 352*288	F	16	26	33	56	66	85
QCIF 176*144	F	16	53	66	113	133	170

Example:

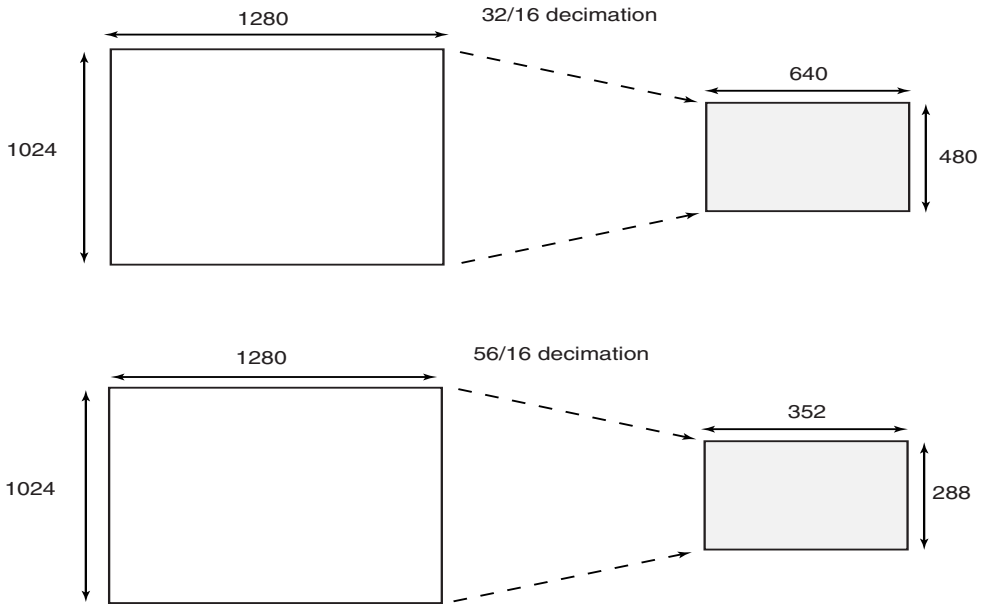
Input 1280*1024 Output=640*480

Hratio = 1280/640 =2

Vratio = 1024/480 =2.1333

The decimation factor is 2 so 32/16.

Figure 36-5. Resize Examples



36.5.4.2 Color Space Conversion

This module converts YCrCb or YUV pixels to RGB color space. Clipping is performed to ensure that the samples value do not exceed the allowable range. The conversion matrix is defined below:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} C_0 & 0 & C_1 \\ C_0 & -C_2 & -C_3 \\ C_0 & C_4 & 0 \end{bmatrix} \times \begin{bmatrix} Y - Y_{off} \\ C_b - C_{boff} \\ C_r - C_{roff} \end{bmatrix}$$

Example of programmable value to convert YCrCb to RGB:

$$\begin{cases} R = 1.164 \cdot (Y - 16) + 1.596 \cdot (C_r - 128) \\ G = 1.164 \cdot (Y - 16) - 0.813 \cdot (C_r - 128) - 0.392 \cdot (C_b - 128) \\ B = 1.164 \cdot (Y - 16) + 2.107 \cdot (C_b - 128) \end{cases}$$

An example of programmable value to convert from YUV to RGB:

$$\begin{cases} R = Y + 1.596 \cdot V \\ G = Y - 0.394 \cdot U - 0.436 \cdot V \\ B = Y + 2.032 \cdot U \end{cases}$$

36.5.4.3 Memory Interface

Preview datapath contains a data formatter that converts 8:8:8 pixel to RGB 5:5:5 format compliant with 16-bit format of the LCD controller. In general, when converting from a color channel with more bits to one with fewer bits, formatter module discards the lower-order bits. Example: Converting from RGB 8:8:8 to RGB 5:6:5, it discards the three LSBs from the red and blue channels, and two LSBs from the green channel. When grayscale mode is enabled, two memory format are supported. One mode supports 2 pixels per word, and the other mode supports 1 pixel per word.

Table 36-8. Grayscale Memory Mapping Configuration for 12-bit Data

GS_MODE	DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]
0	P_0[11:4]	P_0[3:0], 0000	P_1[11:4]	P_1[3:0], 0000
1	P_0[11:4]	P_0[3:0], 0000	0	0

36.5.4.4 FIFO and DMA Features

Both preview and Codec datapaths contain FIFOs, asynchronous buffers that are used to safely transfer formatted pixels from Pixel clock domain to High Speed Bus (HSB) clock domain. A video arbiter is used to manage FIFO thresholds and triggers a relevant DMA request through the HSB master interface. Thus, depending on FIFO state, a specified length burst is asserted. Regarding HSB master interface, it supports Scatter DMA mode through linked list operation. This mode of operation improves flexibility of image buffer location and allows the user to allocate two or more frame buffers. The destination frame buffers are defined by a series of Frame Buffer Descriptors (FBD). Each FBD controls the transfer of one entire frame and then optionally loads a further FBD to switch the DMA operation at another frame buffer address. The FBD is defined by a series of two words. The first one defines the current frame buffer address, and the second defines the next FBD memory location. This DMA transfer mode is only available for preview datapath and is configured in the PPFBD register that indicates the memory location of the first FBD.

The primary FBD is programmed into the camera interface controller. The data to be transferred described by an FBD requires several burst access. In the example below, the use of 2 ping-pong frame buffers is described.

36.5.4.5 Example

The first FBD, stored at address 0x30000, defines the location of the first frame buffer.

Destination Address: frame buffer ID0 0x02A000

Next FBD address: 0x30010

Second FBD, stored at address 0x30010, defines the location of the second frame buffer.

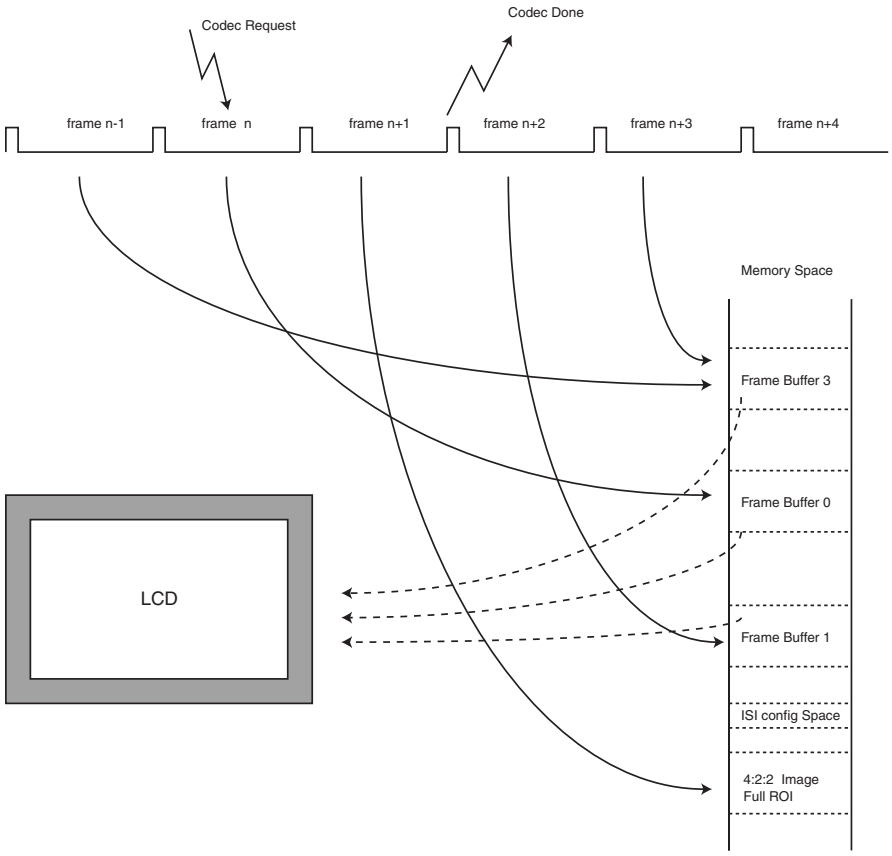
Destination Address: frame buffer ID1 0x3A000

Transfer width: 32 bit

Next FBD address: 0x30000, wrapping to first FBD.

Using this technique, several frame buffers can be configured through the linked list. Figure 36-6 illustrates a typical three frame buffer application. Frame n is mapped to frame buffer 0, frame n+1 is mapped to frame buffer 1, frame n+2 is mapped to Frame buffer 2, further frames wrap. A codec request occurs, and the full-size 4:2:2 encoded frame is stored in a dedicated memory space.

Figure 36-6. Three Frame Buffers Application and Memory Mapping



36.5.5 Codec Path

36.5.5.1 Color Space Conversion

Depending on user selection, this module can be bypassed so that input YCrCb stream is directly connected to the format converter module. If the RGB input stream is selected, this module converts RGB to YCrCb color space with the formulas given below:

$$\begin{bmatrix} Y \\ C_r \\ C_b \end{bmatrix} = \begin{bmatrix} C_0 & C_1 & C_2 \\ C_3 & -C_4 & -C_5 \\ -C_6 & -C_7 & C_8 \end{bmatrix} \times \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} Y_{off} \\ Cr_{off} \\ Cb_{off} \end{bmatrix}$$

An example of coefficients are given below:

$$\begin{cases} Y = 0.257 \cdot R + 0.504 \cdot G + 0.098 \cdot B + 16 \\ C_r = 0.439 \cdot R - 0.368 \cdot G - 0.071 \cdot B + 128 \\ C_b = -0.148 \cdot R - 0.291 \cdot G + 0.439 \cdot B + 128 \end{cases}$$

36.5.5.2 Memory Interface

Dedicated FIFO are used to support packed memory mapping. YCrCb pixel components are sent in a single 32-bit word in a contiguous space (packed). Data is stored in the order of natural scan lines. Planar mode is not supported.

36.5.5.3 DMA Features

Unlike preview datapath, codec datapath DMA mode does not support linked list operation. Only the CODEC_DMA_ADDR register is used to configure the frame buffer base address.

36.6 Image Sensor Interface (ISI) User Interface

Table 36-9. ISI Registers

Offset	Register Name	Register	Access	Reset Value
0x00	ISI Control 1 Register	CR1	Read/Write	0x00000002
0x04	ISI Control 2 Register	CR2	Read/Write	0x00000000
0x08	ISI Status Register	SR	Read	0x00000000
0x0C	ISI Interrupt Enable Register	IER	Write	0x00000000
0x10	ISI Interrupt Disable Register	IDR	Write	0x00000000
0x14	ISI Interrupt Mask Register	IMR	Read	0x00000000
0x18	Reserved	-	-	-
0x1C	Reserved	-	-	-
0x20	ISI Preview Size Register	PSIZE	Read/Write	0x00000000
0x24	ISI Preview Decimation Factor Register	PDECF	Read/Write	0x00000010
0x28	ISI Preview Primary FBD Register	PPFBD	Read/Write	0x00000000
0x2C	ISI Codec DMA Base Address Register	CDBA	Read/Write	0x00000000
0x30	ISI CSC YCrCb To RGB Set 0 Register	Y2R_SET0	Read/Write	0x6832cc95
0x34	ISI CSC YCrCb To RGB Set 1 Register	Y2R_SET1	Read/Write	0x00007102
0x38	ISI CSC RGB To YCrCb Set 0 Register	R2Y_SET0	Read/Write	0x01324145
0x3C	ISI CSC RGB To YCrCb Set 1 Register	R2Y_SET1	Read/Write	0x01245e38
0x40	ISI CSC RGB To YCrCb Set 2 Register	R2Y_SET2	Read/Write	0x01384a4b
0x44-0xFC	Reserved	–	–	–

36.6.1 ISI Control 1 Register

Register Name: CR1

Access Type: Read/Write

Reset Value: 0x00000002

31	30	29	28	27	26	25	24
SFD							

23	22	21	20	19	18	17	16
SLD							

15	14	13	12	11	10	9	8
CODEC_EN	THMASK		FULL	-	FRATE		

7	6	5	4	3	2	1	0
CRC_SYNC	EMB_SYNC	-	PIXCLK_POL	VSYNC_POL	HSYNC_POL	DIS	RST

- **RST: Image sensor interface reset**

0: No action

1: Resets the image sensor interface.

- **DIS: Image sensor disable:**

0: Enable the image sensor interface.

1: Finish capturing the current frame and then shut down the module.

- **HSYNC_POL: Horizontal synchronization polarity**

0: HSYNC active high

1: HSYNC active low

- **VSYNC_POL: Vertical synchronization polarity**

0: VSYNC active high

1: VSYNC active low

- **PIXCLK_POL: Pixel clock polarity**

0: Data is sampled on rising edge of pixel clock

1: Data is sampled on falling edge of pixel clock

- **EMB_SYNC: Embedded synchronization**

0: Synchronization by HSYNC, VSYNC

1: Synchronization by embedded synchronization sequence SAV/EAV

- **CRC_SYNC: Embedded synchronization**

0: No CRC correction is performed on embedded synchronization

1: CRC correction is performed. if the correction is not possible, the current frame is discarded and the CRC_ERR is set in the status register.

- **FRATE: Frame rate [0..7]**

0: All the frames are captured, else one frame every FRATE+1 is captured.

- **FULL: Full mode is allowed**

0: Codec and preview datapaths are not working simultaneously

1: Both codec and preview datapaths are working simultaneously

- **THMASK: Threshold mask**

0: 4, 8 and 16 HSB bursts are allowed

1: 8 and 16 HSB bursts are allowed

2: Only 16 HSB bursts are allowed

- **CODEC_EN: Enable the codec path enable bit**

This bit always read as zero

0: The codec path is disabled

1: The codec path is enabled and the next frame is captured

- **SLD: Start of Line Delay**

SLD pixel clock periods to wait before the beginning of a line.

- **SFD: Start of Frame Delay**

SFD lines are skipped at the beginning of the frame.

36.6.2 ISI Control 2 Register

Register Name: CR2

Access Type: Read/Write

Reset Value: 0x0

31	30	29	28	27	26	25	24
RGB_CFG		YCC_SWAP		-	IM_HSIZE		

23	22	21	20	19	18	17	16
IM_HSIZE							

15	14	13	12	11	10	9	8
COL_SPACE	RGB_SWAP	GRAYSCALE	RGB_MODE	GS_MODE	IM_VSIZE		

7	6	5	4	3	2	1	0
IM_VSIZE							

- **IM_VSIZE: Vertical size of the Image sensor [0..2047]**

Vertical size = IM_VSIZE + 1

- **GS_MODE**

0: 2 pixels per word

1: 1 pixel per word

- **RGB_MODE: RGB input mode**

0: RGB 8:8:8 24 bits

1: RGB 5:6:5 16 bits

- **GRAYSCALE**

0: Grayscale mode is disabled

1: Input image is assumed to be grayscale coded

- **RGB_SWAP**

0: D7 -> R7

1: D0 -> R7

The RGB_SWAP has no effect when the grayscale mode is enabled.

- **COL_SPACE: Color space for the image data**

0: YCbCr

1: RGB

- **IM_HSIZE: Horizontal size of the Image sensor [0..2047]**

Horizontal size = IM_HSIZE + 1

- **YCC_SWAP: Defines the YCC image data**

YCC_SWAP	Byte 0	Byte 1	Byte 2	Byte 3
00: Default	Cb(i)	Y(i)	Cr(i)	Y(i+1)
01: Mode1	Cr(i)	Y(i)	Cb(i)	Y(i+1)
10: Mode2	Y(i)	Cb(i)	Y(i+1)	Cr(i)
11: Mode3	Y(i)	Cr(i)	Y(i+1)	Cb(i)

- **RGB_CFG: Defines RGB pattern when RGB_MODE is set to 1**

RGB_CFG	Byte 0	Byte 1	Byte 2	Byte 3
00: Default	R/G(MSB)	G(LSB)/B	R/G(MSB)	G(LSB)/B
01: Mode1	B/G(MSB)	G(LSB)/R	B/G(MSB)	G(LSB)/R
10: Mode2	G(LSB)/R	B/G(MSB)	G(LSB)/R	B/G(MSB)
11: Mode3	G(LSB)/B	R/G(MSB)	G(LSB)/B	R/G(MSB)

If RGB_MODE is set to RGB 8:8:8, then RGB_CFG = 0 implies RGB color sequence, else it implies BGR color sequence.

36.6.3 ISI Status Register

Register Name: SR

Access Type: Read

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	FR_OVR	FO_C_EMP
7	6	5	4	3	2	1	0
FO_P_EMP	FO_P_OVF	FO_C_OVF	CRC_ERR	CDC_STAT	SOFTRST	DIS	SOF

- **SOF: Start of frame**

0: No start of frame has been detected.

1: A start of frame has been detected.

- **DIS: Image Sensor Interface disable**

0: The image sensor interface is enabled.

1: The image sensor interface is disabled and stops capturing data. The DMA controller and the core can still read the FIFOs.

- **SOFTRST: Software reset**

0: Software reset not asserted or not completed

1: Software reset has completed successfully

- **CDC_STAT: Codec Request Status**

0: Codec request has been asserted

1: Codec request has been serviced

- **CRC_ERR: CRC synchronization error**

0: No crc error in the embedded synchronization frame (SAV/EAV)

1: The CRC_SYNC is enabled in the control register and an error has been detected and not corrected. The frame is discarded and the ISI waits for a new one.

- **FO_C_OVF: FIFO codec overflow**

0: No overflow

1: An overrun condition has occurred in input FIFO on the codec path. The overrun happens when the FIFO is full and an attempt is made to write a new sample to the FIFO.

- **FO_P_OVF: FIFO preview overflow**

0: No overflow

1: An overrun condition has occurred in input FIFO on the preview path. The overrun happens when the FIFO is full and an attempt is made to write a new sample to the FIFO.

- **FO_P_EMP**

0:The DMA has not finished transferring all the contents of the preview FIFO.

1:The DMA has finished transferring all the contents of the preview FIFO.

- **FO_C_EMP**

0: The DMA has not finished transferring all the contents of the codec FIFO.

1: The DMA has finished transferring all the contents of the codec FIFO.

- **FR_OVR: Frame overrun**

0: No frame overrun.

1: Frame overrun, the current frame is being skipped because a vsync signal has been detected while flushing FIFOs.

36.6.4 Interrupt Enable Register

Register Name: IER

Access Type: Write

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	FR_OVR	FO_C_EMP
7	6	5	4	3	2	1	0
FO_P_EMP	FO_P_OVF	FO_C_OVF	CRC_ERR	–	SOFTRST	DIS	SOF

- **SOF: Start of Frame**

1: Enables the Start of Frame interrupt.

- **DIS: Image Sensor Interface disable**

1: Enables the DIS interrupt.

- **SOFTRST: Soft Reset**

1: Enables the Soft Reset Completion interrupt.

- **CRC_ERR: CRC synchronization error**

1: Enables the CRC_SYNC interrupt.

- **FO_C_OVF: FIFO codec Overflow**

1: Enables the codec FIFO overflow interrupt.

- **FO_P_OVF: FIFO preview Overflow**

1: Enables the preview FIFO overflow interrupt.

- **FO_P_EMP**

1: Enables the preview FIFO empty interrupt.

- **FO_C_EMP**

1: Enables the codec FIFO empty interrupt.

- **FR_OVR: Frame overrun**

1: Enables the Frame overrun interrupt.

36.6.5 ISI Interrupt Disable Register

Register Name: IDR

Access Type: Write

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	FR_OVR	FO_C_EMP
7	6	5	4	3	2	1	0
FO_P_EMP	FO_P_OVF	FO_C_OVF	CRC_ERR	–	SOFTRST	DIS	SOF

- **SOF: Start of Frame**

1: Disables the Start of Frame interrupt.

- **DIS: Image Sensor Interface disable**

1: Disables the DIS interrupt.

- **SOFTRST**

1: Disables the soft reset completion interrupt.

- **CRC_ERR: CRC synchronization error**

1: Disables the CRC_SYNC interrupt.

- **FO_C_OVF: FIFO codec overflow**

1: Disables the codec FIFO overflow interrupt.

- **FO_P_OVF: FIFO preview overflow**

1: Disables the preview FIFO overflow interrupt.

- **FO_P_EMP**

1: Disables the preview FIFO empty interrupt.

- **FO_C_EMP**

1: Disables the codec FIFO empty interrupt.

- **FR_OVR: Frame overrun**

1: Disables frame overrun interrupt.

36.6.6 ISI Interrupt Mask Register

Register Name: IMR

Access Type: Read

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	FR_OVR	FO_C_EMP
7	6	5	4	3	2	1	0
FO_P_EMP	FO_P_OVF	FO_C_OVF	CRC_ERR	–	SOFTRST	DIS	SOF

- **SOF: Start of Frame**

0: The Start of Frame interrupt is disabled.

1: The Start of Frame interrupt is enabled.

- **DIS: Image sensor interface disable**

0: The DIS interrupt is disabled.

1: The DIS interrupt is enabled.

- **SOFTRST**

0: The soft reset completion interrupt is enabled.

1: The soft reset completion interrupt is disabled.

- **CRC_ERR: CRC synchronization error**

0: The CRC_SYNC interrupt is disabled.

1: The CRC_SYNC interrupt is enabled.

- **FO_C_OVF: FIFO codec overflow**

0: The codec FIFO overflow interrupt is disabled.

1: The codec FIFO overflow interrupt is enabled.

- **FO_P_OVF: FIFO preview overflow**

0: The preview FIFO overflow interrupt is disabled.

1: The preview FIFO overflow interrupt is enabled.

- **FO_P_EMP**

0: The preview FIFO empty interrupt is disabled.

1: The preview FIFO empty interrupt is enabled.

- **FO_C_EMP**

0: The codec FIFO empty interrupt is disabled.

1: The codec FIFO empty interrupt is enabled.

- **FR_OVR: Frame Overrun**

0: The frame overrun interrupt is disabled.

1: The frame overrun interrupt is enabled.

36.6.7 ISI Preview Size Register

Register Name: PSIZE

Access Type: Read/Write

Reset Value: 0x0

31	30	29	28	27	26	25	24
–	–	–	–	–	–	PREV_HSIZE	

23	22	21	20	19	18	17	16
PREV_HSIZE							

15	14	13	12	11	10	9	8
–	–	–	–	–	–	PREV_VSIZE	

7	6	5	4	3	2	1	0
PREV_VSIZE							

- **PREV_VSIZE: Vertical size for the preview path**

Vertical Preview size = PREV_VSIZE + 1 (480 max)

- **PREV_HSIZE: Horizontal size for the preview path**

Horizontal Preview size = PREV_HSIZE + 1 (640 max)

36.6.8 ISI Preview Decimation Factor Register

Register Name: PDECF

Access Type: Read/Write

Reset Value: 0x00000010

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
DEC_FACTOR							

- **DEC_FACTOR: Decimation factor**

DEC_FACTOR is 8-bit width, range is from 16 to 255. Values from 0 to 16 do not perform any decimation.

36.6.9 ISI Preview Primary FBD Register

Register Name: PPFBD

Access Type: Read/Write

Reset Value: 0x0

31	30	29	28	27	26	25	24
PREV_FBD_ADDR							

23	22	21	20	19	18	17	16
PREV_FBD_ADDR							

15	14	13	12	11	10	9	8
PREV_FBD_ADDR							

7	6	5	4	3	2	1	0
PREV_FBD_ADDR							

- **PREV_FBD_ADDR: Base address for preview frame buffer descriptor**

Written with the address of the start of the preview frame buffer queue, reads as a pointer to the current buffer being used. Forced to word alignement, ie the 2 lowest bits always read zero.

36.6.10 ISI Codec DMA Base Address Register

Register Name: CDBA

Access Type: Read/Write

Reset Value: 0x0

31	30	29	28	27	26	25	24
CODEC_DMA_ADDR							

23	22	21	20	19	18	17	16
CODEC_DMA_ADDR							

15	14	13	12	11	10	9	8
CODEC_DMA_ADDR							

7	6	5	4	3	2	1	0
CODEC_DMA_ADDR							

- **CODEC_DMA_ADDR: Base address for codec DMA**

This register contains codec datapath start address of buffer location. Forced to word alignement, ie the 2 lowest bits always read zero.

36.6.11 ISI Color Space Conversion YCrCb to RGB Set 0 Register

Register Name: Y2R_SET0

Access Type: Read/Write

Reset Value: 0x6832cc95

31	30	29	28	27	26	25	24
C3							
23	22	21	20	19	18	17	16
C2							
15	14	13	12	11	10	9	8
C1							
7	6	5	4	3	2	1	0
C0							

- **C3 : Color Space Conversion Matrix Coefficient C3**

C3 element, default step is 1/128, ranges from 0 to 255/128

- **C2 : Color Space Conversion Matrix Coefficient C2**

C2 element, default step is 1/128, ranges from 0 to 255/128

- **C1 : Color Space Conversion Matrix Coefficient C1**

C1 element, default step is 1/128, ranges from 0 to 255/128

- **C0 : Color Space Conversion Matrix Coefficient C0**

C0 element, default step is 1/128, ranges from 0 to 255/128

36.6.12 ISI Color Space Conversion YCrCb to RGB Set 1 Register

Register Name: Y2R_SET1

Access Type: Read/Write

Reset Value: 0x00007102

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	Cboff	Croff	Yoff	–	–	–	C4

C4

- **C4: Color Space Conversion Matrix coefficient C4**

C4 element default step is 1/128, ranges from 0 to 512/128

- **Yoff: Color Space Conversion Luminance default offset**

0: No offset

1: Offset = 128

- **Croff: Color Space Conversion Red Chrominance default offset**

0: No offset

1: Offset = 16

- **Cboff: Color Space Conversion Blue Chrominance default offset**

0: No offset

1: Offset = 16

36.6.13 ISI Color Space Conversion RGB to YCrCb Set 0 Register

Register Name: R2Y_SET0

Access Type: Read/Write

Reset Value: 0x01324145

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	Roff

23	22	21	20	19	18	17	16
-	C2						

15	14	13	12	11	10	9	8
-	C1						

7	6	5	4	3	2	1	0
-	C0						

- **C0: Color Space Conversion Matrix coefficient C0**

C0 element default step is 1/256, from 0 to 127/256

- **C1: Color Space Conversion Matrix coefficient C1**

C1 element default step is 1/128, from 0 to 127/128

- **C2: Color Space Conversion Matrix coefficient C2**

C2 element default step is 1/512, from 0 to 127/512

- **Roff: Color Space Conversion Red component offset**

0: No offset

1: Offset = 16

36.6.14 ISI Color Space Conversion RGB to YCrCb Set 1 Register

Register Name: R2Y_SET1

Access Type: Read/Write

Reset Value: 0x01245e38

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	Goff

23	22	21	20	19	18	17	16
-	C5						

15	14	13	12	11	10	9	8
-	C4						

7	6	5	4	3	2	1	0
-	C3						

- **C3: Color Space Conversion Matrix coefficient C3**

C0 element default step is 1/128, ranges from 0 to 127/128

- **C4: Color Space Conversion Matrix coefficient C4**

C1 element default step is 1/256, ranges from 0 to 127/256

- **C5: Color Space Conversion Matrix coefficient C5**

C1 element default step is 1/512, ranges from 0 to 127/512

- **Goff: Color Space Conversion Green component offset**

0: No offset

1: Offset = 128

36.6.15 ISI Color Space Conversion RGB to YCrCb Set 2 Register

Register Name: R2Y_SET2

Access Type: Read/Write

Reset Value: 0x01384a4b

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	Boff
23	22	21	20	19	18	17	16
-	C8						
15	14	13	12	11	10	9	8
-	C7						
7	6	5	4	3	2	1	0
-	C6						

- **C6: Color Space Conversion Matrix coefficient C6**

C6 element default step is 1/512, ranges from 0 to 127/512

- **C7: Color Space Conversion Matrix coefficient C7**

C7 element default step is 1/256, ranges from 0 to 127/256

- **C8: Color Space Conversion Matrix coefficient C8**

C8 element default step is 1/128, ranges from 0 to 127/128

- **Boff: Color Space Conversion Blue component offset**

0: No offset

1: Offset = 128

37. On-Chip Debug

Rev: 1.0.0.0

37.1 Features

- **Debug interface in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 3**
- **JTAG access to all on-chip debug functions**
- **Advanced Program, Data, Ownership, and Watchpoint trace supported**
- **NanoTrace JTAG-based trace access**
- **Auxiliary port for high-speed trace information**
- **Hardware support for 6 Program and 2 Data breakpoints**
- **Unlimited number of software breakpoints supported**
- **Automatic CRC check of memory regions**
- **Advanced Program, Data, Ownership, and Watchpoint trace supported**

37.2 Overview

Debugging on the AT32AP7000 is facilitated by a powerful On-Chip Debug (OCD) system. The user accesses this through an external debug tool which connects to the JTAG port and the Auxiliary (AUX) port. The AUX port is primarily used for trace functions, and a JTAG-based debugger is sufficient for basic debugging.

The debug system is based on the Nexus 2.0 standard, class 3, which includes:

- Basic run-time control
- Program breakpoints
- Data breakpoints
- Program trace
- Ownership trace
- Data trace
- Run-time direct memory access

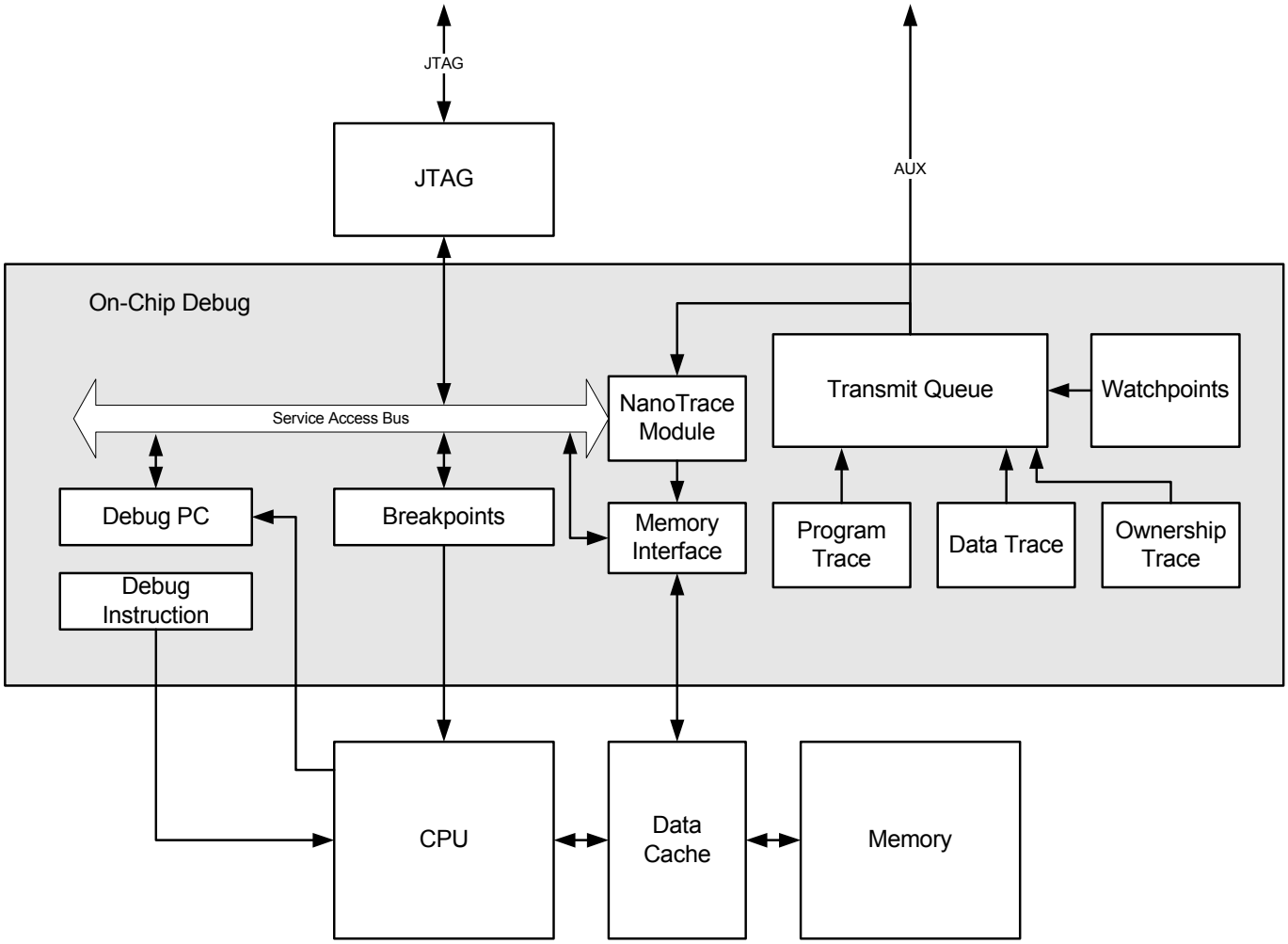
In addition to the mandatory Nexus debug features, the AT32AP7000 implements several useful OCD features, such as:

- Debug Communication Channel between CPU and JTAG
- Run-time PC monitoring
- CRC checking
- NanoTrace
- Software Quality Assurance (SQA) support

The OCD features are controlled by OCD registers, which can be accessed by JTAG when the NEXUS_ACCESS JTAG instruction is loaded. The CPU can also access OCD registers directly using mtdr/mfdr instructions in any privileged mode. The OCD registers are implemented based on the recommendations in the Nexus 2.0 standard, and are detailed in the AVR32AP Technical Reference Manual.

37.3 Block diagram

Figure 37-1. On-Chip Debug block diagram



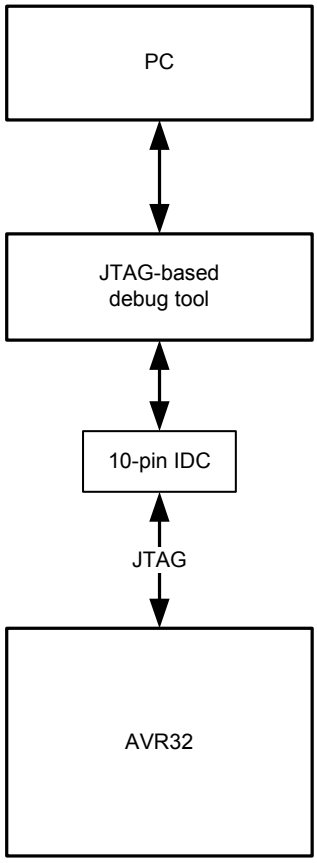
37.4 Functional description

37.4.1 JTAG-based debug features

A debugger can control all OCD features by writing OCD registers over the JTAG interface. Many of these do not depend on output on the AUX port, allowing a JTAG-based debugger to be used.

A JTAG-based debugger should connect to the device through a standard 10-pin IDC connector as described in the AVR32AP Technical Reference Manual.

Figure 37-2. JTAG-based debugger



37.4.1.1 Debug Communication Channel

The Debug Communication Channel (DCC) consists of a pair OCD registers with associated handshake logic, accessible to both CPU and JTAG. The registers can be used to exchange data between the CPU and the JTAG master, both runtime as well as in debug mode.

37.4.1.2 Breakpoints

One of the most fundamental debug features is the ability to halt the CPU, to examine registers and the state of the system. This is accomplished by breakpoints, of which many types are available:

- Unconditional breakpoints are set by writing OCD registers by JTAG, halting the CPU immediately.
- Program breakpoints halt the CPU when a specific address in the program is executed.
- Data breakpoints halt the CPU when a specific memory address is read or written, allowing variables to be watched.
- Software breakpoints halt the CPU when the breakpoint instruction is executed.

When a breakpoint triggers, the CPU enters debug mode, and the D bit in the status register is set. This is a privileged mode with dedicated return address and return status registers. All privileged instructions are permitted. Debug mode can be entered as either OCD Mode, running instructions from JTAG, or Monitor Mode, running instructions from program memory.

37.4.1.3 OCD Mode

When a breakpoint triggers, the CPU enters OCD mode, and instructions are fetched from the Debug Instruction OCD register. Each time this register is written by JTAG, the instruction is executed, allowing the JTAG to execute CPU instructions directly. The JTAG master can e.g. read out the register file by issuing mtdr instructions to the CPU, writing each register to the Debug Communication Channel OCD registers.

37.4.1.4 Monitor Mode

Since the OCD registers are directly accessible by the CPU, it is possible to build a software-based debugger that runs on the CPU itself. Setting the Monitor Mode bit in the Development Control register causes the CPU to enter Monitor Mode instead of OCD mode when a breakpoint triggers. Monitor Mode is similar to OCD mode, except that instructions are fetched from the debug exception vector in regular program memory, instead of issued by JTAG.

37.4.1.5 Program Counter monitoring

Normally, the CPU would need to be halted for a JTAG-based debugger to examine the current PC value. However, the AT32AP7000 also proves a Debug Program Counter OCD register, where the debugger can continuously read the current PC without affecting the CPU. This allows the debugger to generate a simple statistic of the time spent in various areas of the code, easing code optimization.

37.4.1.6 Cyclic Redundancy Check (CRC)

The MIU can be used to automatically calculate the CRC of a block of data in memory. The OCD will then read out each word in the specified memory block and report the CRC32-value in an OCD register.

37.4.1.7 NanoTrace

The MIU additionally supports NanoTrace. This is an AVR32-specific feature, in which trace data is output to memory instead of the AUX port. This allows the trace data to be extracted by JTAG MEMORY_ACCESS, enabling trace features for JTAG-based debuggers. The user must write OCD registers to configure the address and size of the memory block to be used for NanoTrace. The NanoTrace buffer can be anywhere in the physical address range, including internal and external RAM, through an EBI, if present. This area may not be used by the application running on the CPU.

37.4.2 AUX-based debug features

Utilizing the Auxiliary (AUX) port gives access to a wide range of advanced debug features. Of prime importance are the trace features, which allow an external debugger to receive continuous information on the program execution in the CPU. Additionally, Event In and Event Out pins allow external events to be correlated with the program flow.

The AUX port contains a number of pins, as shown in Table 37-1 on page 907. These are multiplexed with PIO lines, and must explicitly be enabled by writing OCD registers before the debug session starts. The AUX port is mapped to two different locations, selectable by OCD Registers, minimizing the chance that the AUX port will need to be shared with an application.

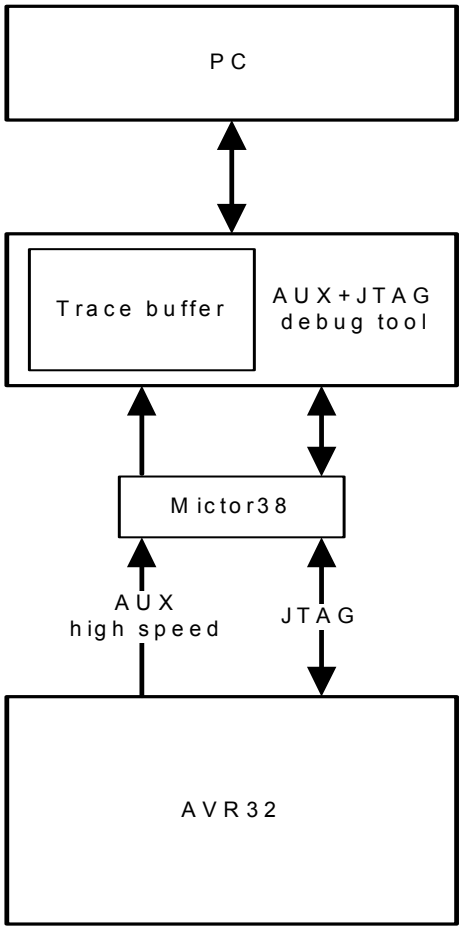
Debug tools utilizing the AUX port should connect to the device through a Nexus-compliant Mictor-38 connector, as described in the AVR32AP Technical Reference manual. This connector

includes the JTAG signals and the RESET_N pin, giving full access to the programming and debug features in the device.

Table 37-1. Auxiliary port signals

Signal	Direction	Description
MCKO	Output	Trace data output clock
MDO[5:0]	Output	Trace data output
MSEO[1:0]	Output	Trace frame control
EVTI_N	Input	Event In
EVTO_N	Output	Event Out

Figure 37-3. AUX+JTAG based debugger



37.4.2.1 Trace operation

Trace features are enabled by writing OCD registers by JTAG. The OCD extracts the trace information from the CPU, compresses this information and formats it into variable-length messages according to the Nexus standard. The messages are buffered in a 16-frame transmit queue, and are output on the AUX port one frame at a time.

The trace features can be configured to be very selective, to reduce the bandwidth on the AUX port. In case the transmit queue overflows, error messages are produced to indicate loss of

data. The transmit queue module can optionally be configured to halt the CPU when an overflow occurs, to prevent the loss of messages, at the expense of longer run-time for the program.

37.4.2.2 *Program Trace*

Program trace allows the debugger to continuously monitor the program execution in the CPU. Program trace messages are generated for every branch in the program, and contains compressed information, which allows the debugger to correlate the message with the source code to identify the branch instruction and target address.

37.4.2.3 *Data Trace*

Data trace outputs a message every time a specific location is read or written. The message contains information about the type (read/write) and size of the access, as well as the address and data of the accessed location. The AT32AP7000 contains two data trace channels, each of which are controlled by a pair of OCD registers which determine the range of addresses (or single address) which should produce data trace messages.

37.4.2.4 *Ownership Trace*

Program and data trace operate on virtual addresses. In cases where an operating system runs several processes in overlapping virtual memory segments, the Ownership Trace feature can be used to identify the process switch. When the O/S activates a process, it will write the process ID number to an OCD register, which produces an Ownership Trace Message, allowing the debugger to switch context for the subsequent program and data trace messages. As the use of this feature depends on the software running on the CPU, it can also be used to extract other types of information from the system.

37.4.2.5 *Watchpoint messages*

The breakpoint modules normally used to generate program and data breakpoints can also be used to generate Watchpoint messages, allowing a debugger to monitor program and data events without halting the CPU. Watchpoints can be enabled independently of breakpoints, so a breakpoint module can optionally halt the CPU when the trigger condition occurs. Data trace modules can also be configured to produce watchpoint messages instead of regular data trace messages.

37.4.2.6 *Event In and Event Out pins*

The AUX port also contains an Event In pin (EVTI_N) and an Event Out pin (EVTO_N). EVTI_N can be used to trigger a breakpoint when an external event occurs. It can also be used to trigger specific program and data trace synchronization messages, allowing an external event to be correlated to the program flow.

When the CPU enters debug mode, a Debug Status message is transmitted on the trace port. All trace messages can be timestamped when they are received by the debug tool. However, due to the latency of the transmit queue buffering, the timestamp will not be 100% accurate. To improve this, EVTO_N can toggle every time a message is inserted into the transmit queue, allowing trace messages to be timestamped precisely. EVTO_N can also toggle when a breakpoint module triggers, or when the CPU enters debug mode, for any reason. This can be used to measure precisely when the respective internal event occurs.

37.4.2.7 Software Quality Analysis (SQA)

Software Quality Analysis (SQA) deals with two important issues regarding embedded software development. *Code coverage* involves identifying untested parts of the embedded code, to improve test procedures and thus the quality of the released software. *Performance analysis* allows the developer to precisely quantify the time spent in various parts of the code, allowing bottlenecks to be identified and optimized.

Program trace must be used to accomplish these tasks without instrumenting (altering) the code to be examined. However, traditional program trace cannot reconstruct the current PC value without correlating the trace information with the source code, which cannot be done on-the-fly. This limits program trace to a relatively short time segment, determined by the size of the trace buffer in the debug tool.

The OCD system in AT32AP7000 extends program trace with SQA capabilities, allowing the debug tool to reconstruct the PC value on-the-fly. Code coverage and performance analysis can thus be reported for an unlimited execution sequence.

38. JTAG and Boundary Scan

Rev.: 1.0.0.0

38.1 Features

- **IEEE1149.1 compliant JTAG Interface**
- **Boundary-Scan Chain for board-level testing**
- **Direct memory access and programming capabilities through JTAG interface**
- **On-Chip Debug access in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0)**

38.2 Overview

Figure 38-1 on page 911 shows how the JTAG is connected in an AVR32 device. The TAP Controller is a state machine controlled by the TCK and TMS signals. The TAP Controller selects either the JTAG Instruction Register or one of several Data Registers as the scan chain (shift register) between the TDI-input and TDO-output. The Instruction Register holds JTAG instructions controlling the behavior of a Data Register.

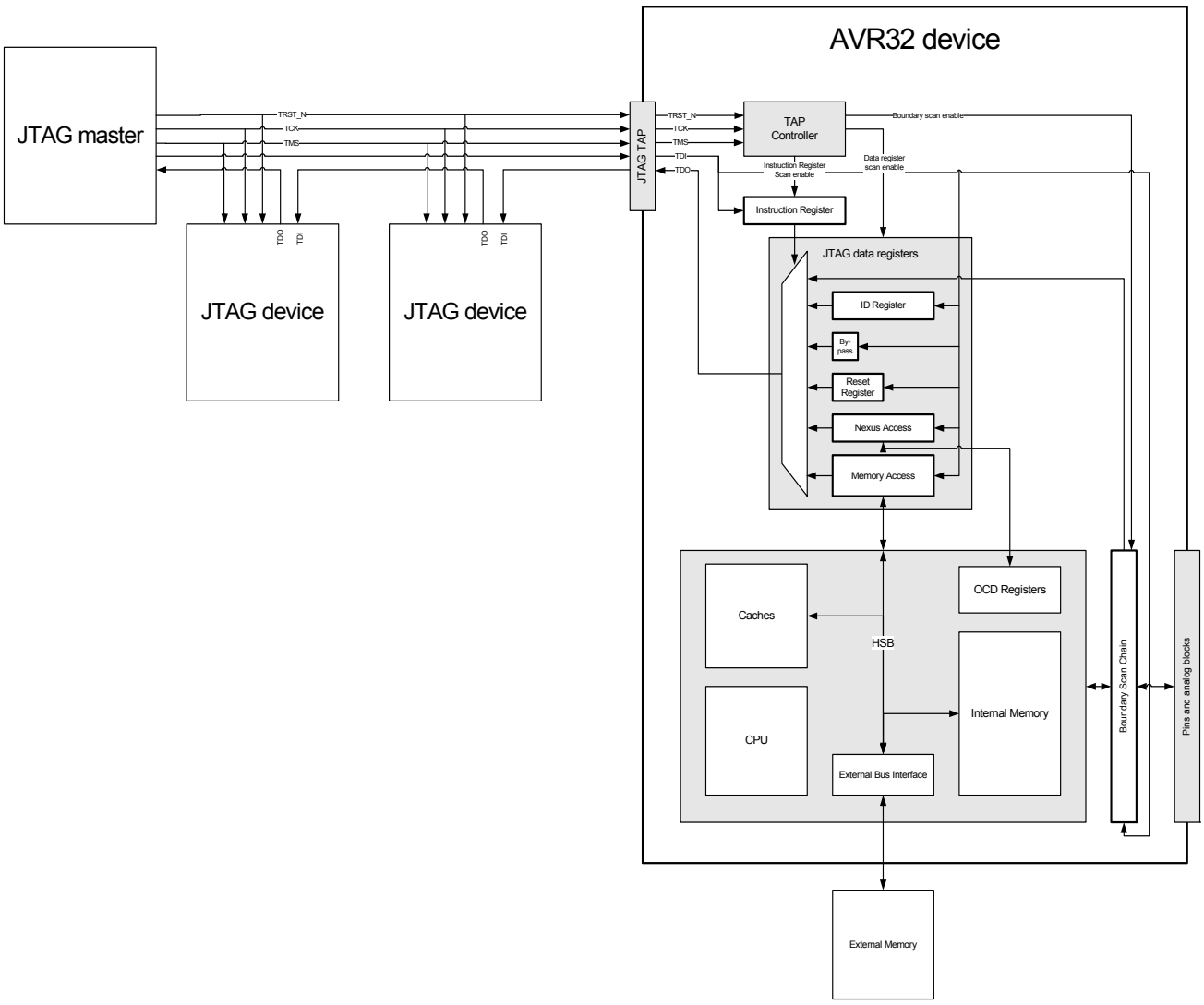
The Device Identification Register, Bypass Register, and the Boundary-Scan Chain are the Data Registers used for board-level testing. The Reset Register can be used to keep the device reset during test or programming.

The Service Access Bus (SAB) interface contains address and data registers for the Service Access Bus, which gives access to on-chip debug, programming, and other functions in the device. The SAB offers several modes of access to the address and data registers, as discussed in ”Service Access Bus” on page 914.

”JTAG Instruction Summary” on page 916 lists the supported JTAG instructions, with references to the description in this document.

38.3 Block diagram

Figure 38-1. JTAG and Boundary Scan access



38.4 Functional description

38.4.1 JTAG interface

The JTAG interface is accessed through the dedicated JTAG pins shown in Table 38-1 on page 912. The TMS control line navigates the TAP controller, as shown in Figure 38-2 on page 912. The TAP controller manages the serial access to the JTAG Instruction and Data registers. Data is scanned into the selected instruction or data register on TDI, and out of the register on TDO, in the Shift-IR and Shift-DR states, respectively. The LSB is shifted in and out first. TDO is high-Z in other states than Shift-IR and Shift-DR.

Independent of the initial state of the TAP Controller, the Test-Logic-Reset state can always be entered by holding TMS high for 5 TCK clock periods. This sequence should always be applied at the start of a JTAG session to bring the TAP Controller into a defined state before applying

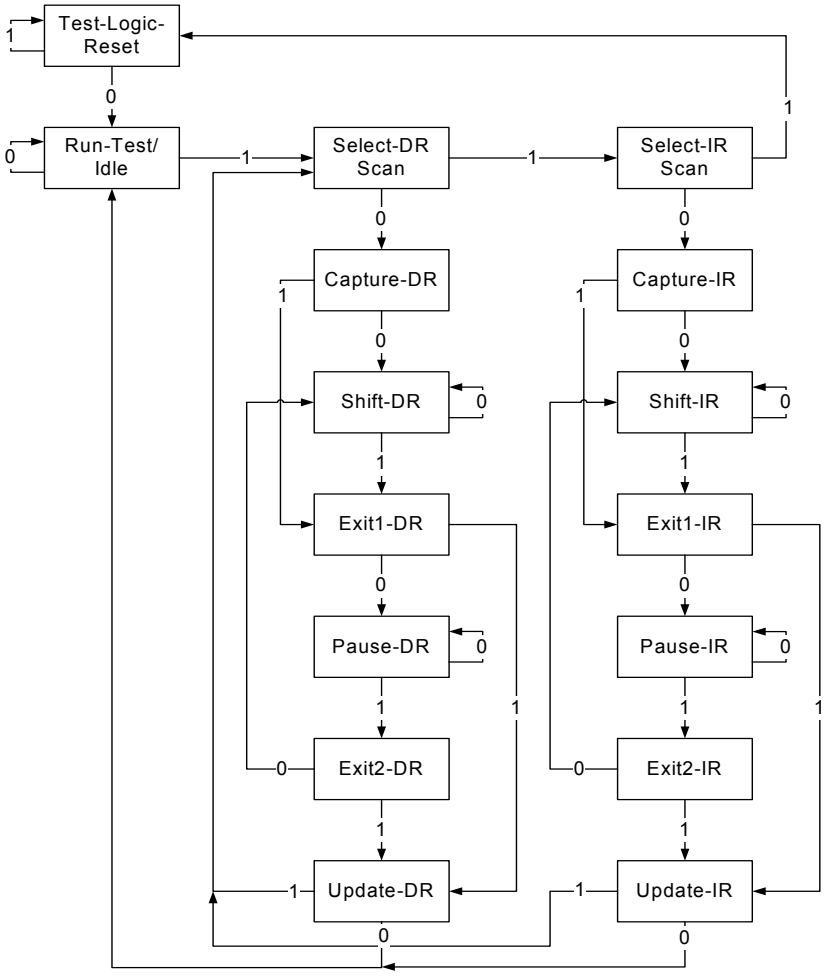
JTAG commands. Applying a 0 on TMS for 1 TCK period brings the TAP Controller to the Run-Test/Idle state, which is the starting point for JTAG operations.

The device implements a 5-bit Instruction Register (IR). A number of public JTAG instructions defined by the JTAG standard are supported, as described in "Public JTAG instructions" on page 917, as well as a number of AVR32-specific private JTAG instructions described in "Private JTAG Instructions" on page 918. Each instruction selects a specific data register for the Shift-DR path, as described for each instruction.

Table 38-1. JTAG pins

Pin	Direction	Description
TCK	Input	Test Clock. Fully asynchronous to system clock frequency.
TMS	Input	Test Mode Select, sampled on rising TCK
TDI	Input	Test Data In, sampled on rising TCK.
TDO	Output	Test Data Out, driven on falling TCK.

Figure 38-2. TAP Controller State Diagram



38.4.2 Typical sequence

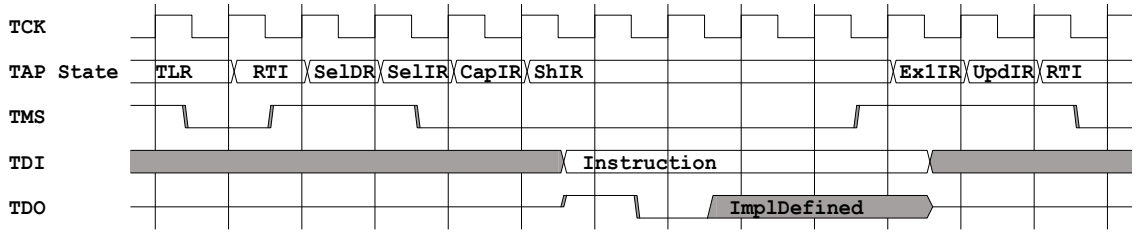
Assuming Run-Test/Idle is the present state, a typical scenario for using the JTAG interface is:

38.4.2.1 Scanning in JTAG instruction

At the TMS input, apply the sequence 1, 1, 0, 0 at the rising edges of TCK to enter the Shift Instruction Register - Shift-IR state. While in this state, shift the 5 bits of the JTAG instructions into the JTAG instruction register from the TDI input at the rising edge of TCK. The TMS input must be held low during input of the 4 LSBs in order to remain in the Shift-IR state. The JTAG Instruction selects a particular Data Register as path between TDI and TDO and controls the circuitry surrounding the selected Data Register.

Apply the TMS sequence 1, 1, 0 to re-enter the Run-Test/Idle state. The instruction is latched onto the parallel output from the shift register path in the Update-IR state. The Exit-IR, Pause-IR, and Exit2-IR states are only used for navigating the state machine.

Figure 38-3. Scanning in JTAG instruction



38.4.2.2 Scanning in/out data

At the TMS input, apply the sequence 1, 0, 0 at the rising edges of TCK to enter the Shift Data Register - Shift-DR state. While in this state, upload the selected Data Register (selected by the present JTAG instruction in the JTAG Instruction Register) from the TDI input at the rising edge of TCK. In order to remain in the Shift-DR state, the TMS input must be held low. While the Data Register is shifted in from the TDI pin, the parallel inputs to the Data Register captured in the Capture-DR state is shifted out on the TDO pin.

Apply the TMS sequence 1, 1, 0 to re-enter the Run-Test/Idle state. If the selected Data Register has a latched parallel-output, the latching takes place in the Update-DR state. The Exit-DR, Pause-DR, and Exit2-DR states are only used for navigating the state machine.

As shown in the state diagram, the Run-Test/Idle state need not be entered between selecting JTAG instruction and using Data Registers.

38.4.3 Boundary-Scan

The Boundary-Scan chain has the capability of driving and observing the logic levels on the digital I/O pins, as well as the boundary between digital and analog logic for analog circuitry having off-chip connections. At system level, all ICs having JTAG capabilities are connected serially by the TDI/TDO signals to form a long shift register. An external controller sets up the devices to drive values at their output pins, and observe the input values received from other devices. The controller compares the received data with the expected result. In this way, Boundary-Scan provides a mechanism for testing interconnections and integrity of components on Printed Circuits Boards by using the 4 TAP signals only.

The four IEEE 1149.1 defined mandatory JTAG instructions IDCODE, BYPASS, SAMPLE/PRELOAD, and EXTEST can be used for testing the Printed Circuit Board. Initial scanning of the data register path will show the ID-code of the device, since IDCODE is the default JTAG instruction. It may be desirable to have the AVR32 device in reset during test mode. If not reset, inputs to the device may be determined by the scan operations, and the internal software may be in an undetermined state when exiting the test mode. Entering reset, the outputs of any Port Pin will instantly enter the high impedance state, making the HIGHZ instruction redundant. If needed, the BYPASS instruction can be issued to make the shortest possible scan chain through the device. The device can be set in the reset state either by pulling the external RESETn pin low, or issuing the AVR_RESET instruction with appropriate setting of the Reset Data Register.

The EXTEST instruction is used for sampling external pins and loading output pins with data. The data from the output latch will be driven out on the pins as soon as the EXTEST instruction is loaded into the JTAG IR-register. Therefore, the SAMPLE/PRELOAD should also be used for setting initial values to the scan ring, to avoid damaging the board when issuing the EXTEST instruction for the first time. SAMPLE/PRELOAD can also be used for taking a snapshot of the external pins during normal operation of the part.

When using the JTAG interface for Boundary-Scan, the JTAG TCK clock is independent of the internal chip clock, which is not required to run.

NOTE: For pins connected to 5V lines care should be taken to not drive the pins to a logic one using boundary scan, as this will create a current flowing from the 3,3V driver to the 5V pullup on the line. Optionally a series resistor can be added between the line and the pin to reduce the current.

38.4.4 Service Access Bus

The AVR32 architecture offers a common interface for access to On-Chip Debug, programming, and test functions. These are mapped on a common bus called the Service Access Bus (SAB), which is linked to the JTAG port through a bus master module, which also handles synchronization between the JTAG and SAB clocks.

When accessing the SAB through the TAP there are no limitations on TCK frequency compared to chip frequency, although there must be an active system clock in order for the SAB accesses to complete. If the system clock is switched off in sleep mode, activity on the TCK pin will restart the system clock automatically, without waking the device from sleep. JTAG masters may optimize the transfer rate by adjusting the TCK frequency in relation to the system clock. This ratio can be measured with the SYNC instruction.

The Service Access Bus uses 36 address bits to address memory or registers in any of the slaves on the bus. The bus supports accesses of words (32 bits). All accesses must be aligned to the size of the access, i.e. word accesses must have the two lowest address bits cleared.

A number of private instructions are used to access SAB resources. Each of these are described in detail in ”Private JTAG Instructions” on page 918. The MEMORY_WORD_ACCESS instruction allows a read or write a word to any 36-bit address on the bus. NEXUS_ACCESS instruction is a Nexus-compliant shorthand instruction for accessing the 32-bit OCD registers in the 7-bit address space reserved for these. These instructions require two passes through the Shift-DR TAP state: one for the address and control information, and one for data.

To increase the transfer rate, consecutive memory accesses can be accomplished by the MEMORY_BLOCK_ACCESS instruction, which only requires a single pass through Shift-DR for data transfer only. The address is automatically increment the address.

The access time to SAB resources depends on the type of resource being accessed. It is possible to read external memory through the EBI, in which case the latency may be very long. It is possible to abort an ongoing SAB access by the CANCEL_ACCESS instruction, to avoid hanging the bus due to an extremely slow slave.

38.4.4.1 *Busy reporting*

As the time taken to perform an access may vary depending on system activity and current chip frequency, all the SAB access JTAG instructions can return a busy indicator. This indicates whether a delay needs to be inserted, or an operation needs to be repeated in order to be successful. If a new access is requested while the SAB is busy, the request is ignored.

The SAB becomes busy when:

- Entering Update-DR in the address phase of any read operation, e.g. after scanning in a NEXUS_ACCESS address with the read bit set.
- Entering Update-DR in the data phase of any write operation, e.g. after scanning in data for a NEXUS_ACCESS write.
- Entering Update-DR during a MEMORY_BLOCK_ACCESS.
- Entering Update-DR after scanning in a counter value for SYNC.
- Entering Update-IR after scanning in a MEMORY_BLOCK_ACCESS if the previous access was a read and data was scanned after scanning the address.

The SAB becomes ready again when:

- A read or write operation completes.
- A SYNC countdown completed.
- A operation is cancelled by the CANCEL_ACCESS instruction.

What to do if the busy bit is set:

- During Shift-IR: The new instruction is selected, but the previous operation has not yet completed and will continue (unless the new instruction is CANCEL_ACCESS). You may continue shifting the same instruction until the busy bit clears, or start shifting data. If shifting data, you must be prepared that the data shift may also report busy.
- During Shift-DR of an address: The new address is ignored. The SAB stays in address mode, so no data must be shifted. Repeat the address until the busy bit clears.
- During Shift-DR of read data: The read data are invalid. The SAB stays in data mode. Repeat scanning until the busy bit clears.
- During Shift-DR of write data: The write data are ignored. The SAB stays in data mode. Repeat scanning until the busy bit clears.

38.4.4.2 *Error reporting*

The Service access port may not be able to complete all accesses as requested. This may be because the address is invalid, the addressed area is read-only or cannot handle byte/halfword accesses, or because the chip is set in a protected mode where only limited accesses are allowed.

The error bit is updated when an access completes, and is cleared when a new access starts.

What to do if the error bit is set:

- During Shift-IR: The new instruction is selected. The last operation performed using the old instruction did not complete successfully.
- During Shift-DR of an address: The previous operation failed. The new address is accepted. If the read bit is set, a read operation is started.
- During Shift-DR of read data: The read operation failed, and the read data are invalid.
- During Shift-DR of write data: The previous write operation failed. The new data are accepted and a write operation started. This should only occur during block writes or stream writes. No error can occur between scanning a write address and the following write data.
- While polling with CANCEL_ACCESS: The previous access was cancelled. It may or may not have actually completed.

38.4.5 Memory programming

The High-Speed Bus (HSB) in the device is mapped as a slave on the SAB. This enables all HSB-mapped memories to be read or written through the SAB using JTAG instructions, as described in ”Service Access Bus” on page 914.

Internal SRAM can always be directly accessed. External static memory or SDRAM can be accessed if the EBI has been correctly configured to access this memory. It is also possible to access the configuration registers for these modules to set up the correct configuration. Similarly, external parallel flash can be programmed by accessing the registers for the flash device through the EBI.

Memory can be written while the CPU is executing, which can be utilized for debug purposes. When downloading a new program, the AVR_RESET instruction should be used to freeze the CPU, to prevent partially downloaded code from being executed.

38.5 JTAG Instruction Summary

The implemented JTAG instructions in the AVR32 are shown in the table below.

Table 38-2. JTAG Instruction Summary

Instruction OPCODE	Instruction	Description	Page
0x01	IDCODE	Select the 32-bit Device Identification register as data register.	917
0x02	SAMPLE_PRELOAD	Take a snapshot of external pin values without affecting system operation.	917
0x03	EXTEST	Select boundary scan chain as data register for testing circuitry external to the device.	917
0x04	INTEST	Select boundary scan chain for internal testing of the device.	917
0x06	CLAMP	Bypass device through Bypass register, while driving outputs from boundary scan register.	918
0x0C	AVR_RESET	Apply or remove a static reset to the device	923
0x10	NEXUS_ACCESS	Select the SAB Address and Data registers as data register for the TAP. The registers are accessed in Nexus mode.	919
0x11	MEMORY_WORD_ACCESS	Select the SAB Address and Data registers as data register for the TAP.	920

Table 38-2. JTAG Instruction Summary

Instruction OPCODE	Instruction	Description	Page
0x12	MEMORY_BLOCK_ACCESS	Select the SAB Data register as data register for the TAP. The address is auto-incremented.	921
0x13	CANCEL_ACCESS	Cancel an ongoing Nexus or Memory access.	922
0x17	SYNC	Synchronization counter	922
0x1F	BYPASS	Bypass this device through the bypass register.	918
Others	N/A	Acts as BYPASS	

38.6 Public JTAG instructions

38.6.1 IDCODE

This instruction selects the 32 bit Device Identification register as Data Register. The Device Identification register consists of a version number, a device number and the manufacturer code chosen by JEDEC. This is the default instruction after power-up.

The active states are:

- Capture-DR: The static IDCODE value is latched into the shift register.
- Shift-DR: The IDCODE scan chain is shifted by the TCK input.

38.6.2 SAMPLE_PRELOAD

JTAG instruction for taking a snap-shot of the input/output pins without affecting the system operation, and pre-loading the scan chain without updating the DR-latch. The Boundary-Scan Chain is selected as Data Register.

The active states are:

- Capture-DR: Data on the external pins are sampled into the Boundary-Scan Chain.
- Shift-DR: The Boundary-Scan Chain is shifted by the TCK input.

EXTEST

JTAG instruction for selecting the Boundary-Scan Chain as Data Register for testing circuitry external to the AVR32 package. The contents of the latched outputs of the Boundary-Scan chain is driven out as soon as the JTAG IR-register is loaded with the EXTEST instruction.

The active states are:

- Capture-DR: Data on the external pins is sampled into the Boundary-Scan Chain.
- Shift-DR: The Internal Scan Chain is shifted by the TCK input.
- Update-DR: Data from the scan chain is applied to output pins.

38.6.3 INTEST

This instruction selects the Boundary-Scan Chain as Data Register for testing internal logic in the device. The logic inputs are determined by the Boundary-Scan Chain, and the logic outputs are captured by the Boundary-Scan chain. The device output pins are driven from the Boundary-Scan Chain.

The active states are:

- Capture-DR: Data from the internal logic is sampled into the Boundary-Scan Chain.
- Shift-DR: The Internal Scan Chain is shifted by the TCK input.
- Update-DR: Data from the scan chain is applied to internal logic inputs.

38.6.4 CLAMP

This instruction selects the Bypass register as Data Register. The device output pins are driven from the Boundary-Scan Chain.

The active states are:

- Capture-DR: Loads a logic ‘0’ into the Bypass Register.
- Shift-DR: Data is scanned from TDI to TDO through the Bypass register.

38.6.5 BYPASS

JTAG instruction selecting the 1-bit Bypass Register for Data Register.

The active states are:

- Capture-DR: Loads a logic ‘0’ into the Bypass Register.
- Shift-DR: Data is scanned from TDI to TDO through the Bypass register.

38.7 Private JTAG Instructions

38.7.1 Notation

The AVR32 defines a number of private JTAG instructions. Each instruction is briefly described in text, with details following in table form.

Table 38-4 on page 919 shows bit patterns to be shifted in a format like "**peb01**". Each character corresponds to one bit, and eight bits are grouped together for readability. The rightmost bit is always shifted first, and the leftmost bit shifted last. The symbols used are shown in Table 38-3.

Table 38-3. Symbol description

Symbol	Description
0	Constant low value - always reads as zero.
1	Constant high value - always reads as one.
a	An address bit - always scanned with the least significant bit first
b	A busy bit. Reads as one if the SAB was busy, or zero if it was not. See ”Busy reporting” on page 915 for details on how the busy reporting works.
d	A data bit - always scanned with the least significant bit first.
e	An error bit. Reads as one if an error occurred, or zero if not. See ”Error reporting” on page 915 for details on how the error reporting works.
p	The chip protected bit. Some devices may be set in a protected state where access to chip internals are severely restricted. See the documentation for the specific device for details. On devices without this possibility, this bit always reads as zero.
r	A direction bit. Set to one to request a read, set to zero to request a write.
x	A don’t care bit. Any value can be shifted in, and output data should be ignored.

In many cases, it is not required to shift all bits through the data register. Bit patterns are shown using the full width of the shift register, but the suggested or required bits are emphasized using **bold** text. I.e. given the pattern "**aaaaaaar** xxxxxxxx xxxxxxxx xxxxxxxx xx", the shift register is 34 bits, but the test or debug unit may choose to shift only 8 bits "**aaaaaaar**".

The following describes how to interpret the fields in the instruction description tables:

Table 38-4. Instruction description

Instruction	Description
IR input value	Shows the bit pattern to shift into IR in the Shift-IR state in order to select this instruction. The pattern is show both in binary and in hexadecimal form for convenience. Example: **10000** (0x10)
IR output value	Shows the bit pattern shifted out of IR in the Shift-IR state when this instruction is active. Example: peb01
DR Size	Shows the number of bits in the data register chain when this instruction is active. Example: 34 bits
DR input value	Shows which bit pattern to shift into the data register in the Shift-DR state when this instruction is active. Multiple such lines may exist, e.g. to distinguish between reads and writes. Example: aaaaaaar xxxxxxxx xxxxxxxx xxxxxxxx xx
DR output value	Shows the bit pattern shifted out of the data register in the Shift-DR state when this instruction is active. Multiple such lines may exist, e.g. to distinguish between reads and writes. Example: xx **xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb**

38.7.2 NEXUS_ACCESS

This instruction allows Nexus-compliant access to on-chip debug registers through the SAB. OCD registers are addressed by their register index, as listed in the AVR32 Technical Reference Manual. The 7-bit register index and a read/write control bit, and the 32-bit data is accessed through the JTAG port.

The data register is alternately interpreted by the SAB as an address register and a data register. The SAB starts in address mode after the NEXUS_ACCESS instruction is selected, and toggles between address and data mode each time a data scan completes with the busy bit cleared.

NOTE: The polarity of the direction bit is inverse of the Nexus standard.

Starting in Run-Test/Idle, OCD registers are accessed in the following way:

1. Select the DR Scan path
2. Scan in the 7-bit address for the OCD register and a direction bit (1=read, 0=write).
3. Go to Update-DR and re-enter Select-DR Scan
4. For a read operation, scan out the contents of the addressed register. For a write operation, scan in the new contents of the register.
5. Return to Run-Test/Idle

For any operation, the full 7 bits of the address must be provided. For write operations, 32 data bits must be provided, or the result will be undefined. For read operations, shifting may be terminated once the required number of bits have been acquired.

Table 38-5. NEXUS_ACCESS details

Instructions	Details
IR input value	**10000** (0x10)
IR output value	peb01
DR Size	34 bits
DR input value (Address phase)	**aaaaaaar** xxxxxxxx xxxxxxxx xxxxxxxx xx
DR input value (Data read phase)	**xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx** xx
DR input value (Data write phase)	**dddddddd dddddddd dddddddd dddddddd** xx
DR output value (Address phase)	xx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb
DR output value (Data read phase)	eb **dddddddd dddddddd dddddddd dddddddd**
DR output value (Data write phase)	xx **xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb**

38.7.3 MEMORY_WORD_ACCESS

This instruction allows access to the entire Service Access Bus data area. Data are accessed through a 34-bit word index, a direction bit, and 32 bits of data. Since word allignment is implied only the 34 most significant bits of the Service Access Bus address is used.

The data register is alternately interpreted by the SAB as an address register and a data register. The SAB starts in address mode after the MEMORY_WORD_ACCESS instruction is selected, and toggles between address and data mode each time a data scan completes with the busy bit cleared.

Starting in Run-Test/Idle, SAB data are accessed in the following way:

1. Select the DR Scan path
2. Scan in the 34-bit address of the data to access, and a direction bit (1=read, 0=write).
3. Go to Update-DR and re-enter Select-DR Scan
4. For a read operation, scan out the contents of the addressed area. For a write operation, scan in the new contents of the area.
5. Return to Run-Test/Idle

For any operation, the full 34 bits of the address must be provided. For write operations, 32 data bits must be provided, or the result will be undefined. For read operations, shifting may be terminated once the required number of bits have been acquired.

Table 38-6. MEMORY_WORD_ACCESS details

Instructions	Details
IR input value	**10001** (0x11)
IR output value	peb01
DR Size	35 bits
DR input value (Address phase)	aaaaaaaa aaaaaaaa aaaaaaaa aaaaaaaa aar
DR input value (Data read phase)	**xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx** xxx

Table 38-6. MEMORY_WORD_ACCESS details (Continued)

Instructions	Details
DR input value (Data write phase)	**dddddddd dddddddd dddddddd dddddddd** xxx
DR output value (Address phase)	xxx xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx
DR output value (Data read phase)	xeb **dddddddd dddddddd dddddddd dddddddd**
DR output value (Data write phase)	xxx **xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb**

38.7.4 MEMORY_BLOCK_ACCESS

This instruction allows access to the entire SAB data area. Up to 32 bits of data are accessed at a time, while the address is sequentially incremented from the previously used address.

In this mode, the SAB address, and access direction is not provided with each access. Instead, the previous address is auto-incremented and the previous operation repeated. The address must be set up in advance with MEMORY_WORD_ACCESS. It is allowed, but not required, to shift data after shifting the address.

This instruction is primarily intended to speed up large quantities of sequential word accesses..

The following sequence should be used:

1. Use the MEMORY_WORD_ACCESS to read or write the first location.
2. Apply MEMORY_BLOCK_ACCESS in the IR Scan path.
3. Select the DR Scan path. The address will now have incremented by 4 (corresponding to the next word location).
4. For a read operation, scan out the contents of the next addressed location. For a write operation, scan in the new contents of the next addressed location.
5. Go to Update-DR
6. If the block access is not complete, return to Select-DR Scan and repeat the access.
7. If the block access is complete, return to Run-Test/Idle

For write operations, 32 data bits must be provided, or the result will be undefined. For read operations, shifting may be terminated once the required number of bits have been acquired.

Table 38-7. MEMORY_BLOCK_ACCESS details

Instructions	Details
IR input value	**10010** (0x12)
IR output value	peb01
DR Size	34 bits
DR input value (Data read phase)	**xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxxx** xx
DR input value (Data write phase)	**dddddddd dddddddd dddddddd dddddddd** xx
DR output value (Data read phase)	eb **dddddddd dddddddd dddddddd dddddddd**
DR output value (Data write phase)	xx **xxxxxxxx xxxxxxxx xxxxxxxx xxxxxxeb**

The overhead using block word access is 4 cycles per 32 bits of data, resulting in an 88% transfer efficiency, or 2.1 MBytes per second with a 20 MHz TCK frequency.

38.7.5 CANCEL_ACCESS

If a very slow memory location is accessed during a SAB memory access, it could take a very long time until the busy bit is cleared, and the SAB becomes ready for the next operation. The CANCEL_ACCESS instruction provides a possibility to abort an ongoing transfer and report a timeout to the user.

When the CANCEL_ACCESS instruction is selected, the current access will be terminated as soon as possible. There are no guarantees about how long this will take, as the hardware may not always be able to cancel the access immediately. The SAB is ready to respond to a new command when the busy bit clears.

Table 38-8. CANCEL_ACCESS details

Instructions	Details
IR input value	**10011** (0x13)
IR output value	peb01
DR Size	1
DR input value	x
DR output value	0

38.7.6 SYNC

This instruction allows external debuggers and testers to measure the ratio between the external JTAG clock and the internal system clock. The SYNC data register is a 16-bit counter that counts down to zero using the internal system clock. The busy bit stays high until the counter reaches zero.

Starting in Run-Test/Idle, SYNC instruction is used in the following way:

1. Select the DR Scan path
2. Scan in an 16-bit counter value
3. Go to Update-DR and re-enter Select-DR Scan
4. Scan out the busy bit, and retry until the busy bit clears.
5. Calculate an approximation to the internal clock speed using the elapsed time and the counter value.
6. Return to Run-Test/Idle

The full 16-bit counter value must be provided when starting the synch operation, or the result will be undefined. When reading status, shifting may be terminated once the required number of bits have been acquired.

Table 38-9. SYNC_ACCESS details

Instructions	Details
IR input value	**10111** (0x17)
IR output value	peb01
DR Size	16 bits
DR input value	dddddddd dddddddd
DR output value	xxxxxxxx xxxxxxeb

38.7.7 AVR_RESET

This instruction allows a debugger or tester to directly control separate reset domains inside the chip. The shift register contains one bit for each controllable reset domain. Setting a bit to one resets that domain and holds it in reset. Setting a bit to zero releases the reset for that domain.

See the device specific documentation for the number of reset domains, and what these domains are.

For any operation, all bits must be provided or the result will be undefined.

Table 38-10. AVR_RESET details

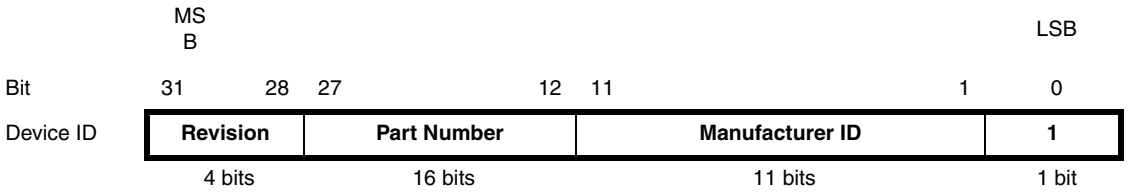
Instructions	Details
IR input value	**01100** (0x0C)
IR output value	p0001
DR Size	Device specific. Typically 5 bits.
DR input value	ddddd
DR output value	ddddd

38.8 JTAG Data Registers

The following device specific registers can be selected as JTAG scan chain depending on the instruction loaded in the JTAG Instruction Register. Additional registers exist, but are implicitly described in the functional description of the relevant instructions.

38.8.1 Device Identification Register

The Device Identification Register contains a unique identifier for each product. The register is selected by the IDCODE instruction, which is the default instruction after a JTAG reset.



Revision This is a 4 bit number identifying the revision of the component. Rev A = 0x0, B = 0x1, etc.

Part Number The part number is a 16 bit code identifying the component.

Manufacturer ID The Manufacturer ID is a 11 bit code identifying the manufacturer. The JTAG manufacturer ID for ATMEL is 0x01F.

38.8.1.1 Device specific ID codes

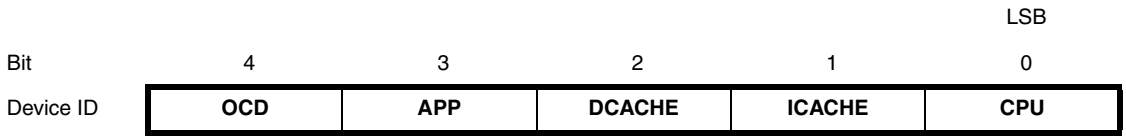
The different device configurations have different JTAG ID codes, as shown in Table 38-11. .

Table 38-11. Device and JTAG ID

Device name	JTAG ID code (r is the revision number)
AT32AP7000	0xr1E8203F

38.8.2 Reset register

The reset register is selected by the AVR_RESET instruction and contains one bit for each reset domain in the device. Setting each bit to one will keep that domain reset until the bit is cleared.



CPU CPU

ICACHE Instruction cache

DCACHE	Data cache and JTAG SAB interface
APP	HSB and PB buses
OCD	On-Chip Debug logic and registers

This register is intended to be used when programming the device, to avoid running partially downloaded code. The following procedure is recommended:

- RESET = OCD | APP | DCACHE | ICACHE | CPU
  - This will bring the entire system back to its reset state, regardless of the preceding state.
- RESET = ICACHE | CPU
  - This keeps the ICache and CPU from fetching and executing partially downloaded instructions.
- Perform the programming operations
- RESET = 0
  - The CPU will start executing from the reset vector.

It is not recommended to use the RESET register for other purposes than described above, as operations may not function correctly when parts of the system are reset.

38.8.3 Boundary-Scan Chain

The Boundary-Scan Chain has the capability of driving and observing the logic levels on the digital I/O pins, as well as driving and observing the logic levels between the digital I/O pins and the internal logic. Typically, output value, output enable, and input data are all available in the boundary scan chain.

The boundary scan chain is described in the BDSL (Boundary Scan Description Language) file available at the Atmel web site.

38.9 SAB address map

The Service Access Bus (SAB) gives the user access to the internal address space and other features through a 36 bits address space. The 4 MSBs identify the slave number, while the 32 LSBs are decoded within the slave's address space. The SAB slaves are shown in Table 38-12.

Table 38-12. SAB Slaves, addresses and descriptions.

Slave	Address [35:32]	Description
Unallocated	0x0	Intentionally unallocated
OCD	0x1	OCD registers
HSB cached	0x4	HSB memory space, as seen by the CPU through the data cache
HSB uncached	0x5	Alternative mapping for HSB space, as seen by the CPU bypassingthe data cache.
Reserved	Other	Unused

39. Boot Sequence

This chapter summarizes the boot sequence of the AT32AP7000. The behaviour after power-up is controlled by the Power Manager.

39.1 Starting of clocks

After power-up, the device will be held in a reset state by the Power-On Reset (POR) circuitry until the voltage has reached the power-on reset rising threshold value (see Electrical Characteristics for details). This ensures that all critical parts of the device are properly reset.

Once the power-on reset is complete, the device will use the XIN0 pin as clock source. XIN0 can be connected either to an external clock, or a crystal. The OSCEN_N pin is connected either to VDD or GND to inform the Power Manager on how the XIN0 pin is connected. If XIN0 receives a signal from a crystal, dedicated circuitry in the Power Manager keeps the part in a reset state until the oscillator connected to XIN0 has settled. If XIN0 receives an external clock, no such settling delay is applied.

On system start-up, the PLLs are disabled. All clocks to all modules are running. No clocks have a divided frequency, all parts of the system recieves a clock with the same frequency as the XIN0 clock.

Note that the power-on reset will release reset at a lower voltage threshold than the minimum specified operating voltage. If the voltage is not guaranteed to be stable by the time the device starts executing, an external brown-out reset circuit should be used.

39.2 Fetching of initial instructions

After reset has been released, the AVR32AP CPU starts fetching instructions from the reset address, which is 0xA000_0000. This address lies in the P2 segment, which is non-translated, non-cacheable, and permanently mapped to the physical address range 0x0000_0000 to 0x2000_0000. This means that the instruction being fetched from virtual address 0xA000_0000 is being fetched from physical address 0x0000_0000. Physical address 0x0000_0000 is mapped to EBI SRAM CS0. This is the external memory the device boots from.

The code read from the SRAM CS0 memory is free to configure the system to use for example the PLLs, to divide the frequency of the clock routed to some of the peripherals, and to gate the clocks to unused peripherals.

40. Mechanical Characteristics

40.1 AVR32AP7000

40.1.1 Thermal Considerations

40.1.1.1 Thermal Data

Table 40-1 summarizes the thermal resistance data depending on the package.

Table 40-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	CTBGA256	41.9	°C/W
θ_{JC}	Junction-to-case thermal resistance		CTBGA256	10.3	

40.1.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

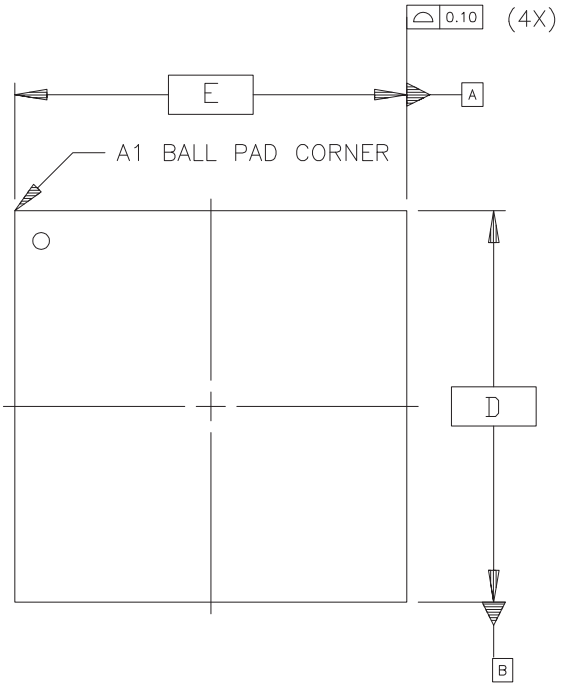
where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 40-4 on page 929.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 40-4 on page 929.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the Power consumption section, in the next chapter.
- T_A = ambient temperature (°C).

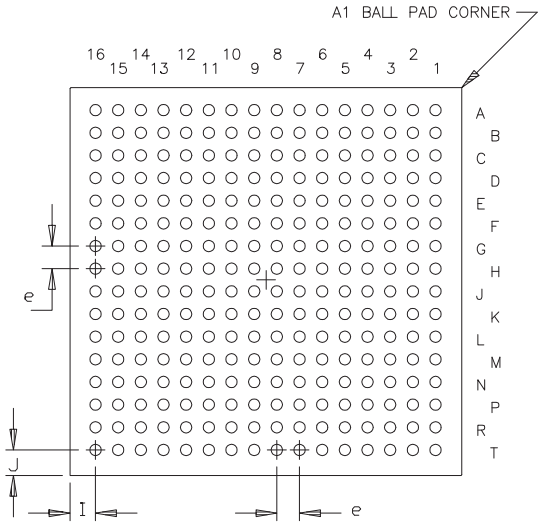
From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

40.1.2 Package Drawings

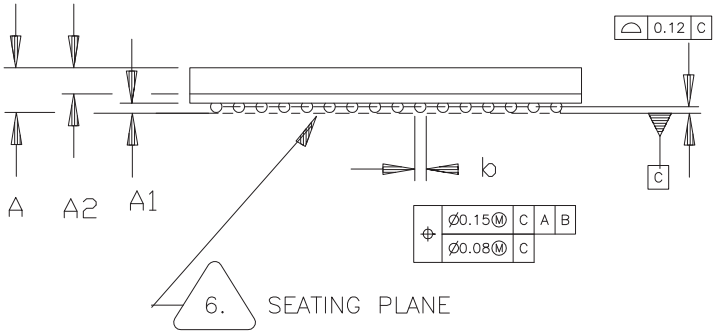
Figure 40-1. 256-balls CTBGA Package Drawing



TOP VIEW



BOTTOM VIEW



SIDE VIEW

	mm		
	MIN	NOM	MAX
A	1.01	1.11	1.21
A1	0.25	0.30	0.35
A2	0.55	0.60	0.65
e	1.00 BSC		
b	0.35	0.40	0.45
E/D	17.00 BSC		
I/J	1.00 REF		

Table 40-2. Soldering Information

Ball Land	0.48 mm
Solder Mask Opening	0.38 mm

Table 40-3. Device and 256-ball CTBGA Package Maximum Weight

650	mg

Table 40-4. 256-ball CTBGA Package Characteristics

Moisture Sensitivity Level	3

Table 40-5. Package Reference

JEDEC Drawing Reference	MO-216
JESD97 Classification	e1

40.1.3 Soldering Profile

Table 40-6 gives the recommended soldering profile from J-STD-20.

Table 40-6. Soldering Profile

Profile Feature	**Green Package**
Average Ramp-up Rate (217°C to Peak)	3°C/sec
Preheat Temperature 175°C ±25°C	60 - 180 sec
Temperature Maintained Above 217°C	60 - 150 sec
Time within 5°C of Actual Peak Temperature	20 - 40 sec
Peak Temperature Range	260 + 0°C
Ramp-down Rate	6°C/sec max
Time 25°C to Peak Temperature	8 minuts max

Note: It is recommended to apply a soldering temperature higher than 250°C. A maximum of three reflow passes is allowed per component.

41. Electrical Characteristics

41.1 Absolute Maximum Ratings

Table 41-1. Absolute Maximum Ratings*

Operating Temperature (Industrial) ..... -40°C to +85°C
Storage Temperature ..... -60°C to +150°C
Voltage on Input Pins with Respect to Ground-0.3V to VDDIO + 0.3V (+3.9V max)
Maximum Operating Voltage (VDDCORE, VDDOSC, VDDPLL and VDDUSB) 1.95V
Maximum Operating Voltage (VDDIO) 3.6V
Total DC Output Current on all I/O lines ..... 350 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

41.2 DC Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C, unless otherwise specified and are certified for a junction temperature up to T_J = 100°C.

Table 41-2. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{VDDCORE}$	DC Supply Core		1.65		1.95	V
V_{VDDBU}	DC Supply Backup		1.65		1.95	
V_{VDDOSC}	DC Supply Oscillator		1.65		1.95	V
V_{VDDPLL}	DC Supply PLL		1.65		1.95	V
V_{VDDUSB}	DC Supply USB		1.65		1.95	V
V_{VDDIO}	DC Supply Peripheral I/Os		3.0		3.6	V
V_{IL}	Input Low-level Voltage		-0.3		+0.8	V
V_{IH}	Input High-level Voltage		2.0		V_{VDDIO}+0.3	V
V_{OL}	Output Low-level Voltage	I_{OL} = 8 mA			0.4	V
		$I_{OL, TDO}$= 2 mA				
V_{OH}	Output High-level Voltage	I_{OH} = 8 mA	V_{VDDIO}-0.4			V
		$I_{OH, TDO}$ = 2 mA				
I_{IL}	Input Leakage Current, Pin Low	Pullup resistors disabled			1	µA
I_{IH}	Input Leakage Current, Pin High	Pullup resistors disabled			1	µA
$R_{PULLUPPIO}$	Pull-up Resistance on PIO pins			190		kΩ

Table 41-2. DC Characteristics (Continued)

$R_{PULLUPCTRL}$	Pull-up Resistance on Control and JTAG pins[1]				13		kΩ
I_O	Output Current					8	mA
$I_{O, TDO}$	Output Current, TDO pin					2	
I_{SC}	Static Current	On $V_{VDDCORE}$ = 1.8V, CPU = 0 Hz All inputs driven; RESET_N=1	T_A =25°C		300		µA
			T_A =85°C			5000	

Note: 1. Includes the TCK, TMS, TDI, OSCEN_N, TRST_N, RESET_N, EVTI_N, and WAKE_N pins.

41.3 Power Consumption

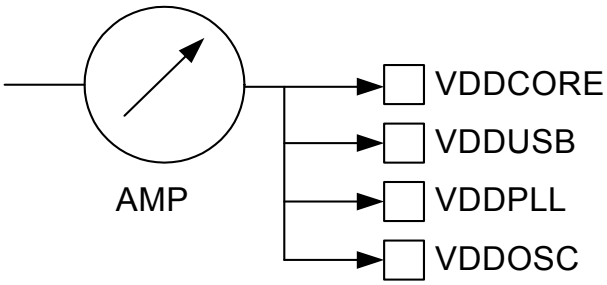
- Typical power consumption of PLLs, Slow Clock and Main Oscillator.
- Power consumption of power supply in Active mode.
- Power consumption by peripheral: calculated as the difference in current measurement after having enabled then disabled the corresponding clock.

41.3.1 Power Consumption versus Modes

The values in Table 41-3 and Table 41-4 on page 932 are measured values of power consumption with operating conditions as follows:

- V_{VDDIO} = 3.3V
- $V_{VDDCORE}$ = V_{VDDUSB}= V_{VDDPLL}= V_{VDDOSC} = 1.8V
- T_A = 25°C
- There is no consumption on the I/Os of the device

Figure 41-1. Measures Schematics



These figures represent the power consumption measured on the power supplies.

Table 41-3. Typical Power Consumption for Different Operating Modes

Mode	Conditions	Typical consumption	Unit
Active[1]	All peripheral clocks deactivated.	500	µA/MHz
Idle	All peripheral clocks activated.	480	
Frozen	All peripheral clocks activated.	280	
Standby	All peripheral clocks activated.	80	

Note: 1. The value is measured at best case condition. Actual current consumption will vary depending on the application.

.

Table 41-4. Power Consumption by Peripheral in Active Mode

Peripheral	Consumption	Unit[1]
PIO Controller	3	µA/MHz
USART	3	
USB	9	
MACB	31	
SMC	1	
SDRAMC	1	
AC97	5	
ISI	3	
Audio DAC	1	
LCDC	31	
TWI	1	
SPI	1	
MCI	7	
SSC	3	
Timer Counter Channels	1	

Note: 1. These numbers are relative to the actual CPU clock frequency, using the standard bus division: HSB and PBB divided by two. PBA divided by four.

41.4 Clock Characteristics

These parameters are given in the following conditions: $V_{VDDCORE}$ = 1.8V, Ambient Temperature = 25°C, unless otherwise specified.

41.4.1 CPU Clock Characteristics

Table 41-5. Guaranteed CPU Clock Frequencies.

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPCPU})$	CPU Clock Frequency (1)	Temp = 85°C, $V_{VDDCORE}$ = 1.8V		150	MHz
$1/(t_{CPCPU})$	CPU Clock Frequency (1)	Temp = 85°C, $V_{VDDCORE}$ = 1.65V		133	MHz

Note: 1. The bus clocks in the system should be divided, relative to the CPU, to be sure they operate in their specified range. The HSB and PBB bus clocks should be divided by two and the PBA bus clock should be divided by four relative to the CPU clock. The division factor of the buses can be set by programming the Power Manager register CKSEL.

Figure 41-2 and Figure 41-3 shows typical maximum CPU frequencies based on a selection of samples from different lots.

Figure 41-2. CPU Clock Frequency vs. $V_{VDDCORE}$ (Typical)

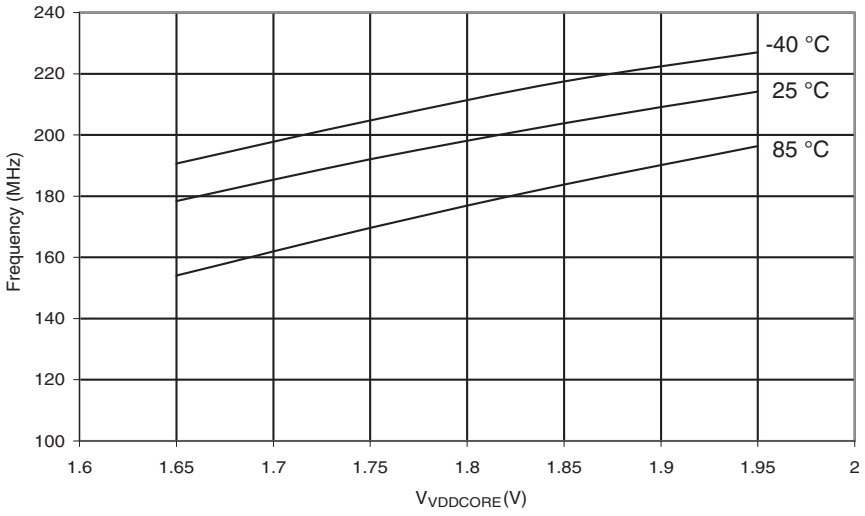
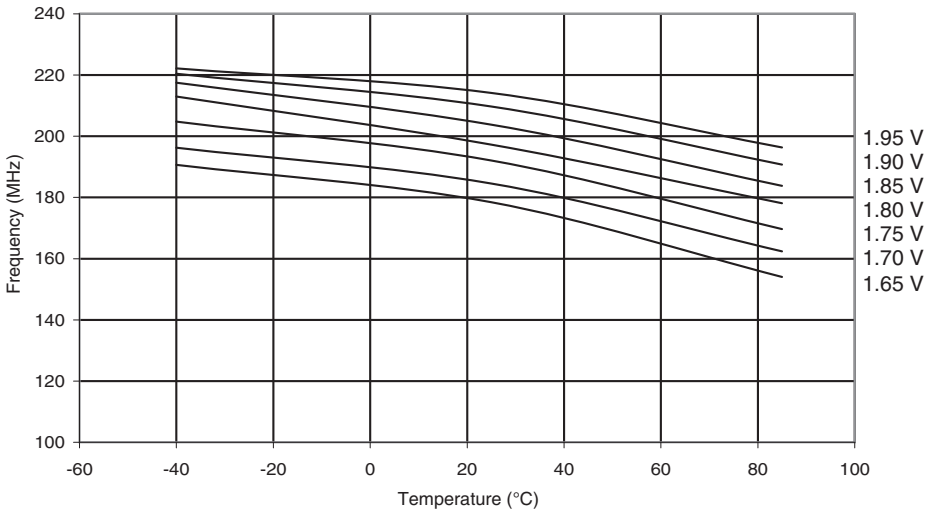


Figure 41-3. CPU Clock Frequency vs. Temperature (Typical)



41.4.2 XIN Clock Characteristics

Table 41-6. XIN Clock Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CPXIN})$	XIN Clock Frequency[1]			50.0	MHz

Note: 1. These characteristics apply only when the Oscillators arein bypass mode (i.e., when OSCEN_N is 1)

41.4.3 RESET_N Characteristics

Table 41-7. RESET_N Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
t_{RESET}	RESET_N minimum pulse length		50		ns

41.5 Crystal Oscillator Characteristics

The following characteristics are applicable to the operating temperature range: T_A = -40°C to 85°C and worst case of power supply, unless otherwise specified.

41.5.1 32 kHz Oscillator Characteristics

Table 41-8. 32 KHz Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CP32KHz})$	Crystal Oscillator Frequency			32 768		Hz
t_{ST}	Startup Time	V_{DDOSC} = 1.8 V R_S = TBD kΩ, C_L = TBD pF(1)		1000		ms

Note: 1. R_S is the equivalent series resistance, C_L is the equivalent load capacitance.

41.5.2 Main Oscillators Characteristics

Table 41-9. Main Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency		10		27	MHz
C_{L1}, C_{L2}	Internal Load Capacitance (C_{L1} = C_{L2})			TBD		pF
t_{ST}	Startup Time			4		ms

Notes: 1. C_S is the shunt capacitance

41.5.3 PLL Characteristics

Table 41-10. Phase Lock Loop Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		80		150	MHz
F_{IN}	Input Frequency		6		32	MHz

Note: 1. Startup time depends on PLL RC filter. A calculation tool is provided by Atmel.

41.6 USB Transceiver Characteristics

41.6.1 Electrical Characteristics

Table 41-11. Electrical Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Levels						
V_{IL}	Low Level				0.8	V
V_{IH}	High Level		2.0			V
V_{DI}	Differential Input Sensivity	|(D+) - (D-)|	0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
C_{IN}	Transceiver capacitance	Capacitance to ground on each line			75	pF
I	Hi-Z State Data Line Leakage	$0V < V_{IN} < 3.3V$	TBD		TBD	µA
R_{EXT}	Recommended External USB Series Resistor	In series with each USB pin with ±5%		39		Ω
Output Levels						
V_{OL}	Low Level Output	Measured with R_L of 1.425 kΩ tied to 3.6V	0		0.3	V
V_{OH}	High Level Output	Measured with R_L of 14.25 kΩ tied to GND	2.8		3.6	V
V_{CRS}	Output Signal Crossover Voltage	Measure conditions described in Figure 41-4	1.3		2.0	V

41.6.2 Switching Characteristics

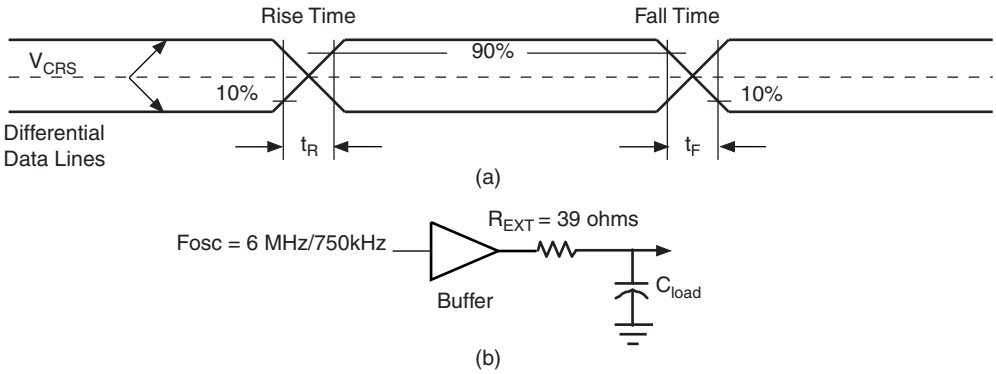
Table 41-12. In Full Speed

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FR}	Transition Rise Time	C_{LOAD} = 50 pF	4		20	ns
t_{FE}	Transition Fall Time	C_{LOAD} = 50 pF	4		20	ns
t_{FRFM}	Rise/Fall time Matching		90		111	%

Table 41-13. In High Speed

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FR}	Transition Rise Time	Specified with test fixture + USB cable	500		TBD	ps
t_{FE}	Transition Fall Time		500		TBD	ps

Figure 41-4. USB Data Signal Rise and Fall Times



41.7 AC Characteristics

41.8 EBI Timings

These timings are given for worst case process, T = 85°C, VDDCORE = 1.65V, VDDIO = 3V and 50 pF load capacitance.

Table 41-14. SMC Clock Signal.

Symbol	Parameter	Max[1]	Units
$1/(t_{CPSMC})$	SMC Controller Clock Frequency	$1/(2t_{cpcpu})$	MHz

Note: 1. The maximum frequenzy of the SMC interface is the same as the max frequnzy for the HSB.

Table 41-15. SMC Read Signals with Hold Settings

Symbol	Parameter	Min	Units
NRD Controlled (READ_MODE = 1)			
SMC_1	Data Setup before NRD High	11.2	ns
SMC_2	Data Hold after NRD High	0	
SMC_3	NRD High to NBS0/A0 Change[1]	nrd hold length * t_{CPSMC} - 1.3	
SMC_4	NRD High to NBS1 Change[1]	nrd hold length * t_{CPSMC} - 1.3	
SMC_5	NRD High to NBS2/A1 Change[1]	nrd hold length * t_{CPSMC} - 1.3	
SMC_6	NRD High to NBS3 Change[1]	nrd hold length * t_{CPSMC} - 1.3	
SMC_7	NRD High to A2 - A25 Change[1]	nrd hold length * t_{CPSMC} - 1.3	
SMC_8	NRD High to NCS Inactive[1]	(nrd hold length - ncs rd hold length) * t_{CPSMC} - 0.6	
SMC_9	NRD Pulse Width	nrd pulse length * t_{CPSMC} - 0.1	
NRD Controlled (READ_MODE = 0)			
SMC_{10}	Data Setup before NCS High	12.4	ns
SMC_{11}	Data Hold after NCS High	0	
SMC_{12}	NCS High to NBS0/A0 Change[1]	ncs rd hold length * t_{CPSMC} - 2.5	
SMC_{13}	NCS High to NBS0/A0 Change[1]	ncs rd hold length * t_{CPSMC} - 2.5	
SMC_{14}	NCS High to NBS2/A1 Change[1]	ncs rd hold length * t_{CPSMC} - 2.5	
SMC_{15}	NCS High to NBS3 Change[1]	ncs rd hold length * t_{CPSMC} - 2.5	
SMC_{16}	NCS High to A2 - A25 Change[1]	ncs rd hold length * t_{CPSMC} - 1.2	
SMC_{17}	NCS High to NRD Inactive[1]	ncs rd hold length - nrd hold length)* t_{CPSMC} - 4.3	
SMC_{18}	NCS Pulse Width	ncs rd pulse length * t_{CPSMC} - 1.5	

Note: 1. hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs rd hold length” or “nrd hold length”.

Table 41-16. SMC Read Signals with no Hold Settings

Symbol	Parameter	Min	Units
NRD Controlled (READ_MODE = 1)			
SMC_{19}	Data Setup before NRD High	15.8	ns
SMC_{20}	Data Hold after NRD High	0	
NRD Controlled (READ_MODE = 0)			
SMC_{21}	Data Setup before NCS High	17.0	ns
SMC_{22}	Data Hold after NCS High	0	

Table 41-17. SMC Write Signals with Hold Settings

Symbol	Parameter	Min	Units
NRD Controlled (READ_MODE = 1)			
SMC_{23}	Data Out Valid before NWE High	(nwe pulse length - 1) * t_{CPSMC} - 1.6	ns
SMC_{24}	Data Out Valid after NWE High(1)	nwe hold length * t_{CPSMC} - 1.5	
SMC_{25}	NWE High to NBS0/A0 Change(1)	nwe hold length * t_{CPSMC} - 1.0	
SMC_{26}	NWE High to NBS1 Change(1)	nwe hold length * t_{CPSMC} - 1.0	
SMC_{29}	NWE High to NBS2/A1 Change(1)	nwe hold length * t_{CPSMC} - 1.0	
SMC_{30}	NWE High to NBS3 Change(1)	nwe hold length * t_{CPSMC} - 1.0	
SMC_{31}	NWE High to A2 - A25 Change(1)	nwe hold length * t_{CPSMC} - 1.6	
SMC_{32}	NWE High to NCS Inactive(1)	(nwe hold length - ncs wr hold length)* t_{CPSMC} - 0.3	
SMC_{33}	NWE Pulse Width	nwe pulse length * t_{CPSMC}	
NRD Controlled (READ_MODE = 0)			
SMC_{34}	Data Out Valid before NCS High	(ncs wr pulse length - 1)* t_{CPSMC} - 1.9	ns
SMC_{35}	Data Out Valid after NCS High(1)	ncs wr hold length * t_{CPSMC} - 3.0	
SMC_{36}	NCS High to NWE Inactive(1)	(ncs wr hold length - nwe hold length)* t_{CPSMC} - 1.5	

Note: 1. hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs wr hold length” or “nwe hold length"

Table 41-18. SMC Write Signals with No Hold Settings (NWE Controlled only).

Symbol	Parameter	Min	Units
SMC_{37}	NWE Rising to A2-A25 Valid	8.0	ns
SMC_{38}	NWE Rising to NBS0/A0 Valid	8.0	
SMC_{39}	NWE Rising to NBS1 Change	8.0	
SMC_{40}	NWE Rising to A1/NBS2 Change	8.0	
SMC_{41}	NWE Rising to NBS3 Change	8.0	
SMC_{42}	NWE Rising to NCS Rising	8.5	
SMC_{43}	Data Out Valid before NWE Rising	(nwe pulse length - 1) * t_{CPSMC} - 4.9	
SMC_{44}	Data Out Valid after NWE Rising	8.4	
SMC_{45}	NWE Pulse Width	nwe pulse length * t_{CPSMC} + 0.3	

Figure 41-5. SMC Signals for NCS Controlled Accesses.

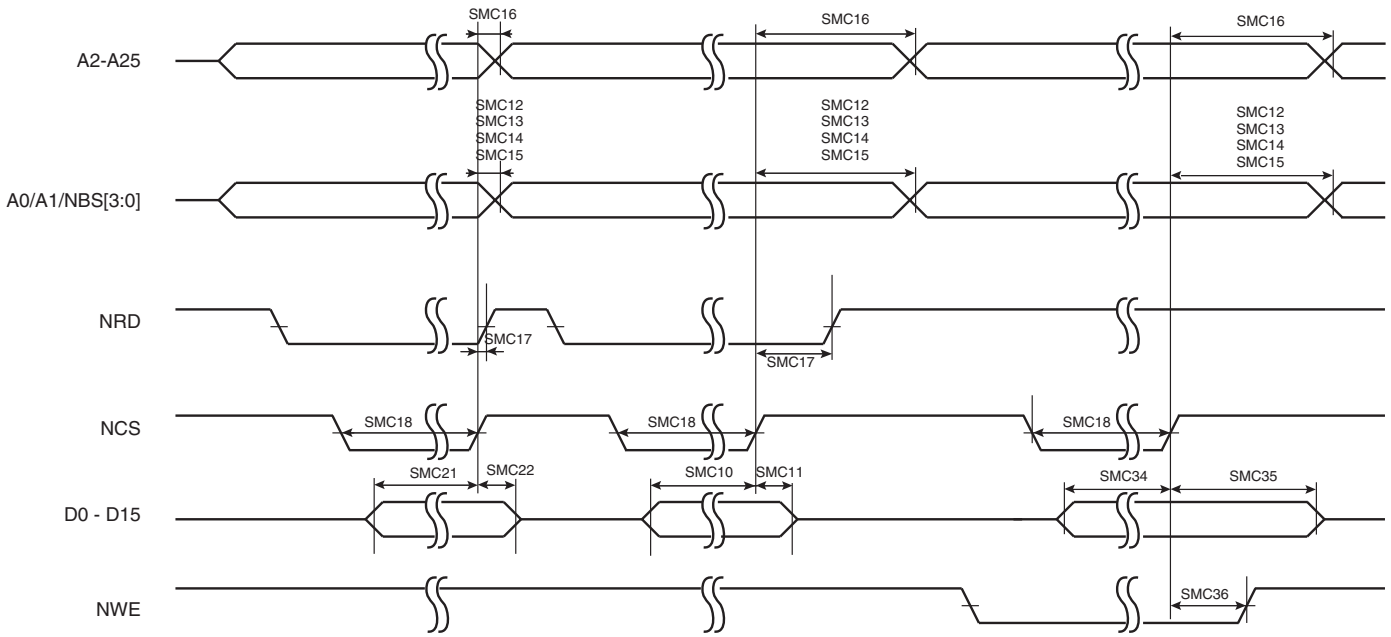
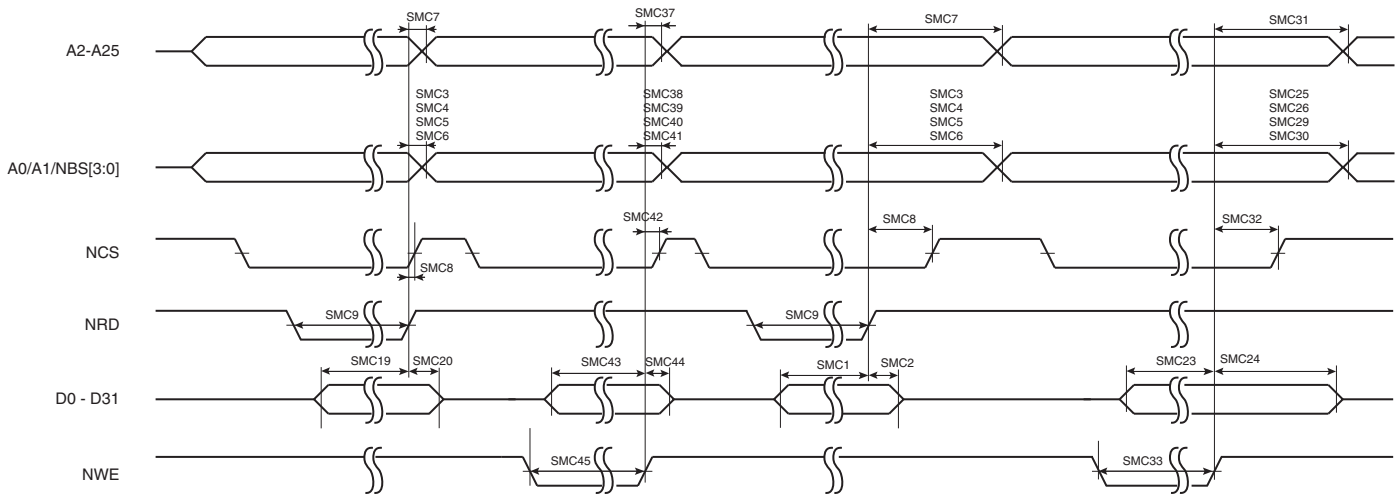


Figure 41-6. SMC Signals for NRD and NRW Controlled Accesses.



41.8.1 SDRAM Signals

These timings are given for 10 pF load on SDCK and 50 pF on other signals.

Table 41-19. SDRAM Clock Signal.

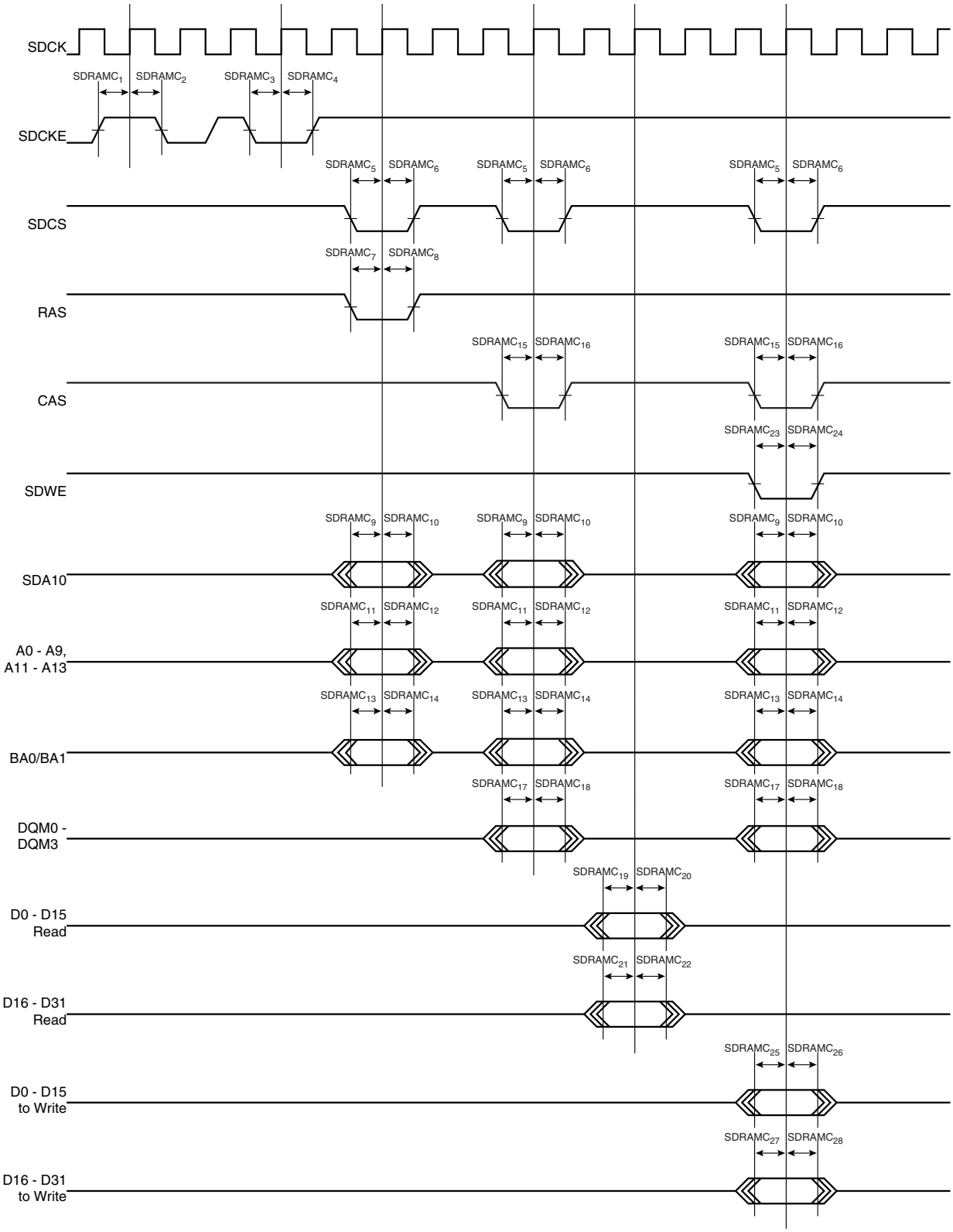
Symbol	Parameter	Max[1]	Units
$1/(t_{CPSDCK})$	SDRAM Controller Clock Frequency	$1/(2t_{cpcpu})$	MHz

Note: 1. The maximum frequenzy of the SDRAMC interface is the same as the max frequnzy for the HSB.

Table 41-20. SDRAM Clock Signal.

Symbol	Parameter	Min	Units
$SDRAMC_1$	SDCKE High before SDCK Rising Edge	6.8	ns
$SDRAMC_2$	SDCKE Low after SDCK Rising Edge	5.8	
$SDRAMC_3$	SDCKE Low before SDCK Rising Edge	6.8	
$SDRAMC_4$	SDCKE High after SDCK Rising Edge	6.2	
$SDRAMC_5$	SDCS Low before SDCK Rising Edge	6.7	
$SDRAMC_6$	SDCS High after SDCK Rising Edge	5.9	
$SDRAMC_7$	RAS Low before SDCK Rising Edge	6.7	
$SDRAMC_8$	RAS High after SDCK Rising Edge	6.9	
$SDRAMC_9$	SDA10 Change before SDCK Rising Edge	6.9	
$SDRAMC_{10}$	SDA10 Change after SDCK Rising Edge	5.7	
$SDRAMC_{11}$	Address Change before SDCK Rising Edge	6.4	
$SDRAMC_{12}$	Address Change after SDCK Rising Edge	4.5	
$SDRAMC_{13}$	Bank Change before SDCK Rising Edge	6.6	
$SDRAMC_{14}$	Bank Change after SDCK Rising Edge	5.2	
$SDRAMC_{15}$	CAS Low before SDCK Rising Edge	7.1	
$SDRAMC_{16}$	CAS High after SDCK Rising Edge	5.9	
$SDRAMC_{17}$	DQM Change before SDCK Rising Edge	6.5	
$SDRAMC_{18}$	DQM Change after SDCK Rising Edge	4.6	
$SDRAMC_{19}$	D0-D15 in Setup before SDCK Rising Edge	2.3	
$SDRAMC_{20}$	D0-D15 in Hold after SDCK Rising Edge	3.9	
$SDRAMC_{21}$	D16-D31 in Setup before SDCK Rising Edge	0.9	
$SDRAMC_{22}$	D16-D31 in Hold after SDCK Rising Edge	4.0	
$SDRAMC_{23}$	SDWE Low before SDCK Rising Edge	6.5	
$SDRAMC_{24}$	SDWE High after SDCK Rising Edge	7.0	
$SDRAMC_{25}$	D0-D15 Out Valid before SDCK Rising Edge	6.2	
$SDRAMC_{26}$	D0-D15 Out Valid after SDCK Rising Edge	4.1	
$SDRAMC_{27}$	D16-D31 Out Valid before SDCK Rising Edge	6.2	
$SDRAMC_{28}$	D16-D31 Out Valid after SDCK Rising Edge	4.5	

Figure 41-7. SDRAMC Signals relative to SDCK.



42. Ordering Information

Table 42-1. Ordering Information

Ordering Code	Package	Package Type	Packing	Temperature Operating Range
AT32AP7000-CTUR	CTBGA256	Green	Reel	Industrial (-40°C to 85°C)
AT32AP7000-CTUT	CTBGA256	Green	Tray	Industrial (-40°C to 85°C)

43. Errata

43.1 Rev. C

1. **SPI FDIV option does not work**
   Selecting clock signal using FDIV = 1 does not work as specified.

   Fix/Workaround
   Do not set FDIV = 1.

2. **SPI Chip Select 0 BITS field overrides other Chip Selects**
   The BITS field for Chip Select 0 overrides BITS fields for other Chip selects.

   Fix/Workaround
   Update Chip Select 0 BITS field to the relevant settings before transmitting with Chip Selects other than 0.

3. **SPI LASTXFER may be overwritten**
   When Peripheral Select (PS) = 0, the LASTXFER-bit in the Transmit Data Register (TDR) should be internally discared. This fails and may cause problems during DMA transfers. Transmitting data using the PDC when PS=0, the size of the transferred data is 8- or 16-bits. The upper 16 bits of the TDR will be written to a random value. If Chip Select Active After Transfer (CSAAT) = 1, the behavior of the Chip Select will be unpredictable.

   Fix/Workaround
   - Do not use CSAAT = 1 if PS = 0

   - Use GPIO to control Chip Select lines

   - Select PS=1 and store data for PCS and LASTXFER for each data in transmit buffer.

4. **SPI LASTXFER overrides Chip Select**
   The LASTXFER bit overrides Chip Select input when PS = 0 and CSAAT is used.

   Fix/Workaround
   - Do not use the CSAAT

   - Use GPIO as Chip Select input

   - Select PS = 1. Transfer 32-bit with correct LASTXFER settings.

5. **MMC data write operation with less than 12 bytes is impossible.**
   MCI data write operation with less than 12 bytes is impossible. The Data Write operation with a number of bytes less than 12 leaves the internal MCI FIFO in an inconsistent state. Subsequent reads and writes will not function properly.

   Fix/Workaround
   Always transfer 12 or more bytes at a time. If less than 12 bytes are transferred, the only recovery mechanism is to perform a software reset of the MCI.

6. **MMC SDIO interrupt only works for slot A**
   If 1-bit data bus width and on other slots than slot A, the SDIO interrupt can not be captured.

Fix/Workaround

Use slot A.

7. **PSIF TXEN/RXEN may disable the transmitter/receiver**

Writing a '0' to RXEN will disable the receiver. Writing '0' to TXEN will disable the transmitter.

Fix/Workaround

When accessing the PS/2 Control Register always write '1' to RXEN to keep the receiver enabled, and write '1' to TXEN to keep the transmitter enabled.

8. **PSIF TXRDY interrupt corrupts transfers**

When writing to the Transmit Holding Register (THR), the data will be transferred to the data shift register immediately, regardless of the state of the data shift register. If a transfer is ongoing, it will be interrupted and a new transfer will be started with the new data written to THR.

Fix/Workaround

Use the TXEMPTY-interrupt instead of the TXRDY-interrupt to update the THR. This ensures that a transfer is completed.

9. **LCD memory error interupt does not work**

Writing to the MERIT-bit in the LCD Interrupt Test Register (ITR) does not cause an interrupt as intended. The MERIC-bit in the LCD Interrupt Clear Register (ICR) cannot be written. This means that if the MERIS-bit in ISR is set, it cannot be cleared.

Fix/Workaround

Memory error interrupt should not be used.

10. **PWM counter restarts at 0x0001**

The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

Fix/Workaround

- The first period is 0x0000, 0x0001, ..., period

- Consecutive periods are 0x0001, 0x0002, ..., period

11. **PWM channel interrupt enabling triggers an interrupt**

When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

Fix/Workaround

When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

12. **PWM update period to a 0 value does not work**

It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

Fix/Workaround

Do not update the PWM_CUPD register with a value equal to 0.

13. **PWM channel status may be wrong if disabled before a period has elapsed**

Before a PWM period has elapsed, the read channel status may be wrong. The CHIDx-bit for a PWM channel in the PWM Enable Register will read '1' for one full PWM period even if the channel was disabled before the period elapsed. It will then read '0' as expected.

Fix/Workaround

Reading the PWM channel status of a disabled channel is only correct after a PWM period

14. **TWI transfer error without ACK**

If the TWI does not receive an ACK from a slave during the address+R/W phase, no bits in the status register will be set to indicate this. Hence, the transfer will never complete.

Fix/Workaround

To prevent errors due to missing ACK, the software should use a timeout mechanism to terminate the transfer if this happens.

15. **SSC can not transmit or receive data**

The SSC can not transmit or receive data when CKS = CKDIV and CKO = none in TCMR or RCMR respectively.

Fix/Workaround

Set CKO to a value that is not "None" and enable the PIO with output driver disabled on the TK/RK pin.

16. **USART - RXBREAK flag is not correctly handled**

The FRAME_ERROR is set instead of the RXBREAK when the break character is located just after the STOP BIT(S) in ASYNCHRONOUS mode.

Fix/Workaround

The transmitting UART must set timeguard greater than 0.

17. **USART - Manchester encoding/decoding is not working.**

Manchester encoding/decoding is not working.

Fix/Workaround

Do not use manchester encoding.

18. **SPI - Disabling SPI has no effect on TDRE flag.**

Disabling SPI has no effect on TDRE whereas the write data command is filtered when SPI is disabled. This means that as soon as the SPI is disabled it becomes impossible to reset the TDRE flag by writing in the SPI_TDR. So if the SPI is disabled during a PDC transfer, the PDC will continue to write data in the SPI_TDR (as TDRE keeps High) till its buffer is empty, and all data written after the disable command is lost.

Fix/Workaround

Disable PDC, 2 NOP (minimum), Disable SPI. When you want to continue the transfer: Enable SPI, Enable PDC.

19. **SPI disable does not work in SLAVE mode.**

SPI disable does not work in SLAVE mode.

Fix/Workaround

Read the last received data, then perform a Software Reset.

20. SCC - First Data transmitted after reset is not DATDEF.

In the first frame transmitted, the first transmitted data that follows the frame synchro is 0, not DATDEF. This happens when:

1. PDC is disabled
2. Reset the SSC
3. Configure the SSC with a transmit START condition different from CONTINUOUS (START = 0)
4. DATDEF = 1
5. Enable the SSC in transmission.

This trouble only appears after a reset and it is only the first frame is affected.

Fix/Workaround

Use the PDC to fill the THR after the enable of the SSC and before the start of the frame.

21. MCI - False data timeout error DTOE may occur.

If a small block (5 bytes) is read through the READ_SINGLE_BLOCK command (CMD17), the flag NOTBUSY will be set and a false data timeout error DTOE occurs.

Fix/Workaround

None.

22. SDRAM - Self-refresh mode

If Entry in Self-refresh mode is followed by SDRAM access and auto-refresh event, TRC timing is not checked for AUTO_REFRESH sequence.

Fix/Workaround

Set the value of TRAS field in user interface with TRC+1.

23. SPI - No TX UNDERRUN flag available

There is no TX UNDERRUN flag available, therefore in slave mode there is no way to be informed of a character lost in transmission.

Fix/Workaround

PDC/PDCA transfers: None.

Manual transfers (no PDC and TX slave only): Read the RHR every time the THR is written. The OVRS flag of the status register will track any UNDERRUN on the TX side.

24. HMATRIX - Fixed priority arbitration does not work

Fixed priority arbitration does not work.

Fix/Workaround

Use Round-robin arbitration instead.

25. OSC32 is not available for RTC, WDT, TIMERs and USARTs at startup

Right after startup the osc32 clock to internal modules is not valid. The osc32 clock will be valid for use approximately 128 osc32 cycles after the the first instruction is executed. This has consequences if you are planning to use the RTC, WDT, going into sleep mode and USARTs with SCK and TCs with TIMER_CLOCK0.

Fix/Workaround

Before executing any code the user should enable the RTC with the smallest prescaler and poll that the RTC is counting before doing anything in your program. Another way to ensure that the osc32 is valid is to use interrupts with TOP=1.

Example:

```
//reset the counter register
  AVR32_RTC.val = 0x0;
//enable the RTC with the smallest prescaler
  AVR32_RTC.ctrl = 0x1;
//wait until the value increases
  while(AVR32_RTC.val == 0);
```

26. SPI can generate a false RXREADY signal in SLAVE mode

In slave mode the SPI can generate a false rxready signal during enabling of the SPI or during the first transfer.

Fix/Workaround

1. Set slave mode, set required CPOL/CPHA
2. Enable SPI
3. Set the polarity CPOL of the line in the opposite value of the required one
4. Set the polarity CPOL to the required one.
5. Read the RXHOLDING register

Transfers can now begin and RXREADY will now behave as expected.

27. EBI address lines 23, 24, and 25 are pulled up when booting up

After reset the EBI address lines 23, 24 and 25 are tristated with pullups. Booting from a flash larger than 8 MB using these lines will fail, as the flash will be accessed with these address bits set.

Fix/Workaround

Add external pulldown resistors (5 kΩ) on these lines if booting from a flash larger than 8 MB using these address lines.

28. SSC - Additional delay on TD output

A delay from 2 to 3 system clock cycles is added to TD output when:

TCMR.START = Receive Start,

TCMR.STTDLY = more than ZERO,

RCMR.START = Start on falling edge / Start on Rising edge / Start on any edge

RFMR.FSOS = None (input)

Fix/Workaround

None.

29. SSC - TF output is not correct

TF output is not correct (at least emitted one serial clock cycle later than expected) when:

TFMR.FSOS = Driven Low during data transfer/ Driven High during data transfer

TCMR.START = Receive start

RFMR.FSOS = None (Input)

RCMR.START = any on RF (edge/level)

Fix/Workaround

None.

30. **USART - TXD signal is floating in Modem and Hardware Handshaking mode**

The TXD signal is floating in Modem and Hardware Handshaking mode, but should be pulled up.

Fix/Workaround

Enable pullup on this line in the PIO.

31. **PWM - Impossible to update a period equal to 0 by using the CUPD register**

It is impossible to UPDATE a period equal to 0 by the using of the UPDATE register (CUPD).

Fix/Workaround

To update a period equal to 0, write directly to the CPRD register.

32. **WDT Clear is blocked after WDT Reset**

A watchdog timer event will, after reset, block writes to the WDT_CLEAR register, preventing the program to clear the next Watchdog Timer Reset.

Fix/Workaround

If the RTC is not used a write to AVR32_RTC.ctrl.pclr = 1, instead of writing to AVR32_WDT.clr, will reset the prescaler and thus prevent the watchdog event from happening. This will render the RTC useless, but prevents WDT reset because the RTC and WDT share the same prescaler. Another sideeffect of this is that the watchdog timeout period will be half the expected timeout period.

If the RTC is used one can disable the Watchdog Timer (WDT) after a WDT reset has occured. This will prevent the WDT resetting the system. To make the WDT functional again a hard reset (power on reset or RESET_N) must be applied. If you still want to use the WDT after a WDT reset a small code can be inserted at the startup checking the AVR32_PM.rcause register for WDT reset and use a GPIO pin to reset the system. This method requires that one of the GPIO pins are available and connected externally to the RESET_N pin. After the GPIO pin has pulled down the reset line the GPIO will be reset and leave the pin tristated with pullup.

33. **USART - The DCD Signal is active high from the USART, but should be active low**

The DCD signal is active high from the USART, but should be active low.

Fix/Workaround

An inverter should be added on this line on the PCB.

34. **MCI Transmit Data Register (TDR) FIFO corruption**

If the number of bytes to be transmitted by the MCI is not a multiple of 4, the Transmit Data Register (TDR) First In First Out data buffer control logic will become corrupted when transmit data is written to the TDR as 32-bit values.

Fix/Workaround

Configure the MCI Mode Register (MR) to accept 8-bit data input by writing a 1 to bit 13 (FBYTE), and transfer each byte of the transmit data to TDR by right aligning the useful value. This allows the number of bytes transferred into the TDR to match the number set up in the BCNT field of the MCI Block Register (BLKR).

35. **Unreliable branch folding**
    In certain situations, branch folding does not work as expected.

    Fix/Workaround
    Write 0 to CPUCR.FE before executing any branch instructions after reset.

36. **USB PLL jitter may cause packet loss during USB hi-speed transmission**
    The USB Hi-speed PLL accuracy is not sufficient for Isochronous USB hi-speed transmission and may cause packet loss. The observed bit-loss is typically < 125 ppm.

    Fix/Workaround
    Do not use isochronous mode if absolute data accuracy is critical.

43.2 Rev. B

Not sampled.

43.3 Rev. A

1. **SPI FDIV option does not work**
    Selecting clock signal using FDIV = 1 does not work as specified.

    Fix/Workaround
    Do not set FDIV = 1.

2. **SPI Chip Select 0 BITS field overrides other Chip Selects**
    The BITS field for Chip Select 0 overrides BITS fields for other Chip selects.

    Fix/Workaround
    Update Chip Select 0 BITS field to the relevant settings before transmitting with Chip Selects other than 0.

3. **SPI LASTXFER may be overwritten**
    When Peripheral Select (PS) = 0, the LASTXFER-bit in the Transmit Data Register (TDR) should be internally discared. This fails and may cause problems during DMA transfers. Transmitting data using the PDC when PS=0, the size of the transferred data is 8- or 16-bits. The upper 16 bits of the TDR will be written to a random value. If Chip Select Active After Transfer (CSAAT) = 1, the behavior of the Chip Select will be unpredictable.

    Fix/Workaround
    - Do not use CSAAT = 1 if PS = 0
    - Use GPIO to control Chip Select lines
    - Select PS=1 and store data for PCS and LASTXFER for each data in transmit buffer.

4. **MMC data write operation with less than 12 bytes is impossible.**

MCI data write operation with less than 12 bytes is impossible. The Data Write operation with a number of bytes less than 12 leaves the internal MCI FIFO in an inconsistent state. Subsequent reads and writes will not function properly.

Fix/Workaround

Always transfer 12 or more bytes at a time. If less than 12 bytes are transferred, the only recovery mechanism is to perform a software reset of the MCI.

5. **MMC SDIO interrupt only works for slot A**

   If 1-bit data bus width and on other slots than slot A, the SDIO interrupt can not be captured.

   Fix/Workaround

   Use slot A.

6. **PSIF TXEN/RXEN may disable the transmitter/receiver**

   Writing a '0' to RXEN will disable the receiver. Writing '0' to TXEN will disable the transmitter.

   Fix/Workaround

   When accessing the PS/2 Control Register always write '1' to RXEN to keep the receiver enabled, and write '1' to TXEN to keep the transmitter enabled.

7. **PSIF TXRDY interrupt corrupts transfers**

   When writing to the Transmit Holding Register (THR), the data will be transferred to the data shift register immediately, regardless of the state of the data shift register. If a transfer is ongoing, it will be interrupted and a new transfer will be started with the new data written to THR.

   Fix/Workaround

   Use the TXEMPTY-interrupt instead of the TXRDY-interrupt to update the THR. This ensures that a transfer is completed.

8. **PSIF Status Register bits return 0**

   The PARITY, NACK and OVRUN bits in the PSIF Status Register cannot be read. Reading these bits will always return zero.

   Fix/Workaround

   None

9. **PSIF Transmit does not work as intended**

   While PSIF receiving works, transmitting using the PSIF does not work.

   Fix/Workaround

   Do not transmit using the PSIF.

10. **LCD memory error interupt does not work**

    Writing to the MERIT-bit in the LCD Interrupt Test Register (ITR) does not cause an interrupt as intended. The MERIC-bit in the LCD Interrupt Clear Register (ICR) cannot be written. This means that if the MERIS-bit in ISR is set, it cannot be cleared.

    Fix/Workaround

    Memory error interrupt should not be used.

11. PWM counter restarts at 0x0001

The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

Fix/Workaround

- The first period is 0x0000, 0x0001, ..., period

- Consecutive periods are 0x0001, 0x0002, ..., period

12. PWM channel interrupt enabling triggers an interrupt

When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

Fix/Workaround

When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

13. PWM update period to a 0 value does not work

It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

Fix/Workaround

Do not update the PWM_CUPD register with a value equal to 0.

14. PWM channel status may be wrong if disabled before a period has elapsed

Before a PWM period has elapsed, the read channel status may be wrong. The CHIDx-bit for a PWM channel in the PWM Enable Register will read '1' for one full PWM period even if the channel was disabled before the period elapsed. It will then read '0' as expected.

Fix/Workaround

Reading the PWM channel status of a disabled channel is only correct after a PWM period has elapsed.

15. Power Manager DIVEN-bit cannot be read

The DIVEN-bit in the Generic Clock Control Register in the Power Manager cannot be read. Reading the register will give a wrong value for DIVEN. Writing to DIVEN works as intended.

Fix/Workaround

Do not read DIVEN. If needed, the written value must be store elsewhere.

16. Watchdog Timer cannot wake the part from sleep

When the CPU has entered sleep mode, the watchdog timer will not be able to reset the system if a watchdog reset occurs. The problem is valid for all sleep modes.

Fix/Workaround

None.

17. Peripherals connected to wrong clock signal

The frequency of the divided clocks for the SPI and the USART is set by the clock configuration for peripheral bus B (PBB) and not by peripheral bus A.

Fix/Workaround

Use clock settings for PBB for the SPI and USART.

18. JTAG CLAMP instruction does not work as intended

During the CLAMP instruction, the Boundary Scan register should be stable and only the BYPASS register selected. Instead, the bscan register will capture and shift as if it was selected, reducing the usefulness of the CLAMP instruction.

Fix/Workaround

None.

19. High current consumption in reset with no clocks enabled

In connection with the datacache RAM access, a higher current consumption than expected can be observed during reset. The error is non-functional and does not affect reliability of the device.

Fix/Workaround

Via software, access the datacache RAM every 100 µs. This prevents the increased current consumption. Example code:

```
mov     r11, lo(0x24002000)
orh     r11, hi(0x24002000)
ld.w    r11, r11[0]         //access first RAM
mov     r10, lo(0x24000000)
orh     r10, hi(0x24000000)
ld.w    r10, r10[0]         //access second RAM
```

20. TWI transfer error without ACK

If the TWI does not receive an ACK from a slave during the address+R/W phase, no bits in the status register will be set to indicate this. Hence, the transfer will never complete.

Fix/Workaround

To prevent errors due to missing ACK, the software should use a timeout mechanism to terminate the transfer if this happens.

21. SSC can not transmit or receive data

The SSC can not transmit or receive data when CKS = CKDIV and CKO = none in TCMR or RCMR respectively.

Fix/Workaround

Set CKO to a value that is not "None" and enable the PIO with output driver disabled on the TK/RK pin.

22. USART - RXBREAK flag is not correctly handled

The FRAME_ERROR is set instead of the RXBREAK when the break character is located just after the STOP BIT(S) in ASYNCHRONOUS mode.

Fix/Workaround

The transmitting UART must set timeguard greater than 0.

23. USART - Manchester encoding/decoding is not working.

Manchester encoding/decoding is not working.

Fix/Workaround

Do not use manchester encoding.

24. SPI - Disabling SPI has no effect on TDRE flag.

Disabling SPI has no effect on TDRE whereas the write data command is filtered when SPI is disabled. This means that as soon as the SPI is disabled it becomes impossible to reset the TDRE flag by writing in the SPI_TDR. So if the SPI is disabled during a PDC transfer, the PDC will continue to write data in the SPI_TDR (as TDRE keeps High) till its buffer is empty, and all data written after the disable command is lost.

Fix/Workaround

Disable PDC, 2 NOP (minimum), Disable SPI. When you want to continue the transfer: Enable SPI, Enable PDC.

25. SPI disable does not work in SLAVE mode.

SPI disable does not work in SLAVE mode.

Fix/Workaround

Read the last received data, then perform a Software Reset.

26. SCC - First Data transmitted after reset is not DATDEF.

In the first frame transmitted, the first transmitted data that follows the frame synchro is 0, not DATDEF. This happens when:

1. PDC is disabled

2. Reset the SSC

3. Configure the SSC with a transmit START condition different from CONTINUOUS (START = 0)

4. DATDEF = 1

5. Enable the SSC in transmission.

This trouble only appears after a reset and it is only the first frame is affected.

Fix/Workaround

Use the PDC to fill the THR after the enable of the SSC and before the start of the frame.

27. MCI - False data timeout error DTOE may occur.

If a small block (5 bytes) is read through the READ_SINGLE_BLOCK command (CMD17), the flag NOTBUSY will be set and a false data timeout error DTOE occurs.

Fix/Workaround

None.

28. SDRAM - Self-refresh mode

If Entry in Self-refresh mode is followed by SDRAM access and auto-refresh event, TRC timing is not checked for AUTO_REFRESH sequence.

Fix/Workaround

Set the value of TRAS field in user interface with TRC+1.

29. SPI - No TX UNDERRUN flag available

There is no TX UNDERRUN flag available, therefore in slave mode there is no way to be informed of a character lost in transmission.

Fix/Workaround

PDC/PDCA transfers: None.

Manual transfers (no PDC and TX slave only): Read the RHR every time the THR is written. The OVRS flag of the status register will track any UNDERRUN on the TX side.

30. HMATRIX - Fixed priority arbitration does not work

Fixed priority arbitration does not work.

Fix/Workaround

Use Round-robin arbitration instead.

31. OSC32 is not available for RTC, WDT, TIMERs and USARTs at startup

Right after startup the osc32 clock to internal modules is not valid. The osc32 clock will be valid for use approximately 128 osc32 cycles after the the first instruction is executed. This has consequences if you are planning to use the RTC, WDT, going into sleep mode and USARTs with SCK and TCs with TIMER_CLOCK0.

Fix/Workaround

Before executing any code the user should enable the RTC with the smallest prescaler and poll that the RTC is counting before doing anything in your program. Another way to ensure that the osc32 is valid is to use interrupts with TOP=1.

Example:

```
//reset the counter register
  AVR32_RTC.val = 0x0;
//enable the RTC with the smallest prescaler
  AVR32_RTC.ctrl = 0x1;
//wait until the value increases
  while(AVR32_RTC.val == 0);
```

32. SPI can generate a false RXREADY signal in SLAVE mode

In slave mode the SPI can generate a false rxready signal during enabling of the SPI or during the first transfer.

Fix/Workaround

1. Set slave mode, set required CPOL/CPHA
2. Enable SPI
3. Set the polarity CPOL of the line in the opposite value of the required one
4. Set the polarity CPOL to the required one.
5. Read the RXHOLDING register

Transfers can now begin and RXREADY will now behave as expected.

33. EBI address lines 23, 24, and 25 are pulled up when booting up

After reset the EBI address lines 23, 24 and 25 are tristated with pullups. Booting from a flash larger than 8 MB using these lines will fail, as the flash will be accessed with these address bits set.

Fix/Workaround

Add external pulldown resistors (5 kΩ) on these lines if booting from a flash larger than 8 MB using these address lines.

34. SSC - Additional delay on TD output

A delay from 2 to 3 system clock cycles is added to TD output when:

TCMR.START = Receive Start,

TCMR.STTDLY = more than ZERO,

RCMR.START = Start on falling edge / Start on Rising edge / Start on any edge

RFMR.FSOS = None (input)

Fix/Workaround

None.

35. SSC - TF output is not correct

TF output is not correct (at least emitted one serial clock cycle later than expected) when:

TFMR.FSOS = Driven Low during data transfer/ Driven High during data transfer

TCMR.START = Receive start

RFMR.FSOS = None (Input)

RCMR.START = any on RF (edge/level)

Fix/Workaround

None.

36. USART - TXD signal is floating in Modem and Hardware Handshaking mode

The TXD signal is floating in Modem and Hardware Handshaking mode, but should be pulled up.

Fix/Workaround

Enable pullup on this line in the PIO.

37. PWM - Impossible to update a period equal to 0 by using the CUPD register

It is impossible to UPDATE a period equal to 0 by the using of the UPDATE register (CUPD).

Fix/Workaround

To update a period equal to 0, write directly to the CPRD register.

38. WDT Clear is blocked after WDT Reset

A watchdog timer event will, after reset, block writes to the WDT_CLEAR register, preventing the program to clear the next Watchdog Timer Reset.

Fix/Workaround

If the RTC is not used a write to AVR32_RTC.ctrl.pclr = 1, instead of writing to AVR32_WDT.clr, will reset the prescaler and thus prevent the watchdog event from happening. This will render the RTC useless, but prevents WDT reset because the RTC and WDT share the same prescaler. Another sideeffect of this is that the watchdog timeout period will be half the expected timeout period.

If the RTC is used one can disable the Watchdog Timer (WDT) after a WDT reset has occured. This will prevent the WDT resetting the system. To make the WDT functional again a hard reset (power on reset or RESET_N) must be applied. If you still want to use the WDT after a WDT reset a small code can be inserted at the startup checking the AVR32_PM.rcause register for WDT reset and use a GPIO pin to reset the system. This method requires that one of the GPIO pins are available and connected externally to the

RESET_N pin. After the GPIO pin has pulled down the reset line the GPIO will be reset and leave the pin tristated with pullup.

39. USART - The DCD Signal is active high from the USART, but should be active low

The DCD signal is active high from the USART, but should be active low.

Fix/Workaround

An inverter should be added on this line on the PCB.

40. MCI Transmit Data Register (TDR) FIFO corruption

If the number of bytes to be transmitted by the MCI is not a multiple of 4, the Transmit Data Register (TDR) First In First Out data buffer control logic will become corrupted when transmit data is written to the TDR as 32-bit values.

Fix/Workaround

Configure the MCI Mode Register (MR) to accept 8-bit data input by writing a 1 to bit 13 (FBYTE), and transfer each byte of the transmit data to TDR by right aligning the useful value. This allows the number of bytes transferred into the TDR to match the number set up in the BCNT field of the MCI Block Register (BLKR).

41. Unreliable branch folding

In certain situations, branch folding does not work as expected.

Fix/Workaround

Write 0 to CPUCR.FE before executing any branch instructions after reset.

42. USB PLL jitter may cause packet loss during USB hi-speed transmission

The USB Hi-speed PLL accuracy is not sufficient for Isochronous USB hi-speed transmission and may cause packet loss. The observed bit-loss is typically < 125 ppm.

Fix/Workaround

Do not use isochronous mode if absolute data accuracy is critical.

44. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

44.1 Rev. M 09/09

1. Updated ”Errata” on page 945.

44.2 Rev. L 09/09

1. Updated ”Errata” on page 945.

44.3 Rev. K 09/07

1. PIO Controller C Multiplexing table updated in ”Peripherals” on page 75“.
2. Added section ”USBA” on page 81 in Clock Connections in ”Peripherals” on page 75.
3. USBA feature list updated in ”Peripherals” on page 75.
4. Renamed clk_slow to clk_osc32 in Table 9-4 on page 80.
5. Updated organisation of User Interface in ”HSB Bus Matrix (HMATRIX)” on page 144.
6. Updated special bus granting mechanism in ”HSB Bus Matrix (HMATRIX)” on page 144.
7. Added product dependencies in ”DMA Controller (DMACA)” on page 174.
8. Added product dependencies in ”Peripheral DMA Controller (PDC)” on page 237.
9. Added description of multi-drive in ”Parallel Input/Output Controller (PIO)” on page 253.
10. Added MDER/MDDR/MDSR to pin logic diagram in ”Parallel Input/Output Controller (PIO)” on page 253.
11. SPI pins must be enabled to use local loopback.
12. Updated description of the OVRES bit in ”Serial Peripheral Interface (SPI)” on page 293.
13. Updated bit description of TXEMPTY in the ”USART Channel Status Register” on page 435.
14. Number of chip select lines updatedin figures and tables, changed from 8 to 6 in ”Static Memory Controller (SMC)” on page 492.
15. Made the MDR register Read/Write instead of Read in ”SDRAM Controller (SDRAMC)” on page 534.
16. Removed the PWSEN and PWSDIS bits from the ”Control Register” on page 588.
17. Added PDCFBYTE and removed the PWSDIV bits from the ”Control Register” on page 588
18. Added note about terminating the transfers in sleep modes in product dependencies in ”Ethernet MAC (MACB)” on page 606.
19. Added note about reading the Status Register clears the interrupt flag in ”Timer/Counter (TC)” on page 740.
20. Added debug operation to product dependencies in ”Timer/Counter (TC)” on page 740.
21. Added debug operation to product dependencies in ”Pulse Width Modulation Controller (PWM)” on page 777.

22. Consistently used the term LCDC Core Clock through the document when referring to the generic clock that drives the LCD Core and is used to generate PCLK and the other LCD synchronization signals.
23. Updated typos in ”LCD Controller (LCDC)” on page 803.
24. Rewritten the Register Configuration Guide and renamed it “Register Configuration Example“ in ”LCD Controller (LCDC)” on page 803.
25. Updated formula for pixel clock in ”LCD Control Register 1” on page 846.
26. Updated HOZVAL description in ”LCD Frame Configuration Register” on page 851.
27. Updated ”PLL Characteristics” on page 935.
28. Updated ”Errata” on page 945.

44.4 Rev. J 07/07

1. USB Signals updated in ”Signals Description” on page 4.
2. The PX0 - PX53 Signals added in ”Signals Description” on page 4.
3. SDCS signals removed from PIO Controller Multiplexing tables in ”Peripherals” on page 75.
4. SDCS1 signal removed from figures and tables, and SDCS0 renamed to SDCS in ”External Bus Interface (EBI)” on page 157.
5 SmartMedia renamed to NAND Flash in some description to avoid confusion in ”External Bus Interface (EBI)” on page 157.
6. Updated the reset state of the SMC Mode register in Table 27-9 on page 523.
7. Updated ”Mechanical Characteristics” on page 927.
8. Updated pad parameters in ”DC Characteristics” on page 930.
9 Updated pad parameters in ”Clock Characteristics” on page 933.
10. Updated ”USB Transceiver Characteristics” on page 936.
11. Updated ”EBI Timings” on page 938.

44.5 Rev. I 04/07

1. Updated ”Features” on page 1.
2. Updated tables in ”Signals Description” on page 4.
3. Updated Table 9-2 on page 77, Table 9-9 on page 82, and Table 9-9 on page 82 in the ”Peripherals” on page 75.
4. Updated module names and abbreviations through the datasheet.

44.6 Rev. H 02/07

1. Updated ”Features” on page 1.
2. Updated ”Part Description” on page 2.
3. Added VBG pin in ”Signals Description” on page 4.
3. Changed direction in the EVTI_N signal in ”Signals Description” on page 4.
4. Updated ”Blockdiagram” on page 13.
5. Updated Registers in ”Power Manager (PM)” on page 96.

6. “Pulling OSCEN_N low” replaced by “Pulling OSCEN_N high” in ”32 KHz oscillator operation” on page 98.
7. Added note in ”32 KHz oscillator operation” on page 98.
8. Updated register names in ”Real Time Counter (RTC)” on page 120.
9. Updated register names in ”Watchdog Timer (WDT)” on page 127.
10. Updated register descriptions in ”HSB Bus Matrix (HMATRIX)” on page 144.
11. Updated CFRNW to a separate signal in ”External Bus Interface (EBI)” on page 157.
12. Updated register descriptions in ”DMA Controller (DMACA)” on page 174.
13. Added registers and updated register descriptions in ”Parallel Input/Output Controller (PIO)” on page 253.
14. Updated bit names in ”Serial Peripheral Interface (SPI)” on page 293.
15. Updated flow charts in ”Two-wire Interface (TWI)” on page 322.
16. Updated bit name in the PSR register in ”PS/2 Module (PSIF)” on page 340.
17. Added second instance of ps2 interface in ”PS/2 Module (PSIF)” on page 340.
18. Updated register descriptions in ”Synchronous Serial Controller (SSC)” on page 352.
19. Updated register names in ”Static Memory Controller (SMC)” on page 492.
20. Updated register names in ”Error Corrected Code (ECC) Controller” on page 562.
21. Updated register descriptions in ”Ethernet MAC (MACB)” on page 606.
22. Updated register descriptions in ”LCD Controller (LCDC)” on page 803.
23. Updated register descriptions in ”Image Sensor Interface (ISI)” on page 873.
24. Removed JTAG specification references in ”Debug and Test” on page 909.
25. Updated ”Electrical Characteristics” on page 930.
26. Updated memory locations.

44.7 Rev. G 10/06

1. Package text changed from CABGA to CTBGA.
2. Occurrences of APB and AHB changed to Peripheral Bus (PB) and High Speed Bus (HSB) respectively.
3. Updated ”Hi-Speed USB Interface (USBA)” on page 666.
4. Added ”Errata” on page 945.

44.8 Rev. F 07/06

1. Removed 150CGU from ”Ordering Information” on page 97.

44.9 Rev. E 05/06

1. Added ”USB Device - High Speed (480 Mbits/s)” on page 665.

44.10 Rev. D 04/06

1. Some occurences of AP7000 renamed to AT32AP7000.
2. Updated ”Real Time Counter” on page 117.
3. Updated ”Audio DAC - (DAC)” on page 480
4. Updated ”DC Characteristics” on page 89.
5. Updated ”Ordering Information” on page 97.

44.11 Rev. C 04/06

1. Initial revision.

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