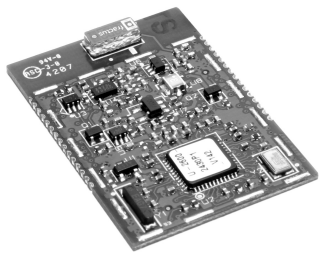
DEVELOPMENT KIT
(Info Click here)

LPR2430ERA

High Power 802.15.4 Module with Chip Antenna

- *2.4 GHz Spread Spectrum Transceiver Module*
- *Small Size, Light Weight, Built-In Antenna*
- *Sleep Current less than 3 µA*
- *FCC, Canadian IC and ETSI Certified for Unlicensed Operation*

The LPR2430ERA 2.4 GHz transceiver module is a low cost, high-power solution for peer-to-peer, point-to-point and point-to-multipoint wireless designs. LPR2430ERA modules provide the flexibility and versatility to serve applications ranging from cable replacements to sensor networks. Based on the IEEE 802.15.4 wireless standard, the LPR2430ERA module is easy to integrate, requires no external antenna, and provides robust wireless communications in applications where mesh network operation is not required. The LPR2430ERA includes CNL V2.0 Network Layer firmware which features a flexible and simple-to-use Application Programming Interface.



Shown with Shield Removed

LPR2430ERA Absolute Maximum Ratings

Rating	Value	Units
All Input/Output Pins	-0.3 to +6.0	V
Non-Operating Ambient Temperature Range	-40 to +85	°C

LPR2430ERA Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency Range			2405		2475	MHz
Operating Frequency Tolerance			-300		300	kHz
Spread Spectrum Method				Direct Sequence		
Modulation Type				O-QPSK		
Number of RF Channels				15		
RF Data Transmission Rate				250		kb/s
Symbol Rate Tolerance					120	ppm
RF Channel Spacing				5		MHz
Receiver Sensitivity, 10E-5 BER				-95		dBm
Upper Adjacent Channel Rejection, +5 MHz				41		dB
Lower Adjacent Channel Rejection, -5 MHz				30		dB
Upper Alternate Channel Rejection, +10 MHz				55		dB
Lower Alternate Channel Rejection, -10 MHz				53		dB
Maximum RF Transmit Power				18		dBm
Transmit Power Adjustment					20	dB
Optimum Antenna Impedance				50		Ω

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LPR2430ERA Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
ADC Input Range			0		3.3	V
ADC Input Resolution				11		bits
ADC Input Impedance			55			MΩ
PWM Output Resolution*			8		16	bits
UART Baud Rates			1.2, 2.4, 4.8, 9.6 (default), 19.2, 28.8, 38.4, 57.6, 76.8, 115.2			kb/s
Digital I/O:						
Logic Low Input Level			-0.3		0.5	V
Logic High Input Level			2.8		3.6	V
Logic Input Internal Pull-up/Pull-down Resistor			20			KΩ
GPIO3 Logic Low Sink Current					20	mA
Power Supply Voltage Range	V_{CC}		+3.3		+5.5	Vdc
Power Supply Voltage Ripple					10	mV_{P-P}
Receive Mode Current				33		mA
Transmit Mode Current				130		mA
Sleep Mode Current					3	µA
Operating Temperature Range			-40		85	°C

*PWM0 has 8-bit resolution, PWM1 has 16-bit resolution. Built-in PWM output filters suppress ripple to 7 bits. Additional filtering can be added externally.

CAUTION: Electrostatic Sensitive Device. Observe precautions when handling.

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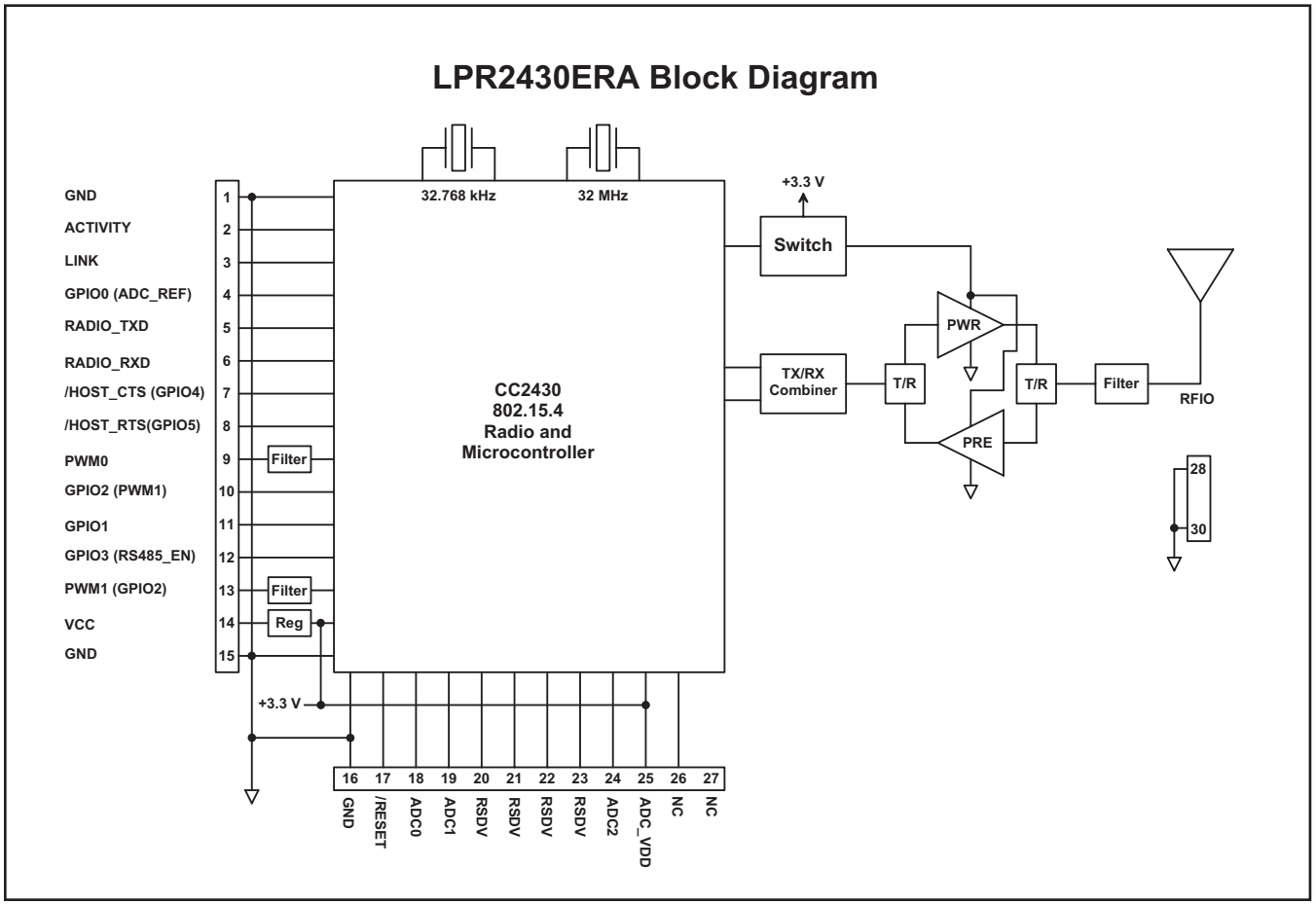


Figure 1

LPR2430ERA Hardware

The major hardware component of the LPR2430ERA is the CC2430 IEEE 802.15.4 compatible transceiver with integrated 8051 microcontroller. The LPR2430ERA operates in the frequency band of 2405 to 2475 MHz at a nominal output power of 63 mW.

The LPR2430ERA includes a low noise preamplifier in the receiver path and a power amplifier in the transmitter path, greatly increasing the operating range of the CC2430. Two crystals are provided to operate the CC2430, a 32 MHz crystal for normal operation and a 32.768 kHz crystal for precision sleep mode operation.

The LPR2430ERA provides a variety of application hardware interfaces including a UART interface, three 11-bit ADC inputs, two PWM (DAC) outputs, and six general purpose digital I/O ports.

LPR2430ERA Firmware

The main firmware components in the LPR2430ERA include the 802.15.4 Media Access Control (MAC) layer and the CNL V2.0 Networking Layer. CNL V2.0 supports up to 63 remotes. Network topologies include point-to-point, point-to-multipoint and peer-to-peer. CNL employs one-hop relay forwarding to mitigate network transmission problems such as multipath fading. CNL includes provisions for low-power sleep mode operation with periodic wakeup and report. The CNL Application Programming Interface (API) provides an easy-to-use, flexible set of application commands and functions. The API includes support for send/receive serial data, read/write GPIO, read ADC inputs, write PWM outputs and module configuration services. In addition, CNL supports analog and digital I/O binding, which maps an ADC measurement and the states of two digital inputs on one LPR2430ERA to a PWM output and two digital outputs on another LPR2430ERA. See the *LPR2430 Series Integration Guide* for complete details of the CNL API.

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LPR2430ERA I/O Pad Descriptions

Pin	Name	I/O	Description
1	GND	-	Power supply and signal ground. Connect to the host circuit board ground.
2	ACTIVITY	O	RF activity indicator. Output pulses high when a packet is sent or received.
3	LINK	O	Link indicator. Output is high when the radio has successfully joined a network.
4	GPIO0 (ADC_REF)	I/O	Configurable digital I/O port 0. When configured as an output, the power-on state is also configurable. This pin can also be configured as a reference voltage input for the ADCs, 0 to 3.3 V, 1.25 V typical.
5	RADIO_TXD	O	Serial data output (UART) from the radio to the host.
6	RADIO_RXD	I	Serial data input (UART) from the host to the radio.
7	GPIO4 (/HOST_CTS)	I/O	Configurable digital I/O port 4. When configured as an output, the power-on state is also configurable. Also configurable as UART flow control output. The LPR2430 sets this line low to indicate it is ready to accept data from the host on the RADIO_RXD input. When the LPR2430 sets this line high, the host must stop sending data. The default state is GPIO4.
8	GPIO5 (/HOST_RTS)	I/O	Configurable digital I/O port 5. When configured as an output, the power-on state is also configurable. Also configurable as UART flow control input. The host sets this line low to allow data to flow from the RADIO_TXD pin. When the host sets this line high, the LPR2430 will stop sending data to the host. The default state is GPIO5.
9	PWM0	O	Pulse-width modulated output 0 with internal low-pass filter. Provides a DAC function, 0 to 3.3 V.
10	GPIO2 (PWM1)	I/O	Configurable digital I/O port 2. When configured as an output, the power-on state is also configurable. This pin is connected to the input of the low-pass filter driving Pin 13, and is also configurable as a PWM output.
11	GPIO1	I/O	Configurable digital I/O port 1. When configured as an output, the power-on state is also configurable.
12	GPIO3 (RS485_EN)	I/O	Configurable digital I/O port 3. When configured as an output, this high current port can sink up to 20 mA. The power-on output state is also configurable. Can also be configured as active low transmit enable for controlling an RS485 or other half-duplex bus driver.
13	PWM1 (GPIO2)	O	GPIO2 (Pin 10) drives this pin through a low-pass filter. Provides a DAC function when GPIO2 is configured as a PWM output.
14	VCC	I	Power supply input, +3.3 to +5.5 Vdc.
15	GND	-	Power supply and signal grounds. Connect to the host circuit board ground.
16	GND	-	Power supply and signal grounds. Connect to the host circuit board ground.
17	/RESET	I	Active low module hardware reset. Hold this input low when the power supply input is less than 3.3 Vdc. The module firmware boots up and will accept commands about 3 seconds after this input goes high.
18	ADC0	I	11-bit ADC input 0. ADC full scale reading can be referenced to the module's +3.3 V regulated supply, the ADC's internal +2.5 V reference, or ADC_REF (Pin 4).
19	ADC1	I	ADC input 1. Same configuration options as ADC0.
20	RSVD	-	Reserved pin. Leave unconnected.
21	RSVD	-	Reserved pin. Leave unconnected.
22	RSVD	-	Reserved pin. Leave unconnected.
23	RSVD	-	Reserved pin. Leave unconnected.
24	ADC2	I	ADC input 2. Same configuration options as ADC0.
25	ADC_VDD	O	Module's +3.3 V regulated supply, used for ratiometric ADC readings. Current drain should be less than 5 mA.
26	NC	-	No connection.
27	NC	-	No connection.
28	GND	-	RF ground. Connect to the host circuit board ground plane, and to shield when using coaxial cable.
29	NC	-	No connection.
30	GND	-	RF ground. Connect to the host circuit board ground plane, and to shield when using coaxial cable.

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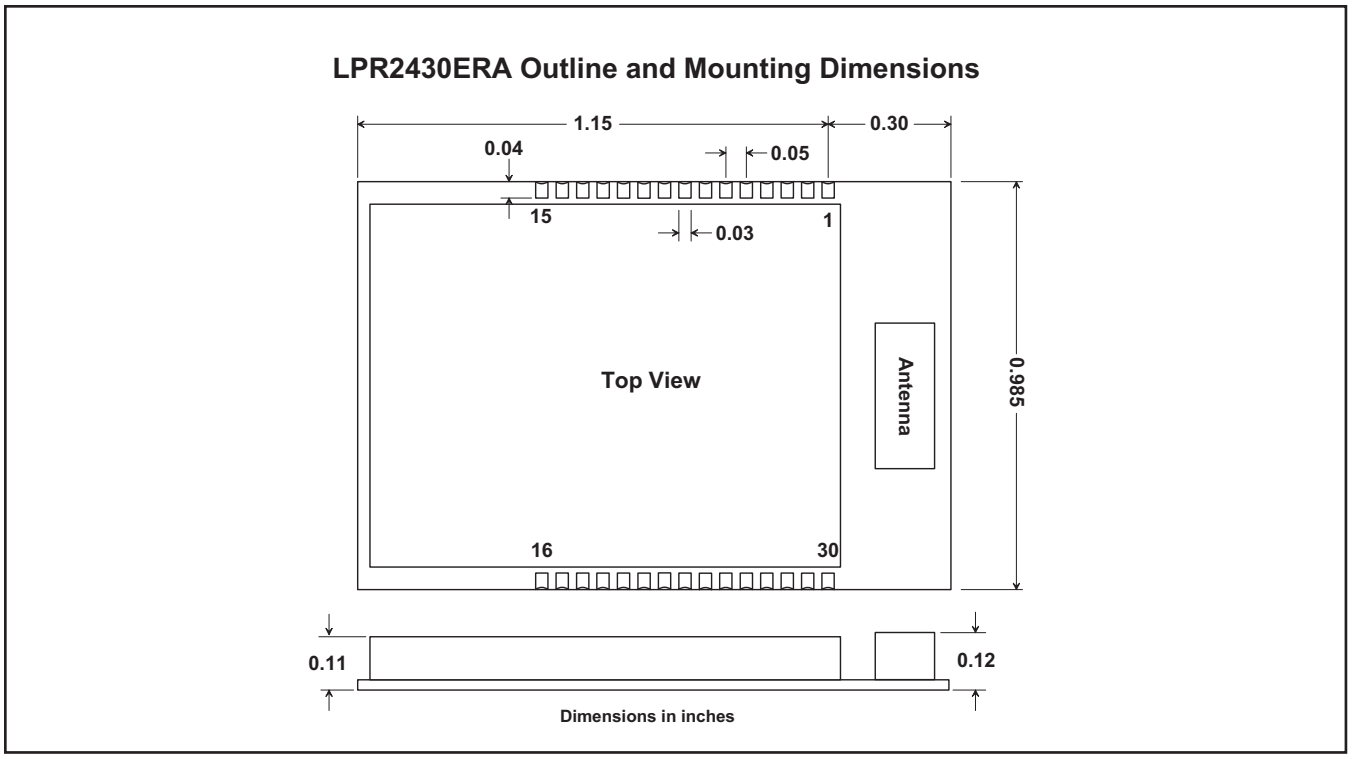
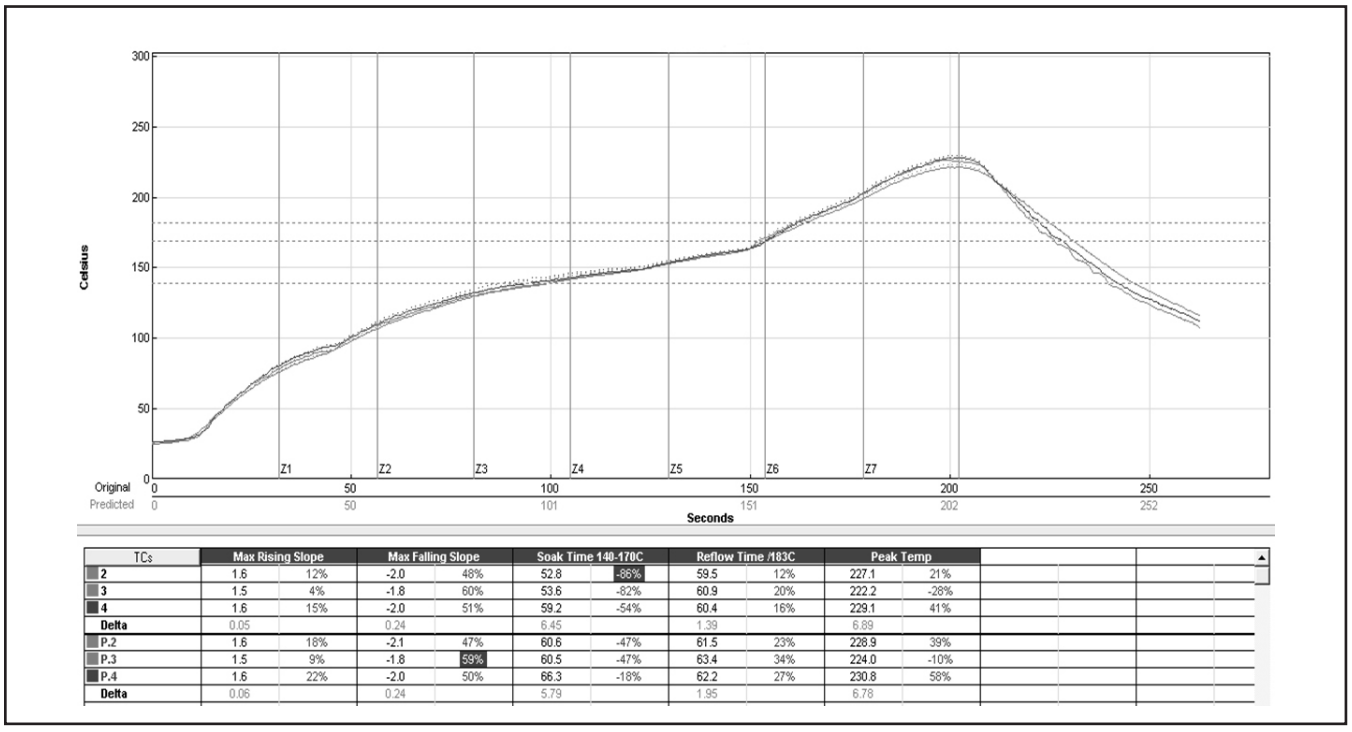


Figure 2

Reflow Profile

An example solder reflow profile for mounting the radio module on its host circuit board is shown in Figure 3.



TCs	Max Rising Slope		Max Falling Slope		Soak Time 140-170C		Reflow Time /183C		Peak Temp	
2	1.6	12%	-2.0	48%	52.8	-86%	59.5	12%	227.1	21%
3	1.5	4%	-1.8	60%	53.6	-82%	60.9	20%	222.2	-28%
4	1.6	15%	-2.0	51%	59.2	-54%	60.4	16%	229.1	41%
Delta	0.05		0.24		6.45		1.38		6.89	
P.2	1.6	18%	-2.1	47%	60.6	-47%	61.5	23%	228.9	39%
P.3	1.5	9%	-1.8	59%	60.5	-47%	63.4	34%	224.0	-10%
P.4	1.6	22%	-2.0	50%	66.3	-18%	62.2	27%	230.8	58%
Delta	0.06		0.24		5.79		1.95		6.78	

Figure 3

Note: Specifications subject to change without notice.

Part # M-2430-0005, Rev A

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