Data Sheet June 1998 File Number 4503

Unbalanced PBX/Key System SLIC, Subscriber Line Interface Circuit

The Intersil HC5503C is a low cost Subscriber Line Interface Circuit (SLIC), that replaces the components of an unbalanced discrete Analog circuit design. The monolithic integrated design provides improved performance and system reliability.

The SLIC provides: current limited DC feed to the subscriber loop, maintains a flat frequency response over the voice band and beyond, has self resetting thermal protection that allows conversation to continue while the fault is present, provides a TTL subscriber off-hook indication even in the presence of longitudinal currents, provides unbalanced 2-wire transmission while maintaining an excellent longitudinal balance and limits system power consumption on short loops.

The HC5503C provides on-hook transmission and longitudinal current rejection in both the on-hook or off-hook conditions. The SLIC needs only one +5V supply in addition to the main battery supply (-24V to -58V) for loop current.

Available in 22PDIP and 24SO packaging. The HC5503C is ideally suited as a replacement for discrete line circuits in low cost analog PABX's, Small Office/Home Office products or Small Key Systems.

Features

- Monolithic Integrated Device
- Single +5V Supply
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Allows Interfacing With All Ringing Systems
- Switch Hook Detection
- Low Power Consumption During Standby

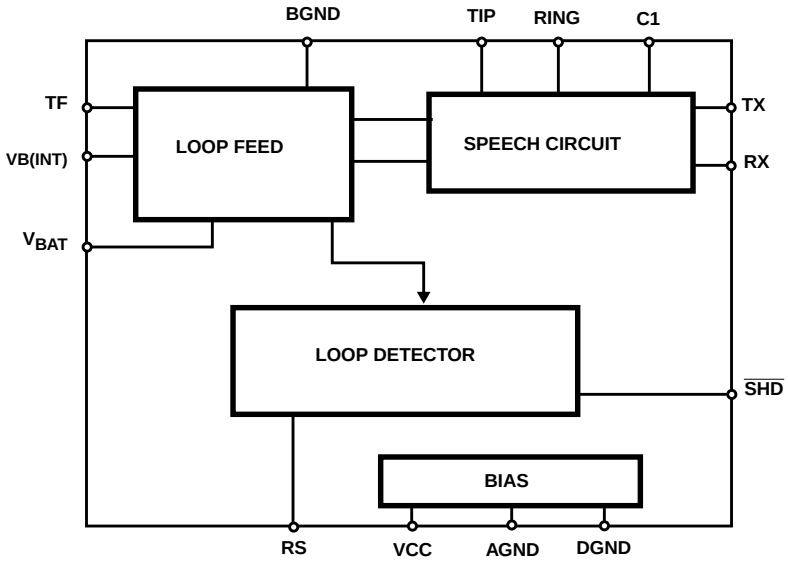
Applications

- PBX Switches (Analog, Digital or ISDN)
- Key Telephone Systems (KTS)
- ISDN PC Plug in Modems
- ISDN Small Office / Home Office (SOHO) Terminal Adapters (TA)
- CTI (Computer Telephony Integration) Products

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HC5503CCP	0 to 75	22 Ld PDIP	E22.4
HC5503CCB	0 to 75	24 Ld SOIC	M24.3

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
http://www.intersil.com or 407-727-9207 | Copyright © Intersil Corporation 1999

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_{BAT}) . . . . . -60 to 0.5V
- (V_{CC}) . . . . . -0.5 to 7V
- (V_{CC} - V_{BAT}) 75V

Operating Conditions

Temperature Range
- HC5503C-5 . . . . . 0^oC to 75^oC

Positive Supply Voltage (V_{CC}) . . . . . 4.75V to 5.25V
Negative Supply Voltage (V_{BAT}) . . . . . -24V to -58V
High Level Logic Input Voltage. 2.4V
Low Level Logic Input Voltage 0.6V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	53
SOIC Package	75

Maximum Junction Temperature Plastic . . . . . 150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Die Characteristics

Transistor Count. 185
Diode Count. 36
Die Dimensions . . . . . 137 x 102
Substrate Potential. . . . . Connected
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_{BAT} = -48V, V_{CC} = 5V, AG = BG = DG = 0V, Typical Parameters $T_A = 25^oC$. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Off-Hook I_B+	$R_L = 600\Omega$, $T_A = 25^oC$	-	-	5.3	mA
Off-Hook I_B-	$R_L = 600\Omega$	-	-	39	mA
Off-Hook Loop Current	$R_L = 1200\Omega$	-	21	-	mA
Off-Hook Loop Current	$R_L = 1200\Omega$, V_{BAT} = -42V, $T_A = 25^oC$	17.5	-	-	mA
Off-Hook Loop Current	$R_L = 200\Omega$	25.5	30	34.5	mA
Switch Hook Detection Threshold	$\overline{SHD} = V_{OL}$	10	-	-	mA
	$\overline{SHD} = V_{OH}$	-	-	5	mA
Dial Pulse Distortion		0	-	5	µs
Longitudinal Balance 2-Wire Off-Hook	$1V_{RMS}$ 200Hz - 3400Hz, (Note 3) IEEE Method $0^oC \le T_A \le 75^oC$	-	65	-	dB
2-Wire On-hook		-	63	-	dB
Tip and Ring to TX, Off-hook		-	58	-	dB
Insertion Loss 2-Wire to TX, RX to 2-Wire	At 1kHz, 0dBm Input Level, Referenced 600Ω	-	±0.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 3)	-	±0.02	±0.05	dB
Idle Channel Noise 2-Wire to TX, RX to 2-Wire	(Note 3)	-	1	5	dBrnC
		-	-89	-85	dBm0p
Trans Hybrid Loss RX to TX	Balance Network Set Up for 600Ω Termination at 1kHz	-	40	-	dB

Electrical Specifications Unless Otherwise Specified, V_{BAT} = -48V, V_{CC} = 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range **(Continued)**

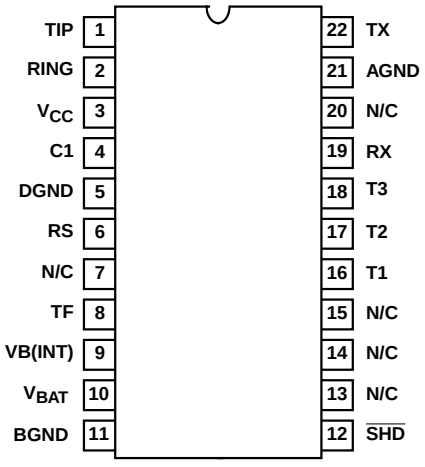
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level, 2-Wire to TX, RX to 2-Wire	V_{CC} = +5V, (Note 3)	2.5	-	-	V_{PEAK}
Level Linearity 2-Wire to TX, RX to 2-Wire	At 1kHz, (Note 3) Referenced to 0dBm Level +3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio V_{CC} to 2-Wire	(Note 3) 200 - 3400kHz, R_L = 600Ω	-	40	-	dB
V_{CC} to Transmit		-	40	-	dB
V_{BAT} to 2-Wire		-	40	-	dB
V_{BAT} to Transmit		-	40	-	dB
Logic Input Current (RS)	0V ≤ V_{IN} ≤ 5V	-	-	±100	µA
Logic Input (RS) Logic ‘0’ V_{IL}		-	-	0.8	V
Logic ‘1’ V_{IH}		2.0	-	5.5	V
Logic Output ($\overline{SHD}$) Logic ‘0’ V_{OL}	I_{LOAD} 800µA, V_{CC} = 5V	-	0.1	0.5	V
Logic ‘1’ V_{OH}	I_{LOAD} 40µA, V_{CC} = 5V	2.7	-	5.0	V

NOTE:

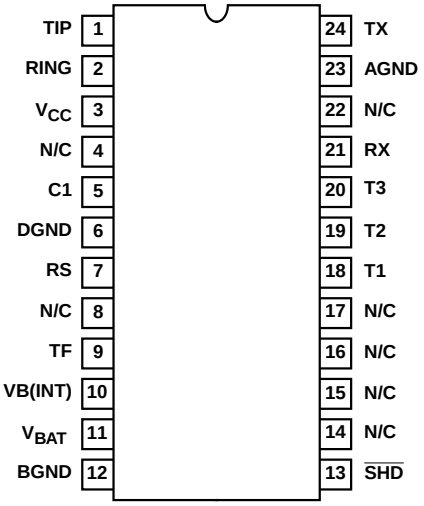
3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pinouts

HC5503C (PDIP)
TOP VIEW



HC5503C (SOIC)
TOP VIEW



Pin Descriptions

PDIP	SOIC	SYMBOL	DESCRIPTION
1	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
2	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	3	V_{CC}	Positive Voltage Source - Most positive supply. V_{CC} is typically 5V.
	4	N/C	No connect. For proper operation this pin should be left floating.
4	5	C_1	Capacitor - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the voice band hybrid. Typical value is 0.3µF, 30V.
5	6	DGND	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
6	7	RS	This pin should be tied to 5V.
7	8	N/C	No connect. For proper operation this pin should be left floating.
8	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Provides voice signals to the telephone set and sink longitudinal current.
9	10	VB(INT)	A low impedance analog output connected to the Ring terminal through a 150Ω feed resistor. This pin provides a loop current path to battery.
10	11	V_{BAT}	Negative Voltage Source - Most negative supply. V_{BAT} has an operational range of -24V to -58V. Frequently referred to as “battery”.
11	12	BGND	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
12	13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
13	14	N/C	No connect. For proper operation this pin should be left floating.
	15	N/C	No connect. For proper operation this pin should be left floating.
14	16	N/C	No connect. For proper operation this pin should be left floating.
15	17	N/C	No connect. For proper operation this pin should be left floating.
16	18	T1	Used during production testing. For proper operation this pin should be connected to pin T2.
17	19	T2	Used during production testing. For proper operation this pin should be connected to pin T1.
18	20	T3	Used during production testing. For proper operation this pin should be connected to Analog Ground pin AGND.
19	21	RX	Receive Input - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
20	22	N/C	No connect. For proper operation this pin should be left floating.
21	23	AGND	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
22	24	TX	Transmit Output - A low impedance analog output which represents the differential voltage across Tip and Ring. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.

NOTE: All grounds (AGND, BGND, and DGND) must be applied before V_{CC} or V_{BAT}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Applications Diagram

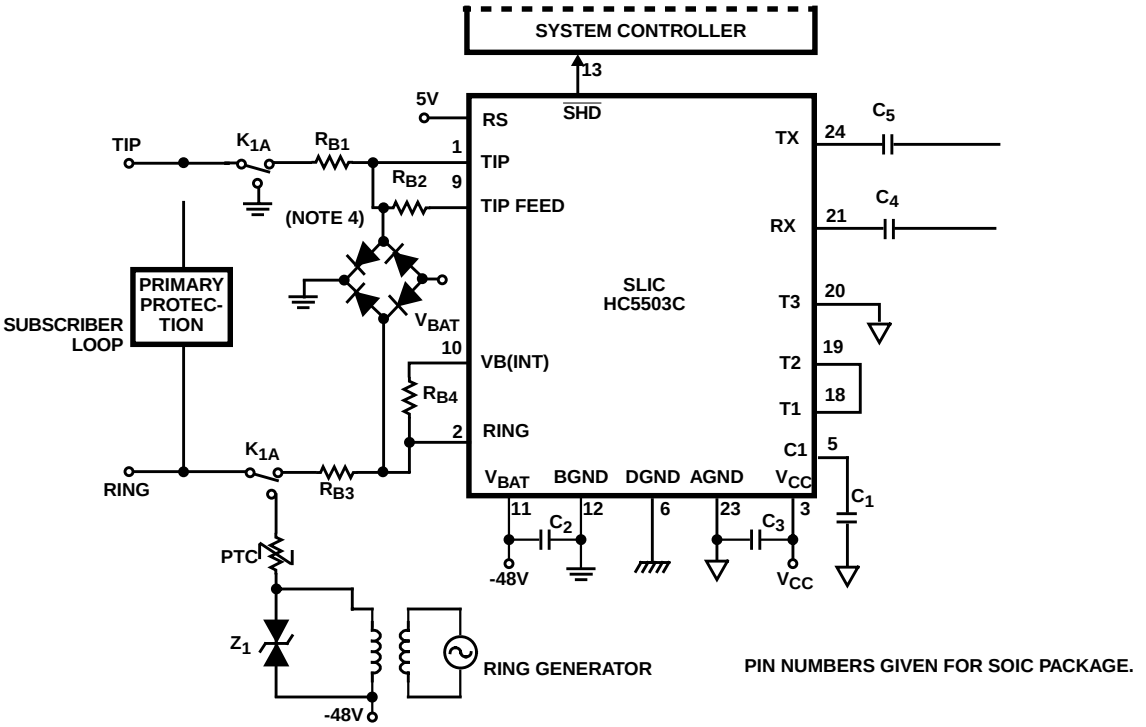


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_1 = 0.3µF, 30V, ±20%

C_2 = 0.01µF, 100V, ±20%

$R_{B1} = R_{B2} = R_{B3} = R_{B4} = 150\Omega$

C_3 = 0.01µF, 20V, ±20%

C_4 = 0.5µF, 20V, ±20%

C5 = 0.5µF, 20V, ±20%

PTC used as ring generator ballast.

NOTES:

4. Secondary protection diode bridge recommended is a 2A, 200V type.
5. All grounds (AG, BG, and DG) must be applied before V_{CC} or V_{BAT}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
6. Application shows Ring Injected Ringing.

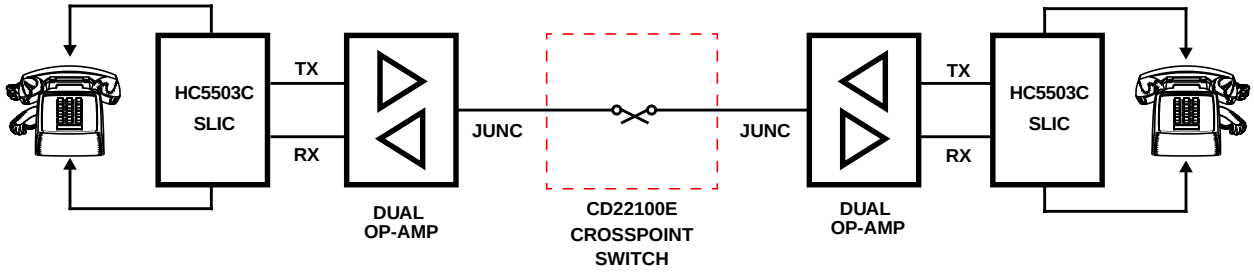


FIGURE 2. TYPICAL ANALOG KEY SYSTEM CONNECTION

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**