RF2917

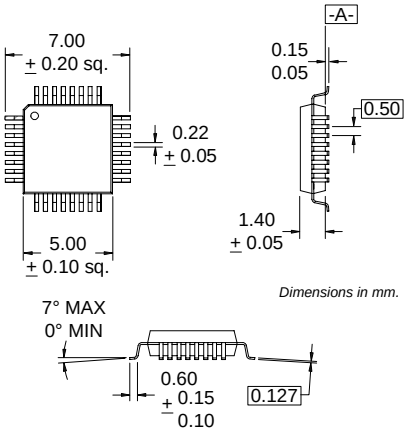
433/868/915MHZ
FM/FSK RECEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Band Systems
- Remote Data Transfers
- Wireless Security Systems

Product Description

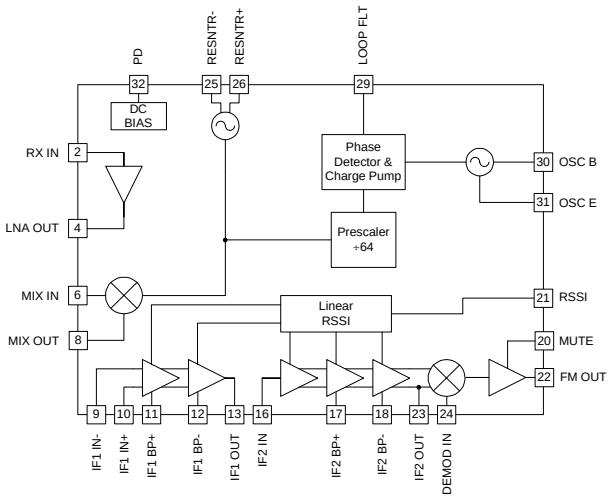
The RF2917 is a monolithic integrated circuit intended for use as a low cost FM or FSK receiver. The device is provided in 32-lead plastic packaging and is designed to provide a fully functional FM receiver. The chip is intended for analog or digital applications in the North American 915MHz ISM band and European 433MHz and 868 MHz ISM bands. The integrated VCO, ÷64 prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator for single channel applications. The selection of linear FM output or digital FSK output is done with the mute pin.



Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] GaAs HBT
- [ ] GaAs MESFET
- [ ] Si Bi-CMOS
- [ ] SiGe HBT
- [ ] Si CMOS

Package Style: LQFP-32_5x5



Functional Block Diagram

Features

- Fully Monolithic Integrated Receiver
- 2.7V to 5.0V Supply Voltage
- Narrowband and Wideband FSK
- 300MHz to 1000MHz Frequency Range
- Power Down Capability
- Analog or Digital Output

Ordering Information

RF2917	433/868/915MHz FM/FSK Receiver
RF2917 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2917 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2917 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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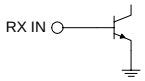
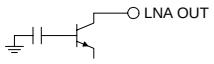
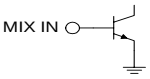
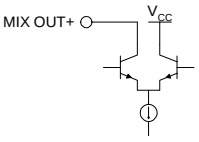
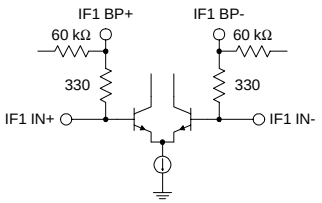
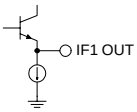
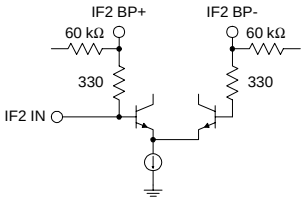
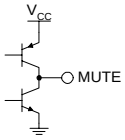
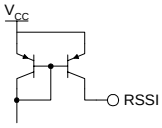
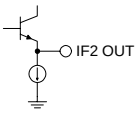
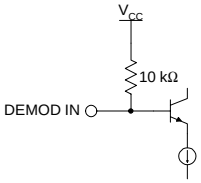
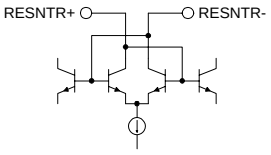
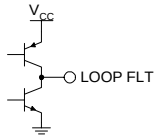
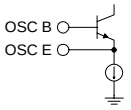
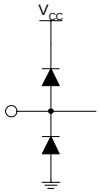
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
PLL Lock Time		10		ms	The PLL lock time is set externally by the bandwidth of the loop filter and start up of the crystal.
PLL Phase Noise		-74		dBc/Hz	915MHz, 5kHz loop BW, 10kHz offset
		-98		dBc/Hz	915MHz, 5kHz loop BW, 100kHz offset
Reference Frequency	0.5		17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current	-40		+40	µA	
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
RX Sensitivity	-98	-101		dBm	IF BW=180kHz, Freq=915MHz, S/N=8dB
LO Leakage		-55		dBm	
RSSI DC Output Range		0.8 to 1.5		V	MUTE = 0; R_L = 51kΩ
RSSI Sensitivity		13		mV/dB	MUTE = 0
RSSI Dynamic Range		60		dB	MUTE = 0
LNA					
Power Gain		18		dB	433MHz, Matched to 50Ω
		16		dB	915MHz, Matched to 50Ω
Noise Figure		3.6		dB	433MHz
		3.8		dB	915MHz
Input IP_3		-8		dBm	915MHz
Input P_{1dB}		-15		dBm	915MHz
RX IN Impedance		82-j86		Ω	433MHz (see Plots)
		77-j43			915MHz (see Plots)
Output Impedance		Open Collector		Ω	
Mixer					Single-ended configuration
Conversion Power Gain		15		dB	433MHz, Matched to 50Ω
		8		dB	915MHz, Matched to 50Ω
Noise Figure (SSB)		17		dB	433MHz, SSB Measurement
		17		dB	915MHz, SSB Measurement
Input IP_3		-20		dBm	433MHz
Input IP_3		-15.5		dBm	915MHz
Input P_{1dB}		-30		dBm	433MHz
Input P_{1dB}		-26		dBm	915MHz
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
Noise Figure		13		dB	
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT- pin 23
Demod Input Impedance		10		kΩ	Pin 24
Data Output Impedance		6.3 - j25.7		kΩ	
Data Output Bandwidth		500		kHz	Z_{LOAD}=1MΩ || 3pF; 3dB dependent on IF and discriminator BW
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ || 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	
FM Output AC Level		200		mV_{PP}	
Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25			kΩ	
Turn On Time		10.2		ms	From PD=1 to valid data out, current eval board
Power Supply					
Voltage		3.6		V	Specifications
	2.7		5.0	V	Operating limits
	2.4			V	Temp>0°C
Current Consumption	5	9	12.3	mA	RX Mode, MUTE=“1”
			1	μA	Power Down Mode

Pin	Function	Description	Interface Schematic
1	VCC1	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 100pF capacitor is recommended for 433MHz applications.	
2	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance when enabled. RX IN is a high impedance when the receiver is disabled.	
3	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
5	GND2	GND2 is connection for the 40 dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
6	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
7	GND3	GND3 is the ground connection for the receiver RF mixer.	
8	MIX OUT	IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application. In addition to the matching components, a 15pF capacitor should be placed from this pin to ground.	
9	IF1 IN-	Balanced IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	
10	IF1 IN+	Functionally the same as pin 9 except non-inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 9.
11	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 100nF bypass capacitor from this pin to ground is required.	See pin 9.
12	IF2 BP-	See pin 11.	See pin 9.
13	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
14	VREF IF	DC voltage reference for the IF limiting amplifiers (typically 1.1V). A 0.1µF capacitor from this pin to ground is required.	
15	GND5	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	

Pin	Function	Description	Interface Schematic
16	IF2 IN	Inverting input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
17	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 100nF bypass capacitor from this pin to ground is required.	See pin 16.
18	IF2 BP-	See pin 17.	See pin 16.
19	VCC3	This pin is used to supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
20	MUTE	This pin is used to select FM, FSK, or mute at the FM OUT pin. MUTE>Vcc - 0.4V turns the FM OUT signal off. MUTE<0.4V turns the FM OUT signal on for FSK digital data. When MUTE is left floating, the FM OUT signal is linear FM.	
21	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage increases with increasing signal strength.	
22	FM OUT	Demodulated output from the discriminator/demodulator. Output levels on this are CMOS compatible in FSK mode (see pin 20). In linear FM mode, the demodulated signal level is approximately 240mVpp on a DC voltage offset. The magnitude of the load impedance is intended to be 1MΩ or greater.	
23	IF2 OUT	IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 24 through a 5pF capacitor (for 10.7MHz IF applications). This capacitor in conjunction with a tank resonant at the IF frequency connected from pin 24 to ground is used to form an FM discriminator.	
24	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid a DC path to ground. A DC blocked LC tank resonant at the IF or ceramic discriminator should be connected to this pin.	
25	RESNTR-	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 26.	
26	RESNTR+	See pin 25.	See pin 25.
27	VCC2	This pin is used to supply DC bias to the VCO, prescaler, and PLL. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
28	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	

Pin	Function	Description	Interface Schematic
29	LOOP FLT	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
30	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. A 100pF capacitor should be connected between pin 30 and pin 31.	
31	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. A 100pF capacitor should be connected from this pin to ground.	See pin 30.
32	PD	This pin is used to power up or down the RF2917. A logic high (PWR DWN >2.0V) powers up the receiver and PLL. A logic low (PWR DWN <1.0V) powers down circuit to standby mode.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 3, 5, 7-19, 21-24, 27-31.	

RF2917 Theory of Operation and Application Information

The RF2917 is part of a family of low-power RF transceiver IC's developed for wireless data communication devices operating in the European 433/868MHz ISM bands or the U.S. 915MHz ISM band. This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products. The RF2917 realizes a highly integrated, single-conversion FM/FSK receiver with the addition of a reference crystal, intermediate frequency (IF) filtering, and a few passive components. The LNA (low noise amplifier) input of the RF2917 is easily matched to a front-end filter or antenna by means of a DC blocking capacitor and reactive components. The receiver local oscillator (LO) is generated by an internalized VCO, PLL and phase discriminator in conjunction with the external reference crystal, loop filter and VCO resonator components. The receiver IF section is optimized to interface with low cost 10.7MHz ceramic filters, and its -3dB bandwidth of 25MHz also allows it to be used (with lower gain) at higher frequencies with other types of filters.

FM/FSK SYSTEMS

The receiver output functionality is determined by the tri-state MUTE input. The three output configurations are linear FM, FSK and mute. An on-chip 1.6MHz RC filter, which follows the demodulator output, filters the harmonics of the IF signal from the output data.

When in the FM mode, the FM OUT signal is the buffered output from the quadrature demodulator. The output signal has a fixed DC offset of V_{CC}-1.0V, while the AC level is dependent on the FM deviation, with a maximum level of 240mV_{P-P} For optimum operation in either FM or FSK mode, FM deviation needs to exceed (with margin) the carrier frequency error anticipated between the receiver and transmitter.

When in the FSK mode, the FM OUT signal is clipped, having a rail-to-rail output level. The FM OUT pin is only capable of driving rail-to-rail output into a very high impedance and small capacitance, with the amount of capacitance determining the FM OUT bandwidth. For a 3pF load, the bandwidth is in excess of 500kHz. The rail-to-rail output is also limited by the frequency deviation and bandwidth of the IF filters. With the 180kHz bandwidth filters on the evaluation boards, the rail-to-rail output is limited to less than 140kHz. Choosing the right IF bandwidth and deviation versus data rate (modulation index) is important in evaluating the applicability of the RF2917 for a given data rate.

AM SYSTEMS

The RF2919 is recommended for use in ASK/OOK applications, however, the RF2917 may be utilized in an AM system by using the RSSI (received signal strength indicator) output to recover the modulation. The FM output mode should be selected for AM operation because of the higher RSSI resolution in FM mode.

RSSI

The RSSI output signal is supplied from a current source and therefore requires a resistor to convert it to a voltage. The RSSI is linear over the same range of input power for both FM and FSK modes, but the FM mode has higher RSSI resolution. For a 51kΩ resistive load, the RSSI will range from 1.0V to 2.6V in FM mode and from 0.8V to 1.5V in FSK mode (3.6V supply). A small parallel capacitor is suggested to limit the bandwidth and filter noise.

APPLICATION AND LAYOUT CONSIDERATIONS

The RX IN pin is DC-biased, requiring a DC blocking capacitor. If the RF filter has DC blocking characteristics, such as a ceramic dielectric filter, then a DC blocking capacitor is not necessary. When in power down mode, the RX IN impedance increases. Therefore, in a half-duplex application, the RF2917 RX IN may share the RF filter with a transmitter output having a similar high impedance power down characteristic. Care must be taken in this case to account for loading effects of the transmitter on the receiver, and vice versa, in matching the filter to both the transmitter and receiver.

The VCO is a very sensitive block in this system. RF signals feeding back into the VCO by either radiation or coupling of traces may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonators and varactor are very important. The capacitor and varactor should be closest to the RF2917 pins and the trace length should be as short as possible. The inductors can be placed further away and any trace inductance can be compensated by reducing the value of the inductors. Printed inductors may also be used with careful design. For best results, the physical layout should be as symmetrical as possible.

When using loop bandwidths lower than the 5kHz shown on the evaluation board, better supply filtering at the resonators (and lower V_{CC} noise as well) will help reduce the phase noise of the VCO; a series resistor of 100Ω to 200Ω and a 1μF or larger capacitor

may be used. Phase noise is generally more critical in narrowband applications where adjacent channel selectivity is a concern, but it can also contribute to raising the noise floor of the receiver, thereby degrading sensitivity.

For the interface between the LNA and mixer, the coupling capacitor should be as close to the RF2917 pins as possible, with the bias inductor being further away. Once again, the value of the inductor may be changed to compensate for trace inductance. The output impedance of the LNA is on the order of several kΩ, which makes matching to 50Ω difficult. If image filtering is desired, a high impedance filter is recommended. If no filtering is used, the match to the mixer input need not be a good conjugate match, because of the high gain of the IF amplifier stages. In fact, a conjugate match between the LNA and mixer will not significantly improve sensitivity, but will have an adverse effect on system IIP3 and increase the likelihood of IF instability.

Because of the high gain of the IF section, care should be taken in laying out the IF filtering and discriminator components to minimize the possibility of instability. In particular, inductive feedback may occur between the inductor of a discrete (LC) discriminator and any inductor(s) in the IF interstages. Orthogonal placement of inductors will generally minimize coupling. Indicators that an instability may exist include poor sensitivity and a high RSSI level when no input signal is present.

The quadrature tank of the discriminator may be implemented with ceramic discriminators available from a variety of sources. This design works well for wideband applications, and where the temperature range is limited. The temperature coefficient of a ceramic discriminator may be on the order of ±50ppm/°C. An automatic frequency control loop may be implemented using the DC level of the FM OUT for feedback to an external varactor on the reference crystal. An alternative to the ceramic discriminator is an LC tank. The DEMOD IN pin has a DC bias and must be DC-blocked. This can be done either at the pin or at the ground side of the LC tank (this must also be done if a parallel resistor is used with a ceramic discriminator). The decision whether to use an LC or a ceramic discriminator should be based on the frequency deviation in the system, discriminator Q needed, and frequency and temperature tolerances. Tuning of the LC tank is required to overcome the component tolerances in the tank.

PREDICTING AND MINIMIZING PLL LOCK TIME

The RF2917 implements a conventional on-chip PLL. The VCO is followed by a prescaler, which divides down the output frequency for comparison with the reference oscillator frequency. The output of the phase discriminator is a sequence of pulse width modulated current pulses in the required direction to steer the VCO's control voltage to maintain phase lock, with a loop filter integrating the current pulses. The lock time of this PLL is a combination of the loop transient response time and the slew rate set by the phase discriminator output current, combined with the magnitude of the loop filter capacitance. A good approximation for total lock time of the RF2917 is:

$$LockTime = \frac{D}{F_C} + 35000 \cdot C \cdot dV$$

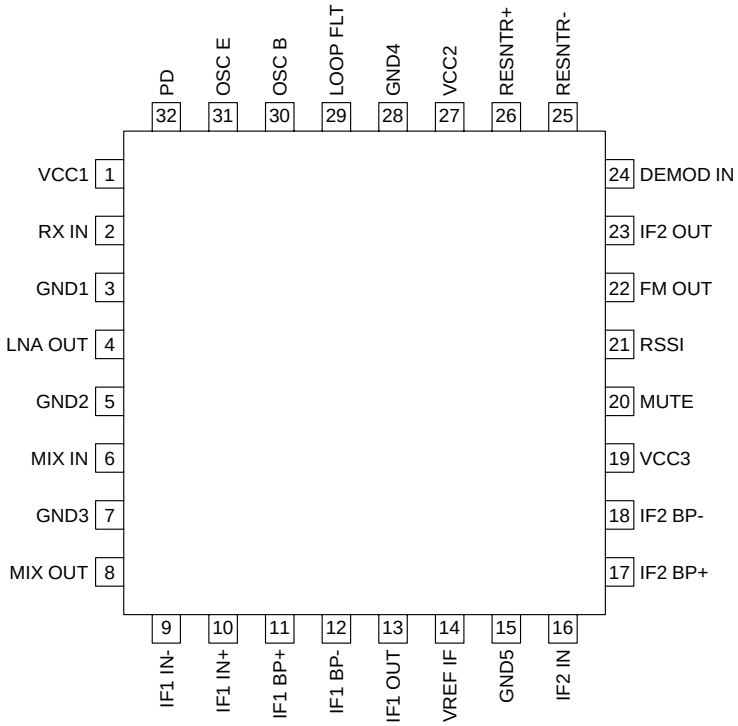
where D is a factor to account for the loop damping, F_C is the loop cut frequency, C is the sum of all shunt capacitors in the loop filter, and dV is the required step voltage change to produce the desired frequency change during the transient. For loops with low phase margin (30° to 40°), use D=2, whereas for loops with better phase margin (50° to 60°), use D=1.

To lock faster, C needs to be minimized.

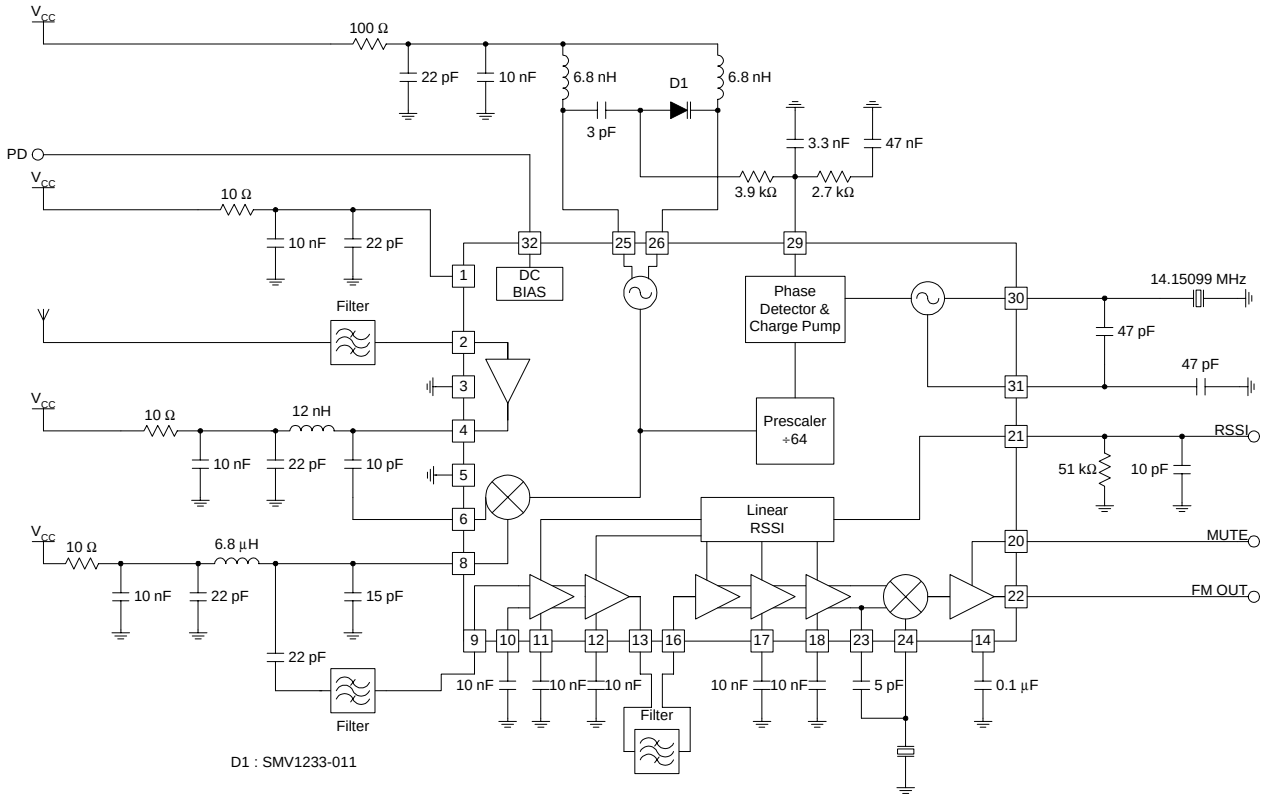
1. Design the loop filter for the minimum phase margin possible without causing loop instability problems; this allows C to be kept at a minimum.

2. Design the loop filter for the highest loop cut frequency possible without distorting low frequency modulation components; this also allows C to be kept at a minimum.

Pin Out

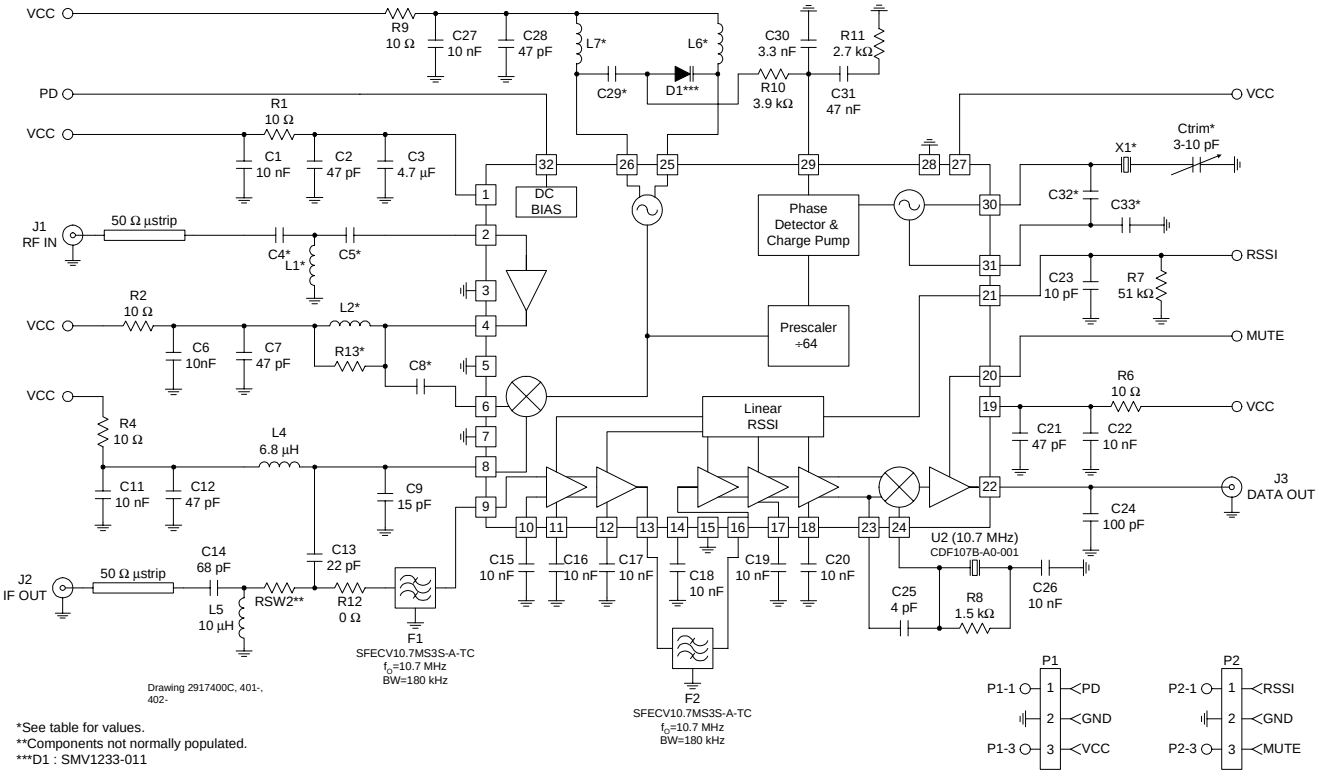

PD 32
OSC E 31
OSC B 30
LOOP FLT 29
GND4 28
VCC2 27
RESNTR+ 26
RESNTR- 25
VCC1 1
RX IN 2
GND1 3
LNA OUT 4
GND2 5
MIX IN 6
GND3 7
MIX OUT 8
24 DEMOD IN
23 IF2 OUT
22 FM OUT
21 RSSI
20 MUTE
19 VCC3
18 IF2 BP-
17 IF2 BP+
9 IF1 IN-
10 IF1 IN+
11 IF1 BP+
12 IF1 BP-
13 IF1 OUT
14 VREF IF
15 GND5
16 IF2 IN

915MHz Application Schematic



Evaluation Board Schematic
H (915MHz), M (868MHz), L (433MHz) boards

(Download Bill of Materials from www.rfmd.com.)

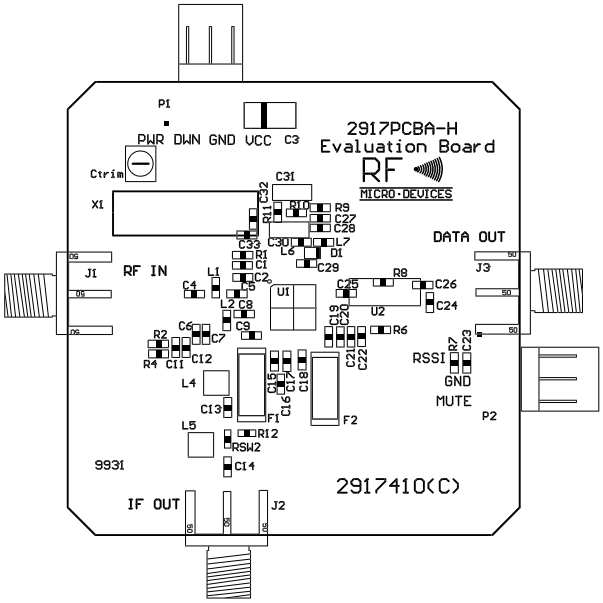


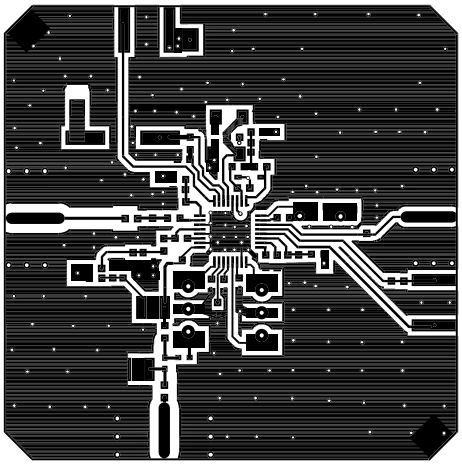
*See table for values.
**Components not normally populated.
***D1 : SMV1233-011

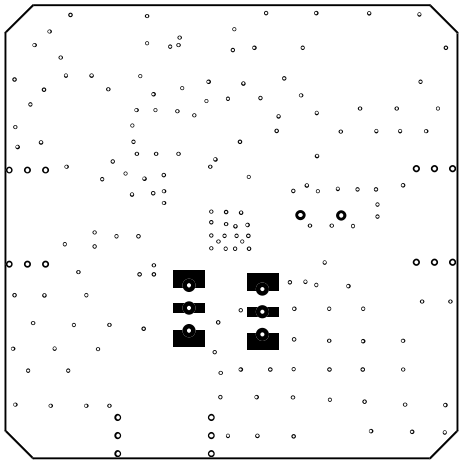
Board	C4 (pF)	L1 (nH)	C5 (pF)	L2 (nH)	R13 (Ω)	C8 (pF)	L6 (nH)	L7 (nH)	C29 (pF)	X1 (MHz)	C32 (pF)	C33 (pF)
L (433MHz)	2	27	100	33	510	9	18	18	9	6.612813	100	100
M (868MHz)	1.5	8.2	100	12	-	1	6.8	6.8	3	13.41015	100	100
H (915MHz)	2	6.8	22	12	-	1	6.8	6.8	3	14.15099	47	47

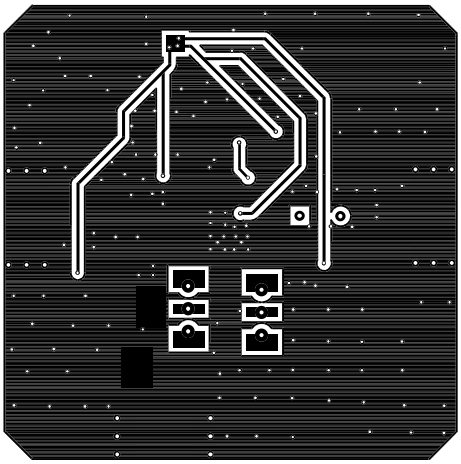
Evaluation Board Layout - M and H
Board Size 2.0” x 2.0”

Board Thickness 0.040”, Board Material FR-4, Multi-Layer
(Same board layout is being used for the -M and -H versions.)

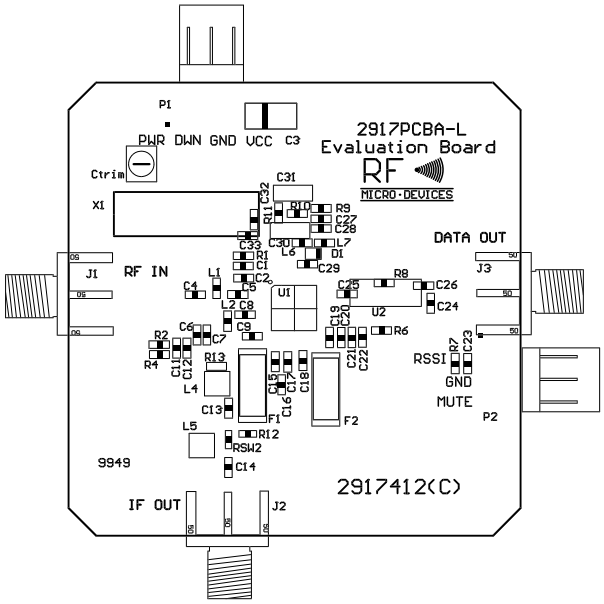


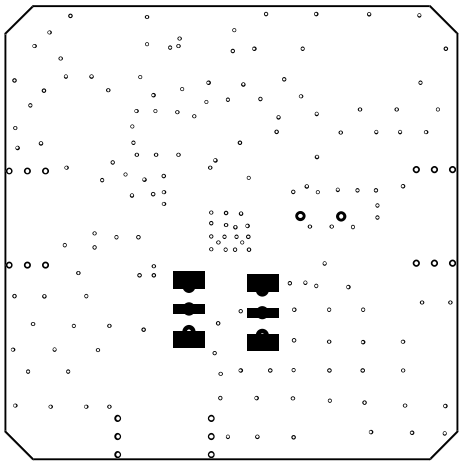


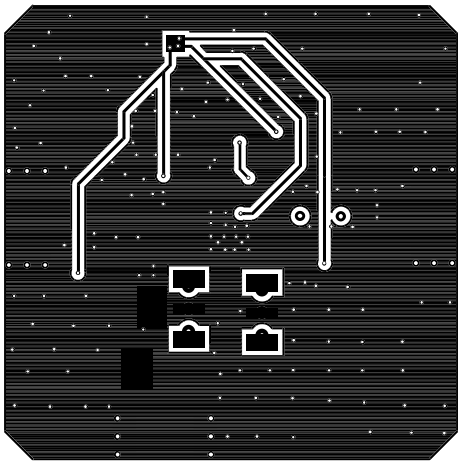




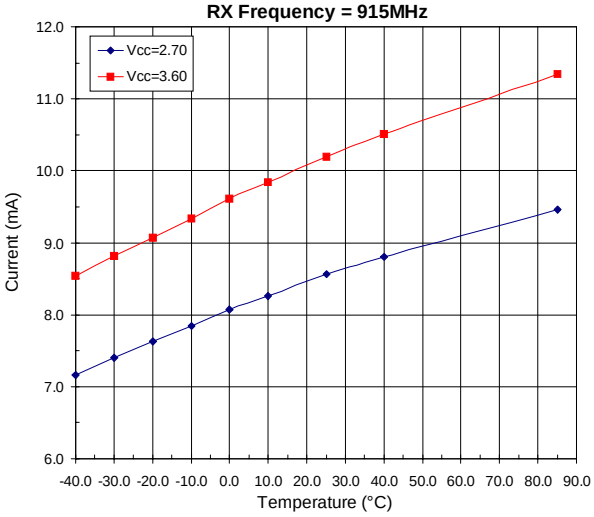
Evaluation Board Layout - L
Board Size 2.0” x 2.0”
Board Thickness 0.048”, Board Material FR-4, Multi-Layer



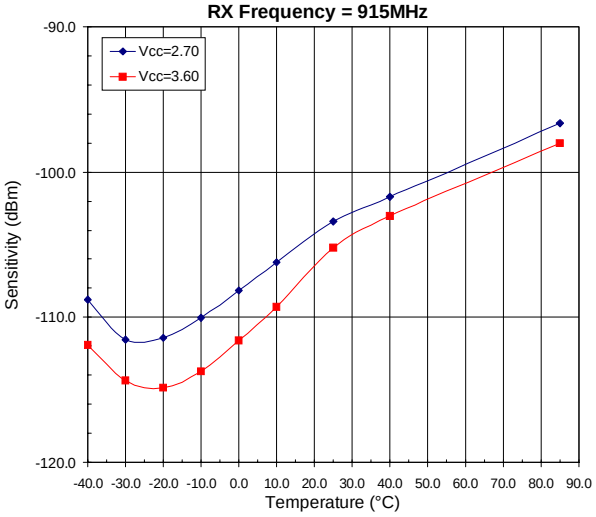




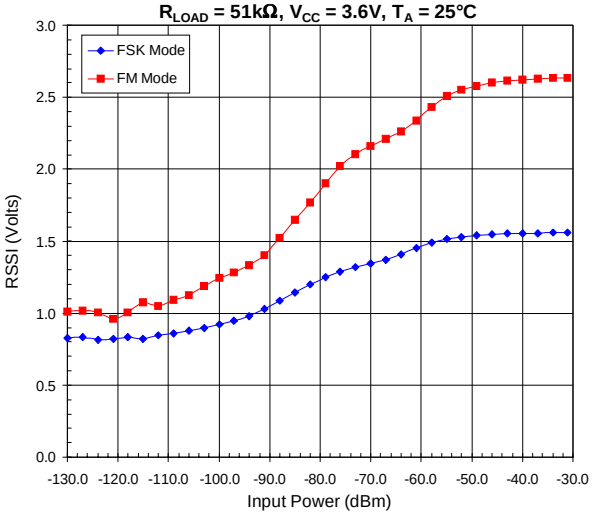
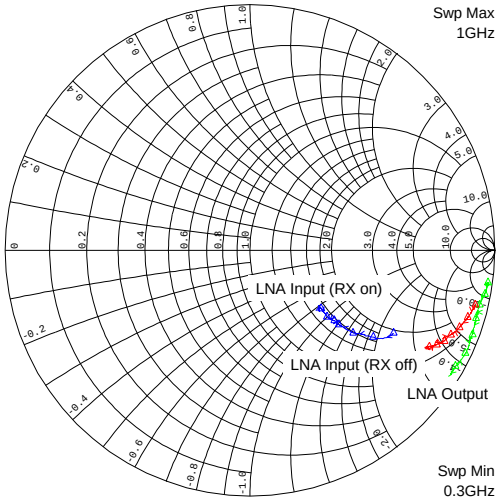
Current versus Temperature
RX Frequency = 915MHz



Sensitivity versus Temperature
RX Frequency = 915MHz



RSSI versus Input Power
R_{LOAD} = 51kΩ, V_{CC} = 3.6V, T_A = 25°C



LNA Impedance