TEXAS INSTRUMENTS

TL431, TL431A, TL431B
TL432, TL432A, TL432B

SLVS543O – AUGUST 2004 – REVISED JANUARY 2015

TL43xx Precision Programmable Reference

1 Features

- Reference Voltage Tolerance at 25°C
  - 0.5% (B Grade)
  - 1% (A Grade)
  - 2% (Standard Grade)
- Adjustable Output Voltage: V_{ref} to 36 V
- Operation From −40°C to 125°C
- Typical Temperature Drift (TL431B)
  - 6 mV (C Temp)
  - 14 mV (I Temp, Q Temp)
- Low Output Noise
- 0.2-Ω Typical Output Impedance
- Sink-Current Capability: 1 mA to 100 mA
-

2 Applications

- Adjustable Voltage and Current Referencing
- Secondary Side Regulation in Flyback SMPSs
- Zener Replacement
- Voltage Monitoring
- Comparator with Integrated Reference

3 Description

The TL431 and TL432 devices are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between V_{ref} (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies. The TL432 device has exactly the same functionality and electrical specifications as the TL431 device, but has different pinouts for the DBV, DBZ, and PK packages.

Both the TL431 and TL432 devices are offered in three grades, with initial tolerances (at 25°C) of 0.5%, 1%, and 2%, for the B, A, and standard grade, respectively. In addition, low output drift versus temperature ensures good stability over the entire temperature range.

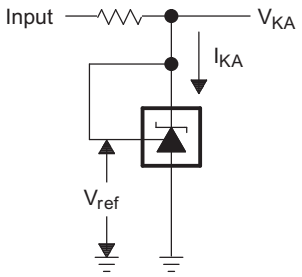
The TL43xxC devices are characterized for operation from 0°C to 70°C, the TL43xxI devices are characterized for operation from –40°C to 85°C, and the TL43xxQ devices are characterized for operation from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TL43xx	SOT-23-3 (3)	2.90 mm x 1.30 mm
	SOT-23-5 (5)	2.90 mm x 1.60 mm
	SOIC (8)	4.90 mm x 3.90 mm
	PDIP (8)	9.50 mm x 6.35 mm
	SOP (8)	6.20 mm x 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision N (January 2014) to Revision O — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, , *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added Applications. ... 1
- Moved *Typical Characteristics* into *Specifications* section. ... 14

Changes from Revision M (July 2012) to Revision N — **Page**

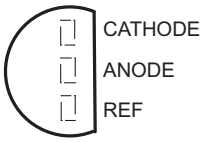
- Updated document formatting ... 1
- Removed *Ordering Information* table. ... 3
- Added Application Note links. ... 21

Changes from Revision K (June 2010) to Revision L — **Page**

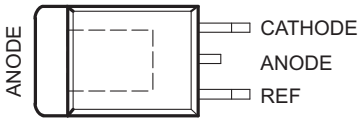
- Deleted T_A values under TEST CONDITIONS for $V_{I(dev)}$ and $I_{I(dev)}$ PARAMETERS in the *Electrical Characteristics* table. .. 5

6 Pin Configuration and Functions

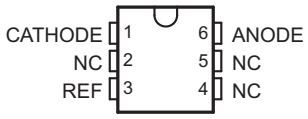
TL431, TL431A, TL431B . . . LP (TO-92/TO-226) PACKAGE
(TOP VIEW)



TL431 . . . KTP (PowerFLEX /TO-252) PACKAGE
(TOP VIEW)

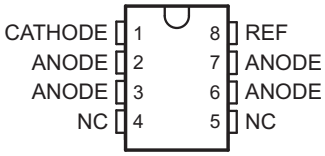


TL431A, TL431B . . . DCK (SC-70) PACKAGE
(TOP VIEW)



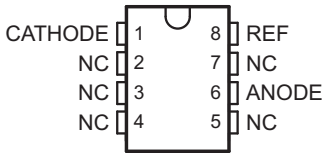
NC − No internal connection

TL431, TL431A, TL431B . . . D (SOIC) PACKAGE
(TOP VIEW)



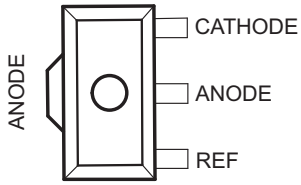
NC − No internal connection

TL431, TL431A, TL431B . . . P (PDIP), PS (SOP),
OR PW (TSSOP) PACKAGE
(TOP VIEW)

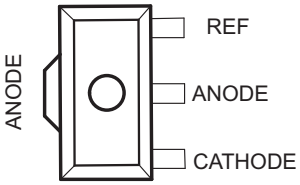


NC − No internal connection

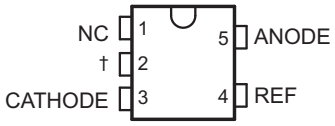
TL431, TL431A, TL431B . . . PK (SOT-89) PACKAGE
(TOP VIEW)



TL432, TL432A, TL432B . . . PK (SOT-89) PACKAGE
(TOP VIEW)

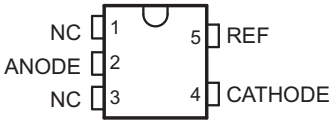


TL431, TL431A, TL431B . . . DBV (SOT-23-5) PACKAGE
(TOP VIEW)



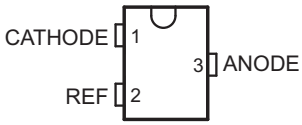
NC − No internal connection
† Pin 2 is attached to Substrate and must be connected to ANODE or left open.

TL432, TL432A, TL432B . . . DBV (SOT-23-5) PACKAGE
(TOP VIEW)

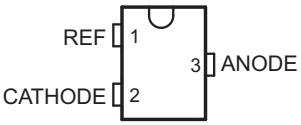


NC − No internal connection

TL431, TL431A, TL431B . . . DBZ (SOT-23-3) PACKAGE
(TOP VIEW)



TL432, TL432A, TL432B . . . DBZ (SOT-23-3) PACKAGE
(TOP VIEW)



Pin Functions

PIN												TYPE	DESCRIPTION
NAME	TLV431x								TLV432x				
	DBZ	DBV	PK	D	P, PS PW	LP	KTP	DCK	DBZ	DBV	PK		
CATHODE	1	3	3	1	1	1	1	1	2	4	1	I/O	Shunt Current/Voltage input
REF	2	4	1	8	8	3	3	3	1	5	3	I	Threshold relative to common anode
ANODE	3	5	2	2, 3, 6, 7	6	2	2	6	3	2	2	O	Common pin, normally connected to ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{KA}	Cathode voltage(2)		37	V
I_{KA}	Continuous cathode current range	–100	150	mA
$I_{I(ref)}$	Reference input current range	–0.05	10	mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ANODE, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Thermal Information

THERMAL METRIC(1)		TL43xx									UNIT
		P	PW	D	PS	DCK	DBV	DBZ	LP	PK	
		8 PINS				6 PINS	5 PINS	3 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85	149	97	95	259	206	206	140	52	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	65	39	46	87	131	76	55	9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.4 Recommended Operating Conditions

See(1)

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		V_{ref}	36	V
I_{KA}	Cathode current		1	100	mA
T_A	Operating free-air temperature	TL43xxC	0	70	°C
		TL43xxI	–40	85	
		TL43xxQ	–40	125	

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

7.5 Electrical Characteristics, TL431C, TL432C

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

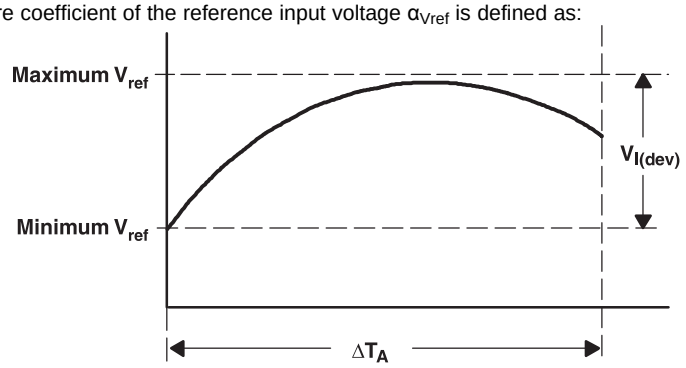
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431C, TL432C			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2440	2495	2550	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA,	SOT23-3 and TL432 devices		6	16	mV
				All other devices		4	25	
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.4	1.2	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	1	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	1	µA
$\lvert z_{KA} \rvert$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{Vref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $\lvert z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $\lvert z' \rvert = \frac{\Delta V}{\Delta I}$ which is approximately equal to $\lvert z_{KA} \rvert \left(1 + \frac{R1}{R2}\right)$.

7.6 Electrical Characteristics, TL431I, TL432I

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

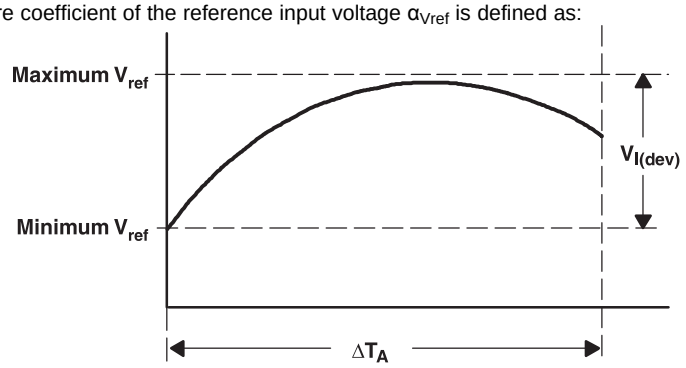
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431I, TL432I			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2440	2495	2550	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA	SOT23-3 and TL432 devices		14	34	mV
				All other devices		5	50	
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	2.5	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	1	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	1	µA
$\|z_{KA}\|$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$ which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

7.7 Electrical Characteristics, TL431Q, TL432Q

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

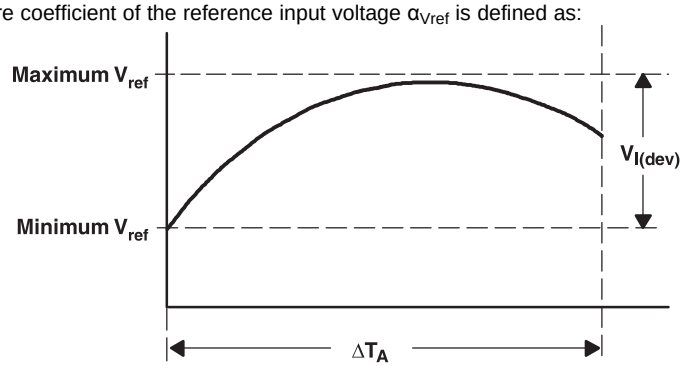
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431Q, TL432Q			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2440	2495	2550	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA			14	34	mV
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	2.5	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	1	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	1	µA
$\|z_{KA}\|$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{^\circ C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25^\circ C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$ which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

7.8 Electrical Characteristics, TL431AC, TL432AC

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

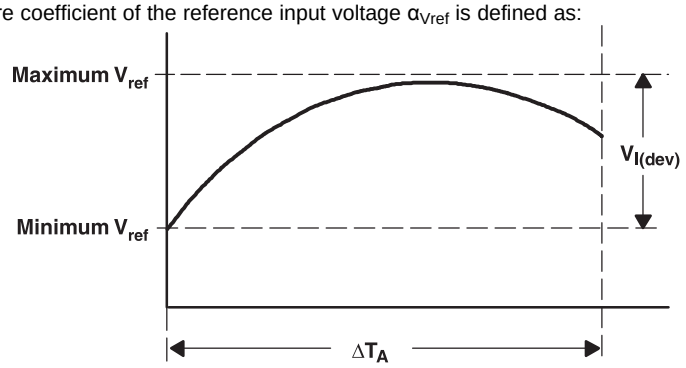
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431AC, TL432AC			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2470	2495	2520	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA	SOT23-3 and TL432 devices		6	16	mV
				All other devices		4	25	
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	1.2	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	0.6	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5	µA
$\|z_{KA}\|$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$

which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

7.9 Electrical Characteristics, TL431AI, TL432AI

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

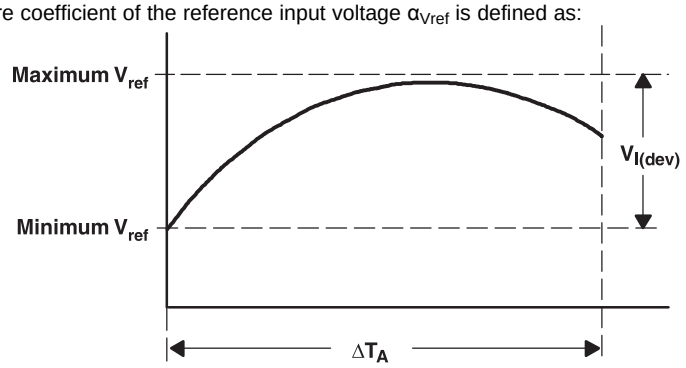
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431AI, TL432AI			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2470	2495	2520	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA	SOT23-3 and TL432 devices		14	34	mV
				All other devices		5	50	
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	2.5	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	0.7	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5	µA
$\lvert z_{KA} \rvert$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{Vref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $\lvert z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $\lvert z' \rvert = \frac{\Delta V}{\Delta I}$ which is approximately equal to $\lvert z_{KA} \rvert \left(1 + \frac{R1}{R2}\right)$.

7.10 Electrical Characteristics, TL431AQ, TL432AQ

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

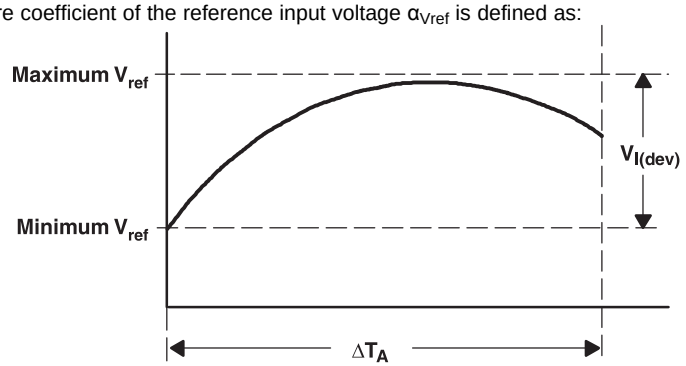
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431AQ, TL432AQ			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2470	2495	2520	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA			14	34	mV
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	2.5	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	0.7	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5	µA
$\lvert z_{KA} \rvert$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{^\circ C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25^\circ C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $\lvert z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $\lvert z' \rvert = \frac{\Delta V}{\Delta I}$ which is approximately equal to $\lvert z_{KA} \rvert \left(1 + \frac{R1}{R2}\right)$.

7.11 Electrical Characteristics, TL431BC, TL432BC

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

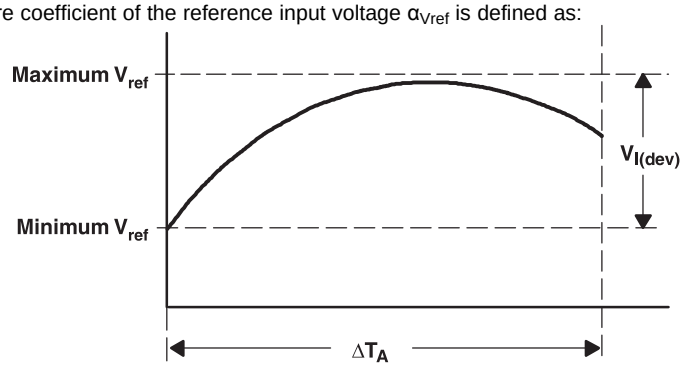
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431BC, TL432BC			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2483	2495	2507	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA			6	16	mV
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	1.2	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	0.6	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5	µA
$\|z_{KA}\|$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{^\circ C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25^\circ C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$ which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

7.12 Electrical Characteristics, TL431BI, TL432BI

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

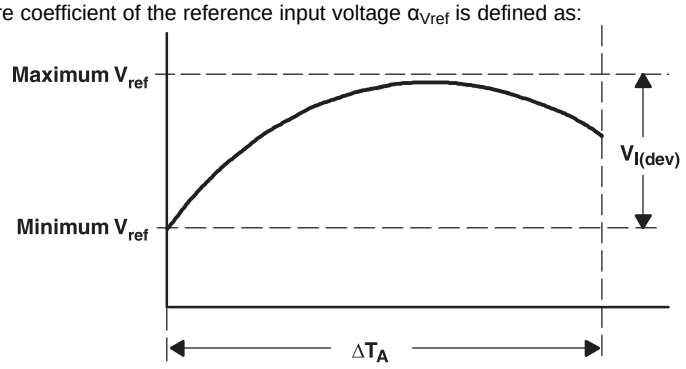
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431BI, TL432BI			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2483	2495	2507	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA			14	34	mV
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	2.5	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	0.7	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5	µA
$\|z_{KA}\|$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{^\circ C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25^\circ C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$ which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

7.13 Electrical Characteristics, TL431BQ, TL432BQ

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

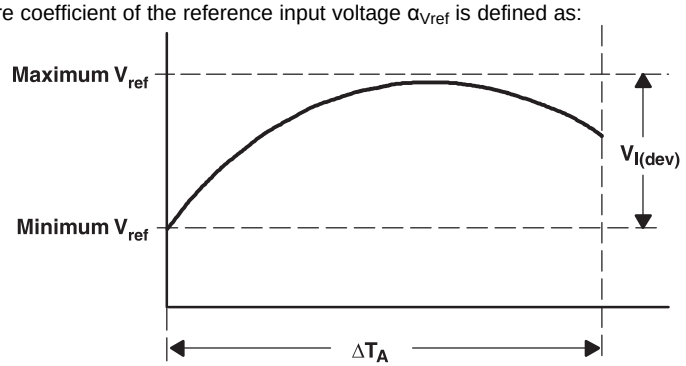
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431BQ, TL432BQ			UNIT
					MIN	TYP	MAX	
V_{ref}	Reference voltage	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA		2483	2495	2507	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range(1)	See Figure 20	V_{KA} = V_{ref}, I_{KA} = 10 mA			14	34	mV
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 21	I_{KA} = 10 mA	ΔV_{KA} = 10 V – V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V – 10 V		–1	–2	
I_{ref}	Reference input current	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range(1)	See Figure 21	I_{KA} = 10 mA, R1 = 10 kΩ, R2 = ∞			0.8	2.5	µA
I_{min}	Minimum cathode current for regulation	See Figure 20	V_{KA} = V_{ref}			0.4	0.7	mA
I_{off}	Off-state cathode current	See Figure 22	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5	µA
$\|z_{KA}\|$	Dynamic impedance(2)	See Figure 20	V_{KA} = V_{ref}, f ≤ 1 kHz, I_{KA} = 1 mA to 100 mA			0.2	0.5	Ω

(1) The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$\left|\alpha_{vref}\right| \left(\frac{ppm}{^\circ C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25^\circ C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

(2) The dynamic impedance is defined as: $|z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$

When the device is operating with two external resistors (see Figure 21), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$ which is approximately equal to $|z_{KA}|\left(1 + \frac{R1}{R2}\right)$.

7.14 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

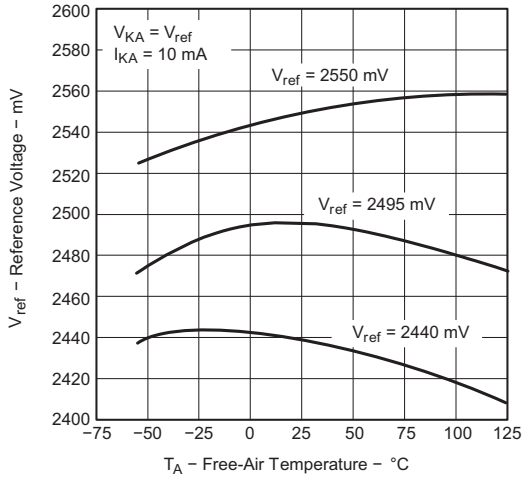


Figure 1. Reference Voltage vs Free-Air Temperature

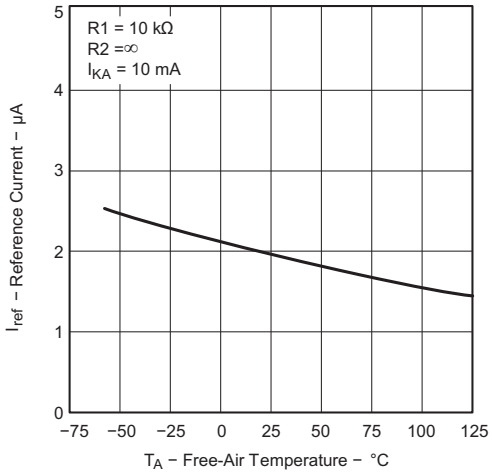


Figure 2. Reference Current vs Free-Air Temperature

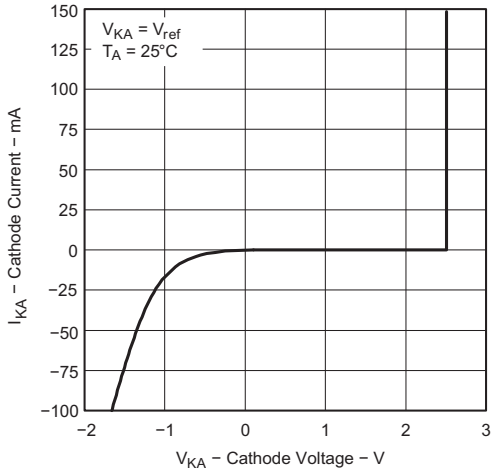


Figure 3. Cathode Current vs Cathode Voltage

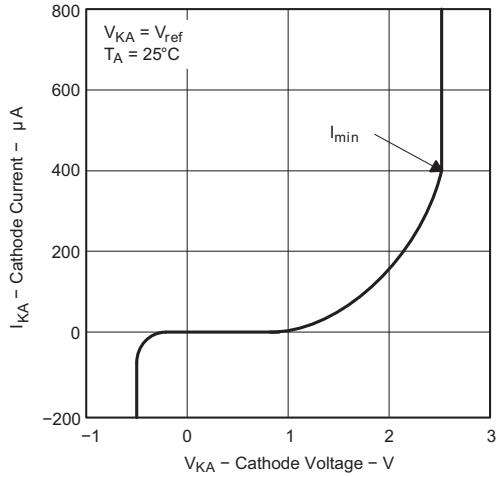


Figure 4. Cathode Current vs Cathode Voltage

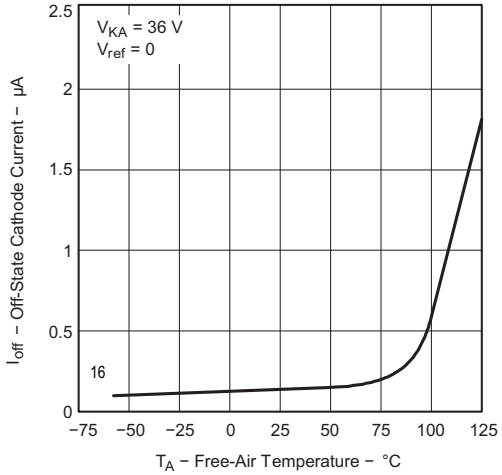


Figure 5. Off-State Cathode Current vs Free-Air Temperature

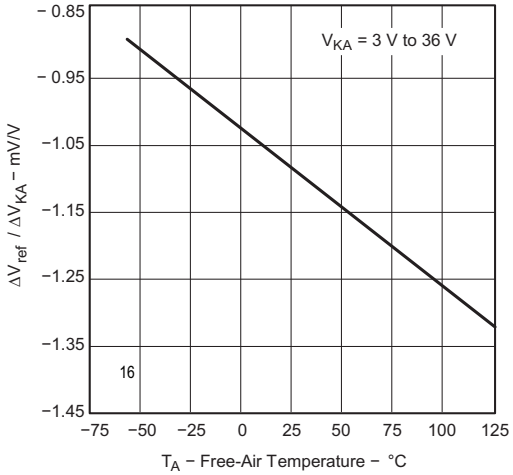


Figure 6. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Free-Air Temperature

Typical Characteristics (continued)

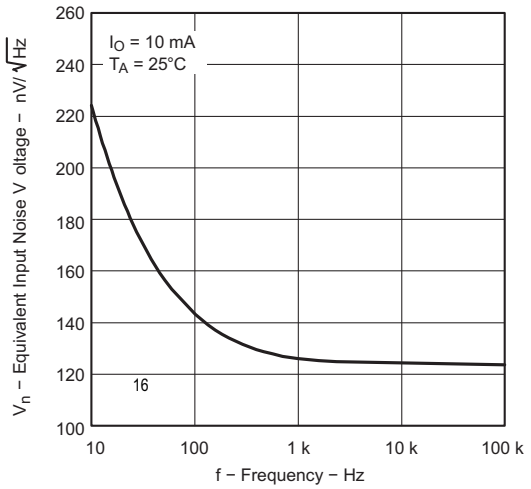


Figure 7. Equivalent Input Noise Voltage vs Frequency

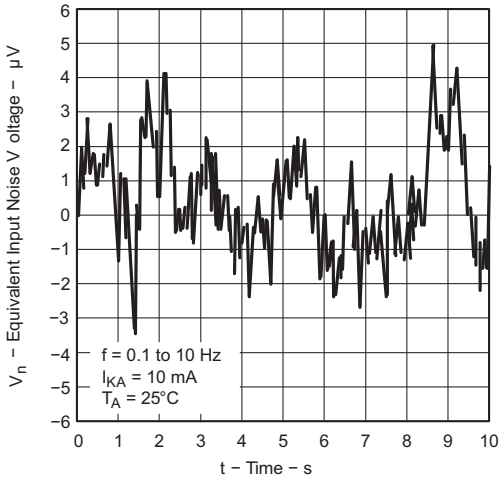


Figure 8. Equivalent Input Noise Voltage Over a 10-S Period

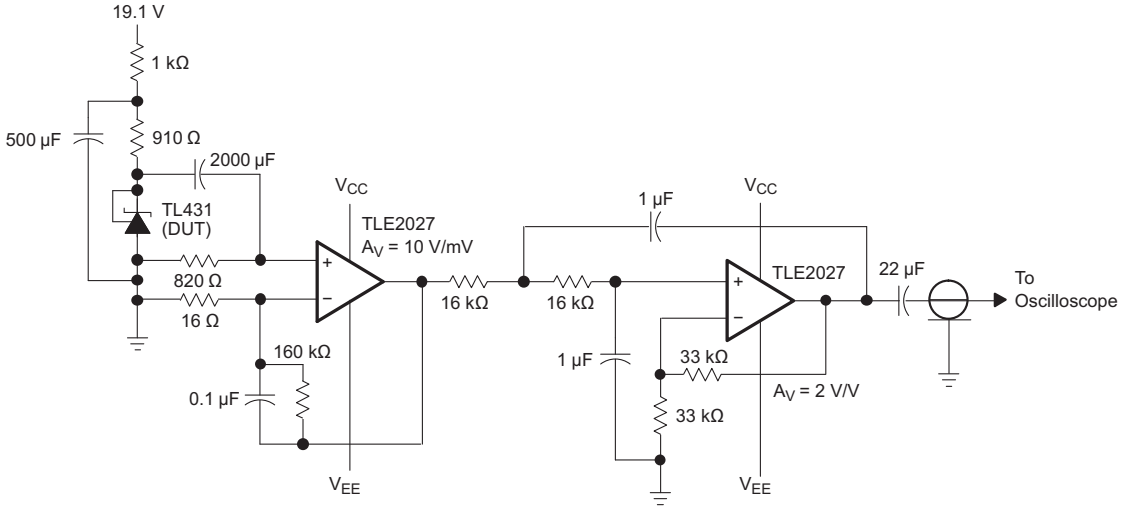


Figure 9. Test Circuit for Equivalent Input Noise Voltage Over a 10-S Period

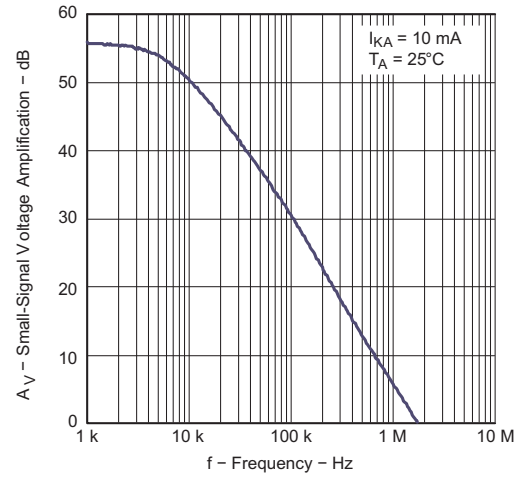


Figure 10. Small-Signal Voltage Amplification vs Frequency

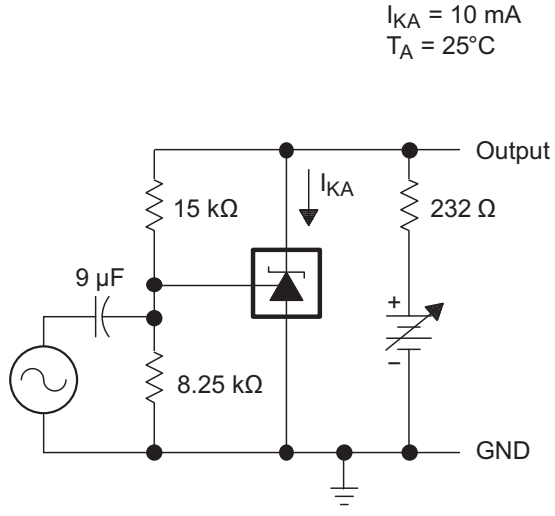


Figure 11. Test Circuit for Voltage Amplification

Typical Characteristics (continued)

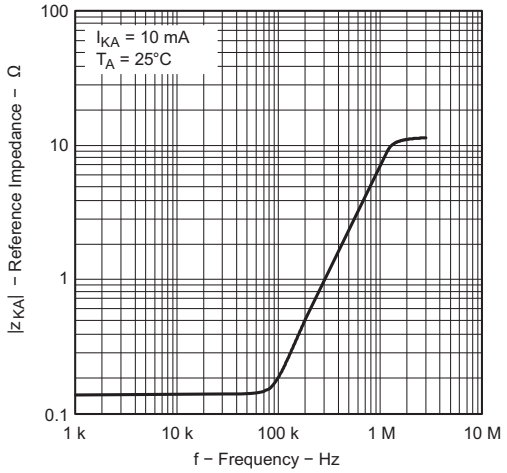


Figure 12. Reference Impedance vs Frequency

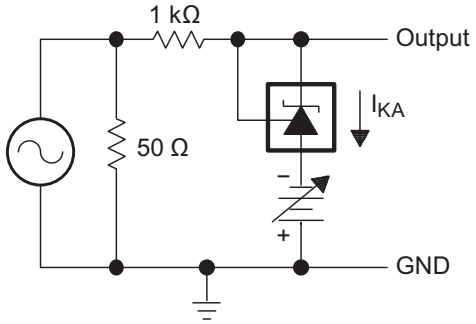


Figure 13. Test Circuit for Reference Impedance

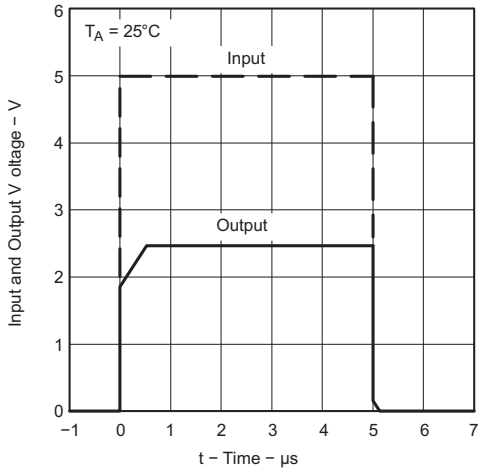


Figure 14. Pulse Response

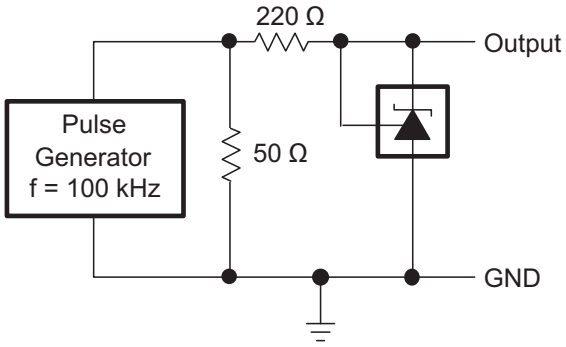
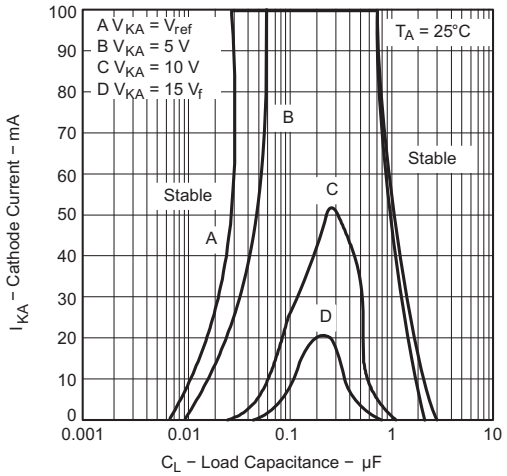


Figure 15. Test Circuit for Pulse Response



The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions, with C_L = 0. V_{BATT} and C_L then are adjusted to determine the ranges of stability.

Figure 16. Stability Boundary Conditions for All TL431 and TL431A Devices
(Except for SOT23-3, SC-70, and Q-Temp Devices)

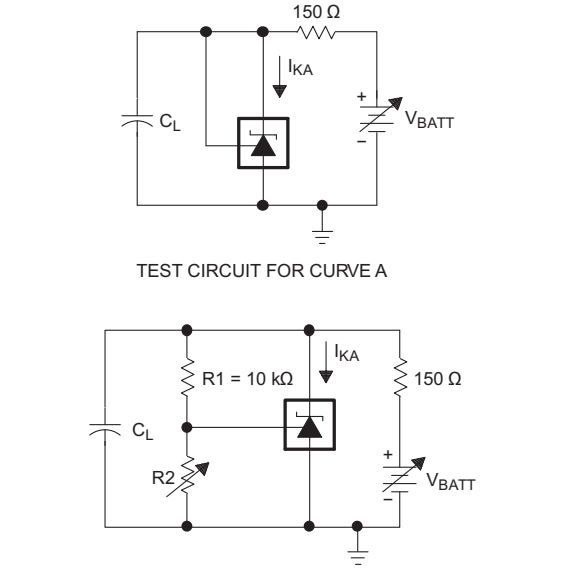
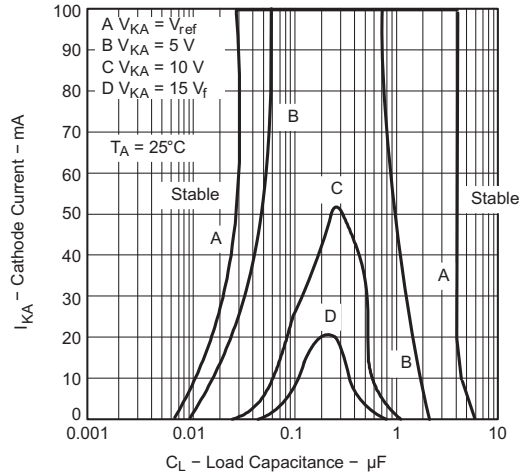


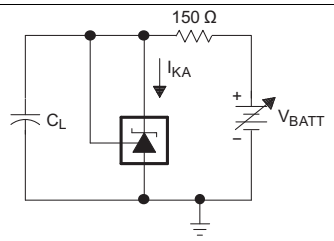
Figure 17. Test Circuits for Stability Boundary Conditions

Typical Characteristics (continued)

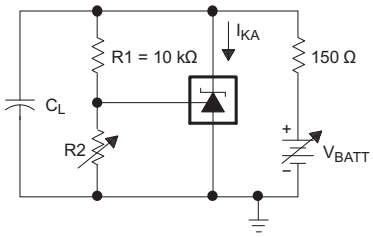


The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions, with C_L = 0. V_{BATT} and C_L then are adjusted to determine the ranges of stability.

Figure 18. Stability Boundary Conditions for All TL431B, TL432, SOT-23, SC-70, and Q-Temp Devices



TEST CIRCUIT FOR CURVE A



TEST CIRCUIT FOR CURVES B, C, AND D

Figure 19. Test Circuit for Stability Boundary Conditions

8 Parameter Measurement Information

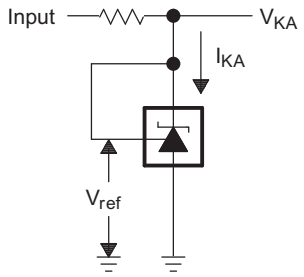


Figure 20. Test Circuit for $V_{KA} = V_{ref}$

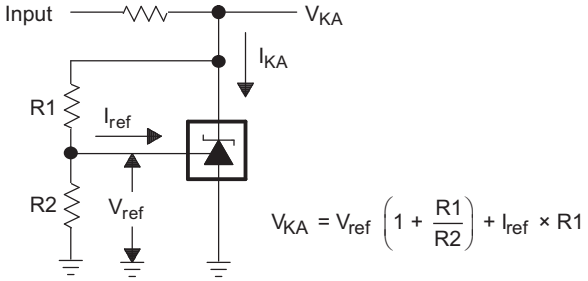


Figure 21. Test Circuit for $V_{KA} > V_{ref}$

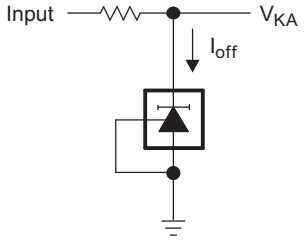


Figure 22. Test Circuit for I_{off}

9 Detailed Description

9.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications, ranging from power to signal path. This is due to it's key components containing an accurate voltage reference & opamp, which are very fundamental analog building blocks. TL43xx is used in conjunction with it's key components to behave as a single voltage reference, error amplifier, voltage clamp or comparator with integrated reference.

TL43xx can be operated and adjusted to cathode voltages from 2.5V to 36V, making this part optimum for a wide range of end equipments in industrial, auto, telecom & computing. In order for this device to behave as a shunt regulator or error amplifier, >1mA (I_{min}(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, 1%, and 2%. These reference options are denoted by B (0.5%), A (1.0%) and blank (2.0%) after the TL431 or TL432. TL431 & TL432 are both functionaly, but have separate pinout options.

The TL43xxC devices are characterized for operation from 0°C to 70°C, the TL43xxI devices are characterized for operation from –40°C to 85°C, and the TL43xxQ devices are characterized for operation from –40°C to 125°C.

9.2 Functional Block Diagram

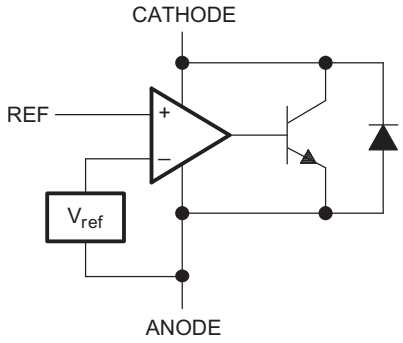


Figure 23. Equivalent Schematic

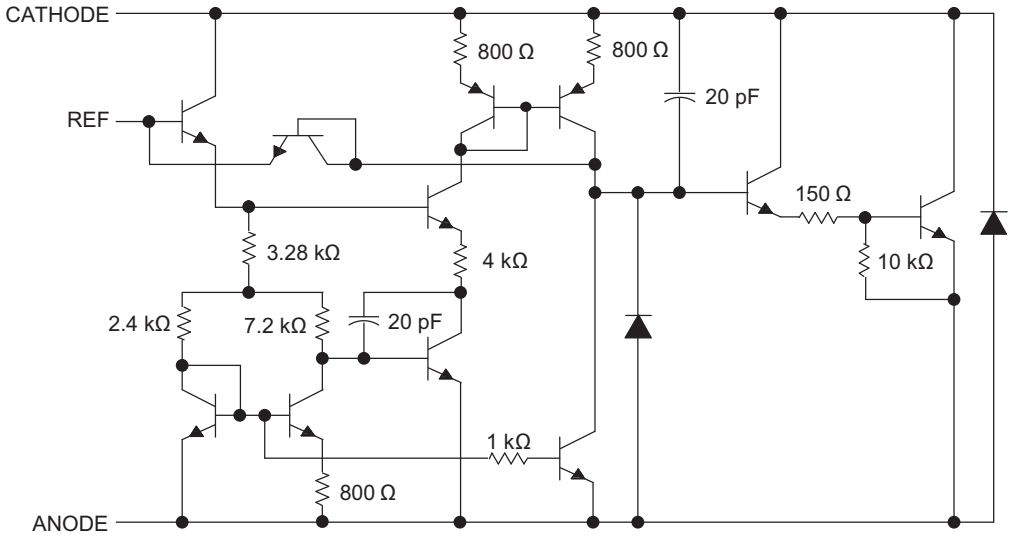


Figure 24. Detailed Schematic

9.3 Feature Description

TL43xx consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, shown in the above schematic (Figure 24). A Darlington pair is used in order for this device to be able to sink a maximum current of 100 mA.

When operated with enough voltage headroom (≥ 2.5 V) and cathode current (I_{KA}), TL431 forces the reference pin to 2.5 V. However, the reference pin can not be left floating, as it needs I_{REF} ≥ 4 µA (please see *Electrical Characteristics, TL431C, TL432C*). This is because the reference pin is driven into an npn, which needs base current in order operate properly.

When feedback is applied from the Cathode and Reference pins, TL43xx behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations in order for it to be in the proper linear region giving TL43xx enough gain.

Unlike many linear regulators, TL43xx is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor Figure 24 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

9.4 Device Functional Modes

9.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of TL43xx is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, TL43xx will have the characteristics shown in Figure 23. With such high gain in this configuration, TL43xx is typically used as a comparator. With the reference integrated makes TL43xx the prefered choice when users are trying to monitor a certain level of a single signal.

9.4.2 Closed Loop

When the cathode/output voltage or current of TL43xx is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TL43xx use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail. The linked application notes will help the designer make the best choices when using this part.

Application note SLVA482 will provide a deeper understanding of this devices stability characteristics and aid the user in making the right choices when choosing a load capacitor. Application note SLVA445 assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

10.2 Typical Applications

10.2.1 Comparator With Integrated Reference

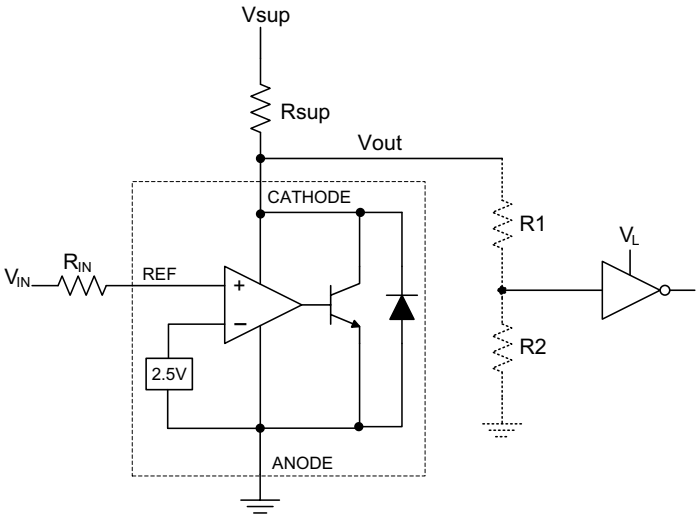


Figure 25. Comparator Application Schematic

Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters listed in *Table 1* as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to 5 V
Input Resistance	10 kΩ
Supply Voltage	24 V
Cathode Current (Ik)	5 mA
Output Voltage Level	~2 V – V_{SUP}
Logic Input Thresholds VIH/VIL	V_L

10.2.1.2 Detailed Design Procedure

When using TL431 as a comparator with reference, determine the following:

- Input Voltage Range
- Reference Voltage Accuracy
- Output logic input high and low level thresholds
- Current Source resistance

10.2.1.2.1 Basic Operation

In the configuration shown in Figure 25 TL431 will behave as a comparator, comparing the V_{REF} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_K), TL43xx will have enough open loop gain to provide a quick response. This can be seen in Figure 26, where the R_{SUP}=10 kΩ (I_{KA}=500 µA) situation responds much slower than R_{SUP}=1 kΩ (I_{KA}=5 mA). With the TL43xx's max Operating Current (I_{MIN}) being 1 mA, operation below that could result in low gain, leading to a slow response.

10.2.1.2.1.1 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of 2.5 V ±(0.5%, 1.0% or 1.5%) depending on which version is being used. The more overdrive voltage provided, the faster the TL431 will respond.

For applications where TL431 is being used as a comparator, it is best to set the trip point to greater than the positive expected error (i.e. +1.0% for the A version). For fast response, setting the trip point to >10% of the internal V_{REF} should suffice.

For minimal voltage drop or difference from Vin to the ref pin, it is recommended to use an input resistor <10kΩ to provide Iref.

10.2.1.2.2 Output Voltage and Logic Input Level

In order for TL431 to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} & V_{IL}.

As seen in Figure 26, TL431's output low level voltage in open-loop/comparator mode is ~2 V, which is typically sufficient for 5V supplied logic. However, would not work for 3.3 V & 1.8 V supplied logic. In order to accomodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

TL431's output high voltage is equal to V_{SUP} due to TL431 being open-collector. If V_{SUP} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accomadate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 & R2 in Figure 25) is much greater than R_{SUP} in order to not interfere with TL431's ability to pull close to V_{SUP} when turning off.

10.2.1.2.2.1 Input Resistance

TL431 requires an input resistance in this application in order to source the reference current (I_{REF}) needed from this device to be in the proper operating regions while turing on. The actual voltage seen at the ref pin will be $V_{REF}=V_{IN}-I_{REF}*R_{IN}$. Since I_{REF} can be as high as 4 µA it is recommended to use a resistance small enough that will mitigate the error that I_{REF} creates from V_{IN}.

10.2.1.3 Application Curves

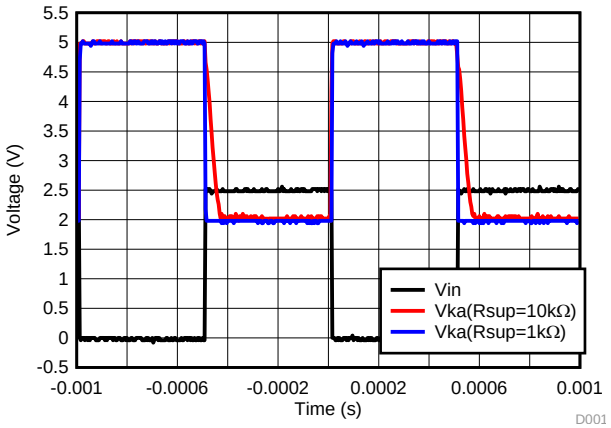


Figure 26. Output Response With Various Cathode Currents

10.2.2 Shunt Regulator/Reference

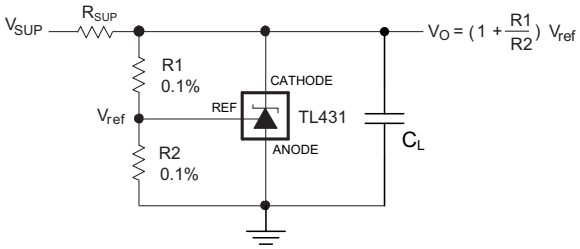


Figure 27. Shunt Regulator Schematic

10.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0 %
Supply Voltage	24 V
Cathode Current (Ik)	5 mA
Output Voltage Level	2.5 V - 36 V
Load Capacitance	100 nF
Feedback Resistor Values and Accuracy (R1 & R2)	10 kΩ

10.2.2.2 Detailed Design Procedure

When using TL431 as a Shunt Regulator, determine the following:

- Input Voltage Range
- Temperature Range
- Total Accuracy
- Cathode Current
- Reference Initial Accuracy
- Output Capacitance

10.2.2.2.1 Programming Output/Cathode Voltage

In order to program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 27, with R1 & R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Figure 27. The cathode voltage can be more accuratel determined by taking in to account the cathode current:

$Vo=(1+R1/R2)*V_{REF}-I_{REF}*R1$

In order for this equation to be valid, TL43xx must be fully biased so that it has enough open loop gain to mitigate any gain error. This can be done by meeting the Imin spec denoted in *Electrical Characteristics, TL431C, TL432C*.

10.2.2.2.2 Total Accuracy

When programming the output above unity gain (V_{KA}=V_{REF}), TL43xx is susceptible to other errors that may effect the overall accuracy beyond V_{REF}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ - Change in reference voltage over temperature
- ΔV_{REF} / ΔV_{KA} - Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ - Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account. Application note SLVA445 assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

10.2.2.2.3 Stability

Though TL43xx is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TL43xx region of stability, shown inFigure 16 and Figure 18. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling. When using additional capacitance between Cathode and Anode, refer to Figure 16 and Figure 18. Also, application note SLVA482 will provide a deeper understanding of this devices stability characteristics and aid the user in making the right choices when choosing a load capacitor.

10.2.2.2.4 Start-up Time

As shown in Figure 28, TL43xx has a fast response up to ~2 V and then slowly charges to it's programmed value. This is due to the compensation capacitance (shown in Figure 24) the TL43xx has to meet it's stability criteria. Despite the secondary delay, TL43xx still has a fast response suitable for many clamp applications.

10.2.2.3 Application Curves

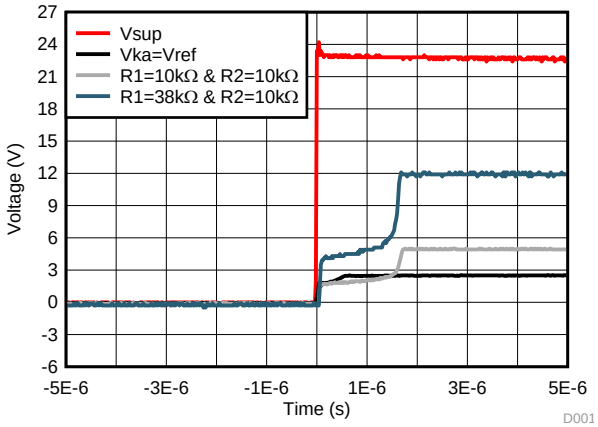
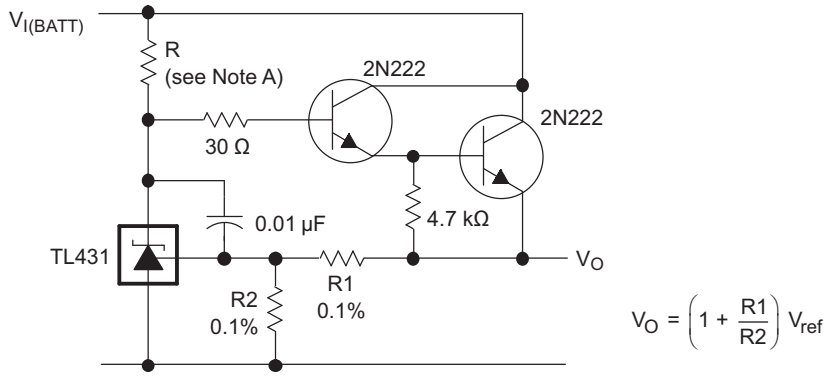


Figure 28. TL43xx Start-up Response

10.3 System Examples



A. R should provide cathode current ≥1 mA to the TL431 at minimum $V_{(BATT)}$.

Figure 29. Precision High-Current Series Regulator

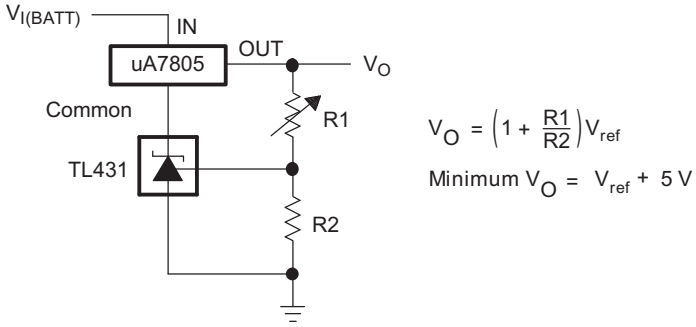


Figure 30. Output Control of a Three-Terminal Fixed Regulator

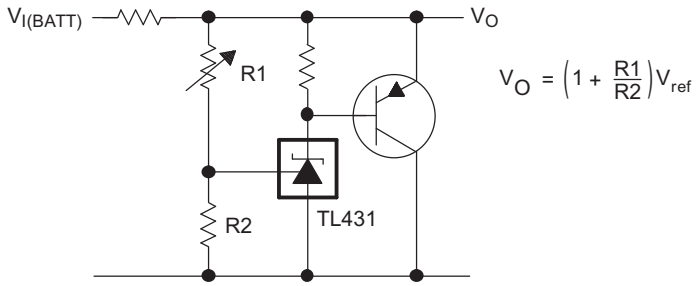
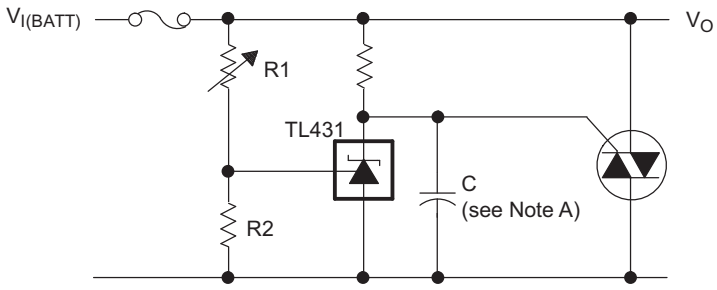


Figure 31. High-Current Shunt Regulator



A. Refer to the stability boundary conditions in Figure 16 and Figure 18 to determine allowable values for C.

Figure 32. Crowbar Circuit

System Examples (continued)

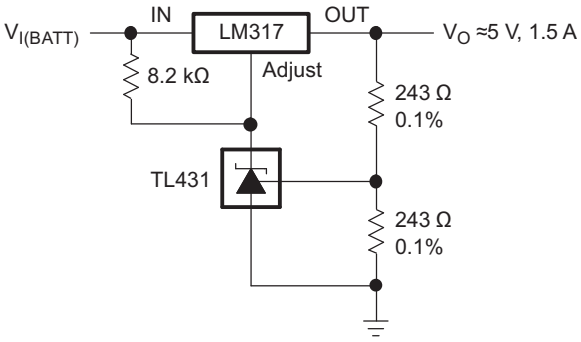
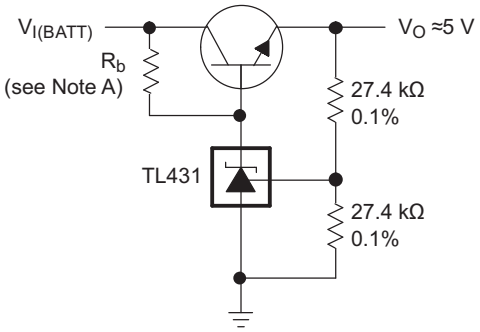


Figure 33. Precision 5-V, 1.5-A Regulator



A. R_b should provide cathode current ≥1 mA to the TL431.

Figure 34. Efficient 5-V Precision Regulator

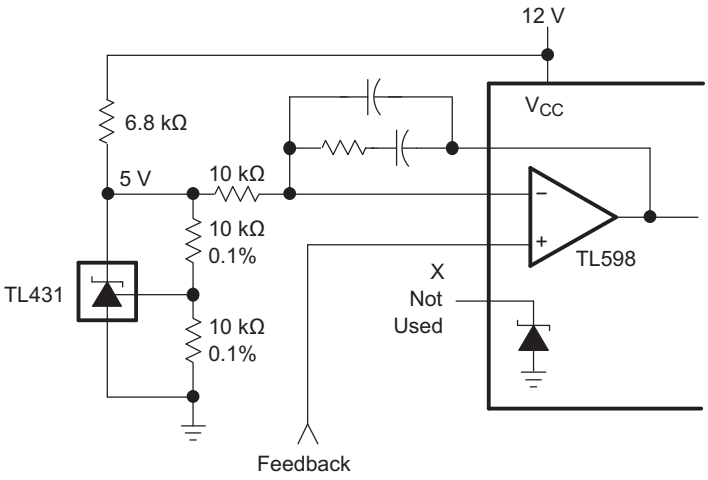
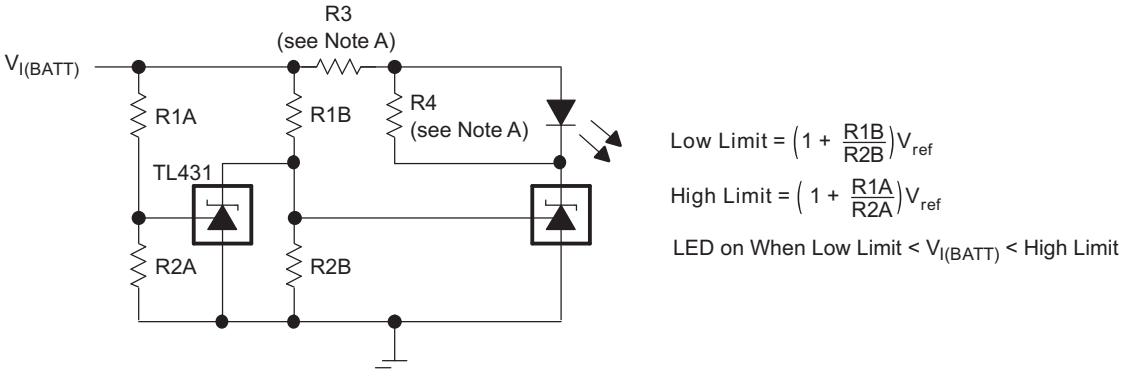


Figure 35. PWM Converter With Reference

System Examples (continued)



A. Select R3 and R4 to provide the desired LED intensity and cathode current ≥1 mA to the TL431 at the available $V_{I(BATT)}$.

Figure 36. Voltage Monitor

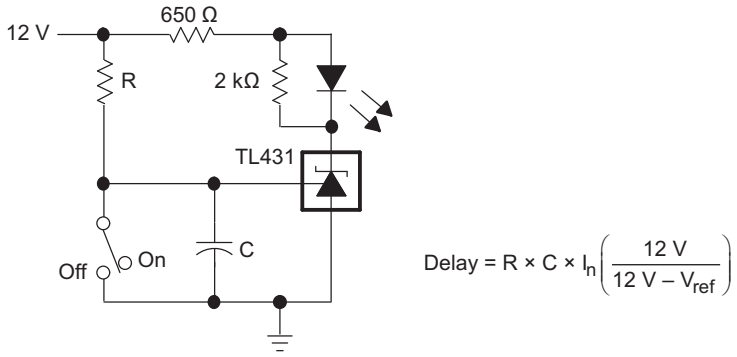


Figure 37. Delay Timer

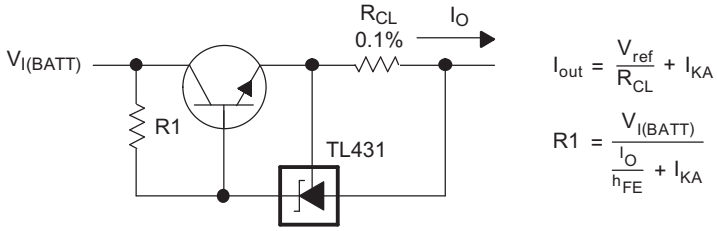


Figure 38. Precision Current Limiter

System Examples (continued)

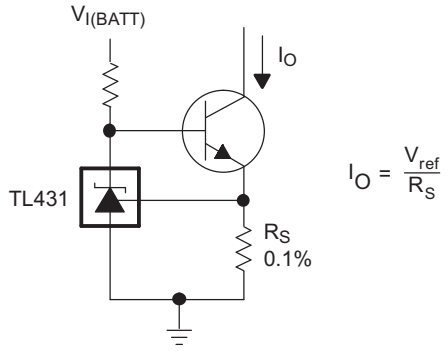


Figure 39. Precision Constant-Current Sink

11 Power Supply Recommendations

When using TL43xx as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 16 and Figure 18.

In order to not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed it's absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

12 Layout

12.1 Layout Guidelines

Bypass capacitors should be placed as close to the part as possible. Current-carrying traces need to have widths appropriate for the amount of current they are carrying; in the case of the TL43xx, these currents will be low.

12.2 Layout Example

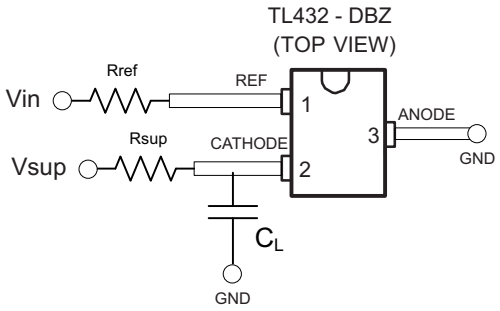


Figure 40. DBZ Layout example

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL431	Click here	Click here	Click here	Click here	Click here
TL431A	Click here	Click here	Click here	Click here	Click here
TL431B	Click here	Click here	Click here	Click here	Click here
TL432	Click here	Click here	Click here	Click here	Click here
TL432A	Click here	Click here	Click here	Click here	Click here
TL432B	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.4 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	431AC	Samples
TL431ACDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(TACG, TACS)	Samples
TL431ACDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TACG	Samples
TL431ACDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TACG	Samples
TL431ACDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(TACG, TACU)	Samples
TL431ACDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(TAC3, TACS, TACU)	Samples
TL431ACDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(TAC3, TACS, TACU)	Samples
TL431ACDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(TAC3, TACS, TACU)	Samples
TL431ACDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(TAC3, TACS, TACU)	Samples
TL431ACDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T4S, T4U)	Samples
TL431ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	431AC	Samples
TL431ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	431AC	Samples
TL431ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	431AC	Samples
TL431ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	431AC	Samples
TL431ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431AC	Samples
TL431ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431AC	Samples
TL431ACLPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431ACLPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431AC	Samples
TL431ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431AC	Samples
TL431ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431AC	Samples
TL431ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL431ACP	Samples
TL431ACPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	4A	Samples
TL431ACPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	4A	Samples
TL431ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431A	Samples
TL431ACPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431A	Samples
TL431ACPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431A	Samples
TL431AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	431AI	Samples
TL431AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(TAIG, TAIS)	Samples
TL431AIDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TAIG	Samples
TL431AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TAIG	Samples
TL431AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(TAIG, TAIU)	Samples
TL431AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TAIG	Samples
TL431AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TAI3, TAIS, TAIU)	Samples
TL431AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TAI3, TAIS, TAIU)	Samples
TL431AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TAI3, TAIS, TAIU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TAI3, TAIS, TAIU)	Samples
TL431AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T5U	Samples
TL431AIDCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T5U	Samples
TL431AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T5U	Samples
TL431AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T5U	Samples
TL431AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	431AI	Samples
TL431AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	431AI	Samples
TL431AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	431AI	Samples
TL431AILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431AI	Samples
TL431AILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431AI	Samples
TL431AILPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431AI	Samples
TL431AILPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431AI	Samples
TL431AILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431AI	Samples
TL431AILPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431AI	Samples
TL431AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL431AIP	Samples
TL431AIPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL431AIP	Samples
TL431AIPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	4B	Samples
TL431AIPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	4B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431AQDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(TAQG, TAQU)	Samples
TL431AQDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(TAQG, TAQU)	Samples
TL431AQDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(TAQ3, TAQS, TAQU)	Samples
TL431AQDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(TAQ3, TAQS, TAQU)	Samples
TL431AQDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(TAQS, TAQU)	Samples
TL431AQDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(TAQS, TAQU)	Samples
TL431AQDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T7U	Samples
TL431AQDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T7U	Samples
TL431AQPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	4D	Samples
TL431AQPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	4D	Samples
TL431BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431B	Samples
TL431BCDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(T3GG, T3GU)	Samples
TL431BCDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(T3GG, T3GU)	Samples
TL431BCDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T3GG	Samples
TL431BCDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T3G3, T3GS, T3GU)	Samples
TL431BCDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T3G3, T3GS, T3GU)	Samples
TL431BCDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T3G3, T3GS, T3GU)	Samples
TL431BCDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T3G3, T3GS, T3GU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431BCDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T2U	Samples
TL431BCDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T2U	Samples
TL431BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431B	Samples
TL431BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431B	Samples
TL431BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431B	Samples
TL431BCLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	T431B	Samples
TL431BCLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	T431B	Samples
TL431BCLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	T431B	Samples
TL431BCP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL431BCP	Samples
TL431BCPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	4C	Samples
TL431BCPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	4C	Samples
TL431BCPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431B	Samples
TL431BCPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431B	Samples
TL431BID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z431B	Samples
TL431BIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(T3FG, T3FU)	Samples
TL431BIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(T3FG, T3FU)	Samples
TL431BIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T3FG	Samples
TL431BIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3F3, T3FS, T3FU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431BIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3F3, T3FS, T3FU)	Samples
TL431BIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3F3, T3FS, T3FU)	Samples
TL431BIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3F3, T3FS, T3FU)	Samples
TL431BIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T3U	Samples
TL431BIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T3U	Samples
TL431BIDCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T3U	Samples
TL431BIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T3U	Samples
TL431BIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z431B	Samples
TL431BIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z431B	Samples
TL431BIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	Z431B	Samples
TL431BIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z431B	Samples
TL431BIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z431B	Samples
TL431BILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	Z431B	Samples
TL431BILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	Z431B	Samples
TL431BILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	Z431B	Samples
TL431BILPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	Z431B	Samples
TL431BIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL431BIP	Samples
TL431BIPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	4I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431BIPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	4I	Samples
TL431BQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T431BQ	Samples
TL431BQDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3HU	Samples
TL431BQDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3HU	Samples
TL431BQDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3HU	Samples
TL431BQDBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3HU	Samples
TL431BQDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T3H3, T3HS, T3HU)	Samples
TL431BQDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T3H3, T3HS, T3HU)	Samples
TL431BQDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T3HS, T3HU)	Samples
TL431BQDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T3HS, T3HU)	Samples
TL431BQDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T8U	Samples
TL431BQDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T8U	Samples
TL431BQDCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T8U	Samples
TL431BQDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T431BQ	Samples
TL431BQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T431BQ	Samples
TL431BQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T431BQ	Samples
TL431BQLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	T431BQ	Samples
TL431BQLPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	T431BQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431BQLPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	T431BQ	Samples
TL431BQLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	T431BQ	Samples
TL431BQLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	T431BQ	Samples
TL431BQPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	3H	Samples
TL431BQPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	3H	Samples
TL431BQPSR	PREVIEW	SO	PS	8	2000	TBD	Call TI	Call TI	-40 to 125		
TL431CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL431C	Samples
TL431CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(T3CG, T3CS)	Samples
TL431CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(T3CG, T3CS)	Samples
TL431CDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T3CG	Samples
TL431CDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T3C3, T3CS, T3CU)	Samples
TL431CDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T3C3, T3CS, T3CU)	Samples
TL431CDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T3CS, T3CU)	Samples
TL431CDBZTG4	ACTIVE	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	0 to 70	(T3CS, T3CU)	Samples
TL431CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL431C	Samples
TL431CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL431C	Samples
TL431CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	TL431C	Samples
TL431CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TL431C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431C	Samples
TL431CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431C	Samples
TL431CLPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431C	Samples
TL431CLPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431C	Samples
TL431CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431C	Samples
TL431CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	TL431C	Samples
TL431CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL431CP	Samples
TL431CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL431CP	Samples
TL431CPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	43	Samples
TL431CPKE6	ACTIVE	SOT-89	PK	3	1000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	0 to 70	43	Samples
TL431CPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	43	Samples
TL431CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431	Samples
TL431CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431	Samples
TL431CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T431	Samples
TL431ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL431I	Samples
TL431IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(T3IG, T3IS)	Samples
TL431IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T3IG	Samples
TL431IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T3IG	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(T3IG, T3IU)	Samples
TL431IDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3I3, T3IS, T3IU)	Samples
TL431IDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3I3, T3IS, T3IU)	Samples
TL431IDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3IS, T3IU)	Samples
TL431IDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T3IS, T3IU)	Samples
TL431IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL431I	Samples
TL431IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	TL431I	Samples
TL431IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL431I	Samples
TL431IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL431I	Samples
TL431ILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431I	Samples
TL431ILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431I	Samples
TL431ILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431I	Samples
TL431ILPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	TL431I	Samples
TL431IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL431IP	Samples
TL431IPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL431IP	Samples
TL431IPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	3I	Samples
TL431IPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	3I	Samples
TL431QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T431Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL431QDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(T3QG, T3QU)	Samples
TL431QDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3QG	Samples
TL431QDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(T3QG, T3QU)	Samples
TL431QDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T3Q3, T3QS, T3QU)	Samples
TL431QDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T3Q3, T3QS, T3QU)	Samples
TL431QDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T3QS, T3QU)	Samples
TL431QDBZTG4	ACTIVE	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 125	(T3QS, T3QU)	Samples
TL431QDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T6U	Samples
TL431QDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T6U	Samples
TL431QDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T6U	Samples
TL431QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T431Q	Samples
TL431QPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	3Q	Samples
TL431QPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	3Q	Samples
TL432ACDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(T4BG, T4BU)	Samples
TL432ACDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T4B3, T4BS, T4BU)	Samples
TL432ACDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T4B3, T4BS, T4BU)	Samples
TL432ACDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T4BS, T4BU)	Samples
TL432ACDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T4BS, T4BU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL432AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(T4AG, T4AU)	Samples
TL432AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4A3, T4AS, T4AU)	Samples
TL432AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4A3, T4AS, T4AU)	Samples
TL432AIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4A3, T4AS, T4AU)	Samples
TL432AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4A3, T4AS, T4AU)	Samples
TL432AIPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	2E	Samples
TL432AQDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T4DU	Samples
TL432AQDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T4DU	Samples
TL432AQDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	T4DU	Samples
TL432AQDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T4D3, T4DS, T4DU)	Samples
TL432AQDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T4D3, T4DS, T4DU)	Samples
TL432AQDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T4DS, T4DU)	Samples
TL432AQDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T4DS, T4DU)	Samples
TL432AQPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	2F	Samples
TL432AQPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	2F	Samples
TL432BCDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TBCU	Samples
TL432BCDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(TBCS, TBCU)	Samples
TL432BCDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(TBCS, TBCU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL432BCDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(TBCS, TBCU)	Samples
TL432BCPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	2G	Samples
TL432BIDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4F3, T4FS, T4FU)	Samples
TL432BIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4F3, T4FS, T4FU)	Samples
TL432BIDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4F3, T4FS, T4FU)	Samples
TL432BIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4F3, T4FS, T4FU)	Samples
TL432BIPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	2H	Samples
TL432BQDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T4H3, T4HS, T4HU)	Samples
TL432BQDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T4H3, T4HS, T4HU)	Samples
TL432BQPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	2J	Samples
TL432CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	(T4CG, T4CU)	Samples
TL432CDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(T4CS, T4CU)	Samples
TL432CPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	2A	Samples
TL432IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(T4IG, T4IU)	Samples
TL432IDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4IS, T4IU)	Samples
TL432IDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T4IS, T4IU)	Samples
TL432IPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	2B	Samples
TL432QDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T4QS, T4QU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL432QPK	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	2C	Samples
TL432QPKG3	ACTIVE	SOT-89	PK	3	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	2C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL431A, TL431B, TL432A, TL432B :

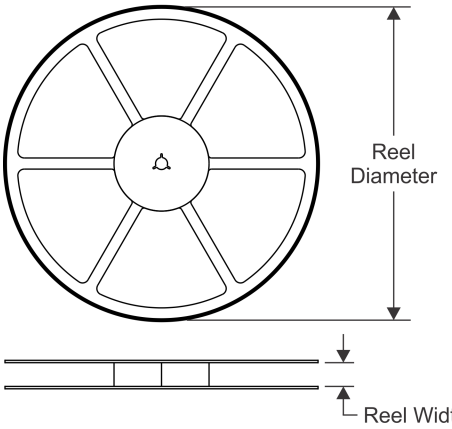
- Automotive: TL431A-Q1, TL431B-Q1, TL432A-Q1, TL432B-Q1

NOTE: Qualified Version Definitions:

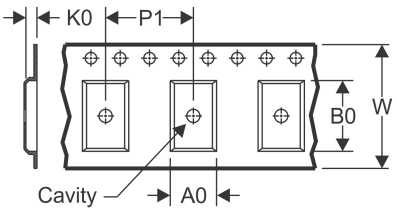
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

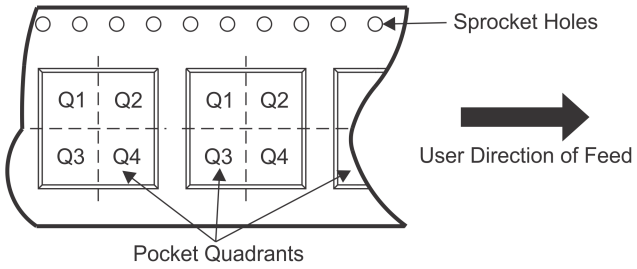


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL431ACDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TL431ACDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TL431ACDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TL431ACDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431ACDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431ACDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431ACDBZT	SOT-23	DBZ	3	250	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431ACDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431ACDCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TL431ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431ACDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TL431ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431ACPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL431ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL431ACPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL431AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TL431AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431AIDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

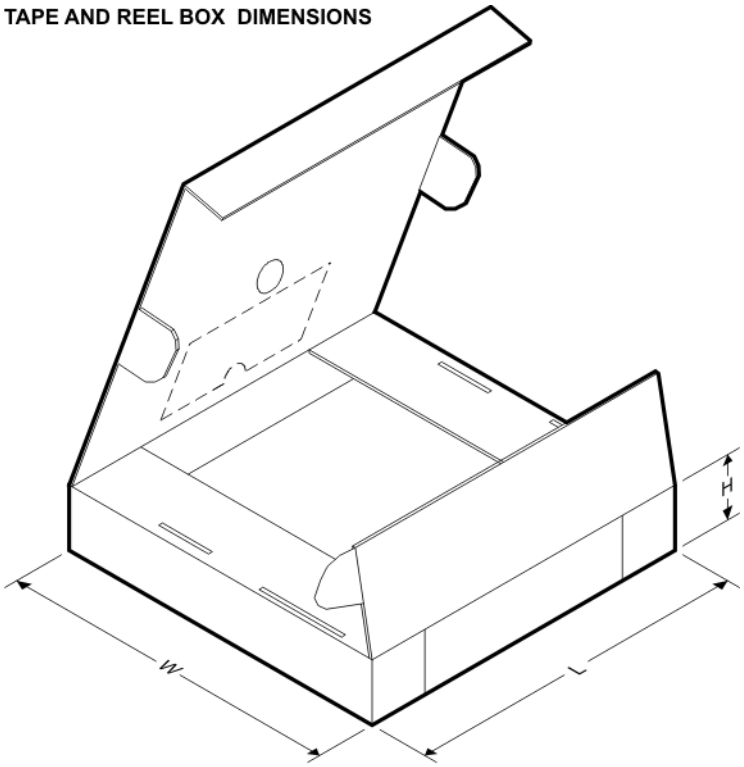
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL431AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431AIDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431AIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431AIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431AIDBZT	SOT-23	DBZ	3	250	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431AIDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431AIDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TL431AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL431AQDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431AQDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TL431AQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431AQDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431AQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431AQDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431AQDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431AQDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431AQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL431BCDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431BCDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431BCDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431BCDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431BCDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BCDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BCDBZT	SOT-23	DBZ	3	250	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431BCDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431BCDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431BCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL431BCPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL431BCPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL431BIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431BIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431BIDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431BIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431BIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BIDBZT	SOT-23	DBZ	3	250	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431BIDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431BIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL431BIDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TL431BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431BIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431BIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL431BQDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL431BQDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL431BQDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL431BQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BQDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BQDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431BQDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431BQDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431BQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TL431CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TL431CDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431CDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL431CDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431CDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431CDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TL431CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431CDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL431CPKE6	SOT-89	PK	3	1000	180.0	13.0	4.91	4.52	1.9	8.0	12.0	Q3
TL431CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL431CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL431IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TL431IDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431IDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL431IDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431IDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431IDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431IDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431IDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TL431IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL431IPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL431QDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL431QDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431QDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL431QDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL431QDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431QDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL431QDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431QDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL431QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL432ACDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL432ACDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432ACDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432ACDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432ACDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL432AIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL432AIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432AIDBZT	SOT-23	DBZ	3	250	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL432AIDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432AIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL432AQDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL432AQDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL432AQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432AQDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432AQDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432AQDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432AQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL432BCDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL432BCDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432BCDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432BCDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432BCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL432BIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432BIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL432BIDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432BIDBZT	SOT-23	DBZ	3	250	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL432BIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL432BQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TL432BQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432BQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL432CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL432CDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432CPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL432IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL432IDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432IDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432IPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TL432QDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TL432QPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL431ACDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TL431ACDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431ACDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431ACDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431ACDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431ACDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TL431ACDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TL431ACDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431ACDCKR	SC70	DCK	6	3000	183.0	183.0	20.0
TL431ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL431ACDR	SOIC	D	8	2500	364.0	364.0	27.0
TL431ACDRG4	SOIC	D	8	2500	340.5	338.1	20.6

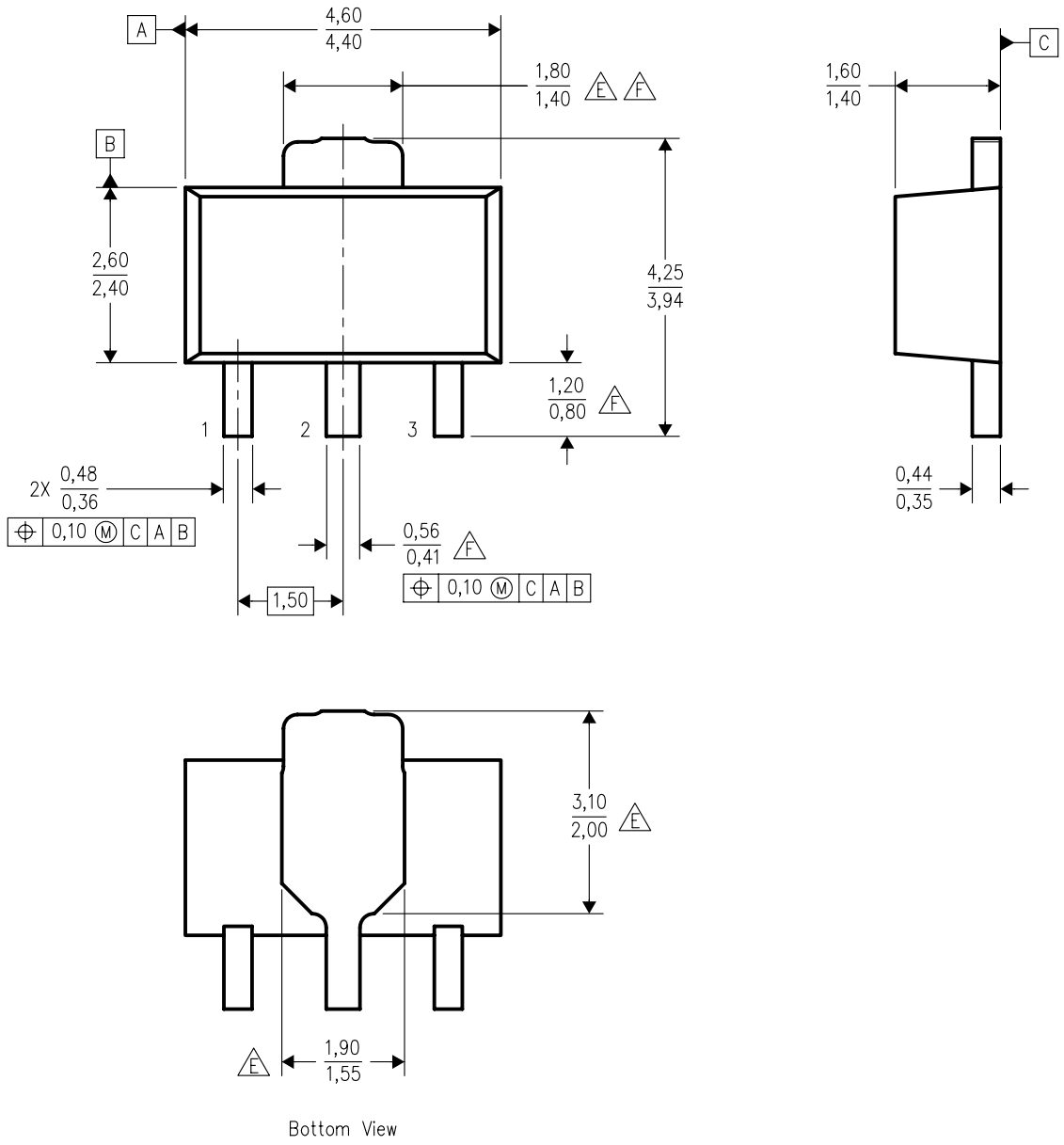
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL431ACPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL431ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL431ACPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL431AIDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TL431AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431AIDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431AIDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431AIDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TL431AIDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TL431AIDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431AIDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TL431AIDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TL431AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL431AIDR	SOIC	D	8	2500	364.0	364.0	27.0
TL431AIDRG4	SOIC	D	8	2500	340.5	338.1	20.6
TL431AIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL431AQDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431AQDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431AQDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431AQDBZRG4	SOT-23	DBZ	3	3000	202.0	201.0	28.0
TL431AQDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431AQDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431AQDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TL431AQDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TL431AQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL431BCDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431BCDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431BCDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431BCDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TL431BCDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431BCDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431BCDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TL431BCDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TL431BCDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TL431BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL431BCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL431BCPSR	SO	PS	8	2000	367.0	367.0	38.0
TL431BCPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL431BIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431BIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431BIDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431BIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL431BIDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431BIDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TL431BIDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431BIDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TL431BIDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TL431BIDR	SOIC	D	8	2500	364.0	364.0	27.0
TL431BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL431BIDRG4	SOIC	D	8	2500	340.5	338.1	20.6
TL431BIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL431BQDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TL431BQDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TL431BQDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL431BQDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431BQDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431BQDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431BQDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431BQDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TL431BQDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TL431BQDR	SOIC	D	8	2500	340.5	338.1	20.6
TL431CDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TL431CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431CDBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TL431CDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431CDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TL431CDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431CDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431CDR	SOIC	D	8	2500	364.0	364.0	27.0
TL431CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL431CDRG4	SOIC	D	8	2500	340.5	338.1	20.6
TL431CPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL431CPKE6	SOT-89	PK	3	1000	182.4	182.4	17.3
TL431CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL431CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL431IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431IDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TL431IDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431IDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL431IDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431IDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431IDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431IDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431IDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL431IDR	SOIC	D	8	2500	364.0	364.0	27.0
TL431IDRG4	SOIC	D	8	2500	340.5	338.1	20.6
TL431IPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL431QDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431QDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL431QDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL431QDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TL431QDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL431QDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL431QDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TL431QDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TL431QDR	SOIC	D	8	2500	340.5	338.1	20.6
TL432ACDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL432ACDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432ACDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432ACDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432ACDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL432AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TL432AIDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432AIDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TL432AIDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432AIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL432AQDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TL432AQDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TL432AQDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432AQDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432AQDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432AQDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432AQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL432BCDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TL432BCDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432BCDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432BCDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432BCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL432BIDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432BIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TL432BIDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432BIDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TL432BIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL432BQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TL432BQDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432BQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL432CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL432CDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432CPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL432IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL432IDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432IDBZT	SOT-23	DBZ	3	250	183.0	183.0	20.0
TL432IPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TL432QDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TL432QPK	SOT-89	PK	3	1000	340.0	340.0	38.0

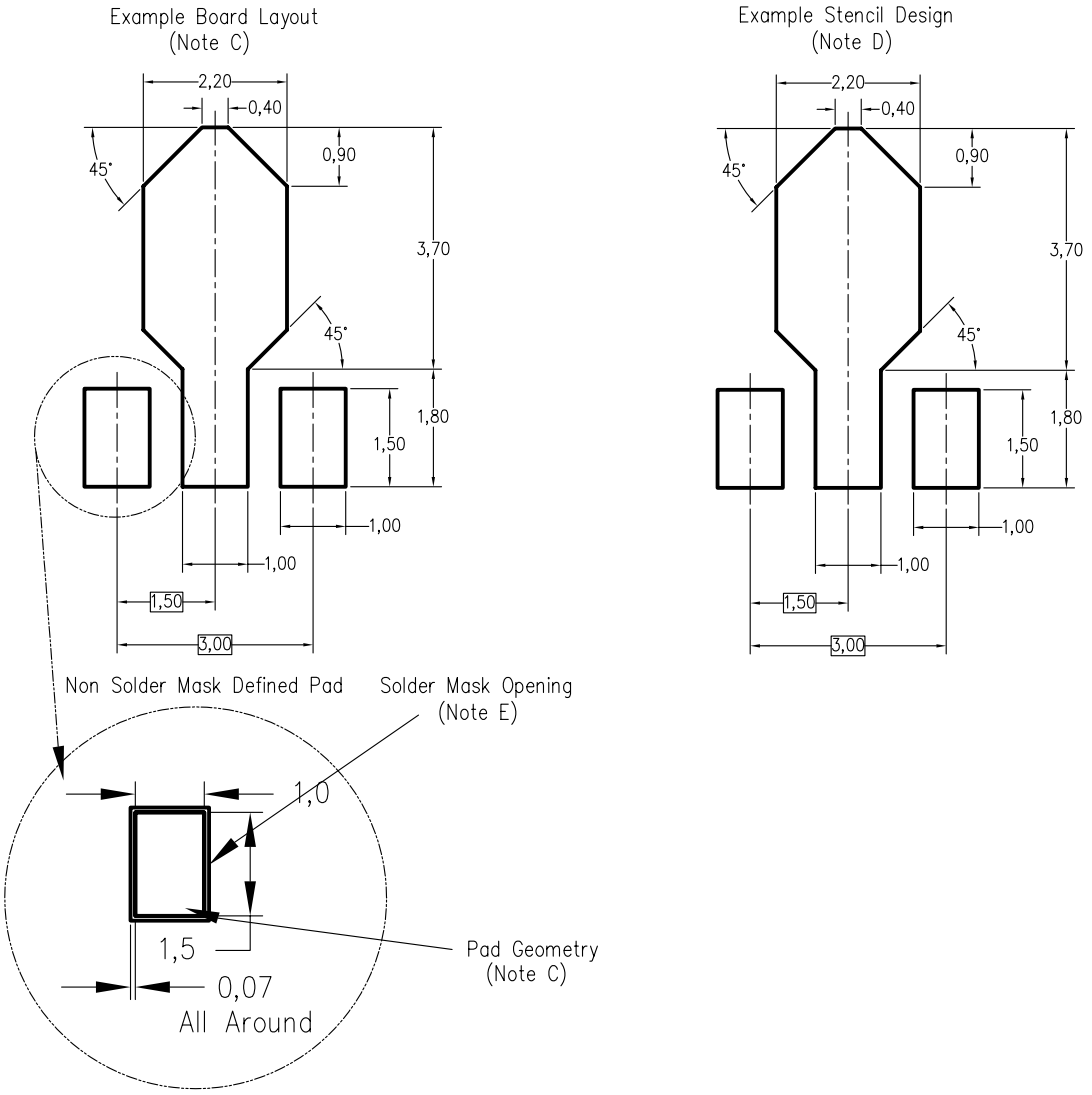
PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



4040234/D 02/2006

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

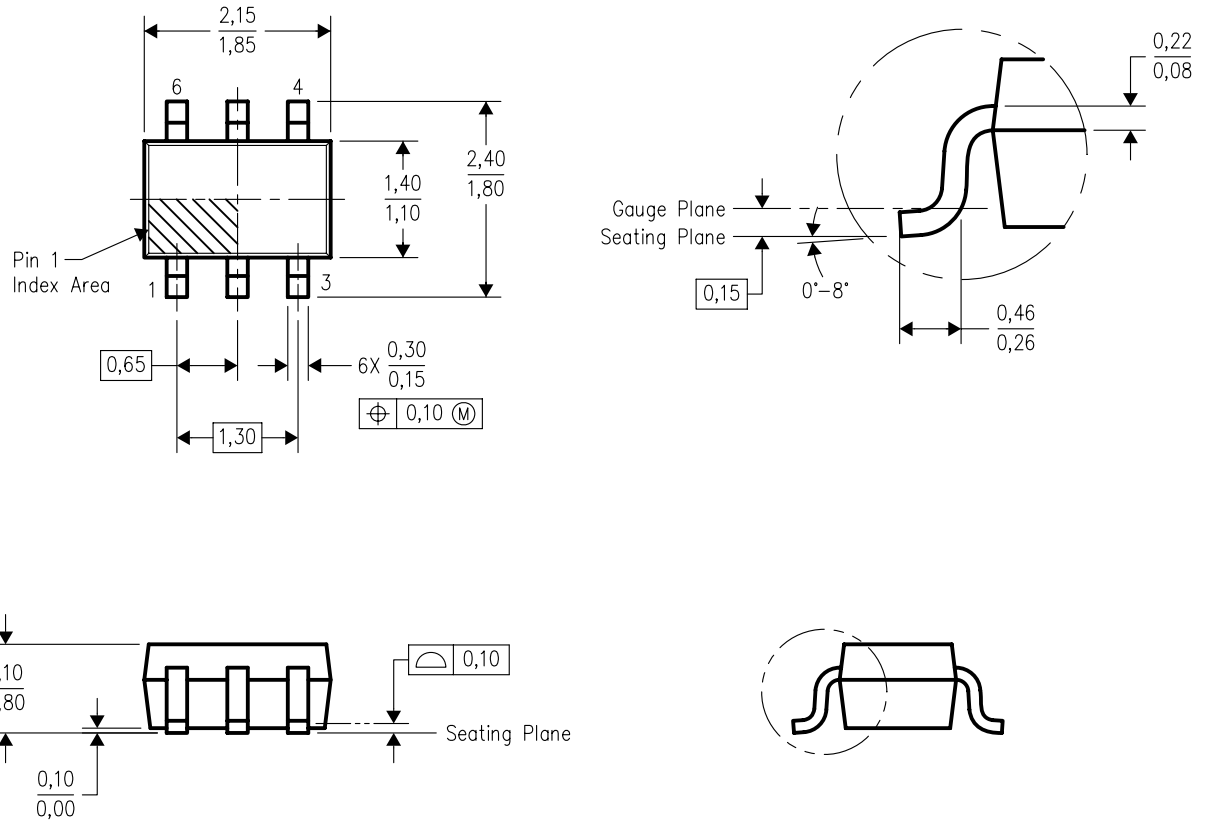
PK (R–PDSO–G3)



4208221/A 09/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

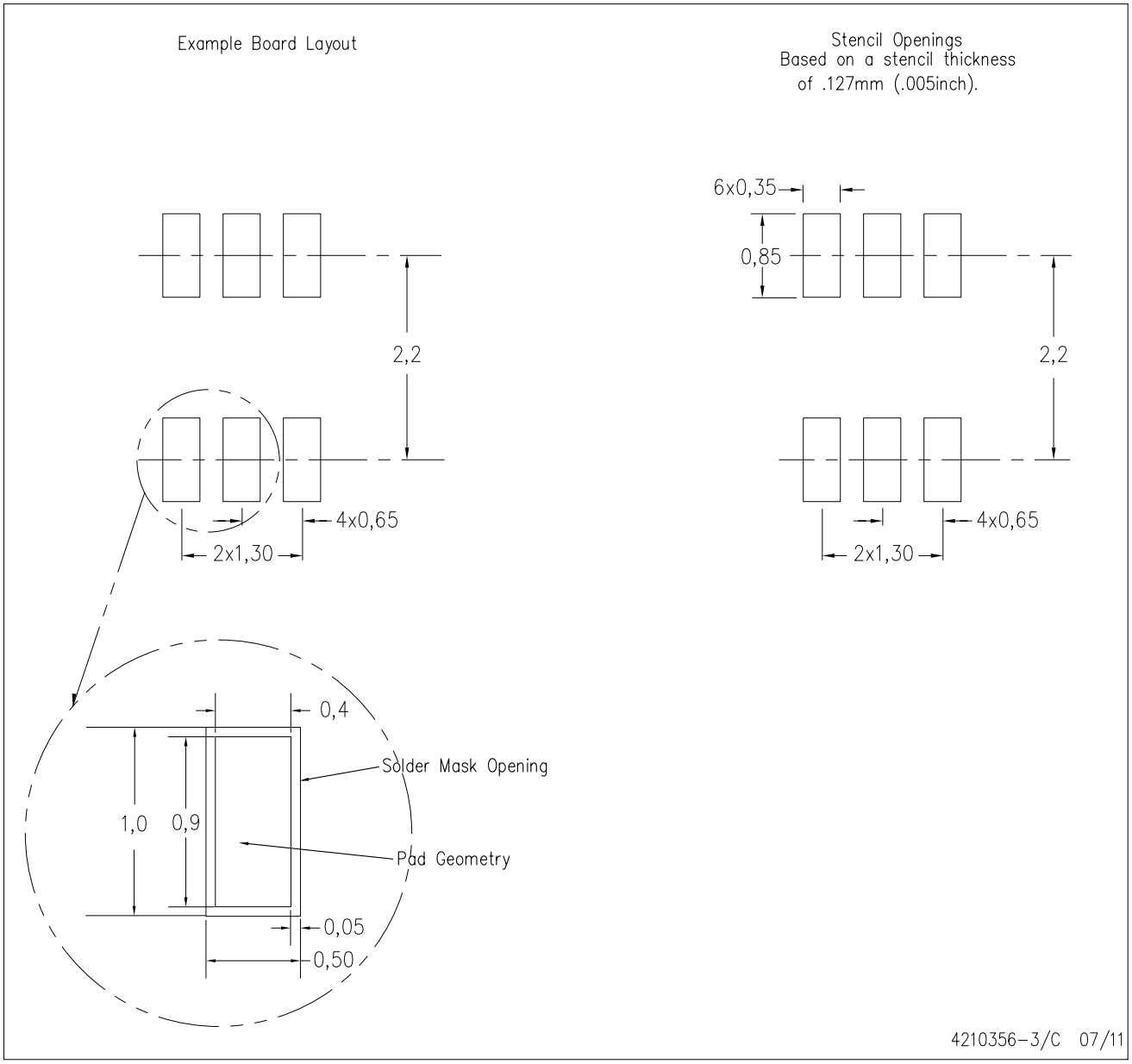
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

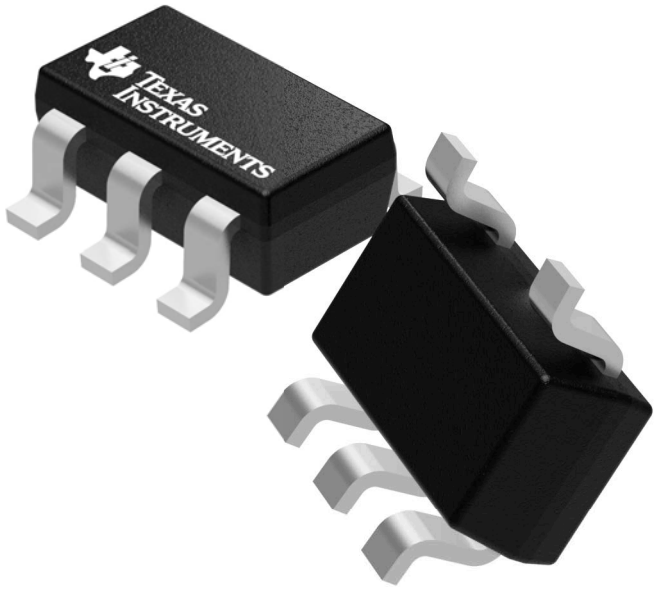
DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



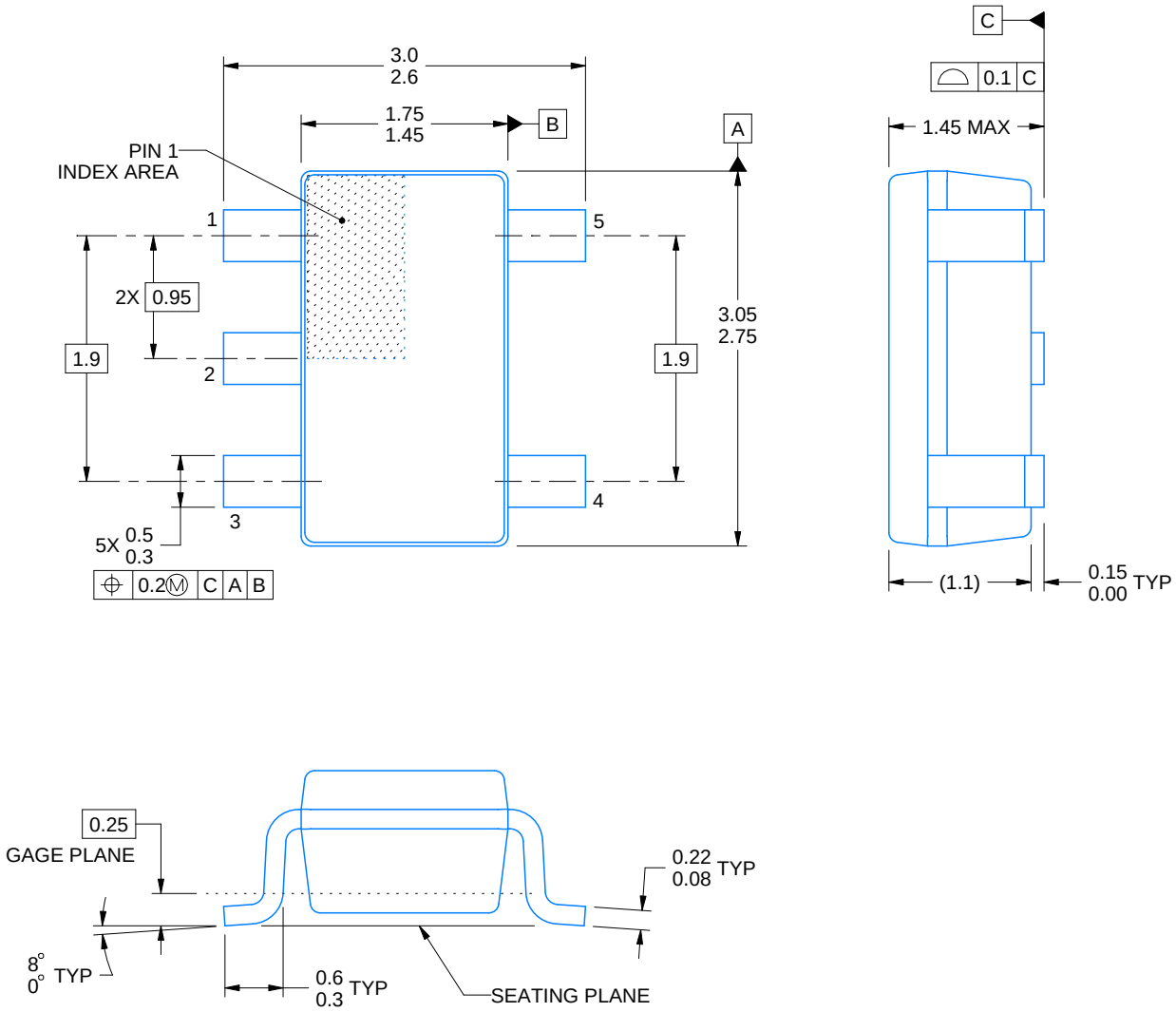
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

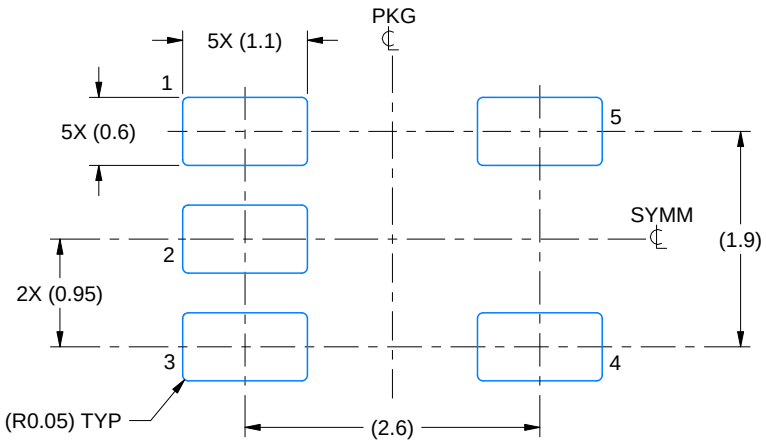
SMALL OUTLINE TRANSISTOR



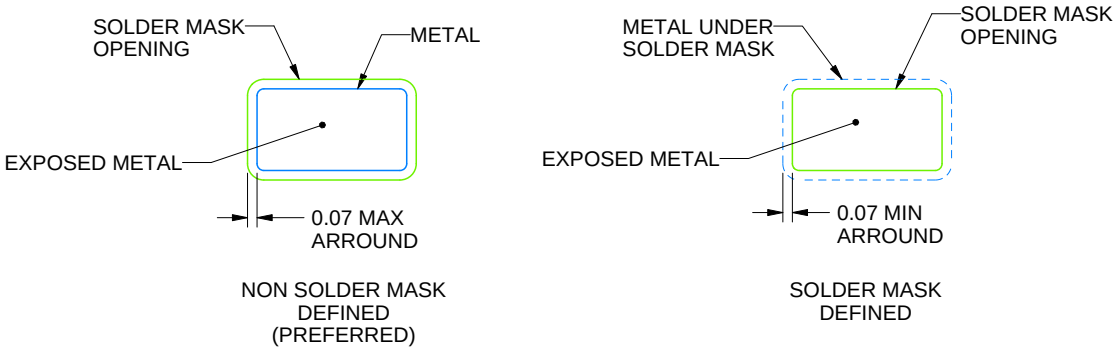
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

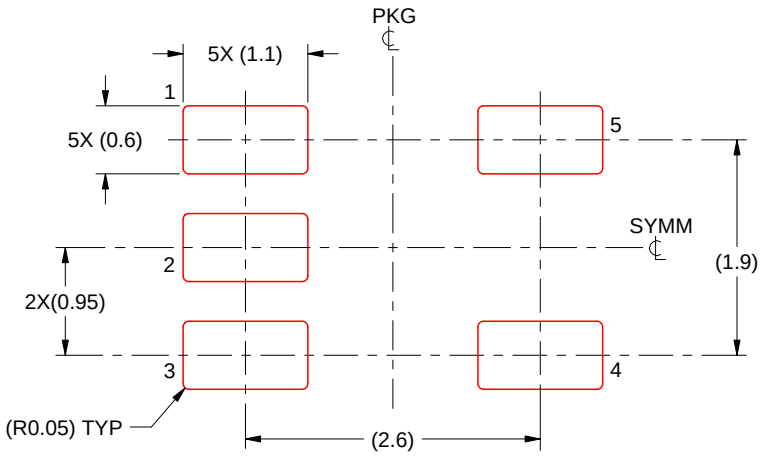


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

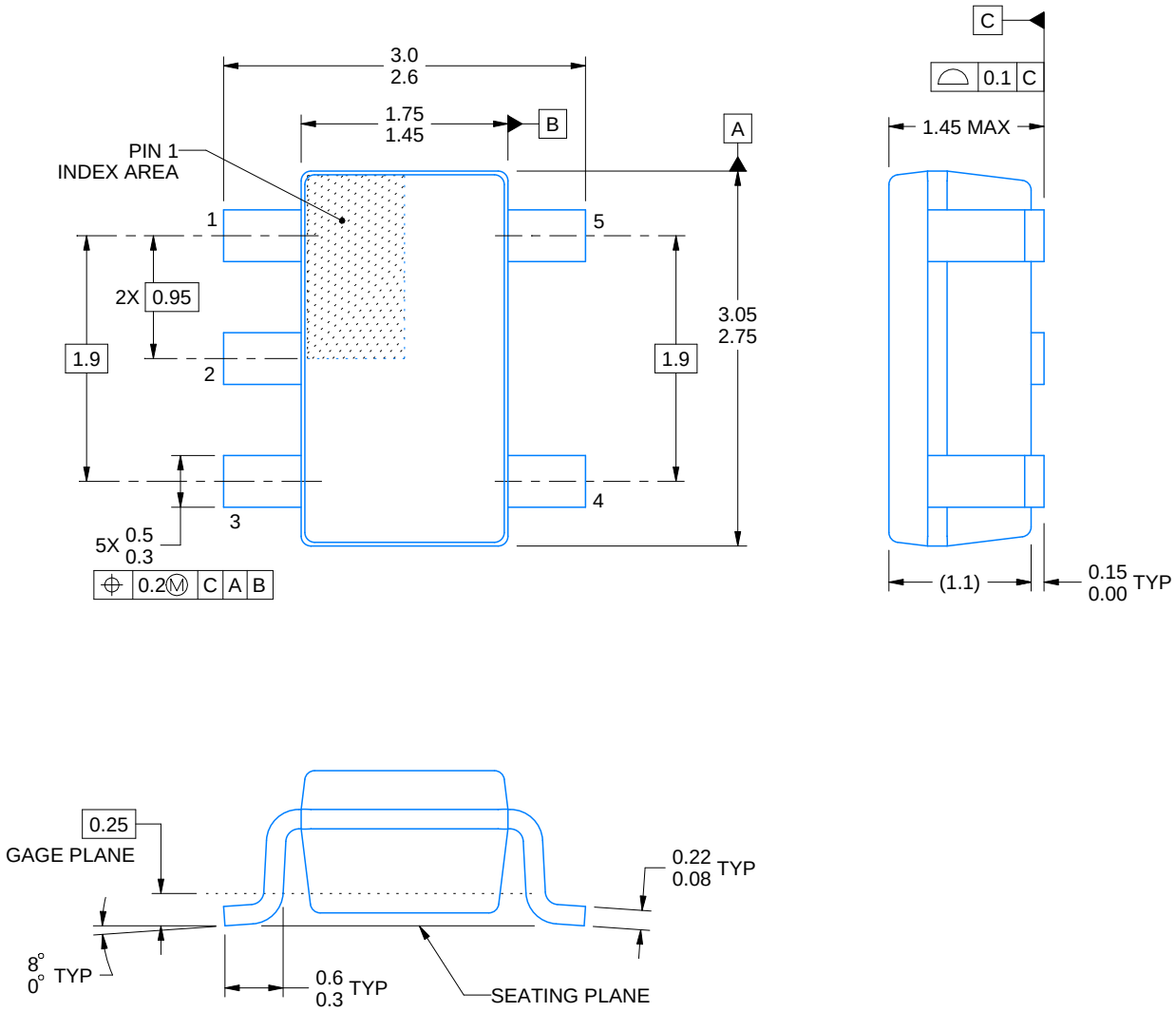
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

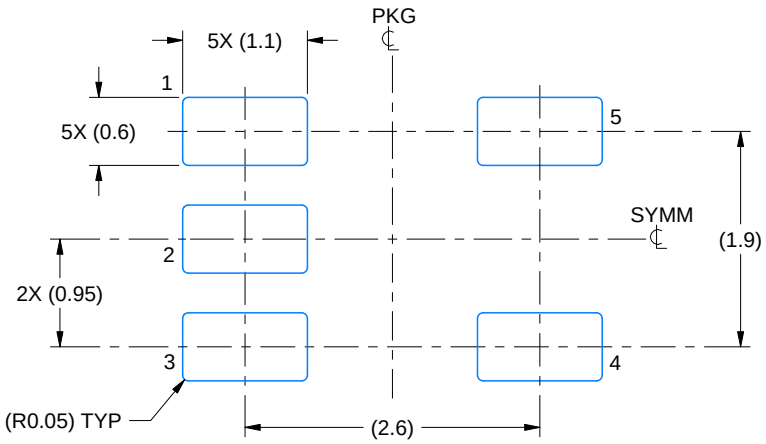
SMALL OUTLINE TRANSISTOR



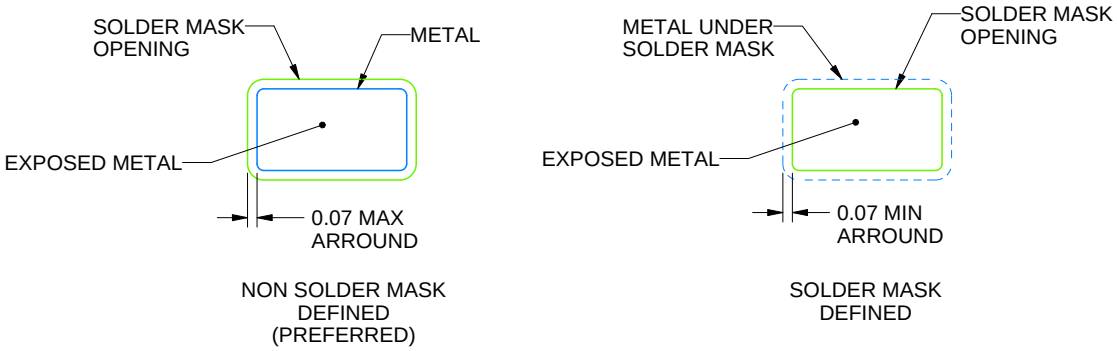
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

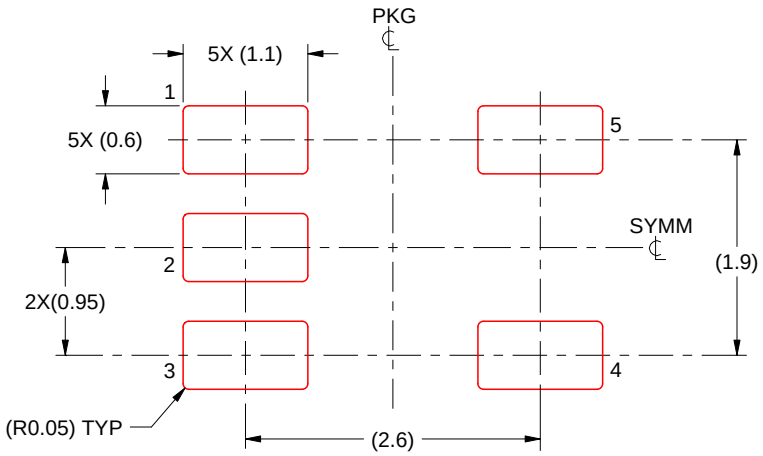


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



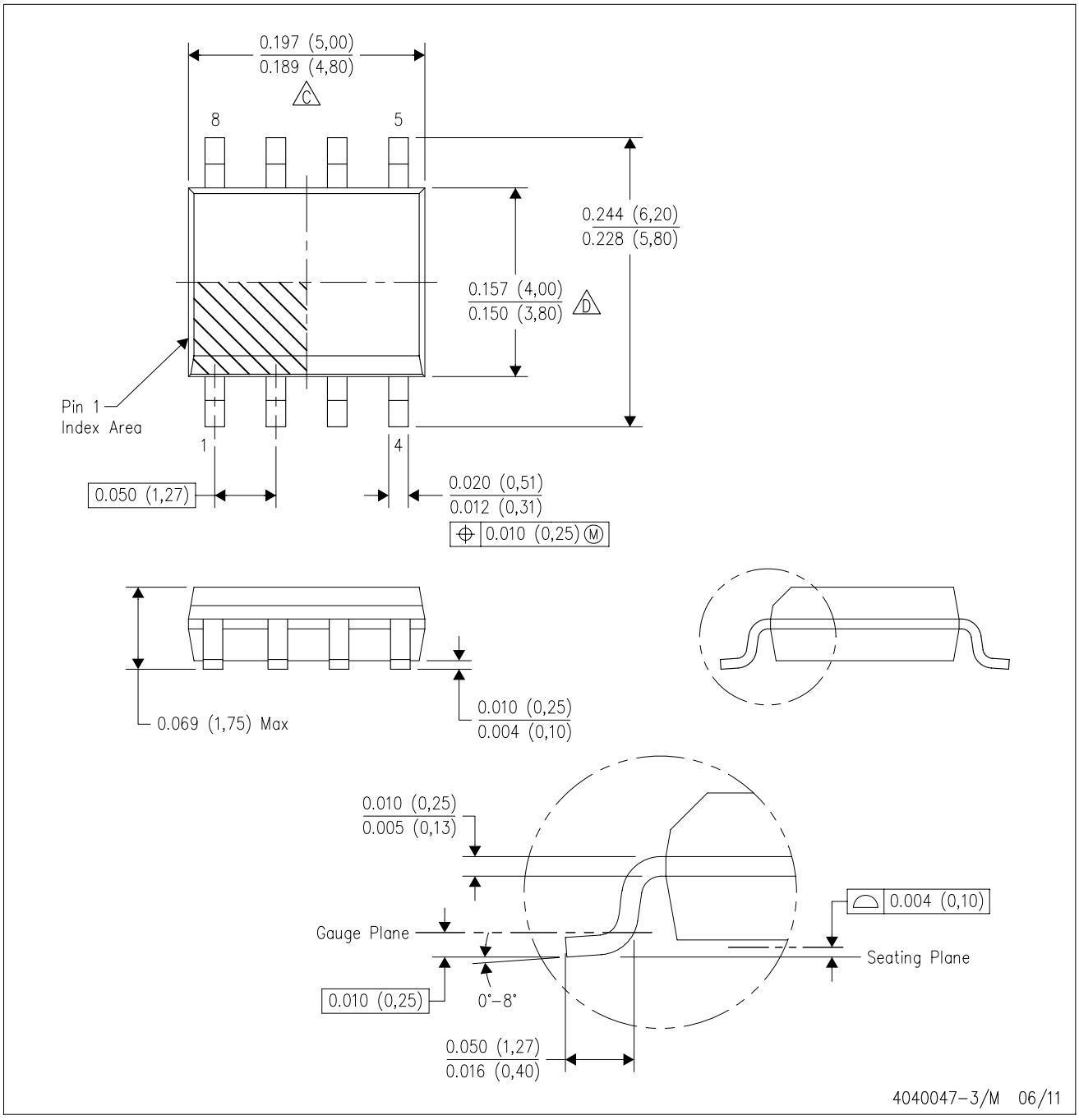
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

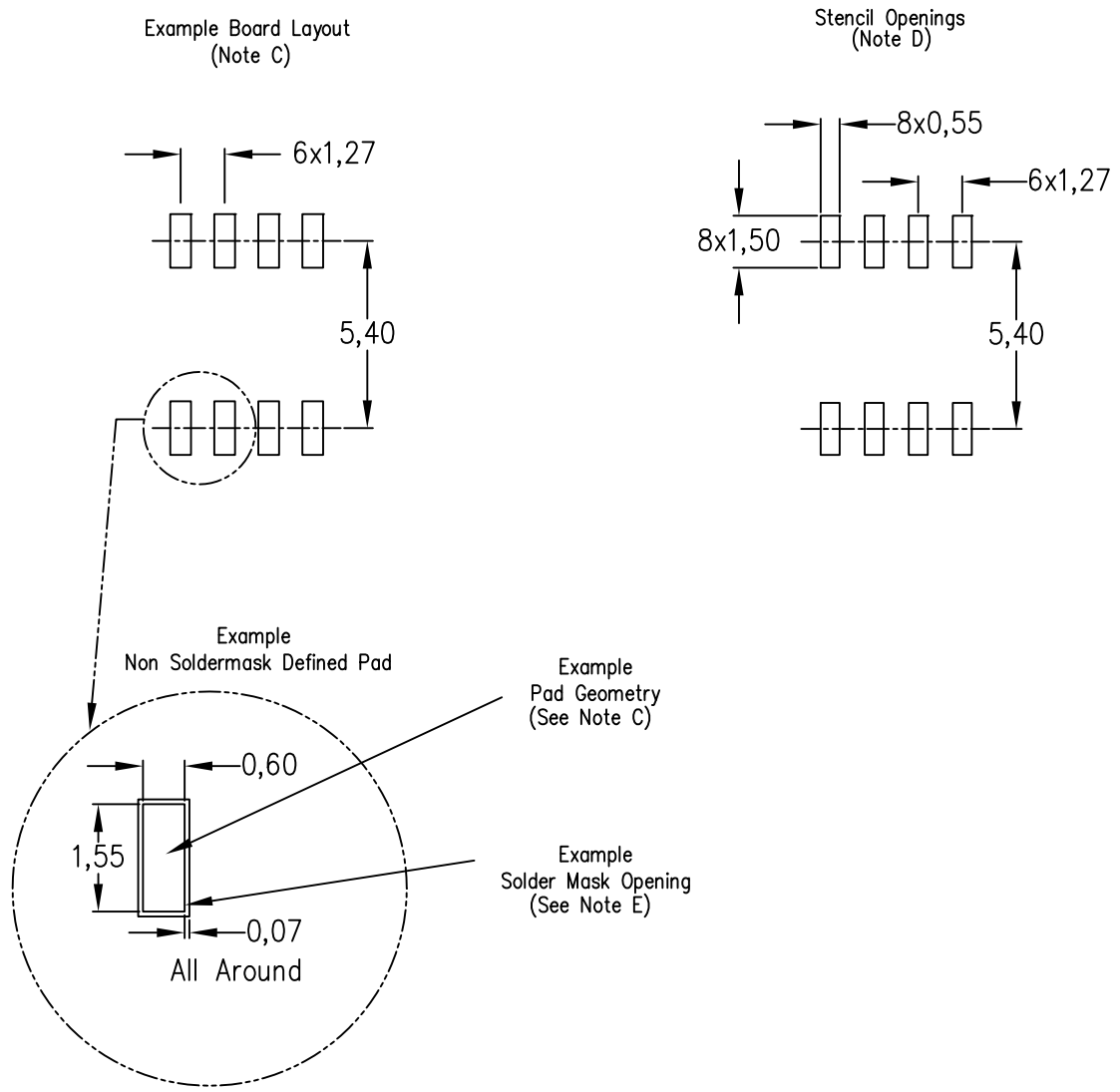
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

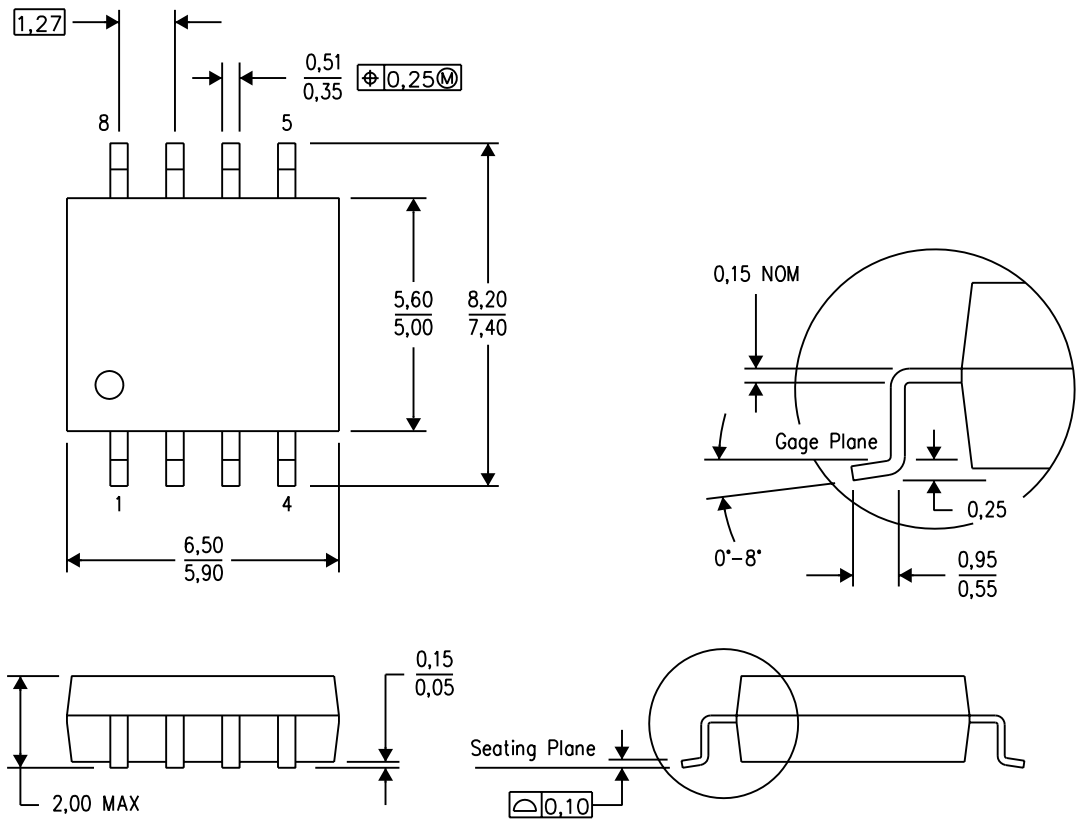
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

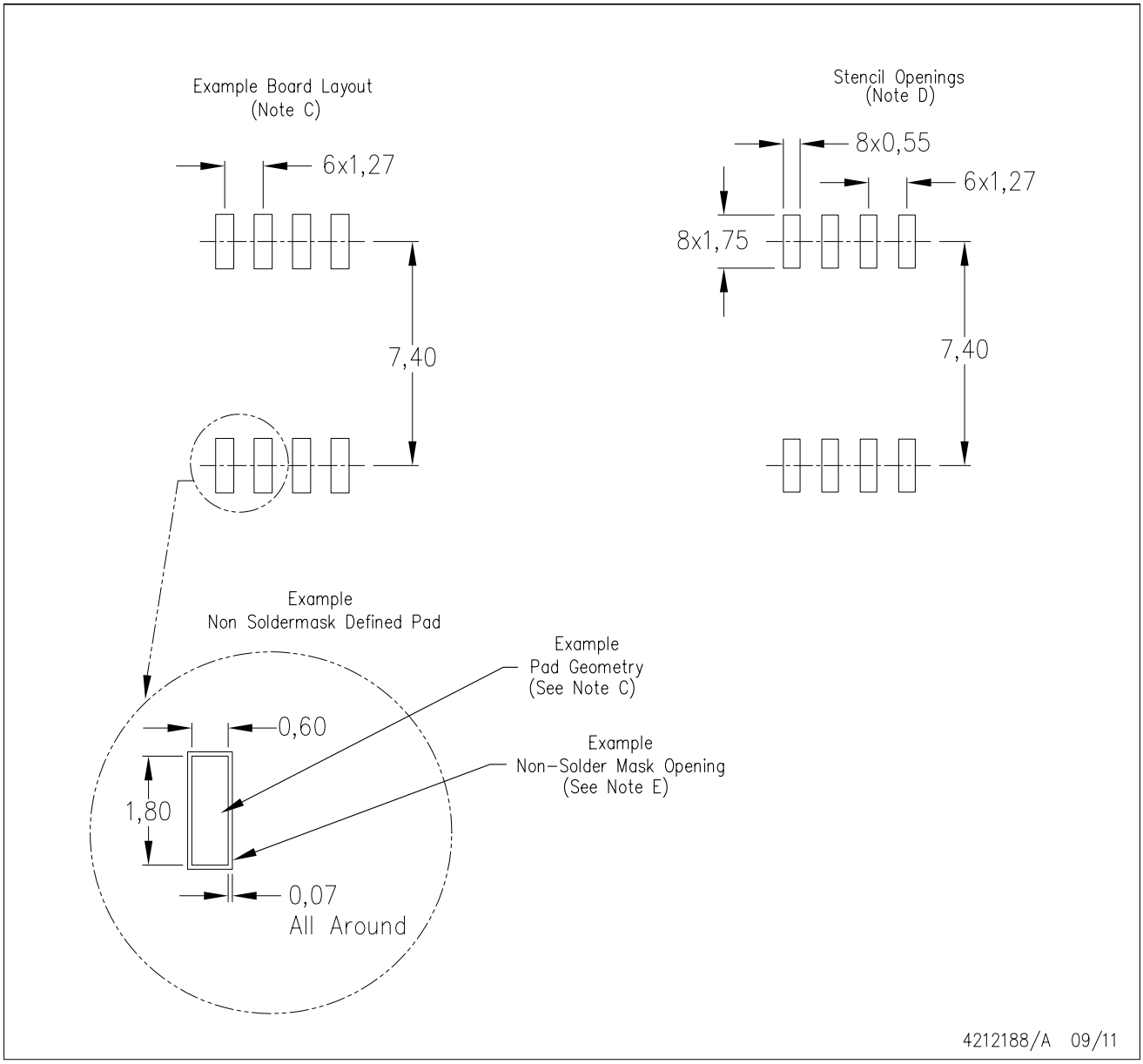
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

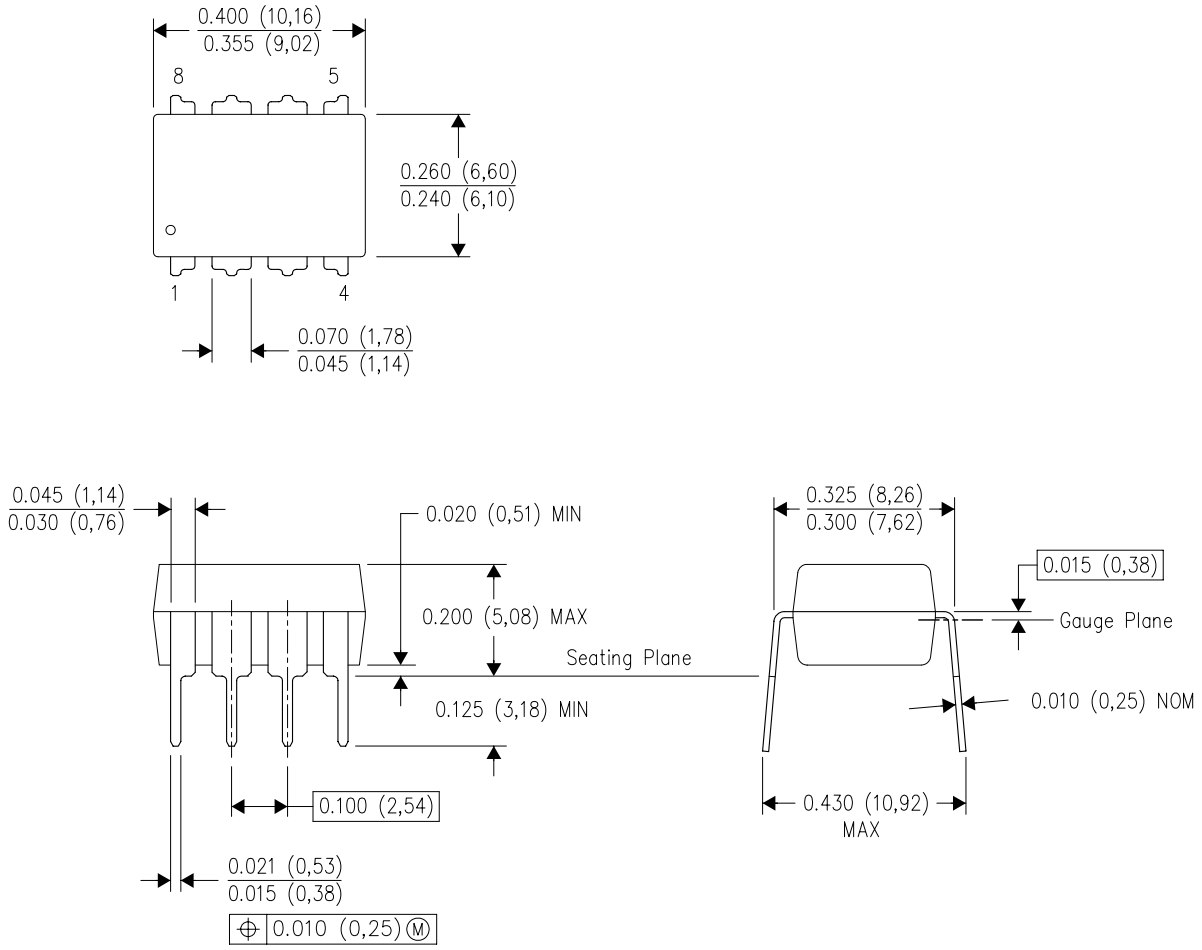
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



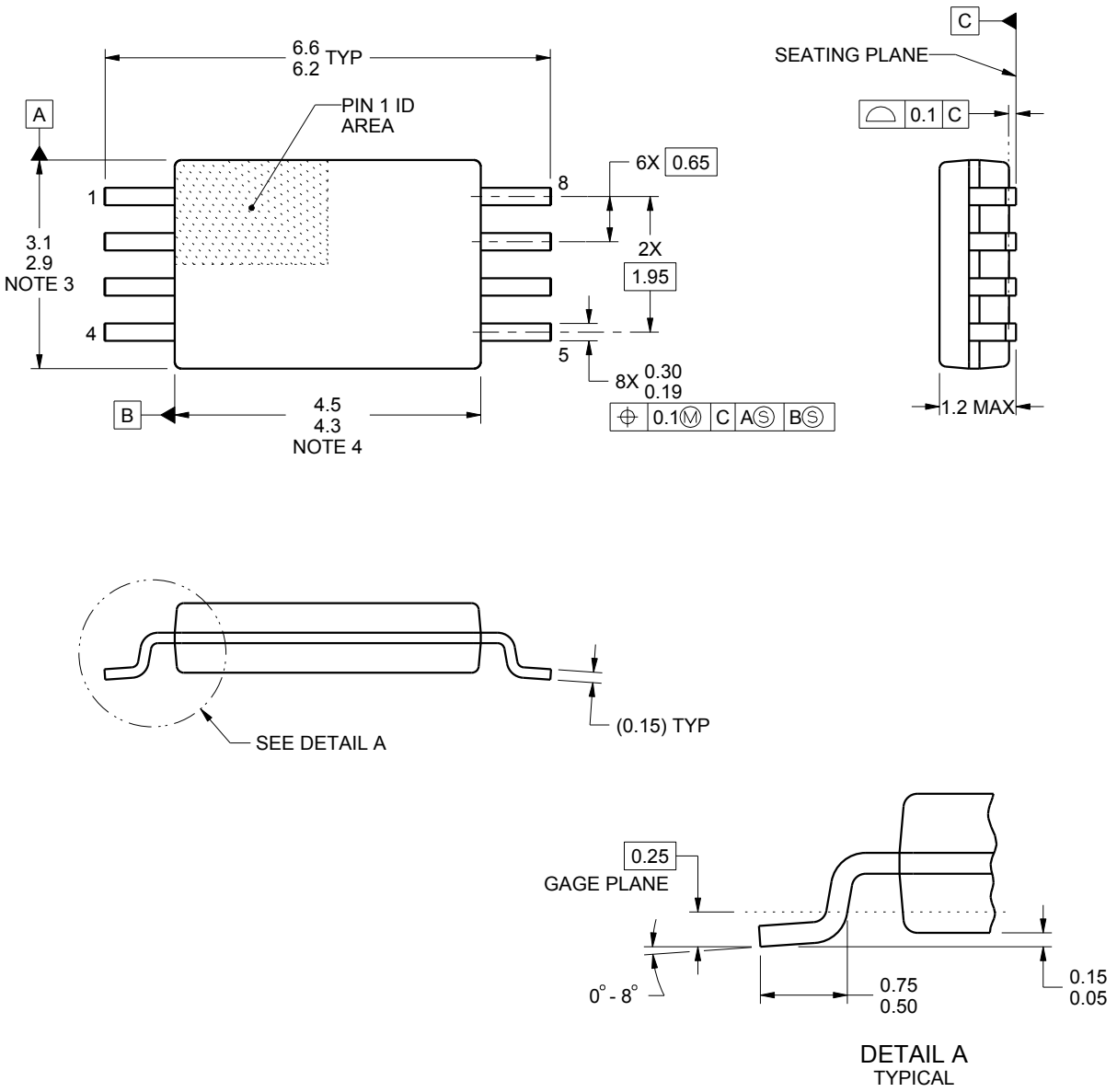
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

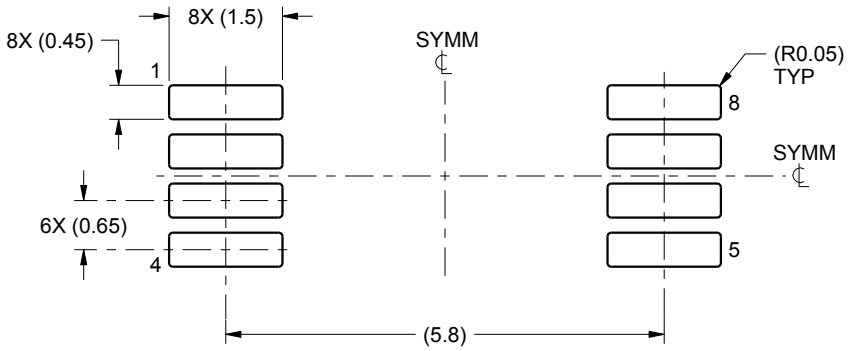
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

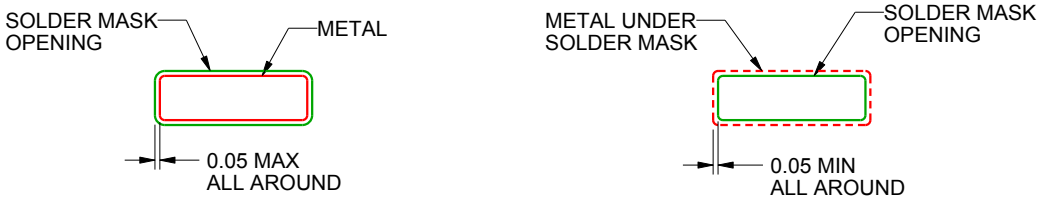


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

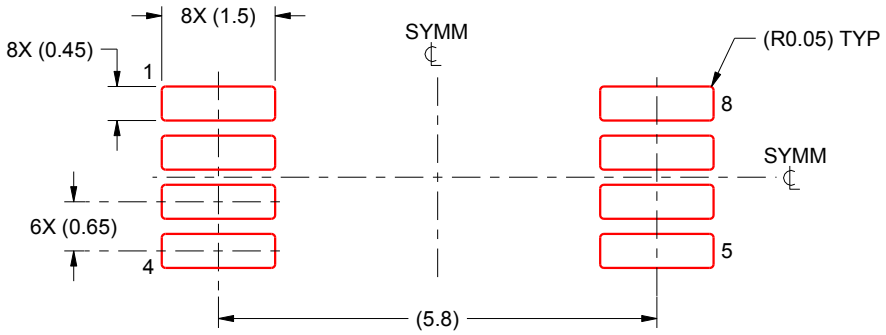


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

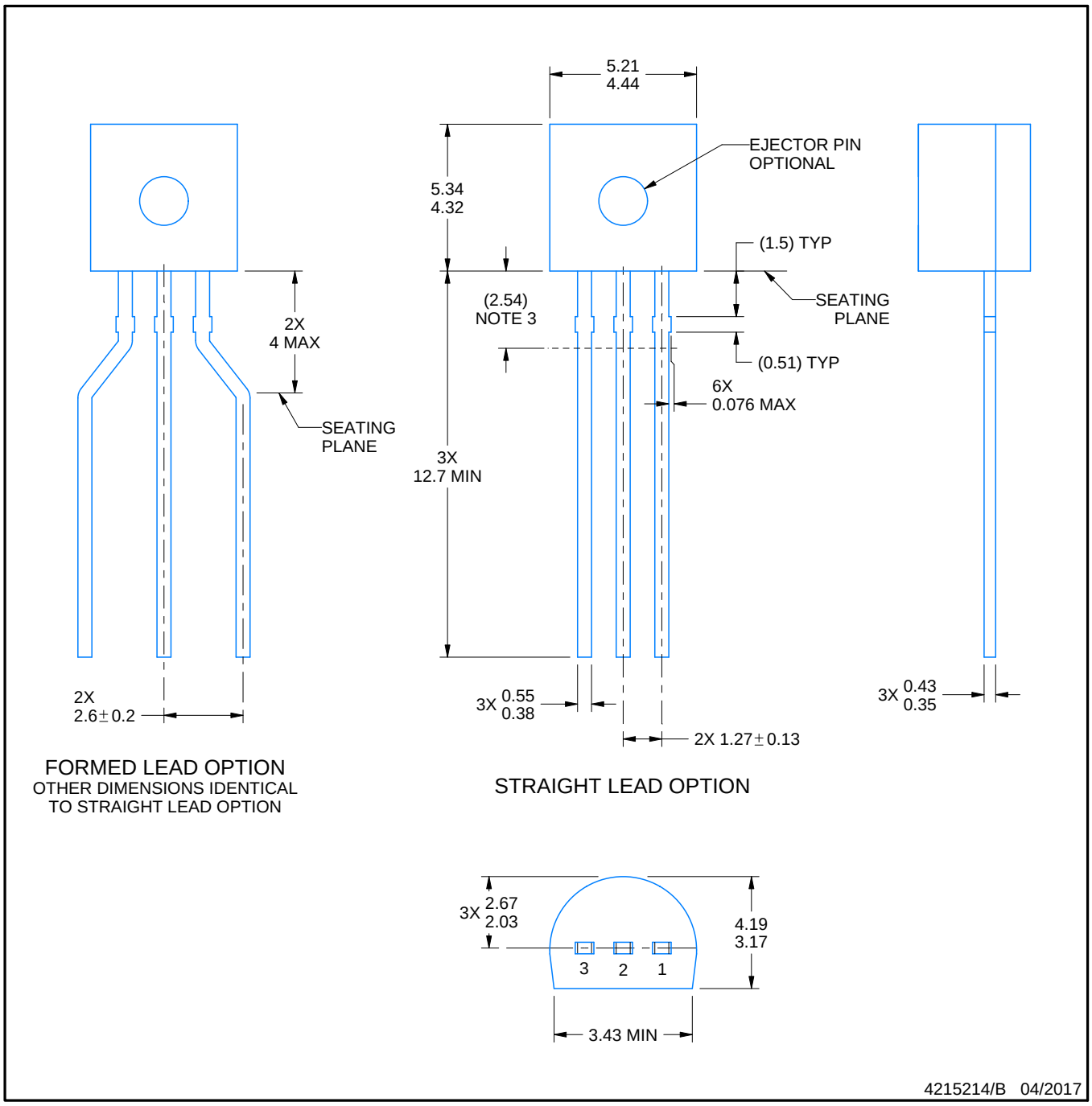
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

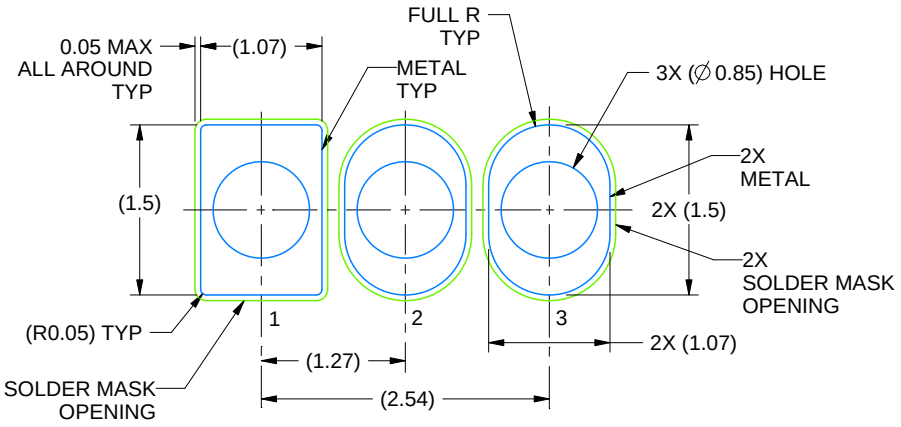
TO-92 - 5.34 mm max height

TO-92

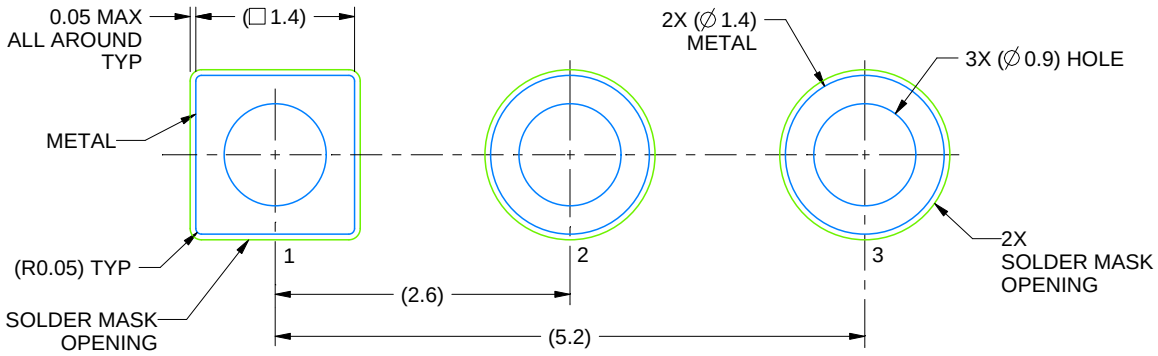


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



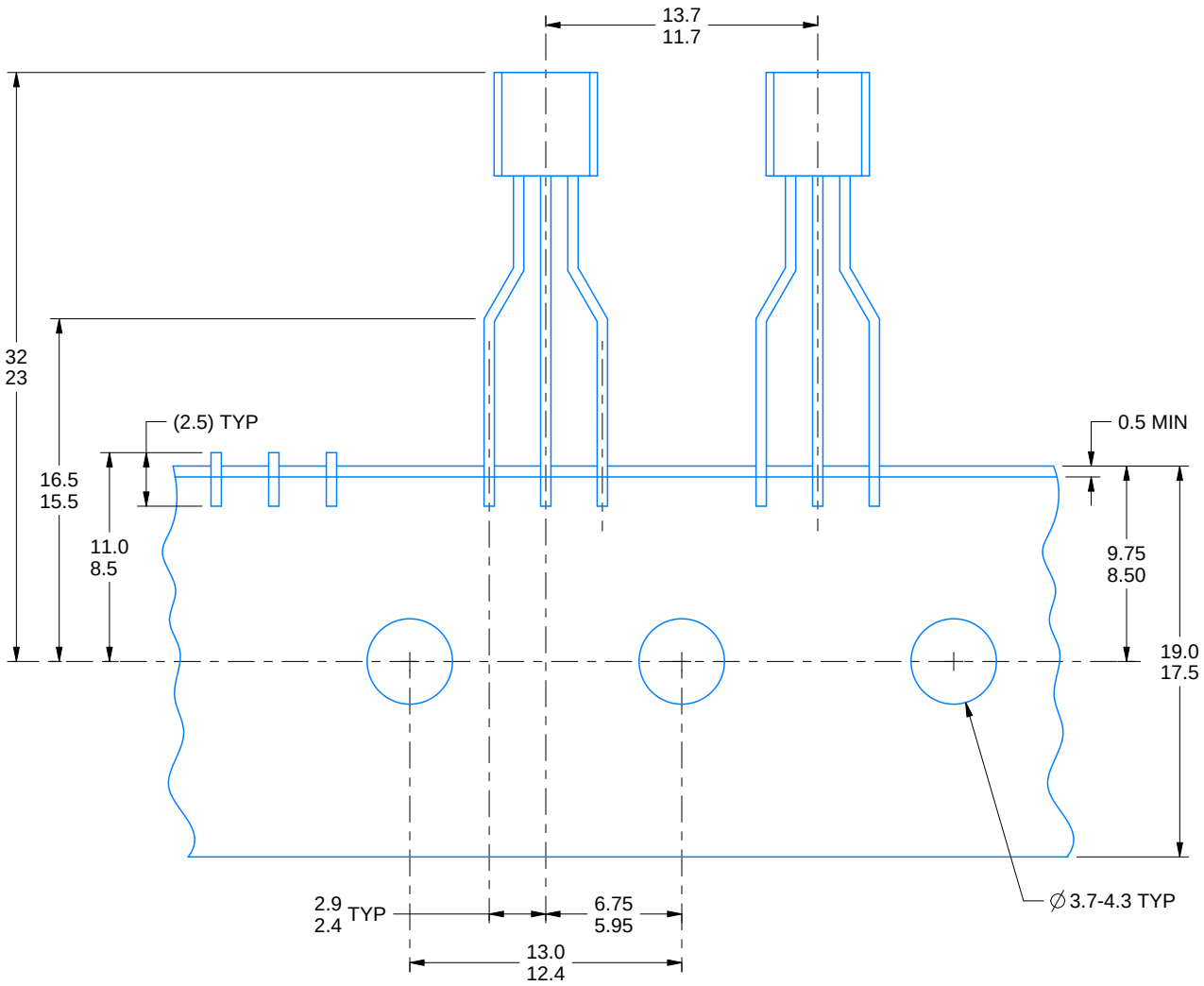
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



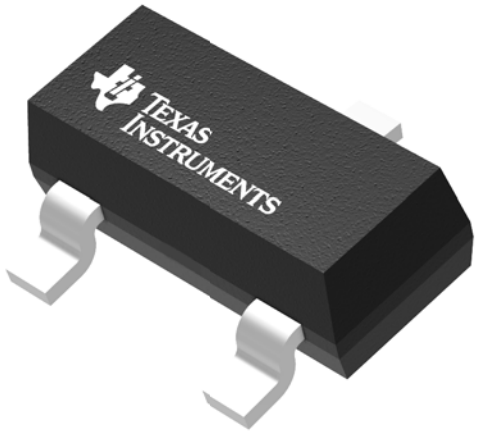
FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



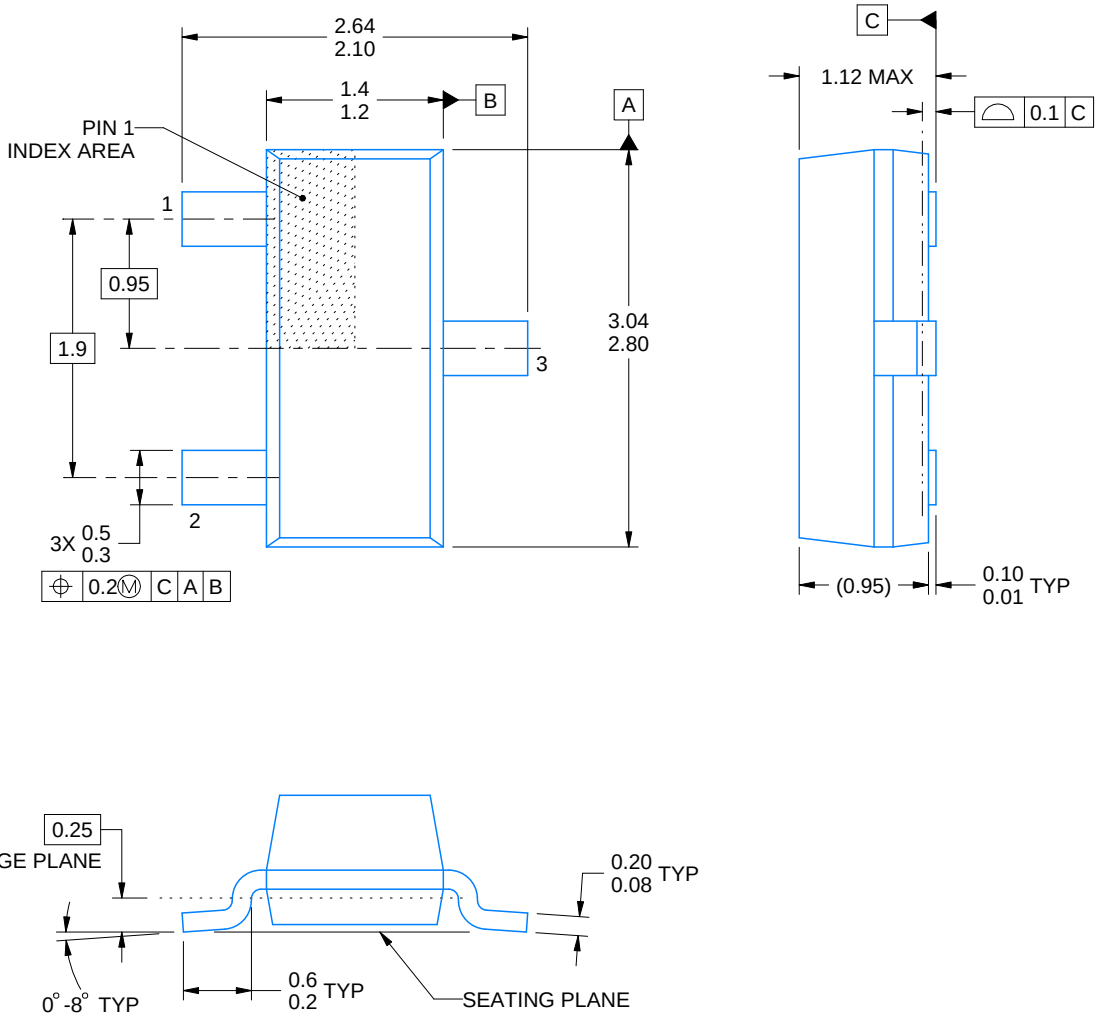
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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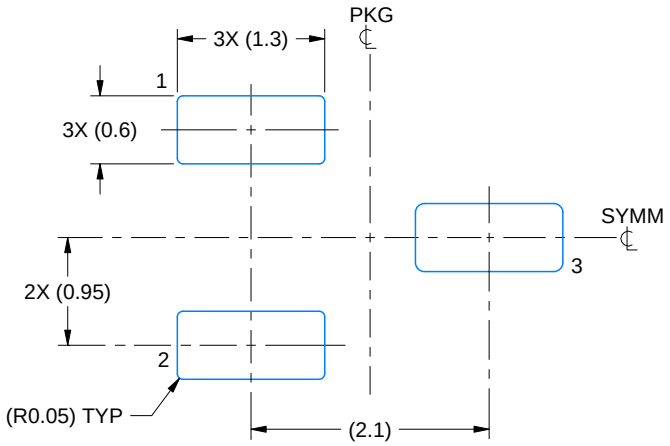
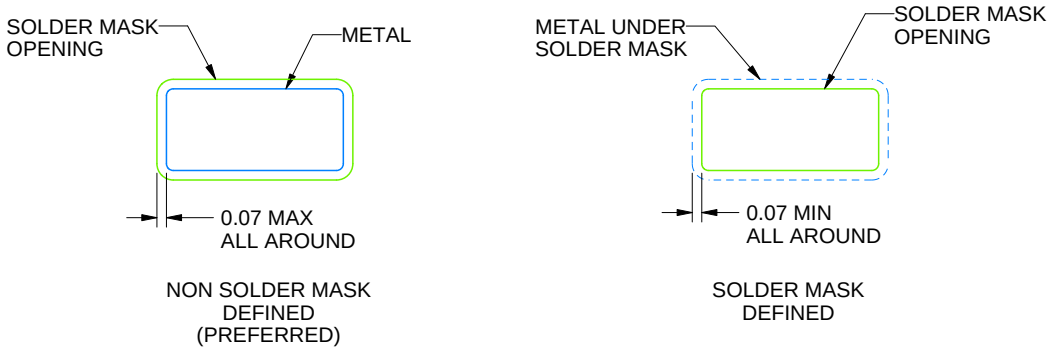
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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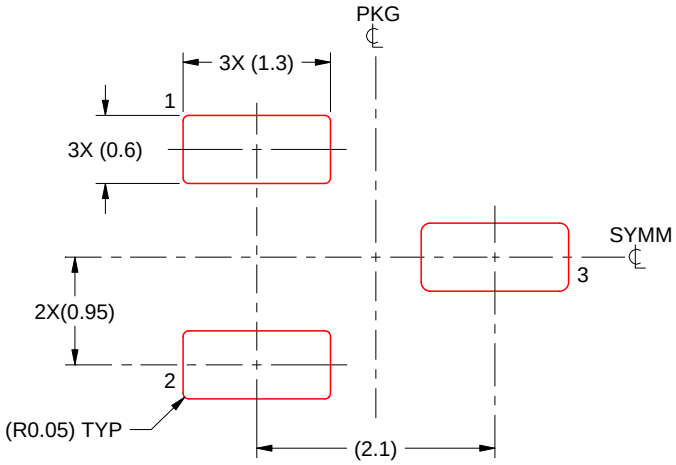
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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