



## Bus Powered USB2.0 Flash Media Controller

### Datasheet

### Product Features

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- Complete System Solution for interfacing SmartMedia<sup>™</sup> (SM) or xD Picture Card<sup>™</sup> (xD), Memory Stick<sup>™</sup> (MS), High Speed Memory Stick (HSMS), Memory Stick PRO (MSPRO), MS Duo<sup>™</sup>, Secure Digital (SD), Mini-Secure Digital (Mini-SD), Transflash (SD), MultiMediaCard<sup>™</sup> (MMC), Reduced Size Multimedia Card (RS-MMC), NAND Flash, Compact Flash<sup>™</sup> (CF), CF Ultra<sup>™</sup> I & II and CF form-factor ATA hard drives to USB2.0 bus.
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
- Support for simultaneous operation of all above devices. (only one at a time of each of the following groups supported: CF or ATA drive, SM or XD or NAND, SD or MMC)
- On-Chip 4-Bit High Speed Memory Stick and MS PRO Hardware Circuitry
- On-Chip firmware reads and writes High Speed Memory Stick and MS PRO
- 1-bit ECC correction performed in hardware for maximum efficiency
- USB Bus Power Certified
- 3.3 Volt I/O with 5V input tolerance
- Complete USB Specification 2.0 Compatibility for Bus Powered Operation
  - Includes USB2.0 Transceiver
  - A Bi-directional Control and a Bi-directional Bulk Endpoint are provided.
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 12K Bytes of internal SRAM for general purpose scratchpad
  - 768 Bytes of internal SRAM for general purpose scratchpad or program execution while re-flashing external ROM
- Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- Internal or External Program Memory Interface
  - 64K Byte Internal Code Space or Optional 64K Byte External Code Space using Flash, SRAM or EPROM memory.
- On Board 12Mhz Crystal Driver Circuit
- On-Chip 1.8V Regulator for Low Power Core Operation
- Internal PLL for 480Mhz USB2.0 Sampling, Configurable MCU clock
- Supports firmware upgrade via USB bus if “boot block” Flash program memory is used
- 15 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
  - Attribute bit controlled features:
    - Activity LED polarity/operation/blink rate
    - Full or Partial Card compliance checking
    - Bus or Self Powered
    - LUN configuration and assignment
    - Write Protect Polarity
    - Detach on no Card Inserted for Notebook apps
    - Cover Switch operation for xD compliance
    - Inquiry Command operation
    - SD Write Protect operation
    - Older CF card support
    - Force USB 1.1 reporting
- Compatible with Microsoft WinXP, WinME, Win2K SP3, Apple OS10, Softconnex, and Linux Multi-LUN Mass Storage Class Drivers
- Win2K, Win98/98SE and Apple OS8.6 and OS9 Multi-LUN Mass Storage Class Drivers available from SMSC
- 128 Pin TQFP Package (1.0mm height, 14mm x14mm footprint); PB free package also available

**ORDERING INFORMATION****Order Number(s):**

USB2224-NE-02 for 128 pin TQFP package

USB2224-NU-02 for 128 pin PB Free TQFP package



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# Chapter 1 General Description

The USB2224 is a USB2.0 Bulk Only Mass Storage Class Peripheral Controller intended for supporting CompactFlash (CF and CF Ultra I/II) in True IDE Mode only, SmartMedia (SM) and XD cards, Memory Stick (MS), Memory Stick DUO (MSDUO) and Memory Stick Pro (MSPRO), Secure Digital (SD), and MultiMediaCard (MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market.

The device consists of a USB2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices.

Provisions for external Flash Memory up to 64K bytes for program storage is provided.

12K bytes of scratchpad SRAM and 768 Bytes of program SRAM are also provided.

Fifteen GPIO pins are provided for indicators, external serial EEPROM for OEM id and system configuration information, and other special functions.

The internal ROM program is capable of implementing any combination of single or multi-LUN CF/SD/MMC/SM/MS reader functions with individual card power control and activity indication. SMSC also provides licenses\*\* for Win98 and Win2K drivers and setup utilities. Note: Please check with SMSC for precise features and capabilities for the current ROM code release.

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## Chapter 2 Acronyms and Definitions

### 2.1 Acronyms

|             |                               |
|-------------|-------------------------------|
| <b>SM:</b>  | SmartMedia                    |
| <b>SMC:</b> | SmartMedia Controller         |
| <b>FM:</b>  | Flash Media                   |
| <b>FMC:</b> | Flash Media Controller        |
| <b>CF:</b>  | Compact Flash                 |
| <b>CFC:</b> | CompactFlash Controller       |
| <b>SD:</b>  | Secure Digital                |
| <b>SDC:</b> | Secure Digital Controller     |
| <b>MMC:</b> | MultiMediaCard                |
| <b>MS:</b>  | Memory Stick                  |
| <b>MSC:</b> | Memory Stick Controller       |
| <b>TPC:</b> | Transport Protocol Code.      |
| <b>ECC:</b> | Error Checking and Correcting |
| <b>CRC:</b> | Cyclic Redundancy Checking    |
| <b>XD:</b>  | XD Picture Card               |

### 2.2 Definitions

**Flash Media DMA UNIT (FMDU):** The control logic in the flash media controller block as shown in the Block Diagram that support the data transfer from CFC, SMC, MSC and SDC to EP2 buffer directly.

**SD/MMC:** the built-in SD controller (SDC) supports both SD and MMC devices.

**Flash Media Controller Data Multiplexer (FMC DATA MUX):** The multiplexer to enable the different data path from the different flash media controllers (CFC, SMC, MSC and SDC).

## Chapter 3 Pin Table

### 3.1 128-Pin Package

Table 3.1 - Pinout

| <b>CompactFlash INTERFACE (28 Pins)</b>          |               |             |            |
|--|---------------|-------------|------------|
| CF_D0  | CF_D1         | CF_D2       | CF_D3      |
| CF_D4  | CF_D5         | CF_D6       | CF_D7      |
| CF_D8  | CF_D9         | CF_D10      | CF_D11     |
| CF_D12   | CF_D13        | CF_D14      | CF_D15     |
| CF_nIOR  | CF_nIOW       | CF_IRQ      | CF_nRESET  |
| CF_IORDY   | CF_nCS0       | CF_nCS1     | CF_SA0     |
| CF_SA1   | CF_SA2        | CF_nCD1     | CF_nCD2    |
| <b>SmartMedia / XD INTERFACE (17 Pins)</b>       |               |             |            |
| SM_D0  | SM_D1         | SM_D2       | SM_D3      |
| SM_D4  | SM_D5         | SM_D6       | SM_D7      |
| SM_ALE   | SM_CLE        | SM_nRE      | SM_nWE     |
| SM_nWP   | SM_nB/R       | SM_nCE      | SM_nCD     |
| SM_nWPS  |               |             |            |
| <b>Memory Stick INTERFACE (7 Pins)</b>           |               |             |            |
| MS_BS  | MS_SDIO/MS_D0 | MS_SCLK     | MS_INS     |
| MS_D1  | MS_D2         | MS_D3       |            |
| <b>SD INTERFACE (7 Pins)</b>                     |               |             |            |
| SD_CMD   | SD_CLK        | SD_DAT0     | SD_DAT1    |
| SD_DAT2  | SD_DAT3       | SD_nWP      |            |
| <b>USB INTERFACE (13 Pins)</b>                   |               |             |            |
| USB+   | USB-          | ATEST       | RBIAS      |
| VDDP   | VSSP          | (2)VDDA     | (2)VSSA    |
| VREG   | XTAL1/CLKIN   | XTAL2       |            |
| <b>MEMORY/IO INTERFACE (27 Pins)</b>             |               |             |            |
| MA0  | MA1           | MA2         | MA3        |
| MA4  | MA5           | MA6         | MA7        |
| MA8  | MA9           | MA10        | MA11       |
| MA12   | MA13          | MA14        | MA15       |
| MD0  | MD1           | MD2         | MD3        |
| MD4  | MD5           | MD6         | MD7        |
| nMRD   | nMWR          | nMCE        |            |
| <b>MISC (18 Pins)</b>                            |               |             |            |
| nRESET   | GPIO1         | GPIO2       | GPIO3      |
| GPIO4  | GPIO5         | GPIO6/ROMEN | GPIO7      |
| GPIO8  | GPIO9         | GPIO10      | GPIO11     |
| GPIO12   | GPIO13        | GPIO14      | GPIO15     |
| nTEST0   | nTEST1        |             |            |
| <b>DIGITAL, POWER, GROUND &amp; NC (11 Pins)</b> |               |             |            |
| (3)VDDIO   | (4)VSSIO      | (2)VDDCORE  | (2)VSSCORE |
| <b>Total 128</b>                                 |               |             |            |

## 3.2 128 Pin List Table

### 3.2.1 128 Pin TQFP

| PIN # | NAME    | MA | PIN # | NAME    | MA | PIN # | NAME      | MA | PIN # | NAME        | MA |
|-------|---------|----|-------|---------|----|-------|-----------|----|-------|-------------|----|
| 1     | MA0     | 8  | 33    | MS_D2   | 8  | 65    | CF_nCD2   | -  | 97    | ATEST       | -  |
| 2     | MA1     | 8  | 34    | MS_D1   | 8  | 66    | CF_IRQ    | -  | 98    | VDDP        | -  |
| 3     | MA2     | 8  | 35    | MS_D0   | 8  | 67    | CF_IORDY  | -  | 99    | XTAL2       | -  |
| 4     | VDDIO   |    | 36    | MS_SCLK | 8  | 68    | CF_nIOR   | 8  | 100   | XTAL1       | -  |
| 5     | MA3     | 8  | 37    | MS_BS   | 8  | 69    | CF_nIOW   | 8  | 101   | VSSP        |    |
| 6     | MA4     | 8  | 38    | SD_nWP  | -  | 70    | CF_nRESET | 8  | 102   | VDDA(REF)   |    |
| 7     | MA5     | 8  | 39    | VDDIO   |    | 71    | CF_nCS0   | 8  | 103   | RBIAS       | -  |
| 8     | MA6     | 8  | 40    | SD_DAT0 | 8  | 72    | CF_nCS1   | 8  | 104   | VSSA(REF)   |    |
| 9     | MA7     | 8  | 41    | SD_DAT1 | 8  | 73    | CF_SA0    | 8  | 105   | VDDA        |    |
| 10    | MA8     | 8  | 42    | SD_DAT2 | 8  | 74    | VDDIO     |    | 106   | USB+        | -  |
| 11    | MA9     | 8  | 43    | SD_DAT3 | 8  | 75    | CF_SA1    | 8  | 107   | USB-        | -  |
| 12    | MA10    | 8  | 44    | SD_CMD  | 8  | 76    | CF_SA2    | 8  | 108   | VSSA        |    |
| 13    | MA11    | 8  | 45    | SD_CLK  | 8  | 77    | SM_D0     | 8  | 109   | nRESET      | -  |
| 14    | MA12    | 8  | 46    | CF_D0   | 8  | 78    | SM_D1     | 8  | 110   | VSSCORE     |    |
| 15    | MA13    | 8  | 47    | CF_D1   | 8  | 79    | VSSIO     |    | 111   | nTEST0      | -  |
| 16    | VDDCORE |    | 48    | CF_D2   | 8  | 80    | SM_D2     | 8  | 112   | nTEST1      | -  |
| 17    | MA14    | 8  | 49    | CF_D3   | 8  | 81    | SM_D3     | 8  | 113   | GPIO1       | 8  |
| 18    | MA15    | 8  | 50    | CF_D4   | 8  | 82    | SM_D4     | 8  | 114   | GPIO2       | 8  |
| 19    | MD0     | 8  | 51    | VSSIO   |    | 83    | SM_D5     | 8  | 115   | GPIO3       | 8  |
| 20    | MD1     | 8  | 52    | VSSCORE |    | 84    | SM_D6     | 8  | 116   | GPIO4       | 8  |
| 21    | MD2     | 8  | 53    | CF_D5   | 8  | 85    | SM_D7     | 8  | 117   | GPIO5       | 8  |
| 22    | MD3     | 8  | 54    | CF_D6   | 8  | 86    | SM_ALE    | 8  | 118   | GPIO6/ROMEN | 8  |
| 23    | VSSIO   |    | 55    | CF_D7   | 8  | 87    | SM_CLE    | 8  | 119   | GPIO7       | 8  |
| 24    | MD4     | 8  | 56    | CF_D8   | 8  | 88    | SM_nRE    | 8  | 120   | GPIO8       | 8  |
| 25    | MD5     | 8  | 57    | CF_D9   | 8  | 89    | SM_nWE    | 8  | 121   | GPIO9       | 8  |
| 26    | MD6     | 8  | 58    | CF_D10  | 8  | 90    | SM_nWP    | 8  | 122   | GPIO10      | 8  |
| 27    | MD7     | 8  | 59    | CF_D11  | 8  | 91    | VDDCORE   |    | 123   | GPIO11      | 8  |
| 28    | nMRD    | 8  | 60    | CF_D12  | 8  | 92    | SM_nCE    | 8  | 124   | VSSIO       |    |
| 29    | nMWR    | 8  | 61    | CF_D13  | 8  | 93    | VREG      |    | 125   | GPIO12      | 8  |
| 30    | nMCE    | 8  | 62    | CF_D14  | 8  | 94    | SM_nWPS   | -  | 126   | GPIO13      | 8  |
| 31    | MS_INS  | -  | 63    | CF_D15  | 8  | 95    | SM_nB/R   | -  | 127   | GPIO14      | 8  |
| 32    | MS_D3   | 8  | 64    | CF_nCD1 | -  | 96    | SM_nCD    | -  | 128   | GPIO15      | 8  |

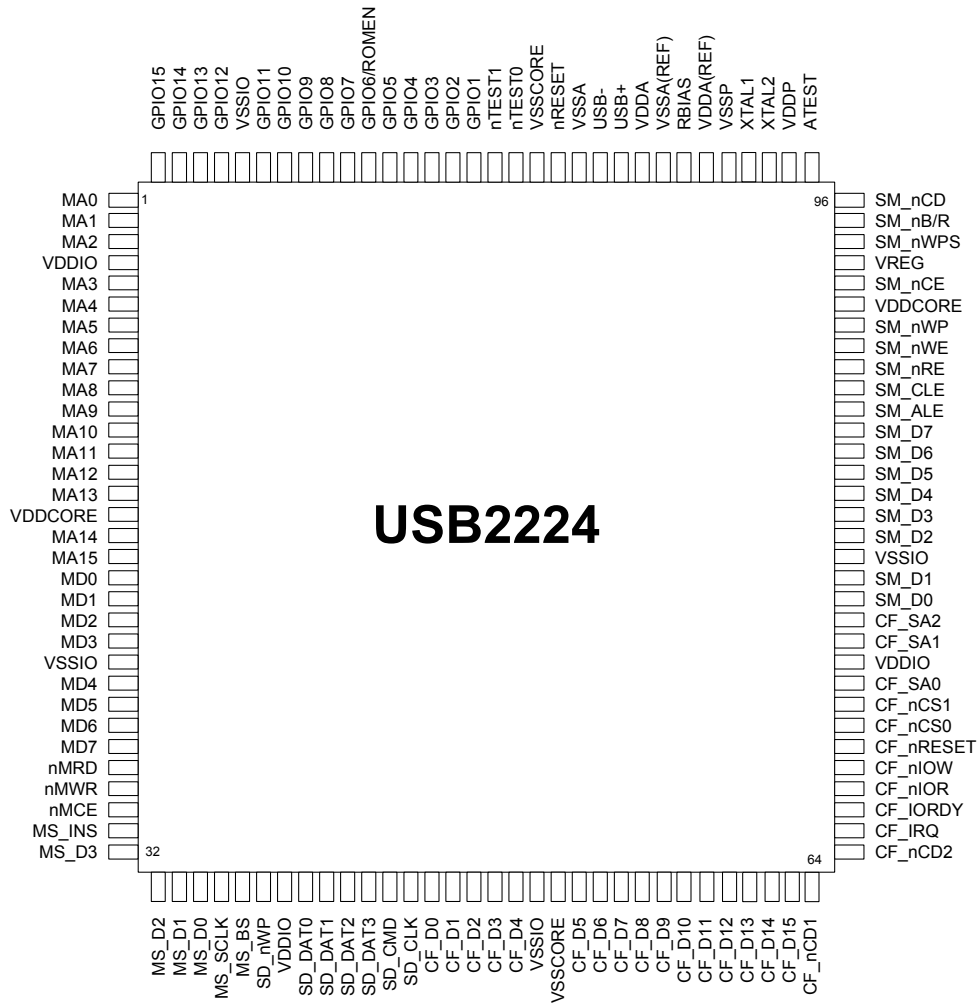
**Note 1:** RBIAS is connected to the Analog Ground plane VSSA(REF) via a resistor.

**Note 2:** When the internal 1.8V regulator is enabled, VDDCORE (91) and VDDP(98), MUST have a 10uf +/- 20%, (equivalent series resistance (ESR) <0.1ohm) bypass capacitor to VSSA.

**Note 3:** VDDA(REF) and VSSA(REF) are same as the VDDA and VSSA respectively.

# Chapter 4 Pin Configuration

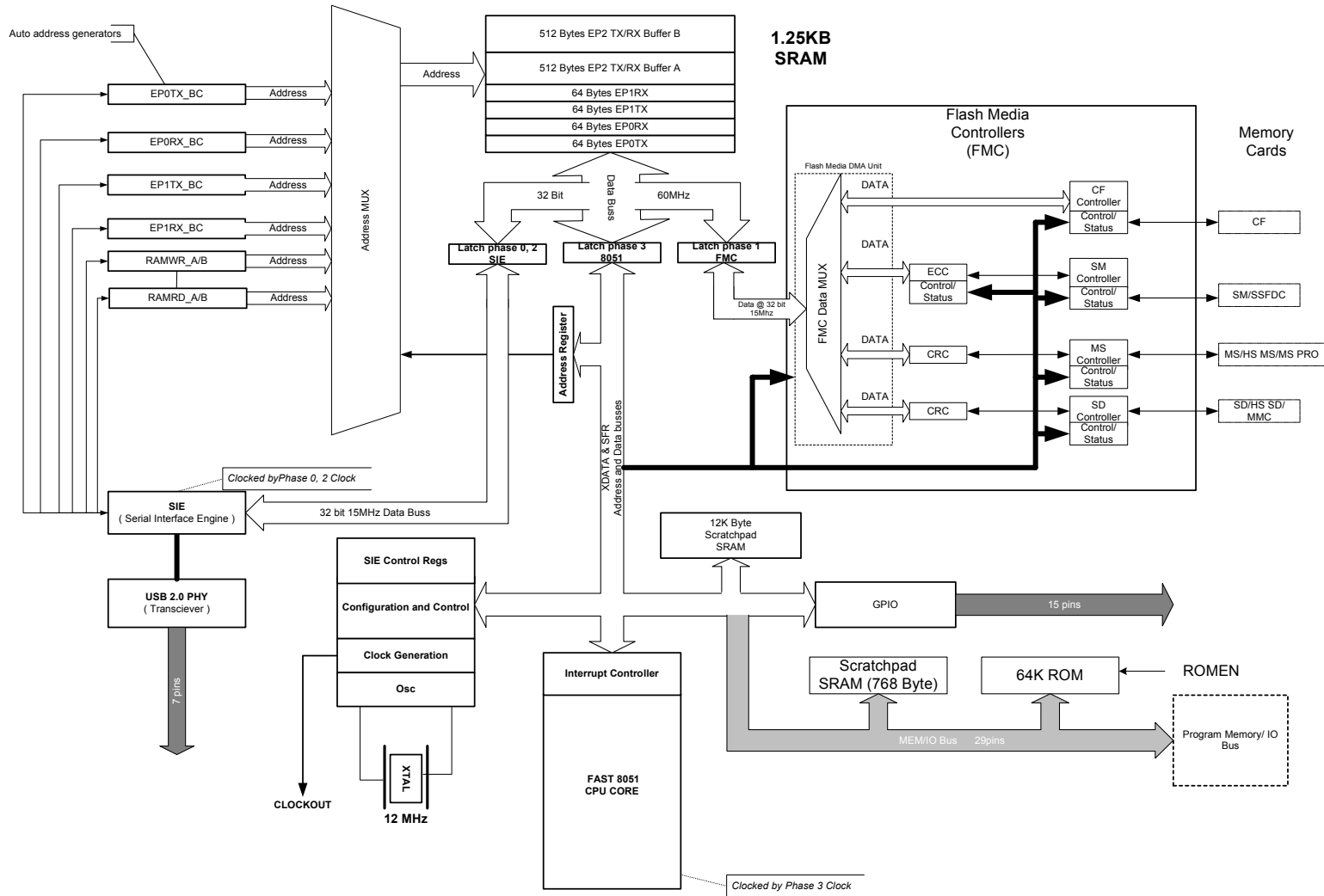
## 4.1 128 Pin TQFP







# Chapter 5 Block Diagram



## Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

### 6.1 Pin Descriptions

**Table 6.1 - Pin Description**

| NAME   | SYMBOL     | BUFFER TYPE | DESCRIPTION   |
|--|------------|-------------|---|
| <b>CompactFlash (In True IDE mode) INTERFACE</b> |            |             |   |
| CF Chip Select 1                                 | CF_nCS1    | O8          | This pin is the active low chip select 1 signal for the CF ATA device   |
| CF Chip Select 0                                 | CF_nCS0    | O8          | This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.  |
| CF Register Address 2                            | CF_SA2     | O8          | This pin is the register select address bit 2 for the CF device.  |
| CF Register Address 1                            | CF_SA1     | O8          | This pin is the register select address bit 1 for the CF device.  |
| CF Register Address 0                            | CF_SA0     | O8          | This pin is the register select address bit 0 for the CF device.  |
| CF Interrupt                                     | CF_IRQ     | IPD         | This is the active high interrupt request signal from the CF device.  |
| CF Data 15-8                                     | CF_D[15:8] | I/O8        | The bi-directional data signals CF_D15-CF_D8 in True IDE mode data transfer. The bi-directional data signal has an internal weak pull-down resistor.  |
| CF Data7-0                                       | CF_D[7:0]  | I/O8        | The bi-directional data signals CF_D7-CF_D0 in the True IDE mode data transfer.<br><br>In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0].<br><br>The bi-directional data signal has an internal weak pull-down resistor. |
| IO Ready   | CF_IORDY   | IPU         | This pin is active high input signal from CF card.  |
| CF Card Detection2                               | CF_nCD2    | IPU         | This card detection pin is connected to the ground on the CF device, when the CF device is inserted.  |
| CF Card Detection1                               | CF_nCD1    | IPU         | This card detection pin is connected to ground on the CF device, when the CF device is inserted.  |

| NAME                          | SYMBOL         | BUFFER TYPE | DESCRIPTION   |
|-------------------------------|----------------|-------------|---|
| CF Hardware Reset             | CF_nRESET      | O8          | This pin is an active low hardware reset signal to CF device.   |
| CF IO Read                    | CF_nIOR        | O8          | This pin is an active low read strobe signal for CF device, when the CFC is enabled.  |
| CF IO Write Strobe            | CF_nIOW        | O8          | This pin is an active low write strobe signal for CF device, when the CFC is enabled.   |
| <b>SmartMedia INTERFACE</b>   |                |             |   |
| SM Write Protect              | SM_nWP         | O8          | This pin is an active low write protect signal for the SM device, when the SMC is enabled.  |
| SM Address Strobe             | SM_ALE         | O8          | This pin is an active high Address Latch Enable signal for the SM device, when the SMC is enabled.  |
| SM Command Strobe             | SM_CLE         | O8          | This pin is an active high Command Latch Enable signal for the SM device, when the SMC is enabled.  |
| SM Data7-0                    | SM_D[7:0]      | I/O8        | These pins are the bi-directional data signal SM_D7-SM_D0, when the SMC is enabled.   |
| SM Read Enable                | SM_nRE         | O8          | This pin is an active low read strobe signal for SM device, when SMC is enabled.  |
| SM Write Enable               | SM_nWE         | O8          | This pin is an active low write strobe signal for SM device, when SMC is enabled.   |
| SM Write Protect Switch       | SM_nWPS        | IPU         | A write-protect seal is detected, when this pin is low.   |
| SM Busy or Data Ready         | SM_nB/R        | I           | This pin is connected to the BSY/RDY pin of the SM device.<br><br>An external pull-up resistor is required on this signal. The pull-up resistor should be attached to the power of SM/NAND flash device.                            |
| SM Chip Enable                | SM_nCE         | O8          | This pin is the active low chip enable signal to the SM device.   |
| SM Card Detection             | SM_nCD         | IPU         | This is the card detection signal from SM device to indicate if the device is inserted.   |
| <b>MEMORY STICK INTERFACE</b> |                |             |   |
| MS Bus State                  | MS_BS          | O8          | This pin is connected to the BS pin of the MS device.<br><br>It is used to control the Bus States 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.   |
| MS System Data In/Out         | MS_SDIO /MS_D0 | I/O8        | This pin is a bi-directional data signal for the MS device. Most significant bit (MSB) of each byte is transmitted first by either MSC or MS device.<br><br>The bi-directional data signal has an internal weak pull-down resistor. |
| MS System Data In/Out         | MS_D1          | IO8PD       | This pin is a bi-directional data signal for the MS device.<br><br>The bi-directional data signal has an internal weak pull-down resistor that is internally controlled.  |
| MS System Data In/Out         | MS_D[3:2]      | I/O8        | This pin is a bi-directional data signal for the MS device.<br><br>The bi-directional data signal has an internal weak pull-down resistor.  |
| MS Card Insertion             | MS_INS         | IPU         | This pin is the card detection signal from the MS device to indicate, if the device is inserted.  |

| NAME                               | SYMBOL          | BUFFER TYPE | DESCRIPTION  |
|------------------------------------|-----------------|-------------|--|
| MS System CLK                      | MS_SCLK         | O8          | This pin is an output clock signal to the MS device.   |
| <b>SD INTERFACE</b>                |                 |             |  |
| SD Data3-0                         | SD_DAT[3:0]     | I/O8        | These are bi-directional data signals.   |
| SD Clock                           | SD_CLK          | O8          | This is an output clock signal to SD/MMC device.   |
| SD Command                         | SD_CMD          | I/O8        | This is a bi-directional signal that connects to the CMD signal of SD/MMC device.  |
| SD Write Protected                 | SD_nWP          | IPD         | This pin is Write Protect Switch input signal with an internal weak pull-down.   |
| <b>USB INTERFACE</b>               |                 |             |  |
| USB Bus Data                       | USB-<br>USB+    | IO-U        | These pins connect to the USB bus data signals.  |
| USB Transceiver Bias               | RBIAS           | I           | A 12.0K $\Omega$ $\pm$ 1% resistor is attached from ground to this pin to set the transceiver's internal bias currents.  |
| Analog Test                        | ATEST           | IOA         | This signal is used for testing the analog section of the chip and should be connected to VDDA for normal operation.   |
| 1.8v Analog Power                  | VDDP            |             | 1.8v Analog Power<br><br>This pin MUST have a 10uf +/- 20%, (equivalent series resistance (ESR) <0.1ohm) bypass capacitor to VSSA. This capacitor should be placed as close to the pin as possible.  |
| Analog Ground Reference            | VSSP            |             | Analog Ground Reference for 1.8v Analog power.   |
| 3.3v Analog Power                  | VDDA            |             | 3.3v Analog Power  |
| Analog Ground Reference            | VSSA            |             | Analog Ground Reference for 3.3v Analog Power.   |
| 1.8v Voltage Regulator for USB PHY | VREG            |             | This pin is connected to 3.3v.   |
| Crystal Input/External Clock Input | XTAL1/<br>CLKIN | ICLKx       | 12Mhz Crystal or external clock input.<br><br>This pin can be connected to one terminal of the crystal or can be connected to an external 12Mhz clock when a crystal is not used.  |
| Crystal Output                     | XTAL2           | OCLKx       | 12Mhz Crystal<br><br>This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.                                      |
| <b>MEMORY/IO INTERFACE</b>         |                 |             |  |
| Memory Data Bus                    | MD[7:0]         | IO8         | When using external program memory, these signals are used to transfer data between the internal CPU and the external program memory.<br><br>When using internal program ROM, internal weak pull up resistors are activated to prevent these pins from floating. |

| NAME                 | SYMBOL       | BUFFER TYPE | DESCRIPTION   |
|----------------------|--------------|-------------|---|
| Memory Address Bus   | MA[15:0]     | O8          | These signals address memory locations within the external memory.  |
| Memory Read Strobe   | nMWR         | O8          | Program Memory Write; active low  |
| Memory Read Strobe   | nMRD         | O8          | Program Memory Read; active low   |
| Memory Chip Enable   | nMCE         | O8          | Program Memory Chip Enable; active low. This signal is asserted, when the device is not in SUSPEND mode.<br><br><b>Note:</b> This signal is held in a logic 'high' state (inactive) during nRESET assertion.  |
| <b>MISC</b>          |              |             |   |
| GPIO6, ROMEN and RXD | GPIO6 /ROMEN | I/O8PU      | <p>This pin has an internal weak pullup resistor that can be enabled or disabled by the state of nRESET. The pullup is enabled when nRESET is active. The pullup is disabled, when the nRESET is inactive (some clock cycles later, after the rising edge of nRESET).</p> <p>The state of this pin is latched internally on the rising edge of nRESET to determine if internal or external program memory is used. The state latched is stored in ROMEN bit of GPIO_IN1 register. After the rising edge of nRESET, this pin may be used as GPIO6 or RXD.</p> <p>When pulled low via an external weak pulldown resistor, an external program memory should be connected to the memory data bus. The USB2224 uses this external bus for program execution.</p> <p>When this pin is left unconnected or pulled high by a weak pullup resistor, the USB2224 uses the internal ROM for program execution.</p> <p>This pin's function while operating from internal ROM is shown in Table 6.3 - GPIO Usage.</p> |
| General Purpose I/O  | GPIO1        | I/O8        | <p>This pin may be used either as input, edge sensitive interrupt input, or output.</p> <p>This pin's function while operating from internal ROM is shown in Table 6.3 - GPIO Usage.</p>  |
| General Purpose I/O  | GPIO2        | I/O8        | <p>This pin may be used either as input, edge sensitive interrupt input, or output.</p> <p>This pin's function while operating from internal ROM is shown in Table 6.3 - GPIO Usage.</p>  |
| General Purpose I/O  | GPIO3        | I/O8        | <p>This pin may be used either as input, edge sensitive interrupt input, or output.</p> <p>This pin's function while operating from internal ROM is shown in Table 6.3 - GPIO Usage.</p>  |

| NAME   | SYMBOL     | BUFFER TYPE | DESCRIPTION   |
|--|------------|-------------|---|
| General Purpose I/O                            | GPIO4      | I/O8        | This pin may be used either as input, edge sensitive interrupt input, or output.<br><br>This pin's function while operating from internal ROM is shown in Table 6.3 - GPIO Usage.   |
| General Purpose I/O                            | GPIO5      | I/O8        | This pin may be used either as input, edge sensitive interrupt input, or output.<br><br>This pin's function while operating from internal ROM is shown in Table 6.3 - GPIO Usage.   |
| General Purpose I/O                            | GPIO7      | I/O8        | This pin may be used either as input, edge sensitive interrupt input, or output.<br><br>This pin's function while operating from internal ROM is shown in Table 6.3 - GPIO Usage.   |
| General Purpose I/O                            | GPIO[15:8] | I/O8        | These pins may be used either as input, or output.<br><br>These pins' functions while operating from internal ROM are shown in Table 6.3 - GPIO Usage.  |
| RESET input                                    | nRESET     | IS          | This active low signal is used by the system to reset the chip. The active low pulse should be at least 1μs wide.   |
| TEST Input                                     | nTEST[0:1] | I           | These signals are used for testing the chip. User should normally tie them high externally.   |
| <b>DIGITAL POWER, GROUNDS, and NO CONNECTS</b> |            |             |   |
| 1.8v Digital Core Power                        | VDDCORE    |             | +1.8V Core power<br><br>All VDDCORE pins must be connected together on the circuit board.<br><br>Pin 91 MUST have a 10uf +/- 20%, (equivalent series resistance (ESR) <0.1ohm) bypass capacitor to VSSA, and this capacitor should be placed as close to the pin as possible. |
| 3.3v Digital I/O power                         | VDDIO      |             | +3.3V I/O power   |
| VDDCORE reference ground                       | VSSCORE    |             | VDDCORE ground Reference  |
| VDDIO reference ground                         | VSSIO      |             | VDDIO ground reference  |

**Note 1:** Hot-insertion capable card connectors are required for all of flash medias. It is required for SD connector to have Write Protect switch. This allows the chip to detect MMC card.

**Note 2:** nMCE is normally asserted except when the system is in standby mode.

## 6.2 Buffer Type Descriptions

**Table 6.2 - USB2224 Buffer Type Descriptions**

| BUFFER | DESCRIPTION  |
|--------|--|
| I      | Input  |
| IPU    | Input with controlled internal weak pull-up resistor.          |
| IPD    | Input with controlled internal weak pull-down resistor.        |
| IS     | Input with Schmitt trigger                                     |
| I/O8   | Input/Output with 8mA drive                                    |
| I/OD8  | Input/Open drain output ... 8mA sink                           |
| O8     | Output with 8mA drive  |
| I/O8PU | Input/Output with 8mA drive controlled weak pull-up resistor   |
| I/O8PD | Input/Output with 8mA drive controlled weak pull-down resistor |
| ICLKx  | XTAL clock input   |
| OCLKx  | XTAL clock output  |
| I/O-U  | Analog Input/Output Defined in USB specification               |
| O-U    | Analog Output  |
| I-U    | Analog Input   |
| OIA    | Special analog Input/Output                                    |

## 6.3 GPIO Usage Table

**Table 6.3 - GPIO Usage**

| NAME   | ACTIVE LEVEL | SYMBOL                           | DESCRIPTION AND NOTE  |
|--------|--------------|----------------------------------|---|
| GPIO1  | H/L          | ACT/DOOR                         | Media Activity LED / xD Door SW Input   |
| GPIO2  | H            | EE_CS                            | Serial EE PROM chip select  |
| GPIO3  | H            | V_BUS                            | USB V bus detect  |
| GPIO4  | H/L          | EE_DIN/EE_DOUT/xDID              | Serial EE PROM input/output and xD ID pin input   |
| GPIO5  | L            | SD_CD                            | SD Card Detect SW Input. In production ROM versions, this pin must always be pulled high except to indicate SD card insertion. If no SD interface is used, this pin must still be pulled high for proper operation. |
| GPIO6  | H            | A16 ( external ROM only ) /ROMEN | Int/Ext ROM select. External program memory A16 address line connect for DFU.   |
| GPIO7  | H            | EE_CLK                           | Serial EE PROM clock output   |
| GPIO8  | L            | MS Power Control                 | Memory Stick Card Power Control   |
| GPIO9  | L            | CF Power Control                 | CompactFlash Card Power Control   |
| GPIO10 | L            | SM Power Control                 | SmartMedia Card Power Control   |
| GPIO11 | L            | SD Power Control                 | SD/MMC Card Power Control   |

| <b>NAME</b> | <b>ACTIVE LEVEL</b> | <b>SYMBOL</b>     | <b>DESCRIPTION AND NOTE</b>           |
|-------------|---------------------|-------------------|---------------------------------------|
| GPIO12      | H                   | MS/MSPro Activity | Memory Stick(/Pro) Activity Indicator |
| GPIO13      | H                   | CF Activity       | CompactFlash Activity Indicator       |
| GPIO14      | H                   | SM/XDAActivity    | SmartMedia/XD Activity Indicator      |
| GPIO15      | H                   | SD/MMC Activity   | SD/MMC Activity Indicator             |



## Chapter 7 DC Parameters

### 7.1 Maximum Guaranteed Ratings

|   |                |
|---|----------------|
| Operating Temperature Range .....                         | 0°C to +70°C   |
| Storage Temperature Range .....                           | -55° to +150°C |
| Lead Temperature Range (soldering, 10 seconds) .....      | +325°C         |
| Positive Voltage on any pin, with respect to Ground ..... | 5.5V           |
| Negative Voltage on any pin, with respect to Ground ..... | -0.3V          |
| Maximum $V_{DD}$ , $V_{DDP}$ .....                        | +2.5V          |
| Maximum $V_{DDIO}$ , $V_{DDA}$ .....                      | +4.0V          |

\* Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

#### Notes:

- When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.
- The name "VDD" is the same as VDDCORE

### 7.2 DC Electrical Characteristics

( $T_A = 0^\circ\text{C} - 70^\circ\text{C}$ ,  $V_{DDIO}$ ,  $V_{DDA} = +3.3\text{ V} \pm 10\%$ ,  $V_{DD}$ ,  $V_{DDP} = +1.8\text{ V} \pm 10\%$ ,)

| PARAMETER                   | SYMBOL     | MIN | TYP | MAX | UNITS | COMMENTS   |
|-----------------------------|------------|-----|-----|-----|-------|------------|
| <b>I Type Input Buffer</b>  |            |     |     |     |       |            |
| Low Input Level             | $V_{ILI}$  |     |     | 0.8 | V     | TTL Levels |
| High Input Level            | $V_{IHI}$  | 2.0 |     |     | V     |            |
| <b>IS Type Input Buffer</b> |            |     |     |     |       |            |
| Low Input Level             | $V_{ILI}$  |     |     | 0.8 | V     | TTL Levels |
| High Input Level            | $V_{IHI}$  | 2.0 |     |     | V     |            |
| Hysteresis                  | $V_{HYSI}$ |     | 500 |     | mV    |            |

| PARAMETER                | SYMBOL     | MIN | TYP | MAX | UNITS         | COMMENTS   |
|--------------------------|------------|-----|-----|-----|---------------|--|
| <b>ICLK Input Buffer</b> |            |     |     |     |               |  |
| Low Input Level          | $V_{ILCK}$ |     |     | 0.4 | V             |  |
| High Input Level         | $V_{IHCK}$ | 2.2 |     |     | V             |  |
| <b>Input Leakage</b>     |            |     |     |     |               |  |
| (All I and IS buffers)   |            |     |     |     |               |  |
| Low Input Leakage        | $I_{IL}$   | -10 |     | +10 | uA            | $V_{IN} = 0$   |
| High Input Leakage       | $I_{IH}$   | -10 |     | +10 | uA            | $V_{IN} = V_{DDIO}$                                    |
| <b>O8 Type Buffer</b>    |            |     |     |     |               |  |
| Low Output Level         | $V_{OL}$   |     |     | 0.4 | V             | $I_{OL} = 8 \text{ mA} @$<br>$V_{DDIO} = 3.3\text{V}$  |
| High Output Level        | $V_{OH}$   | 2.4 |     |     | V             | $I_{OH} = -4\text{mA} @$<br>$V_{DDIO} = 3.3\text{V}$   |
| Output Leakage           | $I_{OL}$   | -10 |     | +10 | uA            | $V_{IN} = 0 \text{ to } V_{DDIO}$<br><b>(Note 7.1)</b> |
| <b>I/O8 Type Buffer</b>  |            |     |     |     |               |  |
| Low Output Level         | $V_{OL}$   |     |     | 0.4 | V             | $I_{OL} = 8 \text{ mA} @$<br>$V_{DDIO} = 3.3\text{V}$  |
| HIGH OUTPUT LEVEL        | $V_{OH}$   | 2.4 |     |     | V             | $I_{OH} = -4 \text{ mA} @$<br>$V_{DDIO} = 3.3\text{V}$ |
| Output Leakage           | $I_{OL}$   | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{DDIO}$<br><b>(Note 7.1)</b> |
| <b>I/O12 Type Buffer</b> |            |     |     |     |               |  |
| Low Output Level         | $V_{OL}$   |     |     | 0.4 | V             | $I_{OL} = 12 \text{ mA} @$<br>$V_{DDIO} = 3.3\text{V}$ |
| High Output Level        | $V_{OH}$   | 2.4 |     |     | V             | $I_{OH} = -6\text{mA} @$<br>$V_{DDIO} = 3.3\text{V}$   |
| Output Leakage           | $I_{OL}$   | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{DDIO}$<br><b>(Note 7.1)</b> |

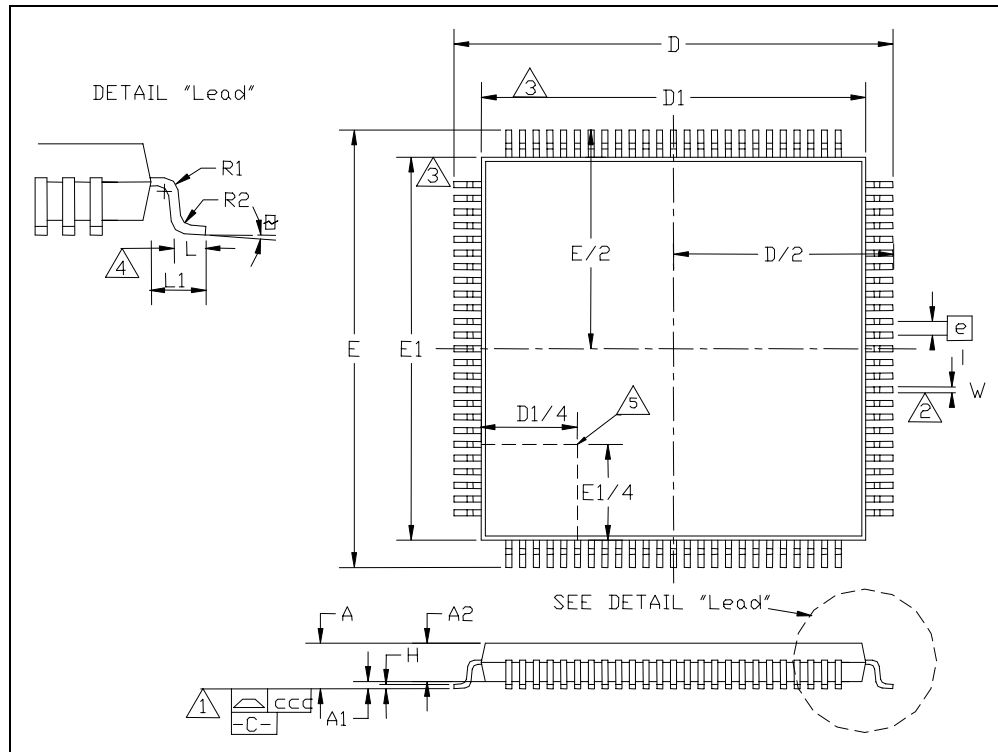
| PARAMETER                          | SYMBOL       | MIN | TYP | MAX | UNITS         | COMMENTS   |
|------------------------------------|--------------|-----|-----|-----|---------------|--|
| <b>I/O24 Type Buffer</b>           |              |     |     |     |               |  |
| Low Output Level                   | $V_{OL}$     |     |     | 0.4 | V             | $I_{OL} = 24 \text{ mA @ } V_{DDIO} = 3.3\text{V}$     |
| High Output Level                  | $V_{OH}$     | 2.4 |     |     | V             | $I_{OH} = -12 \text{ mA @ } V_{DDIO} = 3.3\text{V}$    |
| Output Leakage                     | $I_{OL}$     | -10 |     | +10 | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{DDIO}$<br><b>(Note 7.1)</b> |
| <b>IO-U</b>                        |              |     |     |     |               |  |
| Supply Current Unconfigured        | $I_{CCINIT}$ |     | 45  | 60  | mA            | @ $V_{DD}, V_{DDP} = 1.8\text{V}$                      |
|                                    |              |     | 10  | 20  | mA            | @ $V_{DDIO}, V_{DDA} = 3.3\text{V}$                    |
| Supply Current Active (Full Speed) | $I_{CC}$     |     | 35  | 60  | mA            | @ $V_{DD}, V_{DDP} = 1.8\text{V}$                      |
|                                    |              |     | 15  | 30  | mA            | @ $V_{DDIO}, V_{DDA} = 3.3\text{V}$                    |
| Supply Current Active (High Speed) | $I_{CC}$     |     | 45  | 70  | mA            | @ $V_{DD}, V_{DDP} = 1.8\text{V}$                      |
|                                    |              |     | 15  | 30  | mA            | @ $V_{DDIO}, V_{DDA} = 3.3\text{V}$                    |
| Supply Current Standby             | $I_{CSBY}$   |     | 160 | 180 | $\mu\text{A}$ | @ $V_{DD}, V_{DDP} = 1.8\text{V}$                      |
|                                    |              |     | 215 | 240 | $\mu\text{A}$ | @ $V_{DDIO}, V_{DDA} = 3.3\text{V}$                    |

**Note 7.1** Output leakage is measured with the current pins in high impedance.

**CAPACITANCE  $T_A = 25^\circ\text{C}; f_c = 1\text{MHz}; V_{DD}, V_{DDP} = 1.8\text{V}$**

| PARAMETER               | SYMBOL    | LIMITS |     |     | UNIT | TEST CONDITION   |
|-------------------------|-----------|--------|-----|-----|------|--|
|                         |           | MIN    | TYP | MAX |      |  |
| Clock Input Capacitance | $C_{IN}$  |        |     | 20  | pF   | All pins except USB pins (and pins under test tied to AC ground) |
| Input Capacitance       | $C_{IN}$  |        |     | 10  | pF   |  |
| Output Capacitance      | $C_{OUT}$ |        |     | 20  | pF   |  |

## Chapter 8 Package Outline



**Figure 8.1 - 128 Pin TQFP Package**

**Table 8.1 - 128 Pin TQFP Package Parameters**

|            | MIN        | NOMINAL | MAX   | REMARKS                |
|------------|------------|---------|-------|------------------------|
| <b>A</b>   | ~          | ~       | 1.20  | Overall Package Height |
| <b>A1</b>  | 0.05       | ~       | 0.15  | Standoff               |
| <b>A2</b>  | 0.95       | ~       | 1.05  | Body Thickness         |
| <b>D</b>   | 15.80      | ~       | 16.20 | X Span                 |
| <b>D1</b>  | 13.80      | ~       | 14.20 | X body Size            |
| <b>E</b>   | 15.80      | ~       | 16.20 | Y Span                 |
| <b>E1</b>  | 13.80      | ~       | 14.20 | Y body Size            |
| <b>H</b>   | 0.09       | ~       | 0.20  | Lead Frame Thickness   |
| <b>L</b>   | 0.45       | 0.60    | 0.75  | Lead Foot Length       |
| <b>L1</b>  | ~          | 1.00    | ~     | Lead Length            |
| <b>e</b>   | 0.40 Basic |         |       | Lead Pitch             |
| <b>θ</b>   | 0°         | ~       | 7°    | Lead Foot Angle        |
| <b>W</b>   | 0.13       | 0.18    | 0.23  | Lead Width             |
| <b>R1</b>  | 0.08       | ~       | ~     | Lead Shoulder Radius   |
| <b>R2</b>  | 0.08       | ~       | 0.20  | Lead Foot Radius       |
| <b>ccc</b> | ~          | ~       | 0.08  | Coplanarity            |

**Notes:**

- 1) Controlling Unit: millimeter.
- 2) Tolerance on the true position of the leads is  $\pm 0.035$  mm maximum.
- 3) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
- 4) Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
- 5) Details of pin 1 identifier are optional but must be located within the zone indicated.