OptiMOS™3 Power-Transistors

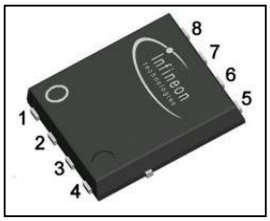
Features

- Dual N-channel, logic level
- Fast switching MOSFETs for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC[1] for target applications
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% Avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

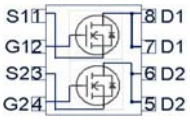
V_{DS}	30	V
$R_{DS(on),max}$	15	mΩ
I_D	20	A

PG-TDSON-8



RoHS

Halogen-Free



Type	Package	Marking
BSC150N03LD G	PG-TDSON-8	150N03LD

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			≤10 secs	steady state	
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	20		A
		V_{GS}=10 V, T_C=100 °C	20		
		V_{GS}=4.5 V, T_C=25 °C	20		
		V_{GS}=4.5 V, T_C=100 °C	17		
		V_{GS}=10 V, T_A=25 °C[3]	12.4	8	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	80		
Avalanche energy, single pulse	E_{AS}	I_D=20 A, R_{GS}=25 Ω	10		mJ
Gate source voltage	V_{GS}		±20		V
Power dissipation	P_{tot}	T_C=25 °C	26		W
		T_A=25 °C[3]	3.6	1.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

[1] J-STD20 and JESD22

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	-	4.9	K/W
		top			20	
Thermal resistance, junction - ambient, 6 cm² cooling area[3)]	R_{thJA}	t≤10 s	-	-	35	
		steady state	-	-	85	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1	-	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=20 A	-	17.6	22	mΩ
		V_{GS}=10 V, I_D=20 A	-	12.5	15	
Gate resistance	R_G		-	1.2	1.8	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=20 A	18	35	-	S

[2)] See figure 3

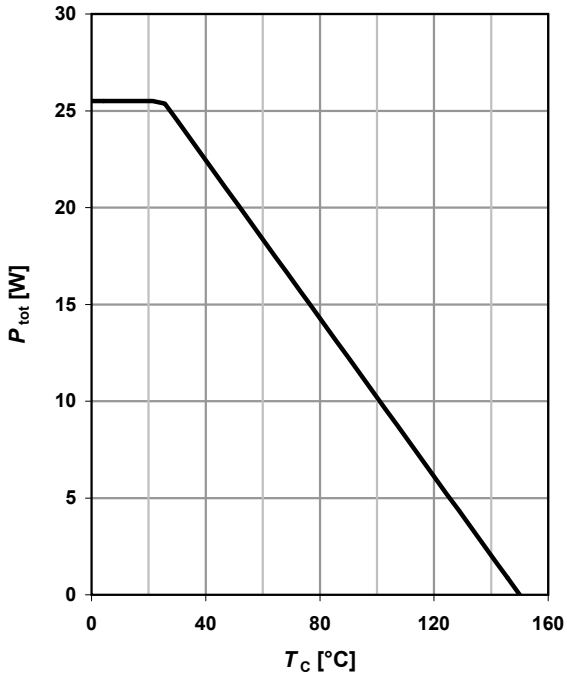
[3)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	850	1100	pF
Output capacitance	C_{oss}		-	350	470	
Reverse transfer capacitance	C_{rss}		-	16	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=20 A, R_G=1.6 Ω	-	2.7	-	ns
Rise time	t_r		-	2.2	-	
Turn-off delay time	$t_{d(off)}$		-	12	-	
Fall time	t_f		-	2.0	-	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V	-	2.6	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.2	-	
Gate to drain charge	Q_{gd}		-	1.2	-	
Switching charge	Q_{sw}		-	2.6	-	
Gate charge total	Q_g		-	4.8	6.4	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V
Gate charge total	Q_g	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 10 V	-	10	13.2	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V	-	4.2	-	
Output charge	Q_{oss}	V_{DD}=15 V, V_{GS}=0 V	-	9	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	20	A
Diode pulse current	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=20 A, T_j=25 °C	-	0.93	1.1	V
Reverse recovery charge	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs	-	-	10	nC

[4)] See figure 16 for gate charge parameter definition

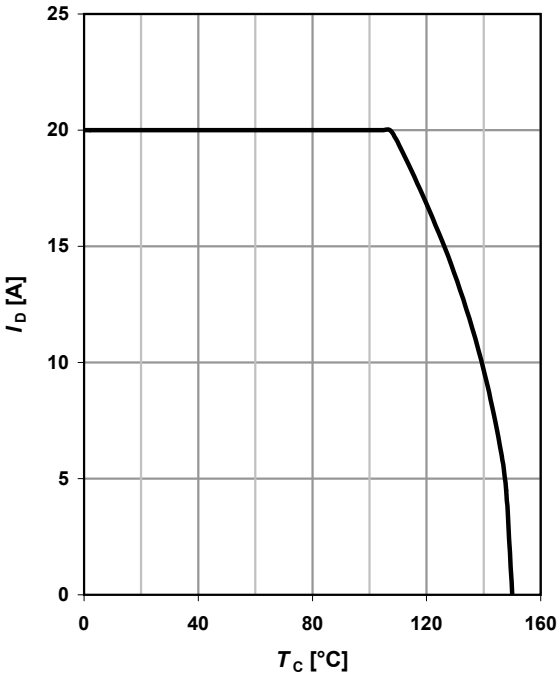
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

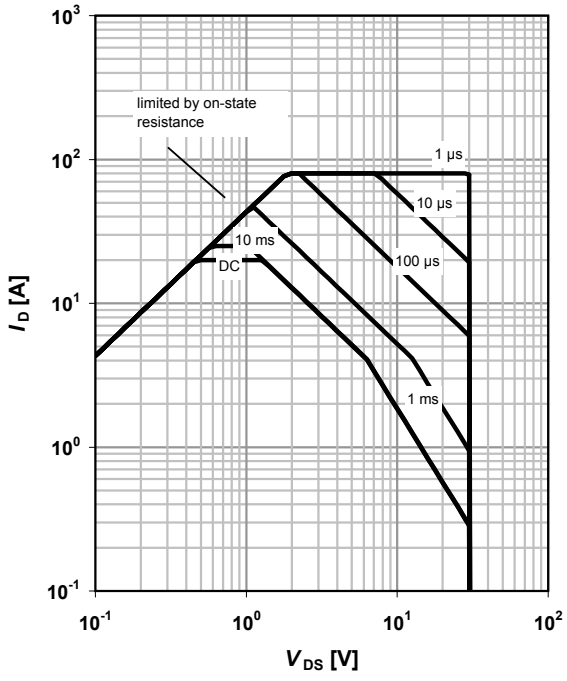
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

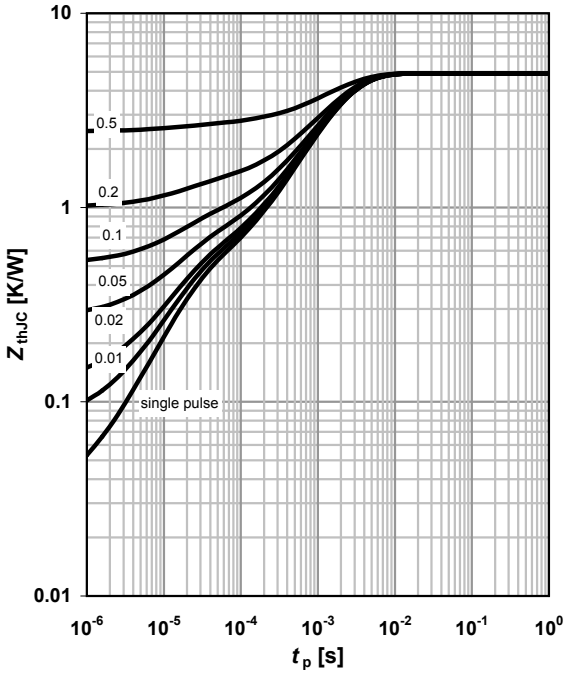
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

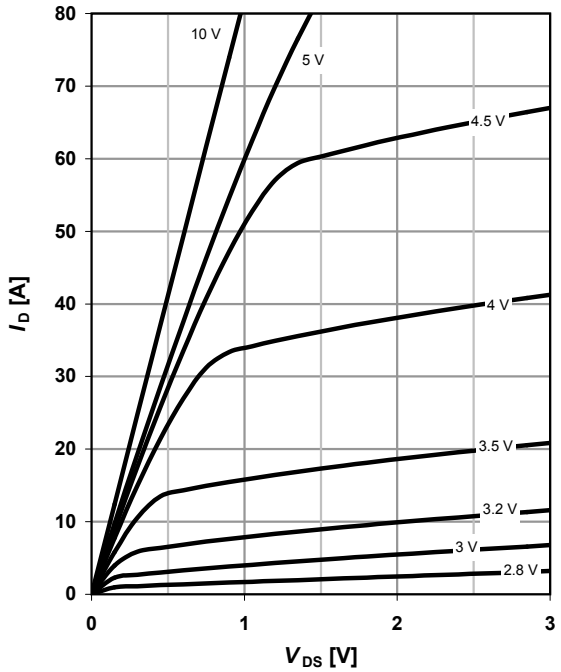
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

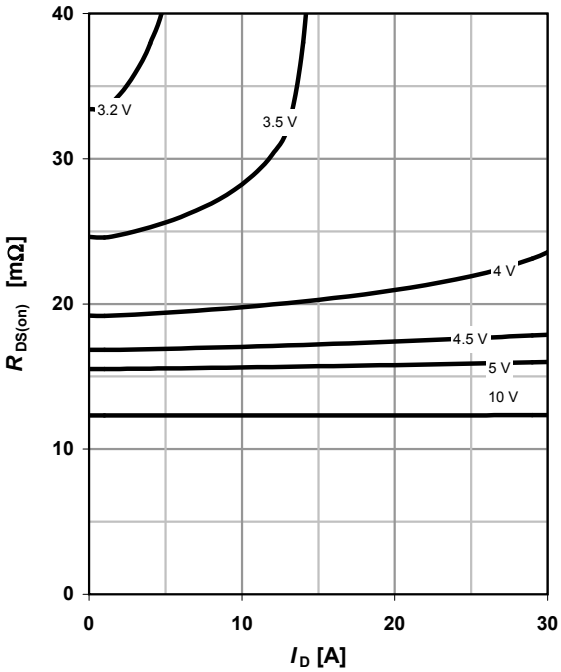
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

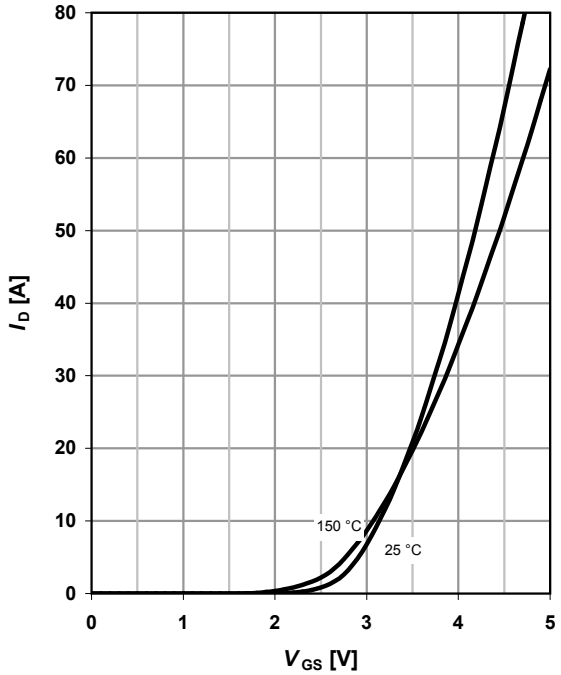
parameter: V_{GS}



7 Typ. transfer characteristics

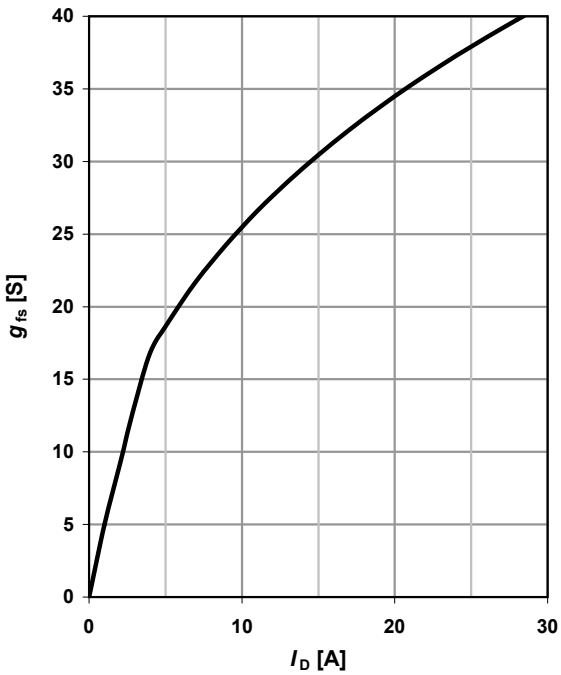
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



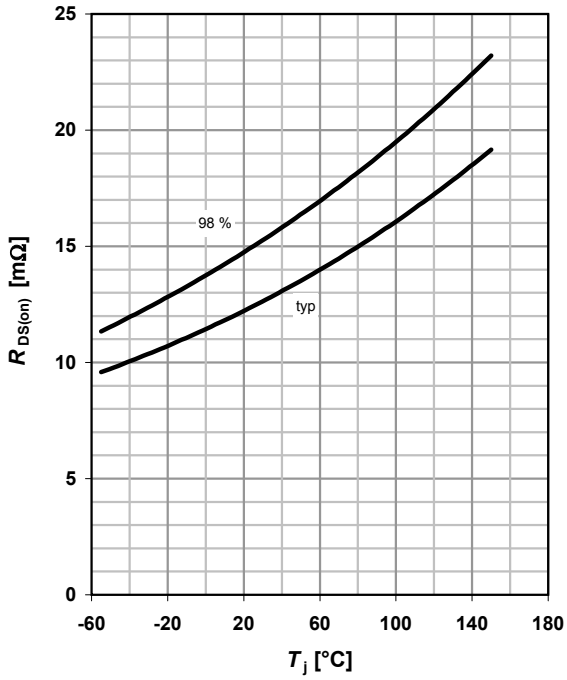
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



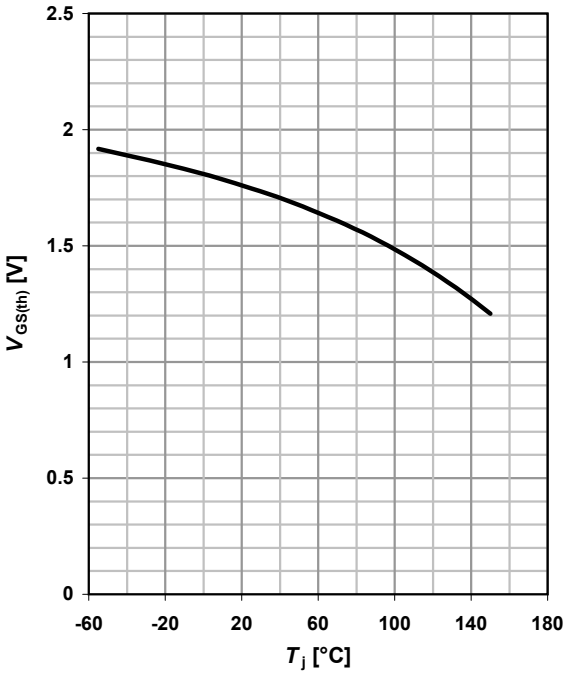
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V



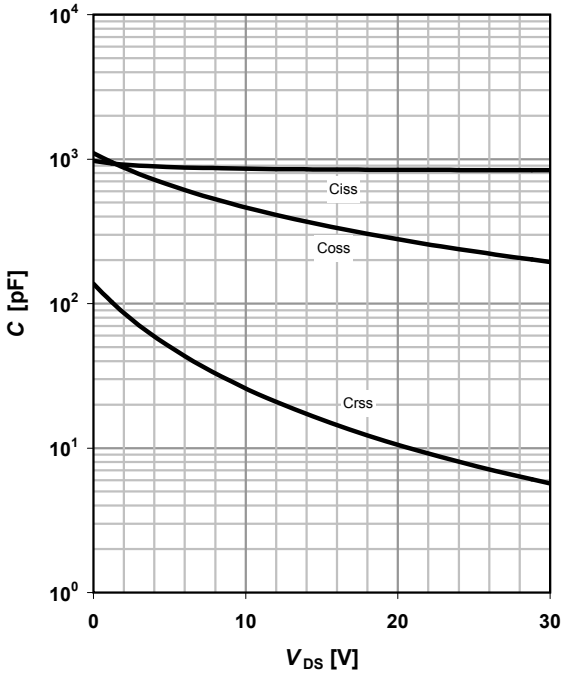
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



11 Typ. capacitances

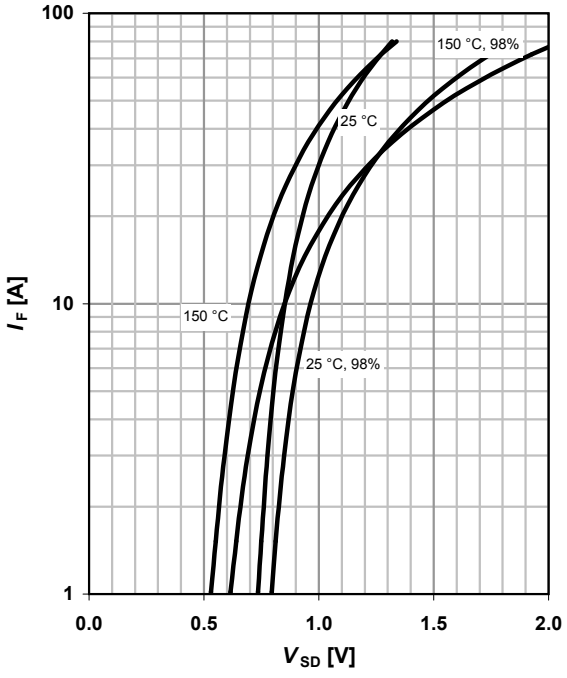
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

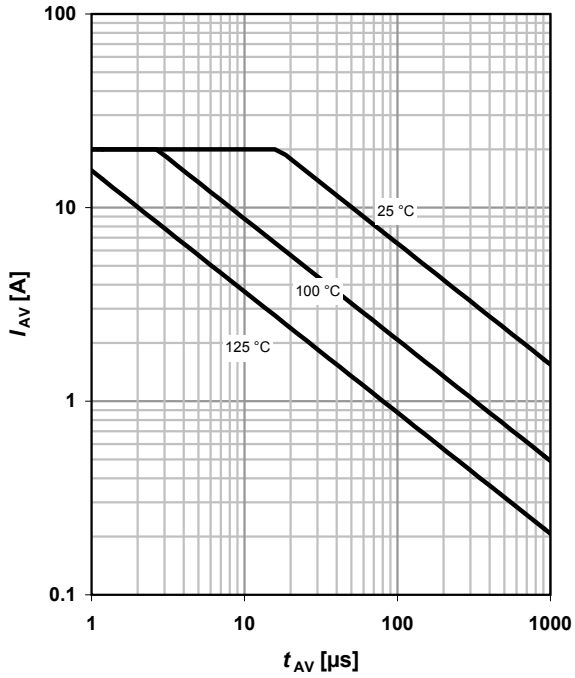
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

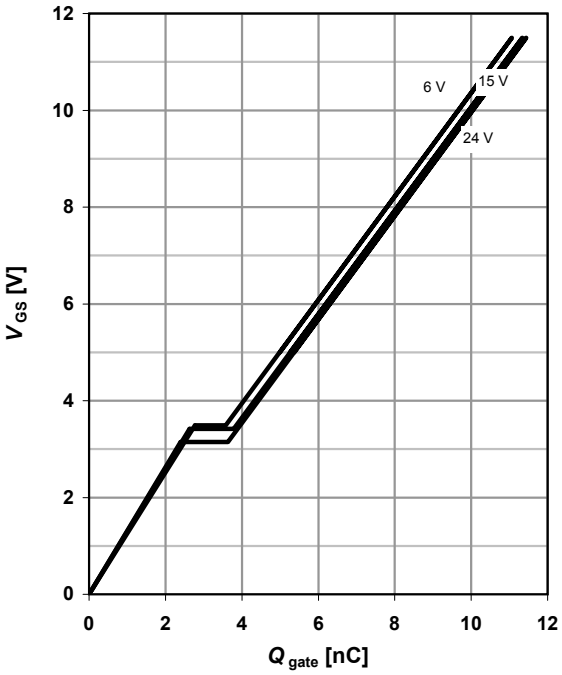
parameter: $T_{j(start)}$



14 Typ. gate charge

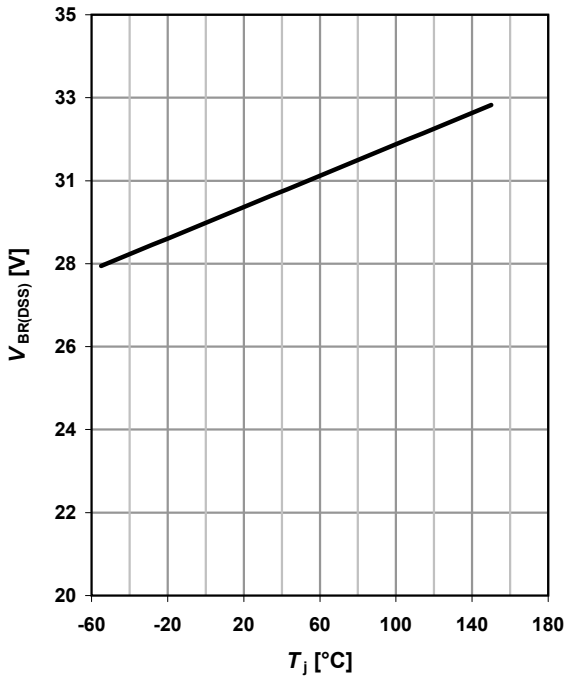
V_{GS}=f(Q_{gate}); I_D=20 A pulsed

parameter: V_{DD}

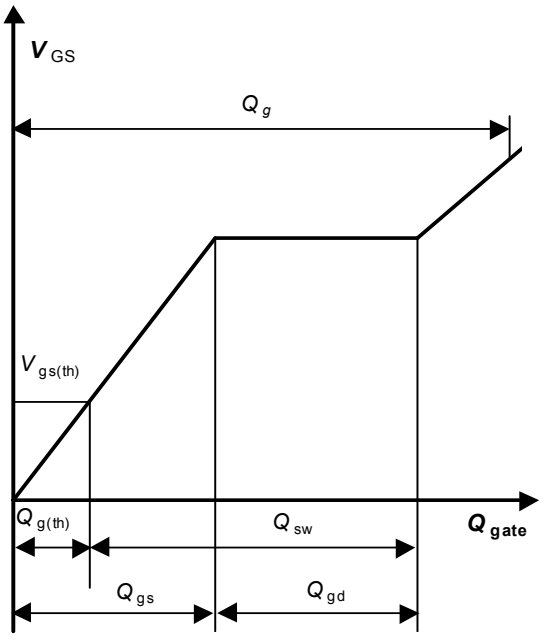


15 Drain-source breakdown voltage

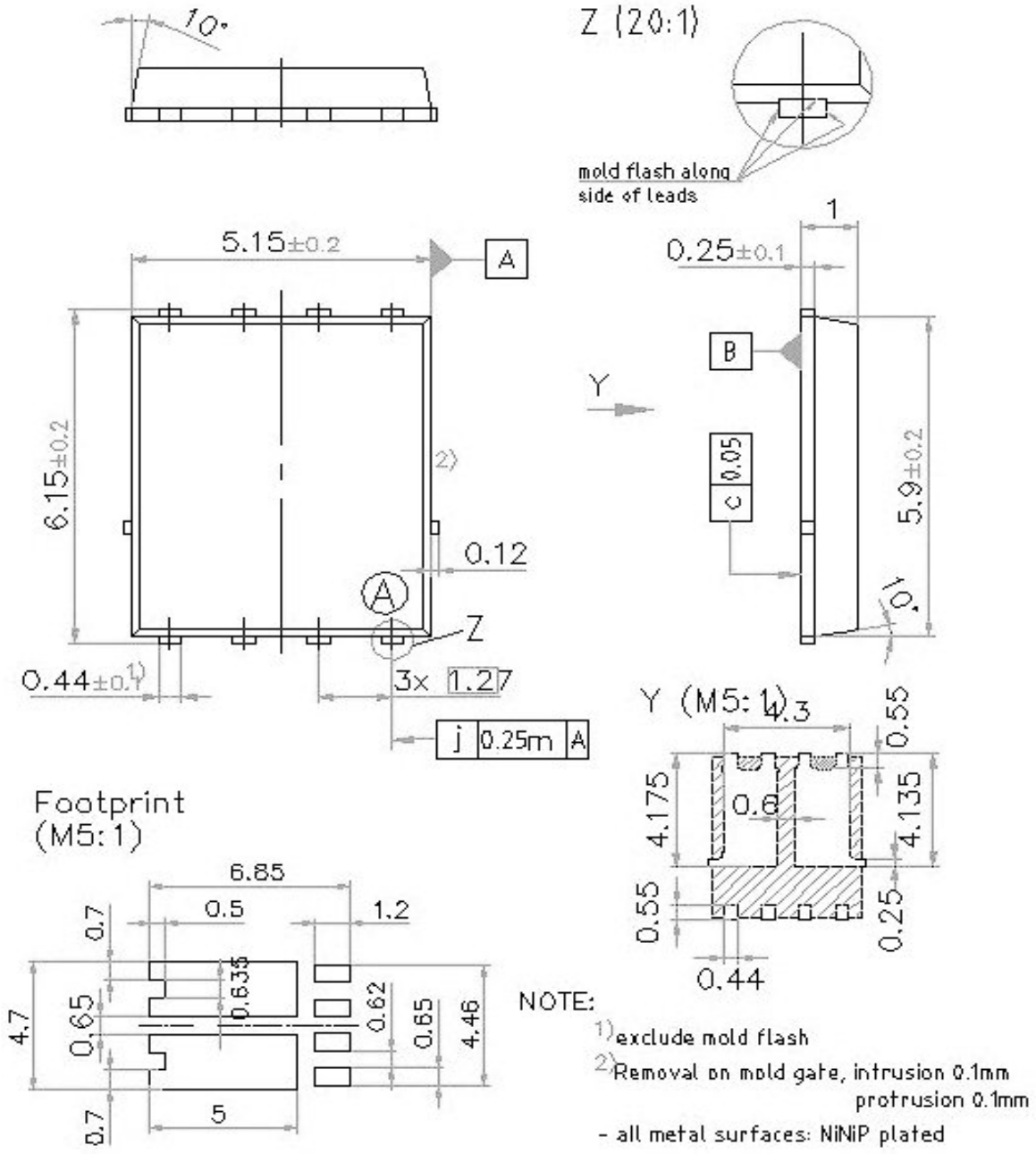
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



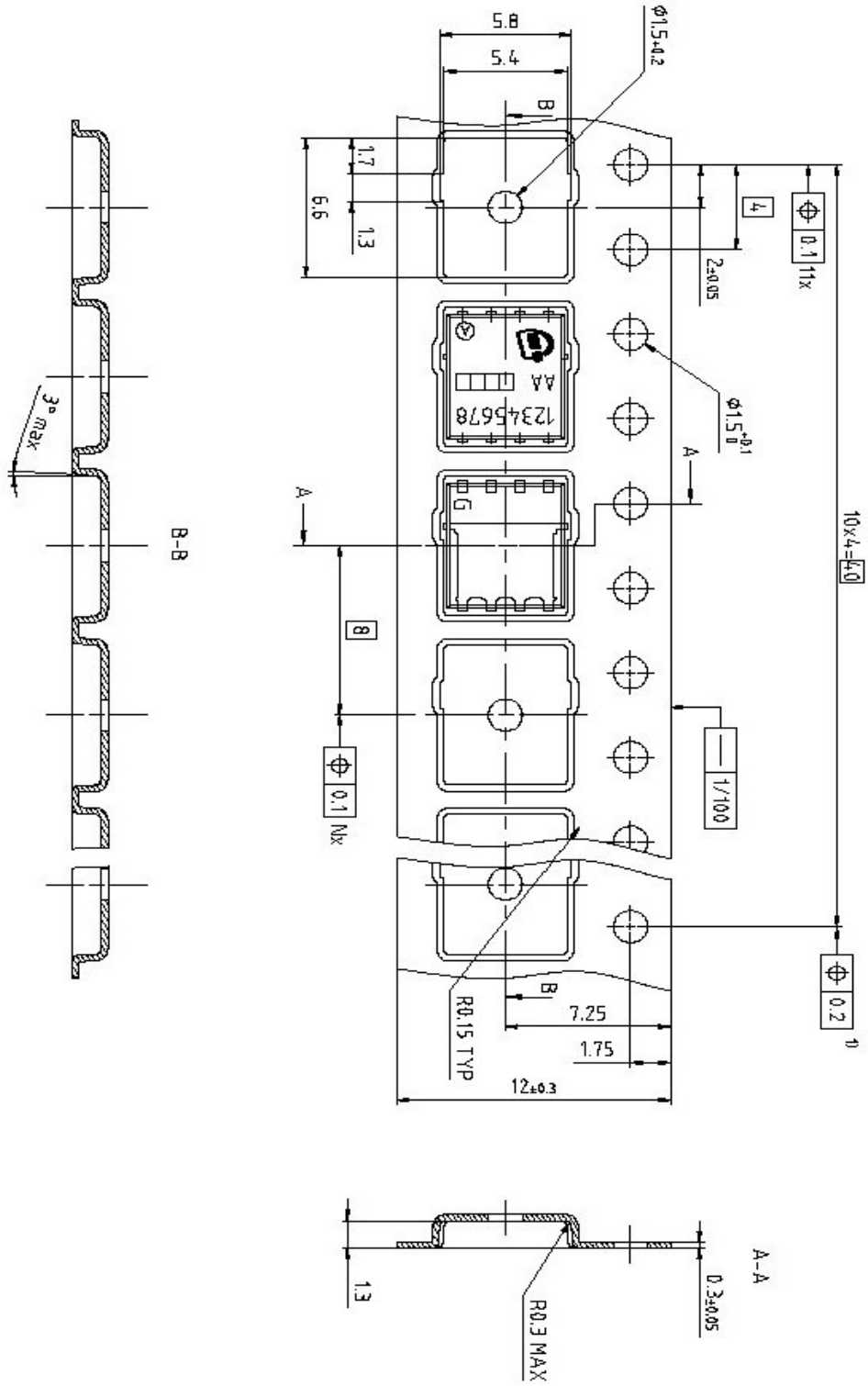
16 Gate charge waveforms



Package Outline and Footprint **PG-TDSON-8 dual**



Tape **PG-TDSON-8**



Dimensions in mm

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