MC100LVE210, MC100E210

Low Voltage Dual 1:4, 1:5 Differential Fanout Buffer

ECL/PECL Compatible

The MC100LVE210 is a low voltage, low skew dual differential ECL fanout buffer designed with clock distribution in mind. The device features two fanout buffers, a 1:4 and a 1:5 buffer, on a single chip. The device features fully differential clock paths to minimize both device and system skew. The dual buffer allows for the fanout of two signals through a single chip, thus reducing the skew between the two fundamental signals from a part–to–part skew down to an output–to–output skew. This capability reduces the skew by a factor of 4 as compared to using two LVE111's to accomplish the same task. The MC100LVE210 works from a –3.3V supply while the MC100E210 provides identical function and performance from a standard –4.5V 100E voltage supply.

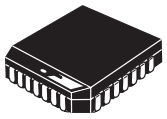
For applications which require a single–ended input, the V_{BB} reference voltage is supplied. For single–ended input applications the V_{BB} reference should be connected to the unused CLK input of a differential pair and bypassed to ground via a 0.01µf capacitor. The input signal is then driven into the selected CLK input.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are identically terminated, even if only one side is being used. In most applications all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

The MC100LVE210, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE210 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of V_{CC}–2.0V will need to be provided. For more information on using PECL, designers should refer to Application Note AN1406/D.

- Dual Differential Fanout Buffers
- 200ps Part–to–Part Skew
- 50ps Typical Output–to–Output Skew
- Low Voltage ECL/PECL Compatible
- 28–lead PLCC Packaging

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PLCC PACKAGE
FN SUFFIX
CASE 776

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



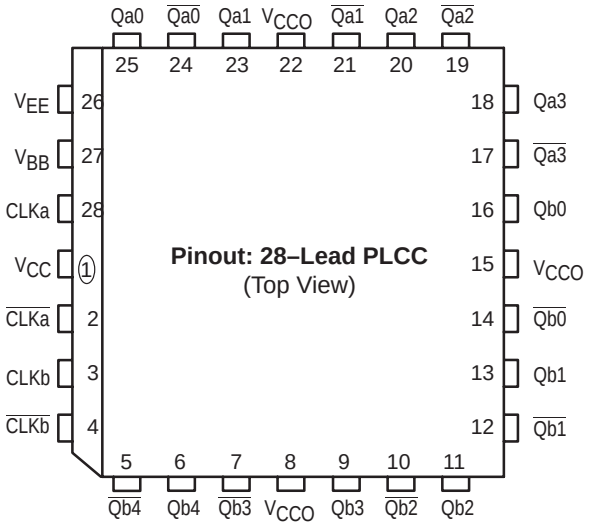
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVE210FN	PLCC	37 Units / Rail
MC100LVE210FNR2	PLCC	500 Tape & Reel
MC100E210FN	PLCC	37 Units / Rail
MC100E210FNR2	PLCC	500 Tape & Reel

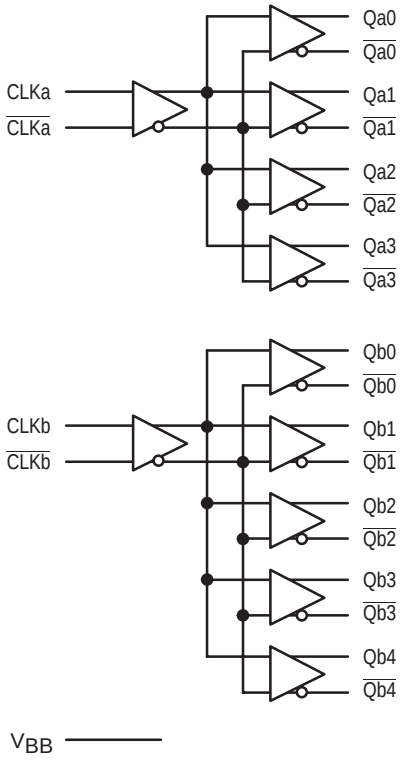
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PIN NAMES

Pins	Function
CLKa, CLKb	Differential Input Pairs
Qa0:3, Qb0:4	Differential Outputs
V_{BB}	V_{BB} Output

LOGIC SYMBOL



MC100LVE210
ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	–3.0		–3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current			55			55			55			65	mA

MC100LVE210
PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	2.215	2.295	2.42	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage[1]	1.47	1.605	1.745	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage[1]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage[1]	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		3.8	3.0		3.8	3.0		3.8	3.0		3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current			55			55			55			65	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

MC100LVE210
AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)	 475 400		 675 700	 475 400		 675 700	 500 450		 700 750	 500 450		 700 750	ps	 Note 1 Note 2
t_{skew}	Within–Device SkewQa Qb Qa Qa,Qb Qb Part–to–Part Skew (Diff)		 50 50	 75 75 200		 50 30	 75 50 200		 50 30	 75 50 200		 50 30	 75 50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE210 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

MC100E210
ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current			55			55			55			65	mA

MC100E210
PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V_{OL}	Output LOW Voltage[1]	3.170	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	3.19	3.295	3.38	V
V_{IH}	Input HIGH Voltage[1]	3.835		4.12	3.835		4.12	3.835		4.12	3.835		4.12	V
V_{IL}	Input LOW Voltage[1]	3.190		3.525	3.190		3.525	3.190		3.525	3.190		3.525	V
V_{BB}	Output Reference Voltage[1]	3.62		3.74	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{CC}	Power Supply Voltage	4.75		5.25	4.75		5.25	4.75		5.25	4.75		5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current			55			55			55			65	mA

1. These values are for V_{CC} = 5.0V. Level Specifications will vary 1:1 with V_{CC}.

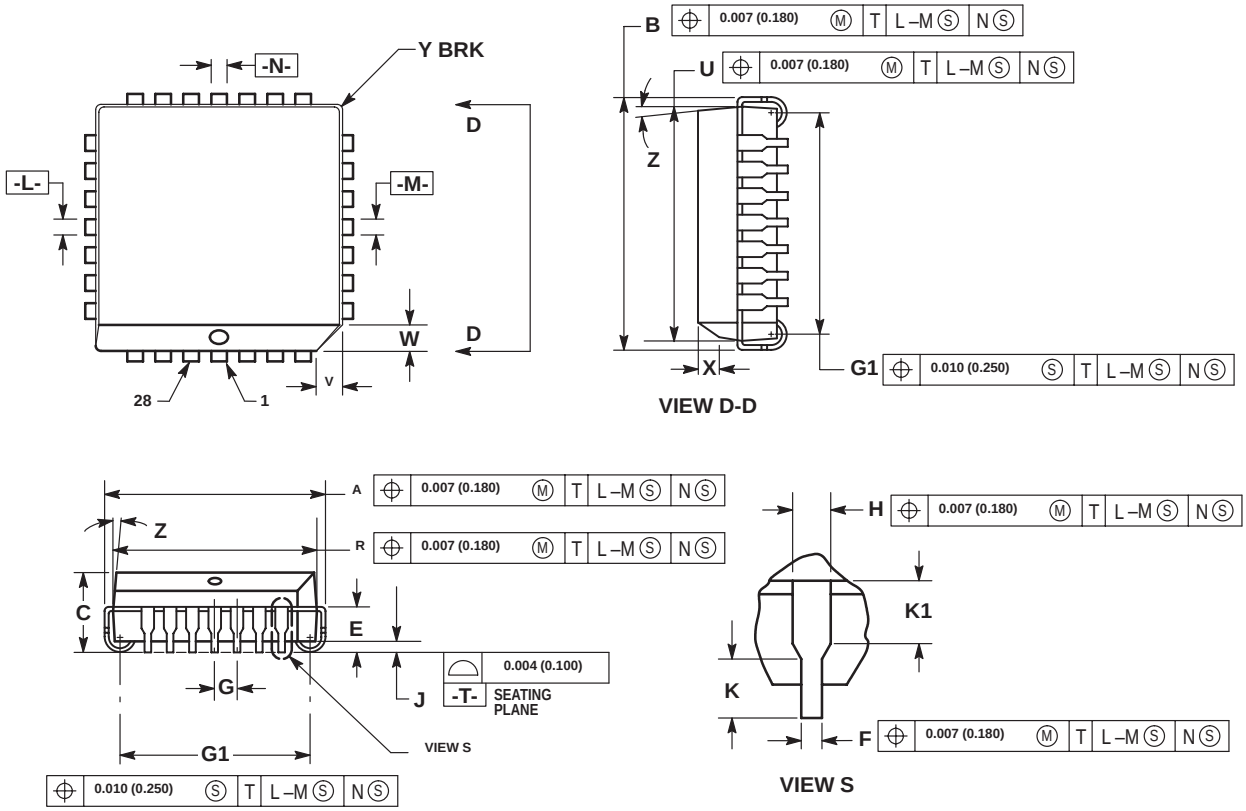
MC100E210
AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)	 475 400		 675 700	 475 400		 675 700	 500 450		 700 750	 500 450		 700 750	ps	 Note 1 Note 2
t_{skew}	Within–Device SkewQa Qb Qa Qa,Qb Qb Part–to–Part Skew (Diff)		 50 50	 75 75 200		 50 30	 75 50 200		 50 30	 75 50 200		 50 30	 75 50 200	ps	Note 3
V_{PP}	Minimum Input Swing	500			500			500			500			mV	Note 4
V_{CMR}	Common Mode Range	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V	Note 5
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E210 as a differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

PACKAGE DIMENSIONS

PLCC PACKAGE
FN SUFFIX
CASE 776–02
ISSUE D



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

Notes

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