LC²MOS Dual 12-Bit DACPORT

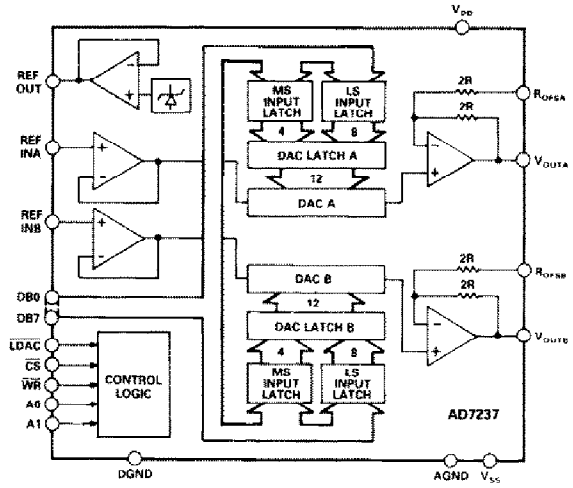
AD7237/AD7247

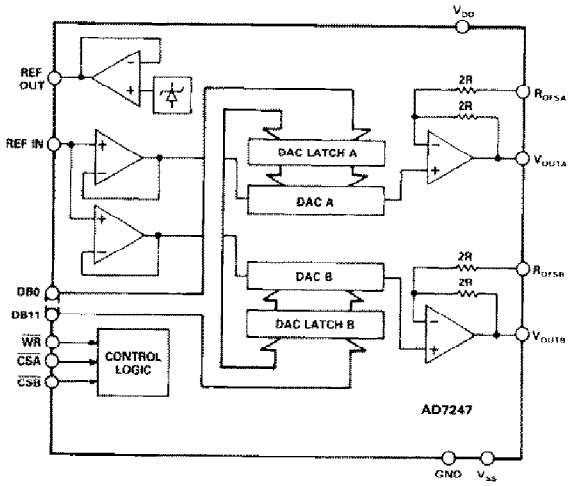
FEATURES

Complete Dual 12-Bit DAC Comprising
- **Two 12-Bit CMOS DACs**
- **On-Chip Voltage Reference**
- **Output Amplifiers**
- **Reference Buffer Amplifiers**

Parallel Loading Structure: AD7247
(8+4) Loading Structure: AD7237
Single or Dual Supply Operation
Low Power – 165 mW typ in Single Supply

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7237/AD7247 is a complete, dual, 12-bit, voltage output digital-to-analog converter with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7247 accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7237 has a double buffered interface structure and an 8-bit wide data bus with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7237 updates the DAC latches and analog outputs.

A REF OUT/REF IN function is provided which allows either the on-chip 5 V reference or an external reference to be used as a reference voltage for the part. For single supply operation, two output ranges of 0 to +5 V and 0 to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7237/AD7247 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3" wide plastic and hermetic dual-in-line package (DIP) and are also packaged in a 24-lead small outline (SOIC) package.

DACPORT is a trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The AD7237/AD7247 is a dual 12-bit DACPORT™ on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. Between them, the AD7237 and AD7247 offer a versatile interface arrangement to either 8-bit or 16-bit data bus structures.

REV. A

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AD7237/AD7247—SPECIFICATIONS (V_{DD} = +15 V[1] ±5%, V_{SS} = 0 V or −15 V[1] ±5%, AGND = DGND = 0 V [AD7237], GND = 0 V [AD7247], REF IN = +5 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A, S[2]	K, B, T	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±3	±3	LSB max	V_{SS} = 0 V or −15 V. DAC Latch Contents All 0s
Bipolar Zero Error[3]	±4	±4	LSB max	V_{SS} = −15 V. DAC Latch Contents 1000 0000 0000
Full-Scale Error[3, 4]	±5	±5	LSB max	
Full-Scale Mismatch[4]	±1	±1	LSB typ	
REFERENCE OUTPUT				
REF OUT				
J, K, A, B Versions	4.97/5.03	4.97/5.03	Vmin/Vmax	
S, T Versions	4.95/5.05	4.95/5.05	Vmin/Vmax	
Reference Temperature Coefficient	±25	±25	ppm/°C typ	
Reference Load Change				
(ΔREF OUT vs. ΔI)	−1	−1	mV max	Reference Load Current Change (0–100 μA)
REFERENCE INPUT				
Reference Input Range	4.95/5.05	4.95/5.05	V min/V max	5 V ± 1%
Input Current[5]	±5	±5	μA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN} (Data Inputs)	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
I_{INH} (Control Inputs)[6]	±10	±10	μA max	V_{IN} = V_{DD}
I_{INL} (Control Inputs)[6]	−150	−150	μA max	V_{IN} = 0 V
Input Capacitance[5]	16	16	pF max	
ANALOG OUTPUTS				
Output Range Resistors	15/30	15/30	kΩ min/kΩ max	
Output Voltage Ranges	+5, +10	+5, +10	V	V_{SS} = 0 V. Pin Strappable
Output Voltage Ranges	+5, +10, ±5	+5, +10, ±5	V	V_{SS} = −15 V. Pin Strappable
DC Output Impedance	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Full-Scale Change				V_{DD} = +15 V, V_{SS} = −15 V
J, K, A, B Versions	10	10	μs max	
S, T Versions	12	12	μs max	
Digital-to-Analog Glitch Impulse[3]	30	30	nV secs typ	
Digital Feedthrough[3]	10	10	nV secs typ	
Digital Crosstalk[3]	30	30	nV secs typ	
POWER REQUIREMENTS				
V_{DD}	+15	+15	V nom	±5% for Specified Performance Unless Otherwise Stated
V_{SS}	−15	−15	V nom	±5% for Specified Performance Unless Otherwise Stated
I_{DD}	15	15	mA max	Output Unloaded. Typically 11 mA
I_{SS} (Dual Supplies)	5	5	mA max	Output Unloaded. Typically 3 mA

NOTES

[1]Parts are functional at V_{DD} = +12 V ±10% and V_{SS} = 0 V or −12 V ±10%. See typical performance graphs.

[2]Temperature ranges are as follows: J, K Versions, −40°C to +85°C; A, B Versions, −40°C to +85°C; S, T Versions, −55°C to +125°C.

[3]See Terminology.

[4]Measured with respect to REF IN and includes unipolar/bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

[6]Control inputs are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$ for the AD7237 and $\overline{CSA}$, $\overline{CSB}$ and $\overline{WR}$ for the AD7247.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +15 V ±5%; V_{SS} = 0 V or −15 V ±5%, AGND = DGND = 0 V [AD7237], GND = 0 V [AD7247])

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	130	150	ns min	$\overline{WR}$ Pulse Width
t_4	128	150	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5[3]	10	15	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[4]	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_7[4]	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_8[4]	100	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 5 and 7.
[3]If 0 ns<t_2<10 ns, add t_2 to t_5. If t_2≥10 ns, add 10 ns to t_5.
[4]AD7237 only.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND (AD7247) . . . . . −0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237) . . . . . −0.3 V to +17 V
V_{DD} to V_{SS} . . . . . −0.3 V to +34 V
AGND to DGND (AD7237) . . . . . −0.3 V , V_{DD} +0.3 V
V_{OUTA}[1], V_{OUTB}[1] to AGND (GND)
. . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
REF OUT to AGND (GND) . . . . . 0 V to V_{DD}
REF IN to AGND (GND) . . . . . −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND (GND) . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . −40°C to +85°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTE
[1]Short-circuit current is typically 80mA. The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Option[2]
AD7237JN	−40°C to +85°C	±1 max	N-24
AD7237KN	−40°C to +85°C	±1/2 max	N-24
AD7237JR	−40°C to +85°C	±1 max	R-24
AD7237KR	−40°C to +85°C	±1/2 max	R-24
AD7237AQ	−40°C to +85°C	±1 max	Q-24
AD7237BQ	−40°C to +85°C	±1/2 max	Q-24
AD7237SQ	−55°C to +125°C	±1 max	Q-24
AD7237TQ	−55°C to +125°C	±1/2 max	Q-24
AD7247JN	−40°C to +85°C	±1 max	N-24
AD7247KN	−40°C to +85°C	±1/2 max	N-24
AD7247JR	−40°C to +85°C	±1 max	R-24
AD7247KR	−40°C to +85°C	±1/2 max	R-24
AD7247AQ	−40°C to +85°C	±1 max	Q-24
AD7247BQ	−40°C to +85°C	±1/2 max	Q-24
AD7247SQ	−55°C to +125°C	±1 max	Q-24
AD7247TQ	−55°C to +125°C	±1/2 max	Q-24

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline (SOIC).

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



AD7237 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

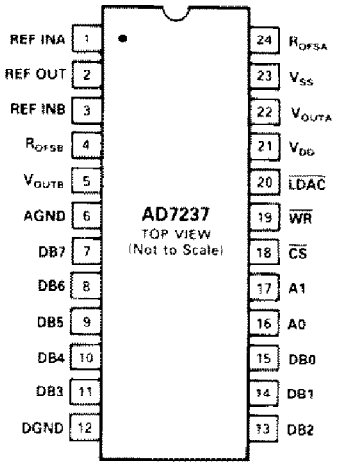
Pin	Mnemonic	Description
1	REF INA	Voltage Reference Input for DAC A. The reference voltage for DAC A is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
2	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF INA, REF INB.
3	REF INB	Voltage Reference Input for DAC B. The reference voltage for DAC B is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
4	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REF INB for the ±5 V range.
5	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
6	AGND	Analog Ground. Ground reference for DACs, reference and output buffer amplifiers.
7	DB7	Data Bit 7.
8–10	DB6–DB4	Data Bit 6 to Data Bit 4.
11	DB3	Data Bit 3/Data Bit 11 (MSB).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	DB2	Data Bit 2/Data Bit 10.
14	DB1	Data Bit 1/Data Bit 9.
15	DB0	Data Bit 0 (LSB)/Data Bit 8.
16	A0	Address Input. Least significant address input for input latches. A0 and A1 select which of the four input latches data is written to (see Table II).
17	A1	Address Input. Most significant address input for input latches.
18	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
20	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latches from the respective input latches on the falling edge of this signal.
21	V_{DD}	Positive Supply, +15 V.
22	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
23	V_{SS}	Negative Supply, −15 V.
24	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REF INA for the ±5 V range.

AD7247 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF IN.
2	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
3	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to + 10 V and ± 5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
4	DB11	Data Bit 11 (MSB).
5	DB10	Data Bit 10.
6	GND	Ground. Ground reference for all on-chip circuitry.
7–15	DB9–DB1	Data Bit 9 to Data Bit 1.
16	DB0	Data Bit 0 (LSB).
17	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is active.
18	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
20	V_{DD}	Positive Supply, +15 V.
21	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
22	V_{SS}	Negative Supply, −15 V.
23	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
24	REF IN	Voltage Reference Input. The common reference voltage for both DACs is applied to this pin. It is internally buffered before being applied to both DACs. The nominal reference voltage for correct operation of the AD7247 is 5 V.

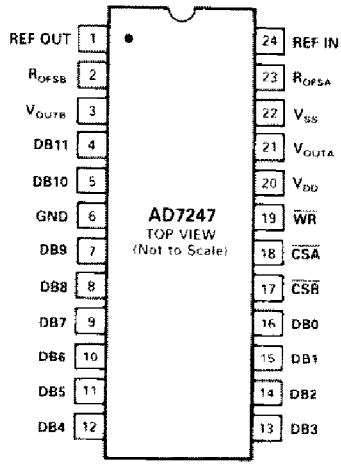
AD7237 PIN CONFIGURATIONS

DIP and SOIC



AD7247 PIN CONFIGURATIONS

DIP and SOIC



TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

SINGLE SUPPLY LINEARITY AND GAIN ERROR

The output amplifiers of the AD7237/AD7247 can have true negative offsets even when the part is operated from a single +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output offset voltage is negative, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1. This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

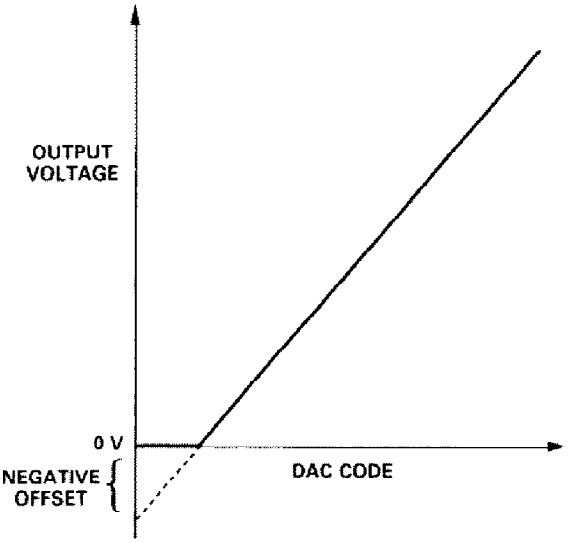


Figure 1. Effect of Negative Offset (Single Supply)

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7237/AD7247 in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset, i.e., linearity is measured between Codes 3 and 4095.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the measured output voltage from V_{OUTA} or V_{OUTB} with all zeros loaded into the DAC latches when the DACs are configured for unipolar output. It is a combination of the offset errors of the DAC and output amplifier.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the voltage measured at V_{OUTA} or V_{OUTB} when the DAC is connected in the bipolar mode and loaded with code 2048. It is due to a combination of offset errors in the DAC, amplifier offset and mismatch in the application resistors around the amplifier.

FULL-SCALE ERROR

Full-Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse injected for the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

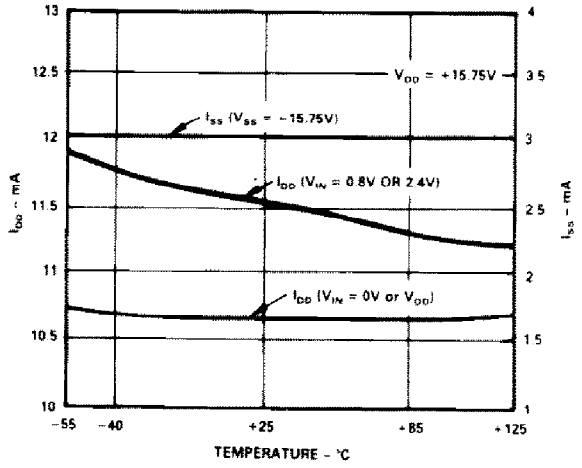
For the AD7237 it is measured with $\overline{LDAC}$ held high. For the AD7247 it is measured with $\overline{CSA}$ and $\overline{CSB}$ held high.

DIGITAL CROSSTALK

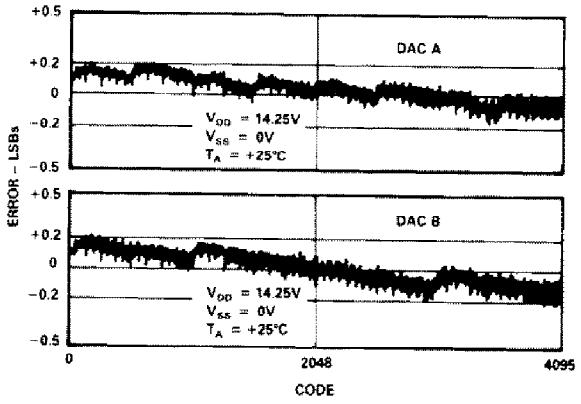
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code to the DAC latch of the other converter. It is specified in nV secs.

DIGITAL-TO-ANALOG GLITCH IMPULSE

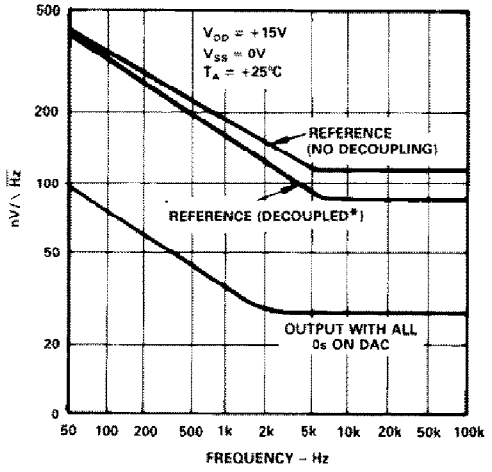
This is the voltage spike that appears at the output of the DAC when the digital code changes before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000).



Power Supply Current vs.Temperature

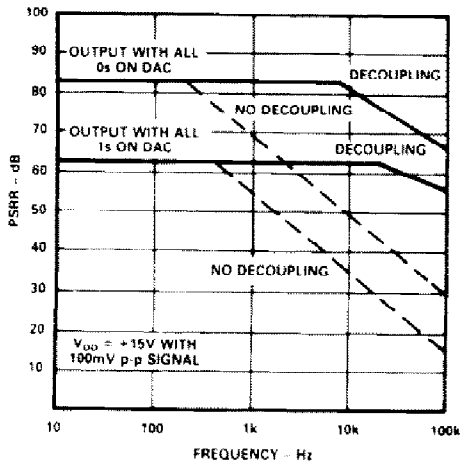


DAC-to-DAC Linearity Matching



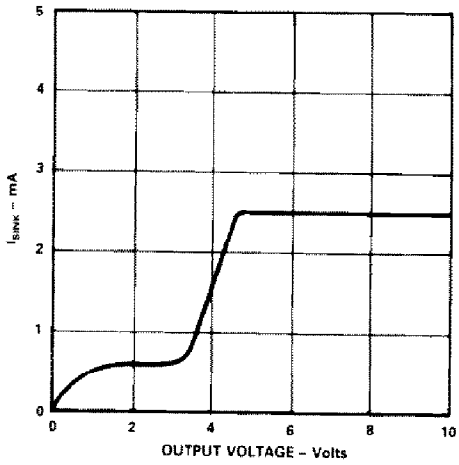
*REFERENCE DECOUPLING COMPONENTS ARE A 200Ω RESISTOR IN SERIES WITH A PARALLEL COMBINATION OF 10μF AND 0.1μF TO GND.

Noise Spectral Density vs. Frequency

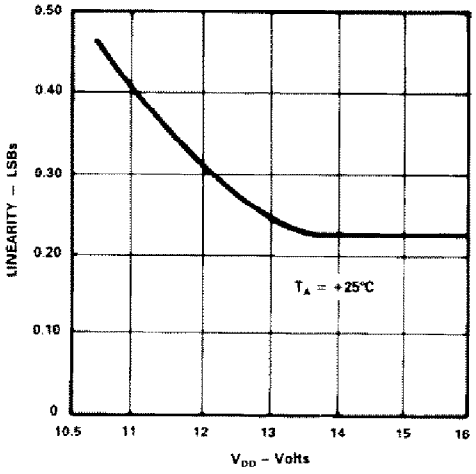


*POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF AND 0.1μF

Power Supply Rejection Ratio vs. Frequency



Single Supply Sink Current vs. Output Voltage



Linearity vs. Power Supply Voltage

CIRCUIT INFORMATION

D/A Section

The AD7237/AD7247 contains two 12-bit voltage-mode D/A converters consisting of highly stable thin film resistors and high speed NMOS single-pole, double-throw switches. The output voltage from the converters has the same polarity as the reference voltage, REF IN, allowing single supply operation. The simplified circuit diagram for one of the D/A converters is shown in Figure 2.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converters. The D/A converters are configured and scaled for a 5 V reference and the device is tested with 5 V applied to REF IN.

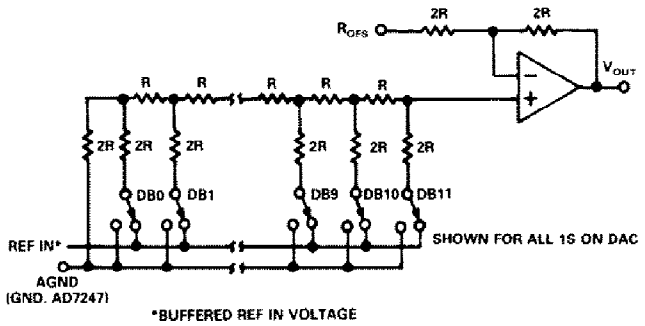


Figure 2. D/A Simplified Circuit Diagram

Internal Reference

The AD7237/AD7247 has an on-chip temperature compensated buried Zener reference (see Figure 3) which is factory trimmed to 5 V ±30 mV (±50 mV for S, T Versions). The reference voltage is provided at the REF OUT pin. This reference can be used to provide the reference voltage for the D/A converter (by connecting the REF OUT pin to the REF IN pin) and the offset voltage for bipolar outputs (by connecting REF OUT to R_{OFS}).

The reference voltage can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled to AGND (GND) with a 200 Ω resistor in series with parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

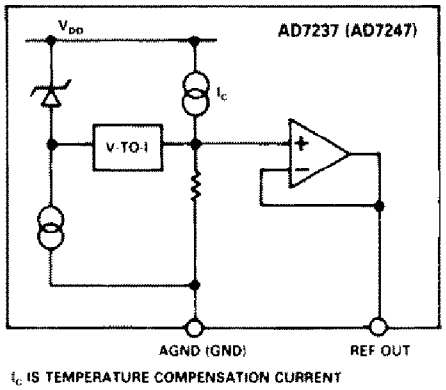


Figure 3. Internal Reference

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7237/AD7247 reference input. References such as the AD586 5 V reference provide the ideal external reference source for the AD7237/AD7247 (see Figure 9).

Op Amp Section

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The R_{OFS} input allows different output voltage ranges to be selected. The buffer amplifier is capable of developing +10 V across a 2 kΩ load to GND. The output amplifier can be operated from a single +15 V supply by tying V_{SS}=0 V. The amplifier can also be operated from dual supplies (±15 V) to allow a bipolar output range of −5 V to +5 V. The advantages of having dual supplies for the unipolar output ranges are faster settling time to voltages near 0 V, full sink capability of 2.5 mA maintained over the entire output range and the elimination of the effects of negative offsets on the transfer characteristic (outlined previously). A plot of the single supply output sink capability of the amplifier is shown in the Typical Performance Graphs section.

INTERFACE LOGIC INFORMATION - AD7247

Table I shows the truth table for AD7247 operation. The part contains a single, parallel 12-bit latch for each DAC. It can be treated as two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control the loading of data to the DAC A latch while $\overline{CSB}$ and $\overline{WR}$ control the loading of the DAC B latch. If $\overline{CSA}$ and $\overline{CSB}$ are both low, with $\overline{WR}$ low, the same data will be written to both DAC latches. All control signals are level triggered and therefore either or both latches can be made transparent. Input data is latched to the respective latch on the rising edge of $\overline{WR}$. Figure 4 shows the input control logic for the AD7247, while the write cycle timing diagram for the part is shown in Figure 5.

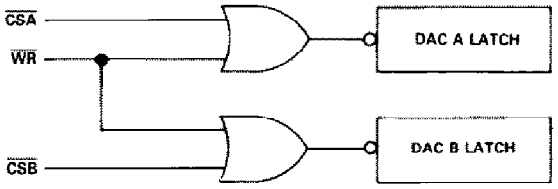


Figure 4. AD7247 Input Control Logic

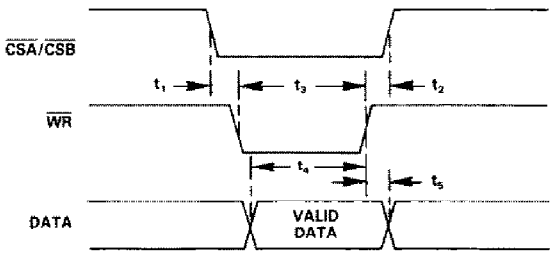


Figure 5. AD7247 Write Cycle Timing Diagram

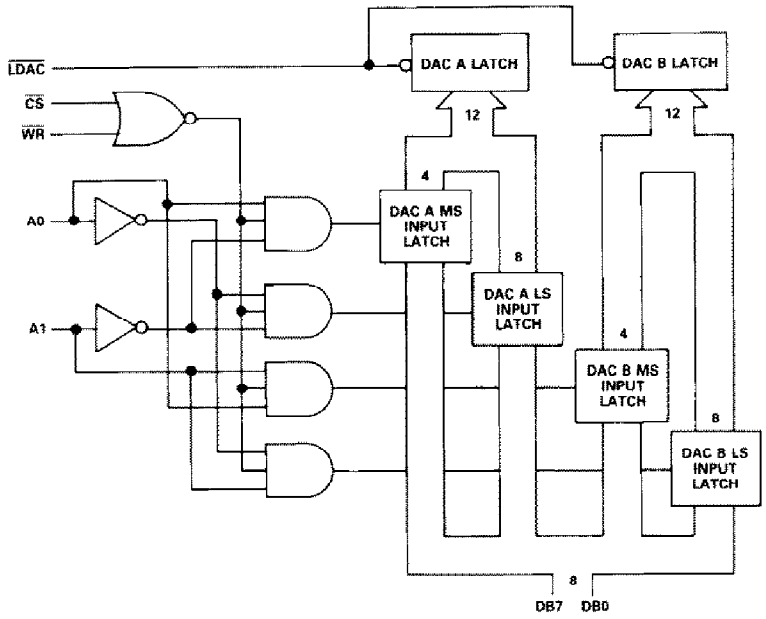


Figure 6. AD7237 Input Control Logic

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	0	DACA Latch Transparent
1	0	0	DACB Latch Transparent
0	0	0	Both DAC Latches Transparent

X = Don't Care

Table I. AD7247 Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DACA and DACB DAC Latches Updated Simultaneously from the Respective Input Latches

X = Don't Care.

Table II. AD7237 Truth Table

INTERFACE LOGIC INFORMATION – AD7237

The input loading structure on the AD7237 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches per DAC – an input latch and a DAC latch. Each input latch is further subdivided into a least significant 8-bit latch and a most significant 4-bit latch. Only the data held in the DAC latches determines the outputs from the part. The input control logic for the AD7237 is shown in Figure 6, while the write cycle timing diagram is shown in Figure 7.

$\overline{CS}$, $\overline{WR}$, A0 and A1 control the loading of data to the input latches. The eight data inputs accept right-justified data. Data can be loaded to the input latches in any sequence. Provided that $\overline{LDAC}$ is held high, there is no analog output change as a result of loading data to the input latches. Address lines A0 and A1 determine which latch data is loaded to when $\overline{CS}$ and $\overline{WR}$ are low. The selection of the input latches is shown in the truth table for AD7237 operation in Table II.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latches to the DAC latches. Both DAC latches, and hence both analog outputs, are updated at the same time. The $\overline{LDAC}$ signal is level triggered and data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7237s.

However, care must be taken while exercising $\overline{LDAC}$ during a write cycle. If an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, there is a possibility of invalid data being latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ return high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulse width.

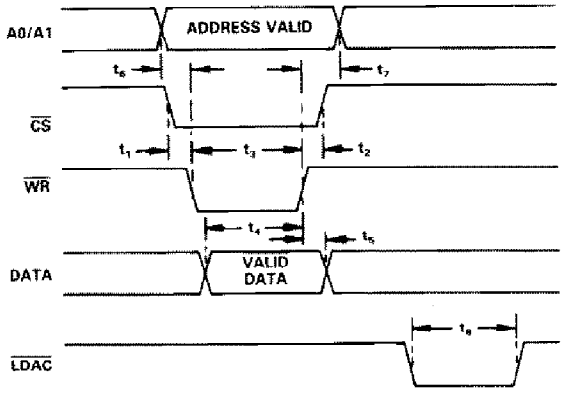


Figure 7. AD7237 Write Cycle Timing Diagram

APPLYING THE AD7237/AD7247

The internal scaling resistors provided on the AD7237/AD7247 allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to +5 V or 0 V to +10 V and a bipolar output range of ±5 V. Connections for the various ranges are outlined below. Since each DAC has its own R_{OFS} input the two DACs on each part can be set up for different output ranges.

Unipolar (0 V to +10 V) Configuration

The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the output offset resistor, R_{OFSA}, or R_{OFSB}, to AGND (GND for AD7247). In this configuration, the AD7237/AD7247 can be operated from single or dual supplies. Figure 8 shows the connection diagram for unipolar operation for DAC A of the AD7237, while the table for output voltage versus digital code in the DAC latch is shown in Table III. Similar connections apply to the AD7247.

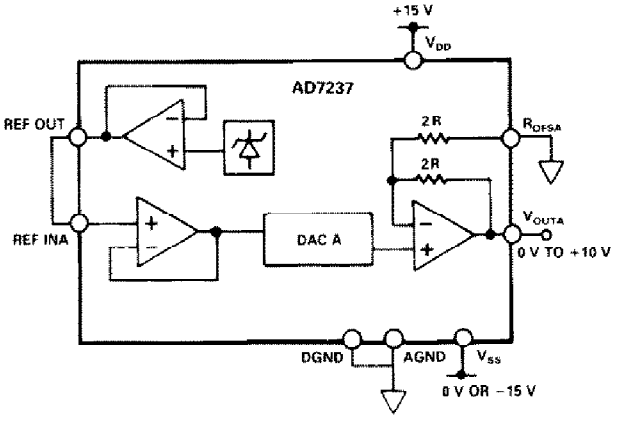


Figure 8. Unipolar (0 to +10 V) Configuration

Unipolar (0 V to +5 V) Configuration

The 0 V to +5 V output voltage range is achieved by tying R_{OFSA} or R_{OFSB} to V_{OUTA} or V_{OUTB}. Once again, the AD7237/AD7247 can be operated single supply or from dual supplies. The table for output voltage versus digital code is as in Table III, with 2 · REF IN replaced by REF IN. Note, for this range, 1 LSB = REF IN · (2^{-12}) = (REF IN/4096).

Bipolar Configuration

The bipolar configuration for the AD7237/AD7247, which gives an output range of −5 V to +5 V, is achieved by connecting R_{OFSA}, or R_{OFSB}, to REF IN. The AD7237/AD7247 must be operated from dual supplies to achieve this output voltage range. Figure 9 shows the connection diagram for bipolar operation for DAC A of the AD7247. An AD586 provides the reference voltage for the DAC but this could be provided by the on-chip reference by connecting REF OUT to REF IN. The code table for bipolar operation is shown in Table IV. Similar connections apply for the AD7237.

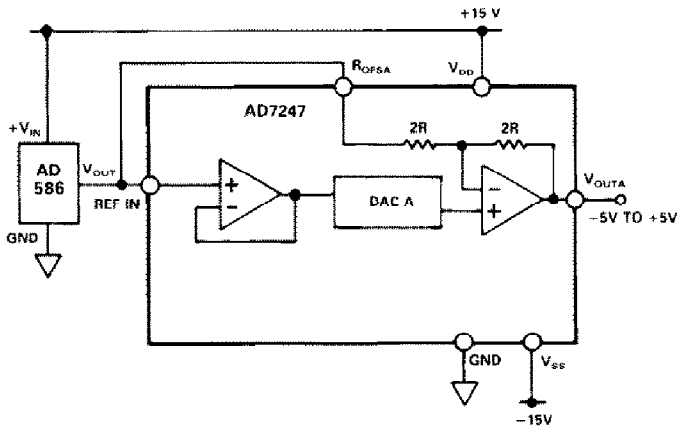


Figure 9. Bipolar Configuration

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+2 · REF IN · (4095/4096)
1000 0000 0001	+2 · REF IN · (2049/4096)
1000 0000 0000	+2 · REF IN · (2048/4096) = +REF IN
0111 1111 1111	+2 · REF IN · (2047/4096)
0000 0000 0001	+2 · REF IN · (1/4096)
0000 0000 0000	0 V

Note: 1 LSB = REF IN/2048.

Table III. Unipolar Code Table (0 to +10 V Range)

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+REF IN · (2047/2048)
1000 0000 0001	+REF IN · (1/2048)
1000 0000 0000	0 V
0111 1111 1111	−REF IN · (1/2048)
0000 0000 0001	−REF IN · (2047/2048)
0000 0000 0000	−REF IN · (2048/2048) = −REF IN

Note: 1 LSB = REF IN/2048.

Table IV. Bipolar Code Table

MICROPROCESSOR INTERFACING – AD7247

Figures 10 to 12 show interfaces between the AD7247 and the ADSP-2101 DSP processor and the 8086 and 68000 16-bit microprocessors. In all three interfaces, the AD7247 is memory-mapped with a separate memory address for each DAC.

AD7247 – ADSP-2101 Interface

Figure 10 shows an interface between the AD7247 and the ADSP-2101. The 12-bit word is written to the selected DAC latch of the AD7247 in a single instruction, and the analog output responds immediately. Depending on the clock frequency of the ADSP-2101, either one or two wait states will have to be programmed into the data memory wait state control register of the ADSP-2101.

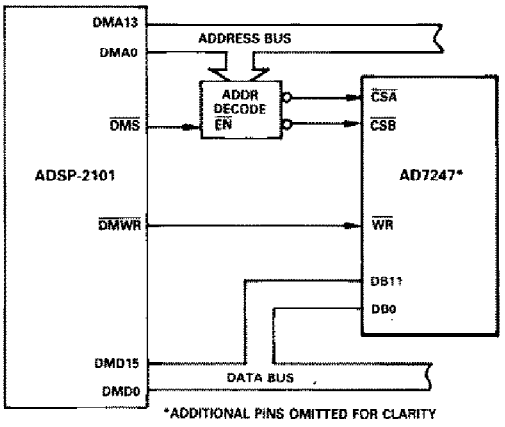


Figure 10. AD7247 to ADSP-2101 Interface

AD7247 – 8086 Interface

Figure 11 shows an interface between the AD7247 and the 8086 microprocessor. The 12-bit word is written to the selected DAC latch of the AD7247 in a single MOV instruction, and the analog output responds immediately.

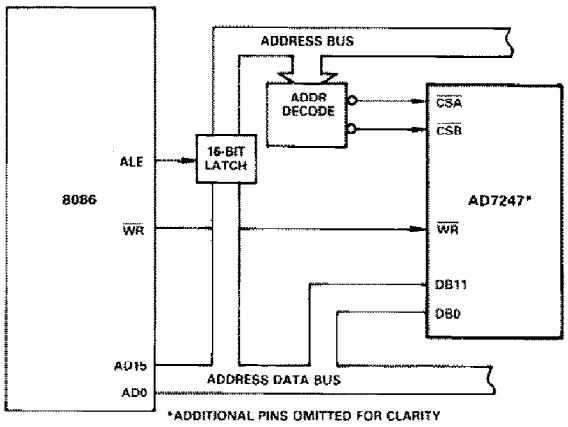


Figure 11. AD7247 to 8086 Interface

AD7247 – MC68000 Interface

Interfacing between the AD7247 and the MC68000 microprocessor is achieved using the circuit of Figure 12. Once again, the 12-bit word is written to the selected DAC latch of the AD7247 in a single MOVE instruction. $\overline{CSA}$ and $\overline{CSB}$ have to be AND-gated to provide a $\overline{DTACK}$ signal for the MC68000 when either DAC latch is selected.

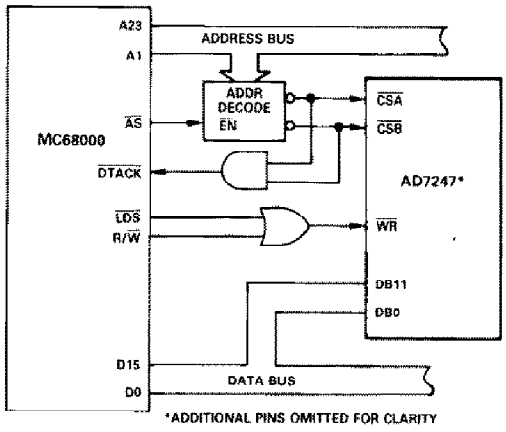


Figure 12. AD7247 to MC68000 Interface

MICROPROCESSOR INTERFACING – AD7237

Figures 13 to 15 show the AD7237 configured for interfacing to microprocessors with 8-bit databus systems. In all cases, data is right-justified, and the AD7237 is memory-mapped with the two lowest address lines of the microprocessor address bus driving the A0 and A1 inputs of the converter.

AD7237 – 8085A/8088 Interface

Figure 13 shows the connection diagram for interfacing the AD7237 to both the 8085A and the 8088. This scheme is also suited to the Z80 microprocessor, but the Z80 address/databus does not have to be demultiplexed. The AD7237 requires five separate memory addresses, one for the each MS latch and one for each LS latch and one for the common $\overline{LDAC}$ input. Data is written to the respective input latch in two write operations.

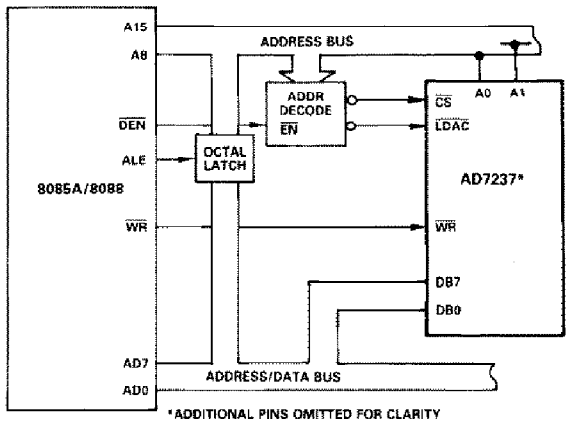


Figure 13. AD7237 to 8085A/8088 Interface

Either high byte or low byte data can be written first to the input latch. A write to the AD7237 DAC Latch address transfers the data from the input latches to the respective DAC latches and updates both analog outputs. Alternatively, the $\overline{LDAC}$ input can be asynchronous or can be common to a number of AD7237s for simultaneous updating of a number of voltage channels.

AD7237 – 68008 Interface

An interface between the AD7237 and the 68008 is shown in Figure 14. In the diagram shown, the $\overline{LDAC}$ is derived from an asynchronous $\overline{LDAC}$ signal, but this can be derived from the address decoder as in the previous interface diagram.

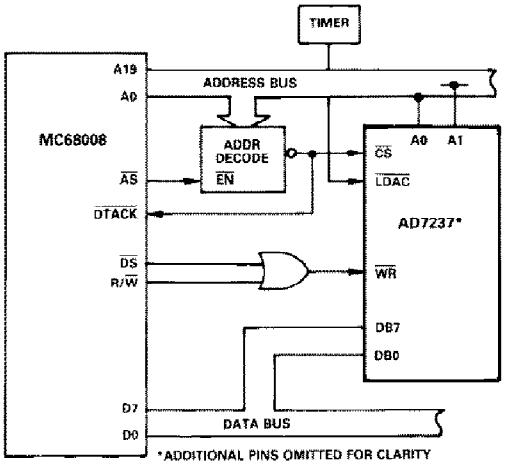


Figure 14. AD7237 to 68008 Interface

AD7237 – 6502/6809 Interface

Figure 15 shows an interface between the AD7237 and the 6502 or 6809 microprocessor. The procedure for writing data to the AD7237 is as outlined for the 8085A/8088 interface. For the 6502 microprocessor, the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

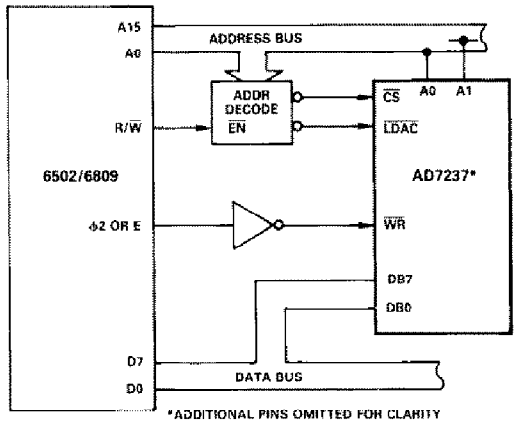
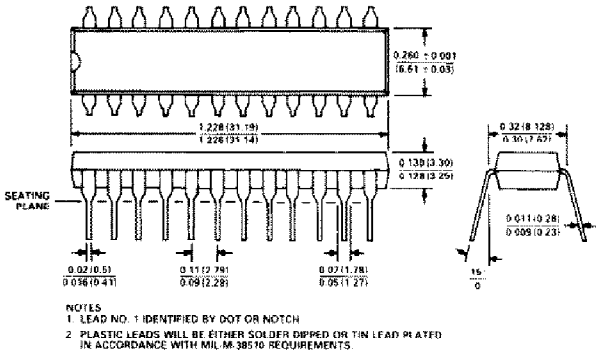


Figure 15. AD7237 to 6502/6809 Interface

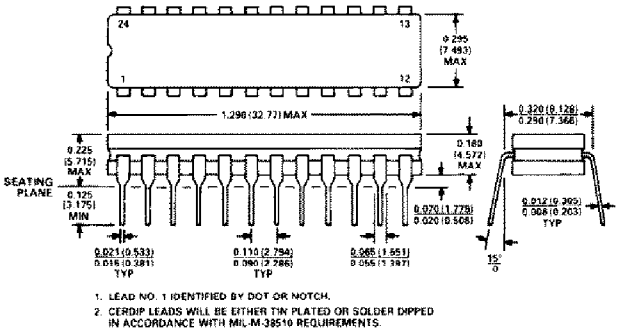
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

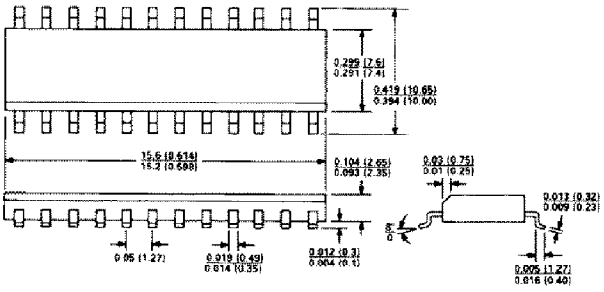
Plastic DIP (N-24)



Cerdip (Q-24)



SOIC (R-24)



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