

RFD16N06, RFD16N06SM

**16A, 60V, 0.047 Ohm,
N-Channel Power MOSFET**

September 1998

Features

- 16A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- *Temperature Compensating* PSpice Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFD16N06	TO-251AA	F16N06
RFD16N06SM	TO-252AA	F16N06

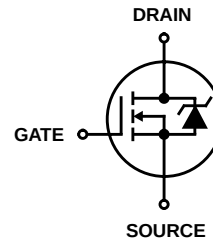
NOTE: When ordering, use the entire part number. Add suffix 9A to obtain the TO-252AA variant in tape and reel, i.e., RFD16N06SM9A.

Description

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

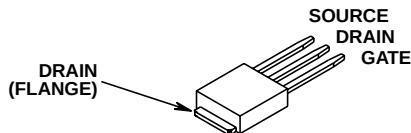
Formerly developmental type TA09771.

Symbol

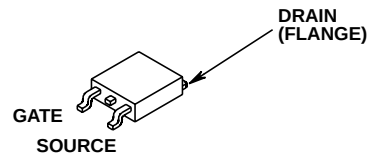


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



RFD16N06, RFD16N06SM

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$

	RFD16N06, RFD16N06SM	UNITS
Drain to Source Voltage (Note 1)	V_{DS} 60	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR} 60	V
Continuous Drain Current	I_D 16	A
Pulsed Drain Current (Note 3)	I_{DM} Refer to Peak Current Curve	A
Gate to Source Voltage	V_{GS} ± 20	V
Pulsed Avalanche Rating	E_{AS} Refer to UIS Curve	W
Power Dissipation	P_D 72	$W/^{\circ}\text{C}$
Linear Derating Factor	0.48	$W/^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering		$^{\circ}\text{C}$
Leads at 0.063in (1.6mm) from Case for 10s	T_L 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V		60	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V		-	-	1	μA
		V _{DS} = 0.8 x Rated BV _{DSS} , T _C = 150°C		-	-	25	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	I _D = 16A, V _{GS} = 10V (Figure 9)		-	-	0.047	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D ≈ 8A, R _L = 3.75Ω, V _{GS} = 10V, R _G = 25Ω (Figures 13, 16, 17)		-	-	65	ns
Turn-On Delay Time	t _{d(ON)}			-	14	-	ns
Rise Time	t _r			-	30	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	55	-	ns
Fall Time	t _f			-	30	-	ns
Turn-Off Time	t _{OFF}			-	-	125	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 48V, I _D = 16A, R _L = 3Ω, I _{G(REF)} = 0.8mA (Figures 18, 19)	-	-	80	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	-	45	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	-	2.2	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	900	-	pF
Output Capacitance	C _{OSS}			-	325	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	100	-	pF
Thermal Resistance Junction to Case	R _{θJC}			-	-	2.083	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-251 and TO-252		-	-	100	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 16\text{A}$	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 16\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

NOTES:

2. Pulse test: pulse width $\leq 300\text{ms}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves

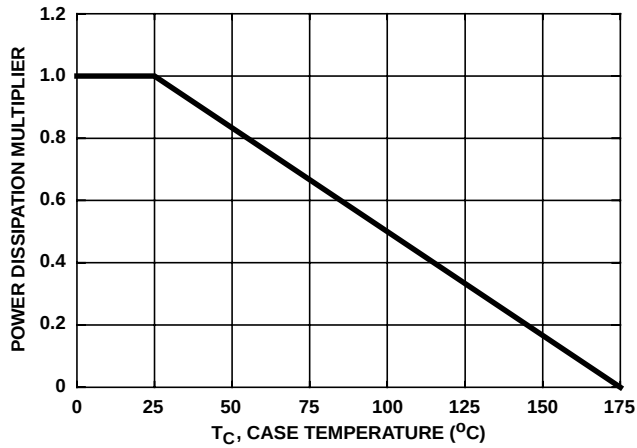


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

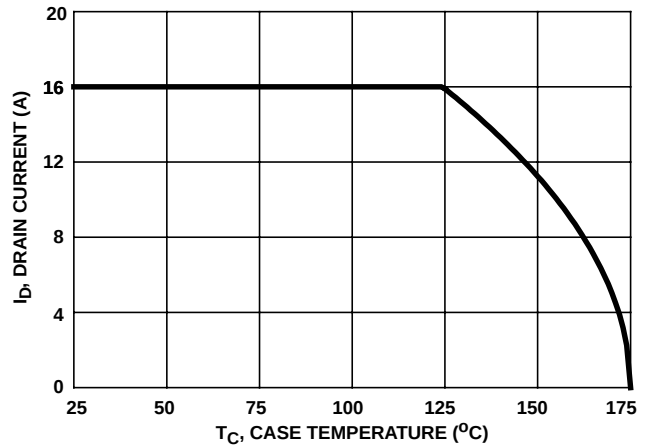


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

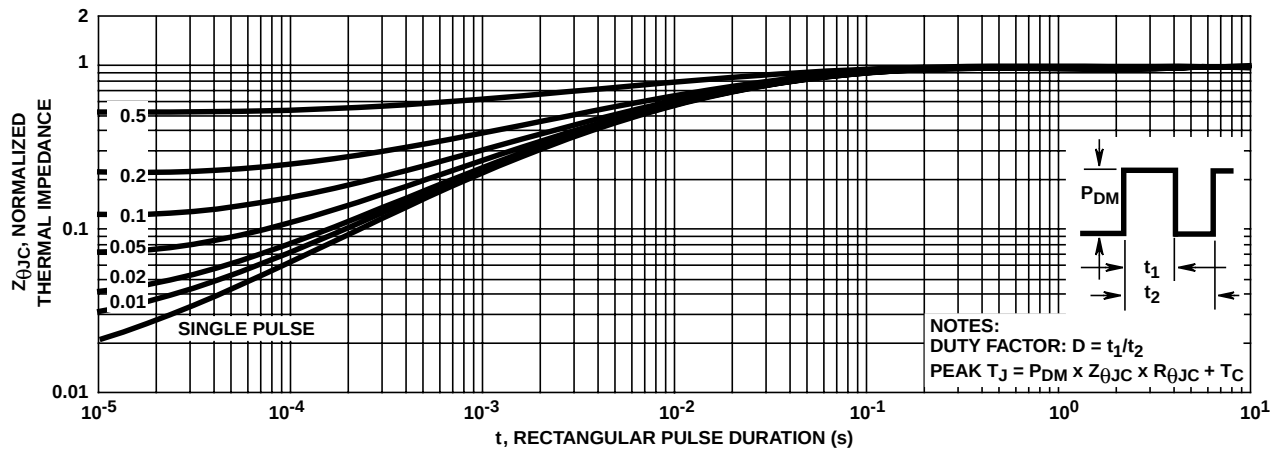


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

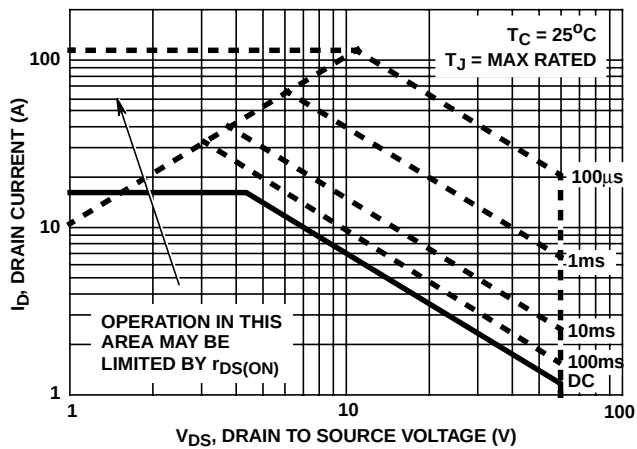


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

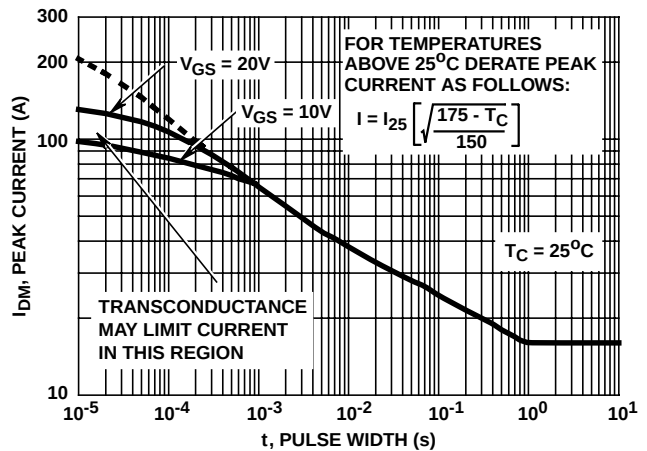
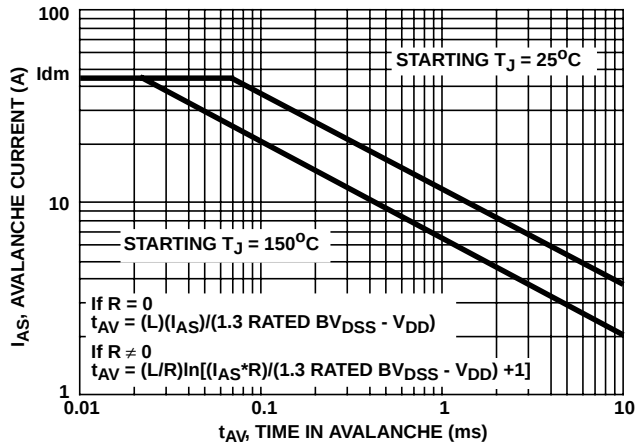


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

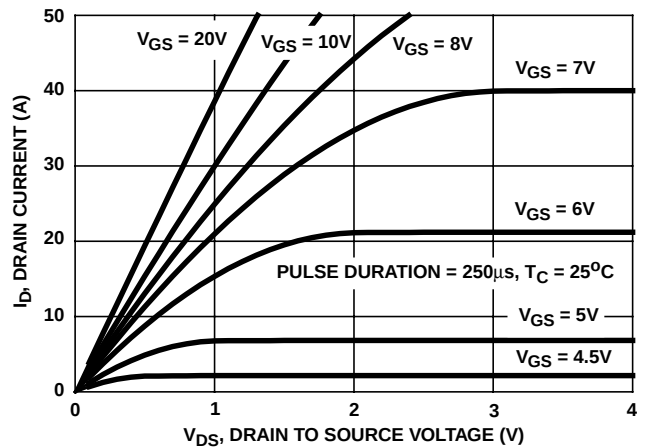


FIGURE 7. SATURATION CHARACTERISTICS

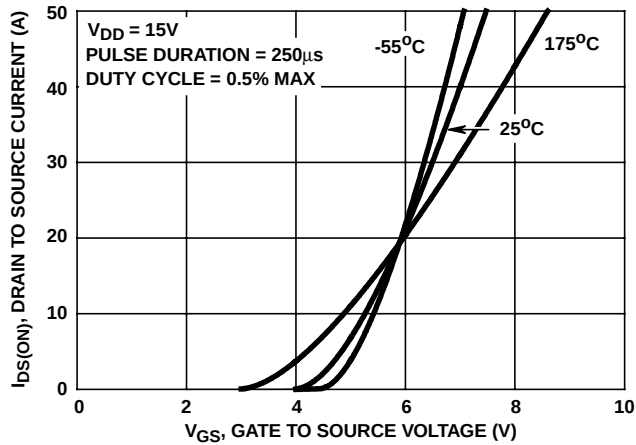


FIGURE 8. TRANSFER CHARACTERISTICS

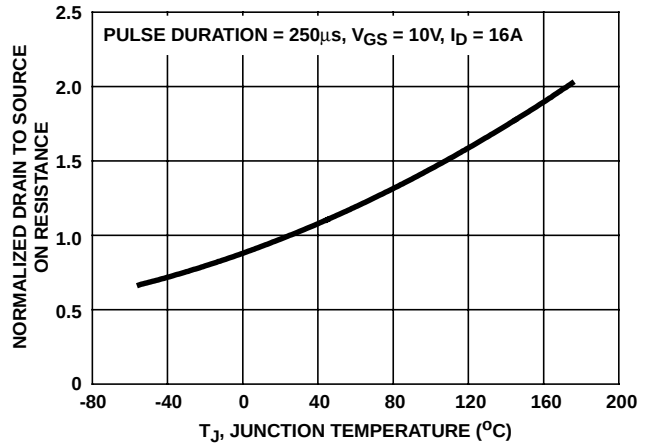


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

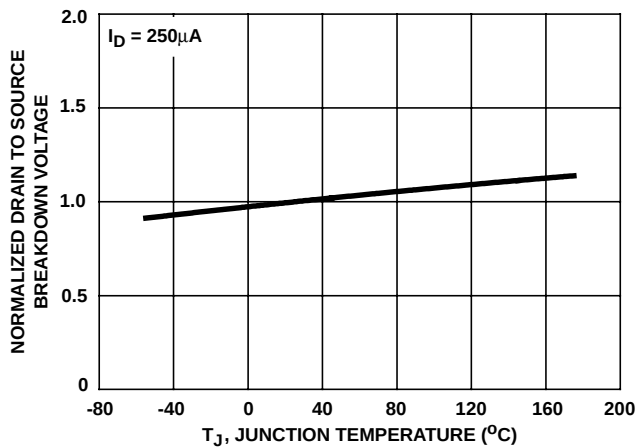


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

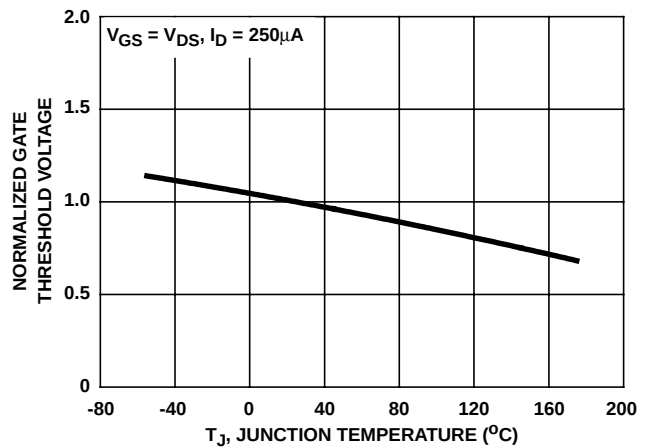


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

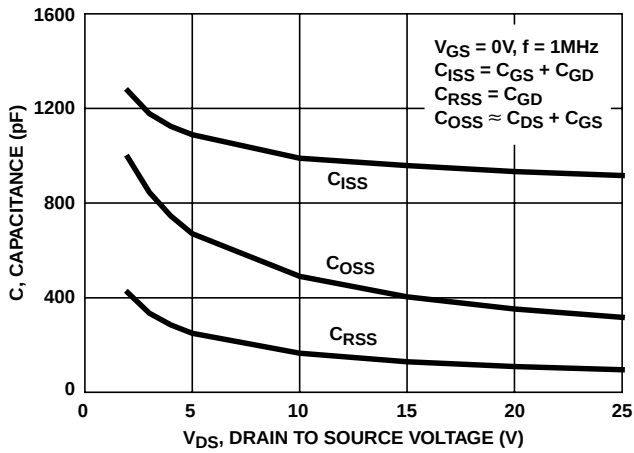
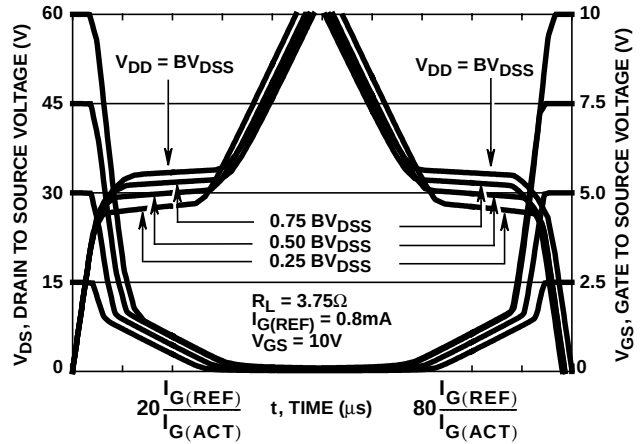


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

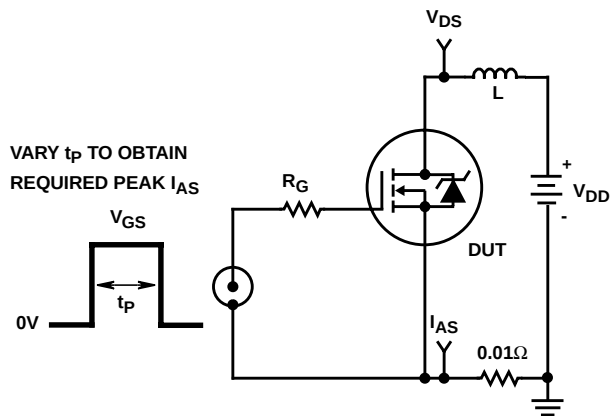


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

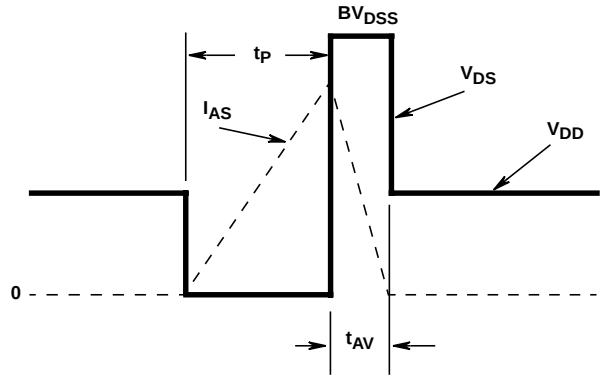


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

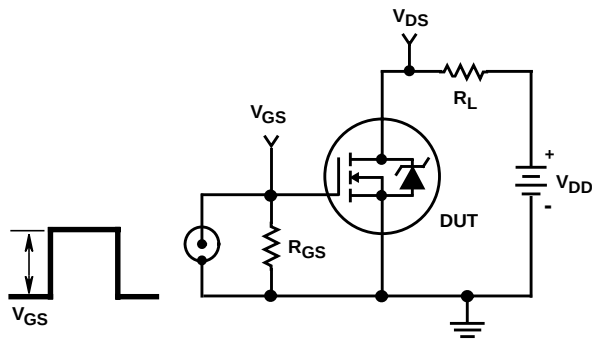


FIGURE 16. SWITCHING TIME TEST CIRCUIT

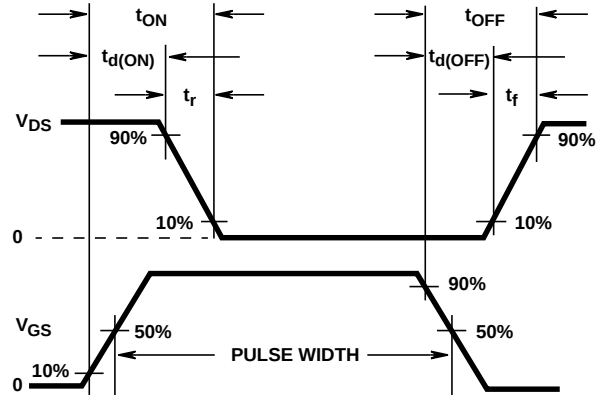


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

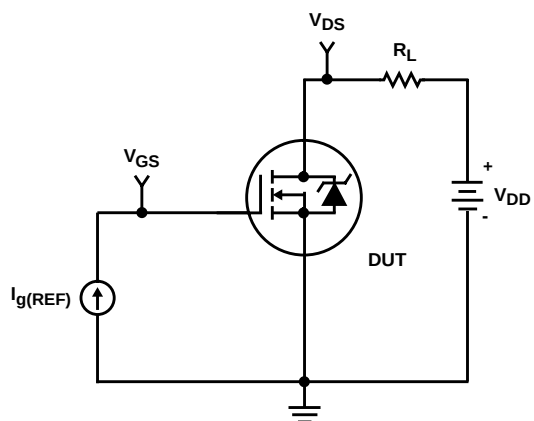


FIGURE 18. GATE CHARGE TEST CIRCUIT

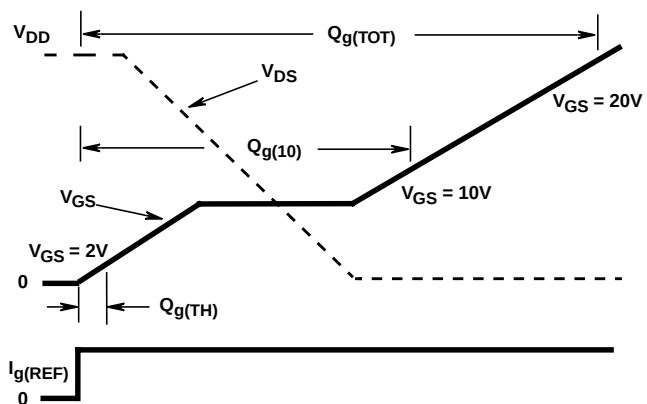


FIGURE 19. GATE CHARGE WAVEFORM

RFD16N06, RFD16N06SM

PSPICE Electrical Model

```
.SUBCKT RFD16N06 2 1 3 ; rev 10/31/94
CA 12 8 1.788e-10
CB 15 14 1.875e-10
CIN 6 8 8.33e-10
```

```
DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD
```

```
EBREAK 11 7 17 18 64.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1
```

```
IT 8 17 1
```

```
LDRAIN 2 5 1e-9
LGATE 1 9 4.56e-9
LSOURCE 3 7 4.13e-9
```

```
MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01
```

```
RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.4e-3
RGATE 9 20 3.0
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 21.5e-3
RVTO 18 19 RVTOMOD 1
```

```
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD
```

```
VBAT 8 19 DC 1
VTO 21 6 0.82
```

```
ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/94,7))}
```

```
.MODEL DBDMOD D (IS = 2.5e-13 RS = 7.1e-3 TRS1 = 3.04e-3 TRS2 = -10e-6 CJO = 1.12e-9 TT = 5.6e-8)
.MODEL DBKMOD D (RS = 2.51e-1 TRS1 = -6.57e-4 TRS2 = 1.66e-6)
.MODEL DPLCAPMOD D (CJO = 6.1e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.96 KP = 16.68 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3 TC2 = -7.19e-7)
.MODEL RDSMOD RES (TC1 = 5.45e-3 TC2 = 1.66e-5)
.MODEL RSCLMOD RES (TC1 = 1.25e-3 TC2 = 17e-6)
.MODEL RVTOMOD RES (TC1 = -5.15e-3 TC2 = -4.83e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.25 VOFF = -3.25)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.25 VOFF = -5.25)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.56 VOFF = 5.56)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 5.56 VOFF = 0.56)
```

```
.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

