Crystal-to-LVDS Integrated Frequency Synthesizer/Fanout Buffer

84427

DATASHEET

General Description

The 84427 is a Crystal-to-LVDS Frequency Synthesizer/Fanout Buffer. The output frequency can be programmed using the frequency select pins. The low phase noise characteristics of the 84427 make it an ideal clock source for 10 Gigabit Ethernet, 10 Gigabit Fibre Channel, OC3 and OC12 applications.

Features

- Six LVDS outputs
- Crystal oscillator interface
- Output frequency range: 77.76MHz to 625MHz
- Crystal input frequency: 19.44MHz, 25MHz or 25.5MHz
- RMS phase jitter at 155.52MHz, using a 19.44MHz crystal (12kHz to 20MHz): 3.4ps (typical)

  Phase noise:

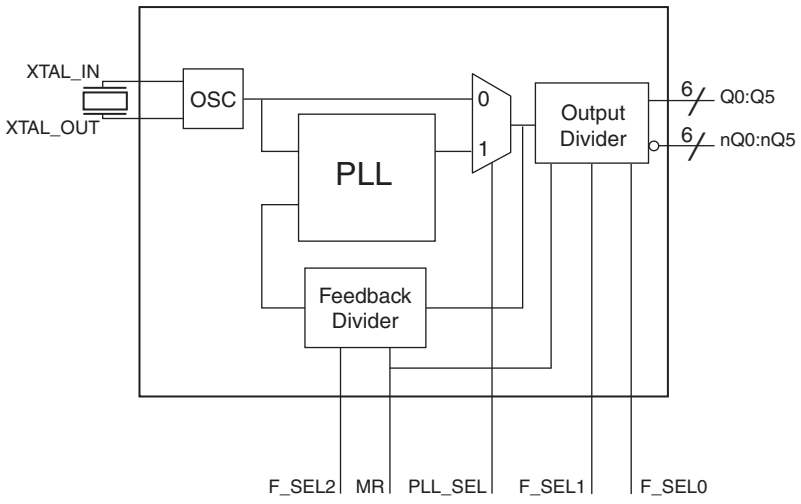
Offset	Noise Power
100Hz	-95 dBc/Hz
1kHz	-110 dBc/Hz
10kHz	-120 dBc/Hz
100kHz	-121 dBc/Hz

- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free RoHS-compliant package

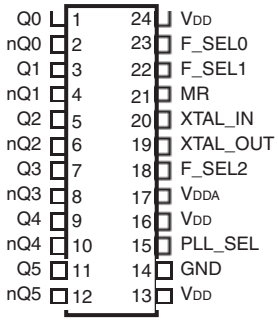
Function Table

Inputs					Output Frequency
F_XTAL	MR	F_SEL2	F_SEL1	F_SEL0	F_OUT
X	1	X	X	X	LOW
19.44MHz	0	1	0	0	77.76MHz
19.44MHz	0	1	0	1	155.52MHz
19.44MHz	0	1	1	0	311.04MHz
19.44MHz	0	1	1	1	622.08MHz
25MHz	0	0	0	0	78.125MHz
25MHz	0	0	0	1	156.25MHz
25MHz	0	0	1	0	312.5 MHz
25MHz	0	0	1	1	625MHz
25.5MHz	0	0	0	1	159.375MHz

Block Diagram



Pin Assignment



84427
24-Lead, 300-MIL SOIC
7.5mm x 15.33mm x 2.3mm body package
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. LVDS interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. LVDS interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. LVDS interface levels.
11, 12	Q5, nQ5	Output		Differential output pair. LVDS interface levels.
13, 16, 24	V_{DD}	Power		Core supply pins.
14	GND			Power supply ground.
15	PLL_SEL	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When HIGH, selects PLL. When LOW, selects XTAL_IN and XTAL_OUT. LVCMOS / LVTTL interface levels.
17	V_{DDA}	Power		Analog supply pin.
18	F_SEL2	Input	Pullup	Feedback frequency select pin. LVCMOS/LVTTL interface levels.
19, 20	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
21	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
22	F_SEL1	Input	Pulldown	Output frequency select pin. LVCMOS/LVTTL interface levels.
23	F_SEL0	Input	Pullup	Output frequency select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	50°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.72	3.3	V_{DD}	V
I_{DD}	Power Supply Current				300	mA
I_{DDA}	Analog Supply Current				30	mA

Table 3B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	MR, F_SEL1	$V_{DD} = V_{IN} = 3.465V$			150	µA
		PLL_SEL, F_SEL0, F_SEL2	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	MR, F_SEL1	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL, F_SEL0, F_SEL2	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 3C. LVDS DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		375	475	575	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.3	1.45	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 4. CRYSTAL CHARACTERISTICS

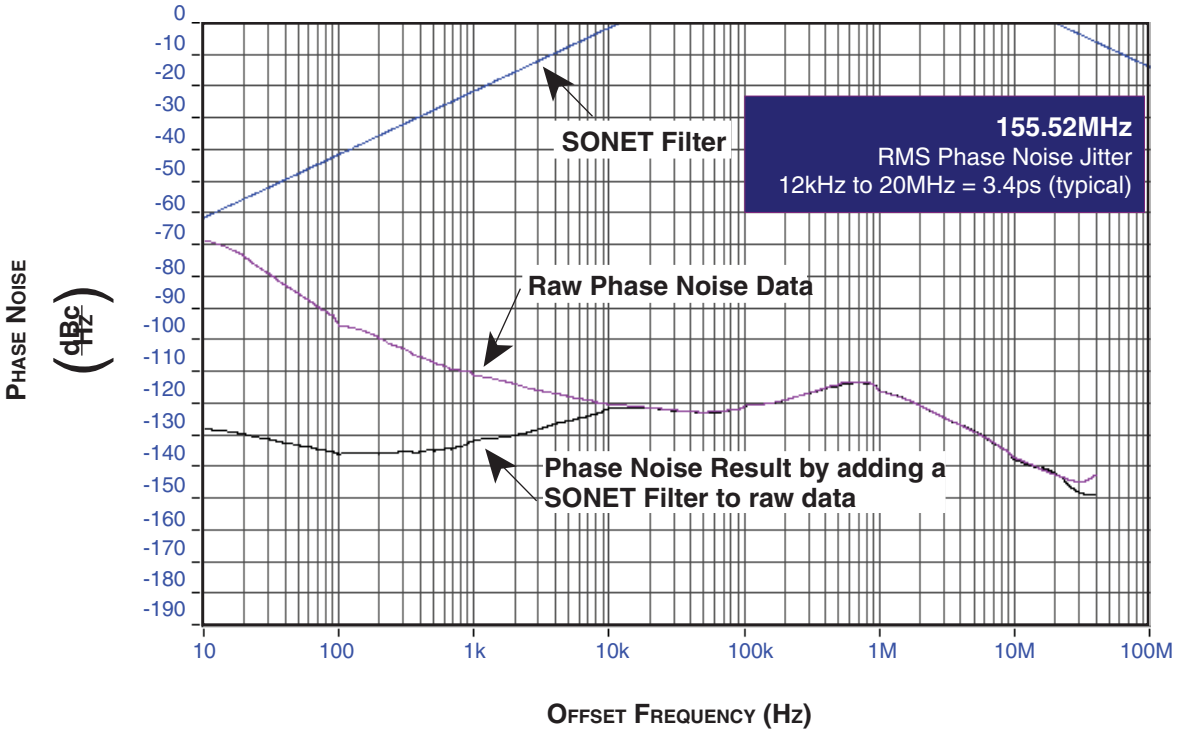
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.44		25.5	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

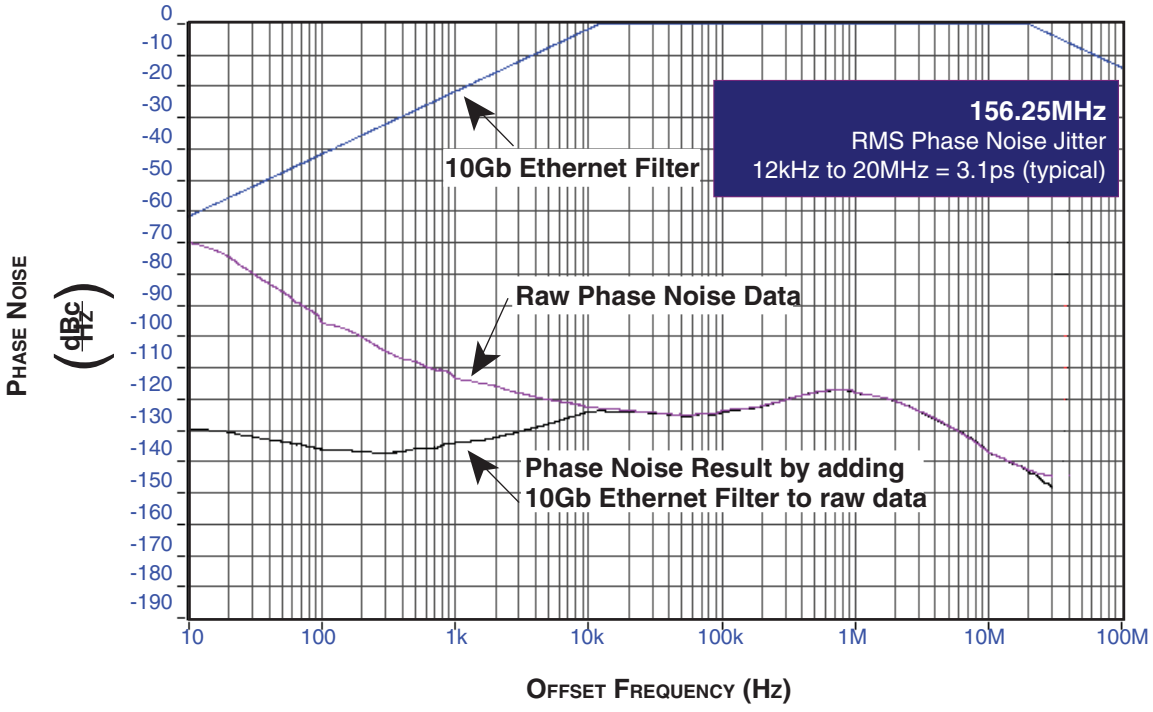
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		77.76		625	MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	155.52MHz, (Integration Range: 12kHz-20MHz)		3.4		ps
		156.25MHz, (Integration Range: 12kHz-20MHz)		3.1		ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2				36	ps
*t*sk(o)	Output Skew; NOTE 3, 4				85	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		47		52	%
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.
NOTE 1: See Phase Noise Plots.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.

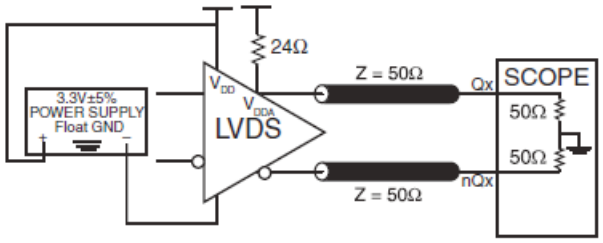
TYPICAL PHASE NOISE AT 155.52MHZ



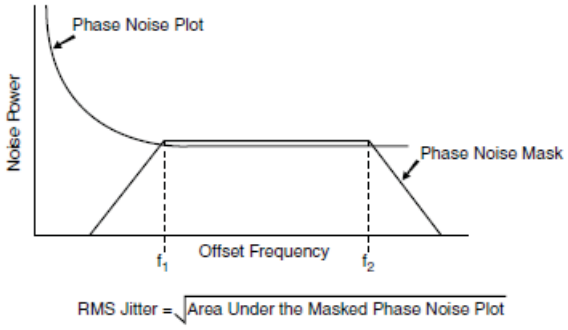
TYPICAL PHASE NOISE AT 156.25MHZ



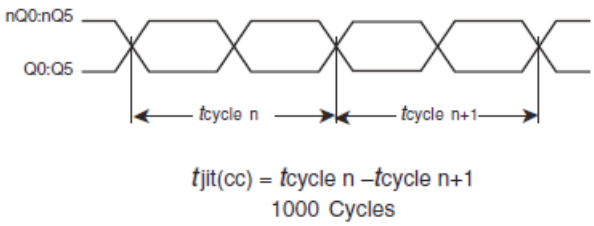
Parameter Measurement Information



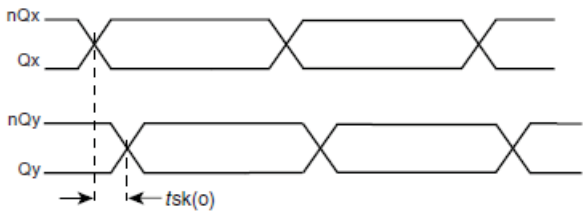
3.3V Output Load AC Test Circuit



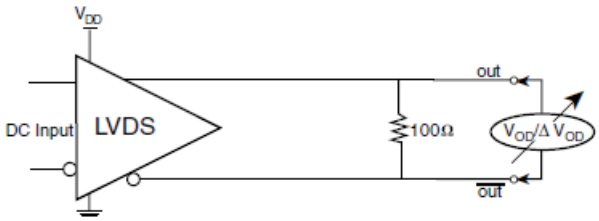
RMS Phase Jitter



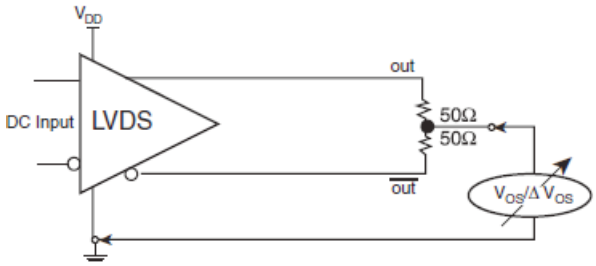
Cycle-to-Cycle Jitter



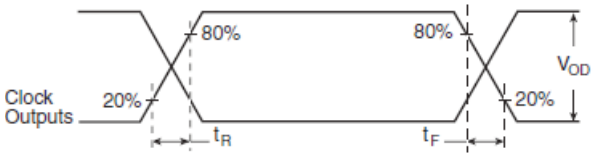
Output Skew



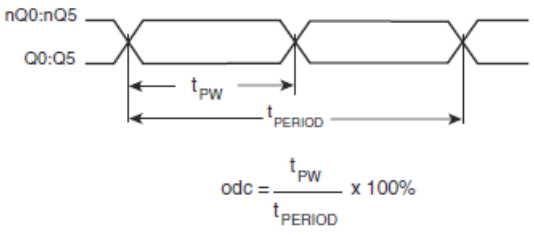
Differential Output Voltage Setup



Offset Voltage Setup



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 84427 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 24Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

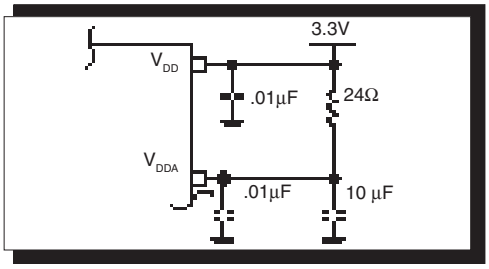


Figure 1. Power Supply Filtering

Crystal Input Interface

The 84427 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

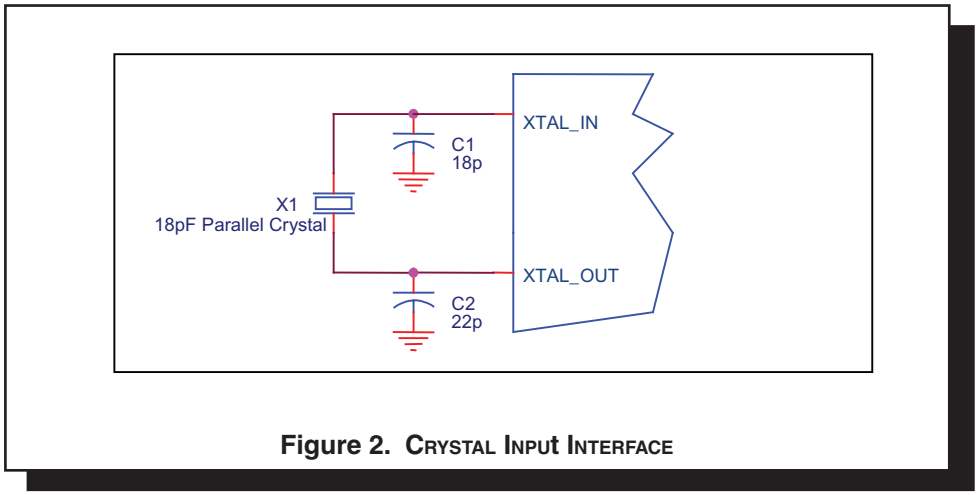


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

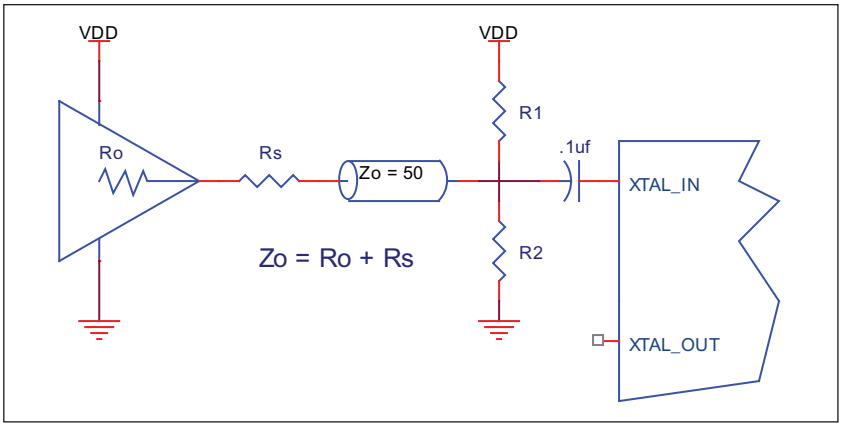


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Outputs:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

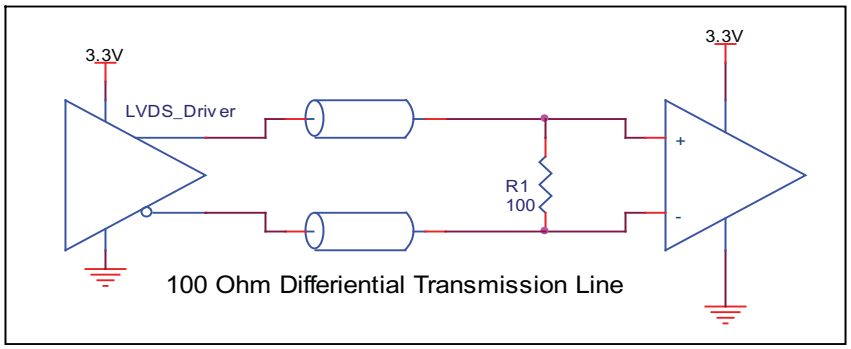


Figure 4. Typical LVDS Driver Termination

Schematic Example

Figure 5A shows a schematic example of using an 84427. In this example, the input is a 25MHz parallel resonant crystal with load capacitor CL=18pF. The frequency fine tuning capacitors C1 and C2 is 22pF and 18pF respectively. This example also shows logic control input handling. The configuration is set at F_SEL[2:0]=101, therefore, the output frequency is 156.25MHz.

It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the V_{DDA} pin as possible.

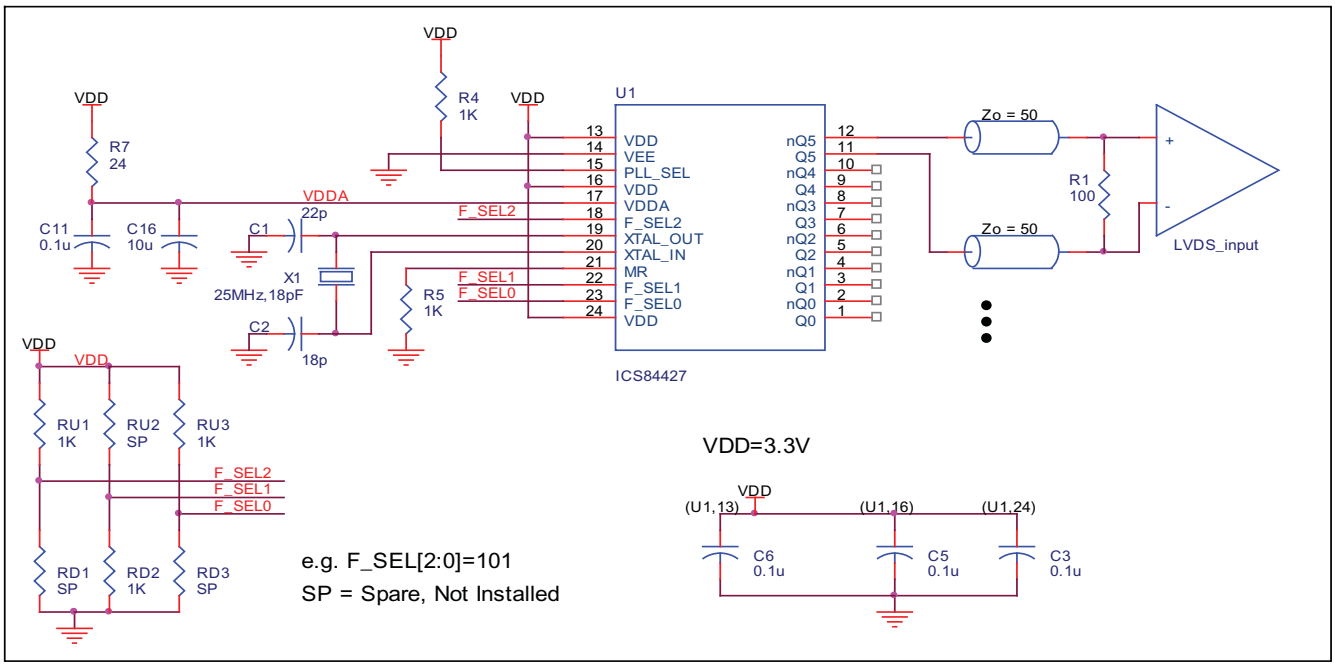


Figure 5A. 84427 Schematic Example

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C3, C5 and C6, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 100Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

Crystal

The crystal X1 should be located as close as possible to the pins 20 (XTAL_IN) and 19 (XTAL_OUT). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

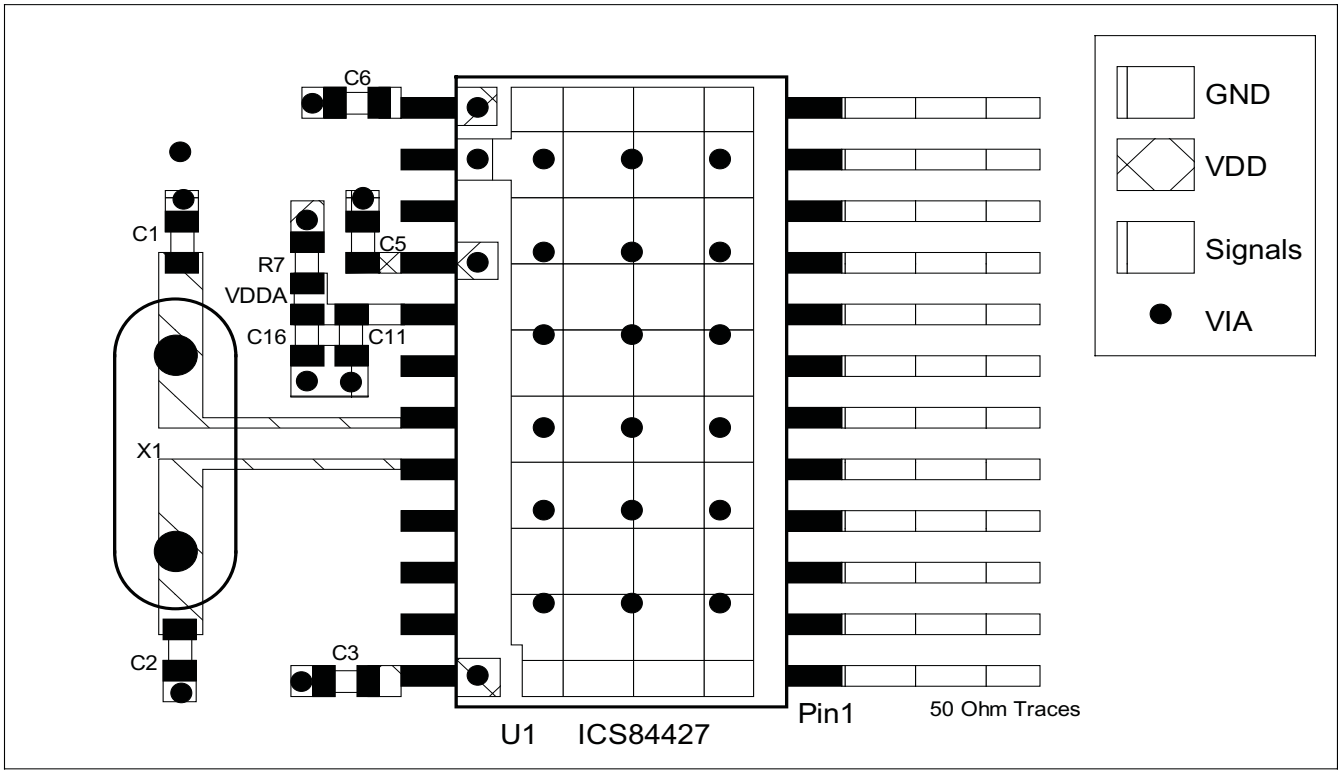


Figure 5B. PCB Board Layout for 84427

Power Considerations

This section provides information on power dissipation and junction temperature for the 84427.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 84427 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (300mA + 30mA) = **1143.45mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 43°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 1.143W * 43°C/W = 119.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24-Pin SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 24 Lead SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 84427 is: 2804

Package Outline - M Suffix for 24 Lead SOIC

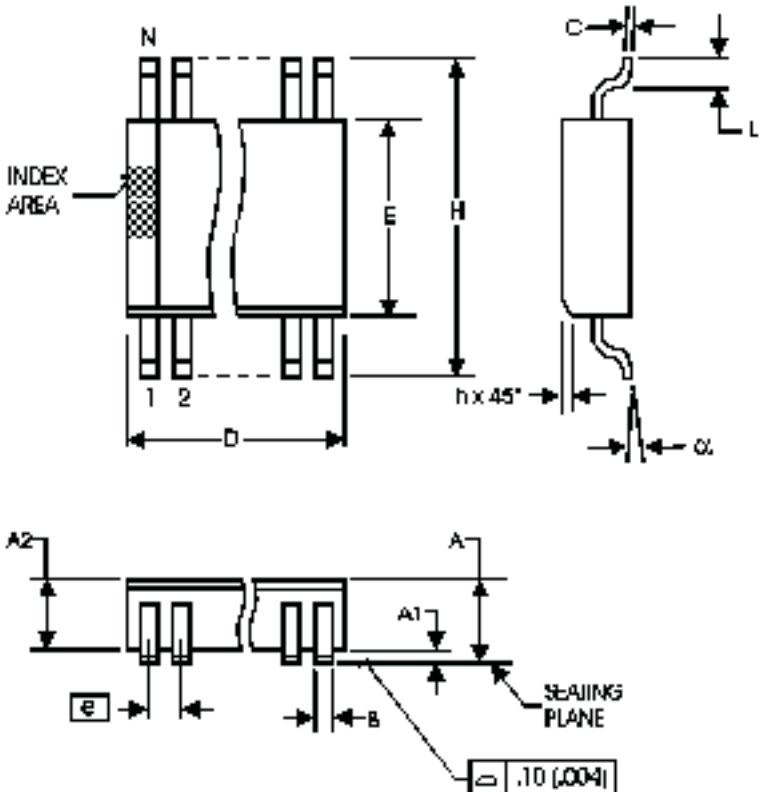


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	15.20	15.85
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
84427CMLF	ICS84427CMLF	24 Lead “Lead-Free” SOIC	tube	0°C to 70°C
84427CMLFT	ICS84427CMLF	24 Lead “Lead-Free” SOIC	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS complaint.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T9	14 16	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column.Added Contact Page.	7/27/10
B	T9	1 14	Product Discontinuation Notice - PDN CQ-15-03. Ordering Information - removed leaded devices.	5/6/15

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