AK2400

High integrated receiver for PMR/LMR

Overview

- □ Operating Supply Voltage : 2.7 to 5.5V
- □ Wide Operating Temperature Range : -40 to +85°C
- □ Delta-Sigma Fractional-N PLL with a frequency switching function
  : No glitch operation for AFC(Automatic Frequency Control) and DFM(Digital Frequency Modulation)
- □ High linearity RF Mixer(1st) and IF Mixer(2nd)
- □ IF Local frequency selectable as usage : 28.8MHz,45.9MHz,50.4MHz,57.6MHz
- □ Frequency tripler generates IF Local signal
- □ Built-in very narrow programmable bandwidth IF BPF (450kHz)
- □ PLL FM detector
- □ RSSI function
- □ Noise squelch circuit
- □ Built-in 12bits 1Msps SAR ADC
- □ Audio output signal S/N (Wide/Narrow) : 50dB / 46dB (Typ.) *De-emphasis + BPF
- □ Compact packaging : 56pin-QFN (8 x 8 mm、0.5 mm pitch)

Applications

- □ Narrowband high performance professional digital wireless systems (Channel spacing for 6.25kHz,12.5kHz)
- □ Public safety and community wireless systems
- □ Marine / mobile communication systems
- □ Low power radio systems
- □ Monitoring and control telemeter systems

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Block Diagram

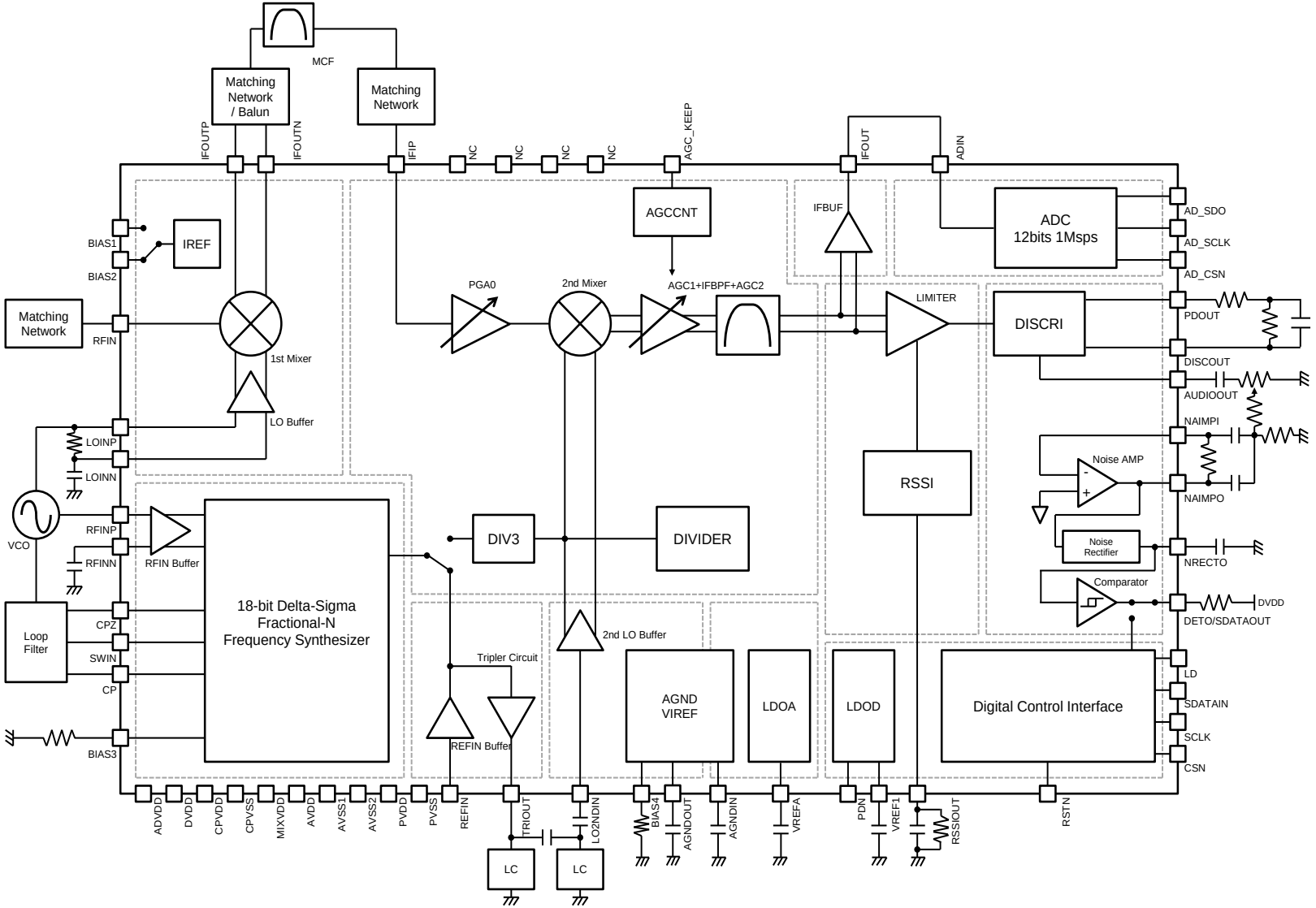


Figure 1 Block Diagram

Function

Block	Description
PLL SYNTH	The Delta-Sigma Fractional-N PLL (Phase Locked Loop) frequency synthesizer by the external VCO and the loop filter.
1stMIX	1st Mixer to convert the RFIN signal down to IF frequency by 1st LO signal.
PGA0+2ndMIX	2nd Mixer to convert the IFIP signal down to 450kHz by 2ndLO signal.
AGC+BPF	The circuit composed of AGC and BPF, where the desired signal is amplified and spurious components included in the signal from the 2nd-mixer are eliminated.
IFBUF	The circuit to output filtered signal by AGC+BPF.
Divider	The circuit to divide the signal from LO2NDIN pin.
LIMITER	The circuit to amplify the signal filtered at the AGC+BPF stage and generate rectangular wave.
DISCRI	The demodulator circuit with PLL FM detector, where the audio signal is recovered.
Noise AMP	The amplifiers to compose the Band-pass filter for noise squelch.
Noise Rectifier	The rectification circuit to detect the noise level.
Comparator	The circuit to compare the noise level with reference voltage level.
RSSI	The circuit to indicate the Received Signal Strength Indicator (RSSI) by generating a DC voltage corresponding to the input level from Limiter.
AGND+VIREF	The circuit to generate internal reference voltage.
Control Logic	The control register controls the status of internal condition by serial data that consists of 1 instruction bit, 5 address bits and 18 data bits.
ADC	12bits 1MSPS A/D converter.

Pin assignment

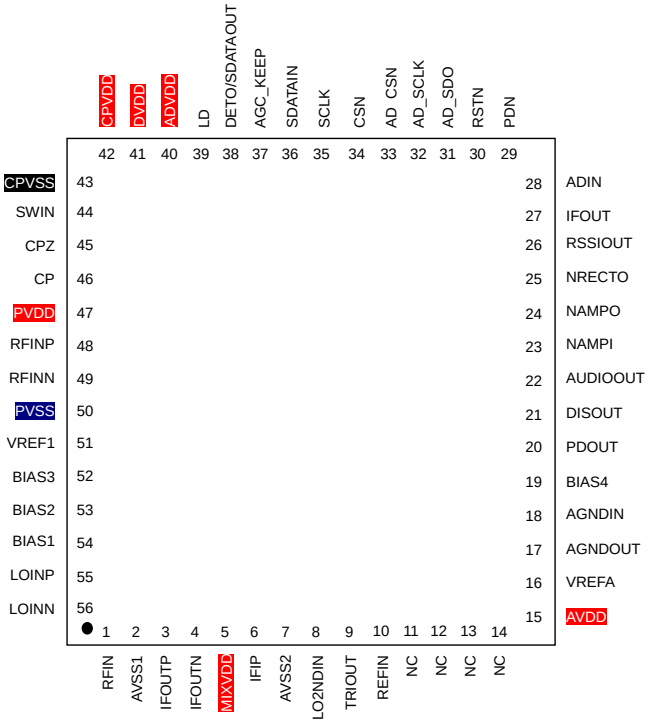


Figure 2 Pin assignment

Note) The exposed pad at the center of the backside should be connected to ground.

Pin/Function

No.	Name	Type	Conditions at power down	Function
1	RFIN	AI	-	RF signal input pin. Connecting a inductor between this pin and ground.
2	AVSS1	PWR	-	Analog VSS power supply pin
3	IFOUTP	AO	-	IF Output Positive .This pin is open drain output. It needs power feeding via an inductor.
4	IFOUTN	AO	-	IF Output Negative .This pin is open drain output. It needs power feeding via an inductor.
5	MIXVDD	PWR	-	Mixer VDD power supply pin
6	IFIP	AI	-	IF signal input pin
7	AVSS2	PWR	-	Analog VSS power supply pin
8	LO2NDIN	AI	-	2nd LO signal input pin
9	TRIOUT	AO	-	Tripler circuit output pin
10	REFIN	AI	-	Reference signal input pin
11	NC	-	Hi-Z	This pin must be left open
12	NC	-	Hi-Z	This pin must be left open
13	NC	-	Hi-Z	This pin must be left open
14	NC	-	Hi-Z	This pin must be left open
15	AVDD	PWR	-	Analog VDD power supply pin
16	VREFA	AO	-	LDO reference pin. Connect the capacitor to stabilize LDO reference voltage
17	AGNDOUT	AO	-	Analog ground output pin. Connect the capacitor to stabilize the analog ground level.
18	AGNDIN	AI	-	Analog ground input pin. Connect the capacitor to stabilize the analog ground level.
19	BIAS4	AO	-	Output pin to connect bias resistor for reference voltage
20	PDOUT	AO	-	Pin1 for Discriminator Low-pass filter
21	DISCOUT	AO	-	Pin2 for Discriminator Low-pass filter
22	AUDIOOUT	AO	-	Demodulated audio signal output pin
23	NAMPI	AI	-	Input pin for noise squelch amplifier
24	NAMPO	AO	-	Output pin for noise squelch amplifier
25	NRECTO	AO	-	Output pin for the rectification circuit
26	RSSIOUT	AO	-	Output pin to connect capacitor for Received Signal Strength Indicator(RSSI)
27	IFOUT	AO	-	Output pin for IFBUF
28	ADIN	AI	-	Input pin for A/D converter
29	PDN	DI	Hi-Z	Power down pin for LDO
30	RSTN	DI	Hi-Z	Hardware reset pin
31	AD_SDO	DO	-	A/D Converter data output pin for serial data
32	AD_SCLK	DI	Hi-Z	A/D Converter clock input pin for serial data
33	AD_CSN	DI	Hi-Z	A/D Converter chip select input pin for serial data
34	CSN	DI	Hi-Z	Chip select input pin for serial data

35	SCLK	DI	Hi-Z	Clock input pin for serial data
36	SDATAIN	DI	Hi-Z	Data input pin for serial data
37	AGC_KEEP	DI	Hi-Z	Input pin for AGC_KEEP function
38	DETO / SDATAOUT	DO	Hi-Z	Signal detect output pin/ Data output pin for serial data
39	LD	DO	Low	Lock detect output pin for PLL
40	ADVDD	PWR	-	AD VDD power supply pin
41	DVDD	PWR	-	Digital VDD power supply pin
42	CPVDD	PWR	-	Charge pump VDD power supply pin
43	CPVSS	PWR	-	Charge pump VSS power supply pin
44	SWIN	AI	Note1,2	Connect to resistance pin for fast lock up
45	CPZ	AI	Note1,2	Connect to the loop filter capacitor
46	CP	AO	Hi-Z	Charge pump output pin
47	PVDD	PWR	-	PLL VDD power supply pin
48	RFINP	AI	-	Prescaler input positive
49	RFINN	AI	-	Prescaler input negative
50	PVSS	PWR	-	PLL VSS power supply pin
51	VREF1	AO	-	LDO reference pin. Connect the capacitor to stabilize LDO reference voltage
52	BIAS3	AO	-	Resistance pin for setting charge pump output current
53	BIAS2	AIO	-	Resistance pin for current adjustment for 1st Mixer
54	BIAS1	AIO	-	Resistance pin for current adjustment for 1st Mixer
55	LOINP	AI	-	Lo input positive
56	LOINN	AI	-	Lo input negative

AI: Analog input pin AO: Analog output pin AIO: Analog I/O pin
PWR: Power supply pin DI: Digital input pin DO: Digital output pin

Note1) When [PDN]="0", {PDSYNTH_N}="0", or [PDN]="1",{PDSYNTH_N}="0", the state of the switch of loop filter selection is ON.

Note2) Power down refers to the state where [PDN]="0" after power-on.

[CPZ] pin should be connected to R2 and C2, which are intermediate nodes, even if the Fast Lockup feature is not used. For the output destination from [CPZ] pin, see "Charge Pump and Loop Filter" on page 36.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD1	-0.3	6.5	V	Note 1
	CPVDD	-0.3	6.5	V	
	MIXVDD	-0.3	5.5	V	
	DVDD	-0.3	6.5	V	
Ground level	VSS	0	0	V	
Analog Input Voltage	V_{AIN}	-0.3	VDD1+0.3 CPVDD+0.3 MIXVDD+0.3	V	Note 1
Digital Input Voltage	V_{DIN}	-0.3	DVDD+0.3	V	
Input Current (Except power supply pin)	I_{IN}	-10	+10	mA	
RF Input Power	RFPOW		12	dBm	
LO Input Power	LOPOW		12	dBm	
Storage Temperature	T_{stg}	-55	125	℃	

Note 1 VDD1 is applied to PVDD, AVDD, ADVDD pins
Note 2 All voltages are relative to the VSS pin.
Note 3 Exceeding these maximum ratings may result in damage to the AK2400. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Temperature	Ta		-40		85	°C
Power Supply voltage	VDD1	PVDD, AVDD, ADVDD	DVDD	3.0	5.5	V
	CPVDD		VDD1	5.0	5.5	V
	MIXVDD		VDD1	5.0	5.5	V
	DVDD		2.7	3.0	5.5	V
Analog Reference Voltage	AGND	AGNDOUT		1/2VREFA		V

Note) All voltages are relative to the VSS pin.

Digital DC Characteristics

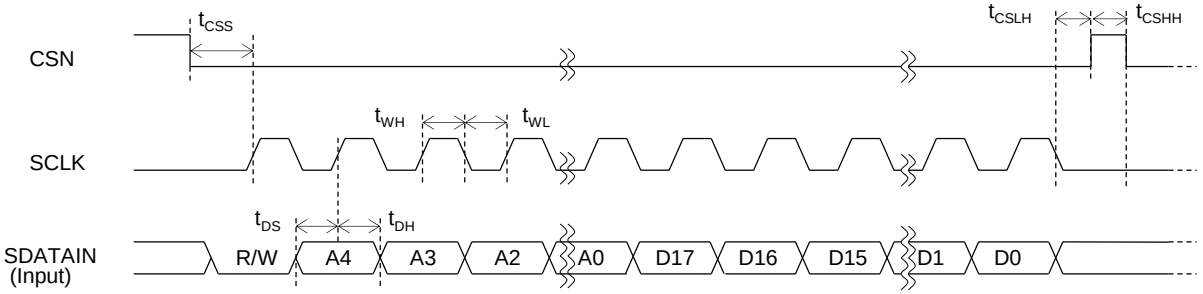
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	RSTN, SCLK, SDATAIN, CSN, PDN, AD_CSN, AD_SCLK,, AGC_KEEP	0.8DVDD			V
Low level input voltage	V_{IL}	RSTN, SCLK, SDATAIN, CSN, PDN, AD_CSN AD_SCLK, AGC_KEEP			0.2DVDD	V
High level input current	I_{IH}	V_{IH}=DVDD RSTN, SCLK, SDATAIN, CSN, PDN, AD_CSN, AD_SCLK, AGC_KEEP			10	uA
Low level input current	I_{IL}	V_{IL}=0V RSTN, SCLK, SDATAIN, CSN, PDN, AD_CSN, AD_SCLK, AGC_KEEP	-10			uA
High level output voltage	V_{OH}	I_{OH}=+0.2mA LD, AD_SDO, DETO/SDATAOUT	DVDD-0.4		DVDD	V
Low level output voltage	V_{OL}	I_{OL}=-0.4mA LD, AD_SDO, DETO/SDATAOUT	0.0		0.4	V

Digital AC Timing

1) Serial Interface Timing

AK2400 is connected to a CPU by three-wired interface through CSN, SCLK, SDATAIN and SDATAOUT pins, which can make reading and writing data for control registers.
Serial data named SDATAIN is consist of 1-bit read and write instruction(R/W), 5-bit address (A4 to A0) and 18-bit data(D17 to D0) in one frame.

Write mode



Read mode

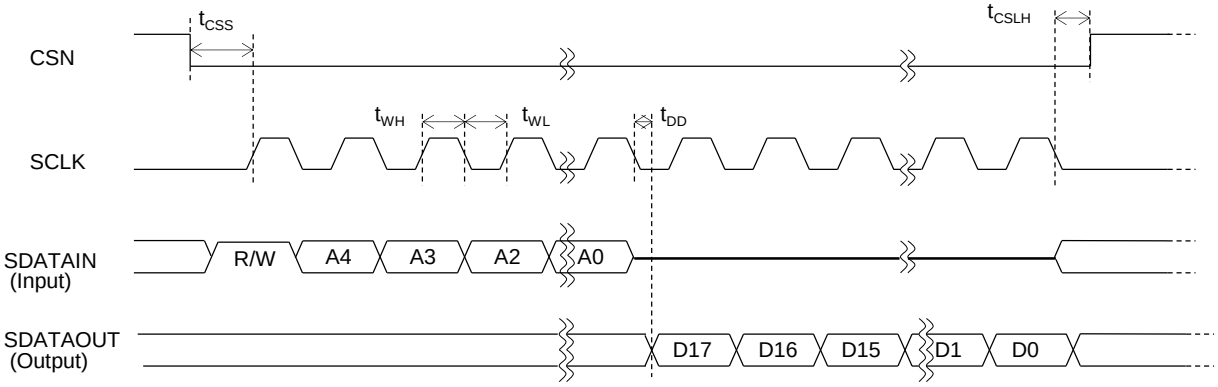


Figure 3 Serial Interface Timing

R/W : Instruction bit controls to write data to AK2400 or read back from it.
When set to low, AK2400 is in write mode. When set to high, AK2400 is in read mode.

A4 to A0 : Register address to be accessed.
D17 to D0 : Write or read date to be accessed.

<1> CSN(Chip select) is normally selected high for disable.
When CSN is set to low, serial interface becomes active.

<2> In write mode, instruction, address and data input from SDATAIN pin are synchronized and latched with the rising edge of 24 iterations of SCLK clock. Set to low between address A0 and data D17.Input data is fixed synchronized with the rising edge of 24th clock. Note that if CSN become “H” before 24th clock, setting data becomes invalid. During the period when CSN is set to “L”, consecutive writing is available.

<3> In read mode, instruction and address are synchronized and latched with the rising edge of 6 iterations of SCLK clock. And the register data are output from SDATAIN pin synchronized with the falling edge of 18 iterations of SCLK clock.
CSN to “H” once reading is completed because consecutive reading is not valid.
Also, in read mode DETO/SDATAOUT pin should be set to SDATAOUT by {SDATAOUT_OE}=”1”.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CSN setup time	t_{CSS}		40			ns
SDATAIN setup time	t_{DS}		20			ns
SDATAIN hold time	t_{DH}		20			ns
SCLK high time	t_{WH}		40			ns
SCLK low time	t_{WL}		40			ns
CSN low hold time	t_{CSLH}		20			ns
CSN high hold time	t_{CSHH}		40			ns
SCLK to SDATA output delay time	t_{DD}	20pF load			40	ns

Note) Digital input and output timing is relative to 0.5DVDD of rising signal and falling signal.

ADC AC Timing

At first, set {PDADC_N}=”1” to operate the A/D Converter. A/D conversion cycle is started by the falling edge of AD_CSN. AD_SDO outputs “0” synchronized with the falling edge of AD_CSN. AD_SDO outputs “0” until the third falling edge of AD_SCLK. From the fourth falling edge, the results of 12 bits A/D conversion are output with MSB first during the 16th edge. A/D conversion cycle is ended on the 16th falling edge, AD_SDO becomes Hi-Z. After the 16th edge, set AD_CSN =”1”. Since A/D converter becomes acquisition phase after the 16th falling edge of AD_SCLK, AD_CSN pin must keep ”1” during the end of “tq” time after AD_SDO became Hi-Z. It is possible to get the available conversion results from the next cycle, since the first A/D conversion result is the dummy cycle (unavailable result).

D11 to D0 : A/D converted data

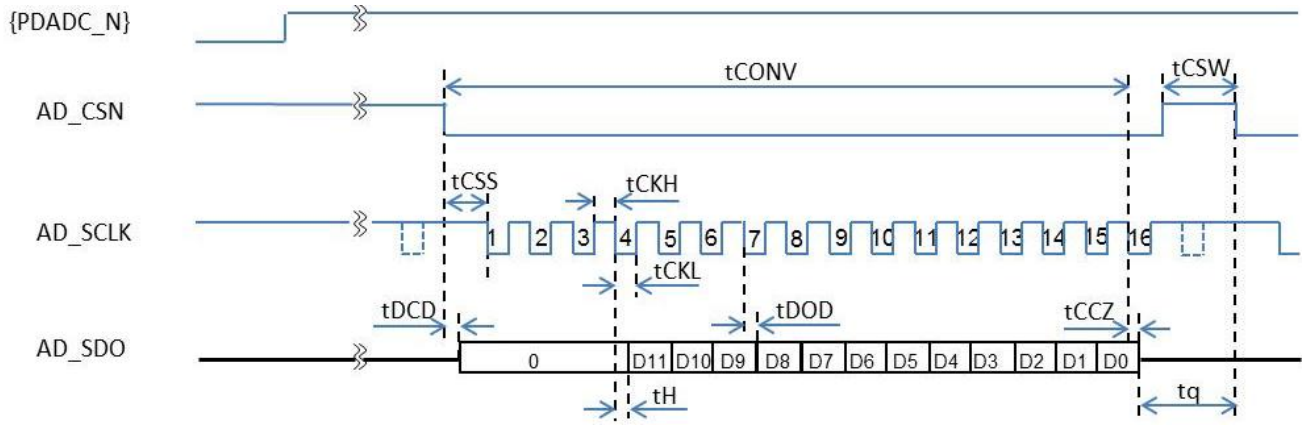


Figure 4 ADC Timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AD_SCLK frequency	fADSCLK				20	MHz
Minimum quiet time required between bus relinquish and start of next conversion	Tq		40			ns
AD_CSN Falling to First SCLK Falling time	tCSS		10			ns
AD_CSN edge to AD_SDO Tri-State Disabled	tDCD				25	ns
AD_SCLK Falling to AD_SDO Output Delay time	tDOD	15pF load			25	ns
AD_SCLK High Pulse Width	tCKH		0.4×tA DSCLK			ns
AD_SCLK Low Pulse Width	tCKL		0.4×tA DSCLK			ns
16th AD_SCLK Falling to AD_SDO Hi-Z State Delay time	tCCZ				25	ns
Minimum AD_CSN Pulse Width	tCSW		25			ns

Note) Digital input and output timing is relative to 0.5DVDD of rising signal and falling signal.

Power-up sequence

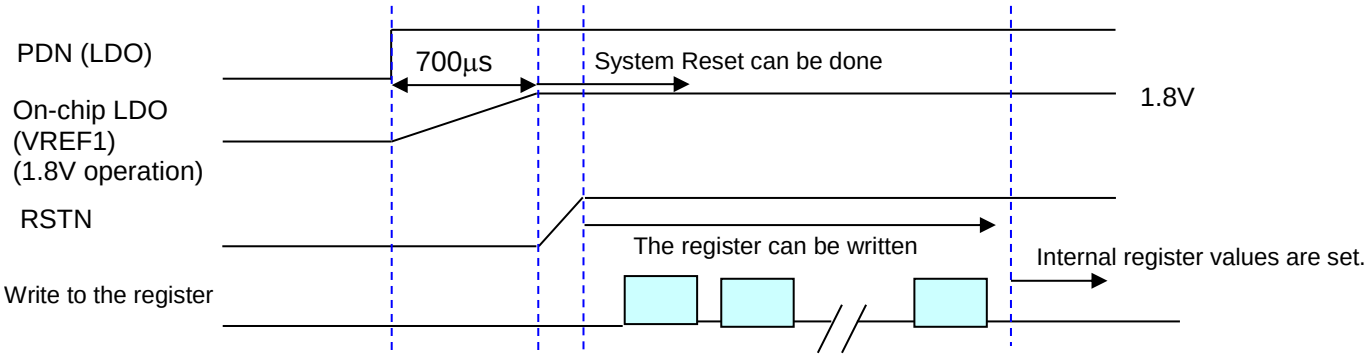


Figure 5 power-up sequence

Note) Power-up sequence assumes VDD ON.
After PDN is set to “High”, registers remain undefined. In order to initialize them, RSTN is set to “High”

System Reset

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Hardware reset signal input width	t_{RSTN}	RSTN pin	1			µs	Note 1)
Software reset		SRST register					Note 2)

Note1) After power-on, be sure to perform a hardware reset operation (register initialization). The system is reset by a Low input of 1us (min.) and enters the normal operation state.

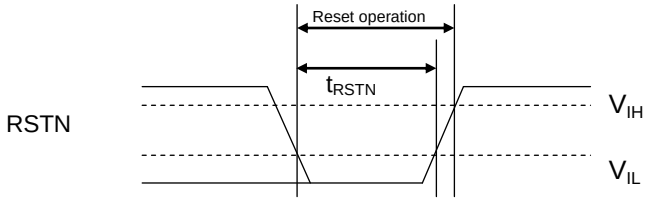


Figure 6 System Reset

During the reset operation, SCLK, SDATAIN and CSN pin should be keep to Low or High.

Ex) SCLK:Low, SDATAIN:Low, CSN:High

Note2) When data 0x09:10101010 is written to the SRST[7:0] register, software reset is performed. This setting initializes the registers and the operation mode is set to mode 2 (Standby 2). After software reset is completed, this register comes to “0”.

Analog Characteristics (PLL SYNTH)

Unless otherwise noted VDD=2.7 to 5.5V, Ta=-40°C to 85°C.

Parameter	Min	Typ.	Max	Unit	Remarks
RF Characteristics					
Input Sensitivity	-10		5	dBm	
Input Frequency	40		500	MHz	Prescaler 4/5
	40		1000	MHz	Prescaler 8/9,16/17
REFIN Characteristics					
Input Sensitivity	0.4		2	Vpp	
Input Frequency		15.3 16.8 19.2		MHz	Note 1)
Phase Frequency Detector					
Phase Detector Frequency			6.4	MHz	
Charge Pump					
Charge Pump 1 Maximum Value		168.9		μA	BIAS3=27kΩ, Note 2)
Charge Pump 1 Minimum Value		21.1		μA	BIAS3=27kΩ, Note 2)
Charge Pump 2 Maximum Value		2.32		mA	BIAS3=27kΩ, Note 3)
Charge Pump 2 Minimum Value		0.84		mA	BIAS3=27kΩ, Note 3)
Icp TRI-STATE Leak Current		1		nA	0.6≦Vcpo≦CPVDD-0.7 (Vcpo:CP pin voltage)
Mismatch between Source and Sink Currents Note 4)			10	%	Vcpo= CPVDD/2 Ta=25°C
Icp vs. Vcpo Note 5)			15	%	0.5≦Vcpo≦CPVDD-0.5 Ta=25°C
Current Consumption					
IDD_SYN1			10	μA	PDN=0
IDD_SYN2		2.4	3.6	mA	Note 6)
IDD_SYN3		0.17		mA	Note 7)

Note 1) REFIN pin is input one third of the 2nd LO input frequency.
Note 2) Charge pump 1 current is determined by the setting in {CP1[2:0]} which is described on page 22.
Note 3) Charge pump 2 current is determined by the setting in {CP2[2:0]} which is described on page 23.
Note 4) Mismatch between Source and Sink Currents: [(|Isink|-|Isource|)/{(|Isink|+|Isource|)/2}] × 100 [%]
Note 5) Icp vs. Vcpo: [{1/2×(|I1|-|I2|)}/{1/2×(|I1|+|I2|)}]×100 [%]
Note 6) [PDN]="High", {PDSYNTH_N}="High" IDD for [PVDD]
Note 7) [PDN]="High", {PDSYNTH_N}="High" IDD for [CPVDD]
IDD does not include the operation current in fast lockup mode.

Note) [PDN]="High", {PDSYNTH_N}="High" , the total current consumption = IDD_SYN2+IDD_SYN3
Note) In the shipment test, the exposed pad on the center of the back of the package is connected to ground.
Note) When 2nd LO input frequency is used 28.8MHz, set {PDTRI_N}=0 and input the 2nd LO signal(28.8MHz) from LO2NDIN pin. Then REFIN Frequency is set 28.8MHz/3=9.6MHz.

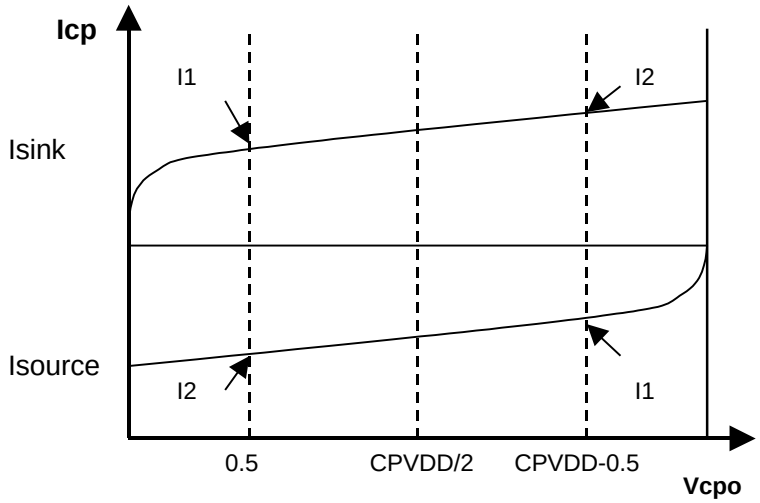


Figure 7 Charge Pump Characteristics - Voltage vs. Current

Analog Characteristics (1st MIXER)

Unless otherwise noted IF output=50MHz, Lo Input Level=-10dBm to +5dBm, {FMIX_HV}=0, {FMIX_IP3}=0, Output Load Resistor (RLoad)=2.2kΩ, VDD=2.7 to 5.5V, Ta=-40°C to 85°C, Test circuit is shown on page 41.

Parameter	Min.	Typ.	Max.	Unit	Remarks
RF Input Frequency	10		2000	MHz	
Lo Input Frequency	10		2000	MHz	
IF output Frequency	20		100	MHz	
Lo Input Power	-10	0	+5	dBm	
Current Adjustment Resistor(BIAS) ({FMIX_HV}=0)	39		100	kΩ	Vdd=2.7 to 5.5V
Current Adjustment Resistor(BIAS) ({FMIX_HV}=1)	18		39	kΩ	Vdd=4.5 to 5.5V
IDD(BIAS=18kΩ, {FMIX_HV}=1)		24		mA	The total current of MIXVDD,IFOUTP, IFOUTN.
IDD(BIAS=47kΩ)		9	13	mA	
IDD({PDFSTMIX_N}=0）		1	10	uA	
RFIN=600MHz, LOIN=550MHz(0dBm), BIAS=47kΩ, Vdd=3V					
Conversion Gain	0.5	3	5	dB	
SSB Noise Figure		8.5	11	dB	Design guarantee value
IP1dB	-3	1		dBm	
IIP3	7	11		dBm	
RFIN=600MHz, LOIN=550MHz(0dBm), BIAS=18kΩ, {FMIX_HV}=1,Vdd=5V					
Conversion Gain		5		dB	
SSB Noise Figure		8.5		dB	Design guarantee value
IP1dB		0		dBm	
IIP3		16		dBm	Design guarantee value
RFIN=600MHz, LOIN=550MHz(0dBm), BIAS=47kΩ, Vdd=3V, {FMIX_IP3}=1					
Conversion Gain		3		dB	
SSB Noise Figure		10		dB	Design guarantee value
IP1dB		0		dBm	
IIP3		14		dBm	Design guarantee value
IDD		7		mA	

Analog Characteristics (2nd IF)

Unless otherwise noted VDD=2.7 to 5.5V, Ta=-40°C to 85°C.
Mode 6, LO2NDIN=50.4MHz,IFIP=50.85MHz, ∆f=±1.5kHz, fmod=1kHz、AGC+BPF=F2, {AGC_OFF}=0, {AGC_KEEP_SEL}=0, {AGC_KEEP}=0, PGA0[2:0]=011. {SDATAOUT_OE}=0. The exposure back pad of the package is connected to VSS. Test circuit is shown on page 45.

1) 2nd LO input

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Parameter	F_{LO}	LO2NDIN		28.8 45.9 50.4 57.6		MHz	
Local Frequency	V_{LO}	LO2NDIN	0.2		2.0	V_{PP}	Note

Note) Input from LO2NDIN pin through DC cut

2) PGA0+2nd Mixer
Analog Characteristics (2nd IF) are included the circuit of IFIP input pin.
The input impedance of 2nd IF_INPUT is 50Ω typ. (See Figure 8 for input matching network)

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Input Impedance			50		Ω	
Input Frequency			F_{LO} ±0.45		MHz	
Voltage Gain			48		dB	

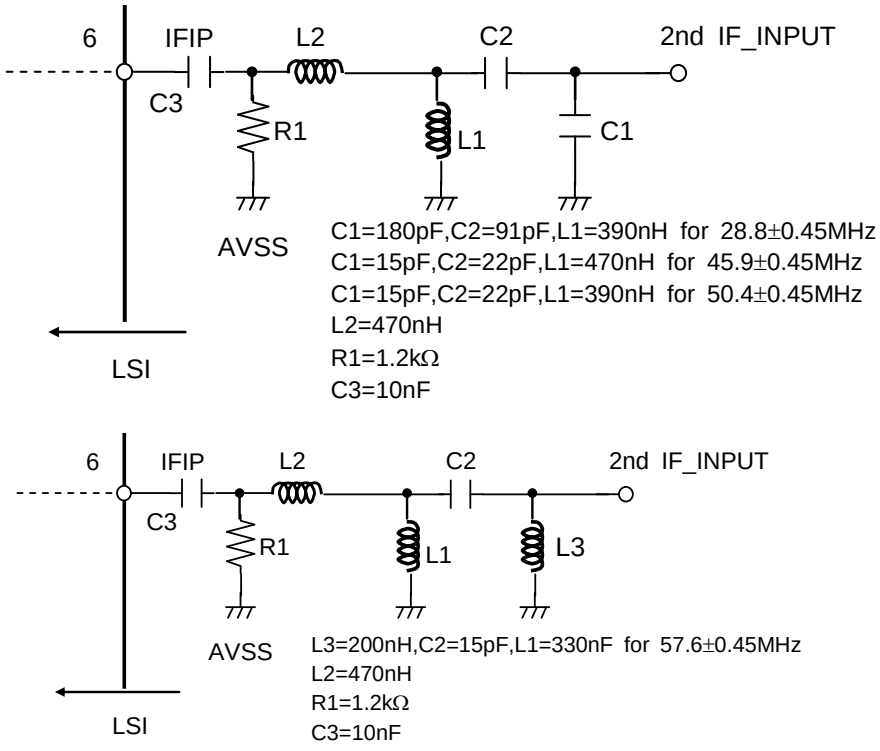


Figure 8 Test circuit of IFIP Input pin (2nd IF)

3) 2nd IF RX overall characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
12dB SINAD	Note 1)		-112		dBm	
2nd IF block Total Gain	Mode 5 Maximum gain setting for AGC IFIP to IFOUT {IFOG[2:0]}=001		101		dB	
	Mode 5 Minimum gain setting for AGC IFIP to IFOUT {IFOG[2:0]}=001		49		dB	
NF	Mode 5, BPF=F3 Maximum gain setting for AGC IFIP to IFOUT {IFOG[2:0]}=001		8		dB	
IIP3	Maximum gain setting for AGC IFIP=50.8635MHz&50.876MHz {IFOG[2:0]}=001		-37		dBm	
IP1dB	Minimum gain setting for AGC {IFOG[2:0]}=001		-40		dBm	
Demodulation Output Level	∆f=±3.0kHz,fmod=1kHz, AGC+BPF=F1,{DISLPF_G[2:0]}=101	70	100	130	mVrms	
	∆f=±1.5kHz,fmod=1kHz, AGC+BPF=F2,{DISLPF_G[2:0]}=001	70	100	130	mVrms	
S/N Ratio	∆f=±3.0kHz,fmod=1kHz,Vin=-47dBm AGC+BPF=F1, {DISLPF_G[2:0]}=101 Note 1)	42	50		dB	
	∆f=±1.5kHz,fmod=1kHz,Vin=-47dBm AGC+BPF=F2, {DISLPF_G[2:0]}=001 Note 1)	36	46		dB	
Audio Frequency characteristics	∆f=±0.5kHz,fmod=3kHz,Vin=-47dBm AGC+BPF=F3, IFIP to AUDIOOUT {DISLPF_G[2:0]}=001 Note 2)	-4.3	-3.5		dB	

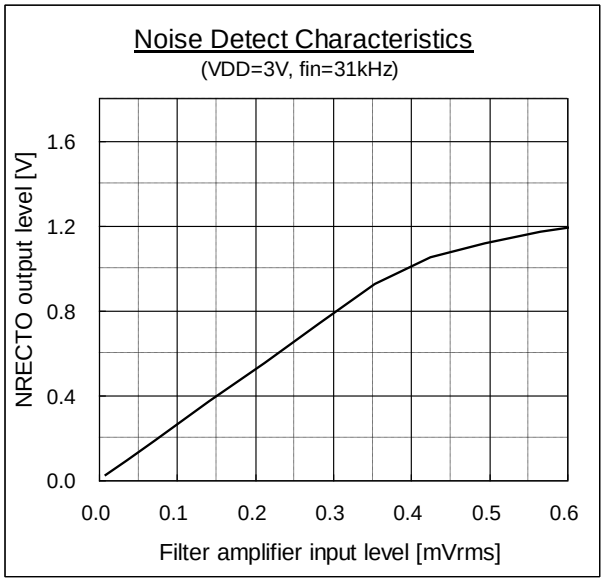
Note 1) With De-emphasis+BPF(0.3 to 3kHz)
Note 2) relative to the output level at fmod=1kHz

4) RSSI Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
RSSI output voltage	IFIP→RSSIOUT, {AGC_OFF}=0 IFIP=-115dBm input		0.6		V	
	IFIP→RSSIOUT, {AGC_OFF}=0 IFIP=-45dBm input		2.2		V	

5) Noise Squelch Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Noise Detection Level	NRECTO→DETO Detect High		0.5	0.7	V	
	NRECTO→DETO Detect Low	0.3	0.4		V	
Noise Detection Characteristics	NAMPI→NRECTO Input : 31kHz, 0.1mVrms		0.3		V	
	NAMPI→NRECTO Input : 31kHz, 0.25mVrms		0.65		V	



6) AGC+BPF

6.1) F0 (E type)

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Attenuation Characteristics (relative to the gain at 450kHz)	435kHz			-50	dB	
	442.5kHz	-6			dB	
	457.5kHz	-6			dB	
	465kHz			-50	dB	
Gain ripple	Within 450±5kHz			3	dB	

6.2) F1 (F type)

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Attenuation Characteristics (relative to the gain at 450kHz)	437.5kHz			-50	dB	
	444kHz	-6			dB	
	456kHz	-6			dB	
	462.5kHz			-50	dB	
Gain ripple	Within 450±4kHz			3	dB	

6.3) F2 (G type)

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Attenuation Characteristics (relative to the gain at 450kHz)	439kHz			-50	dB	
	445.5kHz	-6			dB	
	454.5kHz	-6			dB	
	461kHz			-50	dB	
Gain ripple	Within 450±3kHz			3	dB	

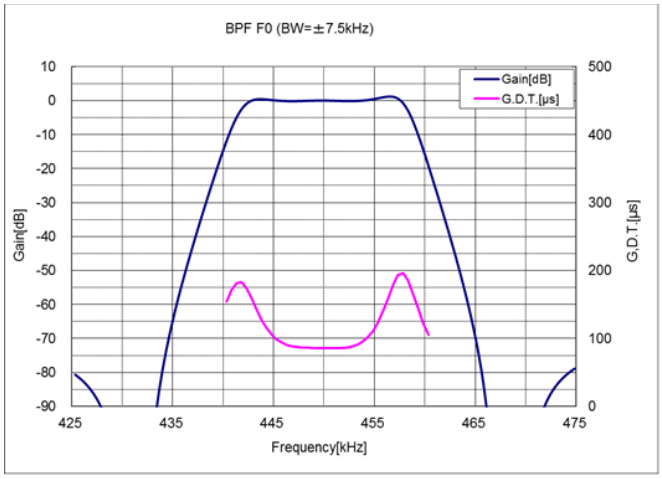
6.4) F3 (H type)

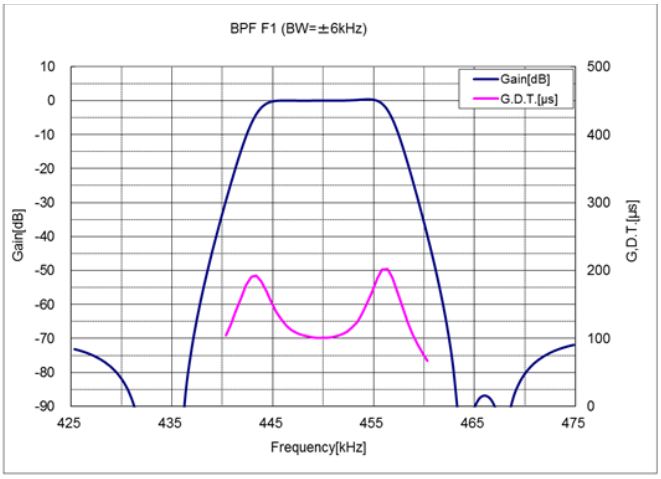
Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Attenuation Characteristics (relative to the gain at 450kHz)	441kHz			-50	dB	
	447kHz	-6			dB	
	453kHz	-6			dB	
	459kHz			-50	dB	
Gain ripple	Within 450±2kHz			2	dB	

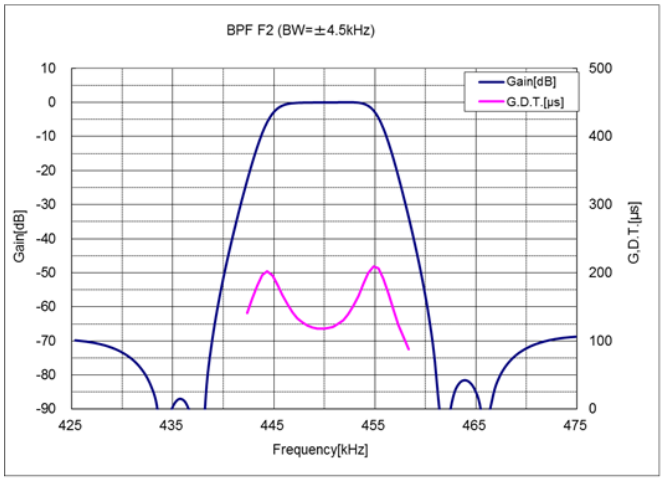
6.5) F4 (J type)

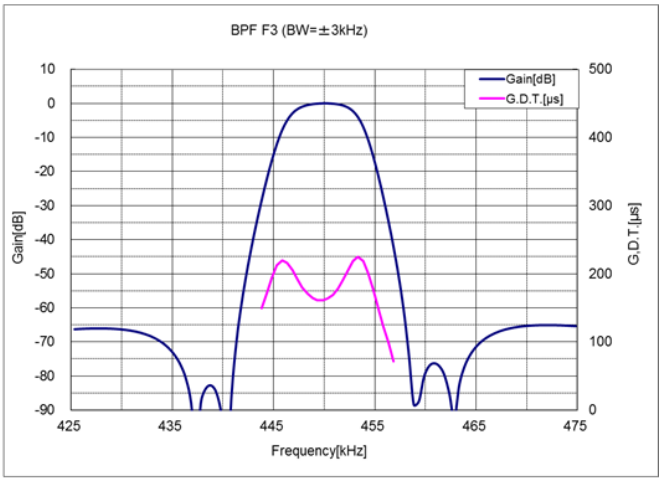
Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Attenuation Characteristics (relative to the gain at 450kHz)	443kHz			-50	dB	
	448kHz	-8			dB	
	452kHz	-8			dB	
	457kHz			-50	dB	
Gain ripple	Within 450±1.5kHz			3.5	dB	

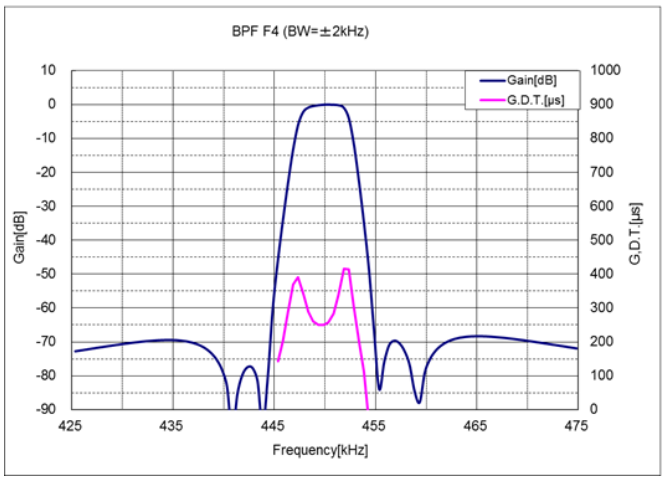
Filter Characteristics











7) IFBUF Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Settling time	IFBUF to IFOUT, IFBUF=0.32Vpp/step C_{L2}=21pF, {IFOG[2:0]}=001		100		ns	

Note) Convergence time within 1% when 0.32Vpp step signal input to IFBUF pin

8) Current Consumption

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current Consumption	IDD0	Mode0 Power down			0.01	mA
	IDD1	Mode1 (Prohibited)			-	mA
	IDD2	Mode2 Standby(Initial value)		0.1	0.15	mA
	IDD3	Mode3		1	1.5	mA
	IDD4	Mode4, Digital Mode 1 with no signal input		7	11	mA
	IDD5	Mode5 Digital Modo 2 with no signal input. Note 2)		7.5	12	mA
	IDD6	Mode6 Analog Mode with no signal input Note 2)		7.5	12	mA
	IDD7	Mode7 Full Power On with no signal nput Note 2)		8.5	13	mA

Note 1) Current Consumption is AVDD pin.
Note 2) Tripler circuit : ON
Note 3) Do not use Mode1.

Analog Characteristics (ADC)

Unless otherwise noted VDD=2.7 to 5.5V, Ta=-40°C to 85°C.
fs=1MHz , ADVDD = 3.0V, AD_SCLK=20MHz

Parameter	Min.	Typ.	Max.	Unit
Resolution		12		Bits
No Missing Codes Note 2)	11			Bits
Integral Nonlinearity (INL) Error		±2		LSB
Differential Nonlinearity (DNL) Error		±1		LSB
Input Voltage Range	0		ADVDD	V
ADVDD Power Current		2	3.8	mA

Note 1) The above is the characteristics of only A/D converter block.
Note 2) Design guarantee value

Register Map and Function Description

Name	Address	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NUM	0x01	NUM [17]	NUM [16]	NUM [15]	NUM [14]	NUM [13]	NUM [12]	NUM [11]	NUM [10]	NUM [9]	NUM [8]	NUM [7]	NUM [6]	NUM [5]	NUM [4]	NUM [3]	NUM [2]	NUM [1]	NUM [0]
	Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INT	0x02	CP1 [2]	CP1 [1]	CP1 [0]	INT [14]	INT [13]	INT [12]	INT [11]	INT [10]	INT [9]	INT [8]	INT [7]	INT [6]	INT [5]	INT [4]	INT [3]	INT [2]	INT [1]	INT [0]
	Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DIV	0x03	0	INTE	CP HiZ	DITH	LDCKSEL[1]	LDCKSEL[0]	LD	CP POLA	PRE [1]	PRE [0]	R1 [7]	R1 [6]	R1 [5]	R1 [4]	R1 [3]	R1 [2]	R1 [1]	R1 [0]
	Initial value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
CP_FAST	0x04	0	FAST EN	CP2 [2]	CP2 [1]	CP2 [0]	FAST [12]	FAST [11]	FAST [10]	FAST [9]	FAST [8]	FAST [7]	FAST [6]	FAST [5]	FAST [4]	FAST [3]	FAST [2]	FAST [1]	FAST [0]
	Initial value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
NSQ	0x05	VTSEL [1]	VTSEL [0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OFFSET	0x06	OFST [17]	OFST [16]	OFST [15]	OFST [14]	OFST [13]	OFST [12]	OFST [11]	OFST [10]	OFST [9]	OFST [8]	OFST [7]	OFST [6]	OFST [5]	OFST [4]	OFST [3]	OFST [2]	OFST [1]	OFST [0]
	Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IFBPF	0x07	AGC_KEEP	AGCLVL_H[2]	AGCLVL_H[1]	AGCLVL_H[0]	AGCLVL_L[2]	AGCLVL_L[1]	AGCLVL_L[0]	CAL	AGC_FAST	AGC_TIME[1]	AGC_TIME[0]	AGC1_STEP	AGC_OFF	BPF_BW [2]	BPF_BW [1]	BPF_BW [0]	LOFREQ [1]	LOFREQ [0]
	Initial value	0	1	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0	1
PGA	0x08	PGA0_LG	PGA2_G [4]	PGA2_G [3]	PGA2_G [2]	PGA2_G [1]	PGA2_G [0]	PGA1_G [5]	PGA1_G [4]	PGA1_G [3]	PGA1_G [2]	PGA1_G [1]	PGA1_G [0]	PGA0_ [2]	PGA0 [1]	PGA0 [0]	IFOG [2]	IFOG [1]	IFOG [0]
	Initial value	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1
SRST	0x09	0	0	0	0	0	0	0	0	0	0	SRST [7]	SRST [6]	SRST [5]	SRST [4]	SRST [3]	SRST [2]	SRST [1]	SRST [0]
	Initial value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PD	0x0A	0	RSSIMD	0	AGC_KEEP_SEL	SDATAOUT_OE	FMIX_IP3	DISLPF_G [2]	DISLPF_G [1]	DISLPF_G [0]	FMIX_HV	PDTRI_N	BS[2]	BS[1]	BS[0]	PDSYNTH_N	PDADC_N	PDFSTMIX_N	BSSEL_FMIX
	Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
PD_AGCG	0x0B								R_AGC1_G[5]	R_AGC1_G[4]	R_AGC1_G[3]	R_AGC1_G[2]	R_AGC1_G[1]	R_AGC1_G[0]	R_AGC2_G[4]	R_AGC2_G[3]	R_AGC2_G[2]	R_AGC2_G[1]	R_AGC2_G[0]
	Initial value								–	–	–	–	–	–	–	–	–	–	–

Note1) Writing into address 0x01 is enabled when writing into address 0x02 is performed. Be sure to write into address 0x01 first and then address 0x02.
Note2) The initial register values are not defined. Therefore, even after [PDN] is set to “High”, each bit initial value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.
Note3) Do not access the data except specified address 0x0c to 0x1F.

Address 0x01

Note) Writing into address 0x01 is enabled when writing into address 0x02 is performed.

NUM[17:0] **: Set the numerator in 2's complementary representation.**

Address 0x02

CP1[2:0]**: Sets the current value for the charge pump in normal operation (Charge Pump 1).**
Charge Pump 1 current is determined by the following formula:
CP1_min = 0.57 / Resistance connected to the [BIAS] pin
Charge Pump 1 current = CP1_min × (CP1 setting + 1)

	Charge Pump 1 current [uA]		
CP1[2:0]	22kΩ	27 kΩ	33 kΩ
000	25.9	21.1	17.3
001	51.8	42.2	34.5
010	77.7	63.3	51.8
011	103.6	84.4	69.1
100	129.5	100.6	86.4
101	155.5	126.7	103.6
110	181.4	147.8	120.9
111	207.3	168.9	138.2

INT[14:0] **: Sets the integer.**

When {PRE[1:0]} ="00", P = 4 is selected and then an integer from 48 to 8191 can be set.
When {PRE[1:0]} ="01", P = 8 is selected and then an integer from 116 to 16383 can be set.
When {PRE[1:0]} ="10" or "11", P = 16 is selected and then an integer from 348 to 32767 can be set.

Address 0x03

INTE **: INTEGER mode**
0 : Disable
1 : Enable (The delta-sigma circuit is integer mode operation.
Don't use DFM operation.)

CPHIZ **: Selects normal or TRI-STATE for the CP1/CP2 output.**
0 : Charge pumps are activated. (Use this setting for normal operation.)
1 : TRI-STATE (The charge pump output is put in the high-impedance (Hi-Z) state.)

DITH **: Selects dithering ON or OFF for a delta-sigma circuit.**
0 : DITH OFF (Low Noise mode)
1 : DITH ON (Low Spurious mode)
When OFFSET register is used, set DITH=0(OFF).

LDCKSEL[1:0] **: Sets phase error values for lock detect.**

When DITH="1" :
VCO frequency > [REFIN] pin input frequency / [LDCKSEL[1:0] setting + 1] × 7
When DITH="0" :
VCO frequency > [REFIN] pin input frequency / [LDCKSEL[1:0] setting + 1] × 4

"00" : 1 cycle of the REFIN clock (This cannot be used for the reference dividing ratio ≤ 3.)
"01" : 2 cycle of the REFIN clock (This cannot be used for the reference dividing ratio ≤ 5.)
"10" : 3 cycle of the REFIN clock (This cannot be used for the reference dividing ratio ≤ 6.)
"11" : 1 cycle of the REFIN clock (This must be used for the reference dividing ratio = 3)

LD **: Selects analog or digital for the lock detect.**

0 : Digital Lock Detect
1 : Analog Lock Detect

CPPOLA **: Selects positive or negative output polarity for Charge Pump1 and Charge Pump2.**

0 : Positive
1 : Negative

PRE[1:0] **: Selects a dividing ratio for the prescaler.**

"00" : P=4
"01" : P=8
"10" : P=16
"11" : P=16

R1[7:0] **: Sets a dividing ratio for the reference clock.**

This can be set in the range from 3 (3 divisions) to 255 (255 divisions). 0 to 2 cannot be set.

Address 0x04

FASTEN **: Enables or disables the Fast Lockup mode. FAST**

0 : The switchover settings specified in CP2[2:0] and FAST[12:0] are disabled.
1 : The switchover settings specified in CP2[2:0] and FAST[12:0] are enabled.

CP2[2:0] **: Sets the current value for the charge pump for the Fast Lockup mode**

(Charge Pump 2).
Charge Pump 2 current is determined by the following formula:
CP2_min = 0.57 / Resistance connected to the [BIAS] pin
Charge Pump 2 current = CP2_min × (CP2 setting + 4) [mA]

	Charge Pump 2 current [mA]		
CP2[2:0]	33kΩ	27 kΩ	22 kΩ
000	0.69	0.84	1.04
001	0.86	1.06	1.30
010	1.04	1.27	1.55
011	1.21	1.48	1.81
100	1.38	1.69	2.07
101	1.55	1.90	2.33
110	1.73	2.11	2.59
111	1.90	2.32	2.85

FAST[12:0] **: Sets the FAST counter value.**

A decimal number from 1 to 8191 can be set. This counter value is used to set the time period during which the charge pump for the Fast Lockup mode is ON.
The charge pump for the Fast Lockup mode is turned OFF after the time period calculated by [this count value x phase detector frequency cycle]. 0 cannot be set.

Address 0x05

VTSEL[1:0] **:Sets the noise detection level of noise squelch circuit.**

00 : 0.4V/0.5V (default)　　01 : 0.8V/0.9V
10 : 1.1V/1.2V　　11 : 1.4V/1.5V

Address 0x06

OFST[17:0] **: Set the adjustable frequency offset in 2's complementary representation.**

OFFSET register must be written at the speed calculated by "1/3.5*RF Frequency/(INT+7)". If the writing speed is faster than this, the setting isn't valid.
This register is offset from carrier frequency.
After this register is accessed, NUM[17:0] and INT[14:0] are recalculated and their recalculated data are used in delta-sigma and N-divider. When this register is not used, this register must be written 00000 (hexadecimal).
When OFFSET register is used, set DITH=0(OFF).

Address 0x07

AGC_KEEP **: The function of AGC1/2 gain keeping**

When the AGC function is active, the gain setting of AGC1/2 is kept during {AGC_KEEP}=1. On the other hand, the gain setting of AGC1/2 is changed by IFIP signal during {AGC_KEEP}=0.

0 : the gain setting of AGC1/2 is changed by IFIP signal. (default)
1 : the gain setting of AGC1/2 is kept.

AGCLVL_H[2:0]**: Setting the upper limit of AGC threshold level.**

AGCLVL_H [2]	AGCLVL_H [1]	AGCLVL_H [0]	upper limit
0	0	0	-5dB
0	0	1	-4dB
0	1	0	-3dB
0	1	1	-2dB
1	0	0	-1dB
1	0	1	0dB (default)
1	1	0	1dB
1	1	1	2dB

AGCLVL_L[2:0]: Setting the lower limit of AGC threshold level.

AGCLVL_L [2]	AGCLVL_L [1]	AGCLVL_L [0]	lower limit
0	0	0	-8dB
0	0	1	-6dB
0	1	0	-4dB
0	1	1	-2dB
1	0	0	0dB (default)
1	0	1	1dB
1	1	0	2dB
1	1	1	3dB

Note 1) When the AGC1/2 output level is bigger than the upper limit value, AGC1/2 gain is decreased. When the AGC1/2 output level is smaller than the lower limit value, AGC1/2 gain is increased. The upper/lower limit level is tunable based on default setting limit value.
Note 2) When AGC function is active ({AGC_OFF}=0), AGC1/2 works as Note1..

CAL **: Discriminator circuit calibration start trigger Discriminator**

0 : Invalid
1 : Start

Note) : Calibration is performed synchronized with the rising edge of {CAL}.
After calibration completed, this register is set to "0" automatically. It takes 1.3ms before calibration is completed. Refer to "calibration procedure" for further information.

AGC_FAST **: AGC control switching**

0 : AGC control is operated with AGC response time described in AGC_TIME[1:0].
1 : The time constant of response time is changed by conditions that AGC1/AGC2 output level converges between the upper limit and lower limit(convergence) or not(attack/release).
attack/release : AGC response time is the same as AGC_TIME="00".
convergence : AGC response time is set with ACG_TIME[1:0].
This setting provides the fast response time that can be followed the burst signal. (default)

AGC_TIME[1:0] **: AGC response time setting**

This register set response time for AGC1 gain and AGC2 gain to change by 1step.

AGC_TIME [1]	AGC_TIME [0]	AGC response time [ms]					
		AGC1_STEP=0 setting			AGC1_STEP=1 setting		
		State A	State B	State C	State A	State B	State C
0	0	(0.6)	(8.5)	(8.5)	(0.4)	(4.4)	(4.4)
0	1	(67)	(95)	(95)	(34)	(58)	(58)
1	0	(134)	(182)	(182)	(67)	(111)	(111)
1	1	(267)	(355)	(355)	(134)	(218)	(218)

Note) : Values above indicate response time during AGC gain changes from maximum to minimum or from minimum to maximum.

State A: AGC1 output level is beyond the upper limit.
State B: AGC1 output level is within the upper limit and AGC2 output level is beyond the upper limit.
State C: AGC2 output level is under the lower limit.

AGC1_STEP **: AGC1 gain switching range setting**

0 : ±1dB
1 : ±2dB (default)

AGC_OFF **: AGC ON/OFF setting**

0 : ON (default)
1 : Off

BPF_BW[2:0] **: BPF band width setting**

BPF_BW [2]	BPF_BW [1]	BPF_BW [0]	Name	6dB attenuation	Attenuation band width	Remarks
1	0/1	0/1	F0	±7.5kHz	±15kHz (within 50dB)	
0	0	0	F1	±6kHz	±12.5kHz (within 50dB)	
0	0	1	F2	±4.5kHz	±11kHz (within 50dB)	
0	1	0	F3	±3kHz	±9kHz (within 50dB)	
0	1	1	F4	±2kHz	±7kHz (within 50dB)	8dB attenuation at F4 : ±2kHz

LOFREQ[1:0] **: Local frequency setting**

LOFREQ [1]	LOFREQ [0]	Local Frequency
0	0	45.9MHz
0	1	50.4MHz
1	0	57.6MHz
1	1	28.8MHz

Address 0x08

PGA0[2:0]**: Gain setting of PGA0+2nd MIX**

PGA0[2]	PGA0[1]	PGA0[0]	PGA0+2nd MIX gain [dB]
0	0	0	(42)
0	0	1	(44)
0	1	0	(46)
0	1	1	(48) (default)
1	0	0	(50)
1	0	1	(52)
1	1	0	(54)
1	1	1	(56)

Note) Test circuit is shown Figure 8 on page 15.

PGA0_LG**: When {PGA0_LG}=1, PGA0+2nd MIX gain is fixed 28dB regardless of {PGA0[2:0]}.**

0 : PGA0+2nd MIX gain is controlled by setting of {PGA0[2:0]} (default)

1 : PGA0+2nd MIX gain is 28dB fixed regardless of setting of {PGA0[2:0]}.

PGA2_G[4:0] **: When AGC_OFF="1", AGC2 gain setting is available.**

PGA2_G[4]	PGA 2_G[3]	PGA 2_G[2]	PGA 2_G[1]	PGA 2_G[0]	Gain[dB]
0	1	1	0	0	12
0	1	0	1	1	11
0	1	0	1	0	10
0	1	0	0	1	9
0	1	0	0	0	8
0	0	1	1	1	7
0	0	1	1	0	6
0	0	1	0	1	5
0	0	1	0	0	4
0	0	0	1	1	3
0	0	0	1	0	2
0	0	0	0	1	1
0	0	0	0	0	0

Note: Do not set the combination of the code which is not defined in the table given above.

PGA1_G[5:0] **: When AGC_OFF="1", AGC1 gain setting is available.**

PGA1_G[5]	PGA1_G[4]	PGA1_G[3]	PGA1_G[2]	PGA1_G[1]	PGA1_G[0]	Gain[dB]
0	1	0	1	0	1	21
0	1	0	1	0	0	20
0	1	0	0	1	1	19
0	1	0	0	1	0	18
0	1	0	0	0	1	17
0	1	0	0	0	0	16
0	0	1	1	1	1	15
0	0	1	1	1	0	14
0	0	1	1	0	1	13
0	0	1	1	0	0	12
0	0	1	0	1	1	11
0	0	1	0	1	0	10
0	0	1	0	0	1	9
0	0	1	0	0	0	8
0	0	0	1	1	1	7
0	0	0	1	1	0	6
0	0	0	1	0	1	5
0	0	0	1	0	0	4
0	0	0	0	1	1	3
0	0	0	0	1	0	2
0	0	0	0	0	1	1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
1	1	1	1	1	0	-2
1	1	1	1	0	1	-3
1	1	1	1	0	0	-4
1	1	1	0	1	1	-5
1	1	1	0	1	0	-6
1	1	1	0	0	1	-7
1	1	1	0	0	0	-8
1	1	0	1	1	1	-9
1	1	0	1	1	0	-10
1	1	0	1	0	1	-11
1	1	0	1	0	0	-12
1	1	0	0	1	1	-13
1	1	0	0	1	0	-14
1	1	0	0	0	1	-15
1	1	0	0	0	0	-16
1	0	1	1	1	1	-17
1	0	1	1	1	0	-18
1	0	1	1	0	1	-19

Note: Do not set the combination of the code which is not defined in the table given above.

IFOG[2:0] **: IFBUF Gain setting.**

IFOG [2]	IFOG [1]	IFOG [0]	IFBUF Gain[dB]
0	0	0	0
0	0	1	3 (default)
0	1	0	6
0	1	1	9
1	0	0	12
1	0	1	15

Address 0x09

Software-reset

When data 0x09:10101010 is written to the SRST[7:0] register, software reset is performed.

Address 0x0A

PDN,BS[2:0] **: 2nd IF Block Operation mode setting**

PDN	BS [2]	BS [1]	BS [0]	Mode name	LDO D	LDOA, AGNDI N	LOBUF , VIREF	2nd MIX ～SMF, DIV, AGCCNT	IFBU F	LIMITE R, RSSI	DISCRI, Noise Squelch
0	-	-	-	Mode0 (Power Down0)	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	1	Mode1 (Note 1)	ON	OFF	OFF	OFF	OFF	OFF	OFF
1	0	1	0	Mode2 (Initial value)	ON	ON	OFF	OFF	OFF	OFF	OFF
1	0	1	1	Mode3	ON	ON	ON	OFF	OFF	OFF	OFF
1	1	0	0	Mode4	ON	ON	ON	ON	ON	OFF	OFF
1	1	0	1	Mode5	ON	ON	ON	ON	ON	ON	OFF
1	1	1	0	Mode6	ON	ON	ON	ON	OFF	ON	ON
1	1	1	1	Mode7	ON	ON	ON	ON	ON	ON	ON

Note 1) : Do not use Mode1.

Note 2) : Do no set the combination of the code which is not defined in the table given above.

DISLPF_G[2:0]: **Setting of the demodulation output level**

DISLPF_G[2]	DISLPF_G [1]	DISLPF_G [0]	Demodulation output level when ±1.5kHz dev. signal input
0	0	1	100mVrms
0	1	0	200mVrms
0	1	1	300mVrms
1	0	1	50mVrms
1	1	0	100mVrms
1	1	1	150mVrms

Note) The demodulation output level (±1.5kHz dev. signal input, AUDIOOUT pin output) can be set to 50mVrms typ. to 300mVrms typ. by setting of {DISLPF_G[2:0]}.

Note) Do no set the combination of the code which is not defined in the table given above.

***AGC_KEEP_SEL*: Select AGC function of gain keeping**

This register set the control way of the function of gain keeping.

0 : Control by the register {AGC_KEEP} setting (default)
1 : Control by the pin of AGC_KEEP

***SDATAOUT_OE*: Select output signal of DETO/SDATAOUT pin**

The signal of DETO or SDATAOUT can be output from DETO/SDATAOUT pin.

0 : DETO signal output (default)
1 : SDATAOUT signal output

***FMIX_IP3*: NF/IIP3 priority select of 1st Mixer**

IIP3 performance of 1st Mixer is improved by setting {FMIX_IP3}=1 without more supply current. Then Current Adjustment Resistor (BIAS1/2) must be used < 47kΩ. If NF performance is more important than IIP3, setting {FMIX_IP3}=0.

0 : NF performance is preference (default)
1 : IIP3 performance improvement

***FMIX_HV*: High IIP3 mode of 1st Mixer**

IIP3 performance of 1st Mixer is improved by adjustment of BIAS1/2 resistance and setting {FMIX_HV}="1". When FMIX_HV="1" setting, MIXVDD must be set more than 4.5V.

0 : BIAS1/2 ≥ 39kΩ (default)
1 : 18kΩ ≤ BIAS1/2 < 39kΩ

***PDTRI_N*: Tripler circuit On/Off**

REFIN signal can be input from LO2NDIN pin by setting tripler circuit off.
Then REFIN input is one third of the 2nd LO input frequency.

0 : Off (default)
1 : On

***PDSYNTH_N*: SYNTH On/Off**

0 : Off (default)
1 : On

***PDADC_N*: ADC On/Off**

0 : Off (default)
1 : On

***PDFSTMIX_N*: 1st MIXER On/Off**

0 : Off (defaut)
1 : On

***BSSEL_FMIX*: Bias resistance select**

0 : BIAS2 pin is enable (default)
1 : BIAS1 pin is enable

Address Ox0B

***R_AGC1_G[5:0]*: Read the gain setting of AGC1 when {AGC_OFF}=0**
***R_AGC2_G[4:0]*: Read the gain setting of AGC2 when {AGC_OFF}=0**

Block Diagram (PLL SYNTH)

The AK2400 is a Delta-Sigma Fractional-N PLL (Phase Locked Loop) frequency synthesizer with a frequency switching function, covering a wide range of frequencies from 10 to 1000MHz. This product consists of an 18-bit Delta-Sigma modulator, a low-noise phase frequency comparator, a highly accurate charge pump, a reference divider, dual-module prescaler (P/P+1) and frequency offset adjustable circuits. An excellent PLL can be achieved by combining this synthesizer with the external loop filter and VCO (Voltage Controlled Oscillator). The operating supply voltage is from 2.7 to 5.5V; and the charge pump and serial interface can be driven by individual supply voltages.

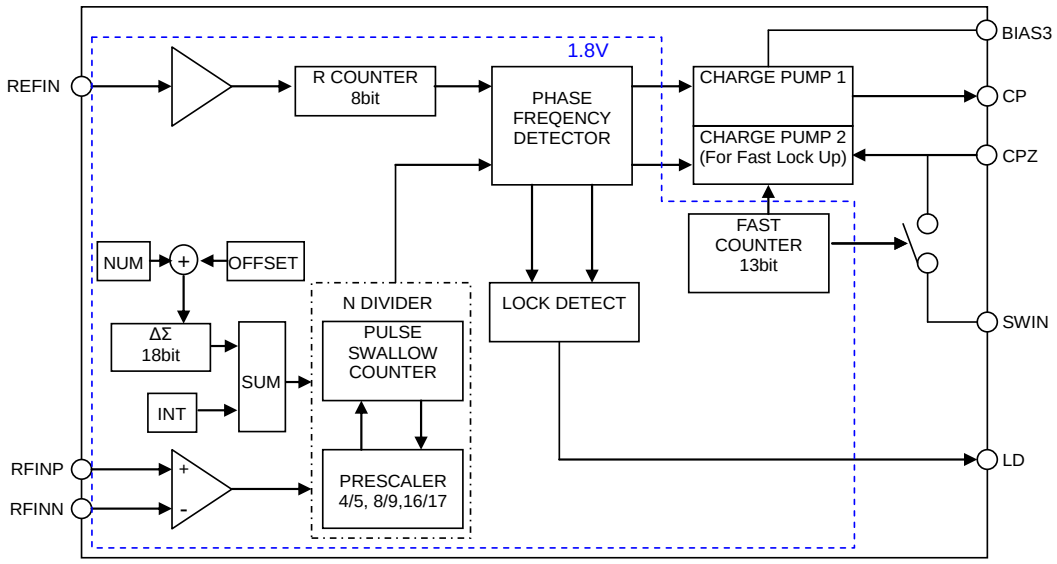


Figure 9 Block Diagram (PLL SYNTH)

Lock Detect function (PLL SYNTH)

In AK2400, “lock detect” output can be selected by D[11] = {LD} in <Address3>. When {LD} is set to “1”, the phase frequency detector output provides a phase detection status as an analog level (comparison result). This is called “Analog Lock Detect”. When {LD} is set to “0”, the lock detect signal outputs according to the on-chip logic. This is called “Digital Lock Detect”.

Analog Lock Detect
In analog lock detect, the phase frequency detector output comes from the [LD] pin.

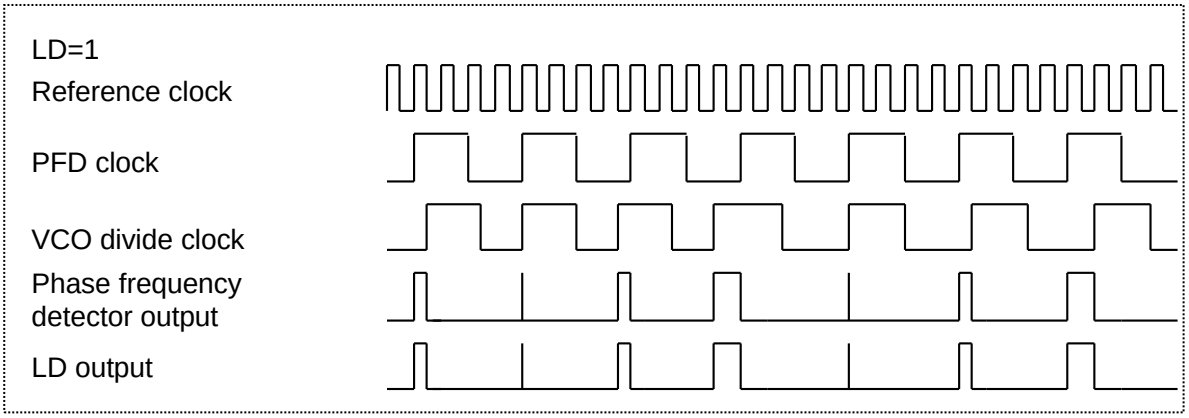


Figure 10 Analog Lock Detect

Digital Lock Detect
In the digital lock detect, the LD pin outputs ”Low” every time when the frequency is set. And the LD pin outputs is “High” (which means the locked state) when a phase error smaller than T is detected for 63 times consecutively. If the phase error is larger than T is detected for 63 times consecutively when the LD pin outputs “High”, the LD pin outputs “Low”(which means the unlocked state).

The accuracy of the phase detect is set by LDCKSEL[1:0].
“00” : 1 cycle of the REFIN clock (This cannot be used for the reference dividing ratio ≤ 3.)
“01” : 2 cycle of the REFIN clock (This cannot be used for the reference dividing ratio ≤ 5.)
“10” : 3 cycle of the REFIN clock (This cannot be used for the reference dividing ratio ≤ 6.)

Since the AK2400 is a Delta-Sigma Fractional-N type, a phase error up to 7 times larger than the VCO period frequency may occur in the phase frequency detector. Therefore the LDCKSEL[1:0] setting should be large enough to cover the amplitude of the Delta-Sigma Fractional frequency. However, if the VCO frequency does not satisfy either of the following formula, the digital lock detect cannot be used. In such case, the analog lock detect should be used.

When {DITH} = D[14] in <Address3> is set to ”1” (DITH ON):
VCO frequency > [REFIN] pin input frequency / [LDCKSEL[1:0] setting + 1] × 7
When {DITH} = D[14] in <Address3> is set to “0” (DITH OFF):
VCO frequency > [REFIN] pin input frequency / [LDCKSEL[1:0] setting + 1] × 4

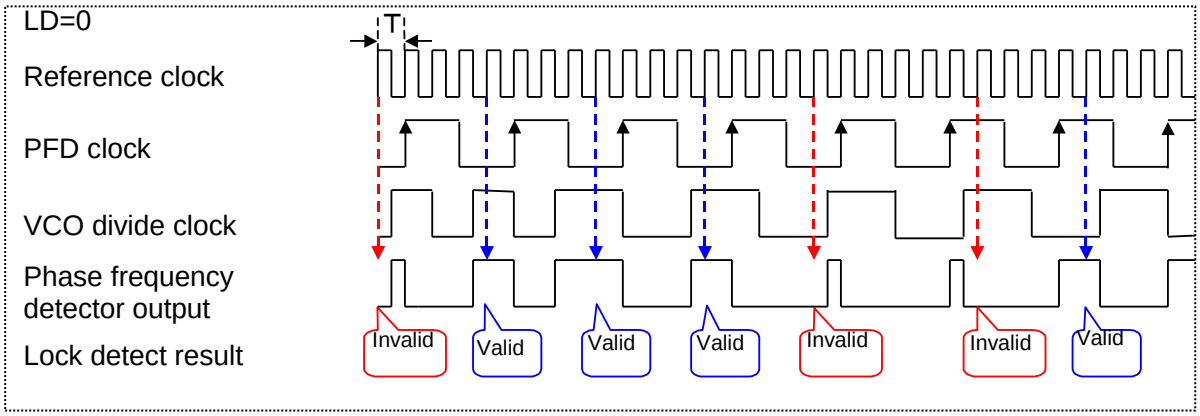


Figure 11 Digital Lock Detect

Transition Flow Chart: Unlock State to Lock State

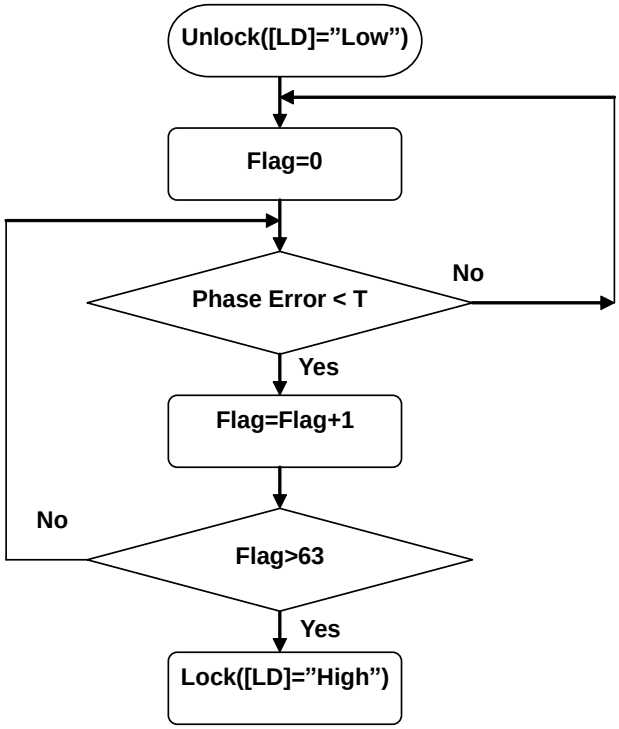


Figure 12-1 Unlock State to Lock State

Transition Flow Chart: Lock State to Unlock State

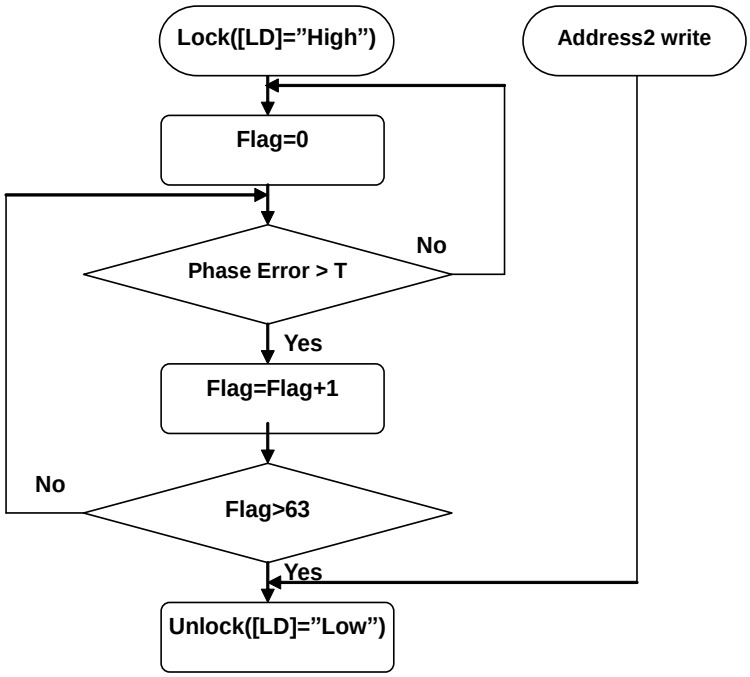


Figure 12-2 Digital Lock Detect

Frequency Setting (PLL SYNTH)

Frequency Setup

AK2400 is a Fractional-N type synthesizer that takes 2^{18} as the denominator, which calculates the integer and numerator to be set using the following formulas:

$$\text{Frequency setting} = F_{PFD} \times (\text{Integer} + \text{Numerator} / 2^{18})$$
$$\text{Integer} = \text{ROUND}(\text{Target Frequency} / F_{PFD})$$
$$\text{Numerator} = \text{ROUND}\{(\text{Target Frequency} - \text{Integer} \times F_{PFD}) / (F_{PFD} / 2^{18})\}$$

Note)
ROUND: Rounded off to the nearest integer
F_{PFD} : Phase Frequency Detector comparative Frequency ([REFIN] pin input frequency / R divider ratio)

Calculation examples

Example 1) The numerator is positive when the target frequency is 950.0375MHz and the Phase Frequency Detector comparative Frequency is 1MHz.

Integer = 950.0375MHz / 1MHz = 950.0375
It is rounded off to 950 (decimal) = 3B6 (hexadecimal) = 0011 1011 0110 (binary)
Numerator = (950.0375MHz - 950 × 1MHz) / (1MHz / 2^{18}) = 9830.4
It is rounded off to 9830 (decimal) = 2666 (hexadecimal) = 10 0110 0110 0110 (binary)
Frequency setting =1MHz × (950 + 9830 / 2^{18}) = 950.0374985MHz
(In this case the error between the calculated frequency and the target frequency is 1.5Hz.)

Example 2) The numerator is negative when the target frequency is 950.550MHz and the Phase Frequency Detector comparative Frequency is 1MHz.

Integer = 950.550MHz / 1MHz = 950.550
It is rounded off to 951 (decimal) = 3B7 (hexadecimal) = 0011 1011 0111 (binary)
Numerator = (950.550MHz - 951 × 1MHz) / (1MHz / 2^{18}) = -117964.8
It is rounded off to -117965 (decimal), which is deduced from 2^{18} to be converted into binary for 2's complementary expression.
2^{18} - 117965 (decimal) = 144179 (decimal) = 23333 (hexadecimal) = 10 0011 0011 0011 0011 (binary)
Frequency setting =1MHz × (951 + (-117965/2^{18})) = 950.5499992MHz
(In this case the error between the calculated frequency and the target frequency is 0.8Hz.)

Frequency switching adjustment (PLL SYNTH)

AK2400 has an offset adjustable register which can tune the carrier frequency set by {NUM[17:0]} in <Address1>
and {INT[14:0]} in <Address2>. When the offset register: {OFST[17:0]} in <Address6> is accessed, {NUM[17:0]} and {INT[14:0]} are recalculated automatically and their recalculated data are used in delta-sigma and N-divider. This operation is suitable for AFC and DFM applications.
When frequency offset is not used, the offset register must be written 00000 (hexadecimal).
When OFFSET register is used, set DITH=0(OFF).

Setting examples

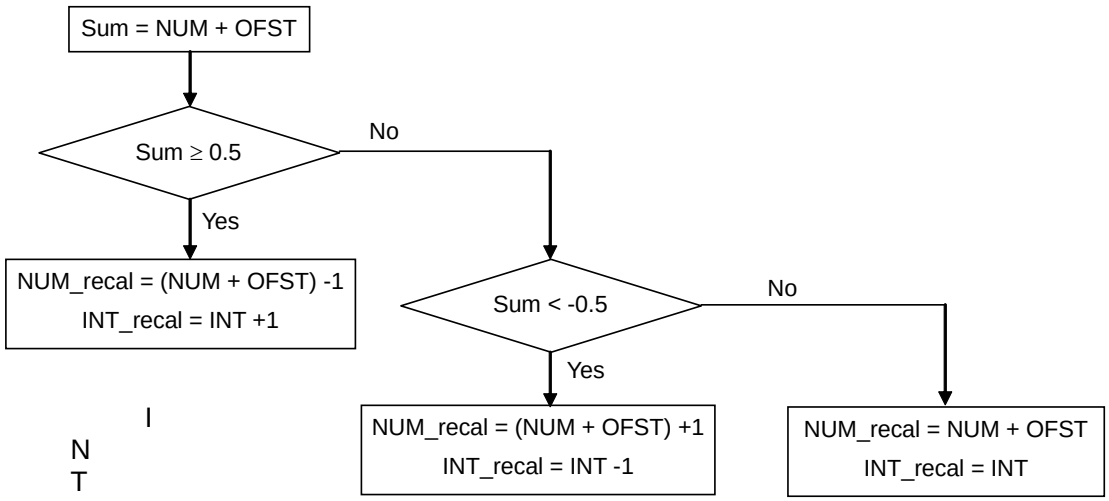
Example 1) The frequency offset is positive when the frequency offset is 100Hz and the Phase Frequency Detector comparative frequency is 1MHz.

Frequency offset = 100Hz / (1MHz/2^{18}) = 26.2
It is round off to 26 (decimal) = 1A (hexadecimal) = 11010 (binary)

Example 2) The frequency offset is negative when the frequency offset is -100Hz and the Phase Frequency Detector comparative frequency is 1MHz.

Frequency offset = -100Hz / (1MHz/2^{18}) = -26.2
It is round off to -26 (decimal), which is deduced from 2^{18} to be converted into binary for 2's complementary expression.
2^{18} – 26 = 262118 (decimal) = 3FFE6 (hexadecimal) = 11 1111 1111 1110 0110 (binary)

Algorithm of recalculation



written data in integer register {INT[14:0]}
NUM written data in numerator register {NUM[17:0]}
OFST written data in offset register {OFST[17:0]}
INT_recal recalculated integer data
NUM_recal recalculated numerator data

Figure 13 Frequency switching adjustment

Charge Pump and Loop Filter (PLL SYNTHE)

AK2400 has two charge pumps; Charge Pump 1 for normal operation and Charge Pump 2 for Fast Lockup mode. The internal timer is used to switch these two charge pumps to achieve a Fast Lock PLL.
The loop filter is external and connected to [CP], [SWIN] and [CPZ] pins. [CPZ] pin should be connected to R2 and C2, which are intermediate nodes, even if the Fast Lockup is not used. Therefore, R2 must be connected to [CP] pin, while C2 must be connected to the ground.
R2 and R2' are connected in parallel with internal switch in Fast Lockup. These R2 and R2' parallel resistance value is required for calculating loop bandwidth and phase margin in Fast Lockup operation.

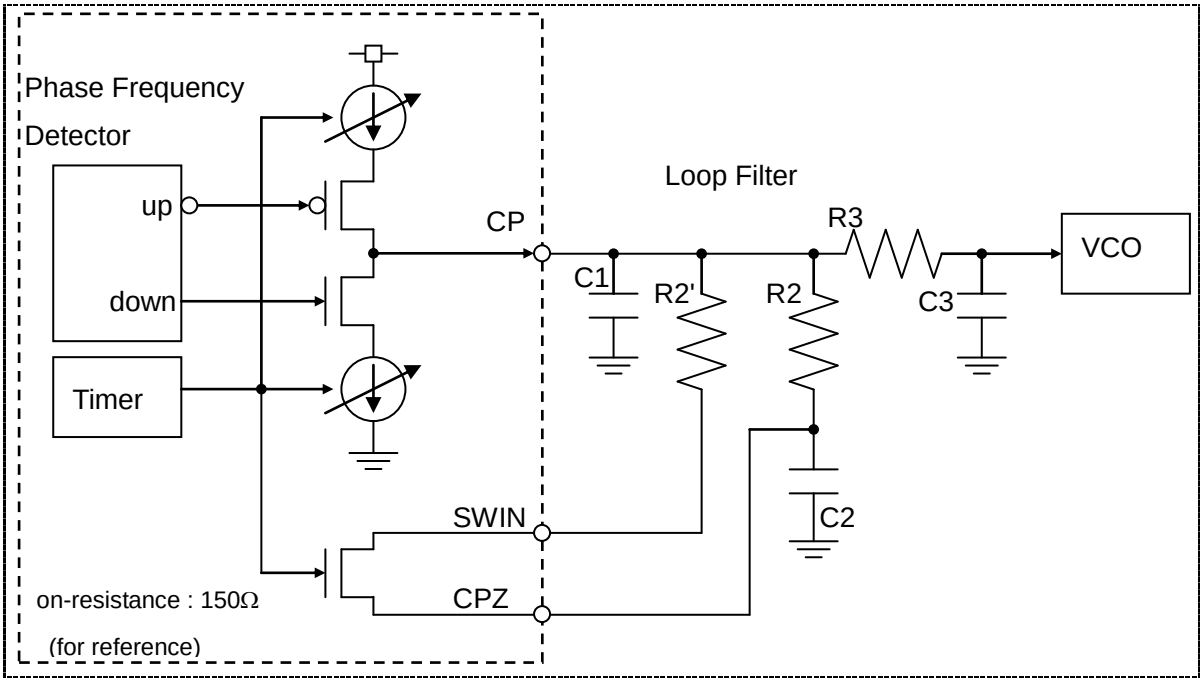


Figure 14 Charge pump and Loop Filter

Fast lock-up mode (PLL SYNTH)

Setting D[16] = {FASTEN} in <Address4> to “1” enables the Fast Lock Up mode for the AK2400
Changing a frequency setting (The frequency is changed at the rising edge of [CSN], when <Address1> and <Address2> are accessed.) or [PDSYNTH_N] pin is set from ”Low” to ”High” with {FASTEN}=1 enables the Fast Lockup mode. The loop filter switch turns ON during the timer period specified by the counter value in D[12:0] = {FAST[12:0]} in <Address4>, and the charge pump for the Fast Lockup mode (Charge Pump 2) is enabled. After the timer period elapsed, the loop filter switch turns OFF. The charge pump for normal operation (Charge Pump 1) is enabled. D[12:0] ={ FAST[12:0]} in <Address4> is used to set the timer period for this mode.
The following formula is used to calculate the time period:

Phase detector frequency cycle x counter value set in {FAST[12:0]}

The charge pump current can be changed with the register setting in 8 steps in normal operation (Charge Pump 1) and 8 steps in the Fast Lockup operation (Charge Pump 2).
The charge pump current for normal operation (Charge Pump 1) is determined by the setting in {CP1[2:0]}, which is a 3-bit address of D[17:15] in <Address2>, and a value of the resistance connected to the BIAS3 pin. The following formulas show the relationship between the resistance value, the register setting and the electric current value.

Charge Pump 1 minimum current (CP1_min) = 0.57 / Resistance connected to the BIAS3 pin
Charge Pump 1 current = CP1_min × ({CP1[2:0]} + 1)

The charge pump current for the Fast Lockup mode operation (Charge Pump 2 current) is determined by the setting in {CP2[2:0]}, which is a 3-bit address of D[15:13] in <Address4>, and a value of the resistance connected to the BIAS3 pin. The following formula show the relationship between the resistance value, the register setting and the electric current value.

Charge Pump 2 minimum current (CP2_min) = 5.7 / Resistance connected to the BIAS3 pin
Charge Pump 2 minimum current (CP2_min) = CP2_min × ({CP2[2:0]} + 4)

The allowed range value for the resistance (connected to the BIAS3 pin (19)) is from 22 to 33 [kΩ] for both normal and Fast Lockup mode operations.

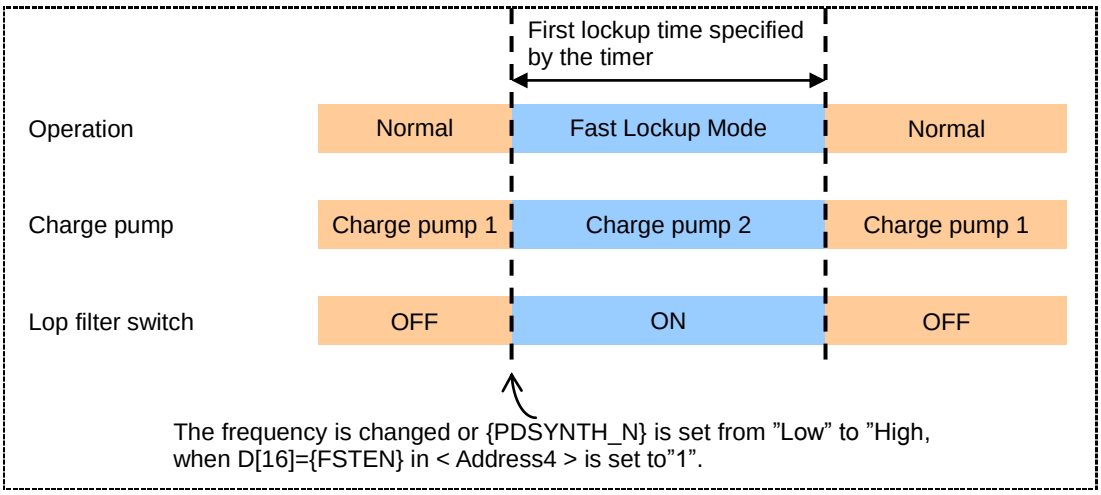


Figure 15 Timing Chart for Fast Lockup Mode

Calibration Procedure (Discriminator)

AK2400 employs a function to calibrate free-running frequency of VCO in Discriminator and demodulated signal level. Before starting RX Operation, calibration is required in order to acquire proper VCO operation range and demodulated signal level.

Following procedure is required before calibration.

<1> Start up the external TCXO and continuously supply LO signal to AK2400.
<2> Set “110” to 0x0A {BS[2:0]} and start up all circuits. After this operation, the circuits necessary for calibration (LOBUF, VIREF, Discriminator) will be powered on and calibration can be possible in 500us.
<3> Calibration is begun by setting "1" to address 0x07 {CAL}. When the calibration is executed once, the calibration operation cannot be stopped excluding master reset. Even if "0" is written in {CAL}, the calibration is completely executed.
<4> Calibration data is maintained excluding the time when the master reset is executed or DVDD power supply is down.
<5> It takes 1.5ms for Discriminator to become steady after the calibration is completed.

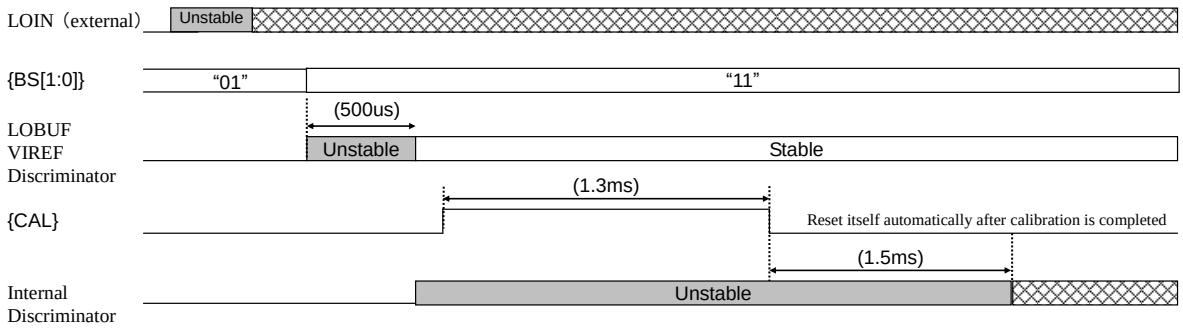


Figure 16 Power-up sequence recommendation

Typical Evaluation Board Schematic (PLL SYNTH)

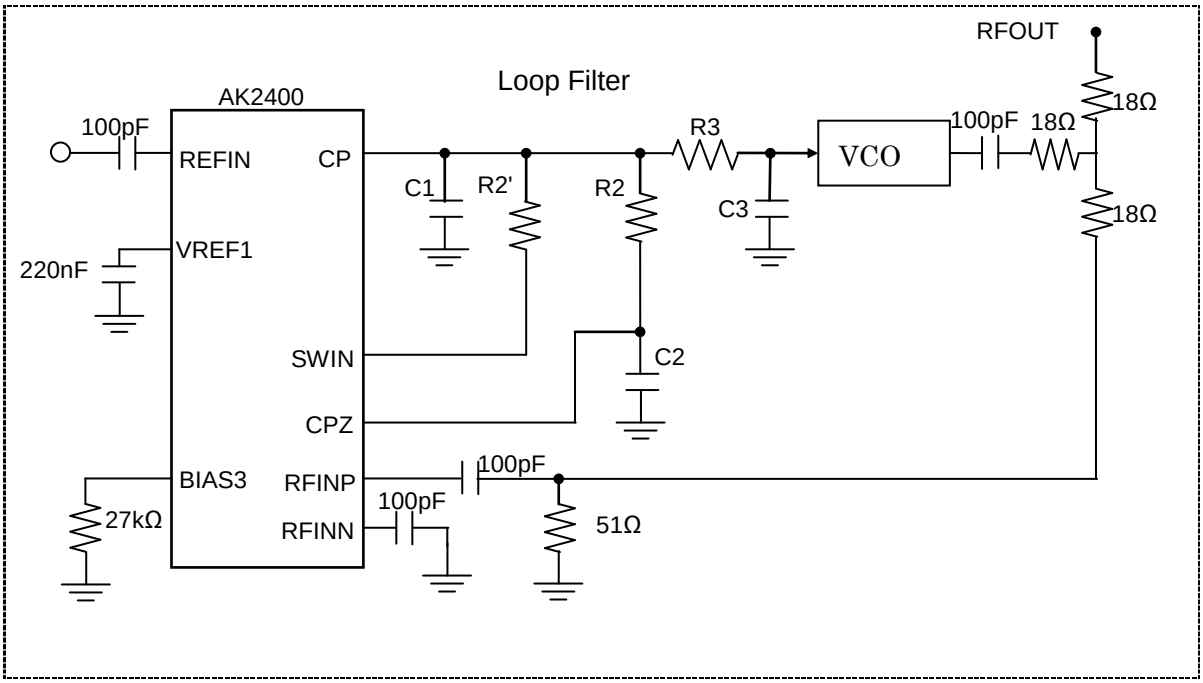


Figure 17 Typical Evaluation Board Schematic (PLL SYNTH)

[CPZ] pin should be connected to R2 and C2, which are intermediate nodes, even if the Fast Lockup feature is not used. For the output destination from [CPZ] pin, see “Charge Pump and Loop Filter” on page 36.

R2 and R2’ are connected in parallel with internal switch in Fast Lockup. These R2 and R2’ parallel resistance value is required for calculating loop bandwidth and phase margin in Fast Lockup. The on-resistance value of the internal switch is 150Ω for reference.

1. PVDD, CPVDD

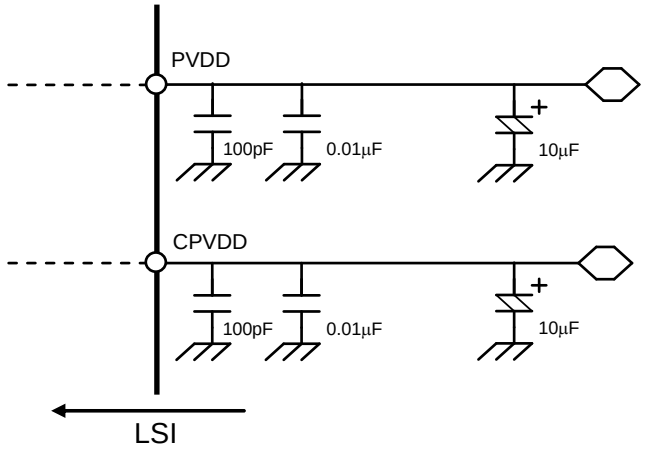
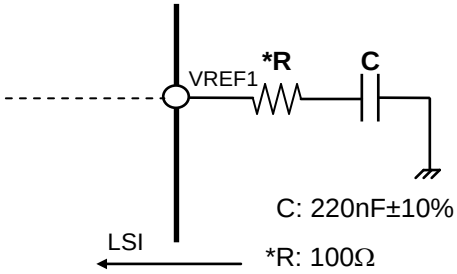


Figure 18 PVDD, CPVDD

2. VREF1



* Additional resistor for anti-noise characteristics of 1stMixer.

Figure 19 PVDD, CPVDD

3. REFIN

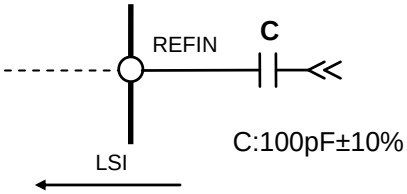
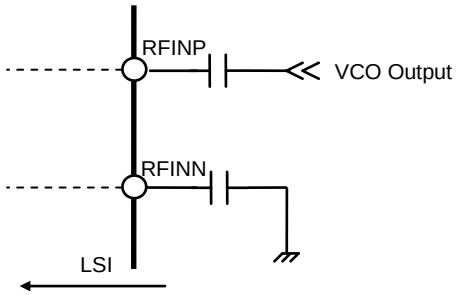


Figure 20 REFIN

4. RFINP, RFINN



Refer to typical Evaluation Board Schematic.

Figure 21 RFINP, RFINN

5. BIAS3

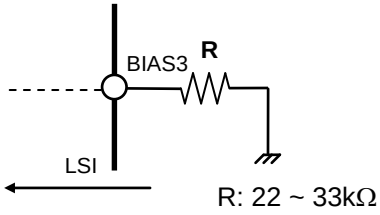


Figure 22 BIAS3

Typical Evaluation Board Schematic (1st MIXER)

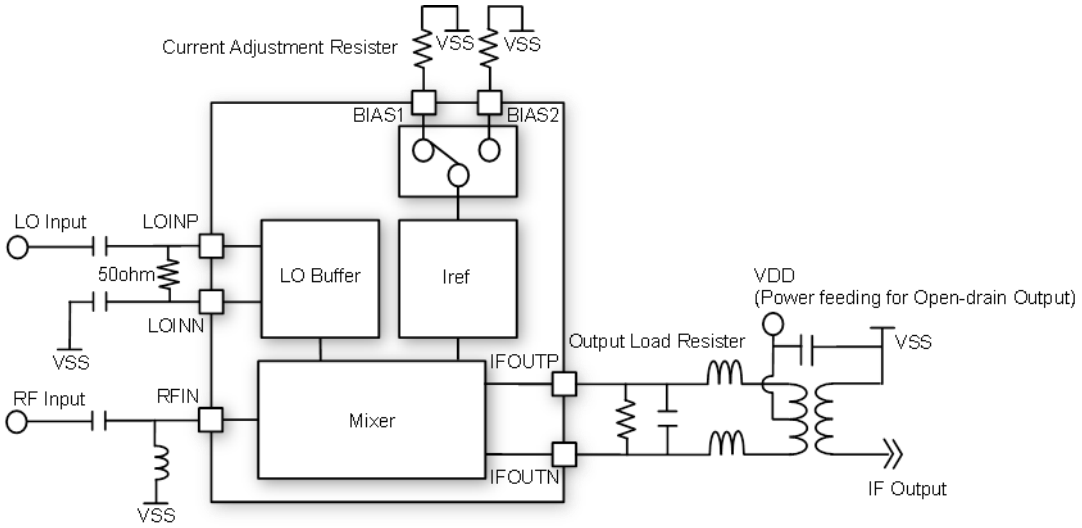


Figure 23 Typical Evaluation Board Schematic (1st MIXER)

Note 1) The exposed pad at the center of the backside should be connected to ground.
Note 2) The open drain output needs power feeding via a inductor. (IFOUTP pin and IFOUTN pin)
Note 3) It is necessary to adjust impedance matching as to its setting frequency. (RF input and IF output)
Note 4) If 1st Mixer is not used, each pin are terminated as below.
Register {BSSEL_FMIX}, {PDFSTIX_N}, {FMIX_HV} and {FMIX_IP3} on Address 0x0A must be set to 0

No.	Name	Terminating condition
1	RFIN	OPEN
2	AVSS1	VSS
3	IFOUTP	OPEN
4	IFOUTN	OPEN
5	MIXVDD	VSS
53	BIAS2	VSS
54	BIAS1	VSS
55	LOINP	OPEN
56	LOINN	OPEN

·Impedance matching network for RF Input pin

RF Input port with impedance matching network (highpass filter) is shown as below. Typical evaluation board component values in 50Ω interface are shown as below.

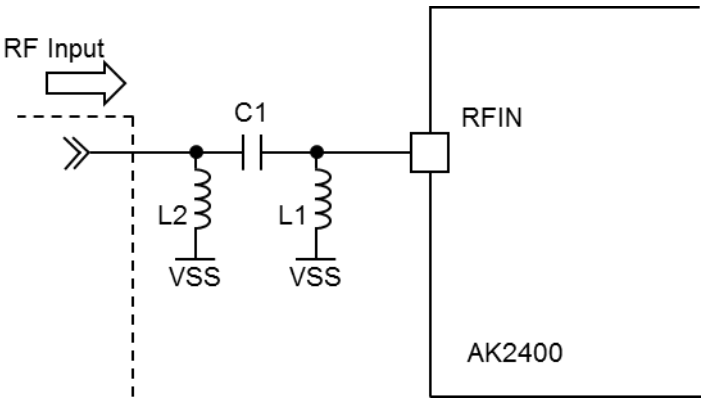


Figure 24 RF Input port with impedance matching network

RF Input Frequency [MHz]	C1 [pF]	L1 [nH]	L2 [nH]
70	82	200	-
160	39	100	-
300	18	33	-
600	18	33	-
900	18	33	-

·Impedance matching network for LO Input pin

LOIN port can be matched with resistive impedance matching network in 10MHz < LO Input < 2000MHz. Typical evaluation board component values in 50Ω interface is shown as below.

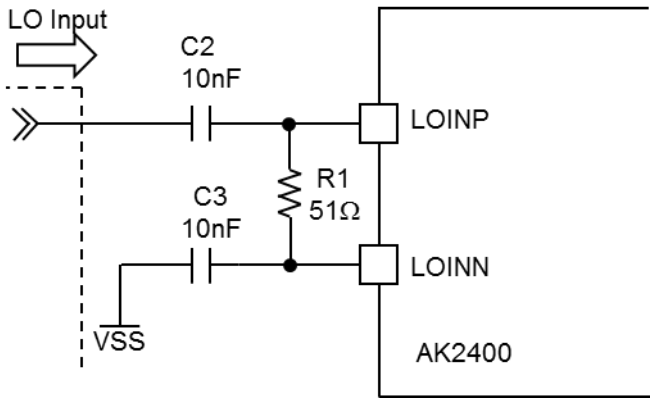


Figure 25 LO Input port with impedance matching network

·Impedance matching network for IF Output pin

IF output port with impedance matching network (lowpass filter and balun) is shown as below. IFOUTP and IFOUTN pins need power feeding via center tap of balun. Typical evaluation board component values in 50Ω interface are shown as below.

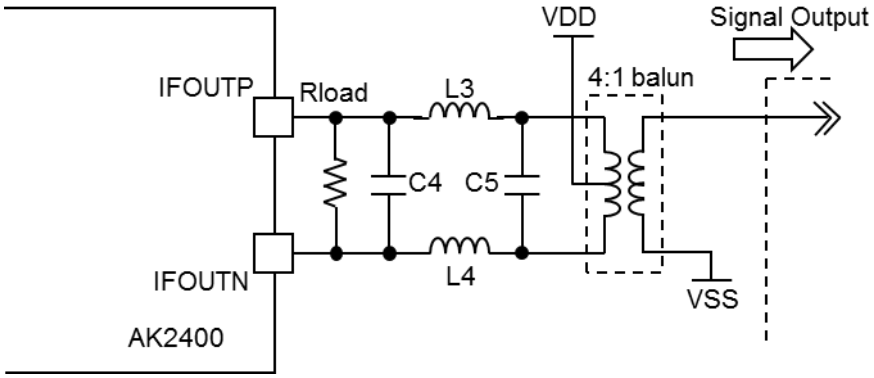


Figure 26 IF output port with impedance matching network

IF Output Frequency [MHz]	Rload [kΩ]	L3/L4 [nH]	C4 [pF]	C5 [pF]
29.25	2.2	1800	6	-
46.35	2.2	1000	3.3	-
50.85	2.2	1000	2.4	-
58.05	2.2	1000	1.6	-

·Impedance matching network with LC

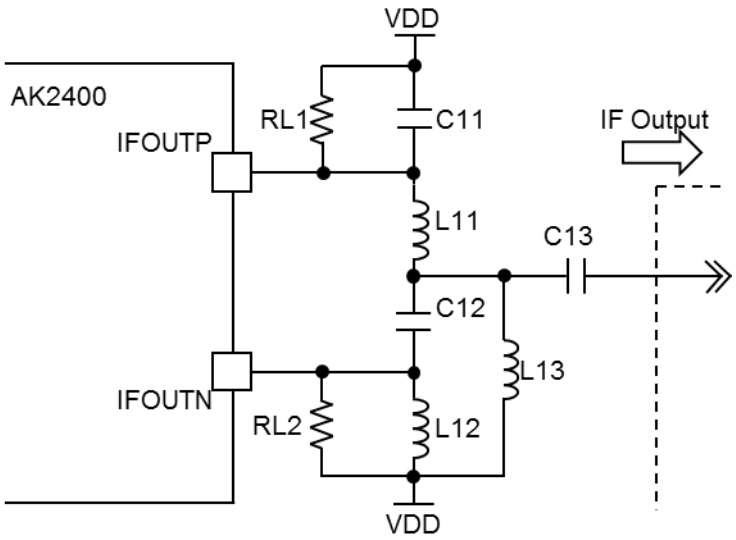


Figure 27 Impedance matching network with LC

Impedance matching network with LC is shown. AK2400 1st Mixer has open drain outputs, so RL1 + RL2 is output load resistance. C11and L11 compose lowpass filter. C12 and L12 are for highpass filter. C13 is DC blocking capacitor and L13 is RF choke. OUTP and OUTN pins need power feeding via L11, L12 and L13.

The differential voltage from IFOUTP/N can be converted to a single-ended by L11, L12, C11 and C12 properly. The differential impedance (RL1 + RL2) is converted to single-ended output terminating impedance Ro.

L11, C11, L12 and C12 are calculated as below. fout is IF output frequency.

$$C_{11} = C_{12} = \frac{1}{2\pi * f_{IF} * \sqrt{(R_{L1} + R_{L2}) * R_O}}$$

$$L_{11} = L_{12} = \frac{\sqrt{(R_{L1} + R_{L2}) * R_O}}{2\pi * f_{IF}}$$

For example, in the case of IF Output = 50MHz, Output Load Resistor (Rload) = 2.2kΩ in 50Ω interface, L11, C11, L12 and C12 are calculated as below.

$$C_{11} = C_{12} = \frac{1}{2\pi * (50 * 10\text{^}6) * \sqrt{(2.2 * 10\text{^}3) * 50}} = 9.6\text{pF}$$

$$L_{11} = L_{12} = \frac{\sqrt{(2.2 * 10\text{^}3) * 50}}{2\pi * (50 * 10\text{^}6)} = 1056\text{nH}$$

L13 and C13 should be large enough not to affect the impedance at IF output frequency. In some cases the impedance matching can be optimized by L13 and C13.

For example, in the case of IF Output = 50MHz, Output Load Resistor (Rload) = 2.2kΩ in 50Ω interface, it is recommended to choose 2200nH and 1000pF as L13 and C13. If any correction is needed, it can be adjusted by reducing the value of L13 and C13.

These calculated values are approximation. In some cases, some correction is needed due to the effect of parasitic capacitance of external parts or/and PCBs. The impedance matching network components should be decided through enough evaluation on AK2400.

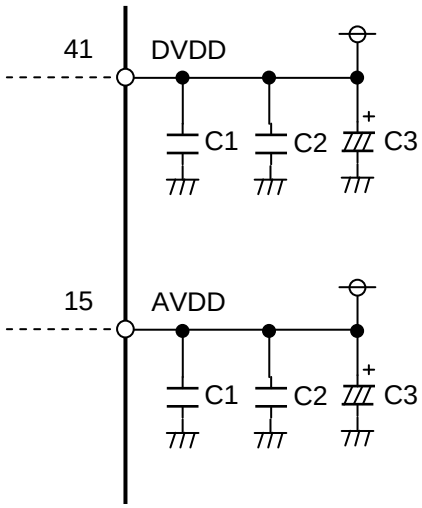
Typical evaluation board component values in 50Ω interface are shown as below.

IF Output Frequency [MHz]	RL1/RL2 [kΩ]	L11/L12 [nH]	C11/C12 [pF]	L13 [nH]	C13 [pF]
29.25	1.1	1800	15	2200	270
46.35	1.1	1000	10	2200	220
50.85	1.1	1000	9.1	2200	82
58.05	1.1	1000	8.2	2200	39

The phase and amplitude balance is achieved at IF Output frequency by using impedance matching network with LC. The port-to-port leakage is improved with the phase and amplitude balance is achieved at RF, LO, and IF frequency with wide band balun.

Typical Evaluation Board Schematic (2nd IF)

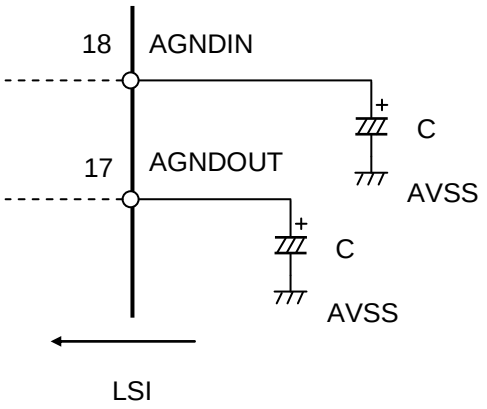
1) Power supply stabilizing capacitors
Connect capacitors between VDD and VSS pins to eliminate ripple and noise included in power supply. For maximum effect, the capacitors should be placed at a shortest distance between the pins.



C1=100pF
C2=0.1μF
C3=10μF (Electrolytic cap)

Figure 28 DVDD, AVDD

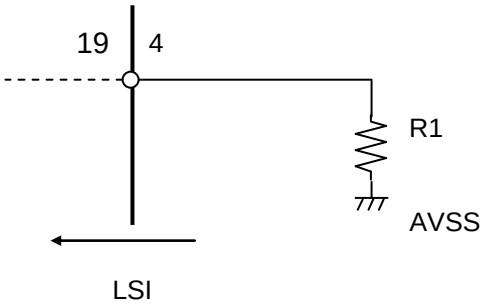
2) AGND stabilizing capacitors
It is recommended that capacitors with 1μF or lager be connected between VSS and the AGND and AGNDIN pins to stabilize the AGND signal. The capacitors must be placed as close to the pins as possible.



C=1μF (Electrolytic capacitor)

Figure 29 AGNDIN, AGNDOUT

3) BIAS4 pin

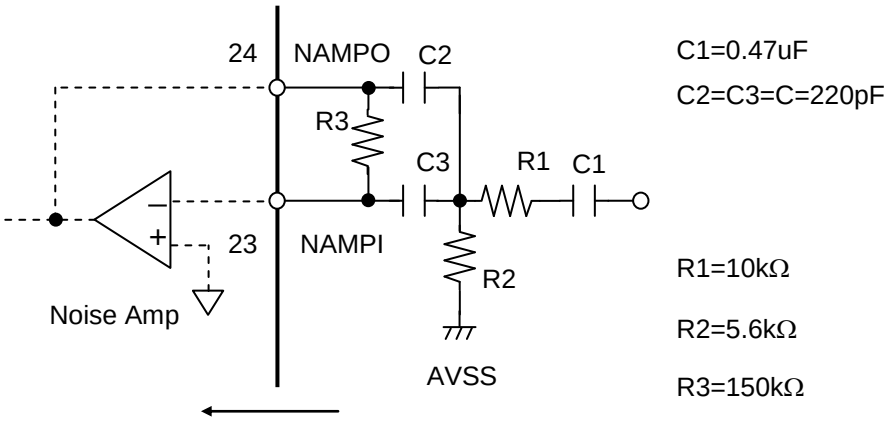


R1=47kΩ±1%

Figure 30 BIAS4

4) Noise Amp

The following gives a sample configuration of a BPF when input frequency is 31kHz.
Some parameters can be calculated using following (1) to (3) equations.



(1) $f_0 = \dfrac{1}{2\pi\sqrt{R_3(R_1 // R_2)C^2}}$ LSI

(2) $G_v = \dfrac{R_3}{2R_1}$

(3) $Q^2 = \dfrac{R_3}{4(R_1 // R_2)}$

Figure 31 NAMPO, NAMPI

5) NRECTO pin

Rise time of noise detection is proportionate to C1=0.1μF and internal resistance 75kΩ

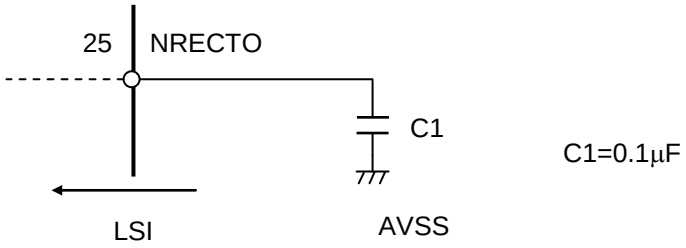


Figure 32 NRECTO

6) RSSIOUT pin

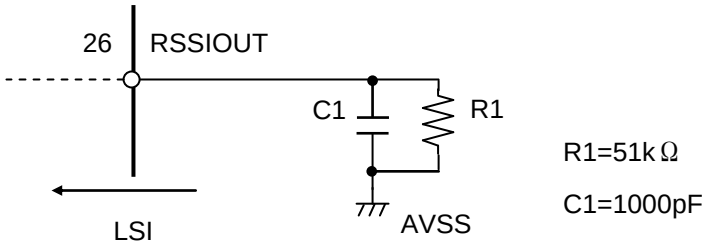


Figure 33 RSSIOUT

7) Discriminator

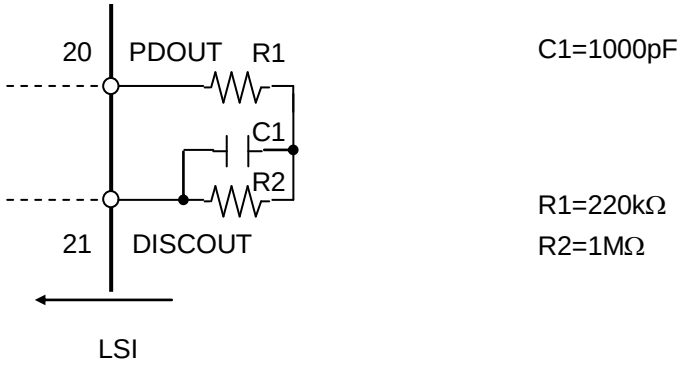


Figure 34 Discriminator

8) Tripler circuit

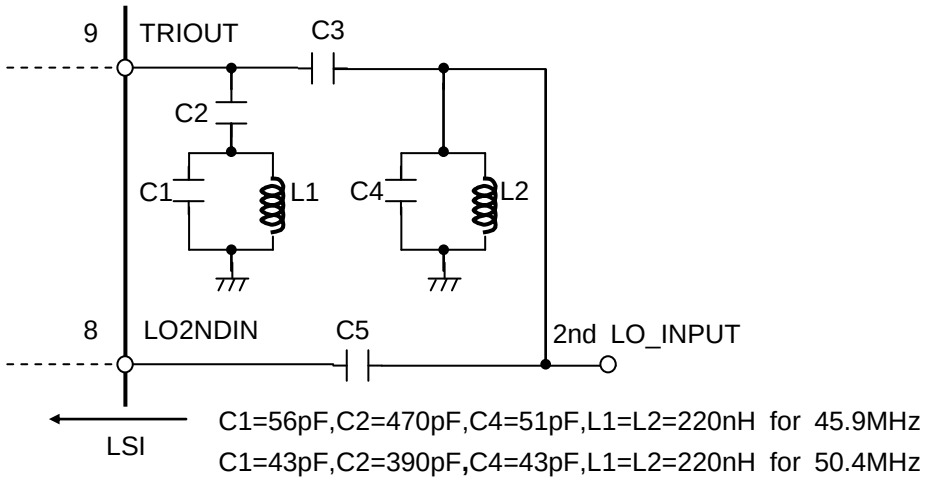


Figure 35 Tripler circuit

9) VREFA output

It is recommended that capacitors with 220nF or lager be connected between AVSS and VREFA pin to stabilize the VREFA signal. The capacitors must be placed as close to the pins as possible.

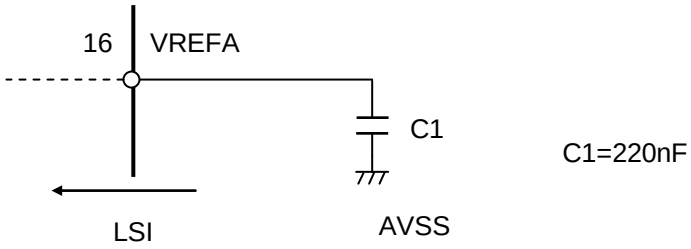


Figure 36 VREFA

10) DETO/SDATAOUT output

When {SDATAOUT_OE} is set “0“, DETO signal is output. DETO is open-drain output.

When {SDATAOUT_OE} is set “1“, SDATAOUT signal is output. SDATAOUT is CMOS output and output level is DVDD voltage.

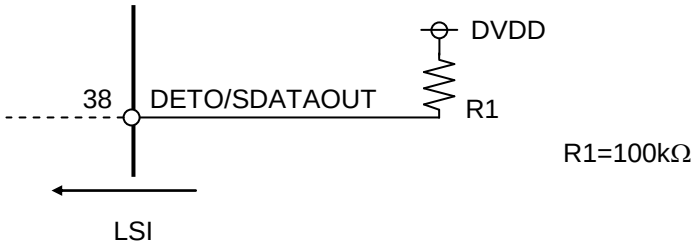
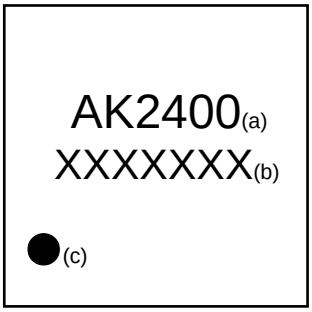


Figure 37 DETO/SDATAOUT

Package

Marking



a: Product number : AK2400
b: Date code : XXXXXXX
c: 1 pin marking : ●
d: Style : QFN
e: Number of pins : 56

Figure 38 Marking

Mechanical Outline

Package: 56pin-QFN (8 x 8 mm、0.5 mm pitch)

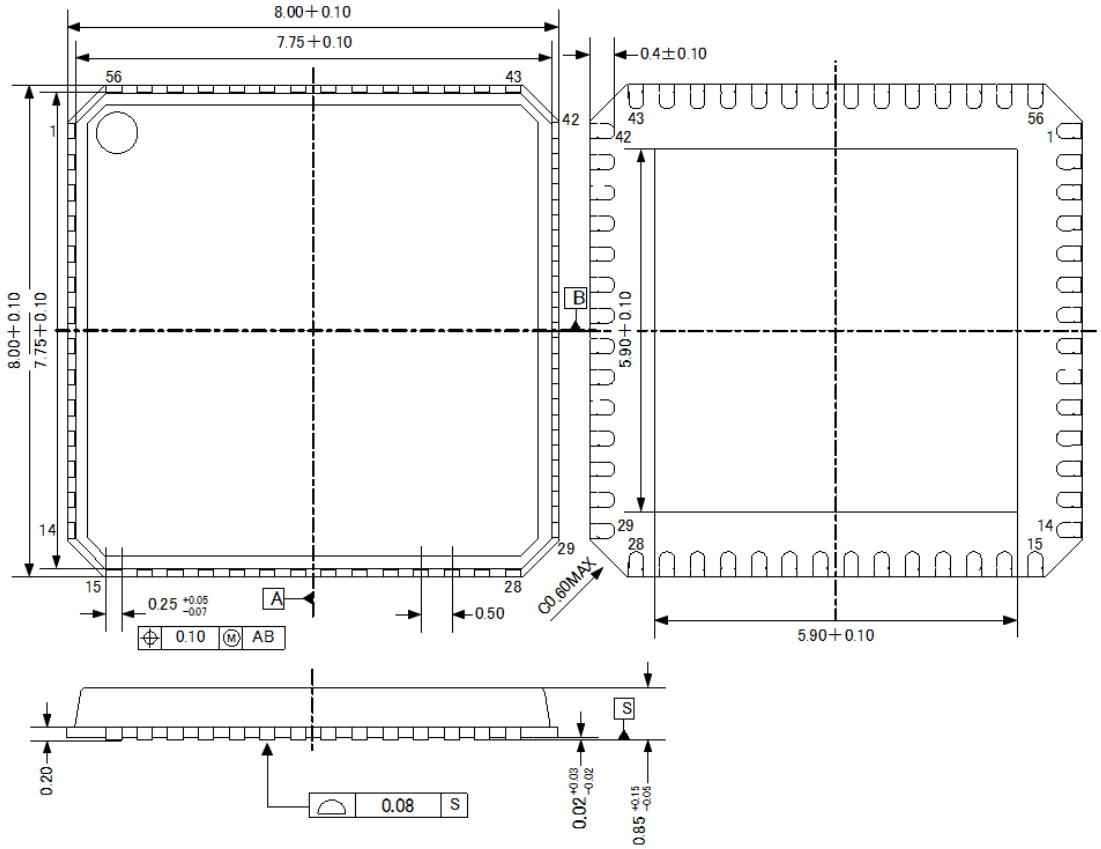


Figure 39 Mechanical Outline

Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
14/10/23	00	Initial Version		
15/04/23	01	Spec change	20, 28	Prohibit Mode1
		Spec addition	15	Expand input frequency range of 2ndMixer to FLO±0.45MHz
		Annotation addition	22, 24, 35	When OFFSET register is used, set DITH=0(OFF).

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●Related Parts

Part#	Discription	Comments
Mixer		
AK1220	100MHz~900MHz High Linearity Down Conversion Mixer	IIP3:+22dBm
AK1222	100MHz~900MHz Low Power Down Conversion Mixer	IDD:2.9mA
AK1224	100MHz~900MHz Low Noise, High Liniarity Down Conversion Mixer	NF:8.5dB, IIP3:+18dBm
AK1228	10MHz~2GHz Up/Down Conversion Mixer	3V Supply, NF:8.5dB
AK1221	0.7GHz~3.5GHz High Linearity Down Conversion Mixer	IIP3:+25dBm
AK1223	3GHz~8.5GHz High Linearity Down Conversion Mixer	IIP3:+13dB, NF:15dB
PLL Synthesizer		
AK1541	20MHz~600MHz Low Power Fractional-N Synthesizer	IDD:4.6mA
AK1542A	20MHz~600MHz Low Power Integer-N Synthesizer	IDD:2.2mA
AK1543	400MHz~1.3GHz Low Power Fractional-N Synthesizer	IDD:5.1mA
AK1544	400MHz~1.3GHz Low Power Integer-N Synthesizer	IDD:2.8mA
AK1590	60MHz~1GHz Fractional-N Synthesizer	IDD:2.5mA
AK1545	0.5GHz~3.5GHz Integer-N Synthesizer	16-TSSOP
AK1546	0.5GHz~3GHz Low Phase Noise Integer-N Synthesizer	Normalized C/N:-226dBc/Hz
AK1547	0.5GHz~4GHz Integer-N Synthesizer	5V Supply
AK1548	1GHz~8GHz Low Phase Noise Integer-N Synthesizer	Normalized C/N:-226dBc/Hz
IFVGA		
AK1291	100~300MHz Analog Signal Control IF VGA w/ RSSI	Dynamic Range:30dB
integrated VCO		
AK1572	690MHz~4GHz Down Conversion Mixer with Frac.-N PLL and VCO	IIP3:24dBm, -111dBc/Hz@100kHz
AK1575	690MHz~4GHz Up Conversion Mixer with Frac.-N PLL and VCO	IIP3:24dBm, -111dBc/Hz@100kHz
IF Reciever (2nd Mixer + IF BPF + FM Detector)		
AK2364	Built-in programmable AGC+BPF, FM detector IC	IFBPF:±10kHz ~ ±4.5kHz
AK2365A	Built-in programmable AGC+BPF, IFIC	IFBPF:±7.5kHz ~ ±2kHz
Analog BB for PMR/LMR		
AK2345C	CTCSS Filter, Encoder, Decoder	24-VSOP
AK2360/ AK2360A	Inverted frequency(3.376kHz/3.020kHz) scrambler	8-SON
AK2363	MSK Modem/DTMF Receiver	24-QFN
AK2346B	0.3-2.55/3.0kHz Analog audio filter, Emphasis, Compandor, scrambler, MSK Modem	24-VSOP
AK2346A		24-QFN
AK2347B	0.3-2.55/3.0kHz Analog audio filter Emphasis, Compandor, scrambler, CTCSS filter	24-VSOP
Function IC		
AK2330	8-bit 8ch Electronic Volume	VREF can be selected for each channel
AK2331	8-bit 4ch Electronic Volume	VREF can be selected for each channel

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