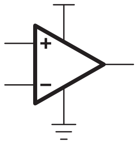
FAMILY OF 880-nA/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH REVERSE BATTERY PROTECTION

Check for Samples: TLV2401-Q1 , TLV2402-Q1, TLV2404-Q1

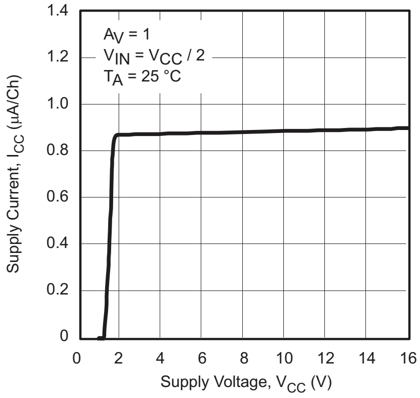
FEATURES

- **Qualified for Automotive Applications**
- **Micro-Power Operation . . . <1 μA/Channel**
- **Input Common-Mode Range Exceeds the Rails . . . –0.1 V to V_{CC} + 5 V**
- **Reverse Battery Protection Up To 18 V**
- **Rail-to-Rail Input/Output**
- **Gain Bandwidth Product . . . 5.5 kHz**
- **Supply Voltage Range . . . 2.5 V to 16 V**
- **Specified Temperature Range: –40°C to 125°C**
- **Ultrasmall Packaging**
  - **5-Pin SOT-23 (TLV2401-Q1)**
  - **8-Pin MSOP (TLV2402-Q1)**
- **Universal OpAmp EVM (Refer to the EVM Selection Guide SLOU060)**

Operational Amplifier



SUPPLY CURRENT
vs
SUPPLY VOLTAGE



DESCRIPTION/ORDERING INFORMATION

The TLV240x family of single-supply operational amplifiers has the lowest supply current available today at only 880 nA per channel. Reverse battery protection guards the amplifier from an overcurrent condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

The low supply current is coupled with extremely low input bias currents enabling them to be used with mega-W resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 390 μV, CMRR of 120 dB and minimum open loop gain of 130 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 16 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 15 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micro-power microcontrollers available today including TI’s MSP430.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in TSSOP.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

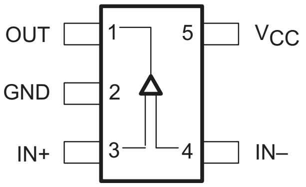
SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS(1)(2)

DEVICE	V_{CC} (V)	V_{IO} (mV)	BW (MHz)	SLEW RATE (V/µs)	$I_{CC/ch}$ (µA)	RAIL-TO-RAIL
TLV240x-Q1(2)	2.5–16	0.390	0.005	0.002	0.880	I/O

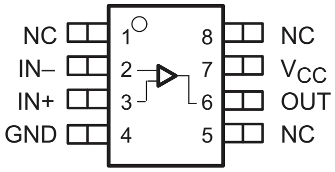
(1) All specifications are typical values measured at 5 V.
(2) This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.

DEVICE INFORMATION

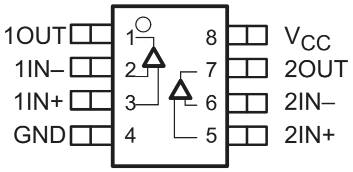
TLV2401-Q1
DBV PACKAGE
(TOP VIEW)



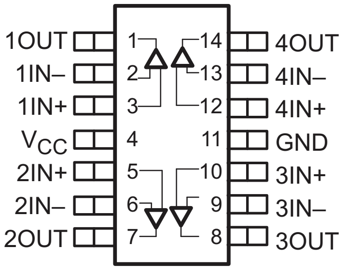
TLV2401-Q1
D PACKAGE
(TOP VIEW)



TLV2402-Q1
D OR DGK PACKAGE
(TOP VIEW)



TLV2404-Q1
D OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	MSOP – DGK	Reel of 2500	TLV2402QDGKRQ1	QWX
	SOIC – D	Reel of 2500	TLV2401QDRQ1	Product Preview
			TLV2402QDRQ1	
			TLV2404QDRQ1	
	SOT – DBV	Reel of 3000	TLV2401QDBVRQ1	Product Preview
	TSSOP – PW	Reel of 2000	TLV2404QPWRQ1	Product Preview

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]			17	V
V_{ID}	Differential input voltage range			±20	V
I_I	Input current range (any input)			±10	mA
I_O	Output current range			±10	mA
	Continuous total power dissipation		See Dissipation Ratings Table		
T_A	Operating free-air temperature range		–40	125	°C
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–60	125	°C
ESD	Electrostatic discharge[3]	Human-Body Model (HBM)		500	V
		Machine Model (MM)		200	
		Field_Induced_Charged Device Model (CDM)		1000	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

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(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Tested in accordance with AEC-Q100.

DISSIPATION RATINGS

PACKAGE	Q_{JC} (°C/W)	Q_{JA} (°C/W)	T_A ≤ 25°C POWER RATING	TA = 125°C POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
PW (14)	29.3	173.6	720 mW	144 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Single supply	2.5	16	V
		Split supply	±1.25	±8	
V_{ICR}	Common-mode input voltage range		–0.1	V_{CC}+5	V
T_A	Operating free-air temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS
DC Performance

V_{CC} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
DC Performance								
V_{IO}	Input offset voltage	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, RS = 50 Ω		25°C		390	1900	µV
				Full range			2800	
αV_{IO}	Offset voltage draft			25°C		3		µV/°C
CMRR	Common mode rejection ratio	V_{IC} = 0 to V_{CC}, RS = 50 Ω	V_{CC} = 2.7 V	25°C	60	120		dB
				Full range	56			
			V_{CC} = 5 V	25°C	65	120		
				Full range	58			
			V_{CC} = 15 V	25°C	73	120		
				Full range	73			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 2.7 V, $V_{O(pp)}$ = 1 V, R_L = 500 kΩ		25°C	130	400		V/mV
				Full range	12			
		V_{CC} = 5 V, $V_{O(pp)}$ = 3 V, R_L = 500 kΩ		25°C	300	1000		
				Full range	37			
		V_{CC} = 15 V, $V_{O(pp)}$ = 6 V, R_L = 500 kΩ		25°C	1000	1800		
				Full range	66			
Input Characteristics								
I_{IO}	Input offset current	$V_O = V_{CC}/2$ V, $V_{IC} = V_{CC}/2$ V, RS = 50 Ω		25°C		25	250	pA
				Full range			400	
I_{IB}	Input bias current			25°C		100	300	pA
				Full range			900	
$r_{i(d)}$	Differential input resistance			25°C		300		MΩ
$C_{i(c)}$	Common-mode input capacitance	f = 100 kHz		25°C		3		pF

ELECTRICAL CHARACTERISTICS
DC Performance (continued)

V_{CC} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
Output Characteristics									
V_{OH}	High-level output voltage	$V_{IC} = V_{CC}/2$, I_{OH} = –2 μA	V_{CC} =2.7 V		25°C	2.65	2.68		V
					Full range	2.63			
			V_{CC} = 5 V		25°C	4.95	4.98		
					Full range	4.93			
			V_{CC} = 15 V		25°C	14.95	14.98		
					Full range	14.93			
		$V_{IC} = V_{CC}/2$, I_{OH} = –50 μA	V_{CC} = 2.7 V		25°C	2.62	2.65		
					Full range	2.6			
			V_{CC} = 5 V		25°C	4.92	4.95		
					Full range	4.9			
			V_{CC} = 15 V		25°C	14.92	14.95		
					Full range	14.9			
V_{OL}	Low-level output voltage	$V_{IC} = V_{CC}/2$, I_{OL} = 2 μA			25°C		90	150	mV
					Full range			180	
		$V_{IC} = V_{CC}/2$, I_{OL} = 50 μA			25°C		180	230	
					Full range			260	
I_O	Output current	V_O = 0.5 V from rail			25°C		±200		μA
Power Supply									
I_{CC}	Supply current (per channel)	$V_O = V_{CC}/2$	V_{CC} =2.7 V or 5 V		25°C		880	990	nA
					Full range			1300	
			V_{CC} = 15 V		25°C		900	1050	
					Full range			1400	
	Reverse supply current	V_{CC} = –18 V, V_{IN} = 0 V, V_O = Open circuit			25°C		50		nA
PSRR	Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 2.7 V or 5 V, $V_{IC} = V_{CC}/2$, No load			25°C	100	120		dB
					Full range	83			
		V_{CC} = 5 to 15 V, $V_{IC} = V_{CC}/2$, No load			25°C	100	120		dB
					Full range	97			
Dynamic Performance									
UGBW	Unity gain bandwidth	R_L = 500 kΩ, C_L = 100 pF			25°C		5.5		kHz
SR	Slew rate at unity gain				25°C		2.5		V/ms
φM	Phase margin	R_L = 500 kΩ, C_L = 100 pF			25°C		60°		
	Gain margin						15		dB
t_S	Settling time	V_{CC} = 2.7 V or 5 V, $V_{(STEP)PP}$ = 1 V, A_V = –1,	C_L = 100 pF R_L = 100 kΩ	0.1%	25°C		1.84		ms
		V_{CC} = 15 V, $V_{(STEP)PP}$ = 1 V, A_V = –1,	C_L = 100 pF R_L = 100 kΩ	0.1%			6.1		
				0.01%			32		

ELECTRICAL CHARACTERISTICS DC Performance (continued)

V_{CC} = 2.7 V, 5 V, and 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Noise/Distortion Performance							
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		800		nV/√Hz
		f = 100 Hz			500		
I_n	Equivalent input noise current	f = 100 Hz			8		fA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input Offset Voltage	vs Common-mode input voltage	Figure 1, Figure 2, Figure 3
I_{IB}	Input Bias Current	vs Free-air temperature	Figure 4, Figure 6, Figure 8
		vs Common-mode input voltage	Figure 5, Figure 7, Figure 9
I_{IO}	Input Offset Current	vs Free-air temperature	Figure 4, Figure 6, Figure 8
		vs Common-mode input voltage	Figure 5, Figure 7, Figure 9
CMRR	Common-mode rejection ratio	vs Frequency	Figure 10
V_{OH}	High-level output voltage	vs High-level output current	Figure 11, Figure 13, Figure 15
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 12, Figure 14, Figure 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	Figure 17
Z_o	Output impedance	vs Frequency	Figure 18
I_{CC}	Supply current	vs Supply voltage	Figure 19
PSRR	Power supply rejection ratio	vs Frequency	Figure 20
A_{VD}	Differential voltage gain	vs Frequency	Figure 21
	Phase	vs Frequency	Figure 21
	Gain-bandwidth product	vs Supply voltage	Figure 22
	SR Slew rate	vs Free-air temperature	Figure 23
φm	Phase margin	vs Capacitive load	Figure 24
	Gain margin	vs Capacitive load	Figure 25
	Supply current	vs Reverse voltage	Figure 26
	Voltage noise over a 10 Second Period		Figure 27
	Large signal follower pulse response		Figure 28, Figure 29, Figure 30
	Small signal follower pulse response		Figure 31
	Large signal inverting pulse response		Figure 32, Figure 33, Figure 34
	Small signal inverting pulse response		Figure 35
	Crosstalk	vs Frequency	Figure 36

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

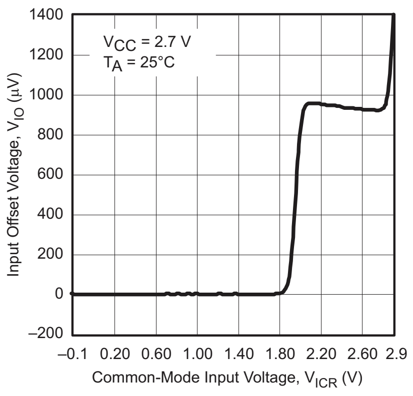


Figure 1.

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

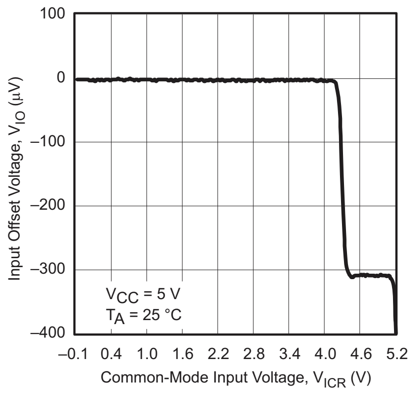


Figure 2.

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

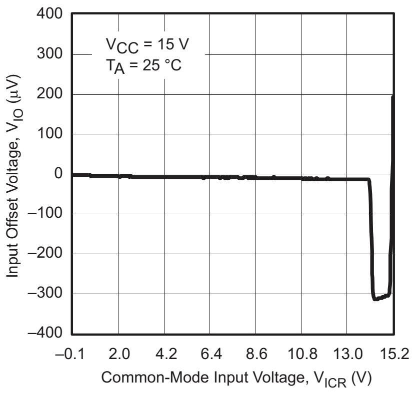


Figure 3.

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

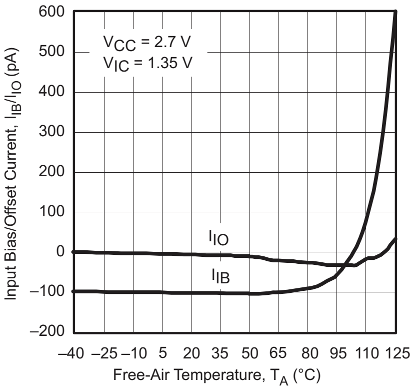


Figure 4.

INPUT BIAS / OFFSET CURRENT vs COMMON MODE INPUT VOLTAGE

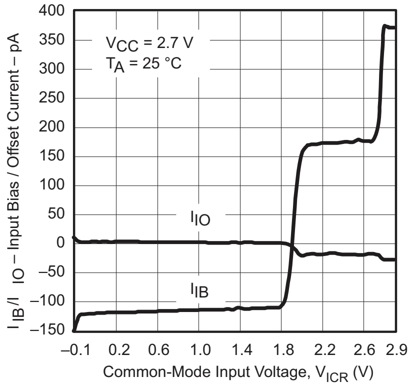


Figure 5.

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

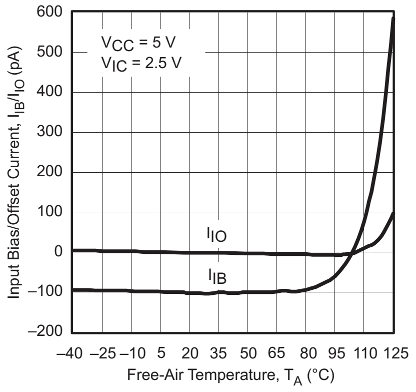


Figure 6.

INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

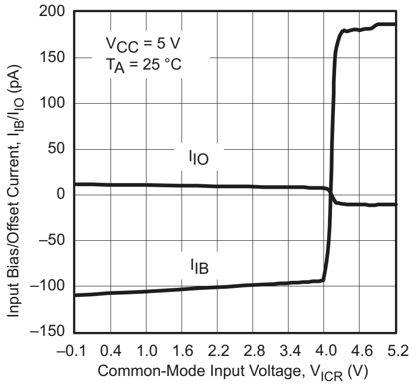


Figure 7.

INPUT BIAS / OFFSET CURRENT vs FREE-AIR TEMPERATURE

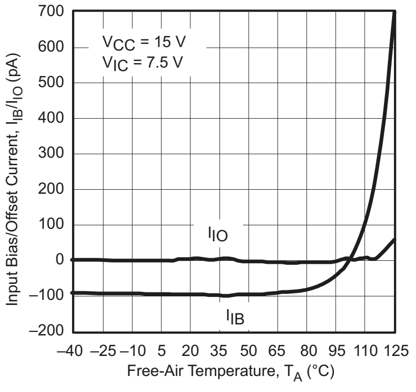


Figure 8.

INPUT BIAS / OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

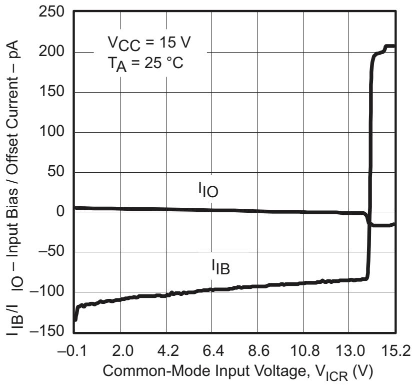


Figure 9.

COMMON-MODE REJECTION RATIO vs FREQUENCY

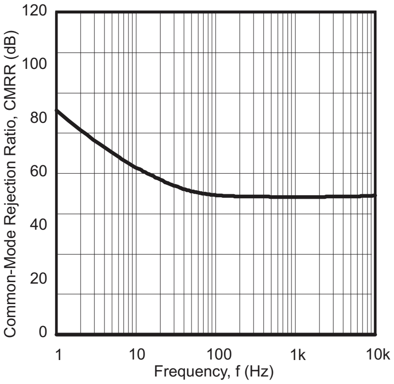


Figure 10.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

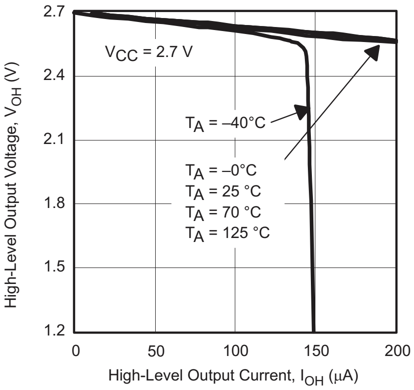


Figure 11.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

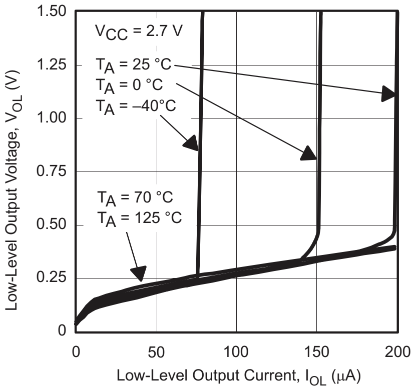


Figure 12.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

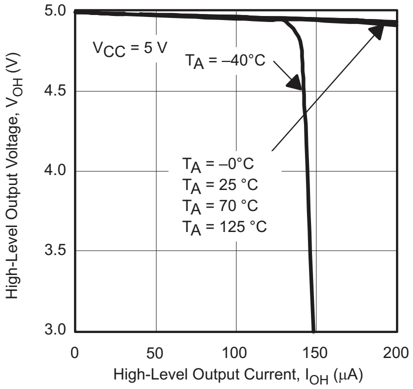


Figure 13.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

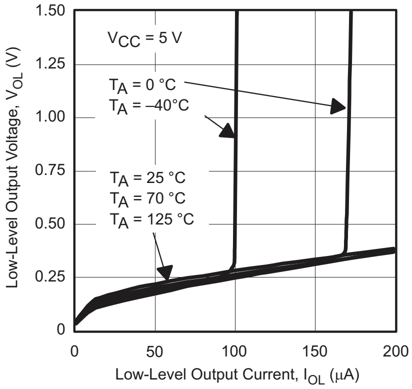


Figure 14.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

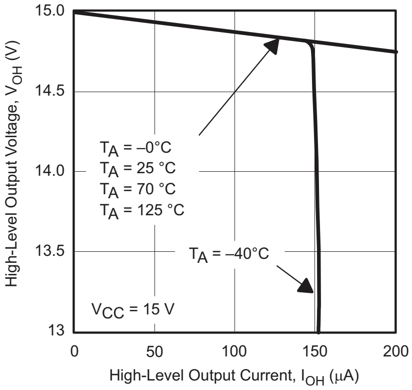


Figure 15.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

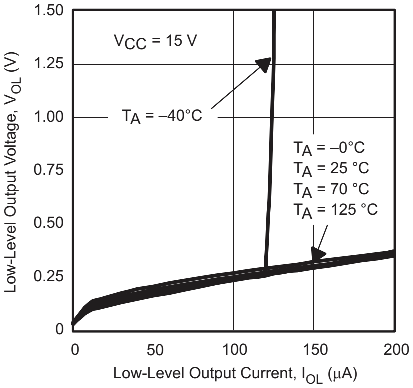


Figure 16.

OUTPUT VOLTAGE PEAK-TO-PEAK vs FREQUENCY

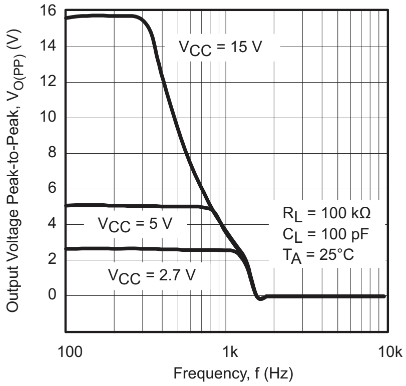


Figure 17.

OUTPUT IMPEDANCE vs FREQUENCY

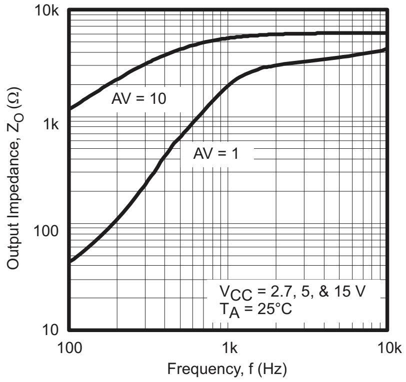


Figure 18.

SUPPLY CURRENT vs SUPPLY VOLTAGE

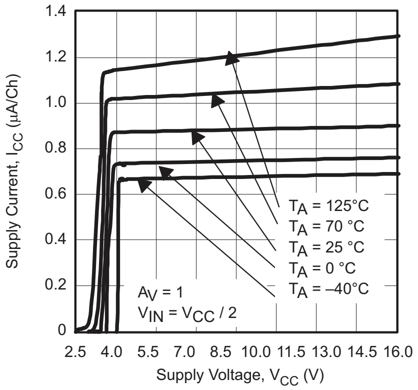


Figure 19.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

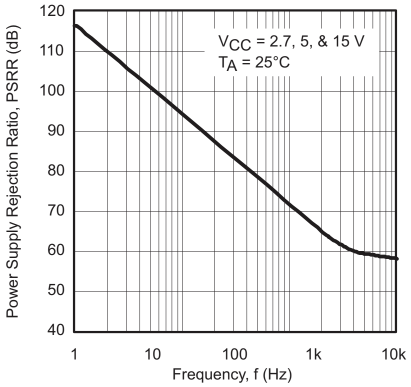


Figure 20.

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

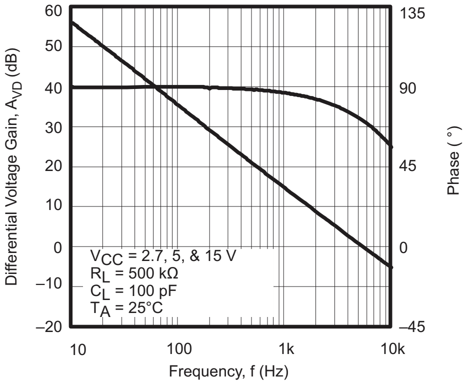


Figure 21.

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

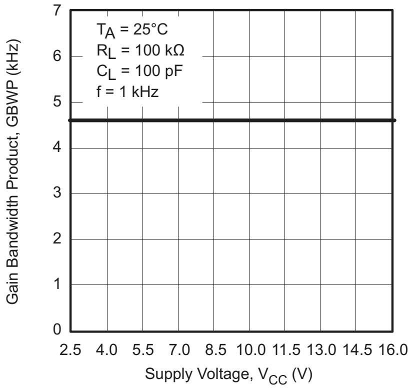


Figure 22.

SLEW RATE vs FREE-AIR TEMPERATURE

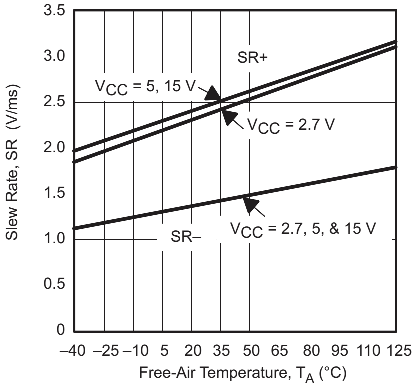


Figure 23.

PHASE MARGIN vs CAPACITIVE LOAD

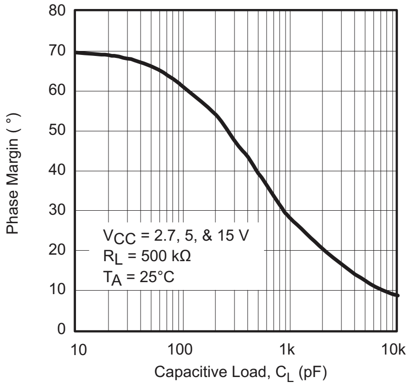


Figure 24.

**GAIN MARGIN
vs
CAPACITIVE LOAD**

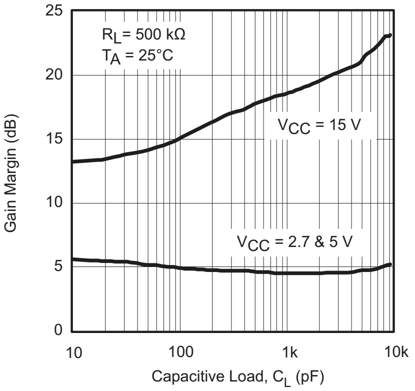


Figure 25.

**SUPPLY CURRENT
vs
REVERSE VOLTAGE**

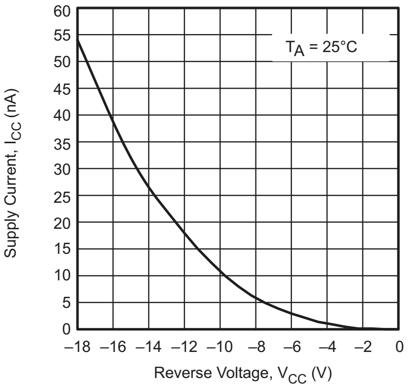


Figure 26.

**VOLTAGE NOISE
OVER A 10 SECOND PERIOD**

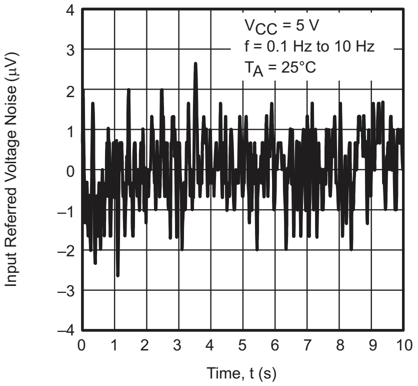


Figure 27.

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE**

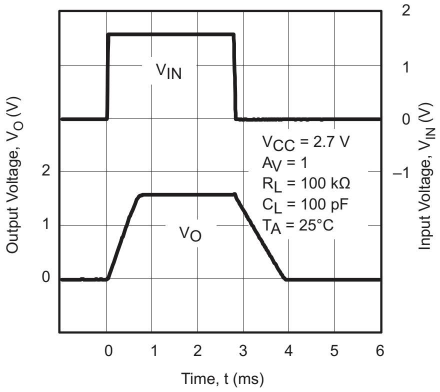


Figure 28.

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE**

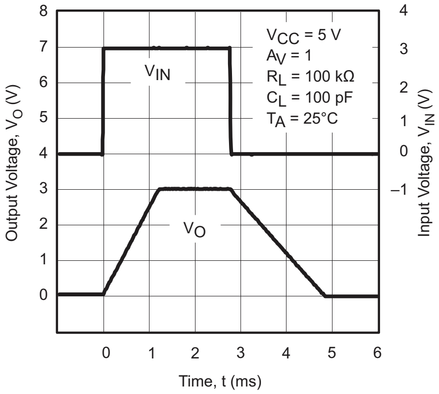


Figure 29.

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE**

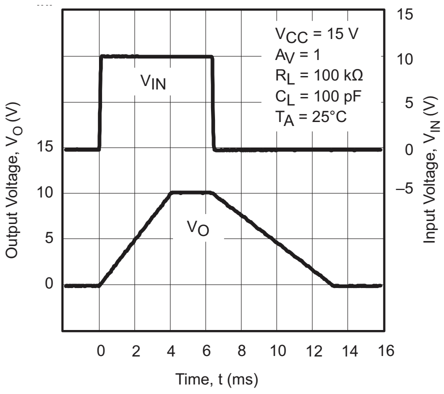


Figure 30.

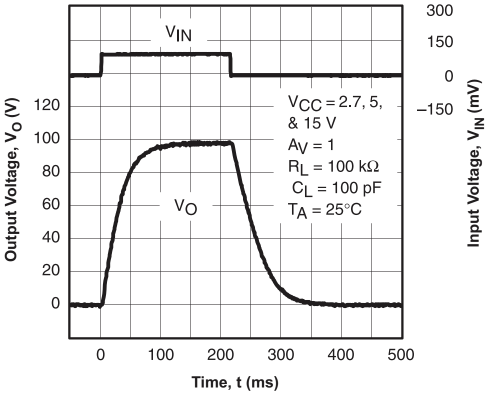


Figure 31.

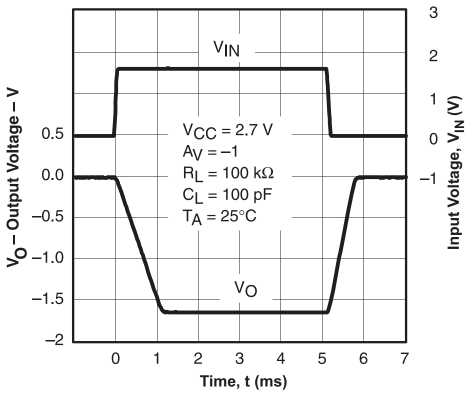


Figure 32.

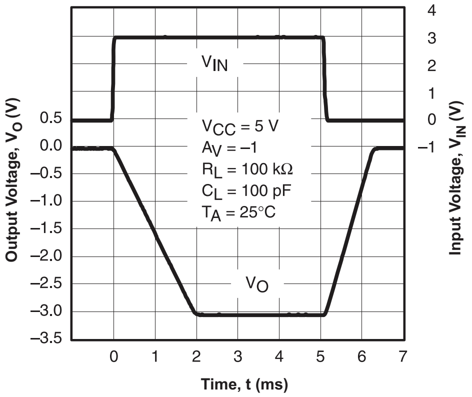


Figure 33.

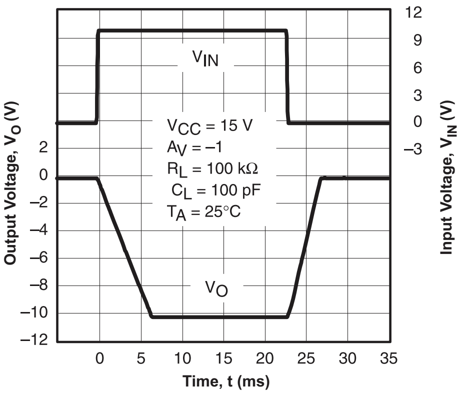


Figure 34.

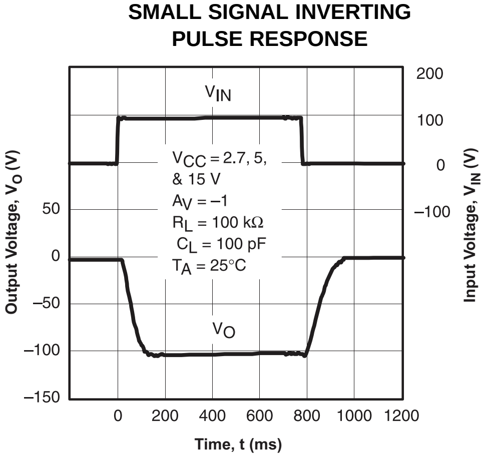


Figure 35.

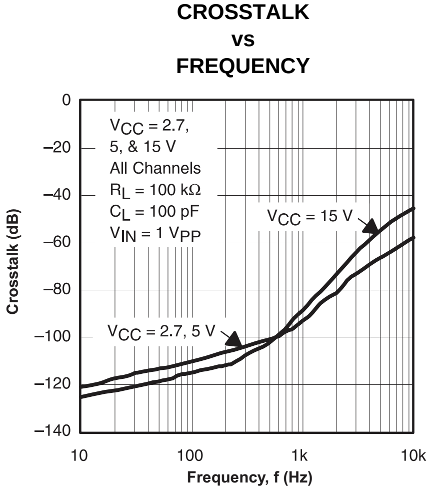


Figure 36.

APPLICATION INFORMATION

Reverse Battery Protection

The TLV240x-Q1 are protected against reverse battery voltage up to 18 V. When subjected to reverse battery condition the supply current is typically less than 100 nA at 25°C (inputs grounded and outputs open). This current is determined by the leakage of 6 Schottky diodes and will therefore increase as the ambient temperature increases.

When subjected to reverse battery conditions and negative voltages applied to the inputs or outputs, the input ESD structure will turn on—this current should be limited to less than 10 mA. If the inputs or outputs are referred to ground, rather than midrail, no extra precautions need be taken.

Common-Mode Input Range

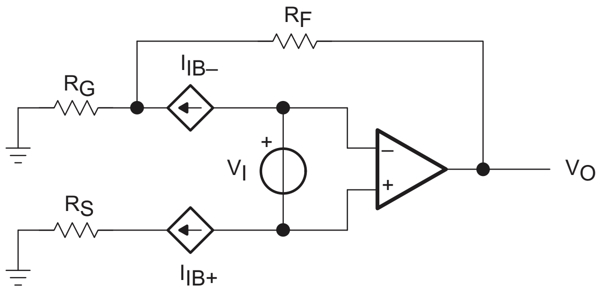
The TLV240x-Q1 has rail-to-rail input and outputs. For common-mode inputs from –0.1 V to V_{CC} – 0.8 V a PNP differential pair will provide the gain.

For inputs between V_{CC} – 0.8 V and V_{CC}, two NPN emitter followers buffering a second PNP differential pair provide the gain. This special combination of NPN/PNP differential pair enables the inputs to be taken 5 V above the rails, because as the inputs go above V_{CC}, the NPNs switch from functioning as transistors to functioning as diodes. This will lead to an increase in input bias current. The second PNP differential pair continues to function normally as the inputs exceed V_{CC}.

The TLV240x-Q1 has a negative common-input range that exceeds ground by 100 mV. If the inputs are taken much below this, reduced open loop gain will be observed with the ultimate possibility of phase inversion.

Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 37. Output Offset Voltage Model

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 38).

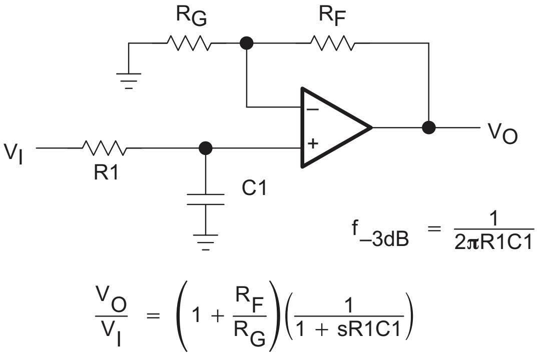


Figure 38. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

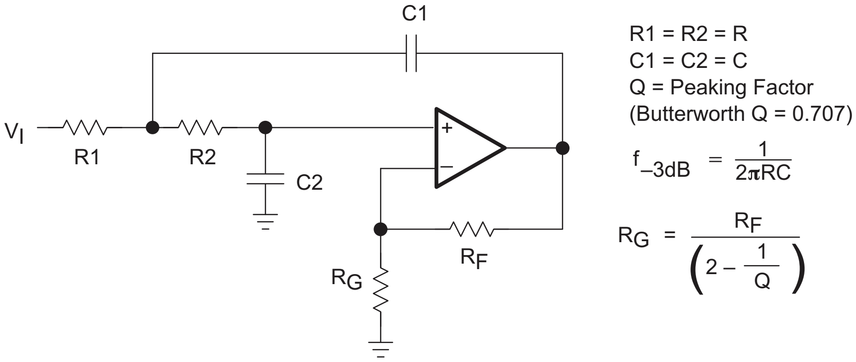


Figure 39. 2-Pole Low-Pass Sallen-Key Filter

Circuit Layout Considerations

To achieve the levels of high performance of the TLV240x-Q1, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-mF tantalum capacitor in parallel with a 0.1-mF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-mF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-mF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

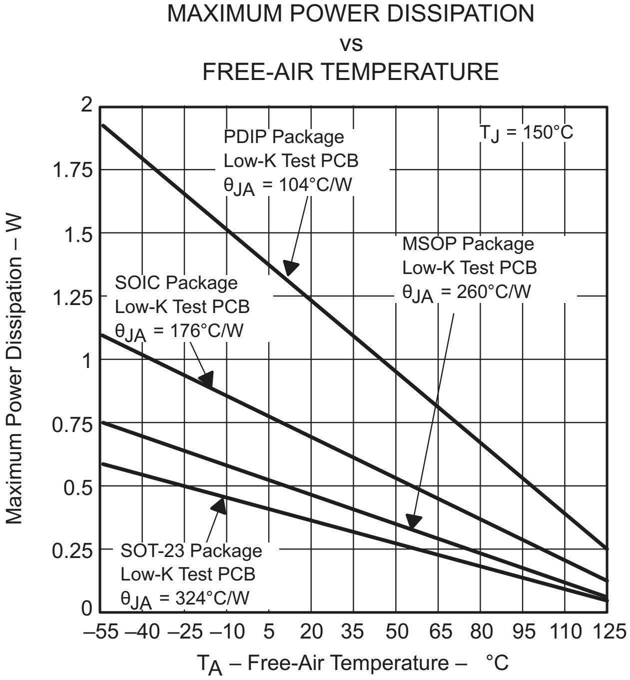
General Power Dissipation Considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 40 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

PD = Maximum power dissipation of THS240x IC (watts)
T_{MAX}= Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



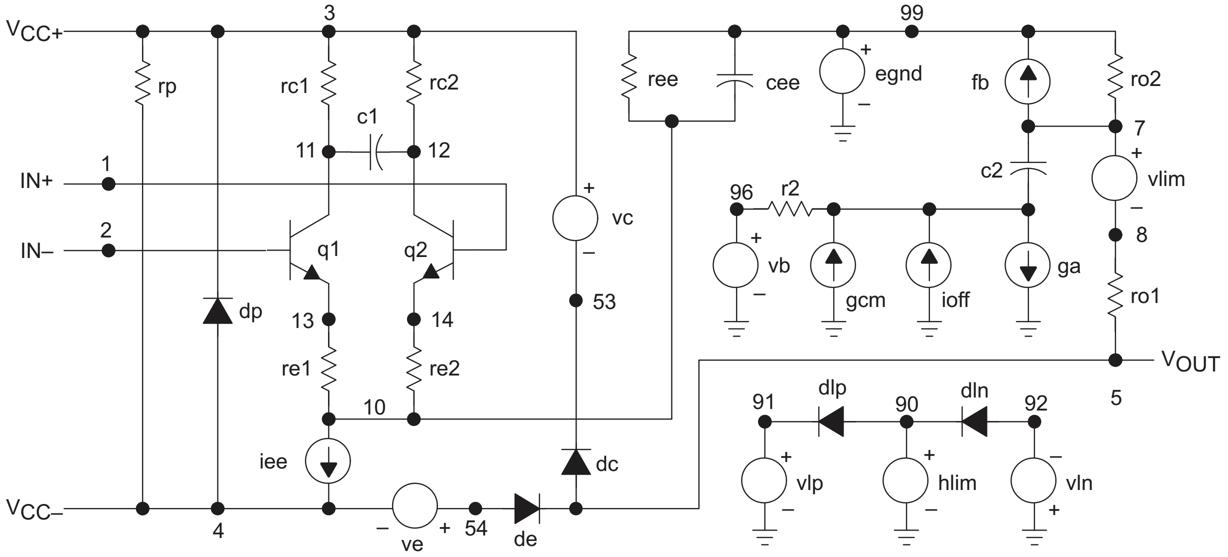
(1) Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 40. Maximum Power Dissipation vs Free-Air Temperature

Macromodel Information

Macromodel information provided was derived using Microsim PartsE Release 8, the model generation software used with Microsim PSpiceE. The Boyle macromodel(1) and subcircuit in Figure 41 are generated using the TLV240x-Q1 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit



```
.subckt 240X_5V–X 1 2 3 4 5
*
c1      11    12    9.8944E–12
c2      6     7     30.000E–12
cee     10    99     8.8738E–12
dc      5     53    dy
de      54    5     dy
dlp     90    91    dx
dln     92    90    dx
dp      4     3     dx
egnd    99    0     poly(2) (3,0) (4,0) 0 .5 .5
fb      7     99    poly(5) vb vc ve vlp vln 0 61.404E6 –1E3 1E3 61E6 –61E6
ga      6     0     11    12    1.0216E–6
gcm     0     6     10    99    10.216E–12
iee     10    4     dc 54.540E–9
ioff    0     6     dc 5e–12
hlim    90    0     vlim 1K
q1      11    2     13 qx1
q2      12    1     14 qx2
r2      6     9     1.00E+05
```

```
rc1     3     11    9.79E+05
rc2     3     12    9.79E+05
re1     13    10    3.04E+04
re2     14    10    3.04E+04
ree     10    99    3.67E+09
ro1     8     5     10
ro2     7     99    10
rp      3     4     1.42E+06
vb      9     0     dc  0
vc      3     53    dc  0.88315
ve      54    4     dc  0.88315
vlim    7     8     dc  0
vlp     91    0     dc  540
vln     0     92    dc  540
.model  dx    D(Is=800.00E–18)
.model  dy    D(Is=800.00E–18 Rs=1m Cjo=10p)
.model  qx1   NPN(Is=800.00E–18 Bf=27.270E21)
.model  qx2   NPN(Is=800.0000E–18 Bf=27.270E21)
.ends
```

Figure 41. Boyle Macromodels and Subcircuit

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV2402QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWX	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV2402-Q1 :

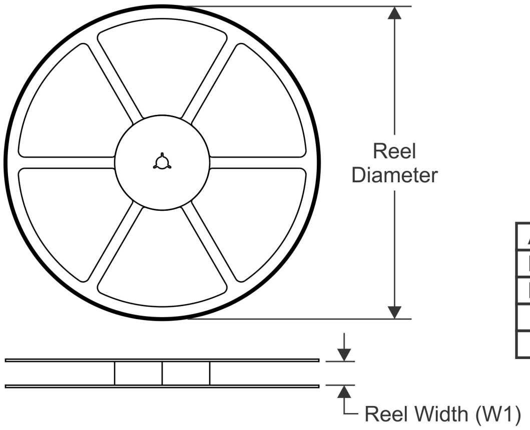
- Catalog: TLV2402

NOTE: Qualified Version Definitions:

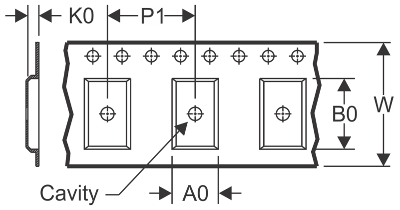
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

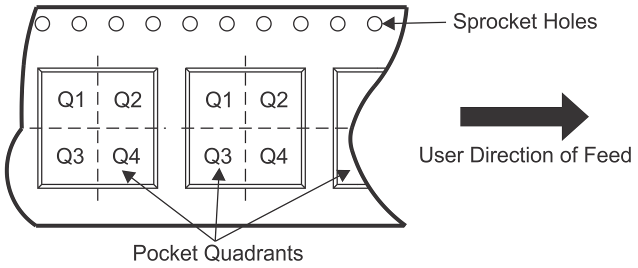


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

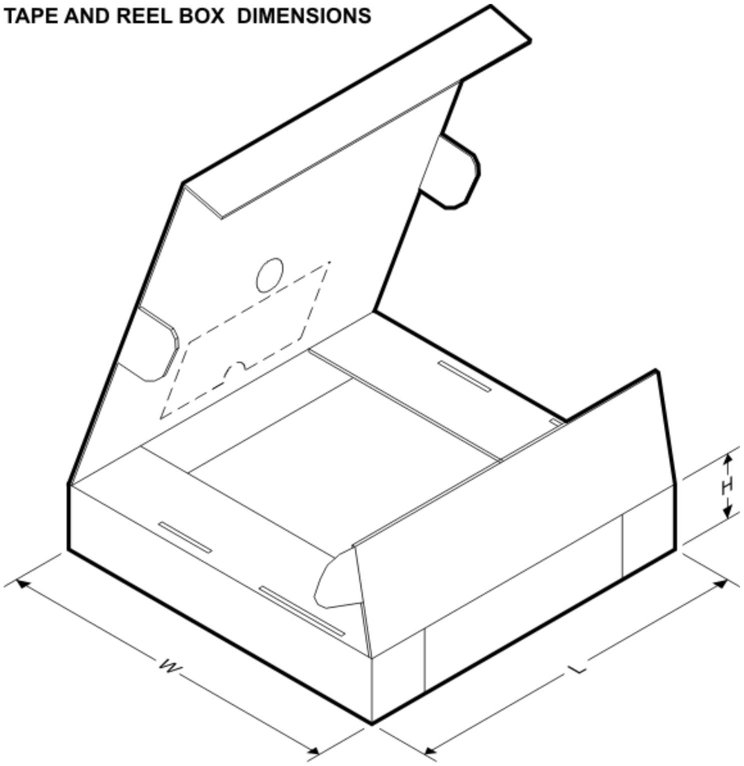
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2402QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

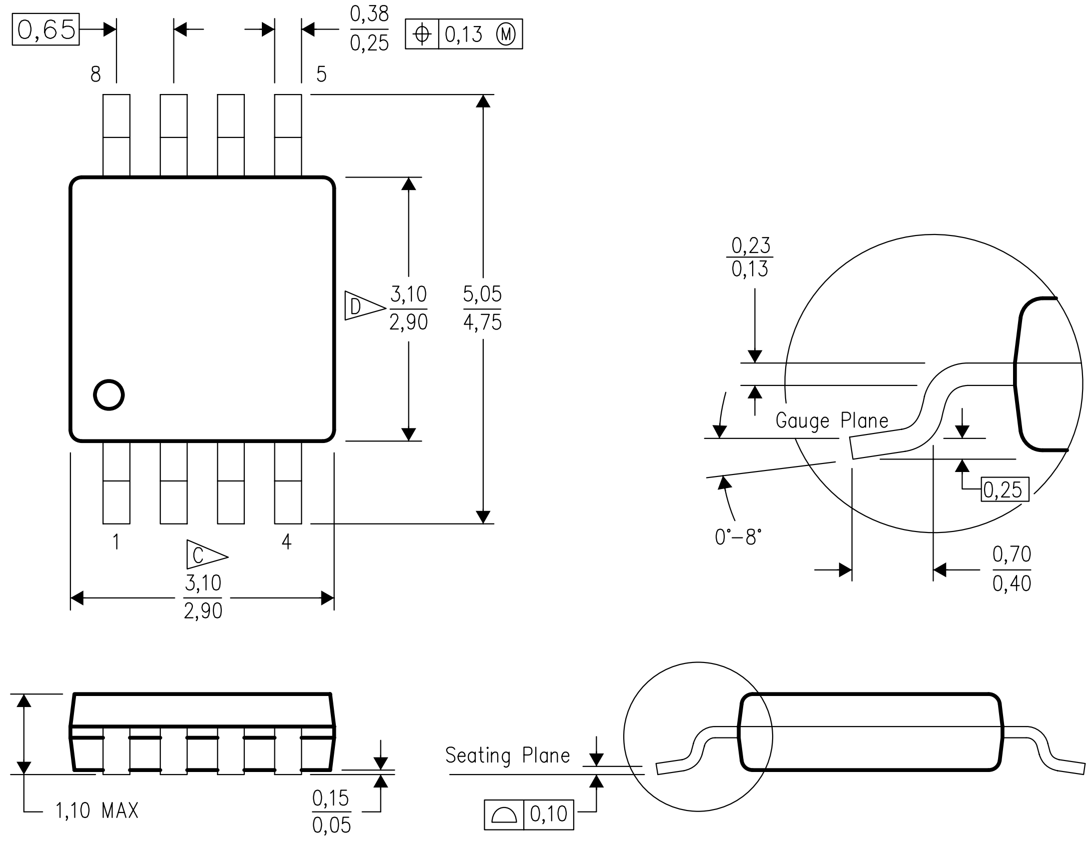
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2402QDGKRQ1	VSSOP	DGK	8	2500	358.0	335.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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