AK4953A

24bit Stereo CODEC with MIC/HP/SPK-AMP

GENERAL DESCRIPTION

The AK4953A is a low power consumption 24bit stereo CODEC with a microphone, headphone and speaker amplifiers. The input circuits include a microphone amplifier and an ALC (Automatic Level Control) circuit, and the output circuits include a cap-less headphone amplifier and a speaker amplifier. It is suitable for portable application with recording/playback function. The integrated charge pump circuit generates a negative voltage and removes the output AC coupling capacitors. The speaker amplifier has a wide operating voltage range, which is from 0.9V to 5.5V, enabling a direct drive to batteries. The AK4953A is available in a small 36pin QFN (5x5mm 0.4mm pitch), utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **Stereo Single-ended input with three Selectors**
- **MIC Amplifier (+29dB/+26dB/+23dB/+20dB/+16dB/+12dB/0dB)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –54dB, 0.375dB Step)
- **ADC Performance: S/(N+D): 82dB, DR, S/N: 88dB (MIC-Amp=+20dB)**
  S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- **Wind-noise Reduction Filter**
- **5 Band Notch Filter**
- **Digital MIC Interface**

2. Playback Function
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –54dB, 0.375dB Step)
- **Digital Volume Control (+12dB ~ –115dB, 0.5dB Step, Mute)**
- **Capacitor-less Stereo Headphone Amplifier**
  - **HP-Amp Performance: S/(N+D): 80dB@24mW, S/N: 96dB**
  - **Output Power: 24mW@16Ω**
  - **Pop Noise Free at Power-ON/OFF**
- **Mono Speaker-Amplifier**
  - **SPK-Amp Performance: S/(N+D): 70dB@250mW, S/N: 95dB**
  - **BTL Output**
  - **Output Power: 400mW@8Ω (SVDD=3.3V)**
    100mW@8Ω (SVDD=1.5V)
- **Beep Generator**

3. Power Management

4. Master Clock:

(1) PLL Mode
- **Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)**
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)**

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 96kHz**
- **PLL Slave Mode (MCKI pin): 7.35kHz, 8kHz, 11.025kHz, 12kHz, 14.7kHz, 16kHz, 22.05kHz, 24kHz, 29.4kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz**
- **PLL Master Mode: 7.35kHz, 8kHz, 11.025kHz, 12kHz, 14.7kHz, 16kHz, 22.05kHz, 24kHz, 29.4kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz**
- **EXT Master/Slave Mode: 7.35kHz ~ 96kHz (256fs), 7.35kHz ~ 48kHz (384fs), 7.35kHz ~ 48kHz (512fs), 7.35kHz ~ 12kHz (1024fs)**

6. μP I/F: 3-wire Serial, I^2C Bus (Ver 1.0, 400kHz Fast-Mode)
7. Master/Slave mode
8. Audio Interface Format: MSB First, 2's complement
- **ADC: 24bit MSB justified, 16/24bit I^2S**
- **DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I^2S**

9. Ta = –30 ~ 85°C (SPK-Amp = OFF)
Ta = –30 ~ 70°C (SPK-Amp = ON)
10. Power Supply:
- **Analog Power Supply (AVDD): 2.85 ~ 3.5V**
- **Digital Power Supply (DVDD): 1.6 ~ 2.0V**
- **Digital I/O Power Supply (TVDD): DVDD ~ 3.5V**
- **Speaker Power Supply (SVDD): 0.9 ~ 5.5V**

11. Package: 36pin QFN (5 x 5mm, 0.4mm pitch)

■ Block Diagram

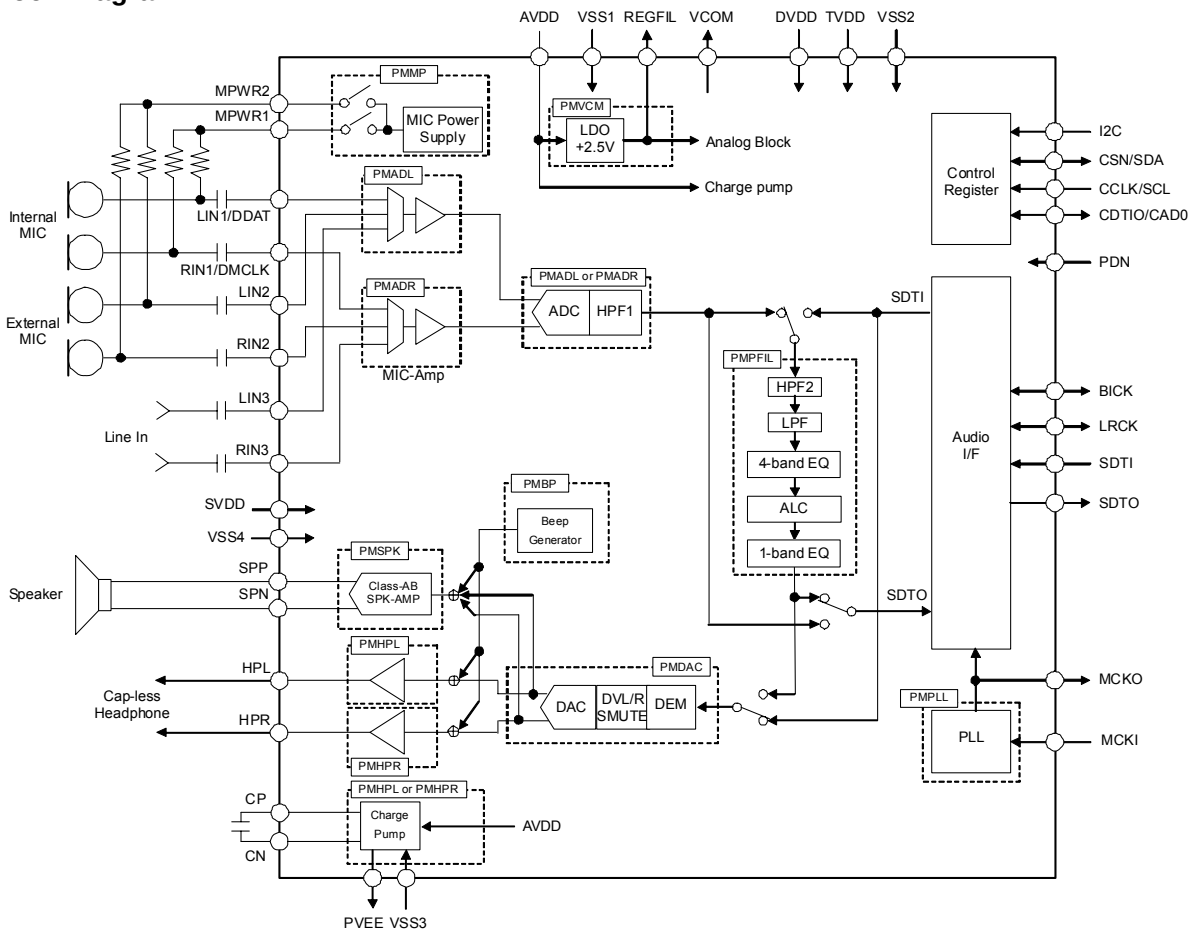
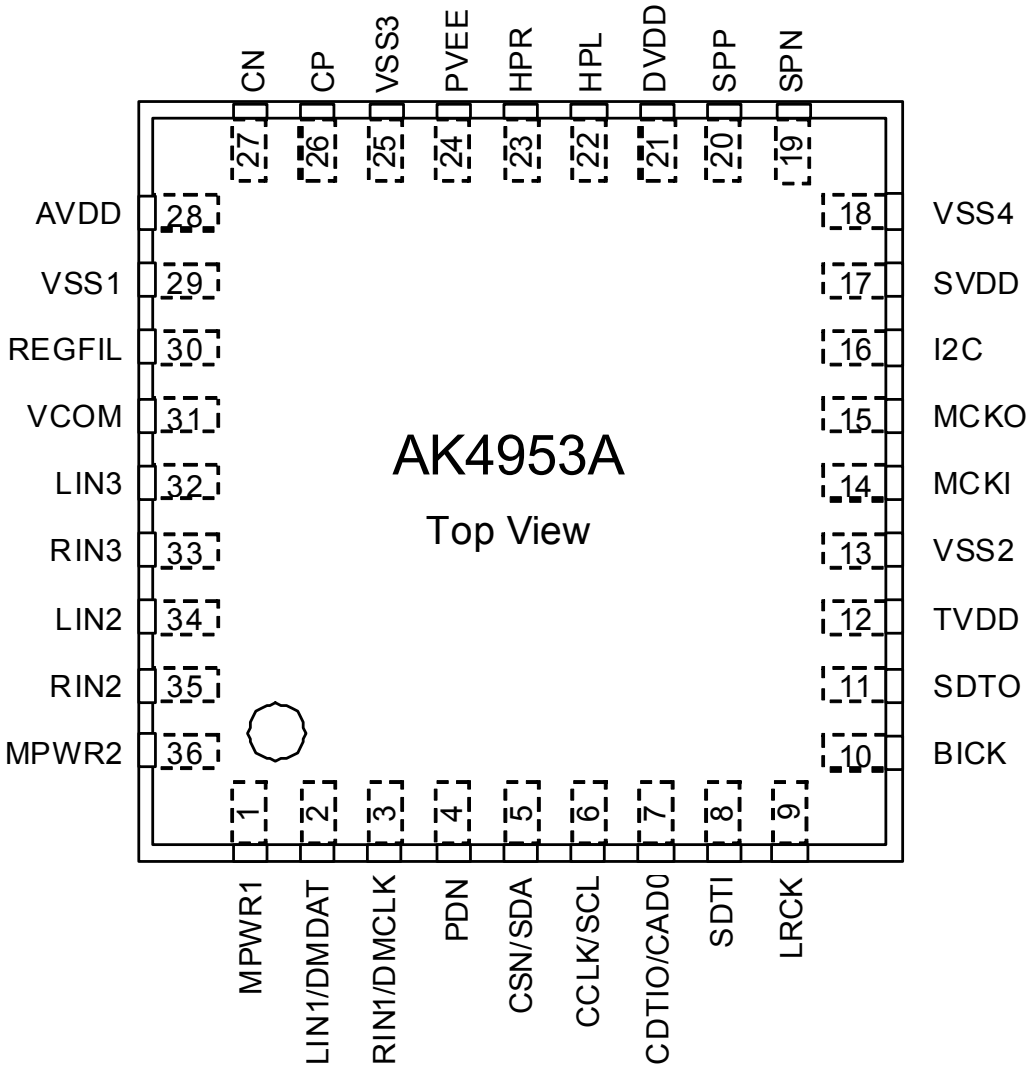


Figure 1. Block Diagram

■ Ordering Guide

AK4953AEN	–30 ~ +85°C	36pin QFN (0.4mm pitch)
AKD4953A	Evaluation board for AK4953A	

■ Pin Layout



■ Comparison with AK4645

Function	AK4645	AK4953A
Resolution	16bit	24bit
AVDD	2.6V ~ 3.6V	2.85V ~ 3.5V
DVDD	2.6V ~ 3.6V	1.6V ~ 2.0V
HVDD	2.6V ~ 5.25V	-
SVDD	-	0.9V ~ 5.5V
TVDD	1.6V ~ 3.6V	DVDD ~ 3.5V
ADC DR, S/N	86dB @ MGAIN = +20dB 95dB @ MGAIN = 0dB	88dB @ MGAIN = +20dB 96dB @ MGAIN = 0dB
DAC S/N	92dB	96dB
Input level	typ. 0.6 x AVDD @ MIC Gain=0dB	typ. 2.4Vpp @ MIC Gain=0dB
Output level (Headphone)	typ. 0.6 x AVDD @LOVL=0dB	typ. 1.75Vpp @ DVOL=0dB
ADC Input Selector	4 Stereo	3 Stereo
MIC Power Output Voltage	0.8 x AVDD	typ 2.3V (2 Line Outputs)
MIC-Amp	0dB/+20dB/+26dB/+32dB	0dB/+12dB/+16dB/+20dB/+23dB/ +26dB/+29dB
Digital MIC I/F	No	Yes
HPF(HPF1) after ADC	Fixed (fc = 0.9Hz)	4 frequencies (fc = 3.4Hz/13.6Hz/108.8Hz/217.6Hz @ fs=44.1kHz)
Notch Filter	No	5 Step (4 Step + 1 Step)
Stereo Emphasis	Yes	No
Output Volume	+36dB ~ -54dB, 0.375dB Step (Note 1) & +12dB ~ -115dB, 0.5dB Step	+36dB ~ -54dB, 0.375dB Step (Note 1) & +12dB ~ -115dB, 0.5dB Step
Speaker-Amp	No	Yes
Master Clock Reference for PLL Mode	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz	11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz
External Clock Mode Master Clock	256fs, 512fs, 1024fs	256fs, 384fs, 512fs, 1024fs
Power Supply Current **(Stereo Recording)** **(Headphone Playback)**	 typ. 7.3mA typ. 10.6mA	 typ. 3.3mA typ. 3.6mA
Package	32QFN (4 x 4mm, 0.4mm pitch)	36QFN (5 x 5mm, 0.4mm pitch)

Note 1. ALC and Volume circuits are shared by input and output. Therefore, it is impossible to use ALC and Volume control function at the same time for both recording and playback mode.

■ Compatibility with AK4953

1. Function

Function	AK4953	AK4953A
Headphone Hi-Z Mode	No	Yes

2. Register

Addr	Bit	AK4953	AK4953A
05H	D2	0 (Pull-down by 10Ω)	0: Pull-down by 10Ω (Default) 1: Hi-Z

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MPWR1	O	MIC Power Supply Pin for Microphone 1
2	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
3	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
4	PDN	I	Power-down & Reset When "L", the AK4953A is in power-down mode and is held in reset. The AK4953A must be always reset upon power-up.
5	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
6	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
7	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L")
	CAD0	I	Chip Address Select Pin (I2C pin = "H")
8	SDTI	I	Audio Serial Data Input Pin
9	LRCK	I/O	Input/Output Channel Clock Pin
10	BICK	I/O	Audio Serial Data Clock Pin
11	SDTO	O	Audio Serial Data Output Pin
12	TVDD	-	Digital I/O Power Supply Pin, 1.6 ~ 3.5V
13	VSS2	-	Ground 2 Pin
14	MCKI	I	External Master Clock Input Pin
15	MCKO	O	Master Clock Output Pin
16	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
17	SVDD	-	Speaker-Amp Power Supply Pin, 0.9 ~ 5.5V
18	VSS4	-	Ground 4 Pin
19	SPN	O	Speaker-Amp Negative Output Pin
20	SPP	O	Speaker-Amp Positive Output Pin
21	DVDD	-	Digital Power Supply Pin, 1.6 ~ 2.0V
22	HPL	O	Lch Headphone-Amp Output Pin
23	HPR	O	Rch Headphone-Amp Output Pin
24	PVEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS3 with 2.2µF±50% capacitor in series.
25	VSS3	-	Ground 3 Pin
26	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2µF±50% capacitor in series.
27	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2µF±50% capacitor in series.
28	AVDD	-	Analog Power Supply Pin, 2.85 ~ 3.5V
29	VSS1	-	Ground 1 Pin
30	REGFIL	O	Regulator Ripple Filter Pin This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
31	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
32	LIN3	I	Lch Analog Input 3 Pin
33	RIN3	I	Rch Analog Input 3 Pin
34	LIN2	I	Lch Analog Input 2 pin
35	RIN2	I	Rch Analog Input 2 Pin
36	MPWR2	O	MIC Power Supply Pin for Microphone 2

Note 2. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3) must not be left floating.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR1, MPWR2, SPN, SPP, HPL, HPR, CP, CN, PVEE, LIN1/DMDAT, RIN1/DMCLK, LIN2, RIN2, LIN3, RIN3	These pins must be open.
Digital	MCKO	This pin must be open.
	MCKI	This pin must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V; Note 3)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	2.5	V
	Digital I/O	TVDD	–0.3	6.0	V
	Speaker-Amp	SVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 5)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 6)		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 7)	Ta = 85°C (Note 8)	Pd1	-	660	mW
	Ta = 70°C (Note 9)	Pd2	-	900	mW

Note 3. All voltages are with respect to ground.
Note 4. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.
Note 5. LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins
Note 6. PDN, CSN, CCLK, CDTIO, SDTI, LRCK, BICK and MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.
Note 7. In case that PCB wiring density is 100% over. This power is the AK4953A internal dissipation that does not include power dissipation of externally connected speakers.
Note 8. The Speaker Amplifier is not available.
Note 9. The Speaker Amplifier is available.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 3)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	2.85	3.3	3.5	V
(Note 10)	Digital	DVDD	1.6	1.8	2.0	V
	Digital I/O	TVDD	DVDD	3.3	3.5	V
	SPK-Amp	SVDD	0.9	3.3	5.5	V

Note 3. All voltages are with respect to ground.

Note 10. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

*** When SVDD is powered ON and the PDN pin is "L", AVDD, DVDD or TVDD can be powered ON/OFF. When TVDD is powered ON and the PDN pin is "L", AVDD, DVDD or SVDD can be powered ON/OFF. When the AK4953A is changed from power down state to power ON, the PDN pin must be "H" after all power supplies are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=TVDD=SVDD=3.3V, DVDD=1.8V; VSS1=VSS2=VSS3=VSS4=0V; fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Units
MIC Amplifier: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins						
Input Resistance			20	30	40	kΩ
Gain	MGAIN2-0 bits = "000"		-1	0	+1	dB
	MGAIN2-0 bits = "001"		+11	+12	+13	dB
	MGAIN2-0 bits = "010"		+15	+16	+17	dB
	MGAIN2-0 bits = "011"		+19	+20	+21	dB
	MGAIN2-0 bits = "100"		+22	+23	+24	dB
	MGAIN2-0 bits = "101"		+25	+26	+27	dB
	MGAIN2-0 bits = "110"		+28	+29	+30	dB
MIC Power Supply: MPWR1, MPWR2 pins						
Output Voltage			2.1	2.3	2.5	V
Output Noise Level (A-weighted)			-	-108	-	dBV
PSRR (f = 1kHz) (Note 11)			-	100	-	dB
Load Resistance			1.0	-	-	kΩ
Load Capacitance			-	-	30	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 pins → ADC → Programmable Filter (IVOL=0dB, EQ=ALC=OFF) → SDTO						
Resolution			-	-	24	Bits
Input Voltage		(Note 12)	0.21	0.24	0.27	Vpp
		(Note 13)	2.16	2.4	2.64	Vpp
S/(N+D) (-1dBFS)	fs=44.1kHz BW=20kHz	(Note 12)	72	82	-	dBFS
		(Note 13)	-	85	-	dBFS
	fs=96kHz BW=40kHz	(Note 12)	-	79	-	dBFS
		(Note 13)	-	80	-	dBFS
D-Range (−60dBFS, A-weighted)		(Note 12)	78	88	-	dB
		(Note 13)	-	96	-	dB
S/N (A-weighted)		(Note 12)	78	88	-	dB
		(Note 13)	-	96	-	dB
Interchannel Isolation		(Note 12)	75	90	-	dB
		(Note 13)	-	100	-	dB
Interchannel Gain Mismatch		(Note 12)	-	0	0.8	dB
		(Note 13)	-	0	0.8	dB

Note 11. PSR is applied to AVDD with 500mpVpp sine wave.
Note 12. MGAIN2-0 bits = "011" (+20dB)
Note 13. MGAIN2-0 bits = "000" (0dB)

Parameter			min	typ	max	Units
DAC Characteristics:						
Resolution			-	-	24	Bits
Headphone-Amp Characteristics: DAC → HPL, HPR pins, ALC=OFF, OVOL=DVOL= 0dB, R_L=16Ω						
Output Voltage (0dBFS)		(0dBFS)	-	1.75	-	Vpp
		(-3dBFS)	1.11	1.24	1.37	Vpp
S/(N+D)	(0dBFS)	fs=44.1kHz, BW=20kHz (Note 14)	-	80	-	dB
	(-3dBFS)	fs=44.1kHz, BW=20kHz	70	80	-	dB
		fs=96kHz, BW=40kHz	-	77	-	dB
S/N (A-weighted)			86	96	-	dB
Interchannel Isolation			75	90	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Output Offset Voltage			- 1	0	+ 1	mV
PSRR (f = 1kHz) (Note 15)			-	80	-	dB
Load Resistance			16	-	-	Ω
Load Capacitance			-	-	300	pF
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, OVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage (Note 16)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SPKG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 17)			-	0.9	-	Vrms
S/(N+D)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	70	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	70	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SPKG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 17)			-	20	-	dB
S/N (A-weighted)			85	95	-	dB
Output Offset Voltage			-30	0	+30	mV
PSRR (f = 1kHz) (Note 18)			-	50	-	dB
Load Resistance			6.8	8	-	Ω
Load Capacitance			-	-	30	pF

Note 14. When CPCK bit = "1".

Note 15. PSR is applied to AVDD or DVDD with 500mpVpp sine wave.

Note 16. The output level is calculated by assuming that output signals are not clipped. In the actual case, the output signal is clipped when DAC outputs 0dBFS signal. Therefore, DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is not clipped.

Note 17. When SVDD = 1.5V.

Note 18. PSR is applied to AVDD or SVDD with 500mpVpp sine wave.

Parameter			min	typ	max	Units
Power Supplies:						
Power Up (PDN pin = "H")						
	MIC + ADC + DAC + Headphone out					
		AVDD+DVDD+TVDD (Note 19)	-	8.9	13.4	mA
		AVDD+DVDD+TVDD (Note 20)	-	6.1	-	mA
		SVDD (No Load)	-	11	17	μA
	MIC + ADC + DAC + Speaker out					
		AVDD+DVDD+TVDD (Note 21)	-	7.8	11.7	mA
		AVDD+DVDD+TVDD (Note 22)	-	5.1	-	mA
		SVDD (No Load)	-	1.3	2.0	mA
	MIC + ADC (Note 23)					
		AVDD+DVDD+TVDD	-	3.3	-	mA
	DAC + Headphone out (Note 24)					
		AVDD+DVDD+TVDD	-	3.6	-	mA
Power Down (PDN pin = "L") (Note 25)						
	AVDD+DVDD+TVDD+SVDD		-	1	10	μA
	SVDD (Note 26)		-	0	10	μA

Note 19. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMHPL=PMHPR= PMVCM=PMPLL=MCKO=PMBP=PMMP=M/S bits = "1". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.6 mA (typ), DVDD= 2.2 mA (typ), TVDD= 2.1 mA (typ).

Note 20. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMADL=PMADR=PMDAC=PMHPL=PMHPR= PMVCM=PMBP=PMMP bits = "1", and PMPFIL bit = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.2 mA (typ), DVDD= 1.8 mA(typ), TVDD= 0.1 mA (typ).

Note 21. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMSPK=PMVCM= PMPLL=MCKO=PMBP=PMMP=M/S bits = "1". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.9 mA (typ), DVDD= 1.8 mA (typ), TVDD= 2.1 mA (typ).

Note 22. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMADL=PMADR=PMDAC=PMSPK=PMVCM= PMBP=PMMP bits = "1", and PMPFIL bit = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.6 mA (typ), DVDD= 1.4 mA(typ), TVDD= 0.1 mA (typ).

Note 23. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMADL=PMADR=PMVCM bits = "1", and PMPFIL bit = "0". AVDD= 2.2 mA (typ), DVDD= 1.0 mA(typ), TVDD= 0.1 mA (typ).

Note 24. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMDAC=PMHPL=PMHPR=PMVCM bits = "1", and PMPFIL bit = "0". AVDD= 2.5 mA (typ), DVDD= 1.1 mA(typ), TVDD= 0 mA (typ).

Note 25. All digital input pins are fixed to TVDD or VSS2.

Note 26. When AVDD, DVDD, and TVDD are powered OFF.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD=TVDD=SVDD=3.3V, DVDD=1.8V; VSS1=VSS2=VSS3=VSS4=0V; fs=44.1kHz,
External Slave Mode, BICK=64fs; 1kHz, 0dBFS input; Headphone & Speaker = No output.

Mode	Power Management Bit							AVDD [mA]	DVDD [mA]	TVDD [mA]	SVDD [mA]	Total Power [mW]
	00H					01H						
	PMVCM	PMSPK	PMDAC	PMADL	PMADR	PMHPL	PMHPR					
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC	1	0	0	1	1	0	0	2.2	1.0	0.1	0	9.4
LIN1 (Mono) → ADC	1	0	0	1	0	0	0	1.5	1.0	0.1	0	7.1
DAC → HP	1	0	1	0	0	1	1	2.5	1.1	0	0	10.2
DAC → SPK	1	1	1	0	0	0	0	1.8	0.7	0	1.3	11.5
LIN1/RIN1 → ADC & DAC → HP	1	0	1	1	1	1	1	3.9	1.8	0.1	0	16.4
LIN1/RIN1 → ADC & DAC → SPK	1	1	1	1	1	0	0	3.1	1.4	0.1	1.3	17.4

Table 1. Power Consumption on Each Operation Mode (typ)

ADC FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta =25°C; AVDD=2.85~3.5V, DVDD=1.6~2.0V, TVDD=DVDD~3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 27)	±0.16dB	PB	0	-	17.3	kHz
	–0.66dB		-	19.4	-	kHz
	–1.1dB		-	19.9	-	kHz
	–6.9dB		-	22.1	-	kHz
Stopband		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 28)		GD	-	16	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz

ADC FILTER CHARACTERISTICS (fs=96kHz)

(Ta =25°C; AVDD=2.85~3.5V, DVDD=1.6~2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 27)	±0.16dB	PB	0	-	37.7	kHz
	–0.66dB		-	42.2	-	kHz
	–1.1dB		-	43.3	-	kHz
	–6.9dB		-	48.0	-	kHz
Stopband		SB	56.8	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 28)		GD	-	16	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	7.4	-	Hz
	–0.5dB		-	21.8	-	Hz
	–0.1dB		-	47.9	-	Hz

Note 27. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 28. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the signal through the programmable filters (First HPF + First LPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 4/fs from the value above if there is no phase change by the IIR filter.

DAC FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
DAC Digital Filter (LPF):						
Passband (Note 29)	±0.05dB −6.0dB	PB	0 -	- 22.05	20.0 -	kHz kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 30)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

DAC FILTER CHARACTERISTICS (fs=96kHz)

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
DAC Digital Filter (LPF):						
Passband (Note 29)	±0.05dB −6.0dB	PB	0 -	- 48.0	43.5 -	kHz kHz
Stopband		SB	52.5	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 30)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 40.0kHz		FR	-	±1.0	-	dB

Note 29. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 30. A calculating delay time which induced by digital filtering. This time is from setting the 24bit data of both channels to input register to the output of analog signal. For the signal through the programmable filters (First HPF + First LPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 7/fs from the value above if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Units
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)						
High-Level Input Voltage	(TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
	(TVDD < 2.2V)		80%TVDD	-	-	V
Low-Level Input Voltage	(TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
	(TVDD < 2.2V)		-	-	20%TVDD	V
Audio Interface & Serial µP Interface (CDTIO, SDA, MCKO, BICK, LRCK, SDTO pins Output)						
High-Level Output Voltage	(Iout = –80µA)	VOH	TVDD–0.2	-	-	V
Low-Level Output Voltage						
	(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
	(SDA pin, 2.0V ≤ TVDD ≤ 3.5V: Iout = 3mA)	VOL2	-	-	0.4	V
	(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Input Leakage Current		Iin	-	-	±10	µA
Digital MIC Interface (DMDAT pin Input ; DMIC bit = "1")						
High-Level Input Voltage		VIH3	65%AVDD	-	-	V
Low-Level Input Voltage		VIL3	-	-	35%AVDD	V
Digital MIC Interface (DMCLK pin Output ; DMIC bit = "1")						
High-Level Output Voltage	(Iout=–80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout= 80µA)	VOL3	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	24.576	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	96	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	24.576	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	96	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter			Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = BICK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	96	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period	PLL3-0 bits = "0010"		tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"		tBCK	-	1/(64fs)	-	ns
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High			tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	24.576	MHz
	384fs		fCLK	2.8224	-	18.432	MHz
	512fs		fCLK	3.7632	-	24.576	MHz
	1024fs		fCLK	7.5264	-	12.288	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing							
Frequency	256fs		fs	7.35	-	96	kHz
	384fs		fs	7.35	-	48	kHz
	512fs		fs	7.35	-	48	kHz
	1024fs		fs	7.35	-	12	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period			tBCK	156.25	-	-	ns
Pulse Width Low			tBCKL	65	-	-	ns
Pulse Width High			tBCKH	65	-	-	ns
External Master Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	24.576	MHz
	384fs		fCLK	2.8224	-	18.432	MHz
	512fs		fCLK	3.7632	-	24.576	MHz
	1024fs		fCLK	7.5264	-	12.288	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
Frequency			fs	7.35	-	96	kHz
Duty Cycle			Duty	-	50	-	%
BICK Output Timing							
Period		BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
		BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle			dBCK	-	50	-	%

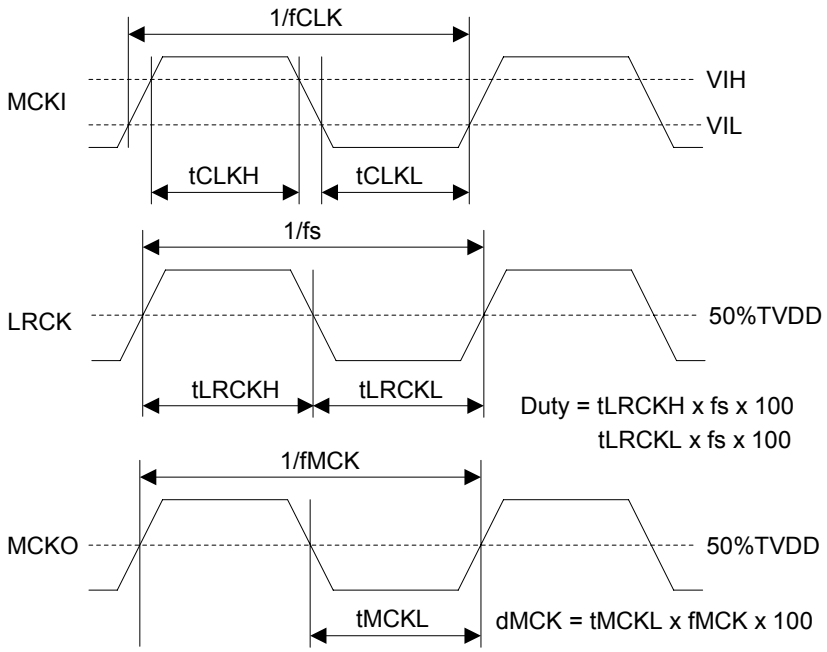
Parameter	Symbol	min	typ	max	Units
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 31)	tMBLR	–20	-	20	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–35	-	35	ns
BICK "↓" to SDTO	tBSD	–35	-	35	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 31)	tLRB	25	-	-	ns
BICK "↑" to LRCK Edge (Note 31)	tBLR	25	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	45	ns
BICK "↓" to SDTO	tBSD	-	-	45	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Control Interface Timing (3-wire Mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 32)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 32)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)(Note 34)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 35)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 31. BICK rising edge must not occur at the same time as LRCK edge.
Note 32. CCLK rising edge must not occur at the same time as CSN edge.
Note 33. I²C-bus is a trademark of NXP B.V.
Note 34. R_L=1kΩ/10% change (pull-up or TVDD)
Note 35. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter		Symbol	min	typ	max	Units
Digital Audio Interface Timing; fs = 7.35kHz ~ 48kHz, C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	ns
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tSDS	50	-	-	ns
DMDAT Hold Time		tSDH	0	-	-	ns
Power-down & Reset Timing						
PDN Pulse Width	(Note 36)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid	(Note 37)					
ADRST1-0 bits = "00"		tPDV	-	1059	-	1/fs
ADRST1-0 bits = "01"		tPDV	-	267	-	1/fs
ADRST1-0 bits = "10", "11"		tPDV	-	2115	-	1/fs

Note 36. The AK4953A can be reset by the PDN pin = "L".
Note 37. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram



Note 38. MCKO is not available at EXT Master mode.

Figure 2. Clock Timing (PLL/EXT Master mode)

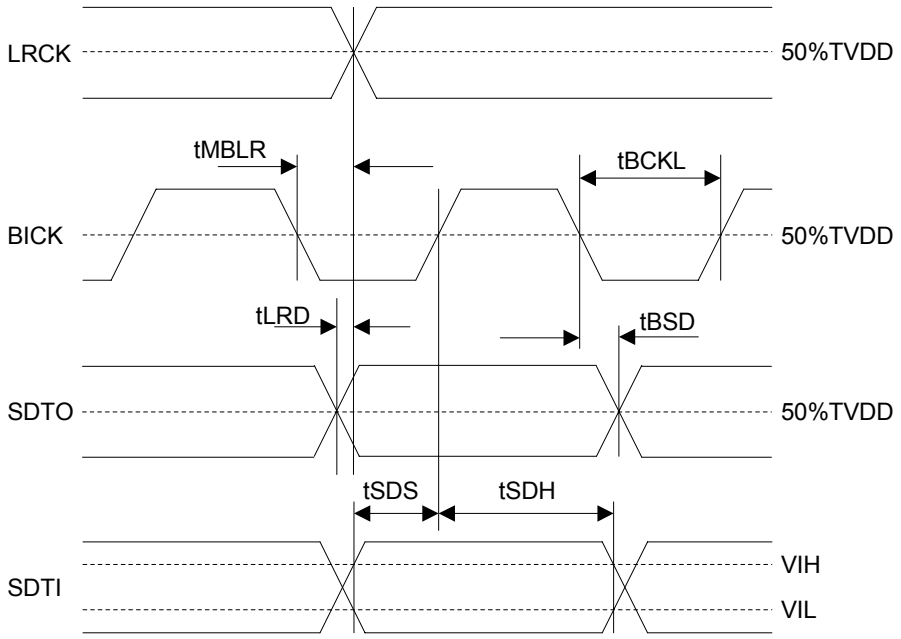


Figure 3. Audio Interface Timing (PLL/EXT Master mode)

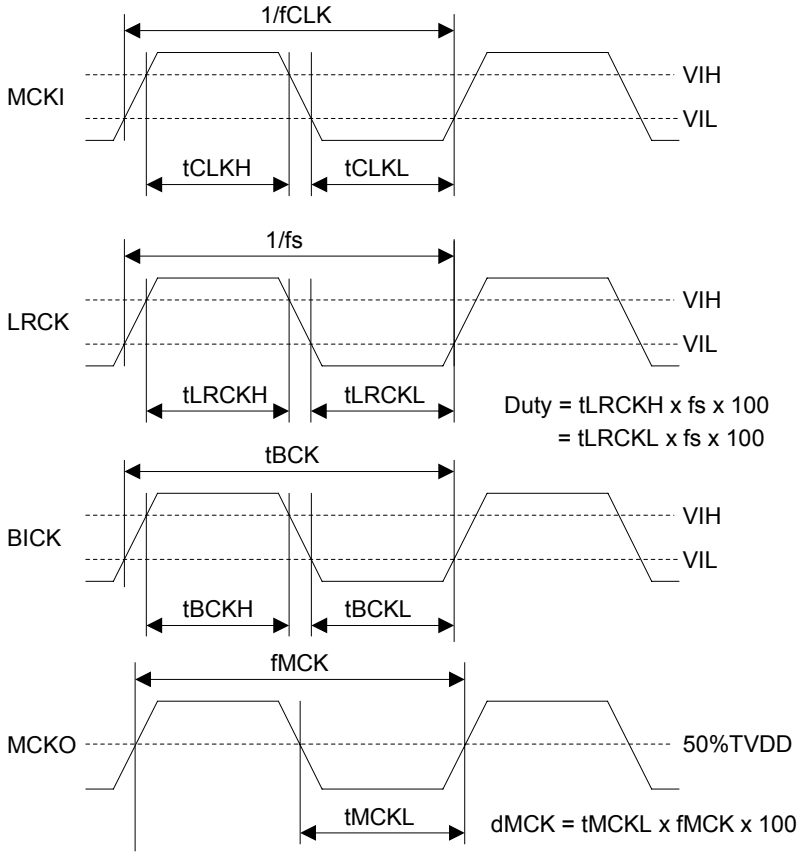


Figure 4. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

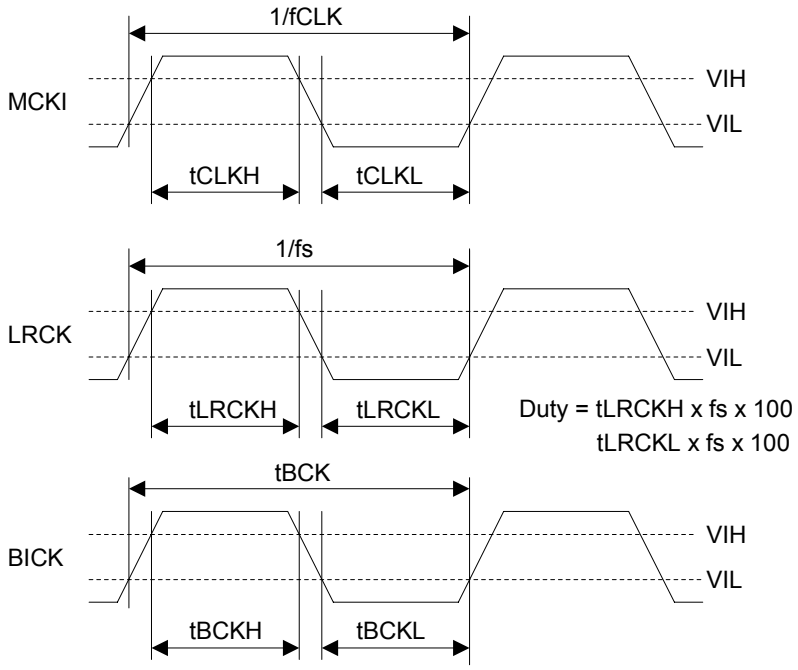


Figure 5. Clock Timing (EXT Slave mode)

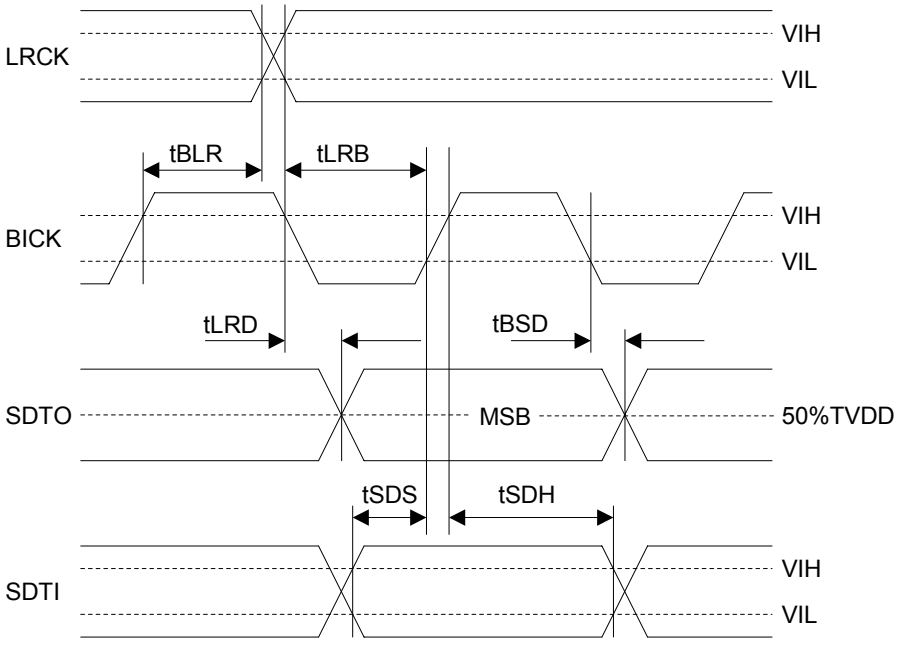


Figure 6. Audio Interface Timing (PLL/EXT Slave mode)

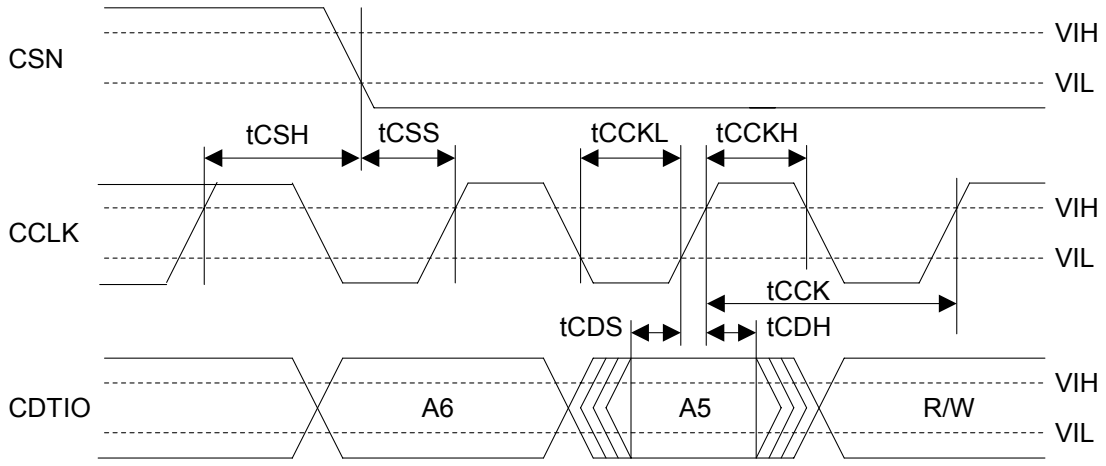


Figure 7. WRITE Command Input Timing

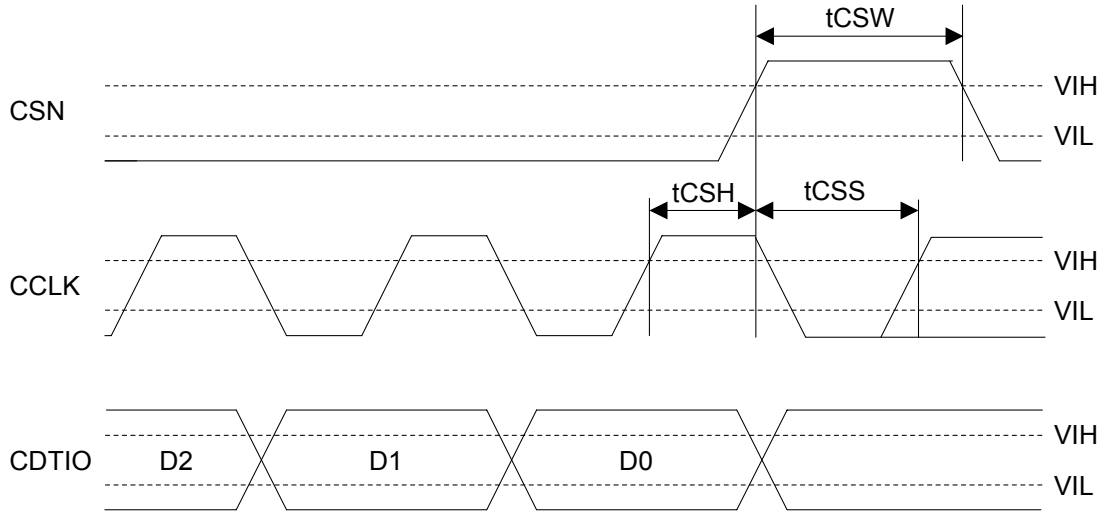


Figure 8. WRITE Data Input Timing

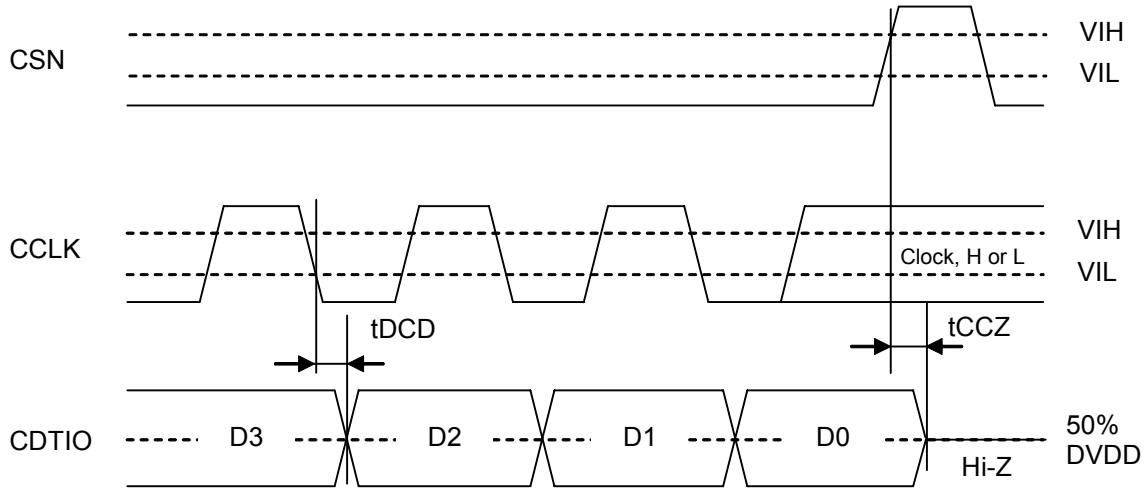


Figure 9. Read Data Output Timing

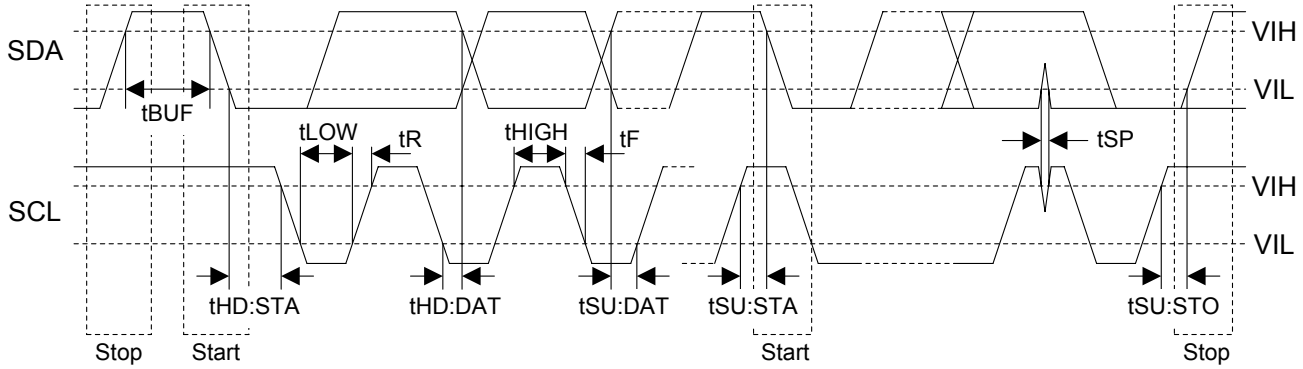


Figure 10. I^{2}C Bus Mode Timing

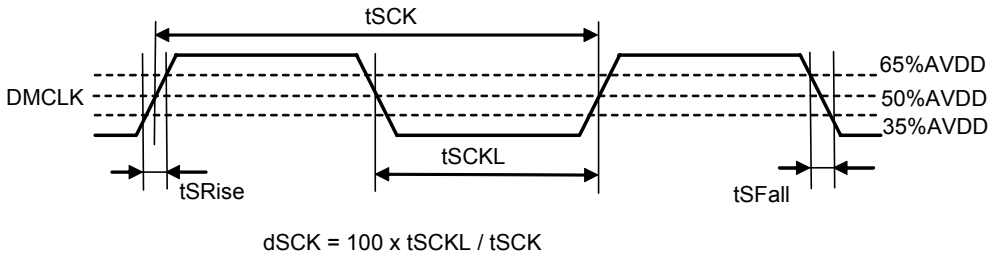


Figure 11. DMCLK Clock Timing

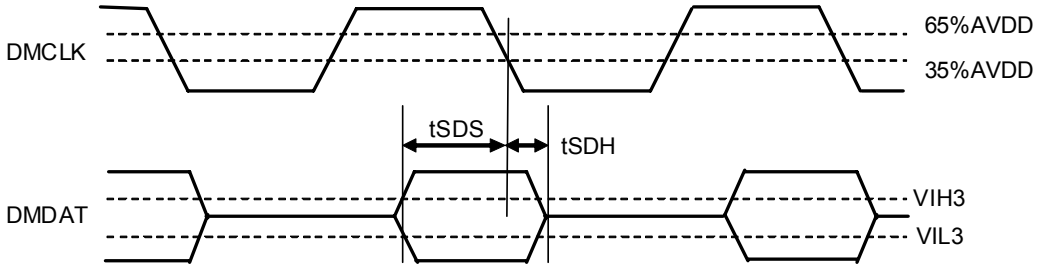


Figure 30. Audio Interface Timing (DCLKP bit = "1")

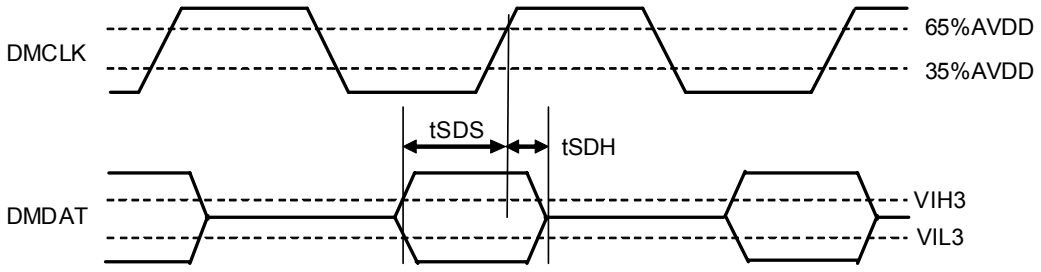


Figure 31. Audio Interface Timing (DCLKP bit = "0")

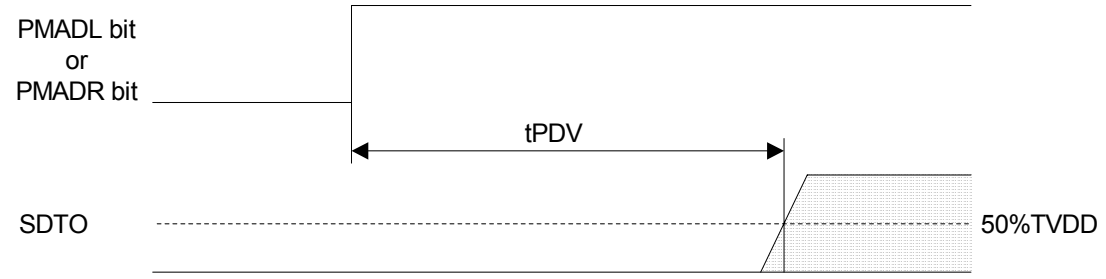


Figure 12. Power Down & Reset Timing 1

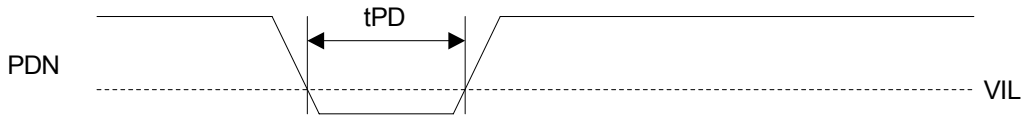


Figure 13. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 2, Table 3).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 39)	1	1	Table 5	Figure 14
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 5	Figure 15
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 5	Figure 16
EXT Slave Mode	0	0	x	Figure 17
EXT Master Mode	0	1	x	Figure 18

Note 39. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin.

Table 2. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: BICK pin)	0	L	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	0	L	Selected by FS3-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by FS3-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Note 40. When PMVCM bit = M/S bit = "1" and MCKI is input, LRCK and BICK are output, even if PMDAC bit = PMADL bit = PMADR bit = "0".

Table 3. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4953A is in power-down mode (PDN pin = "L") and when exits reset state, the AK44953 is in slave mode. After exiting reset state, the AK4953A goes to master mode by changing M/S bit = "1".

When the AK4953A is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4953A must be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 4. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4953A is supplied stable clocks or the sampling frequency is changed after PLL is powered-up (PMPLL bit = "0" → "1"), are shown in Table 5.

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)
2	0	0	1	0	BICK pin	32fs	2 ms
3	0	0	1	1	BICK pin	64fs	2 ms
4	0	1	0	0	MCKI pin	11.2896MHz	10 ms
6	0	1	1	0	MCKI pin	12MHz	10 ms
7	0	1	1	1	MCKI pin	24MHz	10 ms
12	1	1	0	0	MCKI pin	13.5MHz	10 ms
13	1	1	0	1	MCKI pin	27MHz	10 ms
Others	Others				N/A		

Note 41. PLL3-0 bits = "0000"(Default: N/A). When PLL mode is used, PLL3-0 bits must be set before PMPLL bit = "0" → "1".

Table 5. PLL Mode Setting (*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode

When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 6.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	DS bit	Sampling Frequency	
0	0	0	0	0	0	8kHz	(default)
1	0	0	0	1		12kHz	
2	0	0	1	0		16kHz	
3	0	0	1	1		24kHz	
4	0	1	0	0		7.35kHz	
5	0	1	0	1		11.025kHz	
6	0	1	1	0		14.7kHz	
7	0	1	1	1		22.05kHz	
8	1	0	0	0		32kHz	
9	1	0	0	1		48kHz	
10	1	0	1	0	1	64kHz	
11	1	0	1	1		96kHz	
12	1	1	0	0	0	29.4kHz	
13	1	1	0	1		44.1kHz	
15	1	1	1	1	1	88.2kHz	
Others	Others					N/A	

Table 6. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1" (Reference Clock = MCKI pin), (N/A: Not Available)

When PLL2 bit is "0" (PLL reference clock input is BICK pin), the sampling frequency is selected by FS1-0 bits (Table 7).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	DS bit	Sampling Frequency Range	
0	x	x	0	0	0	7.35kHz ≤ fs ≤ 12kHz	(default)
1	x	x	0	1		12kHz < fs ≤ 24kHz	
2	x	x	1	0		24kHz < fs ≤ 48kHz	
3	x	x	1	1	1	48kHz < fs ≤ 96kHz	
Others	Others					N/A	

Table 7. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" PLL Slave Mode 2 (PLL Reference Clock: BICK pin), (x: Don't care, N/A: Not Available)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK pin goes to "L" and the BICK pin goes to "H", and irregular frequency clock is output from the MCKO pin when MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin outputs "L" (Table 8).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After PMPLL bit "0" → "1"	"L" Output	Invalid	"H" Output	"L" Output
PLL Unlock (except the case above)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 10	Table 11	1fs Output

Table 8. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 10 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. DAC should be powered up by PMDAC bit "0" → "1" after PLL is locked.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except the case above)	"L" Output	Invalid
PLL Lock	"L" Output	Table 10

Table 9. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates MCKO, BICK and LRCK clocks. The MCKO output frequency is selected by PS1-0 bits (Table 10) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 11).

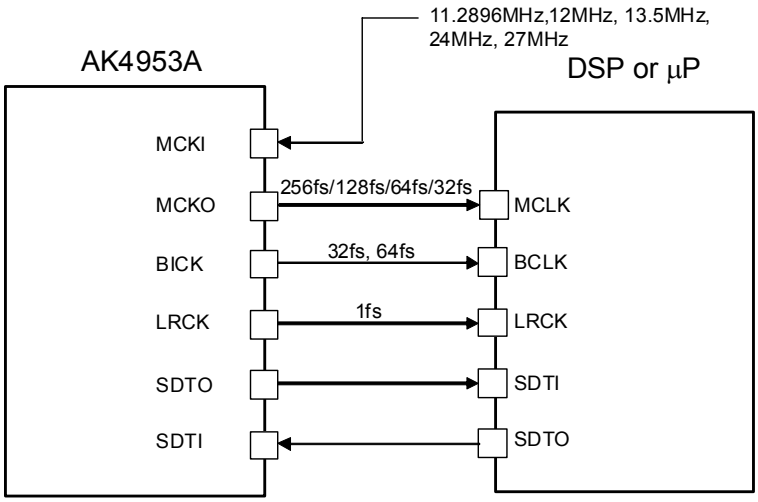


Figure 14. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 10. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 11. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = “1”, M/S bit = “0”)

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pins. The required clock for the AK4953A is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 5).

a) PLL reference clock: MCKI pin

The BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 10) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits and DS bit. (Table 6)

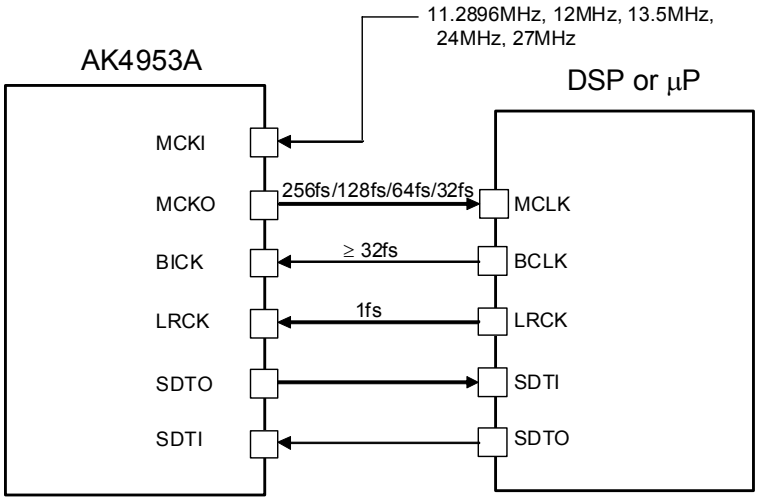


Figure 15. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK pin

The sampling frequency corresponds to a range from 7.35kHz to 96kHz by changing FS3-0 bits and DS bit (Table 7).

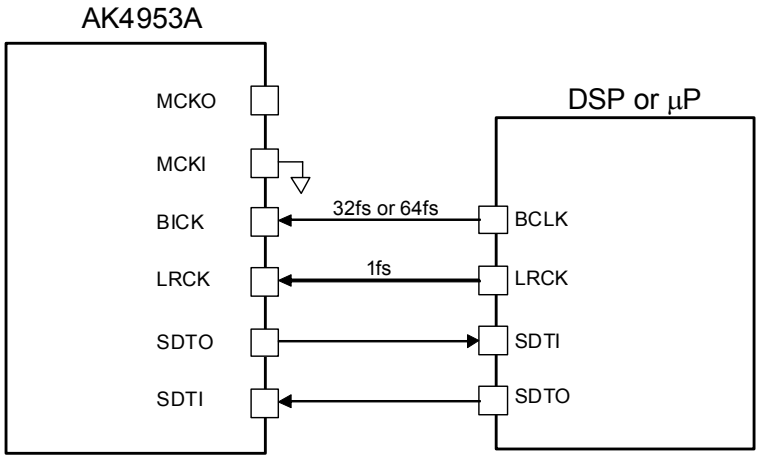


Figure 16. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4953A becomes EXT mode. Master clock can be input to the internal ADC and DAC directly from the MCKI pin without internal PLL circuit operation. This mode is compatible with I/F of a normal audio CODEC. The external clocks required to operate this mode are MCKI (256fs, 384fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) must be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS3-2 bits (Table 12).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	DS bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	0	0	0	256fs	7.35kHz ≤ fs ≤ 12kHz	(default)
1			0	1			12kHz < fs ≤ 24kHz	
2			1	0			24kHz < fs ≤ 48kHz	
3			1	1	1		48kHz < fs ≤ 96kHz	
4	0	1	0	0	0	384fs	7.35kHz ≤ fs ≤ 12kHz	
5			0	1			12kHz < fs ≤ 24kHz	
6			1	0			24kHz < fs ≤ 48kHz	
8	1	0	0	0	0	512fs	7.35kHz ≤ fs ≤ 12kHz	
9			0	1			12kHz < fs ≤ 24kHz	
10			1	0			24kHz < fs ≤ 48kHz	
12	1	1	0	0	0	1024fs	7.35kHz ≤ fs ≤ 12kHz	
Others	Others					N/A	N/A	

Table 12. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0"), (N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through HPL/HPR pins is shown in Table 13.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83 dB
384fs	83 dB
512fs	95 dB
1024fs	96 dB

Table 13. Relationship between MCKI and S/N of HPL/HPR pins

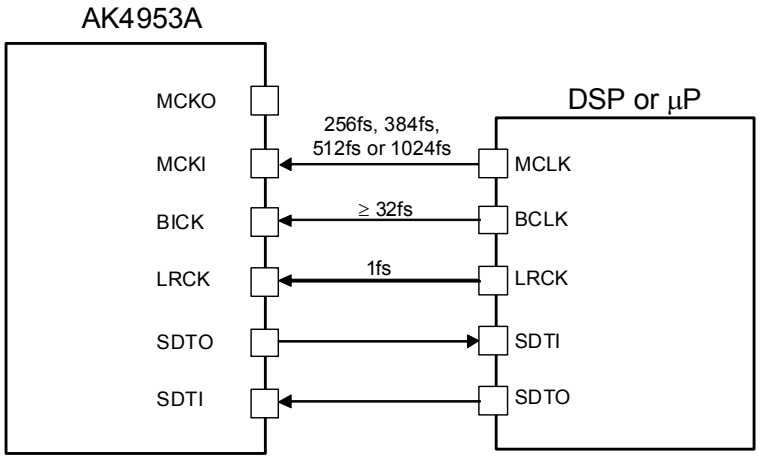


Figure 17. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1")

The AK4953A becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock can be input to the internal ADC and DAC directly from the MCKI pin without the internal PLL circuit operation. The external clock required to operate the AK4953A is MCKI (256fs, 384fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS3-2 bits (Table 14).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	DS bit	MCKI Input Frequency	Sampling Frequency Range	
0	0	0	0	0	0	256fs	7.35kHz ≤ fs ≤ 12kHz	(default)
1			0	1			12kHz < fs ≤ 24kHz	
2			1	0			24kHz < fs ≤ 48kHz	
3			1	1	1		48kHz < fs ≤ 96kHz	
4	0	1	0	0	0	384fs	7.35kHz ≤ fs ≤ 12kHz	
5			0	1			12kHz < fs ≤ 24kHz	
6			1	0			24kHz < fs ≤ 48kHz	
8	1	0	0	0	0	512fs	7.35kHz ≤ fs ≤ 12kHz	
9			0	1			12kHz < fs ≤ 24kHz	
10			1	0			24kHz < fs ≤ 48kHz	
12	1	1	0	0	0	1024fs	7.35kHz ≤ fs ≤ 12kHz	
Others	Others					N/A	N/A	

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = "0", M/S bit = "1") (N/A: Not Available)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be improved by using higher frequency of the master clock. The S/N of the DAC output through HPL/HPR pins is shown in Table 15.

MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
256fs	83 dB
384fs	83 dB
512fs	95 dB
1024fs	96 dB

Table 15. Relationship between MCKI and S/N of LOUT/ROUT pins

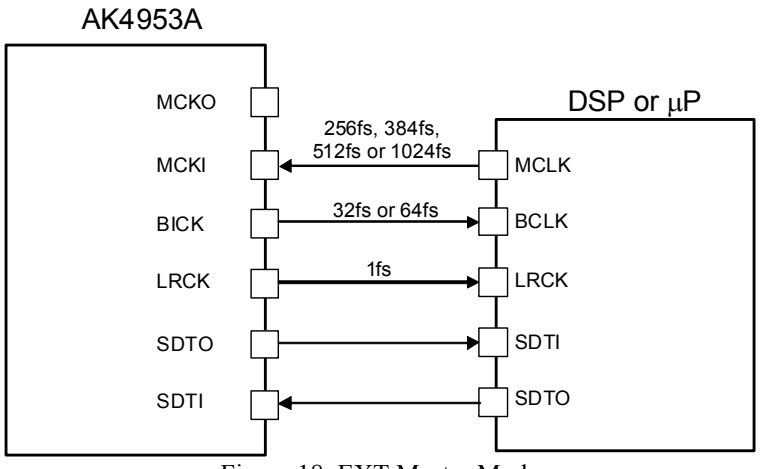


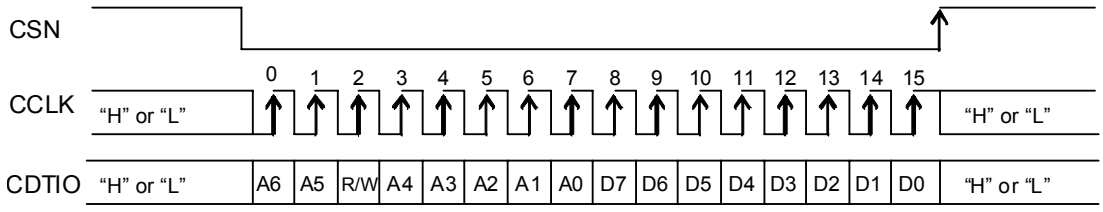
Figure 18. EXT Master Mode

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 16. BICK Output Frequency at Master Mode

■ System Reset

Upon power-up, the AK4953A must be reset by bringing the PDN pin = "L". This reset is released when a dummy command is input after the PDN pin = "H". This ensures that all internal registers reset to their initial value. Dummy command is executed by writing all "0" to the register address 00H. It is recommended to set the PDN pin = "L" before power up the AK4953A.



R/W: READ/WRITE ("1": WRITE)
A6-A0: Register Address (00H)
D7-D0: Control data (Input), (00H)

Figure 19. Dummy Command in 3-wired Serial Mode

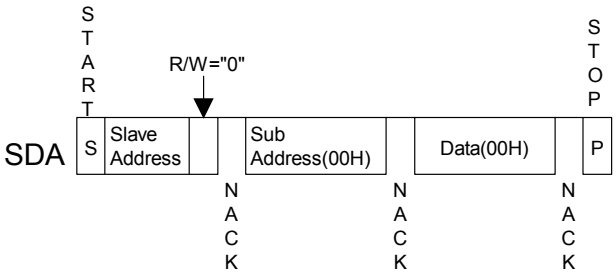


Figure 20. Dummy Command in I^2C-bus Mode

The ADC enters an initialization cycle when the PMADL or PMADR bit is changed from "0" to "1". The initialization cycle time is set by ADRST1-0 bits (Table 17). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, "0". The ADC output reflects the analog input signal after the initialization cycle is complete. When using a digital microphone, the initialization cycle is the same as ADC's.

Note 42. The initial data of ADC has offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer by setting ADRST1-0 bits or do not use the initial data of ADC.

ADRST1 bit	ADRST0 bit	Init Cycle					
		Cycle	fs = 8kHz	fs = 16kHz	fs = 44.1kHz	fs = 96kHz	
0	0	1059/fs	132.4ms	66.2ms	24ms	11ms	(default)
0	1	267/fs	33.4ms	16.7ms	N/A	N/A	
1	0	2115/fs	264.4ms	132.2ms	48ms	22ms	
1	1	2115/fs	264.4ms	132.2ms	48ms	22ms	

Table 17. ADC Initialization Cycle (N/A: Not Available)

■ Audio Interface Format

Four types of data formats are available and selected by setting the DIF1-0 bits (Table 18). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4953A in master mode, but must be input to the AK4953A in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑") of BICK.

Mode	DIF1 bit	DIF0 bit	SDTO (ADC)	SDTI (DAC)	BICK	Figure	
0	0	0	24bit MSB justified	24bit LSB justified	≥ 48fs	Figure 21	
1	0	1	24bit MSB justified	16bit LSB justified	≥ 32fs	Figure 22	
2	1	0	24bit MSB justified	24bit MSB justified	≥ 48fs	Figure 23	(default)
3	1	1	I^2S Compatible	I^2S Compatible	=32fs or ≥ 48fs	Figure 24	

Table 18. Audio Interface Format

If 24-bit (16-bit) data, the output of ADC, is converted to 8-bit data by removing LSB 16-bit (8-bit), "–1" at 24-bit (16bit) data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–65536" at 24-bit ("–256" at 16-bit) data which is a large offset. This offset can be removed by adding the offset of "32768" at 24-bit ("128" at 16-bit) to 24-bit (16-bit) data before converting to 8-bit data.

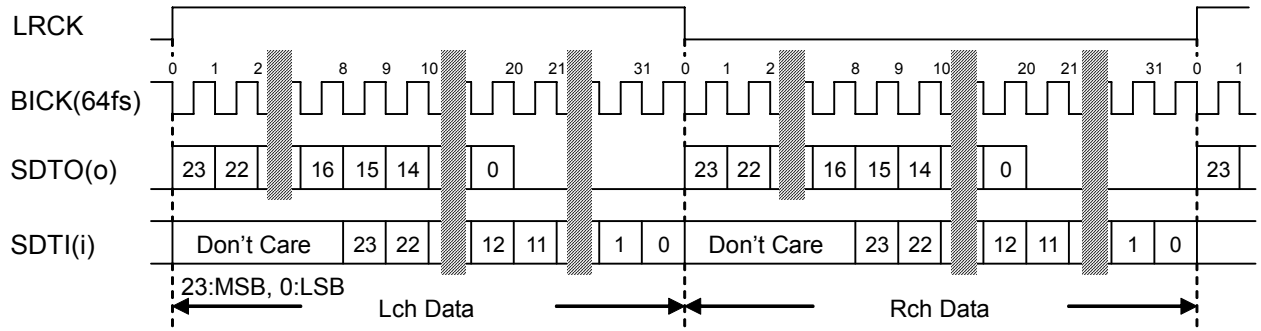


Figure 21. Mode 0 Timing

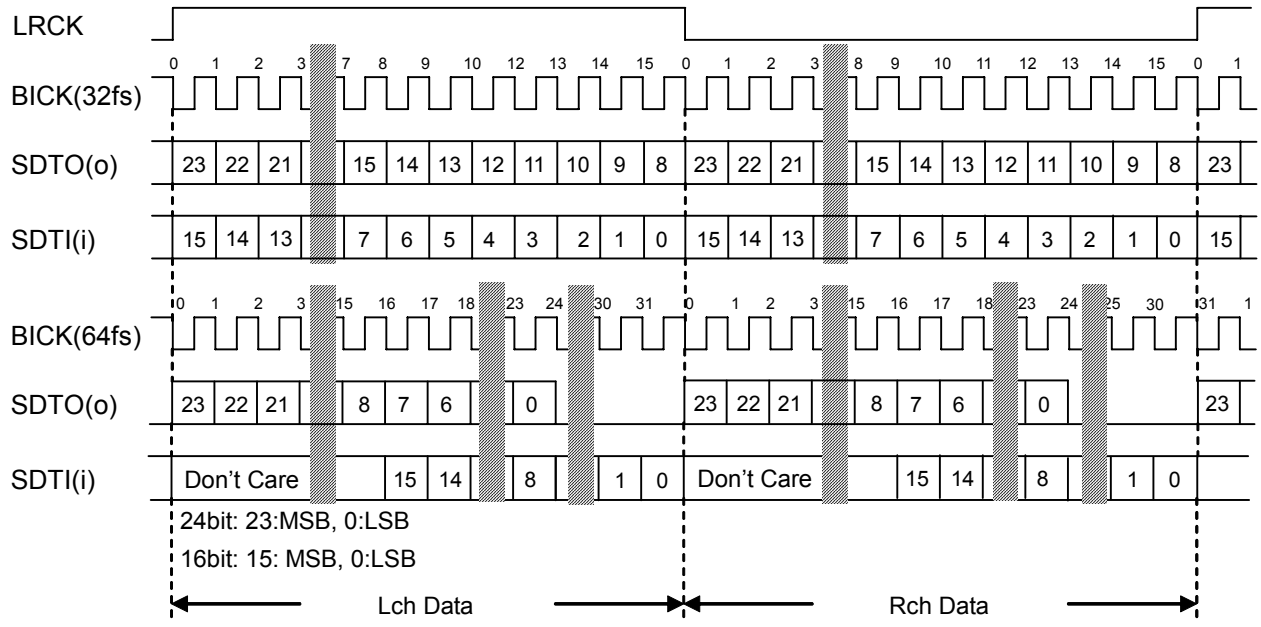


Figure 22. Mode 1 Timing

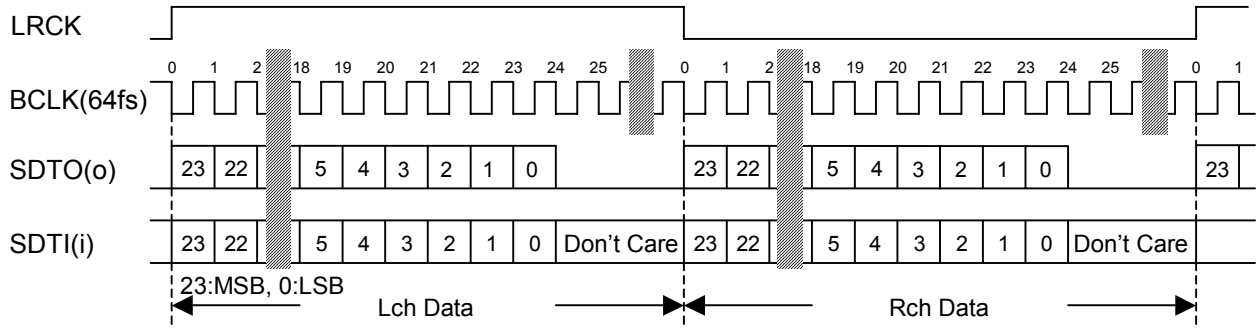


Figure 23. Mode 2 Timing

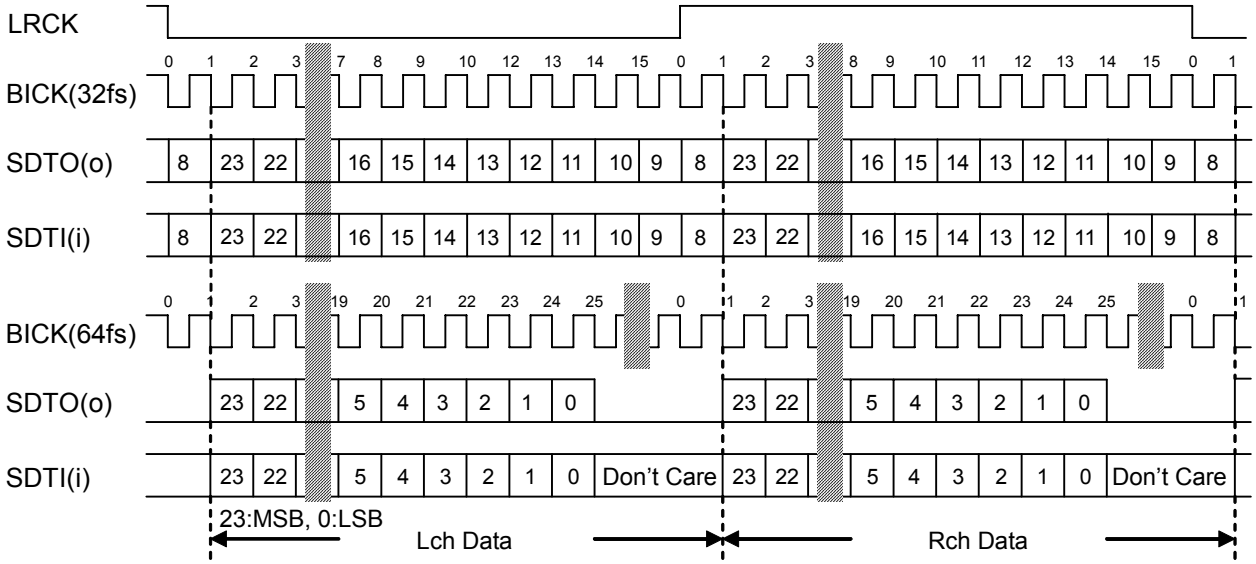


Figure 24. Mode 3 Timing

■ Mono/Stereo Mode

PMADL, PMADR, PMDML and PMDMR bits set mono/stereo ADC operation. When changing ADC operation and analog/digital microphone, PMADL, PMADR, PMDML and PMDMR bits must be set "0" at first. When DMIC bit = "1", PMADL and PMADR bit settings are ignored. When DMIC bit = "0", PMDML and PMDMR bit settings are ignored.

PMADL bit	PMADR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 19. Mono/Stereo ADC operation (Analog MIC)

PMDML bit	PMDMR bit	ADC Lch data	ADC Rch data	
0	0	All "0"	All "0"	(default)
0	1	Rch Input Signal	Rch Input Signal	
1	0	Lch Input Signal	Lch Input Signal	
1	1	Lch Input Signal	Rch Input Signal	

Table 20. Mono/Stereo ADC operation (Digital MIC)

■ MIC/LINE Input Selector

The AK4953A has an input selector. INL1-0 and INR1-0 bits select LIN1/LIN2 /LIN3 and RIN1/RIN2/RIN3, respectively. When DMIC bit = "1", digital microphone input is selected regardless of INL and INR bits.

DMIC bit	INL1 bit	INL0 bit	INR1 bit	INR0 bit	Lch	Rch	
0	0	0	0	0	LIN1	RIN1	(default)
	0	0	0	1	LIN1	RIN2	
	0	0	1	0	LIN1	RIN3	
	0	1	0	0	LIN2	RIN1	
	0	1	0	1	LIN2	RIN2	
	0	1	1	0	LIN2	RIN3	
	1	0	0	0	LIN3	RIN1	
	1	0	0	1	LIN3	RIN2	
	1	0	1	0	LIN3	RIN3	
	Others				N/A	N/A	
1	x	x	x	x	Digital Microphone		

Table 21. MIC/Line In Path Select (x: Don't care, N/A: Not available)

■ MIC Gain Amplifier

The AK4953A has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN3-0 bits (Table 22). The typical input impedance is 30kΩ.

MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0	0dB	
0	0	1	+12dB	
0	1	0	+16dB	
0	1	1	+20dB	(default)
1	0	0	+23dB	
1	0	1	+26dB	
1	1	0	+29dB	
Others			N/A	

Table 22. Input Gain (N/A: Not available)

■ MIC Power

When PMMP bit = "1", the MPWR1 or MPWR2 pin supplies power for the microphones. This output voltage is typically 2.3V and the load resistance is minimum 1kΩ. In case of using two sets of stereo microphones, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR1 and MPWR2 pins (Figure 25).

PMMP bit	MPSEL bit	Output	
0	x	Hi-Z	(default)
1	0	MPWR1 pin	
	1	MPWR2 pin	

Table 23. MIC Power

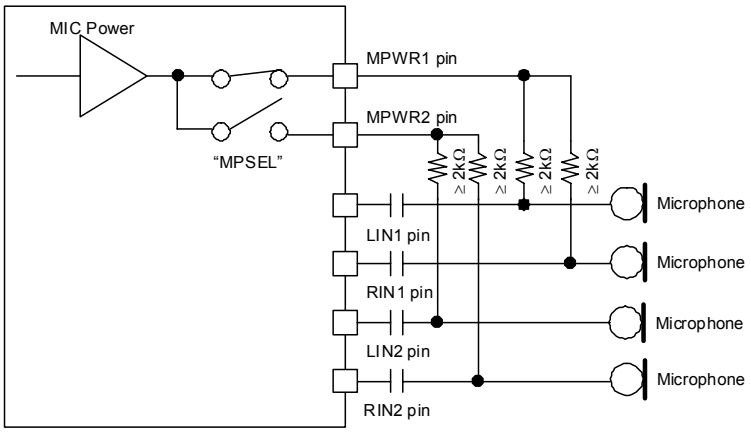


Figure 25. MIC Block Circuit

■ Digital MIC

1. Connection to Digital Microphones

The AK4953A can be connected to a digital microphone by setting DMIC bit = "1", and it supports sampling frequency up to 48kHz. When DMIC bit is set to "1", the LIN1 and RIN1 pins become DMDAT (digital microphone data input) and DMCLK (digital microphone clock supply) pins respectively. The same voltage as AVDD must be provided to the digital microphone. The Figure 26 and Figure 27 show mono/stereo connection examples. The DMCLK signal is output from the AK4953A, and the digital microphone outputs 1bit data, which generated by ΔΣModulator using, from DMDAT. PMDML/R bits control power up/down of the digital block (Decimation Filter and Digital Filter). PMADL/PMADR bits settings do not affect the digital microphone power management. The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4953A is powered down (PDN pin= "L"), the DMCLK and DMDAT pins are floating state. Pull-down resistors must be connected to the DMCLK and DMDAT pins externally to avoid this floating state.

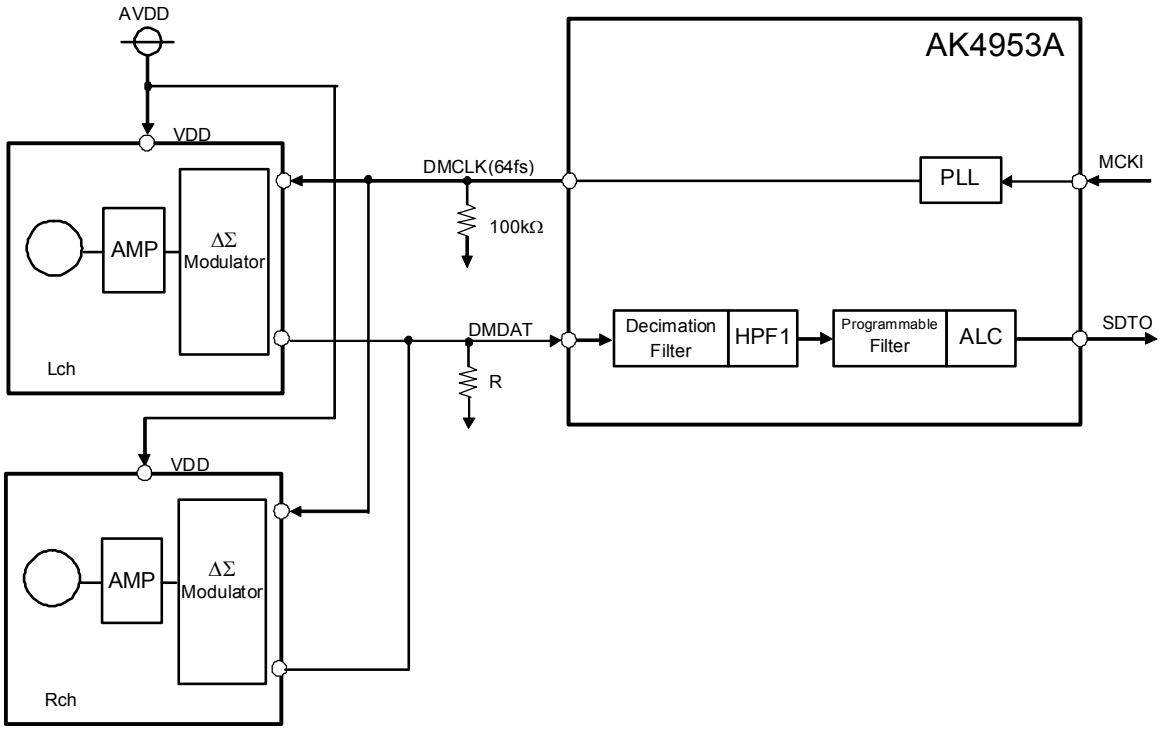


Figure 26. Connection Example of Stereo Digital MIC

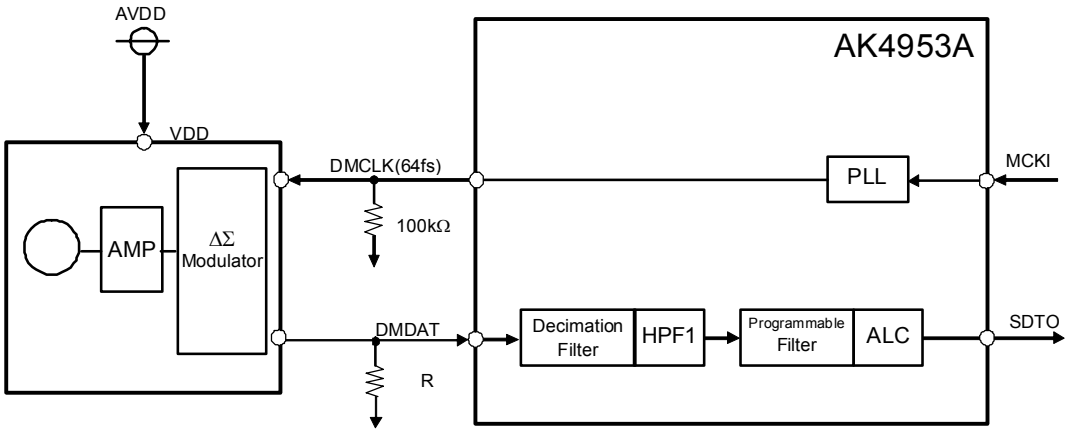


Figure 27. Connection Example of Mono Digital MIC

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = "1, Lch data is input to the decimation filter if DMCLK = "H", and Rch data is input if DMCLK = "L". When DCLKP bit = "0", Rch data is input to the decimation filter if DMCLK = "H", and Lch data is input if DMCLK = "L". The DMCLK pin outputs "L" when DCLKE bit = "0", and only supports 64fs. In this case, necessary clocks must be supplied to the AK4953A for ADC operation. The output data through "the Decimation and Digital Filters" is 24bit full scale when the 1bit data density is 0%~100%.

DCLKP bit	DMCLK = "H"	DMCLK = "L"	
0	Rch	Lch	(default)
1	Lch	Rch	

Table 24. Data In/Output Timing with Digital MIC

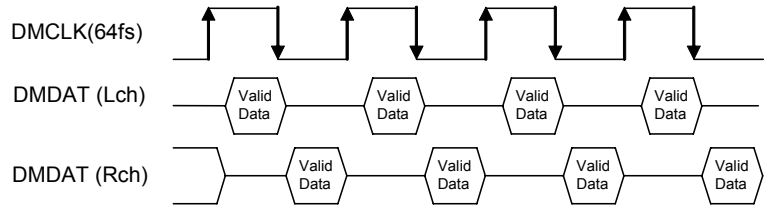


Figure 28. Data In/Output Timing with Digital MIC (DCLKP bit = "1")

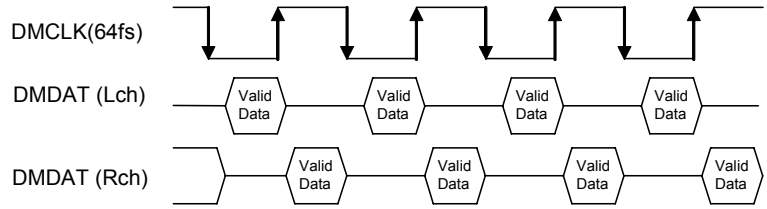
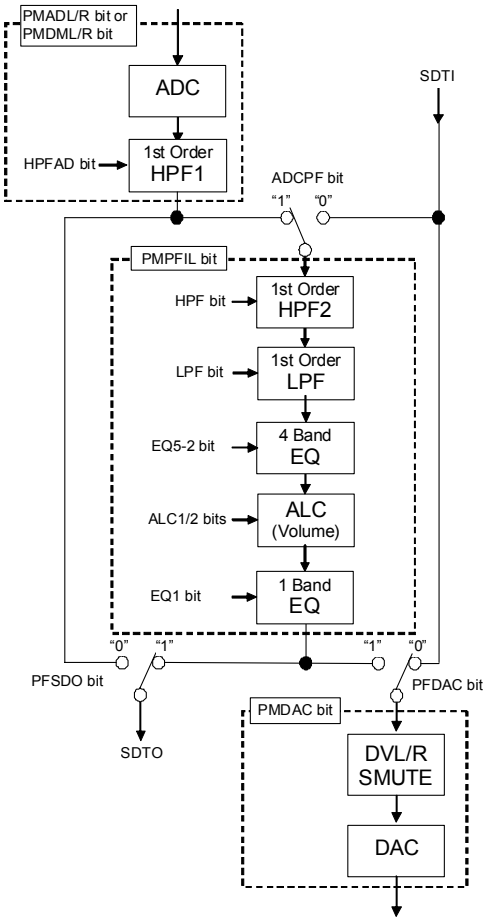


Figure 29. Data In/Output Timing with Digital MIC (DCLKP bit = "0")

■ Digital Block

The digital block consists of the blocks shown in Figure 30. Recording path and playback path is selected by setting ADCPF bit, PFDAC bit and PFSDO bit. (Figure 31 ~ Figure 34, Table 25)



(1) ADC: Includes the Digital Filter (LPF) for ADC as shown in "FILTER CHRACTERISTICS".
(2) HPF1: Includes the Digital Filter (HPF) for ADC as shown in "FILTER CHRACTERISTICS".
(3) DAC: Includes the Digital Filter (LPF) for DAC as shown in "FILTER CHRACTERISTICS".
(4) HPF2: High Pass Filter. Applicable for use as Wind-Noise Reduction Filter. (See "Digital Programmable Filter Circuit")
(5) LPF: Low Pass Filter (See "Digital Programmable Filter Circuit")
(6) 4 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(7) Volume: Input Digital Volume with ALC function. (See "Input Digital Volume" and "ALC Operation")
(8) 1 Band EQ: Applicable for use as Equalizer or Notch Filter. (See "Digital Programmable Filter Circuit")
(9) DVL/R, SMUTE: Digital volume with soft mute function for playback path (See "Output Digital Volume2")

Figure 30. Digital Block Path Select

Mode	ADCPF bit	PFDAC bit	PFSDO bit	Figure
Recording Mode 1	1	0	1	Figure 31
Playback Mode 1	0	1	0	Figure 32
Recording Mode 2 & Playback Mode 2 (Programmable Filter Bypass Mode: PMPFIL bit = "0")	x	0	0	Figure 33
Loopback Mode	1	1	1	Figure 34

Table 25. Recording Playback Mode (x: Don't care)

LPF bit, HPF bit, EQ0 bit, EQ1 bit, EQ2 bit, EQ3 bit, EQ4 bit, EQ5 bit, ACL1 bit and ALC2 bit must be "0" when changing those modes.

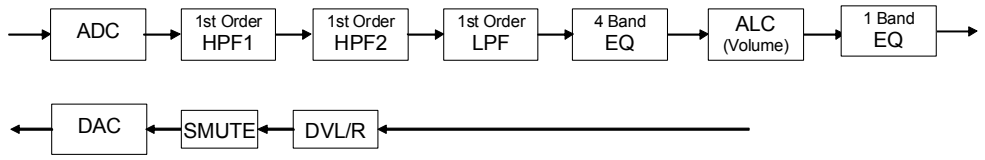


Figure 31. Path at Recording Mode 1 (default)

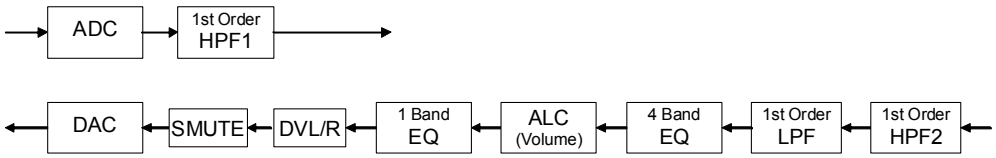


Figure 32. Path at Playback Mode 1

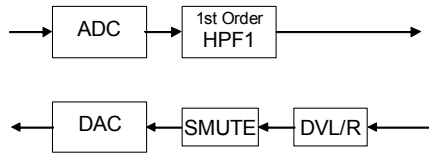


Figure 33. Path at Recording Mode 2 & Playback Mode 2

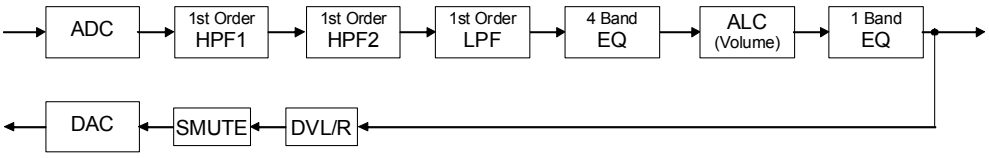


Figure 34. Path at Loopback Mode

■ Digital HPF1

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies of the HPF1 are set by HPFC1-0 bits (Table 26). It is proportional to the sampling frequency (fs) and default is 3.4Hz (@fs = 44.1kHz). HPFAD bit controls the ON/OFF of the HPF1 (HPF ON is recommended).

HPFC1 bit	HPFC0 bit	fc				
		fs=96kHz	fs=44.1kHz	fs=22.05kHz	fs=8kHz	
0	0	7.4Hz	3.4Hz	1.7Hz	0.62Hz	(default)
0	1	29.6Hz	13.6Hz	6.8Hz	2.47Hz	
1	0	236.8Hz	108.8Hz	54.4Hz	19.7Hz	
1	1	473.6Hz	217.6Hz	108.8Hz	39.5Hz	

Table 26. HPF1 Cut-off Frequency

■ Digital Programmable Filter Circuit

(1) High Pass Filter (HPF2)

Normally, this HPF is used for Wind-Noise Reduction. This is composed 1st order HPF. The coefficient of HPF is set by F1A13-0 bits and F1B13-0 bits. HPF bit controls ON/OFF of the HPF2. When the HPF2 is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when HPF bit = "0" or PMPFIL bit = "0". The HPF2 starts operation 4/fs(max) after when HPF bit=PMPFIL bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 43)
HPF: F1A[13:0] bits =A, F1B[13:0] bits =B
(MSB=F1A13, F1B13; LSB=F1A0, F1B0)

$$A = \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.0001 (fc min = 4.41Hz at 44.1kHz)

(2) Low Pass Filter (LPF)

This is composed with 1st order LPF. F2A13-0 bits and F2B13-0 bits set the coefficient of LPF. LPF bit controls ON/OFF of the LPF. When the LPF is OFF, the audio data passes this block by 0dB gain. The coefficient must be set when LPF bit = "0" or PMPFIL bit = "0". The LPF starts operation 4/fs(max) after when LPF bit =PMPFIL bit= "1" is set.

fs: Sampling frequency
fc: Cut-off frequency

Register setting (Note 43)
LPF: F2A[13:0] bits =A, F2B[13:0] bits =B
(MSB=F2A13, F2B13; LSB=F2A0, F2B0)

$$A = \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function

$$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$$

The cut-off frequency must be set as below.
fc/fs ≥ 0.05 (fc min = 2205Hz at 44.1kHz)

(3) 4-band Equalizer & 1-band Equalizer after ALC

This block can be used as Equalizer or Notch Filter. 4-band Equalizer (EQ2, EQ3, EQ4 and EQ5) is switched ON/OFF independently by EQ2, EQ3, EQ4 and EQ5 bits. The equalizer after ALC (EQ1) is controlled by EQ1 bit. When Equalizer is OFF, the audio data passes this block by 0dB gain. E1A15-0, E1B15-0 and E1C15-0 bits set the coefficient of EQ1. E2A15-0, E2B15-0 and E2C15-0 bits set the coefficient of EQ2. E3A15-0, E3B15-0 and E3C15-0 bits set the coefficient of EQ3. E4A15-0, E4B15-0 and E4C15-0 bits set the coefficient of EQ4. E5A15-0, E5B15-0 and E5C15-0 bits set the coefficient of EQ5. The EQx (x=1~5) coefficient must be set when EQx bit = "0" or PMPFIL bit = "0". EQ1-5 start operation 4/fs(max) after when EQx (x=1~5) = PMPFIL bit = "1"is set.

fs: Sampling frequency
$fo_1 \sim fo_5$: Center frequency
$fb_1 \sim fb_5$: Band width where the gain is 3dB different from center frequency
$K_1 \sim K_5$: Gain ($-1 \le K_n \le 3$)

Register setting (Note 43)
EQ1: E1A[15:0] bits =A_1, E1B[15:0] bits =B_1, E1C[15:0] bits =C_1
EQ2: E2A[15:0] bits =A_2, E2B[15:0] bits =B_2, E2C[15:0] bits =C_2
EQ3: E3A[15:0] bits =A_3, E3B[15:0] bits =B_3, E3C[15:0] bits =C_3
EQ4: E4A[15:0] bits =A_4, E4B[15:0] bits =B_4, E4C[15:0] bits =C_4
EQ5: E5A[15:0] bits =A_5, E5B[15:0] bits =B_5, E5C[15:0] bits =C_5
(MSB=E1A15, E1B15, E1C15, E2A15, E2B15, E2C15, E3A15, E3B15, E3C15, E4A15, E4B15, E4C15, E5A15, E5B15, E5C15 ; LSB= E1A0, E1B0, E1C0, E2A0, E2B0, E2C0, E3A0, E3B0, E3C0, E4A0, E4B0, E4C0, E5A0, E5B0, E5C0)

$$A_n = K_n \times \frac{\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}, \quad B_n = \cos(2\pi\, fo_n/fs) \times \frac{2}{1+\tan(\pi fb_n/fs)}, \quad C_n = -\frac{1-\tan(\pi fb_n/fs)}{1+\tan(\pi fb_n/fs)}$$

(n = 1, 2, 3, 4, 5)

Transfer function

$$H(z) = \{1 + h_2(z) + h_3(z) + h_4(z) + h_5(z)\} \times h_1(z)$$

$$h_n(z) = A_n \frac{1 - z^{-2}}{1 - B_n z^{-1} - C_n z^{-2}}$$

(n = 1, 2, 3, 4, 5)

The center frequency must be set as below.
$fo_n / fs < 0.497$

When gain of K is set to "-1", this equalizer becomes a notch filter. When EQ2 ~EQ5 is used as a notch filter, central frequency of a real notch filter deviates from the above-mentioned calculation, if its central frequency of each band is near. The control soft that is attached to the evaluation board has functions that revises a gap of frequency and calculates the coefficient. When its central frequency of each band is near, the central frequency should be revised and confirm the frequency response.

Note 43. [Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X must be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block when ALC bit is "1". When ADCPF bit is "1", ALC circuit operates at recording path. When ADCPF bit is "0", ALC circuit operates at playback path. ALC1 bit controls ON/OFF of ALC operation at recording path, and ALC2 bit controls of ON/OFF of ALC operation at playback path.

Note 44. In this section, VOL means IVL and IVR for recording path, OVL and OVR for playback path.
Note 45. In this section, ALC bit means ALC1 bit for recording path, ALC2 bit for playback path.
Note 46. In this section, REF means IREF for recording path, OREF for playback path.

1. ALC Limiter Operation

During ALC limiter operation, when either L or R channel output level exceeds the ALC limiter detection level (Table 27), the VOL value (same value for both L and R) is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 28). The VOL is then set to the same value for both channels.

When ZELMN bit = "0" (zero cross detection is enabled), the VOL value is changed by ALC limiter operation at the individual zero crossing points of L channel and R channel, or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 29). When ALC output level exceeds full-scale at LFST bit = "1", VOL values are immediately (Period: 1/fs) changed in 1step(L/R common). When ALC output level is less than full-scale, VOL values are changed at the individual zero crossing point of each channels or at the zero crossing timeout.

When ZELMN bit = "1" (zero cross detection is disabled), VOL value is immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds ALC limiter detection level.

LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ −2.5dBFS	−2.5dBFS > ALC Output ≥ −4.1dBFS	(default)
0	1	ALC Output ≥ −4.1dBFS	−4.1dBFS > ALC Output ≥ −6.0dBFS	
1	0	ALC Output ≥ −6.0dBFS	−6.0dBFS > ALC Output ≥ −8.5dBFS	
1	1	ALC Output ≥ −8.5dBFS	−8.5dBFS > ALC Output ≥ −12dBFS	

Table 27. ALC Limiter Detection Level / Recovery Counter Reset Level

LMAT1 bit	LMAT0 bit	ALC Limiter ATT Step				
		ALC Output ≥ LMTH	ALC Output ≥ FS	ALC Output ≥ FS + 6dB	ALC Output ≥ FS + 12dB	
0	0	1	1	1	1	(default)
0	1	2	2	2	2	
1	0	2	4	4	8	
1	1	1	2	4	8	

Table 28. ALC Limiter ATT Step

ZTM1 bit	ZTM0 bit		Zero Crossing Timeout Period				
			8kHz	16kHz	44.1kHz	96kHz	
0	0	128/fs	16ms	8ms	2.9ms	1.3ms	(default)
0	1	256/fs	32ms	16ms	5.8ms	2.7ms	
1	0	512/fs	64ms	32ms	11.6ms	5.3ms	
1	1	1024/fs	128ms	64ms	23.2ms	10.7ms	

Table 29. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

ALC recovery operation wait for the WTM2-0 bits (Table 30) to be set after completing ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 27) during the wait time, ALC recovery operation is executed. The VOL value is automatically incremented by RGAIN1-0 bits (Table 31) up to the set reference level (Table 32) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 29). The ALC recovery operation is executed in a period set by WTM2-0 bits. If the setting of ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, the ALC recovery operation is executed at a period set by ZTM1-0 bits.

For example, when the current VOL value is 30H and RGAIN1-0 bits are set to "01", VOL is changed to 32H by auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the VOL value exceeds the reference level (REF7-0), the VOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

ALC operations correspond to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to a microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation. The speed of first recovery operation is set by RFST1-0 bits (Table 34).

WTM2 bit	WTM1 bit	WTM0 bit		ALC Recovery Operation Waiting Period				
				8kHz	16kHz	44.1kHz	96kHz	
0	0	0	128/fs	16ms	8ms	2.9ms	1.3ms	(default)
0	0	1	256/fs	32ms	16ms	5.8ms	2.7ms	
0	1	0	512/fs	64ms	32ms	11.6ms	5.3ms	
0	1	1	1024/fs	128ms	64ms	23.2ms	10.7ms	
1	0	0	2048/fs	256ms	128ms	46.4ms	21.3ms	
1	0	1	4096/fs	512ms	256ms	92.9ms	42.7ms	
1	1	0	8192/fs	1024ms	512ms	185.8ms	85.3ms	
1	1	1	16384/fs	2048ms	1024ms	371.5ms	170.7ms	

Table 30. ALC Recovery Operation Waiting Period

RGAIN1 bit	RGAIN0 bit	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 31. ALC Recovery GAIN Step

IREF7-0bits	GAIN (0dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E1H	+30.0		
:	:		
92H	+0.375		
91H	0.0		
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 32. Reference Level at ALC Recovery Operation for Recoding

OREF5-0bits	GAIN (0dB)	Step	
3CH	+36.0	1.5dB	(default)
3BH	+34.5		
3AH	+33.0		
:	:		
28H	+6.0		
:	:		
25H	+1.5		
24H	0.0		
23H	-1.5		
:	:		
2H	-51.0		
1H	-52.5		
0H	-54.0		

Table 33. Reference Level at ALC Recovery Operation for Playback

RFST1 bit	RFST0 bit	Recovery Speed	
0	0	Quad Speed	(default)
0	1	8times	
1	0	16times	
1	1	N/A	

Table 34. First Recovery Speed Setting (N/A: Not available)

3. The Volume at ALC Operation

The volume value during ALC operation is reflected in VOL7-0 bits. It is enable to check the current volume value by reading the register value of VOL7-0 bits.

VOL7-0bits	GAIN (0dB)
F1H	+36.0
F0H	+35.625
EFH	+35.25
:	:
C5H	+19.5
:	:
92H	+0.375
91H	0.0
90H	-0.375
:	:
2H	-53.625
1H	-54.0
0H	MUTE

Table 35. Value of VOL7-0 bits

4. Example of ALC Setting

Table 36 and Table 37 show the examples of the ALC setting for recording and playback path.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits must be the same value or larger value than ZTM1-0 bits	001	32ms	100	46.4ms
IREF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC1	ALC enable	1	Enable	1	Enable

Table 36. Example of the ALC Setting (Recording)

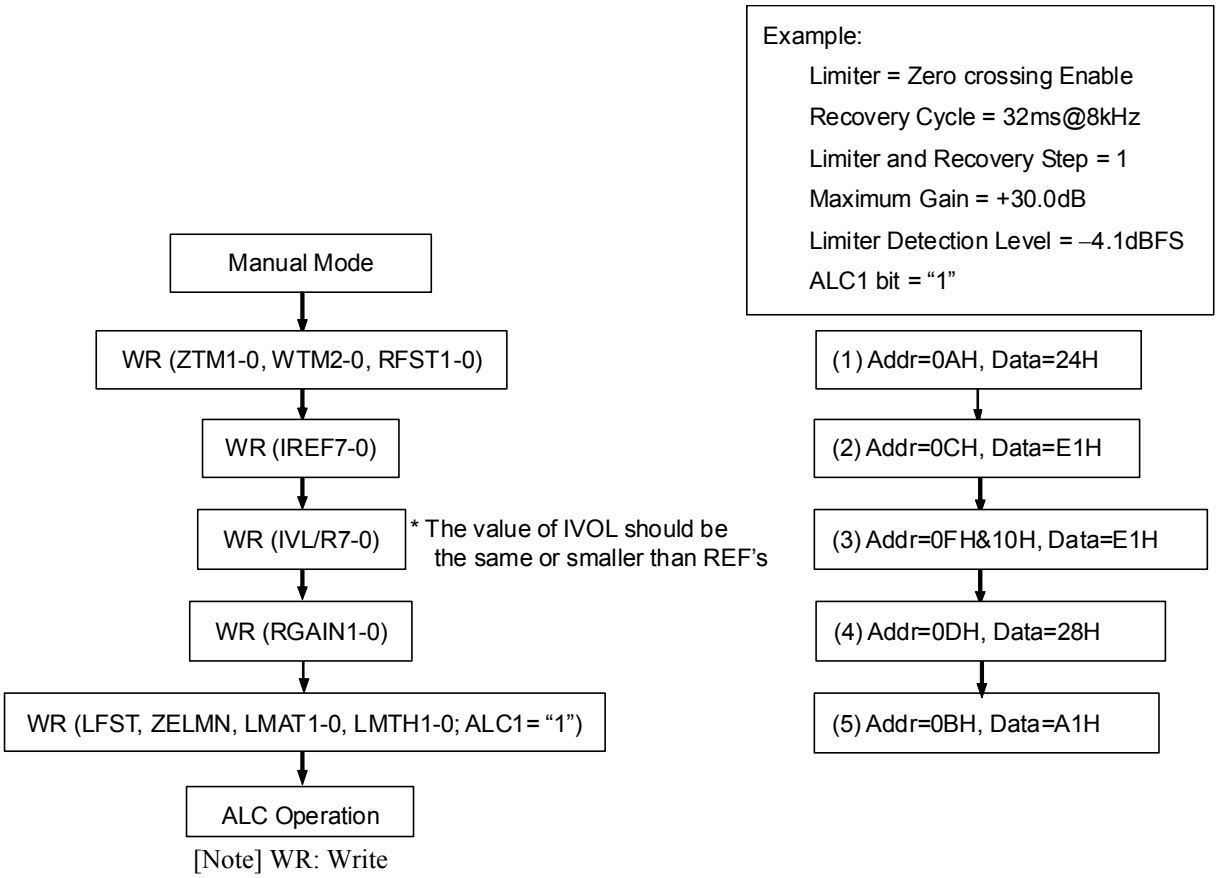
Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	23.2ms
WTM2-0	Recovery waiting period *WTM2-0 bits must be the same value or larger value than ZTM1-0 bits	001	32ms	100	46.4ms
OREF5-0	Maximum gain at recovery operation	28H	+6dB	28H	+6dB
OVL7-0, OVR7-0	Gain of VOL	91H	0dB	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
LFST	Fast Limiter Operation	1	ON	1	ON
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
RFST1-0	Fast Recovery Speed	00	4 times	00	4 times
ALC2	ALC enable	1	Enable	1	Enable

Table 37. Example of the ALC Setting (Playback)

5. Example of registers set-up sequence of ALC Operation

The following registers must not be changed during ALC operation. These bits must be changed after ALC operation is finished by ALC1 bit=ALC2 bit = "0". All ALC outputs are "0" until manual mode starts when ALC1 bit =ALC2 bit = "0".

LMTH1-0, LMAT1-0, ZTM1-0, WTM2-0, RGAIN 1-0, IREF7-0, ZELMN, RFST1-0, LFST bits



[Note] WR: Write

Figure 35. Registers Set-up Sequence at ALC1 Operation (recording path)

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode at ALC1 bit = "0" when ADCPF bit ="1". This mode is used in the case shown below.

1. After exiting reset state, when setting up the registers for ALC operation (ZTM1-0, LMTH and etc.)
2. When the registers for ALC operation (Limiter period, Recovery period and etc.) are changed. For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume control.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 38). The IVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits. Lch and Rch volumes are set individually by IVL7-0 and IVR7-0 bits when IVOLC bit = "0". IVL7-0 bits control both Lch and Rch volumes together when IVOLC bit = "1". When changing the volume, zero cross detection is executed on both Lch and Rch independently.

IVL7-0 bits IVR7-0 bits	GAIN (dB)	Step	
F1H	+36.0	0.375dB	(default)
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 38. Input Digital Volume Setting

If IVL7-0 or IVR7-0 bits are written during PMPFIL bit = "0", IVOL operation starts with the written values after PMPFIL bit is changed to "1".

When writing to IVOL7-0 bits continually, take an interval of zero crossing timeout period or more. If not, the zero crossing counters are reset at each time and the volume will not be changed. However, when writing the same register values as the previous time, the zero crossing counters will not be reset, so that it could be written in an interval less than zero crossing timeout.

■ De-emphasis Filter

The AK4953A includes a digital de-emphasis filter (tc = 50/15μs) which corresponds three kinds frequency (32kHz, 44.1kHz, 48kHz) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 39).

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 39. De-emphasis Control

■ Output Digital Volume (Manual Mode)

The ALC block becomes output digital volume (manual mode) by setting ALC2 bit to "0" when PMPFIL = PMDAC bits = "1" and ADCPF bit is "0". The output digital volume gain is set by the OVL7-0 bit and the OVR7-0 bit (Table 40). When the OVOLC bit = "1", the OVL7-0 bits control both L and R channel volume levels. When the OVOLC bit = "0", the OVL7-0 bits control L channel volume level and the OVR7-0 bits control R channel volume level. When changing the volumes, zero cross detection is executed on both L and R channels independently. The OVOL value is changed at zero crossing or timeout. The zero crossing timeout period is set by ZTM1-0 bits.

OVL7-0 bits OVR7-0 bits	GAIN (0dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		(default)
90H	-0.375		
:	:		
2H	-53.625		
1H	-54.0		
0H	MUTE		

Table 40. Output Digital Volume Setting

When writing to the OVL7-0 bits and OVR7-0 bit continuously, the control register should be written in an interval more than zero crossing timeout. If not, the zero crossing counters are reset at each time and the volume will not be changed. However, when writing the same register values as the previous time, the zero crossing counter will not be reset, so that it could be written in an interval less than zero crossing timeout.

■ Output Digital Volume 2

The AK4953A has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the DVL7-0 and DVR7-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +12 to –115dB or MUTE. When the DVOLC bit = "1", the DVL7-0 bits control both Lch and Rch attenuation levels. When the DVOLC bit = "0", the DVL7-0 bits control Lch level and DVR7-0 bits control Rch level. This volume has soft transition function. Therefore no switching noise occurs during the transition. The DVTM1-0 bits set the transition time between set values of DVL/R7-0 bits (from 00H to FFH) as either 256/fs, 1024/fs or 2048/fs (Table 42). When DVTM1-0 bits = "01", a soft transition between the set values occurs (1024 levels). It takes 1024/fs (=23ms@fs=44.1kHz) from 00H (+12dB) to FFH (MUTE).

DVL7-0 bits DVR7-0 bits	Gain	Step	
00H	+12.0dB	0.5dB	
01H	+11.5dB		
02H	+11.0dB		
:	:		
18H	0dB		(default)
:			
FDH	-114.5dB		
FEH	-115.0dB		
FFH	Mute (- ∞)		

Table 41. Output Digital Volume2 Setting

DVTM1 bit	DVTM0 bit	Transition Time between DVL/R7-0 bits = 00H and FFH				
		Setting	fs=8kHz	fs=44.1kHz	fs=96kHz	
0	0	256/fs	32ms	5.8ms	2.7ms	
0	1	1024/fs	128ms	23ms	11ms	(default)
1	0	2048/fs	256ms	46ms	21ms	
1	1	N/A				

Table 42. Transition Time Setting of Output Digital Volume2 (N/A: Not available)

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is set "1", the output signal is attenuated by -∞ ("0") during the cycle set by DVTM1-0 bits. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the value set by DVL/R7-0 bits from -∞ during the cycle set by DVTM1-0 bits. If the soft mute is cancelled within the cycle set by DVTM1-0 bits after starting the operation, the attenuation is discontinued and returned to the level set by DVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transaction (Figure 36)

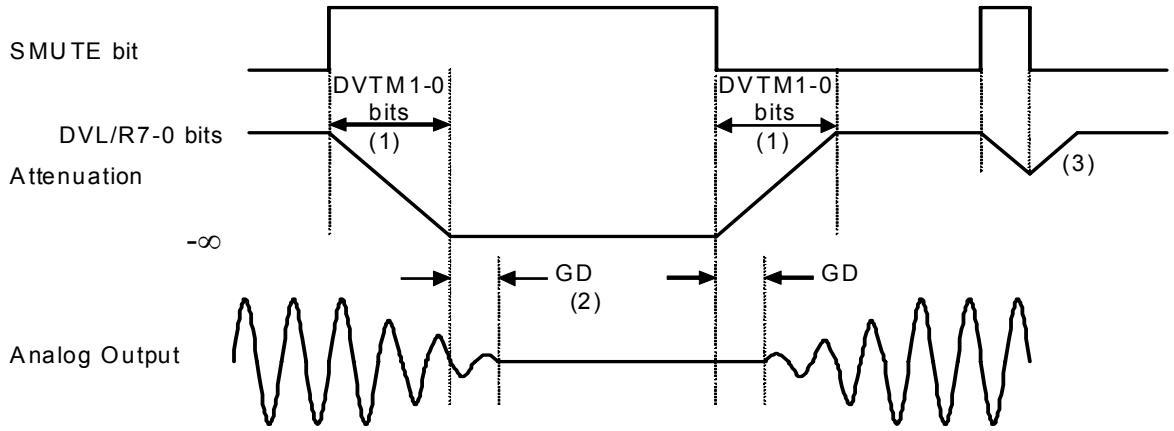


Figure 36. Soft Mute Function

(1) The input signal is attenuated by –∞ ("0") during the cycle set by DVTM1-0 bits.
(2) Analog output corresponding to digital input has group delay (GD).
(3) If soft mute is cancelled within the cycle set by DVTM1-0 bits after starting the operation, the attenuation is discounted and returned to the value set by DVL/R7-0 bits within the same cycle.

■ BEEP Signal Generating Circuit

The AK4953A integrates a BEPP signal generating circuit. When PMSPK bit = "1", the speaker amplifier outputs BEEP signal by setting PMBP bit = "1", and the Headphone amplifier outputs BEEP signal by setting PMBP bit = "1" when PMHPL bit or PMHPR bit = "1".

When PMDAC bit = "1" and PMHPL bit or PMHPR bit = "1", switching noise of connection between the BEEP generating circuit and headphone amplifier can be suppressed by soft transition. The transition time of ON/OFF switching is set by PTS1-0 bits. Soft transition Enable/Disable is controlled by MOFF bit. When this bit is "1", soft transition is disabled and the headphone is switched ON/OFF immediately.

PTS1 bit	PTS0 bit	ON/OFF Time						
		7.35kHz ≤ fs ≤ 24kHz		24kHz < fs ≤ 48kHz		48kHz < fs ≤ 96kHz		
0	0	64/fs	5.3 ~ 8.7ms	128/fs	2.7 ~ 5.3ms	256/fs	2.7 ~ 5.3ms	
0	1	128/fs	10.7 ~ 17.4ms	256/fs	5.3 ~ 10.7ms	512/fs	5.3 ~ 10.7ms	(default)
1	0	256/fs	21.3 ~ 34.8ms	512/fs	10.7 ~ 21.3ms	1024/fs	10.7 ~ 21.3ms	
1	1	512/fs	42.7 ~ 69.7ms	1024/fs	21.3 ~ 42.7ms	2048/fs	21.3 ~ 42.7ms	

Table 43. BEEP (Headphone-Amp) ON/OFF Transition Time

After outputting the signal during the time set by BPON7-0 bits, the AK4953A stops the output signal during the time set by BPOFF7-0 bits (Figure 37). The repeat count is set by BPTM6-0 bit, and the output level is set by BPLVL4-0 bits. When BPCNT bit is "0", if BPOUT bit is written "1", the AK4953A outputs the beep for the times of repeat count. When the output is finished, BPOUT bit is set to "0" automatically. When BPCNT bit is set to "1", it outputs beep signals incessantly regardless of repeat count, on-time nor off-time. The output frequency is set by BPFR1-0 bits.

< Setting parameter >

1) Output Frequency (Table 44, Table 45)
2) ON Time (Table 46, Table 47)
3) OFF Time (Table 48, Table 49)
4) Repeat Count (Table 50)
5) Output Level (Table 51)

*** BPFR1-0, BPON7-0, BPOFF7-0, BPTM6-0 and BPLVL4-0 bits should be set when BPOUT =BPCNT = "0".**

*** BPCNT bit is given priority in BPOUT bit. When BPOUT bit is set to "1", if BPCNT bit is set to "0", BPOUT bit is set to "0" forcibly.**

*** When stopping the BEEP outputs by changing BPCNT bit to "0" from "1", writing to BPOUT and BPCNT bits are inhibited for 10ms. When BEEP is output by setting BPCNT bit = "1", writing to BPOUT and BPCNT bits are inhibited for 10ms after BPOUT bit is changed to "0" or BEEP signal outputs are finished (ON/OFF time and the number of times set by repeated time).**

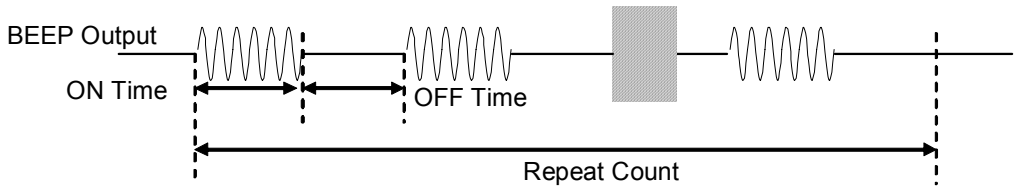


Figure 37. BEEP Signal Output

BPFR1-0 bits	Output frequency of BEEP Generator [Hz]		
	fs = 48kHz system (Note 47)	fs = 44.1kHz system (Note 48)	
00	4000	4009	(default)
01	2000	2005	
10	1297	1297	
11	800	802	

Note 47. Sampling frequency is 8kHz, 16kHz, 32kHz, 48kHz, 64kHz or 96kHz.
Note 48. Sampling frequency is 11.025kHz, 22.05kHz, 44.1kHz or 88.2kHz.

Table 44. Beep Signal Frequency (PLL Master/Slave Mode; MCKI referenced)

BPFR1-0 bits	Output frequency of BEEP Generator [Hz]				
	FS1-0 bits = "00"	FS1-0 bits = "01"	FS1-0 bits = "10"	FS1-0 bits = "11"	
00	fs/2.75	fs/5.5	fs/11	fs/22	(default)
01	fs/5.5	fs/11	fs/22	fs/44	
10	fs/8.5	fs/17	fs/34	fs/68	
11	fs/13.75	fs/27.5	fs/55	fs/110	

Table 45. Beep Signal Frequency (BICK referenced PLL Slave Mode, EXT Master/Slave Mode)

BPON7-0 bits	ON Time of BEEP Generator [msec]		Step[msec]		
	fs=48kHz system (Note 47)	fs=44.1kHz system (Note 48)	fs=48kHz system (Note 47)	fs=44.1kHz system (Note 48)	
0H	8.0	7.98	8.0	7.98	(default)
1H	16.0	15.96			
2H	24.0	23.95			
3H	32.0	31.93			
:	:	:			
FDH	2032	2027.3			
FEH	2040	2035.3			
FFH	2048	2043.4			

Note 47. Sampling frequency is 8kHz, 16kHz, 32kHz, 48kHz, 64kHz or 96kHz
Note 48. Sampling frequency is 11.025kHz, 22.05kHz, 44.1kHz or 88.2kHz

Table 46. Beep Output ON-time (PLL Master/Slave Mode; MCKI referenced)

BPON7-0 bits	ON Time of BEEP Generator [msec]		Step[msec]		
	fs=48kHz system (Note 47)	fs=44.1kHz system (Note 48)	fs=48kHz system (Note 47)	fs=44.1kHz system (Note 48)	
0H	7.33	7.98	7.33	7.98	(default)
1H	14.67	15.96			
2H	22.00	23.95			
3H	29.33	31.93			
:	:	:			
FDH	1862.6	2027.3			
FEH	1970.0	2035.3			
FFH	1877.3	2043.4			

Note 47. Sampling frequency is 8kHz, 16kHz, 32kHz, 48kHz, 64kHz or 96kHz
Note 48. Sampling frequency is 11.025kHz, 22.05kHz, 44.1kHz or 88.2kHz

Table 47. Beep Output ON-time (BICK referenced PLL Slave Mode, EXT Master/Slave Mode)

BPOFF7-0 bits	OFF Time of BEEP Generator [msec]		Step[msec]		
	fs=48kHz system (Note 47)	fs=44.1kHz system (Note 48)	fs=48kHz system (Note 47)	fs =44.1kHz system (Note 48)	
0H	8.0	7.98	8.0	7.98	(default)
1H	16.0	15.96			
2H	24.0	23.95			
3H	32.0	31.93			
:	:	:			
FDH	2032	2027.3			
FEH	2040	2035.3			
FFH	2048	2043.4			

Note 47. Sampling frequency is 8kHz, 16kHz, 32kHz, 48kHz, 64kHz or 96kHz
Note 48. Sampling frequency is 11.025kHz, 22.05kHz, 44.1kHz or 88.2kHz

Table 48. Beep Output OFF-time (PLL Master/Slave Mode; MCKI referenced)

BPOFF7-0 bits	OFF Time of BEEP Generator [msec]		Step[msec]		
	fs=48kHz system (Note 47)	fs=44.1kHz system (Note 48)	fs=48kHz system (Note 47)	fs=44.1kHz system (Note 48)	
0H	7.33	7.98	7.33	7.98	(default)
1H	14.67	15.96			
2H	22.00	23.95			
3H	29.33	31.93			
:	:	:			
FDH	1862.6	2027.3			
FEH	1970.0	2035.3			
FFH	1877.3	2043.4			

Note 47. Sampling frequency is 8kHz, 16kHz, 32kHz, 48kHz, 64kHz or 96kHz
Note 48. Sampling frequency is 11.025kHz, 22.05kHz, 44.1kHz or 88.2kHz

Table 49. Beep Output OFF-time (BICK referenced PLL Slave Mode, EXT Master/Slave Mode)

BPTM6-0 bits	Repeat Count	
0H	1	(default)
1H	2	
2H	3	
:	:	
7DH	126	
7EH	127	
7FH	128	

Table 50. Beep Output Repeat Count

BPLVL4-0 bits	Beep Output Level	STEP	
0H	0dB	3dB	(default)
1H	–3dB		
2H	–6dB		
:	:		
12H	–54dB		
13H	–57dB		
14H	–60dB		

Note 49. Beep output amplitude in 0dB setting is 1.5Vpp from the headphone amplifier, and 2.8Vpp @8Ω (SPKG1-0 bits = “00”) from the speaker amplifier.

Table 51. Beep Output Level

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage (PVEE) from AVDD voltage. The PVEE voltage is used for the headphone amplifier and the speaker amplifier in low voltage mode (LSV bit = "1"). The charge pump circuit starts operation when PMHPL or PMHPR bit = "1", or when LSV bit = PMSPK bit = "1". PMVCM bit must be set "1" to power up the charge pump circuit.

The power up time of the charge pump circuit is 11ms (max). The headphone amplifier and speaker amplifier will be powered up after the charge pump circuit is powered up (when PMHPL or PMHPR bit = "1", or LSV bit = PMSPK bit = "1").

The operating frequency of the charge pump circuit is dependent on the sampling frequency. The operation mode of the headphone amplifier can be changed by the CPCK bit. (Table 52)

CPCK bit	Mode	Power Consumption (DAC → Headphone out)	S/(N+D) (0dBFS)
0	Low power mode	10.2mW	72dB
1	High performance mode	12.1mW	80dB

Table 52. Operation Mode of the Charge Pump (PMHPL or PMHPR bit = "1")

■ Headphone Amplifier (HPL/HPR pins)

The positive voltage of the headphone amplifier uses the power supply to the DVDD pin, therefore 150mA of the maximum power supply capacity is needed. The internal charge pump circuit generates negative voltage (PVEE) from AVDD voltage. The headphone amplifier output is single-ended and centered around on VSS (0V). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω. When HPM bit = "1", the DAC output signal is output to HPL and HPR pins as (L+R)/2 mono signal.

<External Circuit of Headphone-Amp>

An oscillation prevention circuit (0.22μF±20% capacitor and 100Ω±20% resistor) should be put because it has the possibility that Headphone-Amp oscillates in type of headphone.

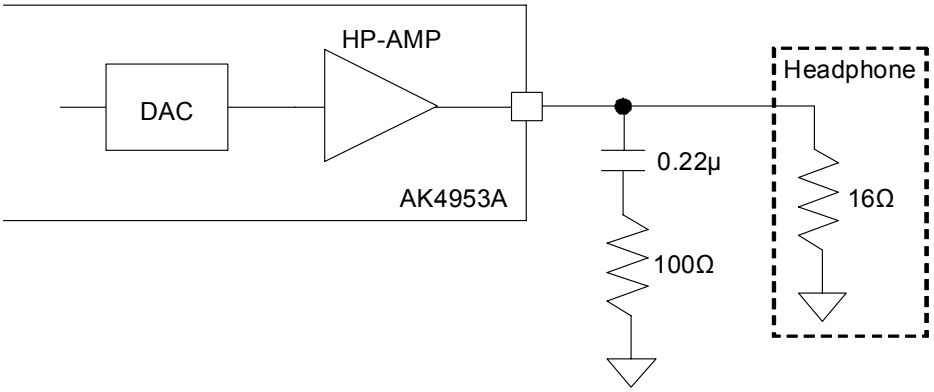


Figure 38. External Circuit of Headphone

When HPZ bit = "0" and PMHPL, PMHPR bits = "1", headphone outputs are in normal operation.

When PMHPL and PMHPR bits = "0", the headphone-amps are powered-down completely. At that time, the HPL and HPR pins go to VSS voltage via the internal pulled-down resistor. The pulled-down resistor is 10Ω (typ). The HPL and HPR pins become Hi-Z state by setting HPZ bit to "1" when PMHPL and PMHPR bit = "0".

The power-up time of the headphone-amps is 35ms (max.), and power-down is executed immediately.

PMVCM bit	PMHPL/R bits	HPZ bit	Mode	HPL/R pins	
x	0	0	Power-down & Mute	Pull-down by 10Ω (typ)	(default)
x	0	1	Power-down	Hi-Z	
1	1	0	Normal Operation	Normal Operation	
1	1	1	N/A	N/A	

Table 53. Headphone Output Status (x: Don't' care, N/A: Not available)

■ Speaker Output

The DAC output signal is input to the speaker amplifier as [(L+R)/2]. The speaker amplifier is mono and BTL output. The gain is set by SPKG1-0 bits. Output level depends on SVDD voltage and SPKG1-0 bits. The AK4953A has a low voltage mode (LSV bit = "1") which the speaker amplifier can be operated by SVDD= 0.9V ~ 2.0V. In low voltage mode, the negative power which is generated by the charge pump circuit using the voltage from the AVDD pin is used. This negative power is not used in normal voltage mode (LSV bit = "0", SVDD=1.8V~5.5V). In low voltage mode, SPKG1-0 bits must be set to "00" and the DAC output level should be set to lower level by setting digital volume so that the speaker amplifier outputs is suppressed to lower level and output signal is not clipped.

SPKG1-0 bits	Gain		
	ALC2 bit = "0"	ALC2 bit = "1"	
00	5.3 dB	7.3 dB	(default)
01	7.3 dB	9.3 dB	
10	9.3 dB	11.3 dB	
11	11.3 dB	13.3 dB	

Table 54. SPK-Amp Gain

SPKG1-0 bits	SPK-Amp Output (DAC Input=0dBFS, SVDD=3.3V)	
	ALC2 bit = "0"	ALC2 bit = "1" (LMTH1-0 bits = "00")
00	3.37Vpp	3.17Vpp
01	4.23Vpp (Note 50)	4.00Vpp
10	5.33Vpp (Note 50)	5.04Vpp (Note 50)
11	6.71Vpp (Note 50)	6.33Vpp (Note 50)

Note 50. The output level is calculated by assuming that output signal is not clipped. In the actual case, the output signal may be clipped when DAC outputs 0dBFS signal. The DAC output level should be set to lower level by setting digital volume so that the speaker amplifier output level is 4.0Vpp or less and output signal is not clipped.

Table 55. SPK-Amp Output Level

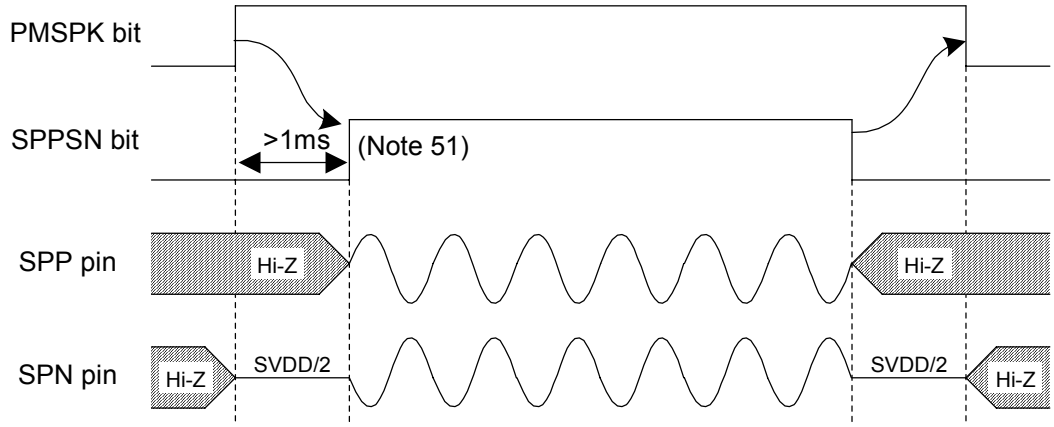
< Speaker-Amp Control Sequence >

The speaker amplifier is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pins are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the speaker amplifier enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs SVDD/2 voltage.

When the PMSPK bit is "1" after the PDN pin is changed from "L" to "H", the SPP and SPN pins rise up from power-save-mode. In this mode, the SPP pin is placed in a Hi-Z state and the SPN pin goes to SVDD/2 voltage. Because the SPP and SPN pins rise up at power-save-mode, this mode can reduce a pop noise. When the AK4953A is powered-down, pop noise can also be reduced by first entering power-save-mode.

PMSPK	SPPSN	Mode	SPP	SPN	
0	x	Power-down	Hi-Z	Hi-Z	(default)
1	0	Power-save	Hi-Z	SVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 56 Speaker-Amp Mode Setting (x: Don't care)



Note 51. This time needs 15ms or more in low voltage mode (LSV bit= "1").
Figure 39. Power-up/Power-down Timing for Speaker-Amp

■ Thermal Shutdown Function

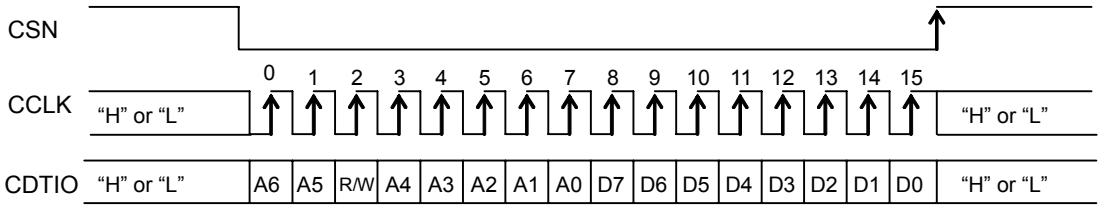
When the internal device temperature rises up irregularly (E.g. Output pins of speaker amplifier are shortened.), the charge pump, headphone amplifier and speaker amplifier are automatically powered down and then THDET bit becomes "1".
When the internal temperature goes down and the thermal shutdown is released, the charge pump, speaker and headphone amplifiers are powered up automatically and THDET bit returns to "0".

■ Serial Control Interface

(1) 3-wire Serial Control Mode

Internal registers may be written by using the 3-wire μP interface pins (CSN, CCLK and CDTIO). The data on this interface consists of Read/Write, Register address (MSB first, 7bits) and Control or Output data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Data writings become available on the rising edge of CSN. When reading the data, the CDTIO pin changes to output mode at the falling edge of 8th CCLK and outputs D7-D0. However this reading function is available only when READ bit = "1". When READ bit = "0", the CDTIO pin stays as Hi-Z even after the falling edge of 8th CCLK. The output finishes on the rising edge of CSN. The CDTIO is placed in a Hi-Z state except when outputting data at read operation mode. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by the PDN pin = "L".

Note 52. Data reading is only available on the following addresses; 00H~19H, 1CH~25H, 30H and 32H~4FH. When reading the address 1AH, 1BH, 26H~2FH, 31H and 50H~7FH the register values are invalid.



R/W: READ/WRITE ("1": WRITE, "0": READ)
A6-A0: Register Address
D7-D0: Control data (Input) at Write Command
Output data (Output) at Read Command

Figure 40. Serial Control I/F Timing

(2) I2C-bus Control Mode (I2C pin = "H")

The AK4953A supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD+0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 41 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 47). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 42). If the slave address matches that of the AK4953A, the AK4953A generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 48). A R/W bit value of "1" indicates that the read operation is to be executed, and "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4953A. The format is MSB first, and those most significant 1bit is fixed to zero (Figure 43). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 44). The AK4953A generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 47).

The AK4953A can perform more than one byte write operation per sequence. After receipt of the third byte the AK4953A generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 4FH prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 49) except for the START and STOP conditions.

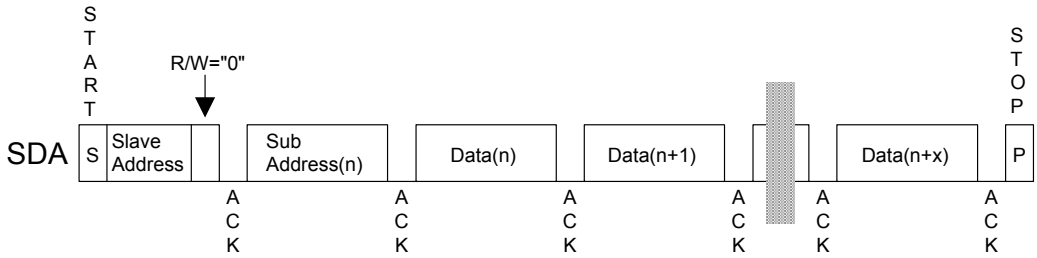


Figure 41. Data Transfer Sequence at I²C Bus Mode

0	0	1	0	0	1	CAD0	R/W

Figure 42. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 43. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 44. The Third Byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4953A. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 4FH prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

Note 52. Data reading is only available on the following addresses; 00H~19H, 1CH~25H, 30H and 32H~4FH. When reading the address 1AH, 1BH, 26H~2FH, 31H and 50H~7FH the register values are invalid.

The AK4953A supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4953A has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4953A generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4953A ceases the transmission.

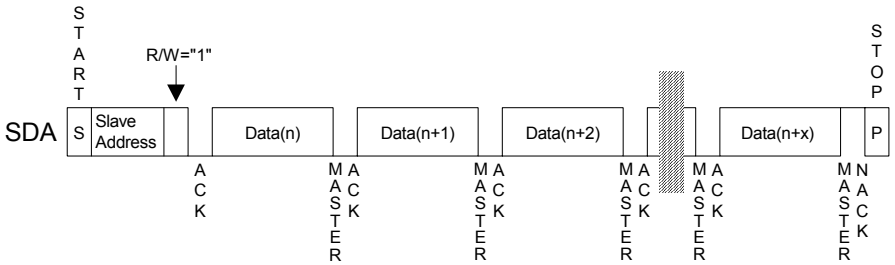


Figure 45. Current Address Read

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4953A then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4953A ceases the transmission.

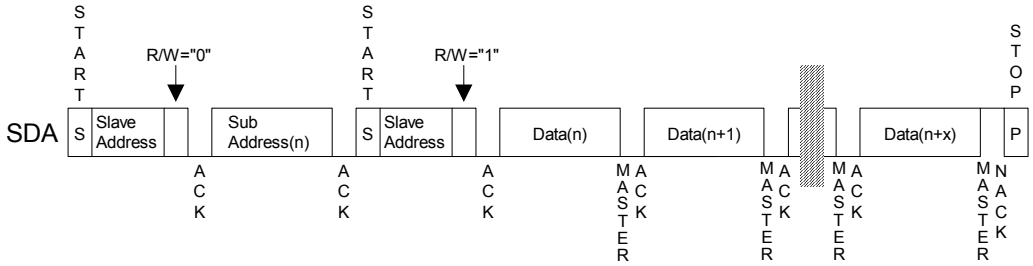


Figure 46. Random Address Read

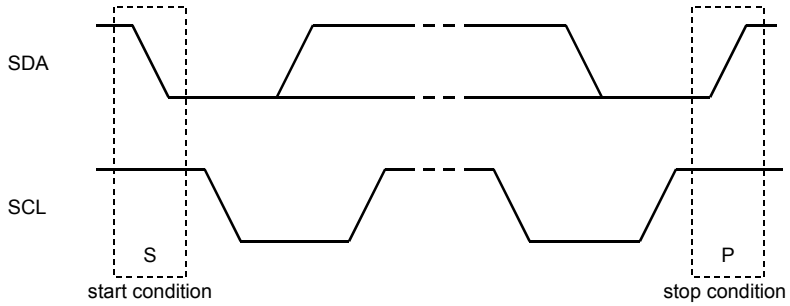


Figure 47. Start Condition and Stop Condition

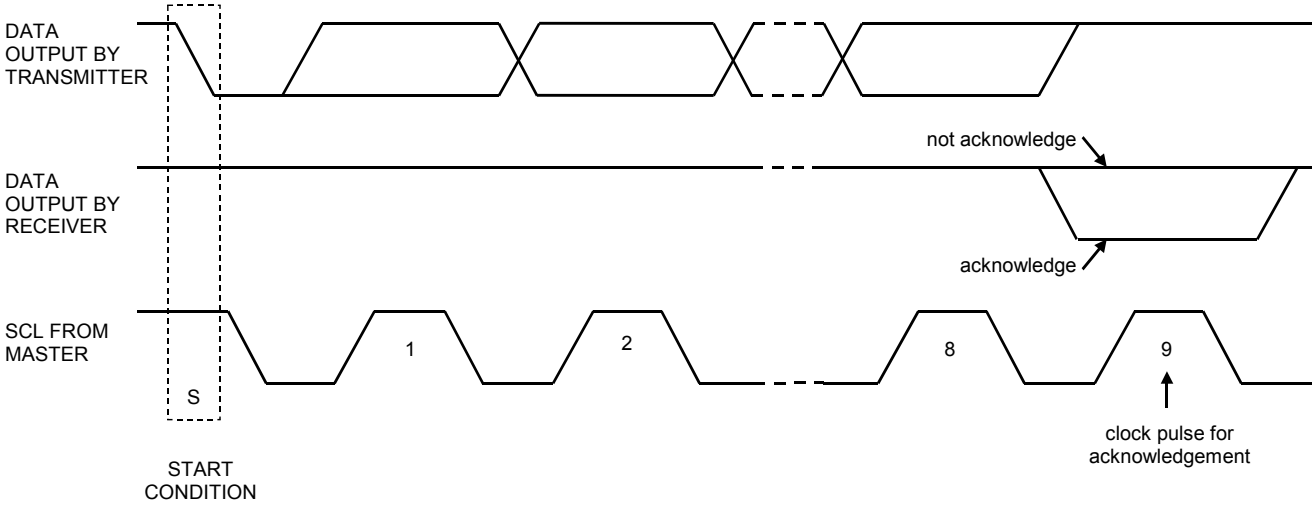


Figure 48. Acknowledge (I^2C Bus)

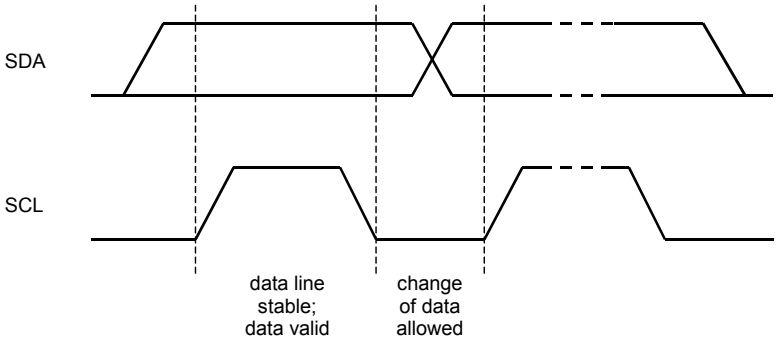


Figure 49. Bit Transfer (I^2C Bus)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	LSV	PMDAC	PMADR	PMADL
01H	Power Management 2	0	0	PMHPL	PMHPR	M/S	0	MCKO	PMPLL
02H	Signal Select 1	SPPSN	0	DACS	MPSEL	PMMP	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	0	0	INR1	INL1	INR0	INL0
04H	Signal Select 3	0	0	PTS1	PTS0	MOFF	HPM	0	0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	HPZ	DIF1	DIF0
06H	Mode Control 2	PS1	PS0	CPCK	DS	FS3	FS2	FS1	FS0
07H	Mode Control 3	READ	THDET	SMUTE	DVOLC	OVOLC	IVOLC	DEM1	DEM0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
09H	Timer Select	ADRST1	ADRST 0	0	0	0	0	DVTM1	DVTM0
0AH	ALC Timer Select	0	ZTM1	ZTM0	WTM2	WTM1	WTM0	RFST1	RFST0
0BH	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	LMTH1	LMTH0
0CH	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
0DH	ALC Mode Control 3	RGAIN1	RGAIN0	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0FH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
11H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
12H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
13H	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
14H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
15H	BEEP Frequency	BPCNT	0	0	0	0	0	BPFR1	BPFR0
16H	BEEP ON Time	BPON7	BPON6	BPON5	BPON4	BPON3	BPON2	BPON1	BPON0
17H	BEEP OFF Time	BPOFF7	BPOFF6	BPOFF5	BPOFF4	BPOFF3	BPOFF2	BPOFF1	BPOFF0
18H	BEEP Repeat Count	0	BPTM6	BPTM5	BPTM4	BPTM3	BPTM2	BPTM1	BPTM0
19H	BEEP Volume Control	BPOUT	0	0	BPLVL4	BPLVL3	BPLVL2	BPLVL1	BPLVL0
1AH	Reserved	0	0	0	0	0	0	0	0
1BH	Reserved	0	0	0	0	0	0	0	0
1CH	Digital Filter Select 1	0	0	LPF	HPF	0	HPFC1	HPFC0	HPFAD
1DH	Digital Filter Mode	0	0	0	0	0	PFDAC	ADCPF	PFSDO
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
26H	Reserved	0	0	0	0	0	0	0	0
27H	Reserved	0	0	0	0	0	0	0	0
28H	Reserved	0	0	0	0	0	0	0	0
29H	Reserved	0	0	0	0	0	0	0	0
2AH	Reserved	0	0	0	0	0	0	0	0
2BH	Reserved	0	0	0	0	0	0	0	0
2CH	Reserved	0	0	0	0	0	0	0	0
2DH	Reserved	0	0	0	0	0	0	0	0
2EH	Reserved	0	0	0	0	0	0	0	0
2FH	Reserved	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
31H	Reserved	0	0	0	0	0	0	0	0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

Note 53. PDN pin = “L” resets the registers to their default values.
Note 54. The bits defined as 0 must contain a “0” value.
Note 55. Reading address 1AH, 1BH, 26H~2FH, 31H and 50H~7FH are not possible.
Note 56. Address 0EH is a read only register. Writing access to 0EH is ignored and does not effect the operation.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	PMSPK	LSV	PMDAC	PMADR	PMADL
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMADL: MIC-Amp Lch and ADC Lch Power Management
0: Power-down (default)
1: Power-up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=24ms @44.1kHz, ADRST1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMADR: MIC-Amp Rch, ADC Rch Power Management
0: Power down (default)
1: Power up
When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (1059/fs=24ms @44.1kHz, ADRST1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

LSV: Low Voltage Operation Mode of the Speaker Amplifier
0: Normal mode: SVDD=1.8V ~ 5.5V (default)
1: Low voltage mode: SVDD=0.9V ~ 2.0V

PMSPK: Speaker-Amp Power Management
0: Power-down (default)
1: Power-up

PMBP: BEEP Generating Circuit Power Management
0: Power-down (default)
1: Power-up

PMVCM: VCOM, Regulator (2.5V) Power Management
0: Power-down (default)
1: Power-up

PMPFIL: Programmable Filter Block (HPF2/LPF/5 Band EQ/ALC) Power Management
0: Power down (default)
1: Power up

All blocks can be powered-down by writing "0" to the address "00H", PMPLL, PMMP, PMHPL, PMHPR, PMDML, PMDMR and MCKO bits. In this case, register values are maintained.

PMVCM bit must be "1" when one of bocks is powered-up. PMVCM bit can only be "0" when the address "00H" and all power management bits (PMPLL, PMMP, PMHPL, PMHPR, PMDML, PMDMR and MCKO) are "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	PMHPL	PMHPR	M/S	0	MCKO	PMPLL
R/W		R	R	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power down (default)
1: PLL Mode and Power up

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

PMHPR: Rch Headphone Amplifier and Charge Pump Power Management
0: Power down (default)
1: Power up

PMHPL: Lch Headphone Amplifier and Charge Pump Power Management
0: Power down (default)
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Signal Select 1	SPPSN	0	DACS	MPSEL	PMMP	MGAIN2	MGAIN1	MGAIN0
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

MGAIN3-0: MIC-Amp Gain Control (Table 22)

PMMP: MPWR pin Power Management
0: Power-down: Hi-Z (default)
1: Power-up

MPSEL: MPWR Output Select
0: MPWR1 pin (default)
1: MPWR2 pin

DACS: Signal Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is in power-save mode. In this mode, the SPP pin goes to Hi-Z and outputs SVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "L", Speaker-Amp is in power-down mode since PMSPK bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SPKG1	SPKG0	0	0	INR1	INL1	INR0	INL0
R/W		R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

INL1-0: ADC Lch Input Source Select (Table 21)
Default: 00 (LIN1 pin)

INR1-0: ADC Rch Input Source Select (Table 21)
Default: 00 (RIN1 pin)

SPKG1-0: Speaker-Amp Output Gain Select (Table 54)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Signal Select 3	0	0	PTS1	PTS0	MOFF	HPM	0	0
R/W		R	R	R/W	R/W	R/W	R/W	R	R
Default		0	0	0	1	0	0	0	0

HPM: Headphone Output Select
0: Stereo (default)
1: Mono
When HPM bit = "1", DAC output signals are output from the headphone amplifier as (L+R)/2.

MOFF: Soft Transition Control of "BEEP → Headphone" Connection ON/OFF
0: Enable (default)
1: Disable

PTS1-0: Soft Transition Time of "BEEP → Headphone" Connection ON/OFF
Default: "01" (Table 43)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	HPZ	DIF1	DIF0
R/W		R/W	R/W	R/W	R/W	R/W	W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 18)
Default: "10" (MSB justified)

HPZ: Pull-down Setting of HP-Amp
0: Pull-down by a 10Ω(typ) resistor. (Default)
1: Hi-Z
When using HPZ bit, set HPZ bit to "1" before starting a speaker amplifier operation, and then write registers according to the sequence in "■ Speaker-Amp Output". Set HPZ bit to "0" before starting a headphone amplifier operation, and then write registers according to the sequence in "■ Headphone-Amp Output".

BCKO: Master Mode BICK Output Frequency Setting (Table 11)

PLL3-0: PLL Reference Clock Select (Table 5)
Default: "0000"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Mode Control 2	PS1	PS0	CPCK	DS	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling frequency (Table 6, Table 7) and MCKI frequency (Table 12, Table 14) Setting
These bits control sampling frequency in PLL mode and control MCKI input frequency in EXT mode.

DS: Double Speed Mode
0: Normal Speed: fs ≤ 48kHz (default)
1: Double Speed: 48kHz < fs ≤ 96kHz

PS1-0: MCKO Frequency Setting (Table 10)
Default: “00” (256fs)

CPCK: Operation Mode of the Charge Pump (Table 52)
0: Low Power Mode (default)
1: High Performance Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Mode Control 3	READ	THDET	SMUTE	DVOLC	OVOLC	IVOLC	DEM1	DEM0
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	1	0	1

DEM1-0: De-emphasis Control (Table 39)
Default: "01" (OFF)

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume levels, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

OVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When OVOLC bit = "1", OVL7-0 bits control both Lch and Rch volume levels, while register values of OVL7-0 bits are not written to OVR7-0 bits. When OVOLC bit = "0", OVL7-0 bits control Lch level and OVR7-0 bits control Rch level, respectively.

DVOLC: Output Digital Volume2 Control Mode Select
0: Independent
1: Dependent (default)
When DVOLC bit = "1", DVL7-0 bits control both Lch and Rch volume levels, while register values of DVL7-0 bits are not written to DVR7-0 bits. When DVOLC bit = "0", DVL7-0 bits control Lch level and DVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

THDET: Thermal Shutdown Detection
0: Thermal Shutdown Off (default)
1: Thermal Shutdown On

READ: Read Function Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Digital MIC	0	0	PMDMR	PMDML	DCLKE	0	DCLKP	DMIC
R/W		R	R	R/W	R/W	R/W	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

DMIC: Digital Microphone Connection Select
0: Analog Microphone (default)
1: Digital Microphone

DCLKP: Data Latching Edge Select
0: Lch data is latched on the DMCLK rising edge (“↑”). (default)
1: Lch data is latched on the DMCLK falling edge (“↓”).

DCLKE: DMCLK pin Output Clock Control
0: “L” Output (default)
1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone (Table 21)
Default: “00”
ADC digital block is powered-down by PMDML = PMDMR bits = “0” when selecting a digital microphone input (DMIC bit = “1”, INL/R bits = “00”, “01” or “10”).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Timer Select	ADRST1	ADRST0	0	0	0	0	DVTM1	DVTM0
R/W		R/W	R/W	R	R	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	1

DVTM1-0: Digital Volume Soft Transition Time Setting (Table 41)
Default: “01” (1024/fs)
This is the transition time between DVL/R7-0 bits = 00H and FFH.

ADRST1-0: ADC Initialization Cycle Setting
00: 1059/fs (default)
01: 267/fs
10: 2115/fs
11: 2115/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ALC Timer Select	0	ZTM1	ZTM0	WTM2	WTM1	WTM0	RFST1	RFST0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

RFST1-0: ALC First recovery Speed (Table 34)
Default: “00” (4times)

WTM2-0: ALC Recovery Waiting Period (Table 30)
Default: “000” (128/fs)
A period of recovery operation when any limiter operation does not occur during ALC operation

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (Table 29)
Default: “00” (128/fs)
In case of the μP WRITE operation or ALC recovery operation, the volume is changed at zero crossing or timeout.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	LFST	ALC2	ALC1	ZELMN	LMAT1	LMAT0	LMTH1	LMTH0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 27)
Default: "00"

LMAT1-0: ALC Limiter ATT Step (Table 28)
Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (default)
1: Disable

ALC1: ALC Enable for Recording
0: Recording ALC Disable (default)
1: Recording ALC Enable

ALC2: ALC Enable for Playback
0: Playback ALC Disable (default)
1: Playback ALC Enable

LFST: ALC Limiter operation when the output level exceed FS(Full-scale) level.
0: The volume is changed at zero crossing or zero crossing time out. (default)
1: When output of ALC is larger than FS, OVOL value is changed immediately (1/fs).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	IREF7	IREF6	IREF5	IREF4	IREF3	IREF2	IREF1	IREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IREF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 32)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	ALC Mode Control 3	RGAIN1	RGAIN0	OREF5	OREF4	OREF3	OREF2	OREF1	OREF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	0	0

OREF5-0: Reference value at Playback ALC Recovery Operation. 0.375dB step, 50 Level (Table 33)
Default: "28H" (+6.0dB)

RGAIN1: ALC Recovery GAIN Step (Table 31)
Default: "00"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
R/W		R	R	R	R	R	R	R	R
Default		1	0	0	1	0	0	0	1

VOL7-0: Current ALC volume value; 0.375dB step, 242 Level. Read operation only (Table 35)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 38)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Lch Output Volume Control	OVL7	OVL6	OVL5	OVL4	OVL3	OVL2	OVL1	OVL0
12H	Rch Output Volume Control	OVR7	OVR6	OVR5	OVR4	OVR3	OVR2	OVR1	OVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	0	0	1

OVL7-0, OVR7-0: Output Digital Volume (Table 40)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
14H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

DVL7-0, DVR7-0: Output Digital Volume2 (Table 41)
Default: "18H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	BEEP Frequency	BPCNT	0	0	0	0	0	BPFR1	BPFR0
R/W		R/W	R	R	R	R	R	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPFR1-0: BEEP Signal Output Frequency Setting (Table 44, Table 45)
Default: "00H"

BPCNT: BEEP Signal Output Mode Setting
0: Once Output Mode. (default)
1: Continuous Mode
In once output mode, the BEEP signal is output by the repeat times set by BPTM6-0 bits.
In continuous mode, the BEEP signal is output while BPCNT bit is "1".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	BEEP ON Time	BPON7	BPON6	BPON5	BPON4	BPON3	BPON2	BPON1	BPON0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPON7-0: BEEP Output ON-time Setting (Table 46, Table 47)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	BEEP OFF Time	BPOFF7	BPOFF6	BPOFF5	BPOFF4	BPOFF3	BPOFF2	BPOFF1	BPOFF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPOFF7-0: BEEP Output OFF-time Setting (Table 48, Table 49)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	BEEP Repeat Count	0	BPTM6	BPTM5	BPTM4	BPTM3	BPTM2	BPTM1	BPTM0
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPTM6-0: BEEP Output Repeat Count Setting (Table 50)
Default: "00H"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
19H	BEEP Volume Control	BPOUT	0	0	BPLVL4	BPLVL3	BPLVL2	BPLVL1	BPLVL0
R/W		R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BPLVL4-0: BEEP Output level Setting (Table 51)
Default: "0H" (0dB)

BPOUT: BEEP Signal Control
0: OFF (default)
1: ON
When BPCNT bit = "0", the beep signal starts outputting by setting BPOUT bit = "1". The Beep signal stops after the number of times that is set by BPTM6-0 bit, and BPOUT bit is set to "0" automatically.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	Digital Filter Select 1	0	0	LPF	HPF	0	HPFC1	HPFC0	HPFAD
R/W		R	R	R/W	R/W	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

HPFAD: HPF1 Control of ADC
0: OFF
1: ON (default)
When HPFAD bit is "1", the settings of HPFC1-0 bits are enabled. When HPFAD bit is "0", HPFAD block is through (0dB).
When PMADL bit = "1" or PMADR bit = "1", set HPFAD bit to "1".

HPFC1-0: Cut-off Frequency Setting of HPF1 (ADC) (Table 26)
Default: "00" (3.4Hz @ fs = 44.1kHz)

HPF: HPF2 Coefficient Setting Enable
0: OFF (default)
1: ON
When HPF bit is "1", the settings of F1A13-0 and F1B13-0 bits are enabled. When HPF bit is "0", HPF block is through (0dB).

LPF: LPF Coefficient Setting Enable
0: OFF (default)
1: ON
When LPF bit is "1", the settings of F2A13-0 and F2B13-0 bits are enabled. When LPF bit is "0", LPF block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Digital Filter Mode	0	0	0	0	0	PFDAC	ADCPF	PFSDO
R/W		R	R	R	R	R	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

PFSDO: SDTO Output Signal Select
0: ADC (+ 1st HPF) Output
1: Programmable Filter / ALC Output (default)

ADCPF: Programmable Filter / ALC Input Signal Select
0: SDTI
1: ADC Output (default)

PFDAC: DAC Input Signal Select
0: SDTI (default)
1: Programmable Filter / ALC Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1FH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
20H	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
21H	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD							

F1A13-0, F1B13-0: HPF2 Coefficient (14bit x 2)
Default: F1A13-0 bits = 0x1FA9, F1B13-0 bits = 0x20AD
fc = 150Hz@fs=44.1kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22H	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
23H	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
24H	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
25H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F2A13-0, F2B13-0: LPF Coefficient (14bit x 2)
Default: “0000H”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30H	Digital Filter Select 2	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

EQ1: Equalizer 1 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ1 bit is "1", the settings of E1A15-0, E1B15-0 and E1C15-0 bits are enabled. When EQ1 bit is "0", EQ1 block is through (0dB).

EQ2: Equalizer 2 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ2 bit is "1", the settings of E2A15-0, E2B15-0 and E2C15-0 bits are enabled. When EQ2 bit is "0", EQ2 block is through (0dB).

EQ3: Equalizer 3 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ3 bit is "1", the settings of E3A15-0, E3B15-0 and E3C15-0 bits are enabled. When EQ3 bit is "0", EQ3 block is through (0dB).

EQ4: Equalizer 4 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ4 bit is "1", the settings of E4A15-0, E4B15-0 and E4C15-0 bits are enabled. When EQ4 bit is "0", EQ4 block is through (0dB).

EQ5: Equalizer 5 Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQ5 bit is "1", the settings of E5A15-0, E5B15-0 and E5C15-0 bits are enabled. When EQ5 bit is "0", EQ5 block is through (0dB).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
32H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
33H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
34H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
35H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
36H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
37H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
38H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
39H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
3AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
3BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
3CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
3DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
3EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
3FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
40H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
41H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
42H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
43H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
44H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
45H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
46H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
47H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
48H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
49H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
4AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
4BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
4CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
4DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
4EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
4FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

E1A15-0, E1B15-0, E1C15-0: Equalizer 1 Coefficient (16bit x3)
Default: “0000H”

E2A15-0, E2B15-0, E2C15-0: Equalizer 2 Coefficient (16bit x3)
Default: “0000H”

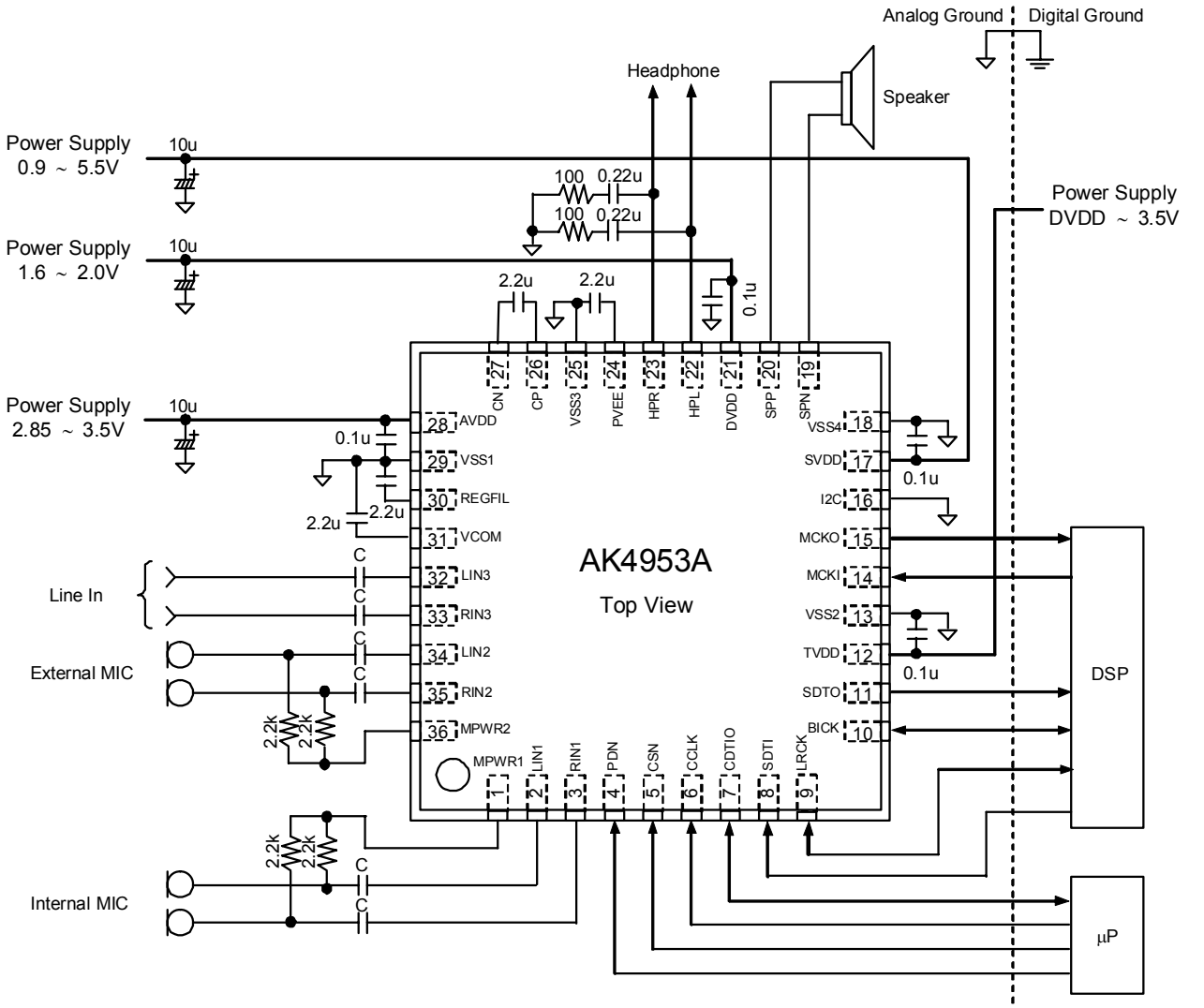
E3A15-0, E3B15-0, E3C15-0: Equalizer 3 Coefficient (16bit x3)
Default: “0000H”

E4A15-0, E4B15-0, E4C15-0: Equalizer 4 Coefficient (16bit x3)
Default: “0000H”

E5A15-0, E5B15-0, E5C15-0: Equalizer 5 Coefficient (16bit x3)
Default: “0000H”

SYSTEM DESIGN

Figure 50 shows the system connection diagram. An evaluation board (AKD4953A) is available for fast evaluation as well as suggestions for peripheral circuitry.



Notes:

- VSS1, VSS2, VSS3 and VSS4 of the AK4953A must be distributed separately from the ground of external controllers.
- All digital input pins must not be left floating.
- When the AK4953A is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, around 100kΩ pull-up resistor must be connected to LRCK and BICK pins of the AK4953A.
- 0.1µF capacitors at power supply pins should be ceramic capacitors. Other capacitors do not have specific types.

Figure 50. System Connection Diagram (3-wire Serial Mode)

1. Grounding and Power Supply Decoupling

The AK4953A requires careful attention to power supply and grounding arrangements. If AVDD, DVDD, TVDD and SVDD are supplied separately, the power-up sequence is not critical. VSS1, VSS2, VSS3 and VSS4 of the AK4953A must be connected to the analog ground plane. System analog ground and digital ground must be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as near to the AK4953A as possible, with the small value ceramic capacitor being the nearest.

2. Internal Regulated Voltage Power Supply

The input voltage to the REGFIL pin is used as power supply (typ. 2.5V) for the internal analog circuit. A 2.2μF±50% electrolytic capacitor connected between the REGFIL and VSS1 pins eliminates the effects of high frequency noise. This capacitor in particular should be connected as close as possible to the pin. No load current may be drawn from the REGFIL pin. All digital signals, especially clocks, should be kept away from the REGFIL pin in order to avoid unwanted coupling into the AK4953A.

3. Voltage Reference

VCOM is a signal ground of this chip (typ. 1.25V). A 2.2μF±50% electrolytic capacitor connected between this pin and the VSS1 pin eliminates the effects of high frequency noise. This capacitor in particular should be connected as close as possible to the pin. No load current may be drawn from the VCOM pin. All digital signals, especially clocks, must be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4953A.

4. Charge Pump

2.2μF±50% capacitors between the CP and CN pins, and the PVEE and VSS3 pins should be low ESR ceramic capacitors. These capacitors must be connected as close as possible to the pins. No load current may be drawn from the PVEE pin.

5. Analog Inputs

The MIC input is single-ended. The input signal range scales with nominally at typ. 2.4Vpp (@ MGAIN = 0dB), centered around the internal signal ground (typ. 1.25V). Usually the input signal is AC coupled using a capacitor (1μF or less is recommended). The cut-off frequency is $fc = 1/(2\pi RC)$. The AK4953A can accept input voltages from VSS1 to AVDD.

6. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit). The headphone output is single-ended and centered around VSS (0V). There is no need for AC coupling capacitors. The speaker outputs are centered on 0.5 x SVDD (typ).

CONTROL SEQUENCE

■ Clock Set up

When any circuits of the AK4953A are powered-up, the clocks must be supplied.

1. PLL Master Mode

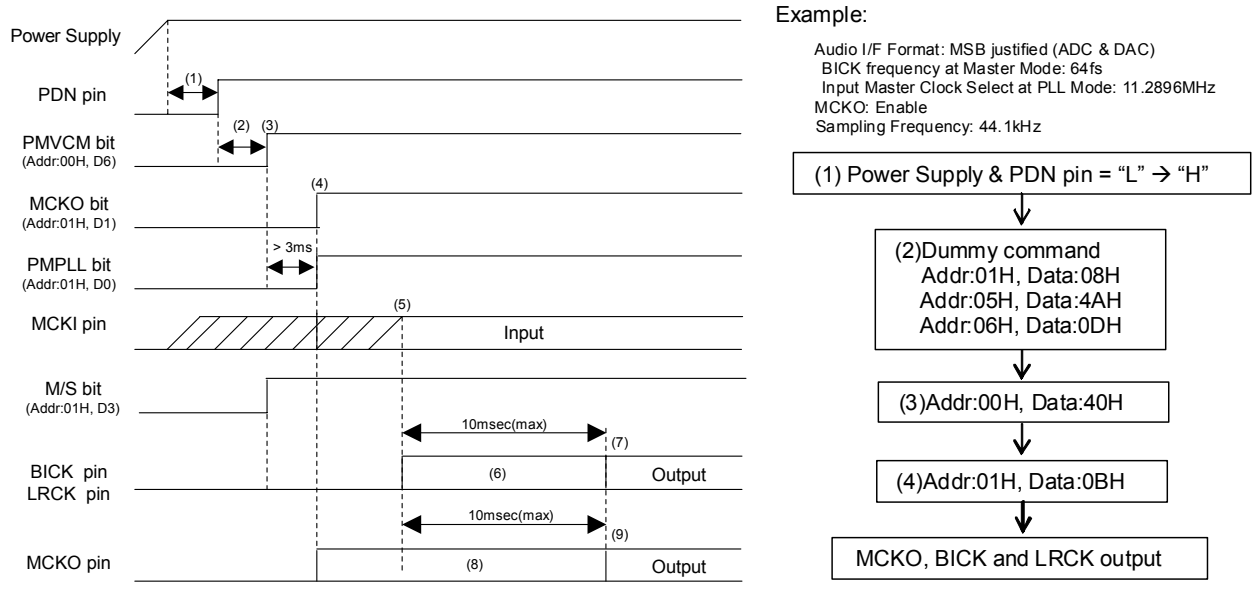


Figure 51. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin "L" → "H".
"L" time of 150ns or more is needed to reset the AK4953A.

(2) After Dummy Command input, M/S, DIF1-0, BCKO, PLL3-0, FS3-0, DS and PS1-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 3ms (max).

(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(5) PLL starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source, and PLL lock time is 10ms (max).

(6) BICK pin outputs "H" and LRCK pin outputs "L" during this period.

(7) The AK4953A starts to output the LRCK and BICK clocks after the PLL became stable. Then normal operation starts.

(8) The invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".

(9) The normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (BICK pin)

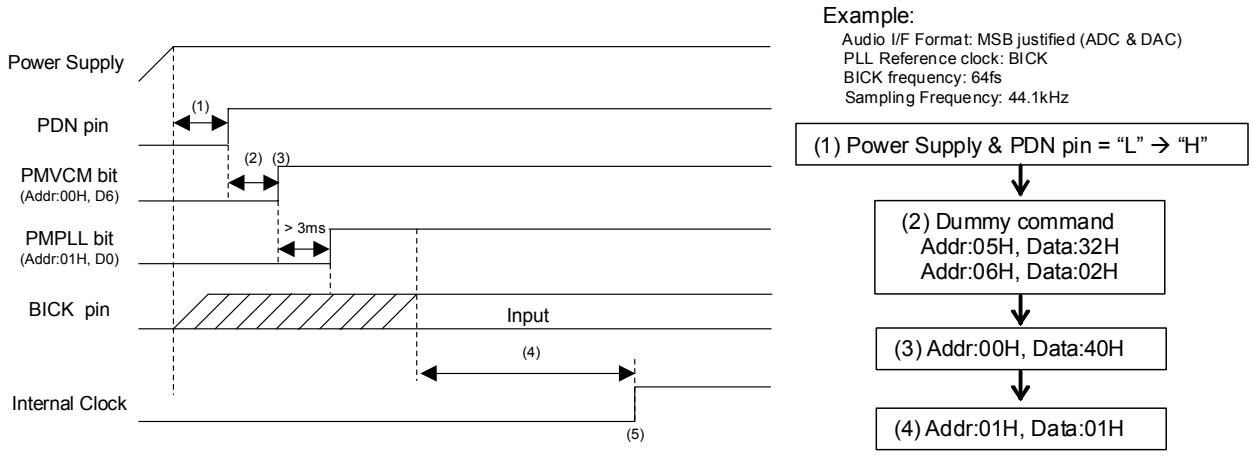


Figure 52. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4953A.

(2) After Dummy Command input, DIF1-0, PLL3-0, FS3-0 and DS bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 3ms (max).

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (BICK pin) is supplied. PLL lock time is 2ms (max) when BICK is a PLL reference clock.

(5) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

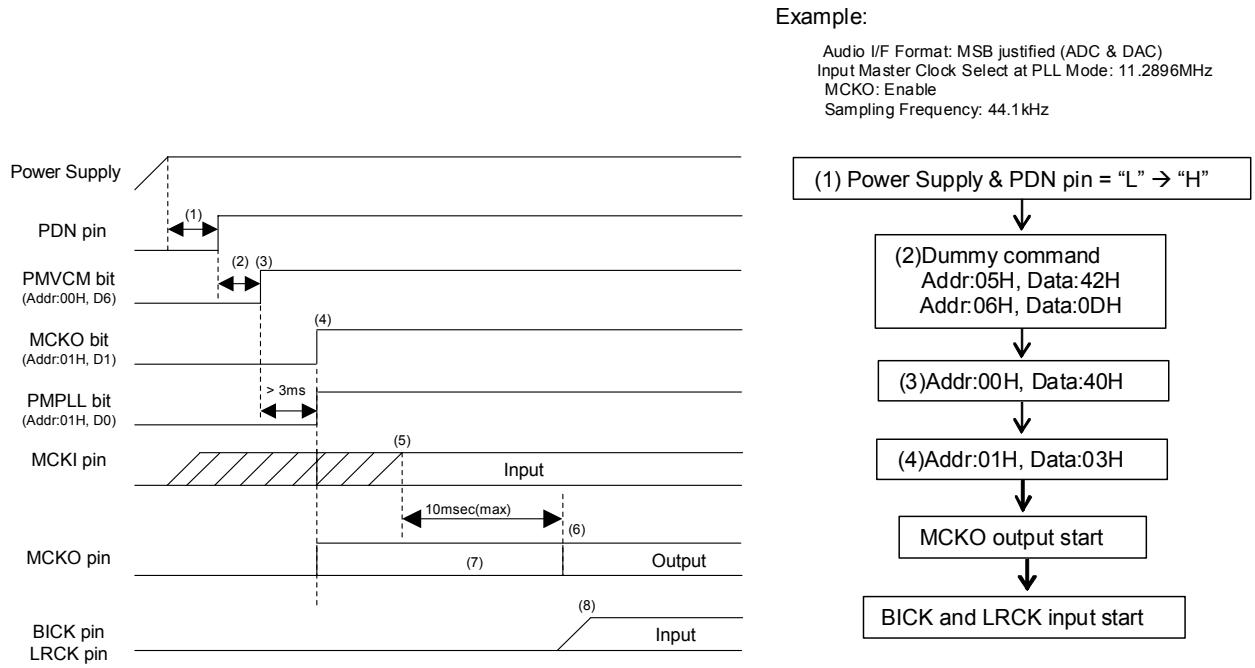


Figure 53. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4953A.

(2) After Dummy Command input, DIF1-0, PLL3-0, FS3-0, DS and PS1-0 bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates. Power up time is 3ms (max).

(4) Enable MCKO output: MCKO bit = "1"

(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 10ms (max).

(6) The normal clock is output from MCKO after PLL is locked.

(7) The invalid frequency is output from MCKO during this period.

(8) BICK and LRCK clocks must be synchronized with MCKO clock.

4. EXT Slave Mode

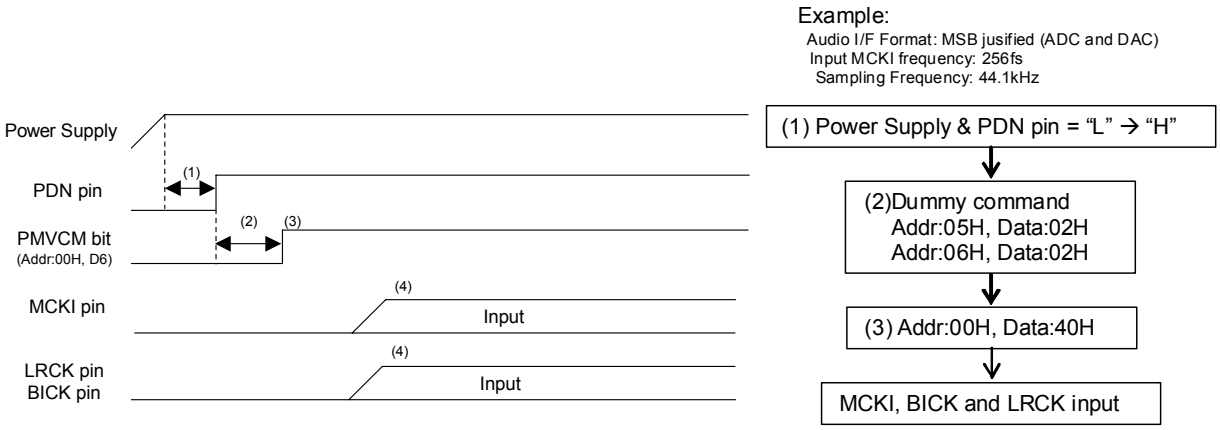


Figure 54. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4953A.

(2) After Dummy Command input, DIF1-0, FS3-0 and DS bits must be set during this period.

(3) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates.

(4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

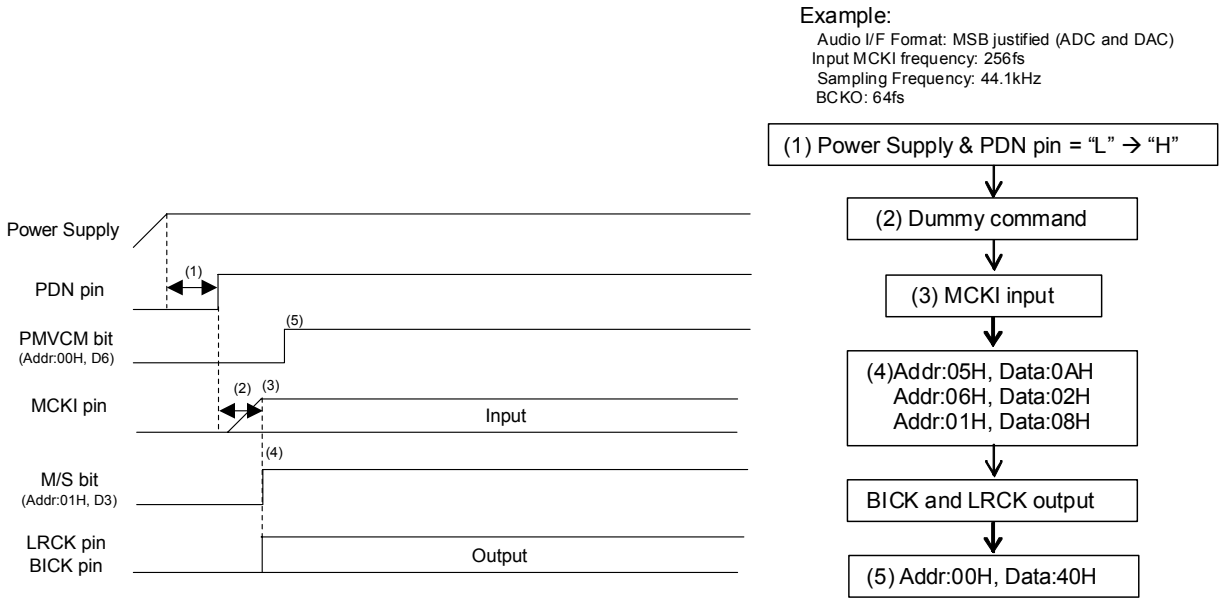


Figure 55. Clock Set Up Sequence (5)

<Example>
(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK4953A.
(2) Dummy Command must be input during this period.
(3) MCKI is supplied.
(4) After DIF1-0, BCKO, FS3-0 and DS bits are set. M/S bit should be set to "1". Then LRCK and BICK are output.
(5) Power Up VCOM and Regulator: PMVCM bit = "0" → "1"
VCOM and Regulator must first be powered-up before the other block operates.

■MIC Input Recording (Stereo)

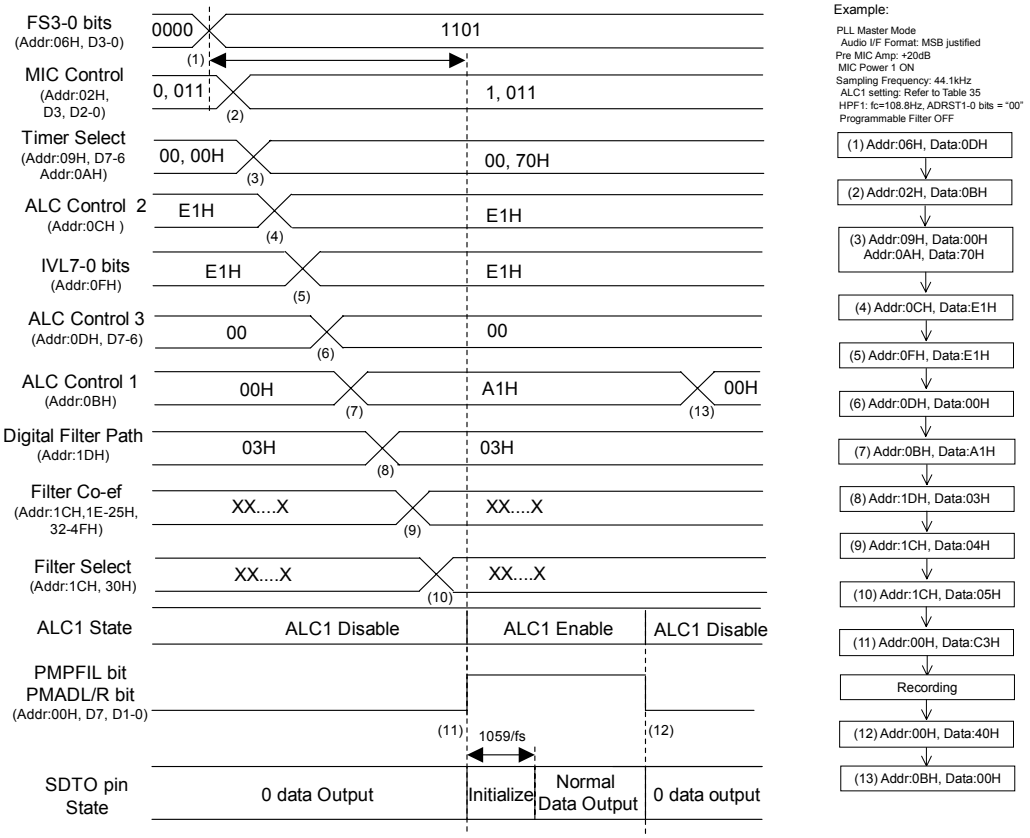


Figure 56. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=44.1kHz. For changing the parameter of ALC, please refer to "Registers Set-up Sequence at ALC1 Operation (recording path)".

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4953A is the PLL mode, MIC, ADC and Programmable Filter of (11) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up MIC Gain (Addr = 02H)
(3) Set up ALC1 Timer, ADRST1-0 bits (Addr = 09H, 0AH)
(4) Set up IREF value at ALC1 (Addtr = 0CH)
(5) Set up IVOL value at ALC1 operation start (Addr = 0FH)
(6) Set up RGAIN1-0 bits (Addr =0DH)
(7) Set up LMTH1-0, LMAT1-0, ZELMN, ALC1 and LFST bits (Addr = 0BH)
(8) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)
(9) Set up Coefficient Programmable Filter (Addr: 1CH, 1EH ~ 25H, 32H ~ 4FH)
(10) Set up of Programmable Filter ON/OFF
(11) Power Up MIC, ADC and Programmable Filter: PMADL =PMADR =PMPFIL bits = "0" →"1"
The initialization cycle time of ADC is 1059/fs=24ms @ fs=44.1kHz, ADRST1-0 bit = "00". ADC outputs "0" data during the initialization cycle. After the ALC1 bit is set to "1", the ALC1 operation starts from IVOL value of (5).
(12) Power Down MIC, ADC and Programmable Filter: PMADL = PMADR = PMPFIL bits = "1" → "0"
(13) ALC Disable: ALC1 bit = "1" → "0"

■Digital MIC Input Recording (Stereo)

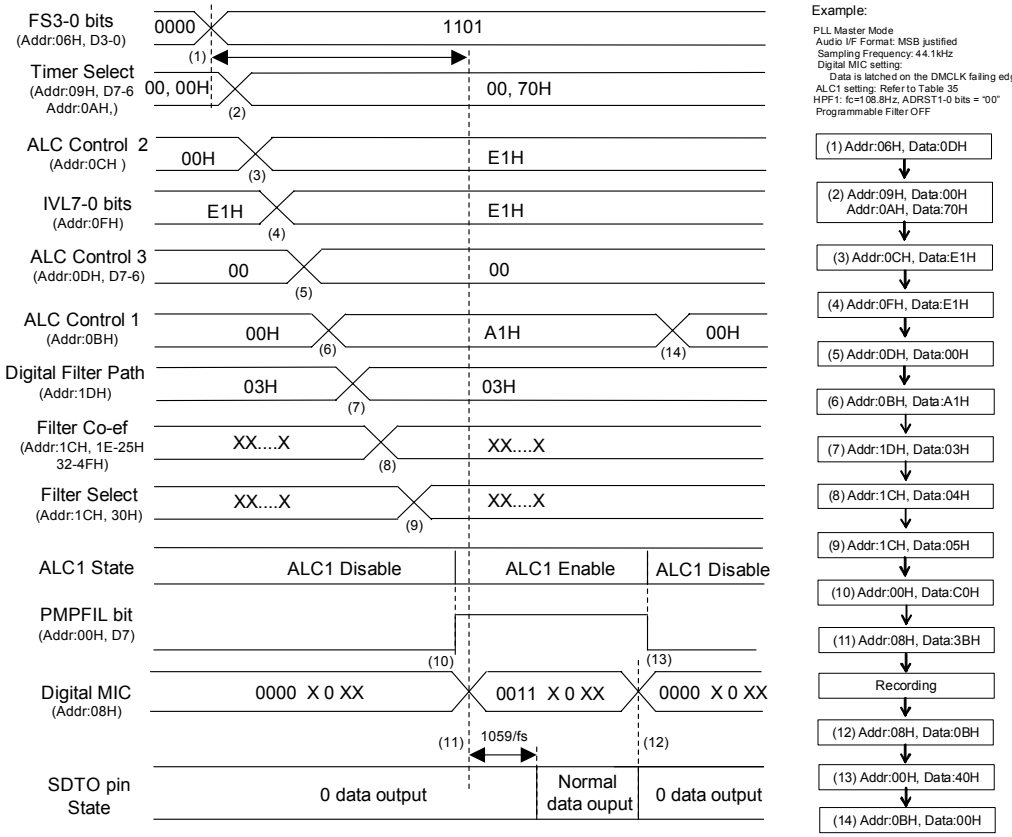


Figure 57. Digital MIC Input Recording Sequence

<Example>

This sequence is an example of ALC1 setting at fs=44.1kHz. For changing the parameter of ALC, please refer to "Registers Set-up Sequence at ALC1 Operation (recording path)".

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4953A is PLL mode, Digital MIC of (11) and Programmable Filter of (10) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up ALC1 Timer and ADRST1-0 bits (Addr = 09H, 0AH)
(3) Set up IREF value for ALC1 (Addtr = 0CH)
(4) Set up IVOL value at ALC1 operation start (Addr = 0FH)
(5) Set up RGAIN1-0 bits (Addr =0DH)
(6) Set up LMTH1-0, LMAT1-0, ZELMN, ALC1, LFST bits (Addr = 0BH)
(7) Set up Programmable Filter Path: PFSDO bit = ADCPF bit = "1" (Addr = 1DH)
(8) Set up Coefficient of Programmable Filter (Addr: 1CH, 1EH ~ 25H, 32H ~ 4FH)
(9) Set up Programmable Filter ON/OFF
(10) Power Up Programmable Filter: PMPFIL bit = "0" → "1"
(11) Set up & Power Up Digital MIC: PMDMR = PMDML bits = "0" →"1"
The initialization cycle time of ADC is 1059/fs=24ms @ fs=44.1kHz, .ADRST1-0 bit = "00". ADC outputs "0" data during initialization cycle. After the ALC1 bit is set to "1", the ALC1 operation starts from IVOL value of (5).
(12) Power Down Digital MIC: PMDMR =PMDML bits = "1" → "0"
(13) Power Down Programmable Filter: PMPFIL bit = "1" → "0"
(14) ALC1 Disable: ALC1 bit = "1" → "0"

■ Headphone-Amp Output

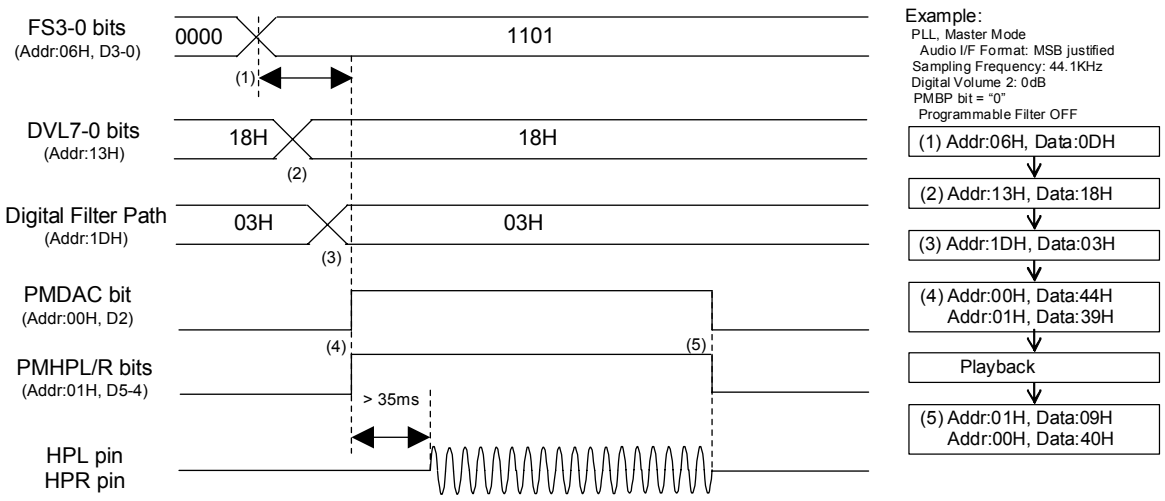


Figure 58. Headphone-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4953A is PLL mode, DAC of (4) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the output digital volume 2 (Addr = 13H)
(3) Set up Programmable Filter Path: PFDAC, ADCPF, PFSDO bits (Addr = 1DH)
(4) Power up DAC and Headphone-Amp: PMDAC = PMHPL = PMHPR bits = "0" → "1"
When PMHPL = PMHPR bits = "1", the charge pump circuit starts to power-up. The power-up time of Headphone-Amp block is 35ms (max).
(5) Power down DAC and Headphone-Amp: PMDAC = PMHPL = PMHPR bits = "1" → "0"

■ Beep Signal Output from Headphone-Amp

1. Power down DAC → Headphone-Amp

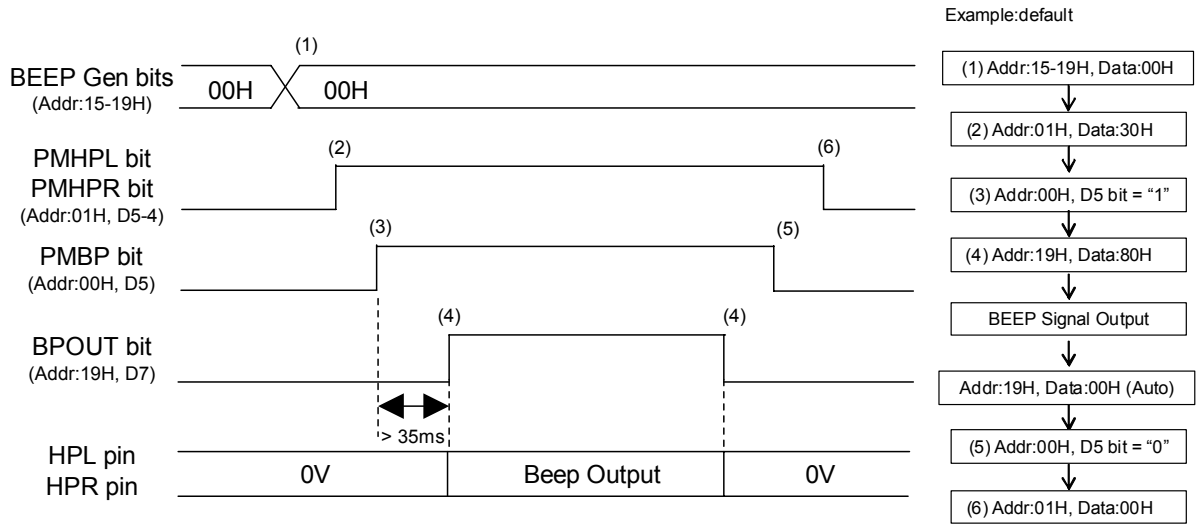


Figure 59. "BEEP Generator → Headphone-Amp" Output Sequence

<Example>
At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up BEEP Generator (Addr: 15H ~ 19H) (When repeat output time BPCNT bit = "0")
(2) Power up Headphone-Amp: PMHPL bit or PMHPR bit = "0" → "1"
(3) Power up BEEP-Generator: PMBP bit = "0" → "1"
Charge pump circuit starts to power-up. The power-up time of Headphone-Amp block is 35ms (max).
(4) BEEP output: BPOUT bit= "0" → "1"
After outputting data particular set times, BPOUT bit automatically goes to "0".
(5) Power down BEEP Generator: PMBP bit = "1" → "0"
(6) Power down Headphone-Amp: PMHPL bit or PMHPR bit = "1" → "0"

2. Power up DAC → Headphone-Amp

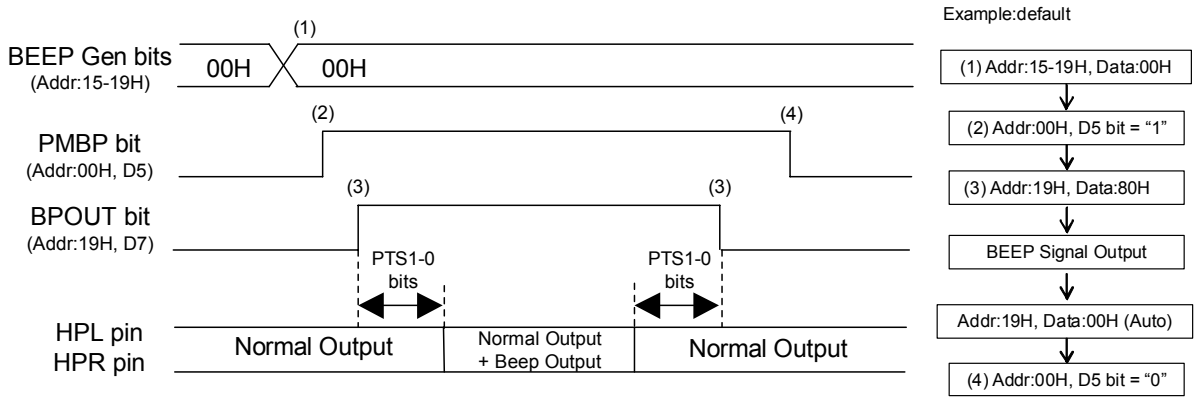


Figure 60. "BEEP Generator → Headphone-Amp" Output Sequence

<Example>
At first, clocks should be supplied according to "Clock Set Up" sequence, and Headphone-Amp output should be started according to "Headphone-Amp Output" sequence.

(1) Set up BEEP Generator (Addr: 15H ~ 19H) (When repeat output time BPCNT bit = "0")
(2) Power up BEEP Generator: PMBP bit = "0" → "1"
(3) BEEP output: BPOUT bit= "0" → "1"
After the transition time by setting PTS1-0 bits, BEEP signal is started to output. After outputting data particular set times, BPOUT bit automatically goes to "0".
(4) Power down BEEP Generator: PMBP bit = "1" → "0"

■ Speaker-Amp Output

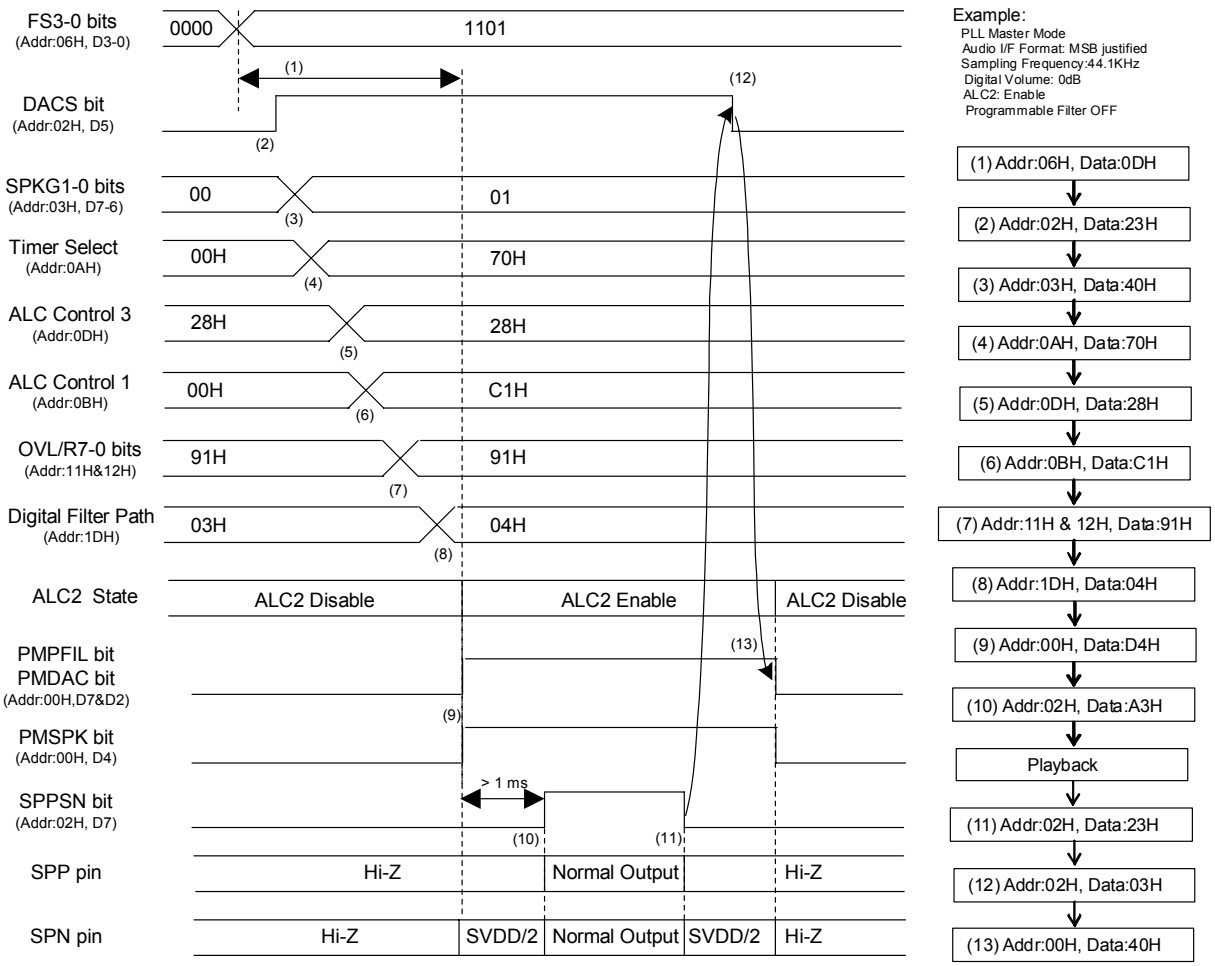


Figure 61. Speaker-Amp Output Sequence

<Example>

At first, clocks must be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bits). When the AK4953A is PLL mode, DAC and Speaker-Amp of (9) must be powered-up in consideration of PLL lock time after a sampling frequency is changed.
(2) Set up the path of DAC → SPK-Amp: DACS bit = "0" → "1"
(3) SPK-Amp gain setting: SPKG1-0 bits = "00" → "01"
(4) Set up Timer Select for ALC2 (Addr = 0AH)
(5) Set up OREF value for ALC2 and RGAIN1-0 bits (Addr = 0DH)
(6) Set up LMTH1-0, LMAT1-0, ZELMIN, ALC2 and LFST bits (Addr = 0BH)
(7) Set up the output digital volume (Addr = 11H, 12H)
Set up OVOL value at ALC2 operation start. When OVOLC bit is "1" (default), OVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition. When ALC2 bit = "0", it could be digital volume control.
(8) Set up Programmable Filter Path: PFDAC, ADCPF, PFSDO bits (Addr = 1DH)
(9) Power up DAC, Programmable Filter and Speaker: PMDAC = PMPFIL = PMSPK bits = "0" → "1"
(10) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
(11) Enter Speaker-Amp Power-save-mode: SPPSN bit = "1" → "0"
(12) Disable the path of "DAC → SPK-Amp": DACS bit = "1" → "0"
(13) Power down DAC, Programmable Filter and Speaker: PMDAC = PMPFIL = PMSPK bits = "1" → "0"

■ Beep Signal Output from Speaker-Amp

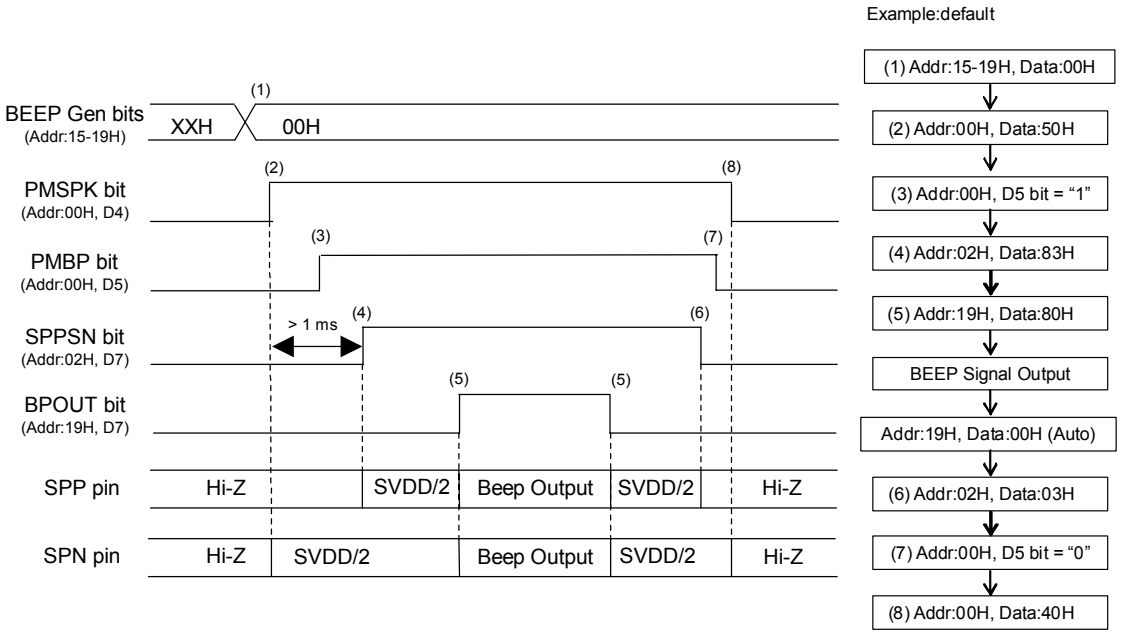


Figure 62. "BEEP Generator → Speaker-Amp" Output Sequence

<Example>
At first, clocks must be supplied according to "Clock Set Up" sequence.

(1) Set up BEEP Generator (Addr: 15H ~ 19H) (When repeat output time BPCNT bit = "0")
(2) Power up Speaker: PMSPK bit = "0" → "1"
(3) Power up BEEP Generator: PMBP bit = "0" → "1"
(4) Exit the power-save-mode of Speaker-Amp: SPPSN bit = "0" → "1"
(5) BEEP output: BPOUT bit= "0" → "1"
After outputting data particular set times, BPOUT bit automatically goes to "0".
(6) Enter Speaker-Amp Power-save-mode: SPPSN bit = "1" → "0"
(7) Power down BEEP Generator: PMBP bit = "1" → "0"
(8) Power down Speaker: PMSPK bit = "1" → "0"

■ Stop of Clock

When any circuits of the AK4953A are powered-up, the clocks must be supplied.

1. PLL Master Mode

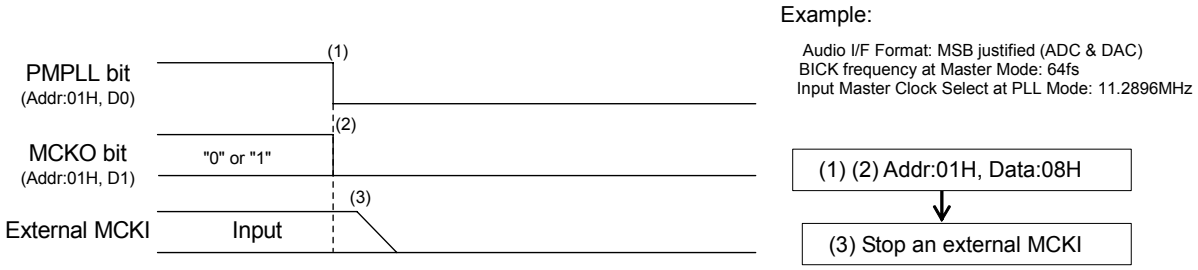


Figure 63. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (BICK pin)

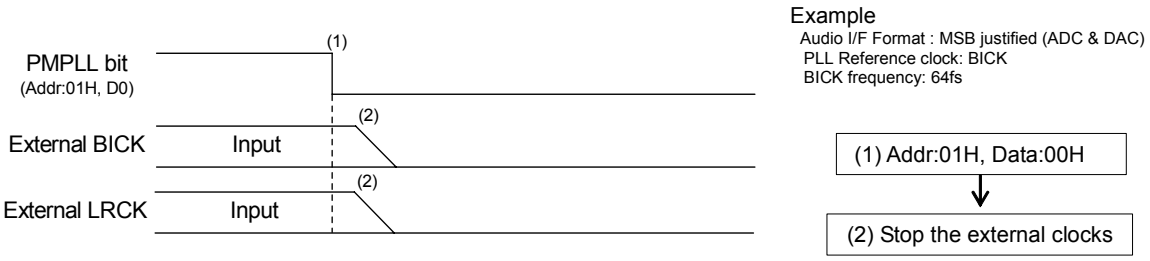


Figure 64. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external BICK and LRCK clocks.

3. PLL Slave (MCKI pin)

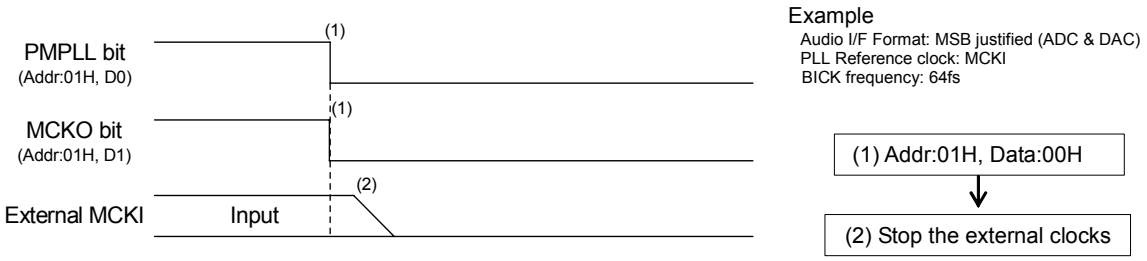


Figure 65. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
Stop MCKO output: MCKO bit = "1" → "0"
(2) Stop the external master clock.

4. EXT Slave Mode

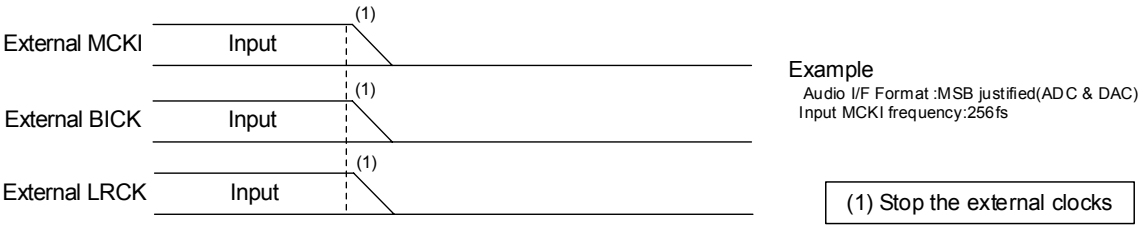


Figure 66. Clock Stopping Sequence (4)

<Example>
(1) Stop the external MCKI, BICK and LRCK clocks.

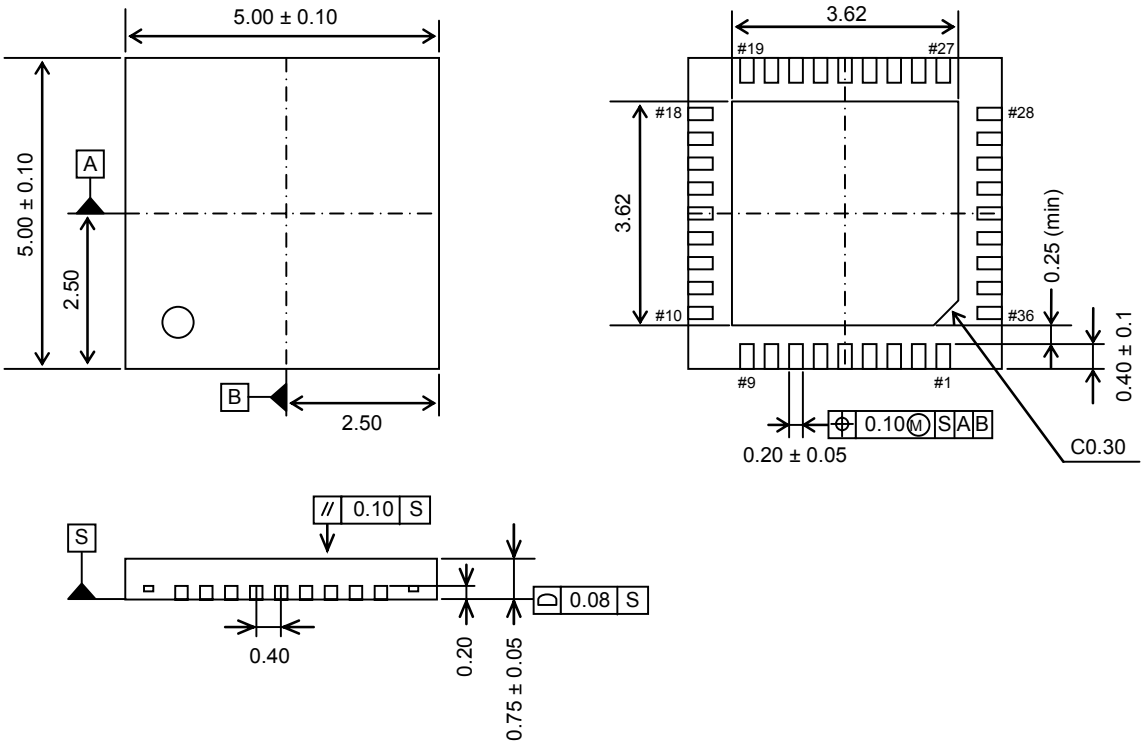
■ Power down

Power supply current can not be shut down by stopping clocks and setting PMVCM bit = "0". Power supply current can be shut down (typ. 1μA) by stopping clocks and setting the PDN pin = "L". When the PDN pin = "L", all registers are initialized.

PACKAGE

36pin QFN (Unit: mm)

TOP VIEW BOTTOM VIEW

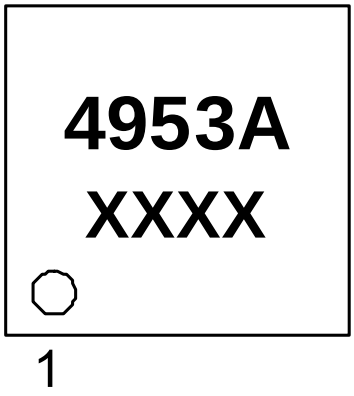


Note: The exposed pad on the bottom surface of the package must be connected to the ground.

■ Material & Lead finish

Package molding compound: Epoxy Resin, Halogen (bromine and chlorine) free
Lead frame material: Cu Alloy
Lead frame surface treatment: Ni/Pd/Au Plate

MARKING



XXXX: Date code (4 digit)
Pin #1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page/Line	Contents
10/10/20	00	First Edition		