SIEMENS

8M × 32-Bit Dynamic RAM Module — HYM 328020GD-50/-60
SMALL OUTLINE MEMORY MODULE

Preliminary Information

- 8 388 608 words by 32-bit organization
- Fast access and cycle time
  50 ns access time
  95 ns cycle time (-50 version)
  60 ns access time
  110 ns cycle time (-60 version)
- Fast page mode capability with
  35 ns cycle time (-50 version)
  40 ns cycle time (-60 version)
- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
  max. 2016 mW active (-50 version)
  max. 1728 mW active (-60 version)

  LVCMOS– 3.6 mW standby
  LVTTL – 28.8 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh, Self Refresh
- 4 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 72 pin, dual read-out, two bank, Small Outline DIMM Module
- Utilizes four 4M × 16 -DRAMs (HYB 3165160T)
- 4096 refresh cycles / 64 ms
- Gold contact pad

The HYM 328020GD -50/-60 is a 32 MByte DRAM module organized as 8 388 608 words by 32-bit in a 72-pin, dual read-out, small outline package comprising four HYB 3165160T 4M × 16 DRAMs in 500 mil wide TSOPII-54 - packages mounted together with four 0.2 µF ceramic decoupling capacitors on a PC board. Each HYB 3165800T is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

These modules are ideal for portable systems applications where high memory capacity is needed.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 328020GD -50	on request	L-DIM-72-2	50 ns DRAM module
HYM 328020GD -60	on request	L-DIM-72-2	60 ns DRAM module

Pin Names

A0-A11	Row Address Input
A0-A9	Column Address Inputs
DQ0 - DQ31	Data Input/Output
RAS0 - RAS3	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
WE	Read / Write Input
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD7	Presence Detect Pins
N.C.	No Connection

Presence-Detect and ID-pin Thruth Table *):

Module	PD1	PD2	PD3	PD4	PD5	PD6	PD7
HYM 328020GD -50	NC	NC	VSS	VSS	VSS	VSS	NC
HYM 328020GD -60	NC	NC	VSS	VSS	NC	NC	NC

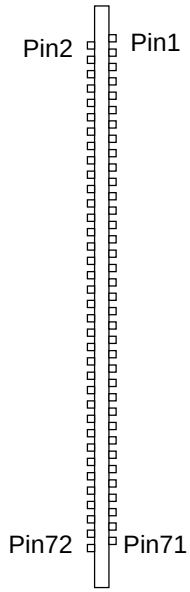
note: PD1 .. PD4 : configuration
PD5 .. PD6 : speed
PD7 : refresh mode (NC = normal refresh)

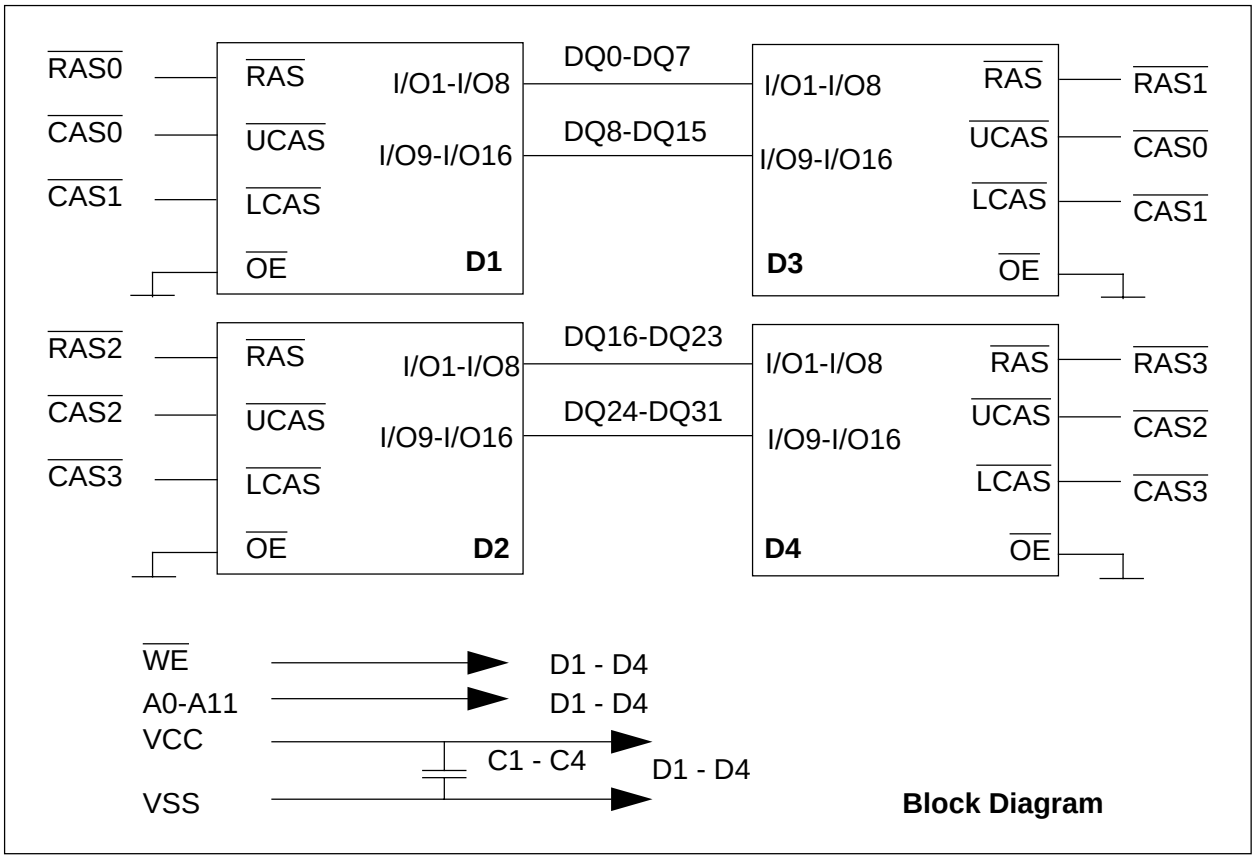
*) according to JEDEC letter ballot JC-42.5-95 Item #646/651

Pin Configuration

PIN	Name	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	37	DQ16	2	DQ0	38	DQ17
3	DQ1	39	VSS	4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	$\overline{CAS2}$	6	DQ4	42	$\overline{CAS3}$
7	DQ5	43	$\overline{CAS1}$	8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	$\overline{RAS1}$	10	VCC	46	NC
11	PD1	47	$\overline{WRITE}$	12	A0	48	NC
13	A1	49	DQ18	14	A2	50	DQ19
15	A3	51	DQ20	16	A4	52	DQ21
17	A5	53	DQ22	18	A6	54	DQ23
19	A10	55	NC	20	NC	56	DQ24
21	DQ8	57	DQ25	22	DQ9	58	DQ26
23	DQ10	59	DQ28	24	DQ11	60	DQ27
25	DQ12	61	VCC	26	DQ13	62	DQ29
27	DQ14	63	DQ30	28	A7	64	DQ31
29	A11	65	NC	30	VCC	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	$\overline{RAS3}$	69	PD5	34	$\overline{RAS2}$	70	PD6
35	DQ15	71	PD7	36	NC	72	VSS

Front Side **Back Side**





Block Diagram

Absolute Maximum Ratings [1)]

Operating temperature range.....0 to 70 ˚C

Storage temperature range.....– 55 to 150 ˚C

Soldering temperature.....260 ˚C

Soldering time.....10 s

Input/output voltage.....-0.5 to min (Vcc+0.5,4.6) V

Power supply voltage.....-0.5V to 4.6 V

Power dissipation.....1.0 W

Data out current (short circuit).....50 mA

DC Characteristics

T_A = 0 to 70 ˚C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	2)
Input low voltage	V_{IL}	– 0.3	0.8	V	2)
Output high voltage (LVTTL) Output „H“ level voltage (Iout = -2mA)	V_{OH}	2.4	–	V	
Output low voltage (LVTTL) Output „L“level voltage (Iout = +2mA)	V_{OL}	–	0.4	V	
Output high voltage (LVCMOS) Output „H“ level voltage (Iout = -100uA)	V_{OH}	Vcc-0.2	-	V	6)
Ouput low voltage (LVCMOS) Output „L“ level voltage (Iout = +100uA)	V_{OL}	-	0.2	V	6)
Input leakage current,any input (0 V < Vin < Vcc , all other pins = 0 V	$I_{I(L)}$	– 10	10	µA	
Output leakage current (DO is disabled, 0 V < $Vout$ < Vcc)	$I_{O(L)}$	– 10	10	µA	
Average Vcc supply current: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC min.)	I_{CC1}	 – –	 560 480	 mA mA	3) 4) 5)
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= Vih)	I_{CC2}	–	8	mA	–
Average Vcc supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = VIH: tRC = tRC min.)	I_{CC3}	 – –	 560 480	 mA mA	3) 5)

DC Characteristics (cont'd)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average *V*cc supply current, during fast page mode: -50 ns version -60 ns version ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: tPC=tPC min.)	I_{CC4}	– –	340 300	mA mA	3) 4) 5)
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= *V*cc-0.2V)	I_{CC5}	–	800	A	–
Average Vcc supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$ cycling: tRC = tRC min.)	I_{CC6}	– –	560 480	mA mA	3) 4)
Self Refresh Current Average Power Supply Current during Self Refresh. ($\overline{CBR}$ cycle with tRAS>TRASSmin, $\overline{CAS}$ held low, $\overline{WE}$ = Vcc-0.2V, Address and Din=Vcc-0.2V or 0.2V)	I_{CC7}	–	800	A	

SO-DIMM PACKAGE OUTLINES

