

### General Description

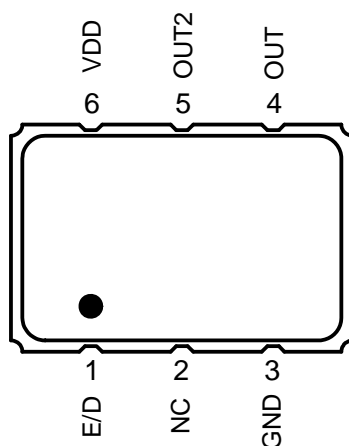
The XLP is an LVPECL Crystal Oscillator with 860fs typical phase jitter over 12kHz to 20 MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the IDT XLP Series Crystal Oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XLP is an excellent choice over the conventional technologies. The XLP has stabilities as tight as  $\pm 20\text{ppm}$  with extremely quick delivery for both standard and custom frequencies

### Features

- Frequency range: 0.750 to 1350 MHz
- Output Type: LVPECL
- Frequency Stability:  $\pm 20\text{ppm}$ ,  $\pm 25\text{ppm}$ ,  $\pm 50\text{ppm}$ , or  $\pm 100\text{ppm}$
- Supply Voltage: 2.5V or 3.3V
- Phase Jitter (1.875MHz to 20MHz): 225fs typical
- Phase Jitter (12kHz to 20MHz): 860fs typical
- Package options: 5.0mm x 3.2mm x 1.2mm (JS6)  
7.0mm x 5.0mm x 1.3mm (JU6)
- Operating Temperatures:  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### Pin Assignment



6-pin CLCC

### Pin Descriptions

Pin Number	Pin Name	Description
1	E/D	Enable/Disable <sup>1</sup> (0=Output Disabled)
2	NC	No connect
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary Output
6	VDD	Supply voltage

1. Pulled high internally.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XLP. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0 V
E/D	-0.5 V to VDD + 0.5 V
OUT	-0.5 V to VDD + 0.5 V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

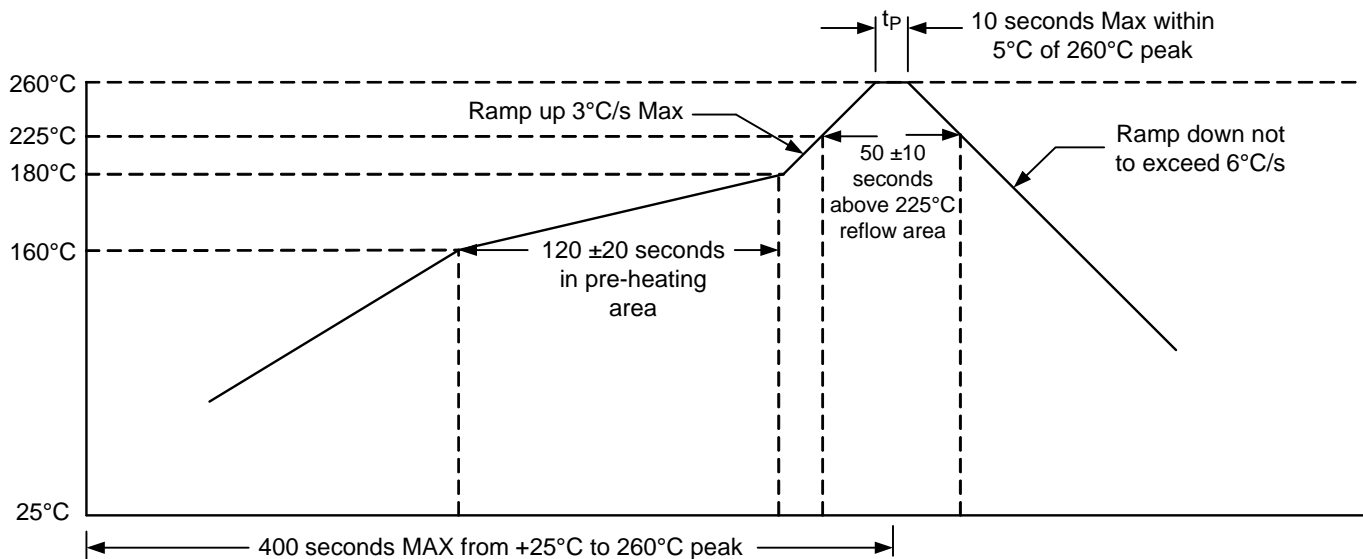
## ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

## Mechanical Testing

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface–3 times
Mechanical Vibration	10–55Hz, 1.5mm amplitude, 1 minute sweep 2 hours each in 3 directions (X, Y, Z)
High Temperature Burn-in	Under power @ 125°C for 2000 hours
Hermetic Seal	He pressure: $4 \pm 1 \text{ kgf/cm}^2$ 2 hour soak

## Solder Reflow Profile



## DC Characteristics

( $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -20^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $-40^\circ$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Common Frequencies			120	mA
Output HIGH Voltage	$V_{OH}$	Standard LVPECL load	2.055		2.405	V
Output LOW Voltage	$V_{OL}$	Standard LVPECL load	1.305		1.650	V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

## AC Characteristics

( $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $T_A = -20^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $-40^\circ$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		1350	MHz
Frequency Stability		Temperature = $-20^\circ\text{C}$ to $+70^\circ\text{C}$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ\text{C}$ to $+85^\circ\text{C}$	$\pm 25$		$\pm 100$	ppm
Aging (1 <sup>st</sup> year)		$T_a = 25^\circ\text{C}$			3	
Aging (10 years)		$T_a = 25^\circ\text{C}$			10	
Output Load		To $V_{DD} - 2.0\text{V}$		50		Ohms
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{PP}$			400	ps
Output Fall Time		80% to 20% $V_{PP}$			400	ps
Output Clock Duty Cycle	$T_{DTCY}$	50% $V_{P-P}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 156.25MHz		5.80		ps
Random Jitter	$R_J$	Frequency = 156.25MHz		1.29		ps
Deterministic Jitter	$D_J$	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		9.3		ps
Total Jitter	$T_J$			27.7		ps
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Common Frequencies		860		fs
Phase Noise Performance Frequency = 156.25MHz	$\phi_{NOISE}$	100Hz of Carrier		-80		dBc/Hz
		1kHz of Carrier		-115		dBc/Hz
		10kHz of Carrier		-117		dBc/Hz
		100kHz of Carrier		-121		dBc/Hz
		1MHz of Carrier		-142		dBc/Hz
		10MHz of Carrier		-150		dBc/Hz
Output Frequency (Common)	$F_{OUT}$	100MHz, 106.25MHz, 125.8MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at  $25^\circ\text{C}$ . We do not recommend hand soldering the devices

## DC Characteristics

( $V_{DD} = 2.5\text{ V} \pm 5\%$ ,  $T_A = -20^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $-40^\circ$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Common Frequencies	33		72	mA
Output HIGH Voltage	$V_{OH}$	Standard LVPECL load		1.40		V
Output LOW Voltage	$V_{OL}$	Standard LVPECL load		0.68		V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

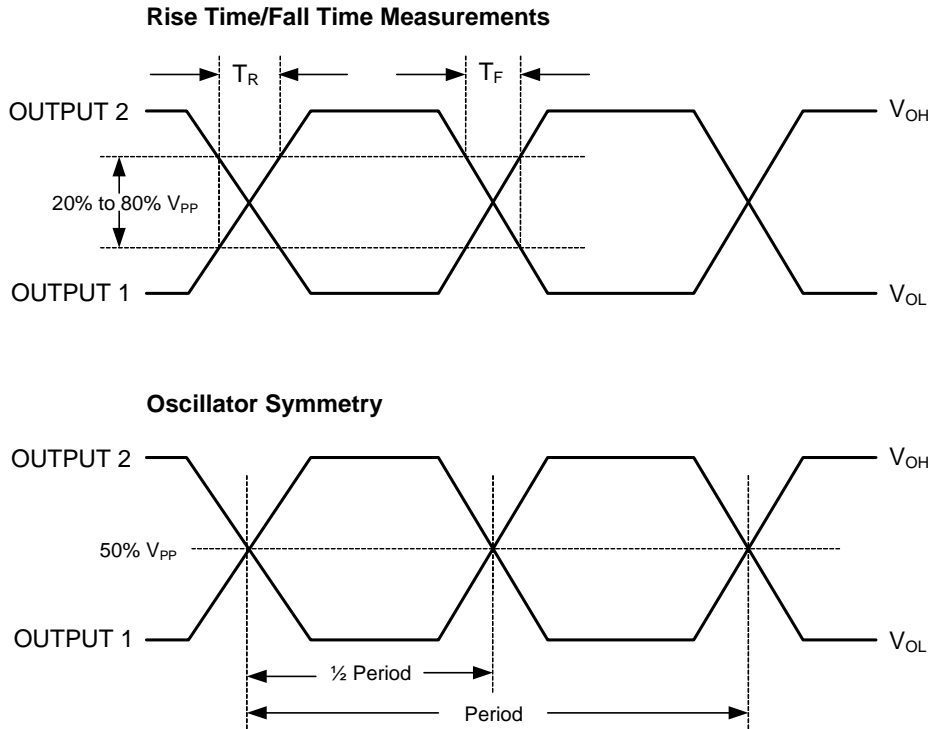
## AC Characteristics

( $V_{DD} = 2.5\text{ V} \pm 5\%$ ,  $T_A = -20^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $-40^\circ$  to  $+85^\circ\text{C}$ )

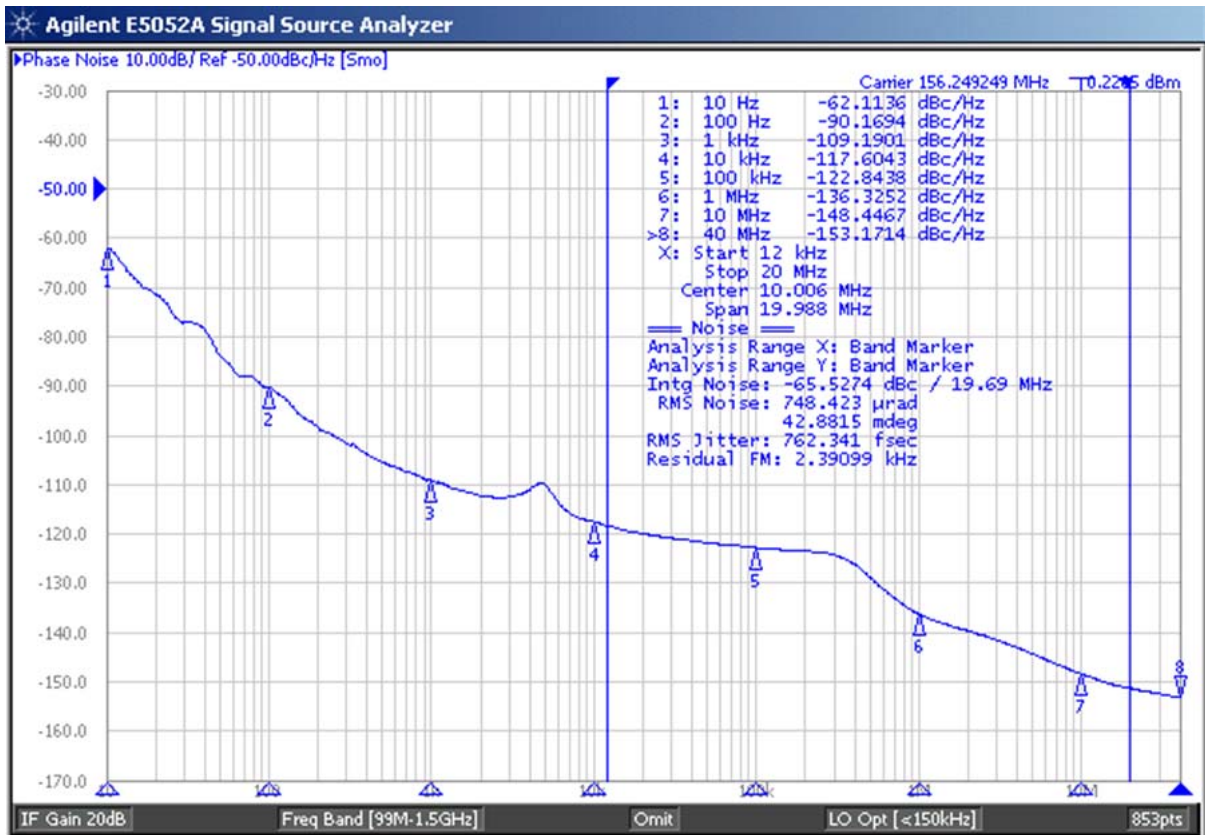
Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		1000	MHz
Frequency Stability		Temperature = $-20^\circ\text{C}$ to $+70^\circ\text{C}$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ\text{C}$ to $+85^\circ\text{C}$	$\pm 25$		$\pm 100$	ppm
Output Load		To $V_{DD} - 2.0\text{V}$		50		Ohms
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{PP}$			400	ps
Output Fall Time		80% to 20% $V_{PP}$			400	ps
Output Clock Duty Cycle	$T_{DTCY}$	50% $V_{P-P}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 156.25MHz		5.12		ps
Random Jitter	$R_J$	Frequency = 156.25MHz		1.36		ps
Deterministic Jitter	$D_J$	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		10.0		ps
Total Jitter	$T_J$			29.3		ps
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Frequency = 156.25MHz		1200		fs
Phase Noise Performance Frequency = 156.25MHz	$\phi_{NOISE}$	100Hz of Carrier		-83.2		dBc/Hz
		1kHz of Carrier		-106.5		dBc/Hz
		10kHz of Carrier		-115.6		dBc/Hz
		100kHz of Carrier		-120.2		dBc/Hz
		1MHz of Carrier		-136.1		dBc/Hz
		10MHz of Carrier		-145.9		dBc/Hz
Output Frequency (Standards)	$F_{OUT}$	100MHz, 106.25MHz, 125.8MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at  $25^\circ\text{C}$ . We do not recommend hand soldering the devices

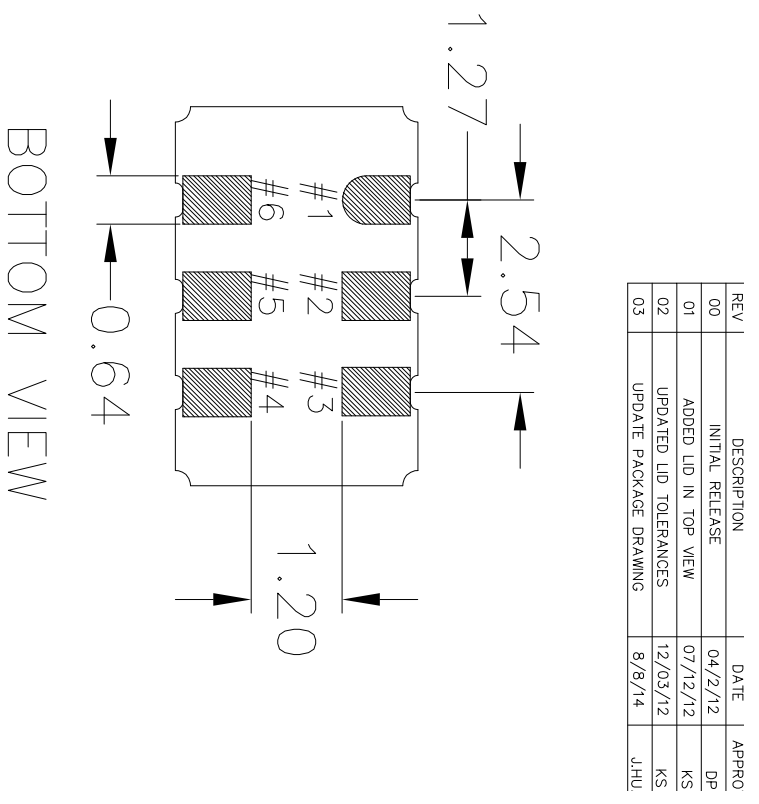
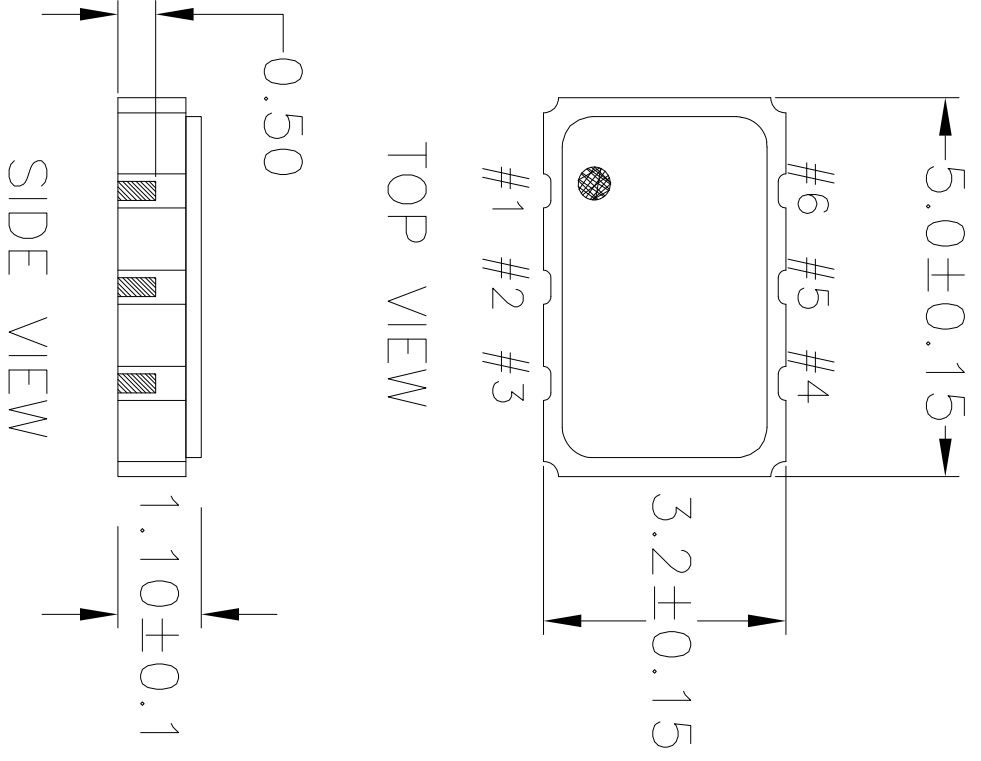
# Output Waveform



# Typical Phase Noise (3.3V)



# JS6 Package Outline and Dimensions



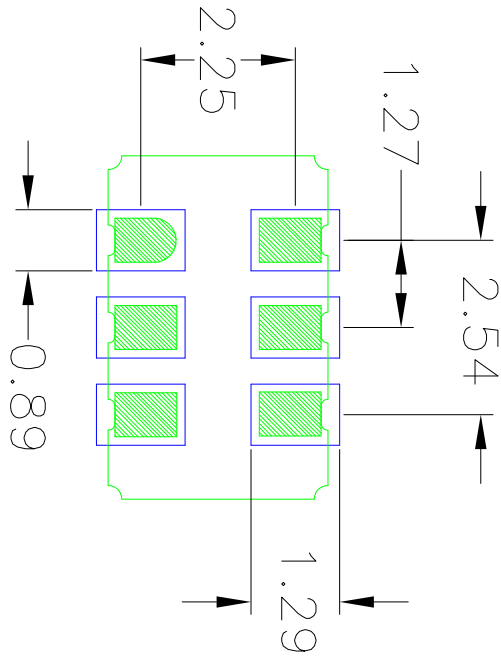
REV	DESCRIPTION	DATE	APPRO
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	JHU

NOTES:  
1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XXX	±
XXXX	
XXXXX	
APPROVALS	DATE
DRAWN: <b>gac</b>	04/2/12
CHECKED	
SIZE	DRAWING No.
C	PSC-4411

6024 Silver Creek Valle  
San Jose, CA 95138  
PHONE: (408) 727-6116  
FAX: (408) 492-8674

# JS6 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

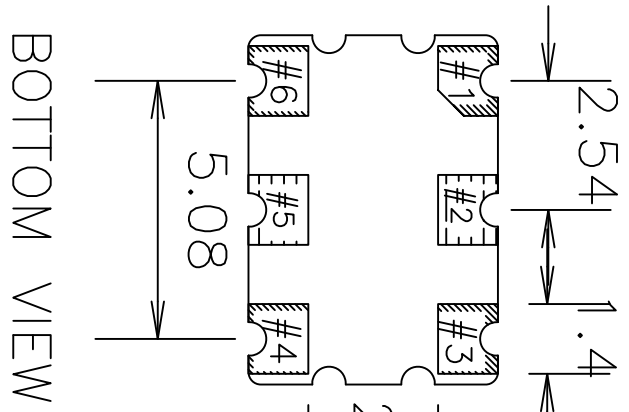
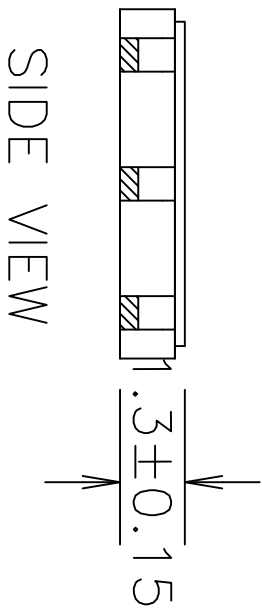
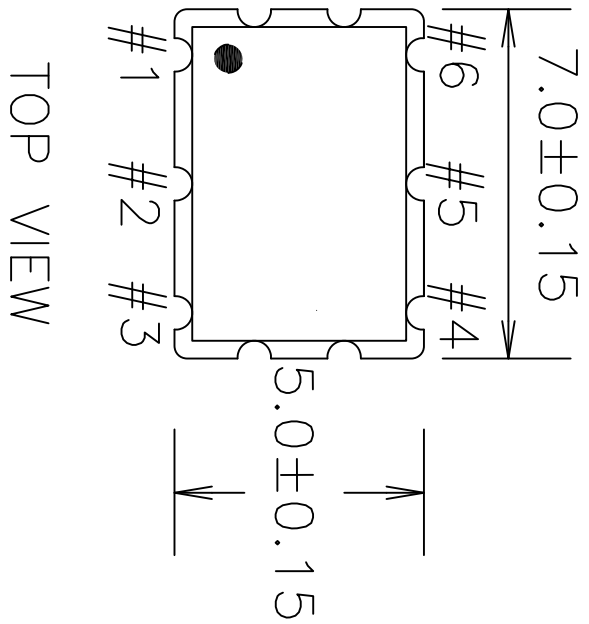
**NOTES:**

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	JHUA

TOLERANCES UNLESS SPECIFIED		<p>6024 Silver Creek Valley Rd San Jose, CA 95138 Phone: (408) 727-6116 Fax: (408) 492-8674</p>
DECIMAL	ANGULAR	
XXX±	±	
XXXX±		
DATE	TITLE	<p>www.IDT.com</p>
04/2/12	JS6 PACKAGE OUTLINE	
DRAWN	5.0 x 3.2 mm BODY	
GALG	1.1 mm Thick	
CHECKED		
SIZE	DRAWING No.	REV
C	PSC-4411	03
DO NOT SCALE DRAWING		SHEET 2 OF 2

# JU6 Package Outline and Dimensions



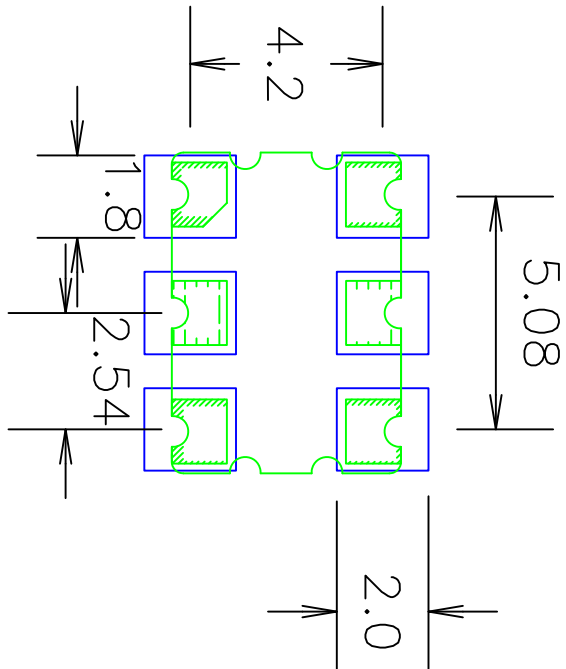
NOTES:  
1. ALL DIMENSIONS IN MM.

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	JHUA

TOLERANCES UNLESS SPECIFIED			6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
DECIMAL	ANGULAR		
XXX±	±	www.IDT.com	
XXXX±			
XXXX±			
APPROVALS	DATE	TITLE	
DRAWN: JCS	10/03/12	JU6 PACKAGE OUTLINE	
CHECKED		7.0 x 5.0 mm BODY	
		1.3 mm Thick	
SIZE	DRAWING No.	REV	
C	PSC-4430	01	



# JU6 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

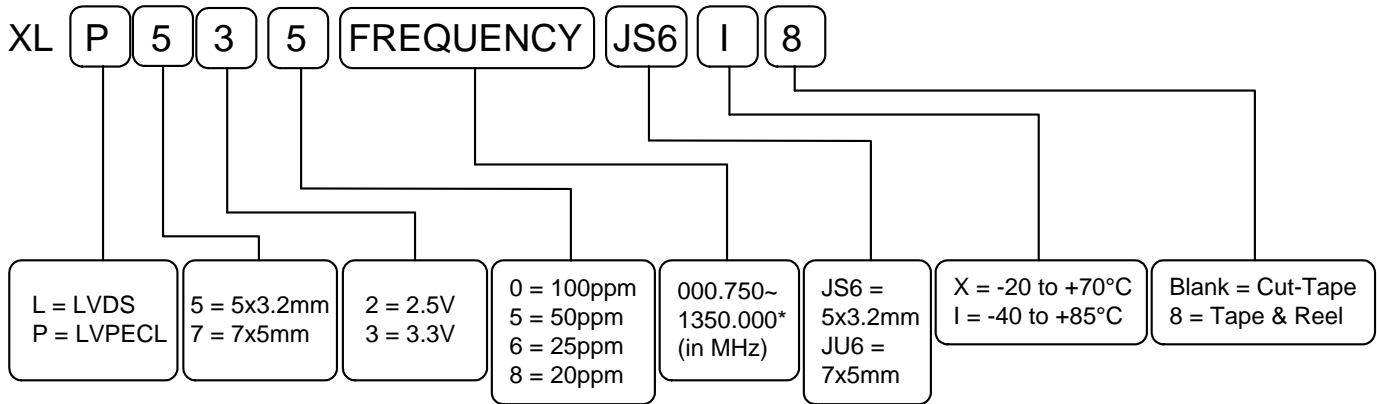
- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
  2. TOP DOWN VIEW. AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
  4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	JHUA

TOLERANCES		UNLESS SPECIFIED	
DECIMAL	±	ANGULAR	±
XXX			
XXX			
XXX			
APPROVALS	DATE	TITLE	
DRAWN: JCS	10/03/12	JU6 PACKAGE OUTLINE	
CHECKED		7.0 x 5.0 mm BODY	
		1.3 mm Thick	
SIZE	DRAWING No.	REV	
C	PSC-4430	01	
DO NOT SCALE DRAWING			SHEET 2 OF 2

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www.IDT.com

## Ordering Information



\* See table or contact IDT for custom frequencies

## Revision History

Rev.	Date	Originator	Description of Change
A	10/17/14	B. Chandhoke	Initial release.
B	12/10/14	B. Chandhoke	1. Added 7 x 5 x 1.3mm JU6 package option and package dimension/landing pattern drawings. 2. Updated ordering information table/graphic to show JU6 package option.



**Corporate Headquarters**  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA

**Sales**  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
www.IDT.com

**Tech Support**  
email: [clocks@idt.com](mailto:clocks@idt.com)

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