IS32WV204816B

2M x 16 (32-Mbit) PSEUDO STATIC RAM

MAY 2004

FEATURES

- Access time: 70ns
- TTL compatible inputs and outputs; tri-state I/O
- Wide Power supply voltage: 2.2V to 3.6V
- CMOS Standby: 70µA (32-Mbit)
- Deep Power Down Standby: 5µA (32-Mbit)
- Deep Power-Down Mode: Data Invalid
- Page Operation Mode: Four Word Access
- Logic compatible with SRAM R/W ($\overline{WE}$) pin.
- Industrial Temperature Range: -40°C to 85°C

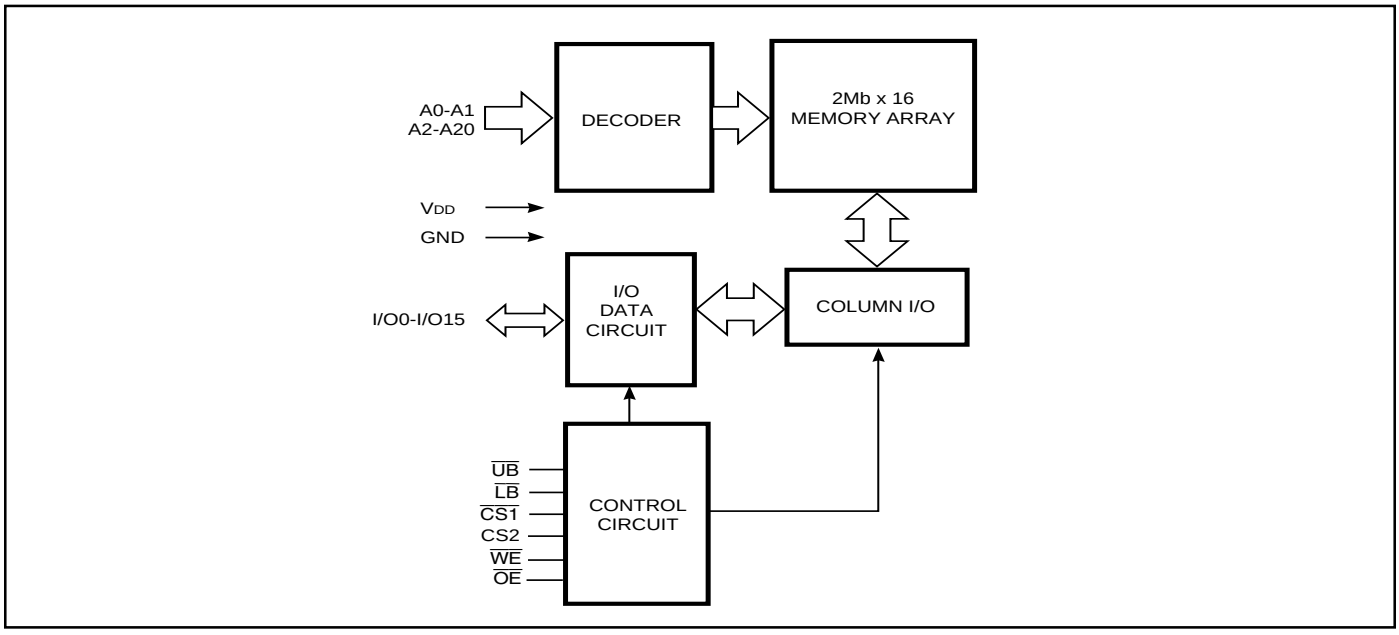
DESCRIPTION

The *ISSI* IS32WV204816B is a high-performance CMOS Pseudo Static RAM, organized as 2Meg x 16 bits.

ISSI CMOS technology provides high density, high speed low power devices that features SRAM-like write timing. Data is written to memory cells on the rising edge of the $\overline{WE}$ signal. With a page size of 4 words, the device has a page access operation. The device also supports deep power-down mode providing low-power standby.

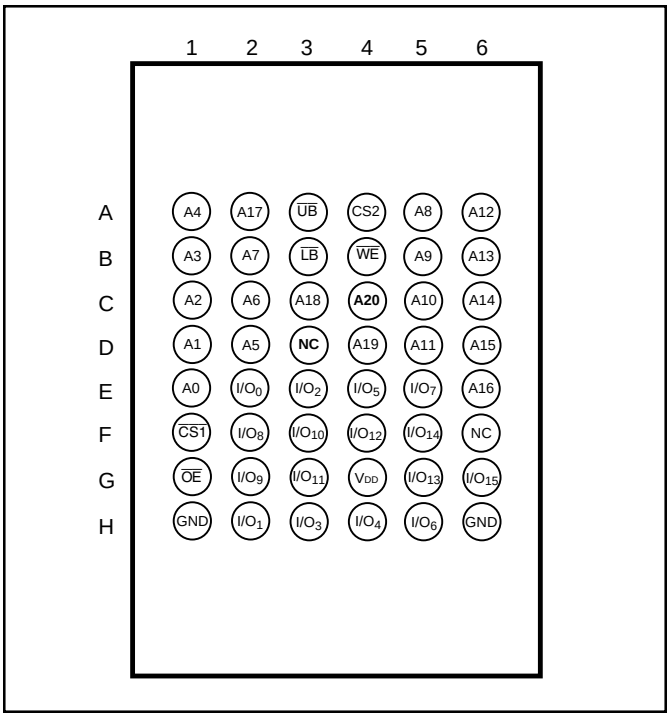
The IS32WV204816B is packaged in a 48-pin mini-BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM

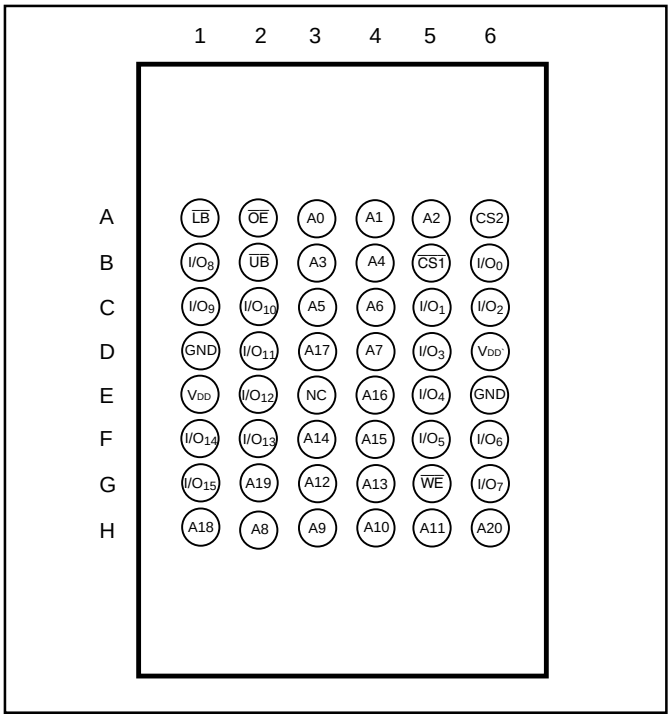


PIN CONFIGURATIONS

48-pin mini-BGA (M) (6mm x 8mm)



48-pin mini-BGA (B) (6mm x 8mm)



PIN DESCRIPTIONS

A0-A20	Address Inputs
A0-A1	Page Address Inputs
I/O0 to I/O15	Data Input/Outputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$	Chip Enable Input
CS2	Chip Select Input
$\overline{LB}$, $\overline{UB}$	Lower & Upper Data Byte Control Input
V_{DD}	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Function	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	ADD	I/O0 to I/O7	I/O8 to I/O15	Power
Read: Word	L	H	L	H	L	L	XX	I/O_{OUT}	I/O_{OUT}	I_{CC1}
Read: Lower Byte	L	H	L	H	L	H	XX	I/O_{OUT}	HIGH-Z	I_{CC1}
Read: Upper Byte	L	H	L	H	H	L	XX	HIGH-Z	I/O_{OUT}	I_{CC1}
Write: Word	L	H	X	L	L	L	XX	D_{IN}	D_{IN}	I_{CC1}
Write: Lower	L	H	X	L	L	H	XX	D_{IN}	INVALID	I_{CC1}
Write: Upper	L	H	X	L	H	L	XX	INVALID	D_{IN}	I_{CC1}
Outputs Disabled	L	H	H	H	X	X	XX	HIGH-Z	HIGH-Z	I_{SB}
Standby	H	H	X	X	X	X	X	HIGH-Z	HIGH-Z	I_{SB}
Deep Power-Down Standby	H	L	X	X	X	X	X	HIGH-Z	HIGH-Z	I_{SB3}

L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, High-Z = High-impedance. XX = At $\overline{CS1}$ falling edge, all addresses (A2 to A20) are valid "IN". Page address signals (A0 and A1) must be V_{IH} or V_{IL}, during entire cycle.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
V_T	Voltage on Any Pin Relative to GND	–0.2 to V_{DD}+3.6	V
V_{DD}	Supply Voltage	–0.2 to V_{DD}+3.6	V
I_{OUT}	Output Current	50	mA
P_D	Power Dissipation	0.6	W
T_{STG}	Storage Temperature	–55 to +150	°C

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Max.	Unit
C_{IN1}	Input Capacitance: A0-A20	10	pF
C_{IN2}	Input Capacitance: $\overline{CS1}$, CS2, $\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$	10	pF
C_{IO}	Data Input/Output Capacitance: I/O0-I/O15	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	2.2		3.6	V
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 03	V
V_{IL}	Input Low Voltage	–0.2	—	0.4	V
V_{DH}	Data Retention Supply Voltage	2.0	—	3.0	V

ELECTRICAL CHARACTERISTICS(1)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{IL}	Input Leakage Current	Any input 0V ≤ V_{IN} ≤ V_{DD} Other inputs not under test = 0V	–1.0	1.0	µA
I_{IO}	Output Leakage Current	Output is disabled (Hi-Z) 0V ≤ V_{OUT} ≤ V_{DD}	–1.0	1.0	µA
V_{OH}	Output High Voltage Level	I_{OH} = –0.5 mA	1.9	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = 1.0 mA	—	0.2	V
$I_{CC}1$	Operating Current	$\overline{CS1}$ =V_{IH}, I_{OUT} = 0mA $\overline{CS1}$ Cycling, t_{RC} = t_{RC} (min.)	—	30	mA
$I_{CC}2$	Page Access Operating Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, I_{OUT} = 0mA Page Add. Cycling, t_{PC} (min.)	—	25	mA
$I_{SB}1$	Standby Current: TTL	$\overline{CS1}$=V_{IH}, CS2=V_{IH}	—	1	mA
$I_{SB}2$	Standby Current: CMOS	$\overline{CS1}$=Vss-0.2V, CS2=V_{DD}-0.2V	—	70	µA
$I_{SB}3$	Standby Current: Deep Power-down	$\overline{CS1}$=0.2V	—	5	µA

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Random Read or Write Cycle Time	85	—	ns
t_{CE}	$\overline{CS1}$ Pulse Width	70	10K	ns
t_{P}	Pre-charge Time	15	—	ns
t_{CEA}	$\overline{CS1}$ Access Time	—	70	ns
t_{OEA}	$\overline{OE}$ Access Time	—	70	ns
t_{OEP}	$\overline{OE}$ Pulse Width	70	—	ns
t_{BEA}	$\overline{LB}$,$\overline{UB}$ Access Time	—	25	ns
t_{APH}	Address (A0 and A1) Hold Time	70	—	ns
t_{ASC}	Address Setup Time	-10	—	ns
t_{AHC}	Address Hold Time	65	—	ns
t_{ASO}, t_{ASW}	Address Setup Time	-10	—	ns
t_{AHO}, t_{AHW}	Address Hold Time	30	—	ns
t_{WHC}	$\overline{WE}$ Hold Time	8	—	ns
t_{RCS}	Read Command Setup Time	8	—	ns
t_{WOS}	Write Command Setup Time	18	—	ns
t_{RCH}	Read Command Hold Time	8	—	ns
t_{WP}	$\overline{WE}$ Pulse Width	70	—	ns
t_{WCH}	$\overline{CS1}$ to End of Write	70	—	ns
t_{CWL}	Write Command to $\overline{CS1}$ Lead Time	70	—	ns
t_{WBH}	$\overline{LB}$,$\overline{UB}$ to End of Write	45	—	ns
t_{BWL}	Write Command to $\overline{LB}$, $\overline{UB}$ Lead time	70	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DSW}	Data Set-up Time from $\overline{WE}$	25	—	ns
t_{DSC}	Data Set-up Time from $\overline{CS1}$	25	—	ns
t_{DSB}	Data Set-up Time from $\overline{LB}$, $\overline{UB}$	25	—	ns
t_{DHW}	Data Hold Time from $\overline{WE}$	0	—	ns
t_{DHC}	Data Hold Time from $\overline{CS1}$	0	—	ns
t_{DHB}	Data Hold Time from $\overline{LB}$, $\overline{UB}$	0	—	ns

Continued

AC CHARACTERISTICS Continued

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Min.	Max.	Units
t_{CLZ}	$\overline{CS1}$ Low to Output Active	10	—	ns
t_{OLZ}	$\overline{OE}$ Low to Output Active	0	—	ns
t_{BLZ}	$\overline{LB}$, $\overline{UB}$ Low to Output Active	0	—	ns
t_{WLZ}	$\overline{WE}$ Low to Output Active	0	—	ns
t_{CHZ}	$\overline{CS1}$ High to Output High-Z	—	20	ns
t_{OHZ}	$\overline{OE}$ High to Output High-Z	—	20	ns
t_{BHZ}	$\overline{LB}$, $\overline{UB}$ High to Output High-Z	—	20	ns
t_{WHZ}	$\overline{OE}$ High to Output High-Z	—	20	ns
t_{PC}	Page Mode Cycle Time	25	—	ns
t_{AA}	Page Mode Address Access Time	—	25	ns
t_{AOH}	Page Mode Output Data Hold Time	5(1)	—	ns
t_{CS}	$\overline{CS1}$ Set-up Time	0	—	ns
t_{CH}	$\overline{CS1}$ Hold Time	200	—	µs
t_{DPD}	$\overline{CS1}$ Pulse Width (Deep Power Down)	10	—	ms

AC Notes:

1. Guarantee minimum 10ns of data valid time under any specific operating condition.
2. After power-up, an initial pause of 200 us with CS2 high is required with the output open condition.
3. Parameters tCHZ, tOHZ, tBHZ and TWHZ define the time at which the output goes the into the open condition and are not output voltage reference levels.
4. During write cycles, input data is latched on the earliest of $\overline{WE}$, $\overline{LB/UB}$, or $\overline{CS1}$ rising edge. Therefore, input data must be valid during the set-up time (tDSC, tDSB or tDSW) and hold time (tDHC, tDHB or tDHW).
5. Address (A2 to A20) inputs are latched on the falling edge of $\overline{OE}$ or $\overline{WE}$. Address (A2 to A20) input must be valid during the set-up time (tASO or tASW) and hold time (tAHO or tAHW).
6. Data can not be retained at deep power-down stand-by mode.
7. If $\overline{OE}$ is high during the write cycle, the outputs will remain at high impedance.
8. During the output state of I/O signals, input signals of reverse polarity must not be applied.
9. $t_{rising} = t_{falling} = 5ns$ for inputs.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	V_{DD}-0.2V to V_{DD}+0.2V
Input Rise and Fall Time	5 ns
Input and Output Timing and Reference Level	V_{REF}
Output Load	See Figures 1 and 2 (1)

Note 1. All AC test to output Load Figure 1, except High-Z use output load Figure 2.

	2.2V to 3.6V
R1(Ω)	3070
R2(Ω)	3150
V_{REF}	1.5V
V_{TM}	2.8V

AC TEST LOADS

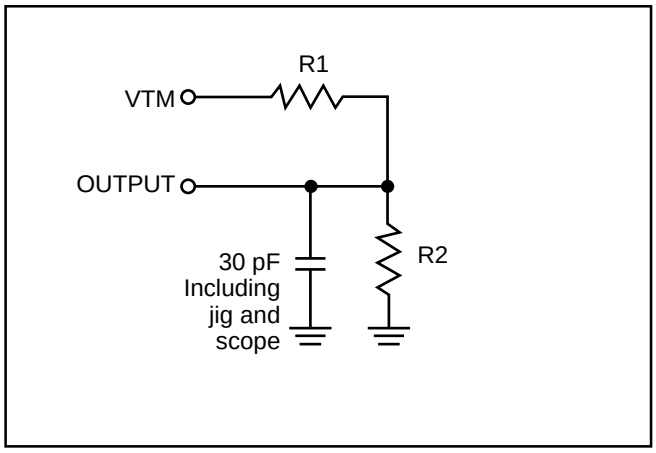


Figure 1

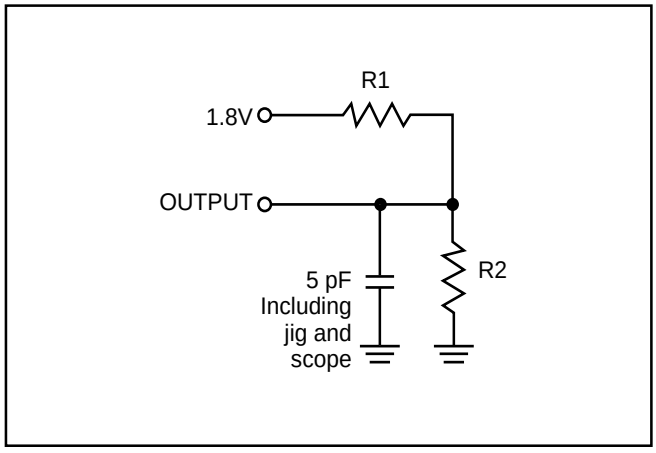
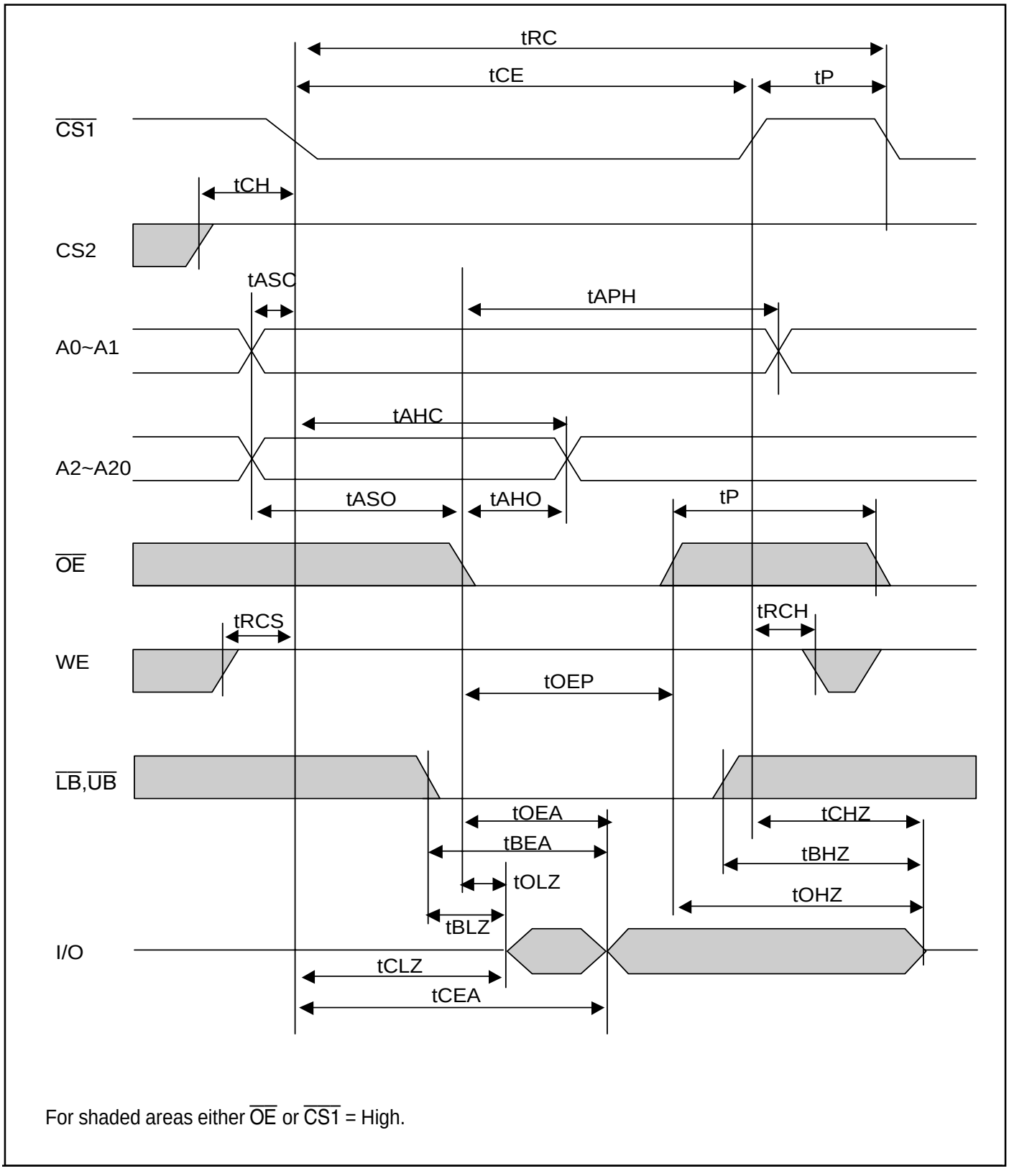


Figure 2

AC WAVEFORMS

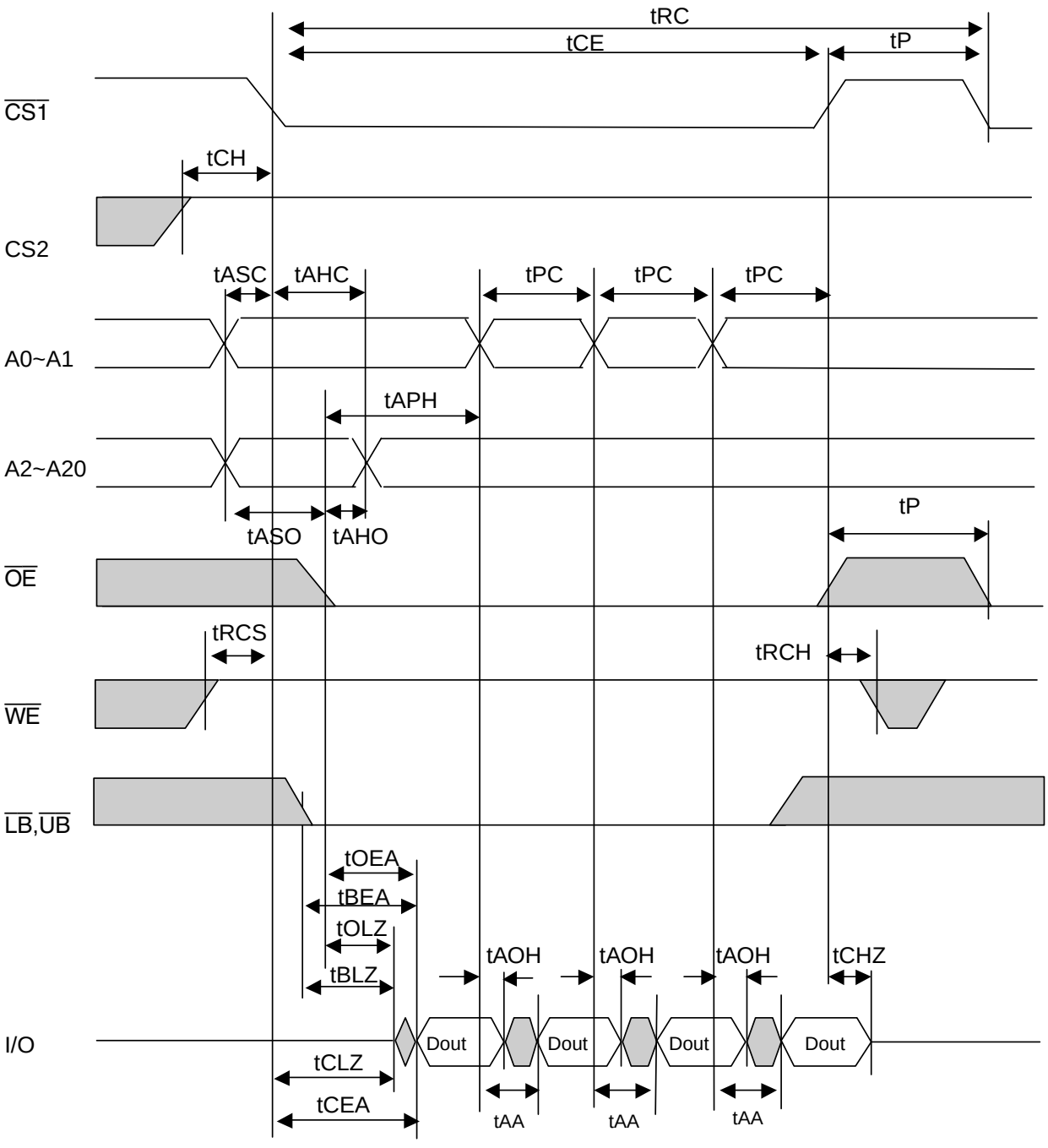
Read Timing



For shaded areas either $\overline{OE}$ or $\overline{CS1}$ = High.

AC WAVEFORMS

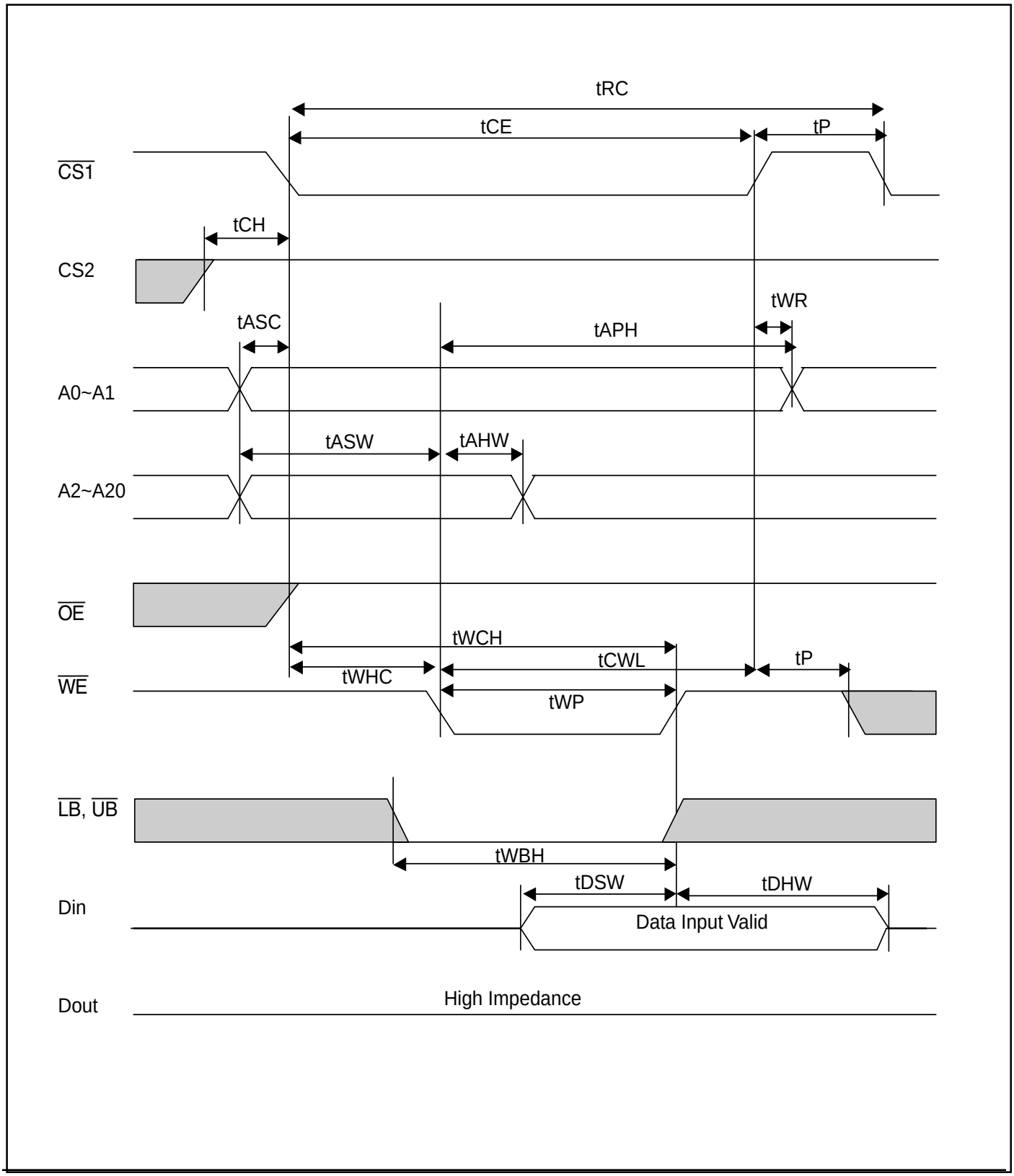
Page Read timing (four word access)



For shaded areas either $\overline{OE}$ or $\overline{CS1}$ = High.

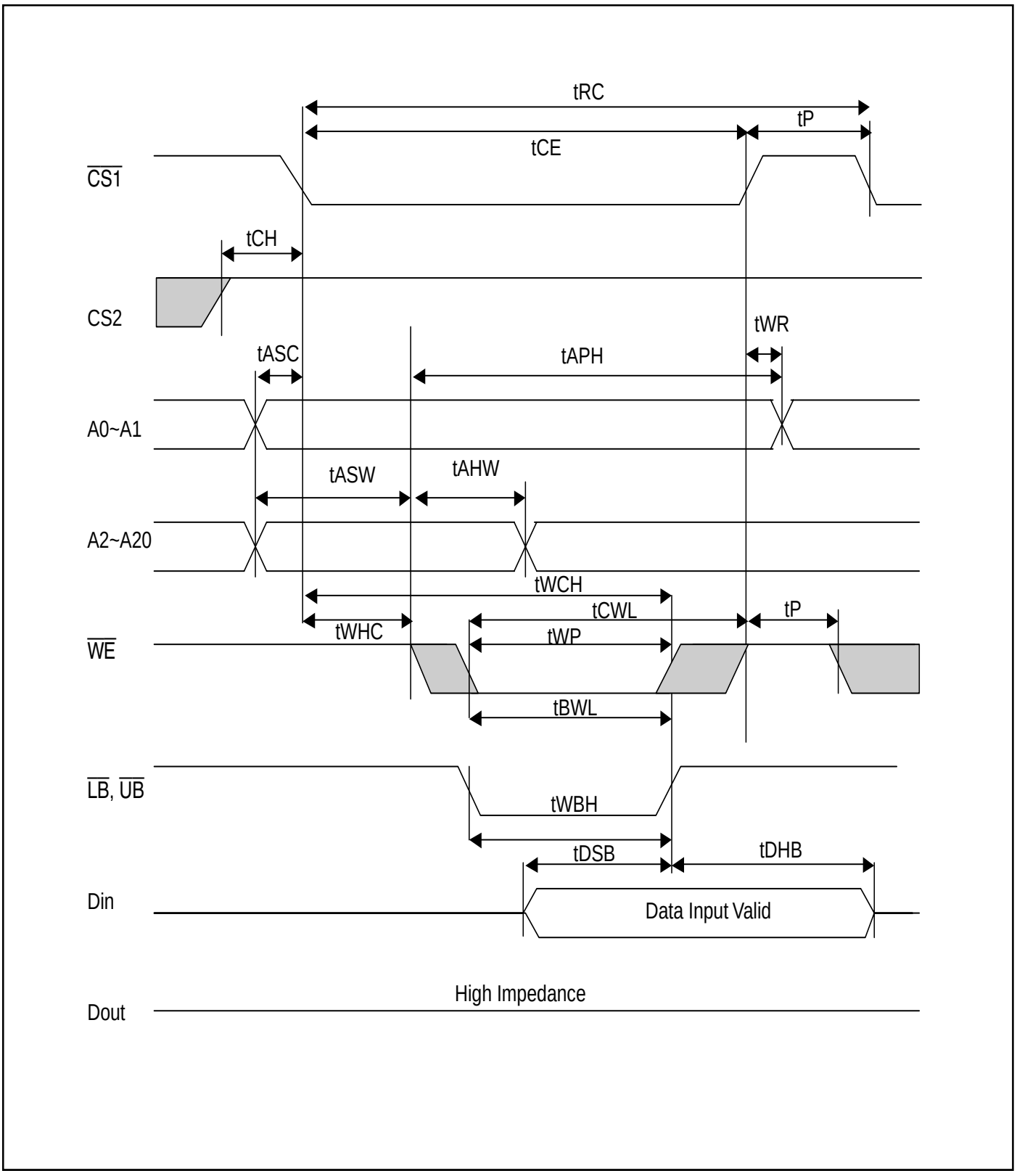
AC WAVEFORMS

Write Timing ($\overline{WE}$ Control Write)



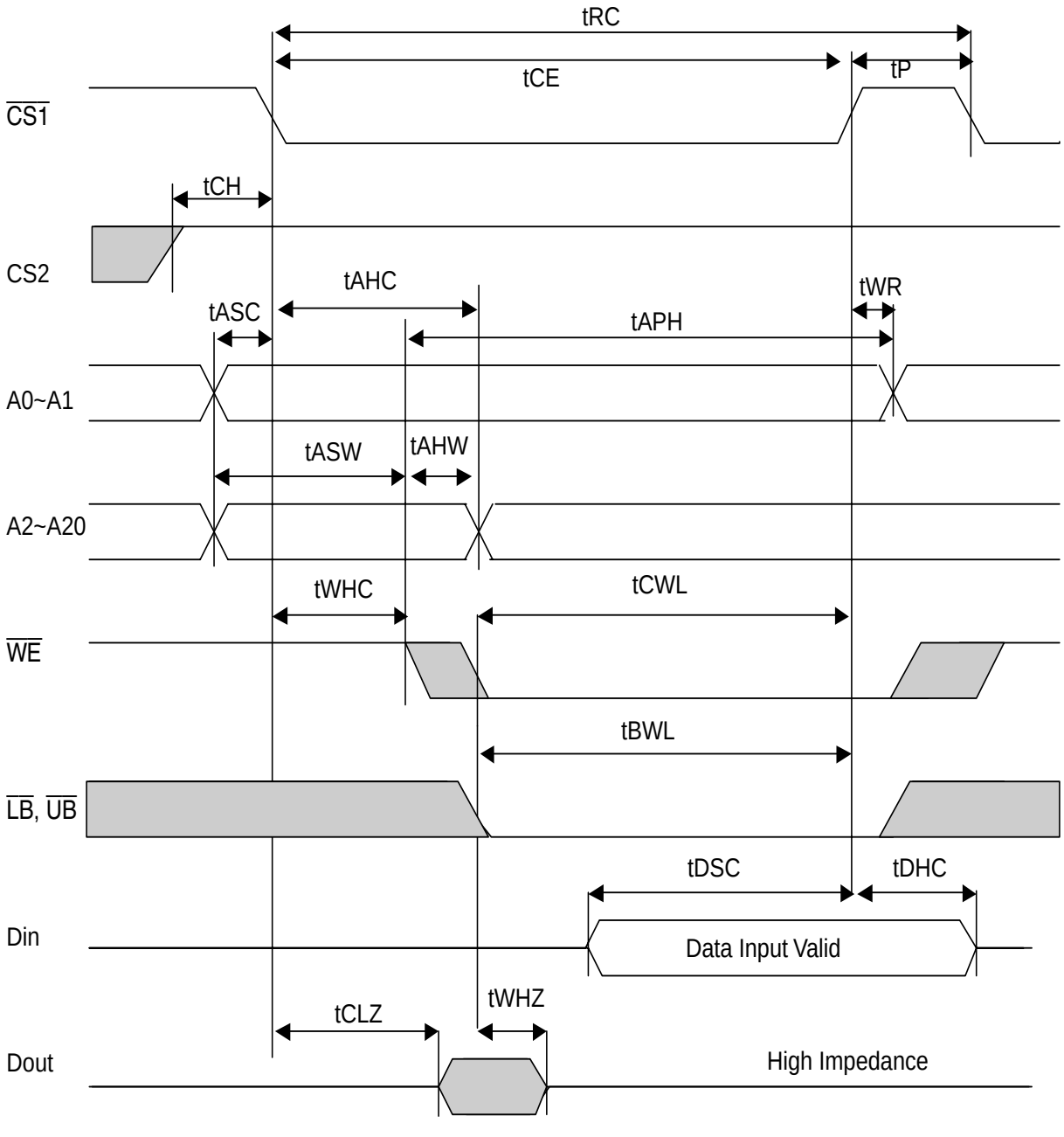
AC Wave Forms

Write Timing ($\overline{LB}$/$\overline{UB}$ Control Write)



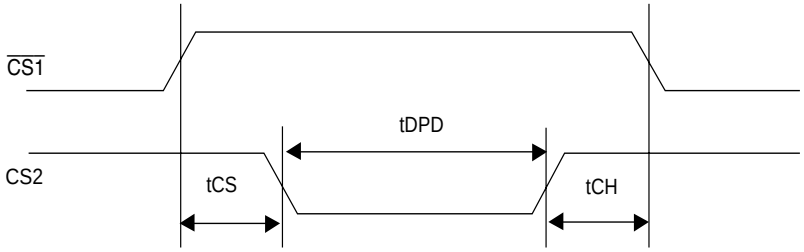
AC Wave Forms

Write Timing ($\overline{CS1}$ Control Write)



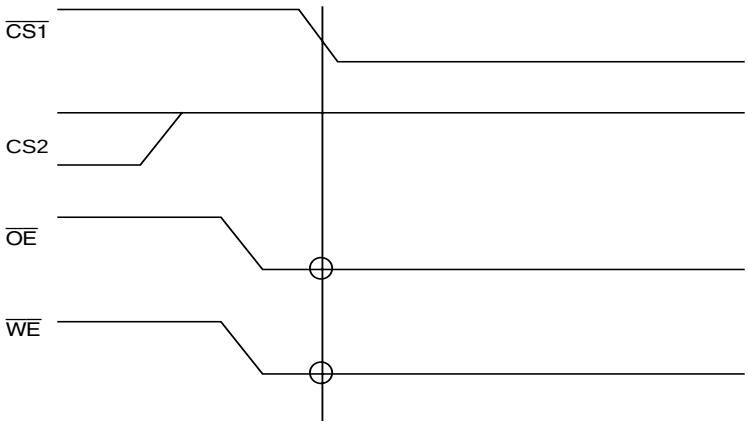
$\overline{OE}$ = High.

Deep Power-Down Timing



Note: During deep power-down stand-by mode, data can not be retained.

Prohibition Timing (Timing shown is prohibited.)



Note: A malfunction may occur, since devices go into test modes for internal use, if both $\overline{OE}$ and $\overline{WE}$ go Low coincident with or before falling edge of $\overline{CS1}$.

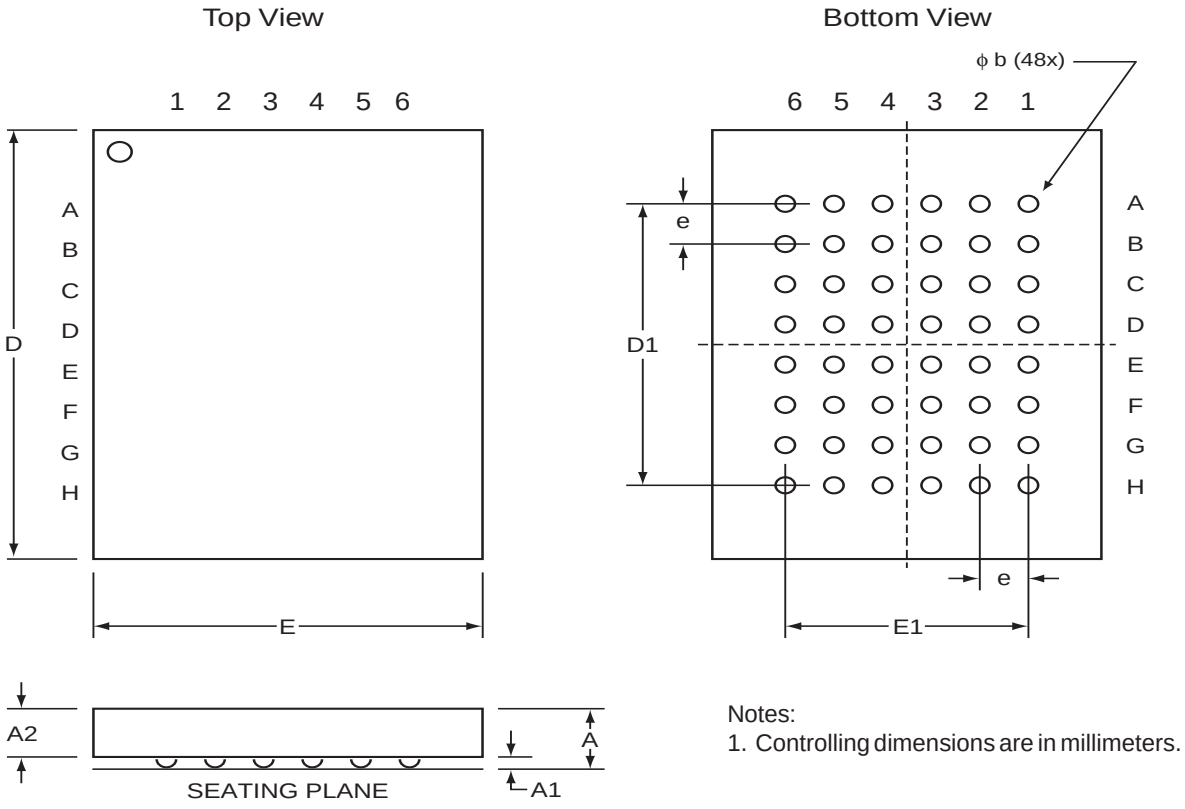
ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS32WV204816B-70MI	Mini BGA (6mm x 8mm) (0.8 mm Pitch)
	IS32WV204816B-70BI	Mini BGA (6mm x 8mm) (0.75 mm Pitch)

PACKAGING INFORMATION

Mini Ball Grid Array
Package Code: B (48-pin)



Notes:
1. Controlling dimensions are in millimeters.

mBGA - 6mm x 8mm

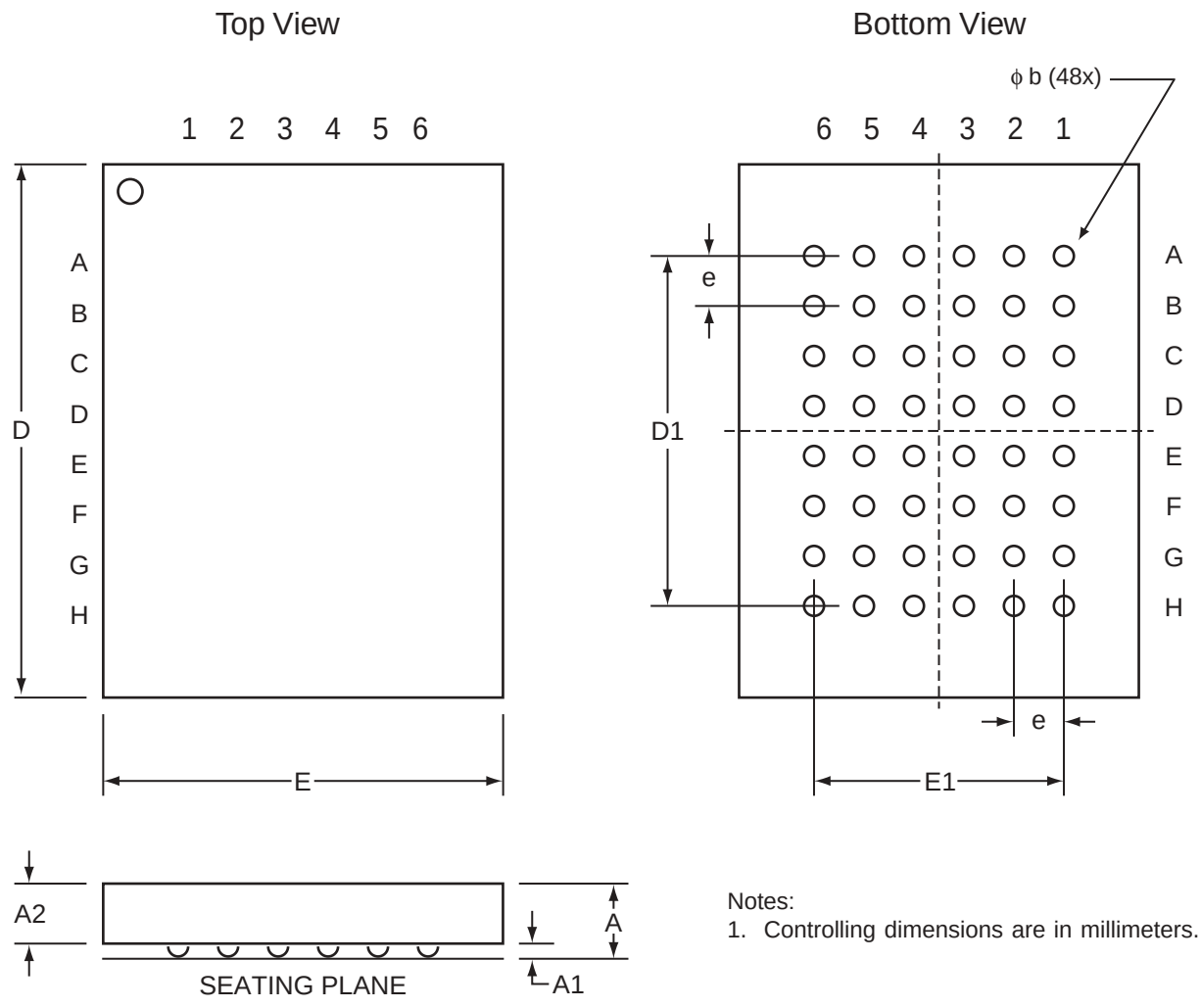
	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**48**				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	7.90	—	8.10	0.311	—	0.319
D1		5.25 BSC			0.207 BSC	
E	5.90	—	6.10	0.232	—	0.240
E1		3.75 BSC			0.148 BSC	
e		0.75 BSC			0.030 BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

mBGA - 8mm x 10mm

	MILLIMETER			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**48**				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	9.90	—	10.10	0.390	—	0.398
D1		5.25 BSC			0.207 BSC	
E	7.90	—	8.10	0.311	—	0.319
E1		3.75 BSC			0.148 BSC	
e		0.75 BSC			0.030 BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

PACKAGING INFORMATION

Mini Ball Grid Array
Package Code: M (48-pin)



Notes:
1. Controlling dimensions are in millimeters.

Mini Ball Grid Array
Package Code: M (48-pin)

mBGA - 6mm x 8mm

	MILLIMETERS			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
N0. Leads		48				
A	—	—	1.20	.—	—	0.047
A1	0.25	—	0.40	0.010	—	0.016
A2	0.60	—	—	0.024	—	—
D	7.90	8.00	8.10	0.311	0.314	0.319
D1		5.60BSC			0.220BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		4.00BSC			0.157BSC	
e		0.80BSC			0.031BSC	
b	0.40	0.45	0.50	0.016	0.018	0.020

mBGA - 7.2mm x 8.7mm

	MILLIMETERS			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
N0. Leads		48				
A	—	—	1.20	—	—	0.047
A1	0 .24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	8.60	8.70	8.80	0.339	0.343	0.346
D1		5.25BSC			0.207BSC	
E	7.10	7.20	7.30	0.280	0.283	0.287
E1		3.75BSC			0.148BSC	
e		0.75BSC			0.030BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

mBGA - 9mm x 11mm

	MILLIMETERS			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
N0. Leads		48				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	10.90	11.00	11.10	0.429	0.433	0.437
D1		5.25BSC			0.207BSC	
E	8.90	9.00	9.10	0.350	0.354	0.358
E1		3.75BSC			0.148BSC	
e		0.75BSC			0.030BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016