National Semiconductor

July 2004

ADC081000
High Performance, Low Power 8-Bit, 1 GSPS A/D Converter

General Description

The ADC081000 is a low power, high performance CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 1.6 GSPS. Consuming a typical 1.4 Watts at 1 GSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist, producing a high 7.5 ENOB with a 500 MHz input signal and a 1 GHz sample rate. Output formatting is offset binary and the LVDS digital outputs are compliant with IEEE 1596.3-1996, with the exception of a reduced common mode voltage of 0.8V.

The converter has a 1:2 demultiplexer that feeds two LVDS buses, reducing the output data rate on each bus to half the sampling rate. The data on these buses are interleaved in time to provide a 500 MHz output rate per bus and a combined output rate of 1 GSPS.

The converter typically consumes less than 10 mW in the Power Down Mode and is available in a 128-lead, thermally enhanced exposed pad LQFP and operates over the industrial ($-40^{\circ}C \le T_A \le +85^{\circ}C$) temperature range.

Features

- Internal Sample-and-Hold
- Single +1.9V ±0.1V Operation
- Adjustable Output Levels
- Guaranteed No Missing Codes
- Low Power Standby Mode

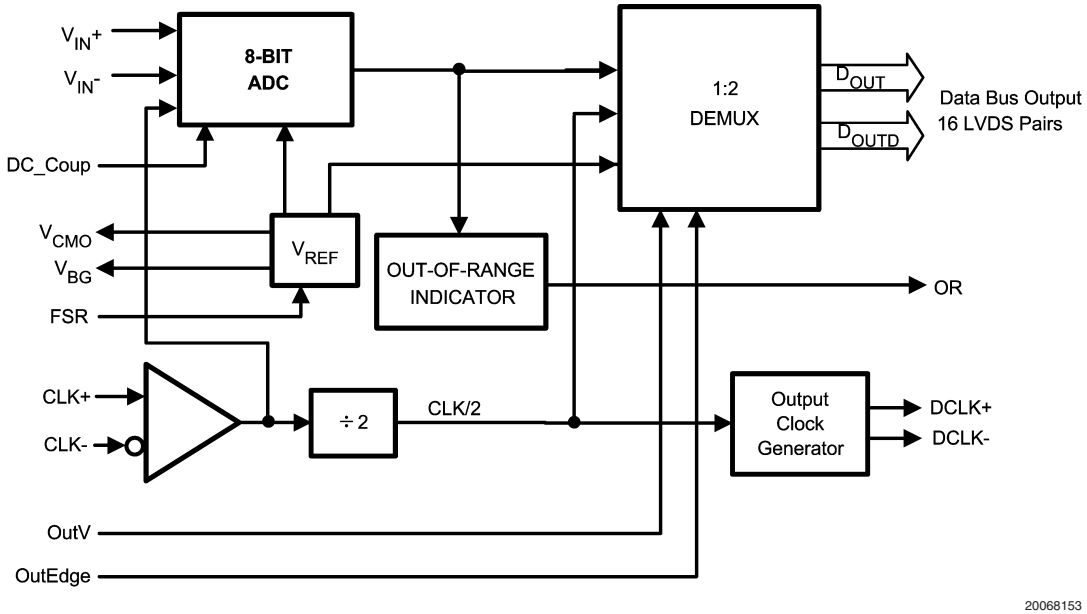
Key Specifications

■ Resolution	8 Bits
■ Max Conversion Rate	1 GSPS (min)
■ ENOB @ 500 MHz Input	7.5 Bits (typ)
■ DNL	±0.25 LSB (typ)
■ Conversion Latency	7 and 8 Clock Cycles
■ Power Consumption	
— Operating	1.45 W (typ)
— Power Down Mode	9 mW (typ)

Applications

- Direct RF Down Conversion
- Digital Oscilloscopes
- Satellite Set-top boxes
- Communications Systems
- Test Instrumentation

Block Diagram



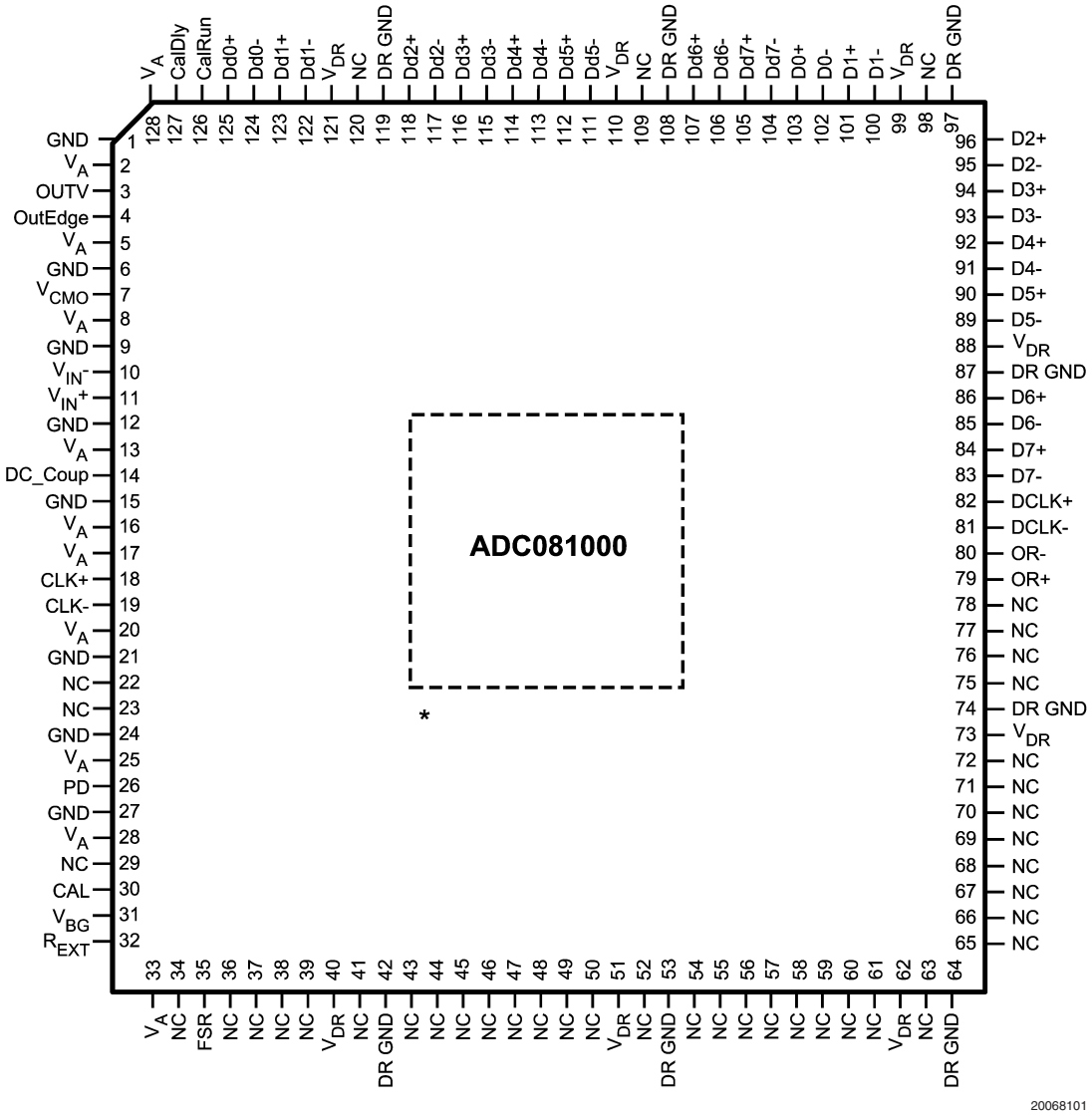
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Ordering Information

Extended Commercial Temperature Range (-40˚C < T_A < +85˚C)	NS Package
ADC081000CIYB	128-Pin Exposed Pad LQFP
ADC081000LEVAL	Evaluation Board

Pin Configuration

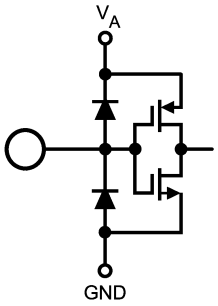
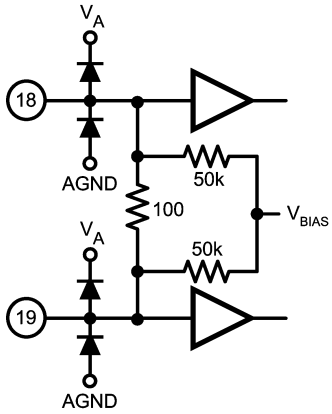
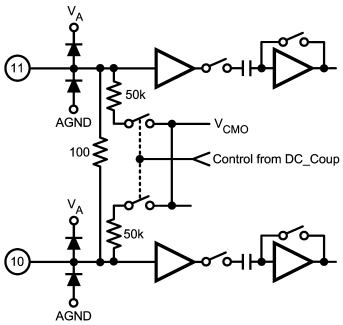


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* Exposed pad on back of package must be soldered to ground plane to ensure rated performance.

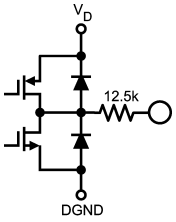
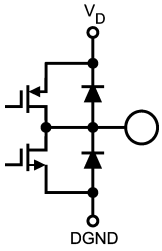
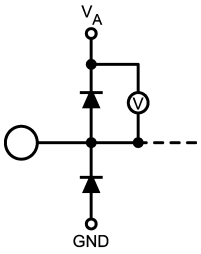
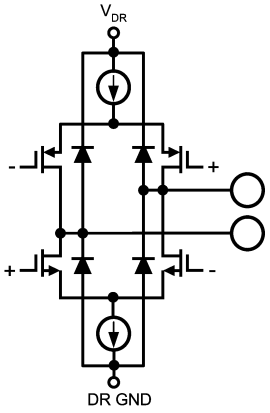
Pin Descriptions and Equivalent Circuits

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
3	OutV		Output Voltage Amplitude set. Tie this pin high for normal differential output amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. See Section 1.5.
4	OutEdge		Output Edge Select. Sets the edge of the DCLK+ (pin 82) at which the output data transitions. The output transitions with the DCLK+ rising edge when this pin is high or on the falling edge when this pin is low. See Section 5.3.
14	DC_Coup		DC Coupling select. When this pin is high, the V_{IN}+ and V_{IN}- analog inputs are d.c. coupled and the input common mode voltage should equal the V_{CMO} (pin 7) output voltage. When this pin is low, the analog input pins are internally biased and the input signal should be a.c. coupled to the analog input pins. See Section 3.0.
26	PD		Power Down Pin. A logic high on this pin puts the ADC into the Power Down mode. A logic low on this pin allows normal operation.
30	CAL		Calibration. A minimum 10 clock cycles low followed by a minimum of 10 clock cycles high on this pin will initiate the self calibration sequence. See Section 1.1.
35	FSR		Full scale Range Select. With a logic low on this pin, the full-scale differential input is 600 mV_{P-P}. With a logic high on this pin, the full-scale differential input is 800 mV_{P-P}. See Section 1.3.
127	CalDly		Calibration Delay. This sets the number of clock cycles after power up before calibration begins. See Section 1.1.
18 19	CLK+ CLK-		Clock input pins for the ADC. The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on the falling edge of CLK+.
11 10	V_{IN}+ V_{IN}-		Analog Signal Differential Inputs to the ADC.

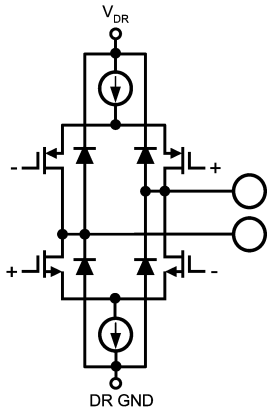
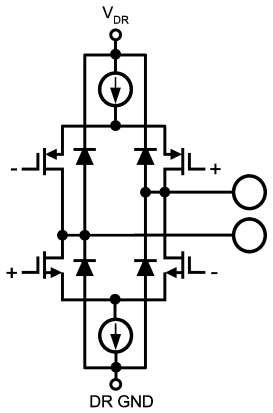
Pin Descriptions and Equivalent Circuits (Continued)

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
7	V_{CMO}		Common Mode Output voltage for V_{IN}+ and V_{IN}- when d.c. input coupling is used. See Section 3.0.
31	V_{BG}		Bandgap output voltage. This pin is capable of sourcing or sinking up to 100 µA.
126	CalRun		Calibration Running indication. This pin is at a logic high when calibration is running.
32	R_{EXT}		External Bias Resistor connection. The required value is 3.3k-Ohms (±0.1%) to ground. See Section 1.1.
83 D7- 84 D7+ 85 D6- 86 D6+ 89 D5- 90 D5+ 91 D4- 92 D4+ 93 D3- 94 D3+ 95 D2- 96 D2+ 100 D1- 101 D1+ 102 D0- 103 D0+			LVDS data output bits sampled second in time sequence. These outputs should always be terminated with a differential 100Ω resistance.

Pin Descriptions and Equivalent Circuits (Continued)

Pin Functions

Pin No.	Symbol	Equivalent Circuit	Description
104 105 106 107 111 112 113 114 115 116 117 118 122 123 124 125	Dd7- Dd7+ Dd6- Dd6+ Dd5- Dd5+ Dd4- Dd4+ Dd3- Dd3+ Dd2- Dd2+ Dd1- Dd1+ Dd0- Dd0+		LVDS data output bits sampled first in time sequence. These outputs should always be terminated with a differential 100Ω resistance.
79 80	OR+ OR-		Out of Range output. A differential high at these pins indicates that the differential input is out of range (outside the range of ±300 mV or ±400 mV as defined by the FSR pin). See Section 1.6.
82 81	DCLK+ DCLK-		Differential Clock Outputs used to latch the output data. Delayed and non-delayed data outputs are supplied synchronous to this signal.
2, 5, 8, 13, 16, 17, 20, 25, 28, 33, 128	V_A		Analog power supply pins. Bypass these pins to GND.
40, 51, 62, 73, 88, 99, 110, 121	V_{DR}		Output Driver power supply pins. Bypass these pins to DR GND.
1, 6, 9, 12, 15, 21, 24, 27	GND		Ground return for V_A
42, 53, 64, 74, 87, 97, 108, 119	DR GND		Ground return for V_{DR}
22, 23, 29, 34, 36 - 39, 41, 43 - 50, 52, 54 - 61, 63, 65 - 72, 75 - 78, 98, 109, 120	NC		No Connection. Make no connection to these pins.

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_{DR})	2.2V
Voltage on Any Input Pin	–0.15V to (V_A +0.15V)
Ground Difference |GND - DR GND|	0V to 100 mV
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Power Dissipation at T_A = 25˚C	2.0 W
ESD Susceptibility (Note 4)	
Human Body Model	2500V
Machine Model	250V
Soldering Temperature, Infrared, 10 seconds (Note 5)	235˚C
Storage Temperature	–65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Ambient Temperature Range	–40˚C ≤ T_A ≤ +85˚C
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Analog Input Common Mode Voltage	1.2V to 1.3V
V_{IN} Differential Voltage Range	$-V_{FS}/2$ to $+V_{FS}/2$
Ground Difference |GND - DR GND|	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	$0.6V_{P-P}$ to $2.0V_{P-P}$

Package Thermal Resistances

Package	θ_{J-C} (Top of Package)	θ_{J-PAD} (Thermal Pad)
128-Lead Exposed Pad LQFP	10˚C / W	2.8˚C / W

Converter Electrical Characteristics

The following specifications apply after calibration for V_A = V_{DR} = +1.9V_{DC}, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential 800mV_{P-P}, C_L = 10 pF, Differential, a.c. coupled Sinewave Clock, f_{CLK} = 1 GHz at 0.5V_{P-P} with 50% duty cycle, R_{EXT} = 3300Ω ± 0.1%, Analog Signal Source Impedance = 100Ω. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**. All other limits T_A = 25˚C, unless otherwise stated. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity		±0.35	**±0.9**	LSB (max)
DNL	Differential Non-Linearity		±0.25	**±0.7**	LSB (max)
	Resolution with No Missing Codes			**8**	Bits
V_{OFF}	Offset Error		–0.45	**–1.5** **0.5**	LSB (min) LSB (max)
TC V_{OFF}	Offset Error Tempco	–40˚C to +85˚C	–3		ppm/˚C
PFSE	Positive Full-Scale Error (Note 9)		–2.2	**±25**	mV (max)
NFSE	Negative Full-Scale Error (Note 9)		–1.1	**±25**	mV (max)
TC PFSE	Positive Full Scale Error Tempco	–40˚C to +85˚C	20		ppm/˚C
TC NFSE	Negative Full Scale Error Tempco	–40˚C to +85˚C	13		ppm/˚C
Dynamic Converter Characteristics					
FPBW	Full Power Bandwidth		1.7		GHz
	Gain Flatness	d.c. to 500 MHz	±0.5		dBFS
		d.c. to 1 GHz	±1.0		dBFS
ENOB	Effective Number of Bits	f_{IN} = 100 MHz, V_{IN} = FSR – 0.5 dB	7.5		Bits
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	7.5	**7.1**	Bits (min)
		f_{IN} = 498 MHz, V_{IN} = FSR – 0.5 dB	7.5	**7.1**	Bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 MHz, V_{IN} = FSR – 0.5 dB	47		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	47	**44.8**	dB (min)
		f_{IN} = 498 MHz, V_{IN} = FSR – 0.5 dB	47	**44.8**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 MHz, V_{IN} = FSR – 0.5 dB	48		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	48	**45.5**	dB (min)
		f_{IN} = 498 MHz, V_{IN} = FSR – 0.5 dB	48	**45.5**	dB (min)

Converter Electrical Characteristics (Continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $800mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Clock, f_{CLK} = 1 GHz at $0.5V_{P-P}$ with 50% duty cycle, $R_{EXT} = 3300\Omega \pm 0.1\%$, Analog Signal Source Impedance = 100Ω. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits T_A = 25˚C, unless otherwise stated. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
THD	Total Harmonic Distortion	f_{IN} = 100 MHz, V_{IN} = FSR – 0.5 dB	-57		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	-57	**–50**	dB (max)
		f_{IN} = 498 MHz, V_{IN} = FSR – 0.5 dB	-57	**–50**	dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 100 MHz, V_{IN} = FSR – 0.5 dB	–64		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	–64		dB
		f_{IN} = 498 MHz, V_{IN} = FSR – 0.5 dB	–64		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 100 MHz, V_{IN} = FSR – 0.5 dB	–64		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	–64		dB
		f_{IN} = 498 MHz, V_{IN} = FSR – 0.5 dB	–64		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 100 MHz, V_{IN} = FSR – 0.5 dB	58.5		dB
		f_{IN} = 248 MHz, V_{IN} = FSR – 0.5 dB	58.5	**50**	dB (min)
		f_{IN} = 498 MHz, V_{IN} = FSR – 0.5 dB	58.5	**50**	dB (min)
IMD	Intermodulation Distortion	f_{IN1} = 121 MHz, V_{IN} = FSR – 7 dB f_{IN2} = 126 MHz, V_{IN} = FSR – 7 dB	-51		dB
	Out of Range Output Code (In addition to OR Output high)	$(V_{IN}+) - (V_{IN}-) >$ + Full Scale		**255**	
		$(V_{IN}+) - (V_{IN}-) <$ – Full Scale		**0**	
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Full Scale Analog Differential Input Range	FSR pin Low	600	**550**	mV_{P-P} (min)
				650	mV_{P-P} (max)
		FSR pin High	800	**750**	mV_{P-P} (min)
				850	mV_{P-P} (max)
V_{CMI}	Common Mode Analog Input Voltage		V_{CMO}	**V_{CMO} – 50** **V_{CMO}+ 50**	mV (min) mV (max)
C_{IN}	Analog Input Capacitance (Note 10)	Differential	0.02		pF
		Each input to ground	1.6		pF
R_{IN}	Differential Input Resistance		100	**94**	Ω (min)
				106	Ω (max)
ANALOG OUTPUT CHARACTERISTICS					
V_{CMO}	Common Mode Output Voltage	I_{CMO} = ±1 µA	1.21	**0.95** **1.45**	V (min) V (max)
TC V_{CMO}	Common Mode Output Voltage Temperature Coefficient	T_A = –40˚C to +85˚C	118		ppm/˚C
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.26	**1.22** **1.33**	V (min) V (max)
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = –40˚C to +85˚C, I_{BG} = ±100 µA	-28		ppm/˚C
CLOCK INPUT CHARACTERISTICS					
V_{ID}	Differential Clock Input Level	Square Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
		Sine Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
I_I	Input Current	V_{IN} = 0V or $V_{IN} = V_A$	±1		µA
C_{IN}	Input Capacitance (Note 10)	Differential	0.02		pF
		Each Input to Ground	1.5		pF

Converter Electrical Characteristics (Continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $800mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Clock, f_{CLK} = 1 GHz at $0.5V_{P-P}$ with 50% duty cycle, $R_{EXT} = 3300\Omega$ ± 0.1%, Analog Signal Source Impedance = 100Ω. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits T_A = 25˚C, unless otherwise stated. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
DIGITAL CONTROL PIN CHARACTERISTICS					
V_{IH}	Logic High Input Voltage	(Note 12)		**1.4**	V (min)
V_{IL}	Logic Low Input Voltage	(Note 12)		**0.5**	V (max)
I_I	Input Current	V_{IN} = 0 or $V_{IN} = V_A$	±1		µA
C_{IN}	Logic Input Capacitance (Note 13)	Each input to ground	1.2		pF
DIGITAL OUTPUT CHARACTERISTICS					
V_{OD}	LVDS Differential Output Voltage	OutV = V_A, measured single-ended	300	**200**	mV_{P-P} (min)
				450	mV_{P-P} (max)
		OutV = GND, measured single-ended	225	**140**	mV_{P-P} (min)
				340	mV_{P-P} (max)
ΔV_{OD} DIFF	Change in LVDS Output Swing Between Logic Levels		±1		mV
V_{OS}	Output Offset Voltage		800		mV
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±1		mV
I_{OS}	Output Short Circuit Current	Output+ & Output- connected to 0.8V	–4		mA
Z_O	Differential Output Impedance		100		Ohms
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = Low	646	**792**	mA (max)
		PD = High	4.5		mA
I_{DR}	Output Driver Supply Current	PD = Low	108	**160**	mA (max)
		PD = High	0.1		mA
P_D	Power Consumption	PD = Low	1.43	**1.8**	W (max)
		PD = High	8.7		mW
PSRR1	D.C. Power Supply Rejection Ratio	Change in Offset Error with change in V_A from 1.8V to 2.0V	73		dB
AC ELECTRICAL CHARACTERISTICS					
f_{CLK1}	Maximum Conversion Rate	T_A = 85˚C	1.1	**1.0**	GHz (min)
		$T_A \leq$ 75˚C	1.3		GHz
		$T_A \leq$ 70˚C	1.6		GHz
f_{CLK2}	Minimum Conversion Rate		200		MHz
	Input Clock Duty Cycle	200 MHz ≤ Input clock frequency < 1 GHz	50	20	% (min)
				80	% (max)
t_{CL}	Input Clock Low Time (Note 12)		500	**200**	ps (min)
t_{CH}	Input Clock High Time (Note 12)		500	**200**	ps (min)
	DCLK Duty Cycle (Note 12)		50	**45**	% (min)
				55	% (max)
t_{LHT}	Differential Low to High Transition Time	10% to 90%, C_L = 2.5 pF	250		ps
t_{HLT}	Differential High to Low Transition Time	10% to 90%, C_L = 2.5 pF	250		ps
t_{OSK}	DCLK to Data Output Skew (Note 11)	50% of DCLK transition to 50% of Data transition	0	**±200**	ps (max)
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data	930		ps

Converter Electrical Characteristics (Continued)

The following specifications apply after calibration for $V_A = V_{DR} = +1.9V_{DC}$, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential $800mV_{P-P}$, C_L = 10 pF, Differential, a.c. coupled Sinewave Clock, f_{CLK} = 1 GHz at $0.5V_{P-P}$ with 50% duty cycle, $R_{EXT} = 3300\Omega \pm 0.1\%$, Analog Signal Source Impedance = 100Ω. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits T_A = 25˚C, unless otherwise stated. (Notes 6, 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 8)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS					
t_{AJ}	Aperture Jitter		0.4		ps rms
t_{OD}	Input Clock to Data Output Delay	50% of Input Clock transition to 50% of Data transition	2.7		ns
	Pipeline Delay (Latency) (Note 11)	"D" Outputs		**7**	Clock Cycles
		"Dd" Outputs		**8**	
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)		500		ns
t_{CAL}	Calibration Cycle Time		46,000		Clock Cycles

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

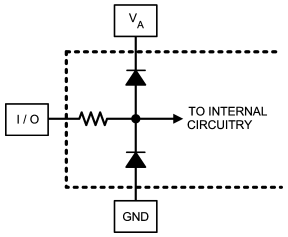
Note 2: All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power, ground and digital output pins.

Note 4: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Note 5: See AN-450, "Surface Mounting Methods and Their Effect on Product Reliability".

Note 6: The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



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Note 7: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.

Note 8: Typical figures are at T_J = 25˚C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See Transfer Characteristic *Figure 2*. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Note 10: The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.65 pF differential and 0.95 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 11: This parameter is guaranteed by design and is not tested in production.

Note 12: This parameter is guaranteed by design and characterization and is not tested in production.

Note 13: The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Note 14: The ADC081000 has two interleaved LVDS output buses, which each clock data out at one half the sample rate. The data at each bus is clocked out at one half the sample rate. The second bus (D0 through D7) has a pipeline latency that is one clock cycle less than the latency of the first bus (Dd0 through Dd7).

Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the fall of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode the aperture delay time (t_{AD}) after the clock goes low.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 1 GSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

- PGE = OE – PFSE
- NGE = –(OE – NFSE) = NFSE – OE
- Gain Error = NFSE – PFSE = PGE + NGE

where PGE is Positive Gain Error, NGE is Negative Gain Error, OE is Offset Error, PFSE is Positive Full-Scale Error and NFSE is Negative Full-Scale Error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. it is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^n$$

where V_{FS} is the differential full-scale amplitude of 600 mV or 800 mV as set by the FSR input and "n" is the ADC resolution in bits, which is 8 for the ADC081000.

LVDS DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) is this absolute value of the difference between the V_D+ and V_D– outputs, each measured with respect to Ground.

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the the D+ and D– pins' output voltages; i.e., [(VD+) + (VD–)] / 2.

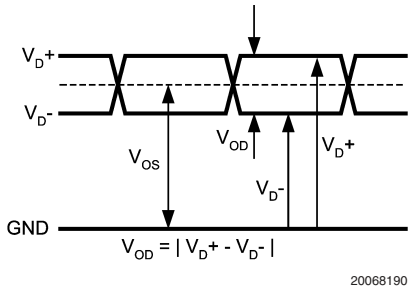


FIGURE 1.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR is a measure of how far the last code transition is from the ideal 1/2 LSB above a differential –800 mV with the FSR pin high, or 1/2 LSB above a differential –600 mV with the FSR pin low. For the ADC081000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

OUTPUT DELAY (t_{OD}) is the time delay after the falling edge of the DCLK before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential +800 mV with the FSR pin high, or 1-1/2 LSB below a differential +600 mV with the FSR pin low. For the ADC081000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in offset error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 50 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

Specification Definitions (Continued)

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

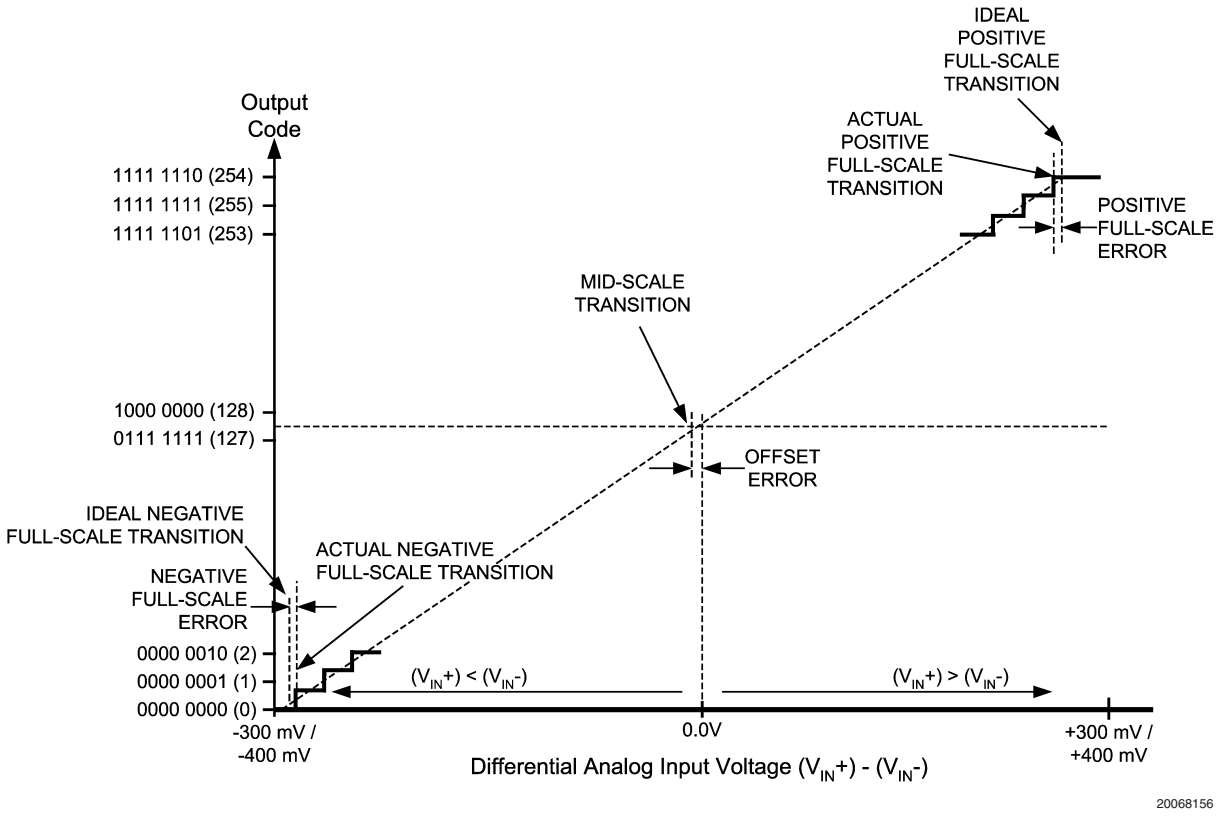


FIGURE 2. Input / Output Transfer Characteristic

Timing Diagrams

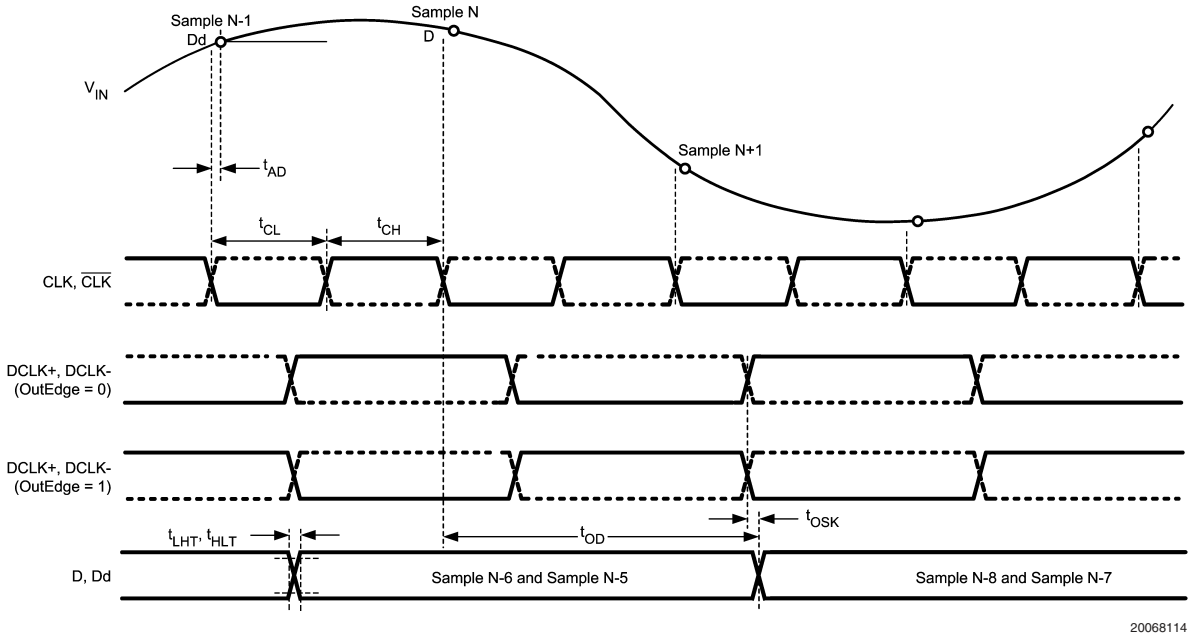
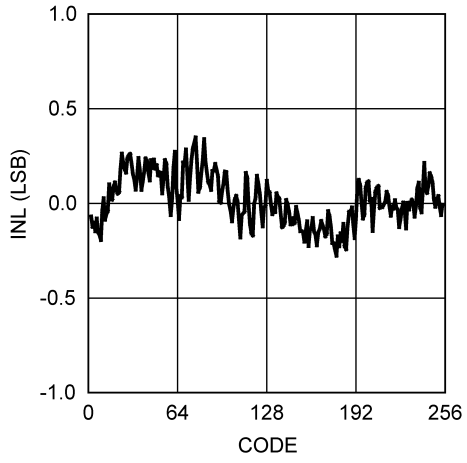


FIGURE 3. ADC081000 Timing

Typical Performance Characteristics

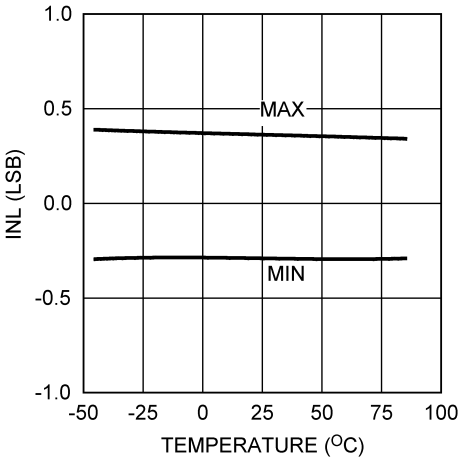
$V_A = V_{DR} = +1.9V$, $f_{CLK} = 1$ GHz (differential clock), $f_{IN} = 248$ MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature.

INL



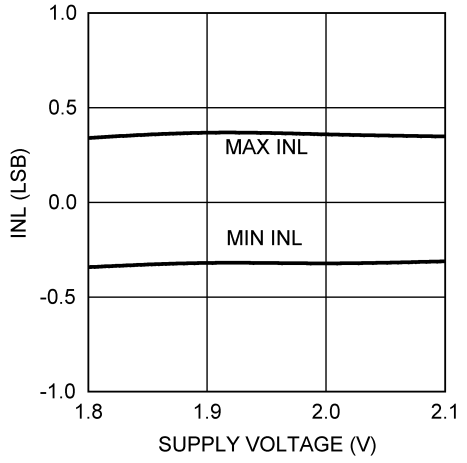
20068117

INL vs. Temperature



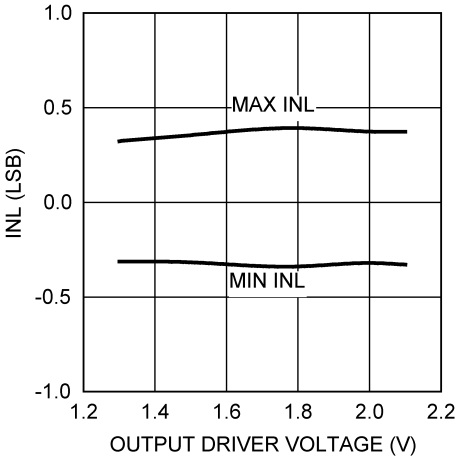
20068118

INL vs. Supply Voltage



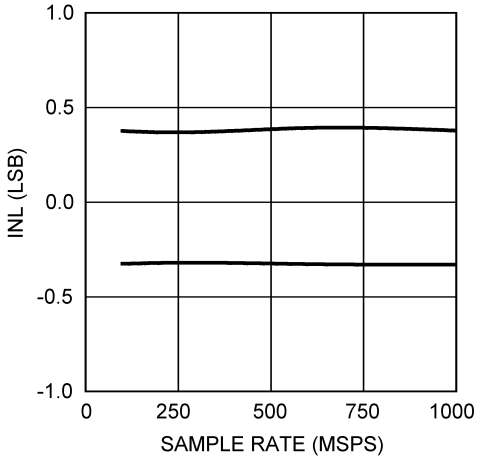
20068119

INL vs. Output Driver Voltage



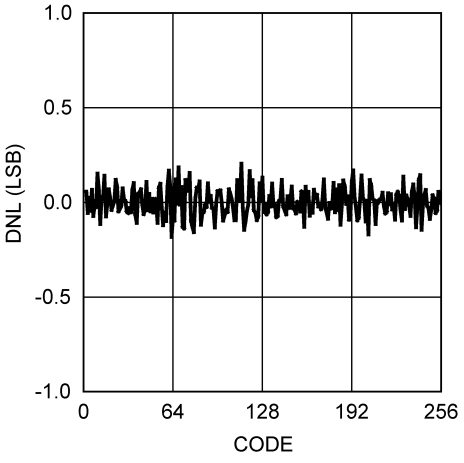
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INL vs. Sample Rate



20068121

DNL

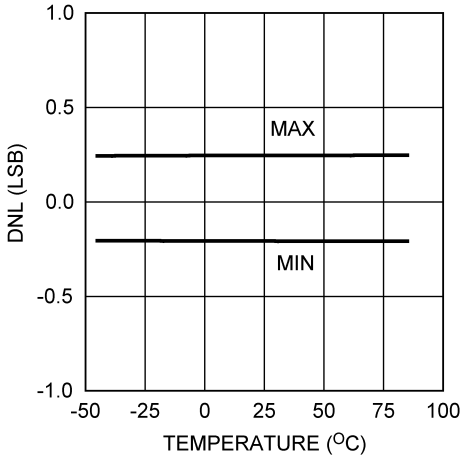


20068122

Typical Performance Characteristics

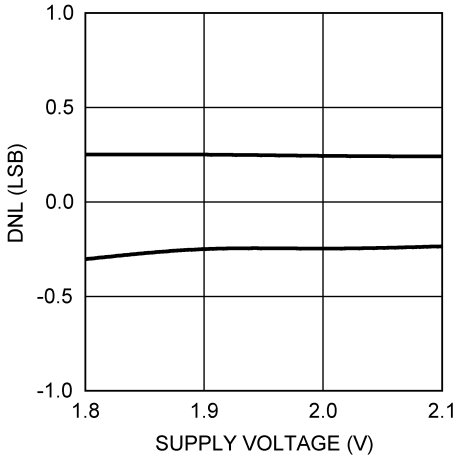
$V_A = V_{DR} = +1.9V$, $f_{CLK} = 1$ GHz (differential clock), $f_{IN} = 248$ MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

DNL vs. Temperature



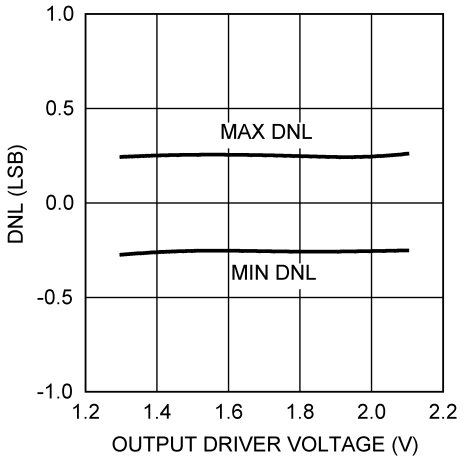
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DNL vs. Supply Voltage



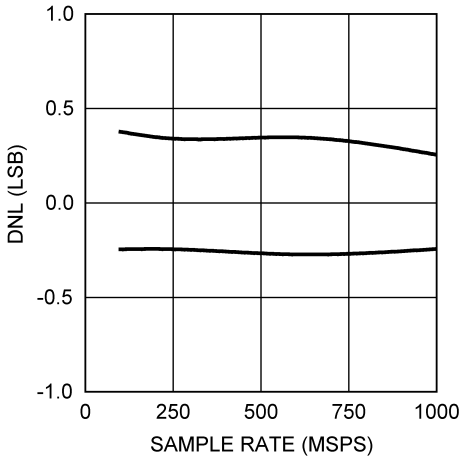
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DNL vs. Output Driver Voltage



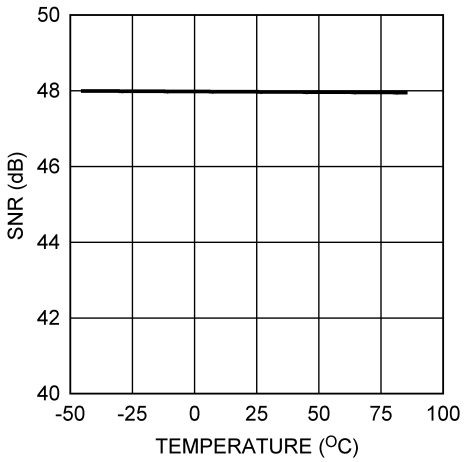
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DNL vs. Sample Rate



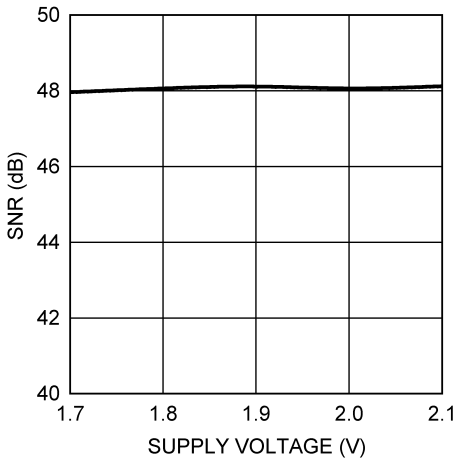
20068126

SNR vs. Temperature



20068127

SNR vs. Supply Voltage

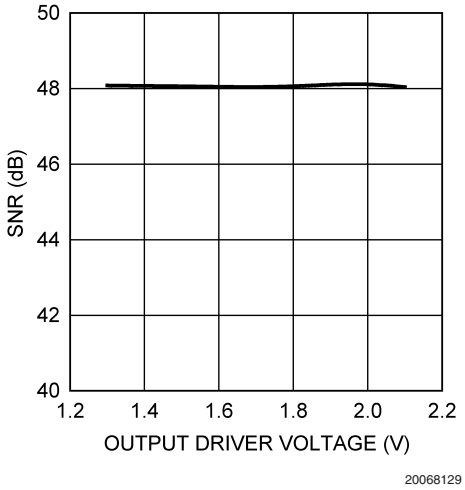


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Typical Performance Characteristics

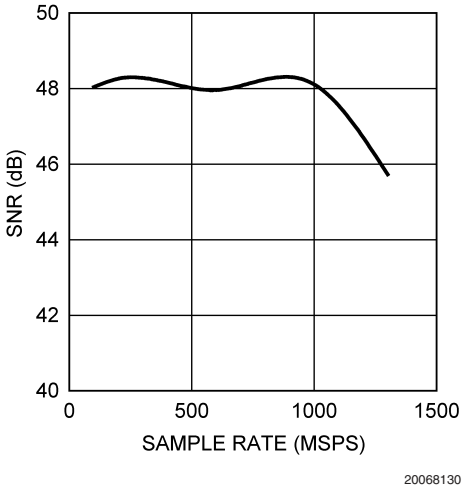
$V_A = V_{DR} = +1.9V$, $f_{CLK} = 1$ GHz (differential clock), $f_{IN} = 248$ MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

SNR vs. Output Driver Voltage



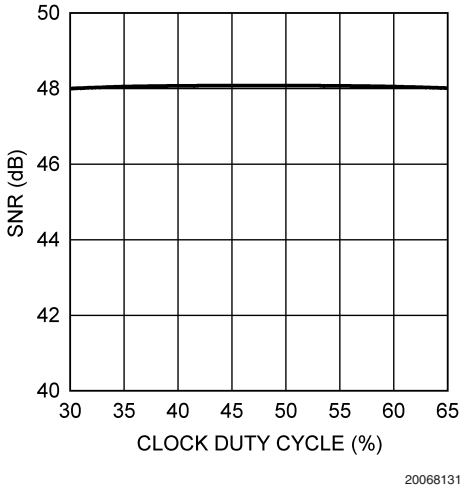
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SNR vs. Sample Rate



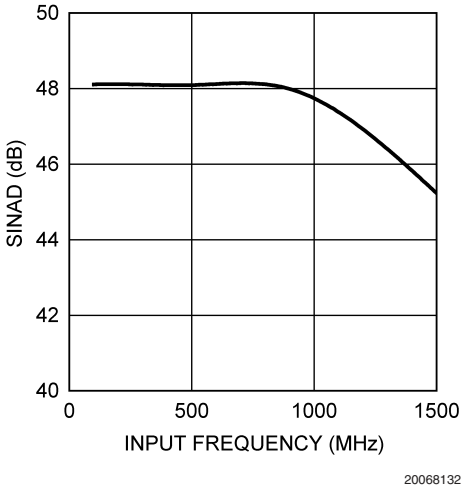
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SNR vs. Clock Duty Cycle



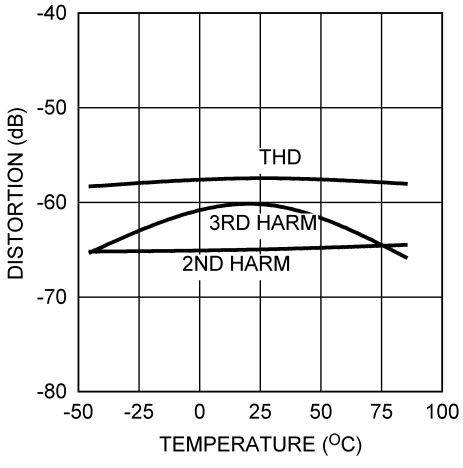
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SNR vs. Input Frequency



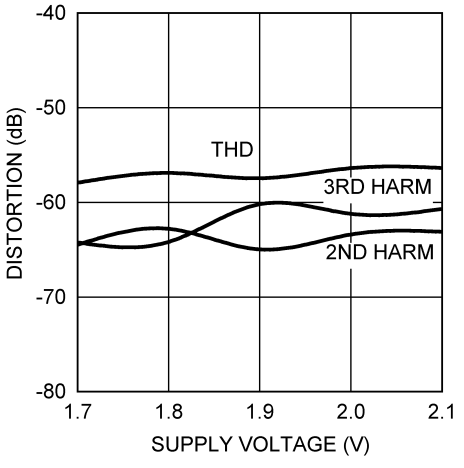
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Distortion vs. Temperature



20068133

Distortion vs. Supply Voltage

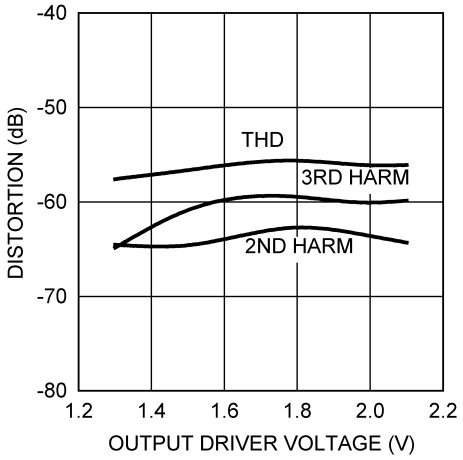


20068134

Typical Performance Characteristics

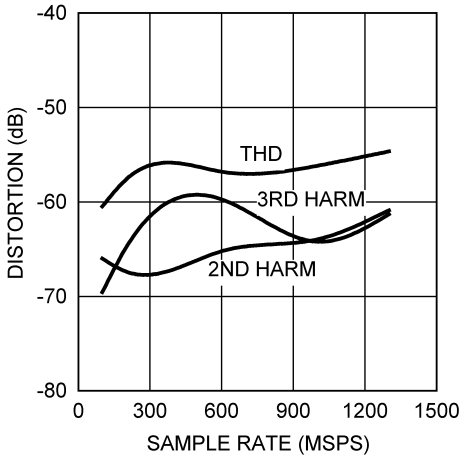
$V_A = V_{DR} = +1.9V$, f_{CLK} = 1 GHz (differential clock), f_{IN} = 248 MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

Distortion vs. Sample Rate



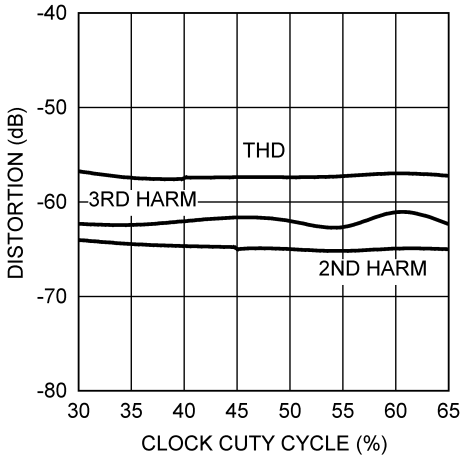
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Distortion vs. Sample Rate



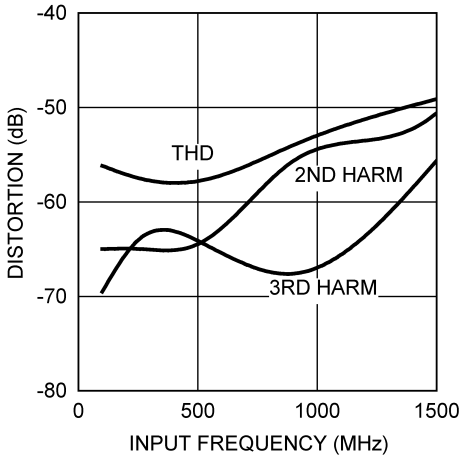
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Distortion vs. Clock Duty Cycle



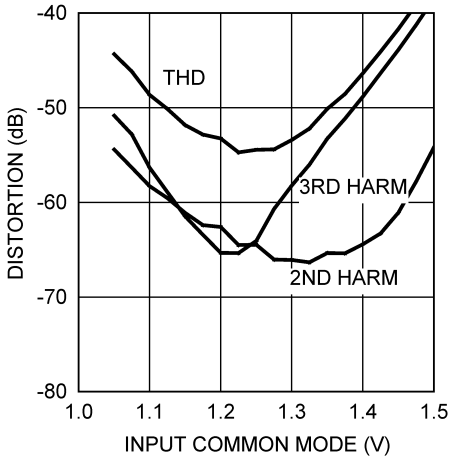
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Distortion vs. Input Frequency



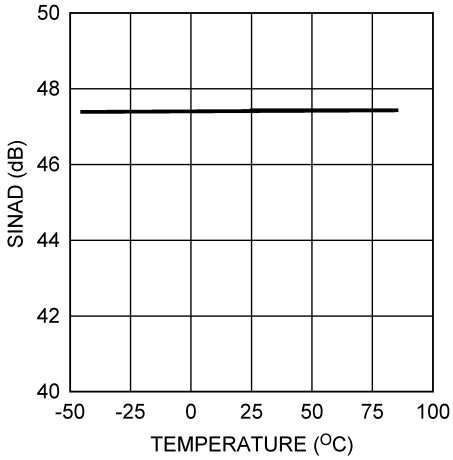
20068138

Distortion vs. Input Common Mode



20068181

SINAD vs. Temperature

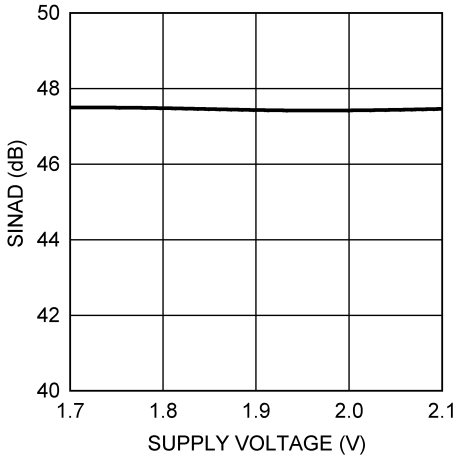


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Typical Performance Characteristics

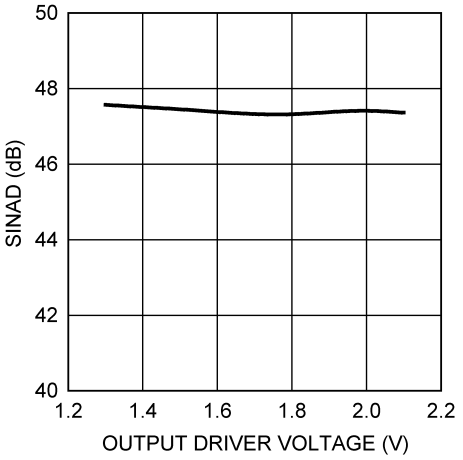
$V_A = V_{DR} = +1.9V$, $f_{CLK} = 1$ GHz (differential clock), $f_{IN} = 248$ MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

SINAD vs. Supply Voltage



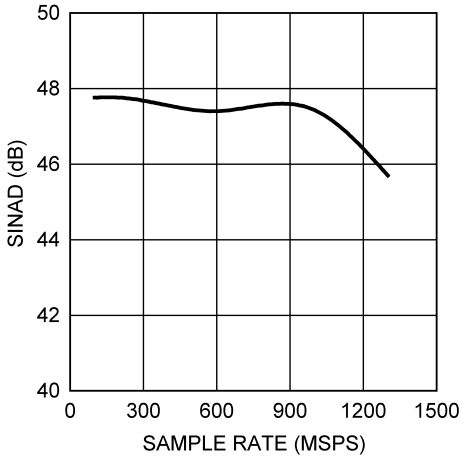
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SINAD vs. Output Driver Voltage



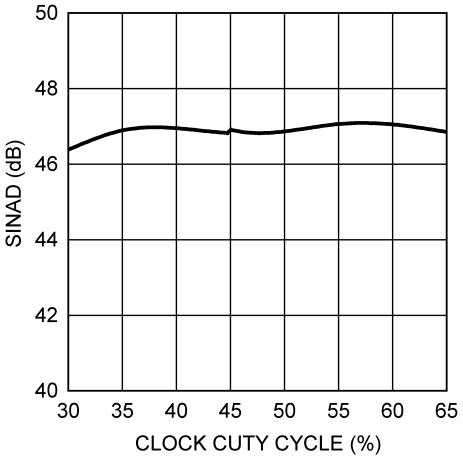
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SINAD vs. Sample Rate



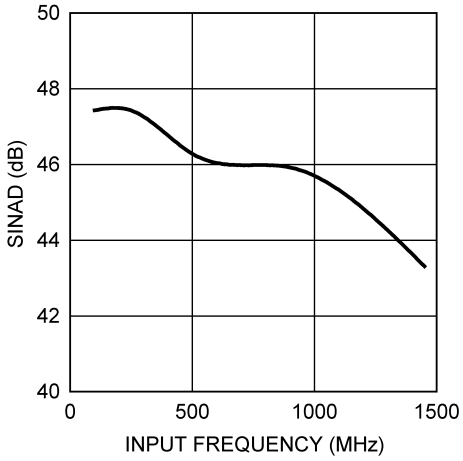
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SINAD vs. Clock Duty Cycle



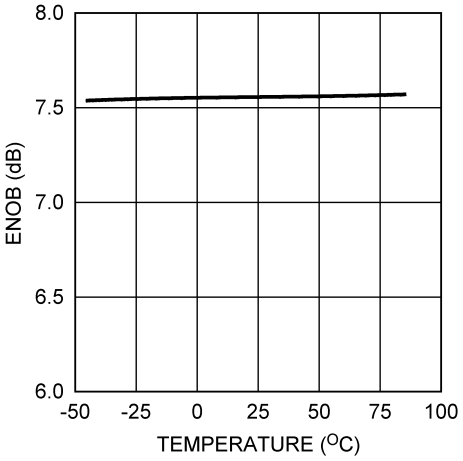
20068143

SINAD vs. Input Frequency



20068160

ENOB vs. Temperature

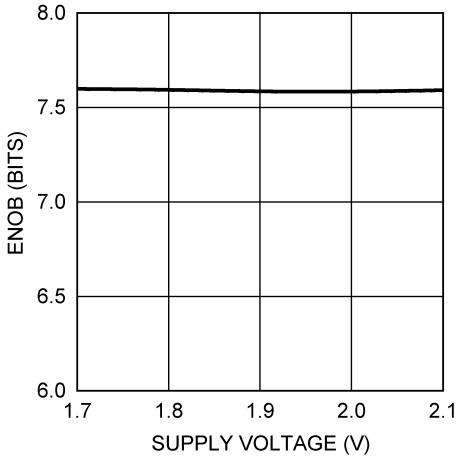


20068161

Typical Performance Characteristics

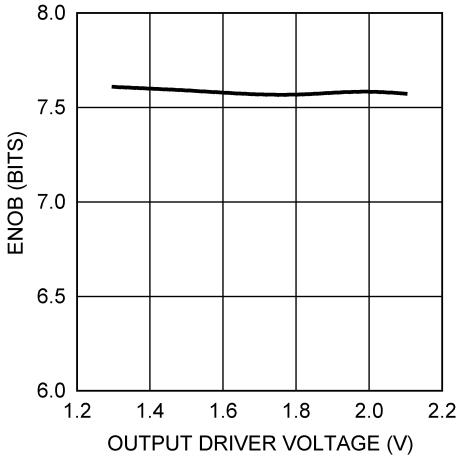
$V_A = V_{DR} = +1.9V$, $f_{CLK} = 1$ GHz (differential clock), $f_{IN} = 248$ MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

ENOB vs. Supply Voltage



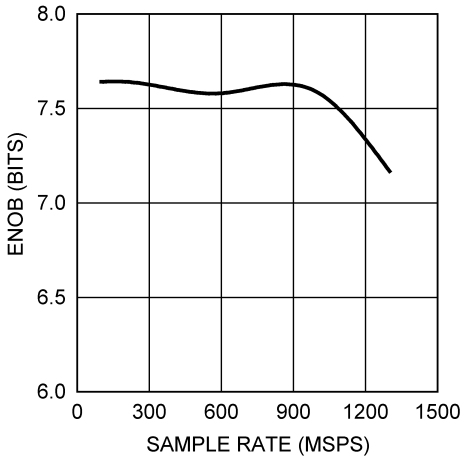
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ENOB vs. Output Driver Voltage



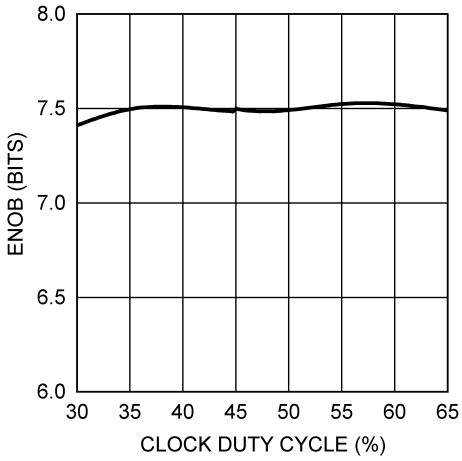
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ENOB vs. Sample Rate



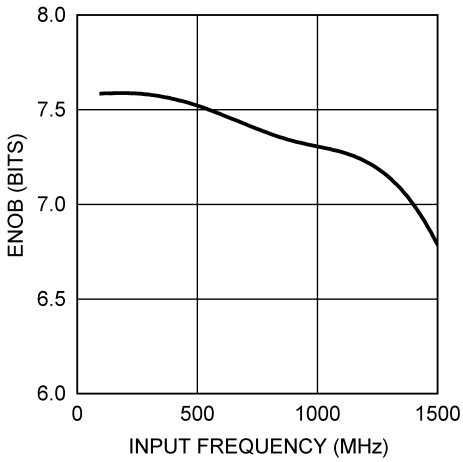
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ENOB vs. Clock Duty Cycle



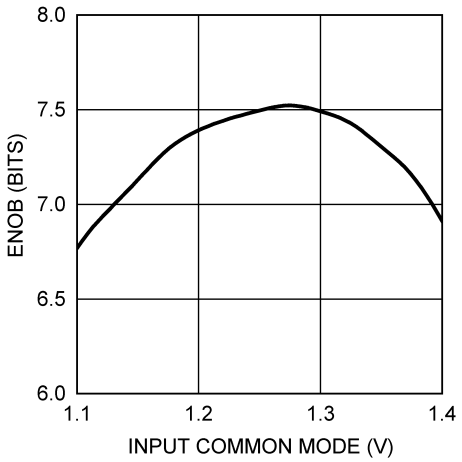
20068165

ENOB vs. Input Frequency



20068166

ENOB vs. Input Common Mode

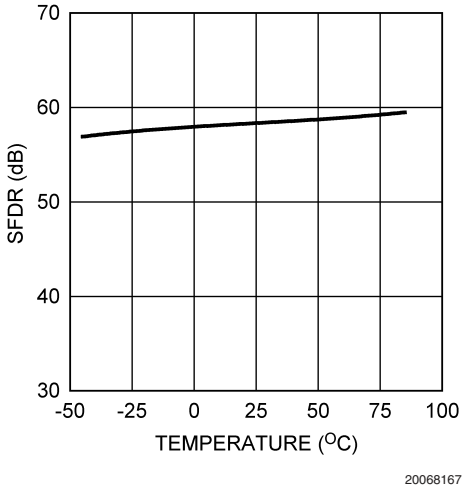


20068182

Typical Performance Characteristics

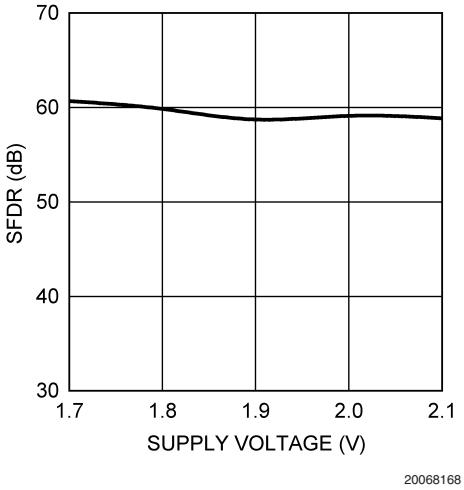
$V_A = V_{DR} = +1.9V$, $f_{CLK} = 1$ GHz (differential clock), $f_{IN} = 248$ MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

SFDR vs. Temperature



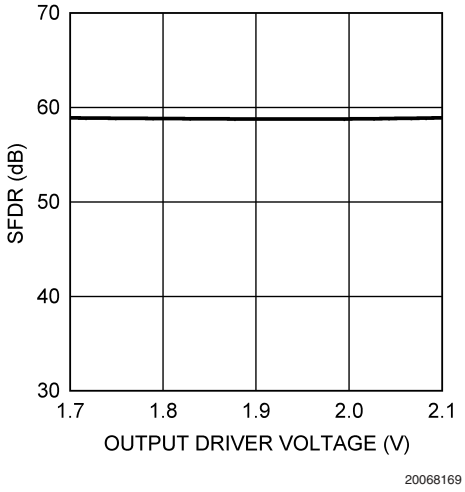
20068167

SFDR vs. Supply Voltage



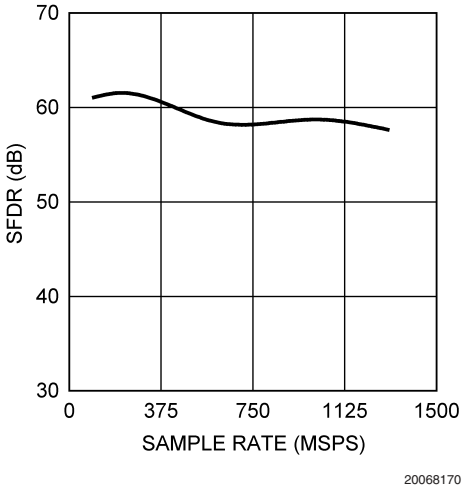
20068168

SFDR vs. Output Driver Voltage



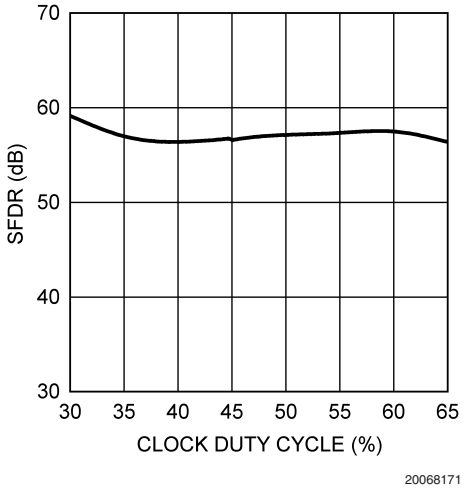
20068169

SFDR vs. Sample Rate



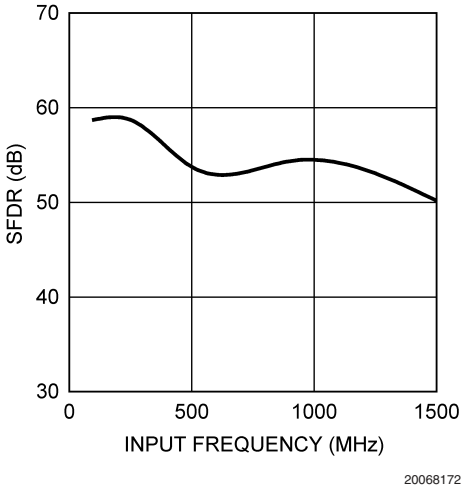
20068170

SFDR vs. Clock Duty Cycle



20068171

SFDR vs. Input Frequency

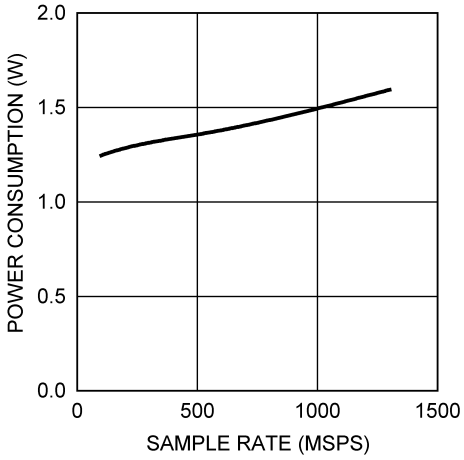


20068172

Typical Performance Characteristics

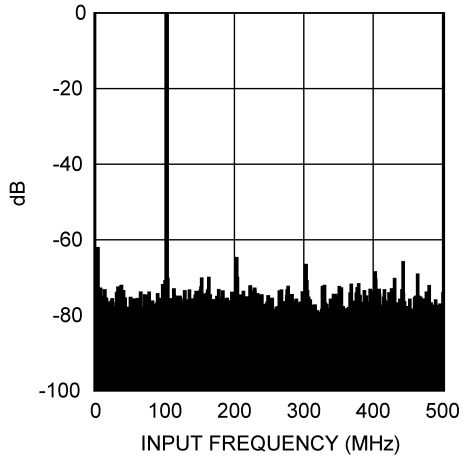
V_A = V_{DR} = +1.9V, f_{CLK} = 1 GHz (differential clock), f_{IN} = 248 MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

Power Consumption vs. Sample Rate



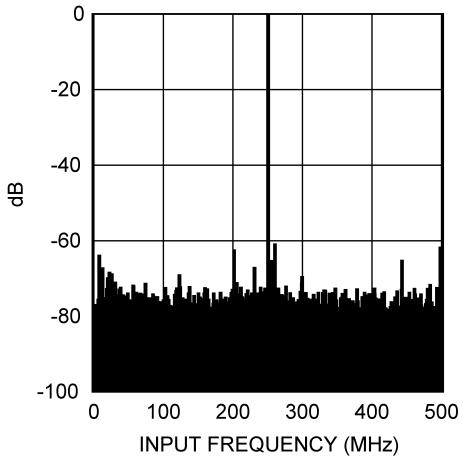
20068174

Spectral Response @ f_{IN} = 100 MHz



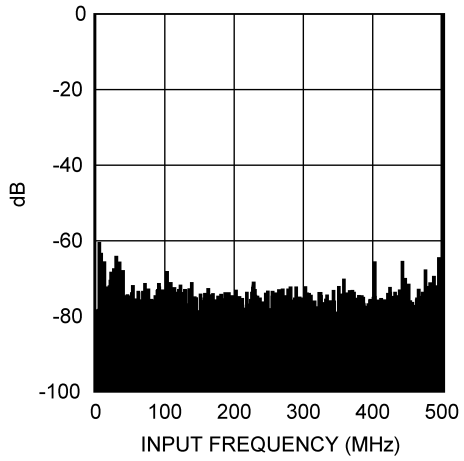
20068175

Spectral Response @ f_{IN} = 248 MHz



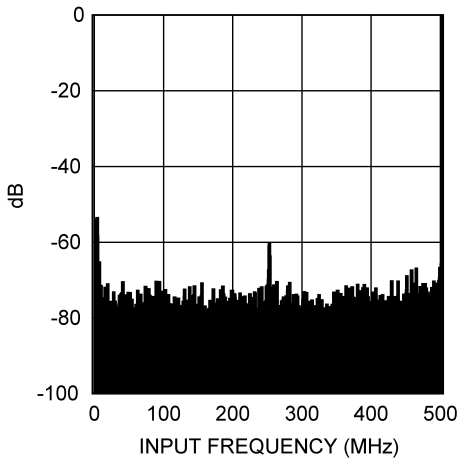
20068176

Spectral Response @ f_{IN} = 498 MHz



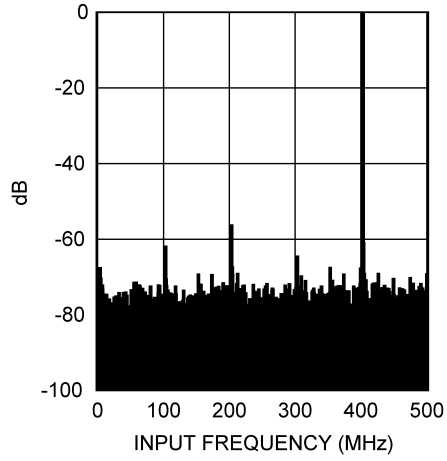
20068177

Spectral Response @ f_{IN} = 1.5 GHz



20068178

Spectral Response @ f_{IN} = 1.6 GHz

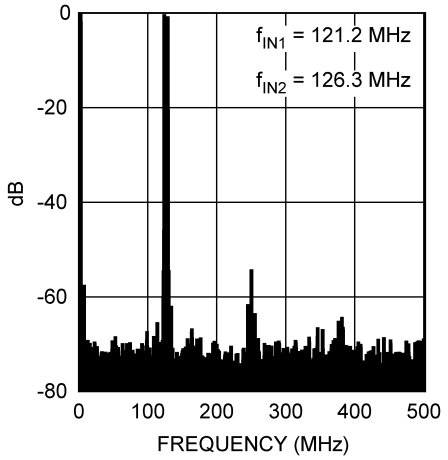


20068179

Typical Performance Characteristics

$V_A = V_{DR} = +1.9V$, $f_{CLK} = 1$ GHz (differential clock), $f_{IN} = 248$ MHz, Differential Inputs, unless otherwise stated. Parameters shown across temperature were measured after recalibration at each temperature. (Continued)

Intermodulation Distortion



20068183

Functional Description

The ADC081000 is a versatile, high performance, easy to use A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. The ADC081000 uses a calibrated folding and interpolating architecture that achieves over 7.5 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption, while Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

1.0 OVERVIEW

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 200 MSPS to 1.6 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. The OR (Out of Range) output is activated whenever the correct output code would be outside of the 00h to FFh range.

The converter has a 1:2 demultiplexer that feeds two LVDS output buses. The data on these buses provide an output word rate on each bus at half the ADC sampling rate and must be interleaved by the user to provide output words at the full conversion rate.

The output levels may be selected to be normal or reduced. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

The voltage reference for the ADC081000 is derived from a 1.254V bandgap reference which is made available to the user at the V_{BG} pin. This output is capable of sourcing or sinking ±100 µA.

The internal bandgap derived reference voltage has a nominal value of 600 mV or 800 mV, as determined by the FSR pin and described in Section 1.3. There is no provision for the use of an external reference voltage.

The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with self calibration, enables flat SINAD/ENOB response beyond 1.0 GHz. The ADC081000 output data signaling is LVDS and the output format is offset binary.

1.1 Self-Calibration

A self-calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR), SFDR and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command.

Running the self calibration is important for this chip's functionality and is *required* in order to obtain adequate performance. In addition to the requirement to be run at power-up, self calibration must be re-run whenever the sense of the FSR pin is changed.

For best performance, we recommend that self calibration be run 20 seconds or more after application of power and whenever the operating ambient temperature changes more than 30˚C since calibration was last performed. See Section 5.1.2 for more information.

During the calibration process, the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This external resistor must be placed between pin 32 and ground and must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because R_{EXT} is also used to set the proper bias current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least 10 clock cycles, then holding it high for at least another 10 clock cycles. There is no need to bring the CAL pin low after the 10 clock cycles of CAL high to begin the calibration routine. Holding the CAL pin high upon power up, however, will prevent the calibration process from running until the CAL pin experiences the above-mentioned 10 clock cycles low followed by 10 cycles high.

The CalDly pin is used to select one of two delay times after the application of power to the start of calibration. This calibration delay is 2^{24} clock cycles (about 16.8 ms at 1 GSPS) with CalDly low, or 2^{30} clock cycles (about 1.07 seconds at 1 GSPS) with CalDly high. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

Calibration can not be initiated or run while the device is in the power-down mode. See Section 1.7 for information on the interaction between Power Down and Calibration.

1.2 Acquiring the Input

Data is acquired at the falling edge of CLK+ (pin 18) and the digital equivalent of that data is available at the digital outputs 7 clock cycles later for the "D" output bus and 8 clock cycles later for the "Dd" output bus. There is an additional internal delay called t_{OD} before the data is available at the outputs. See the Timing Diagram. The ADC081000 will convert as long as the clock signal is present and the PD pin is low.

1.3 The Analog Inputs

The ADC081000 must be driven with a differential input signal. It is important that the inputs either be a.c. coupled to the inputs with the DC_Coup pin grounded or d.c. coupled with the DC_Coup pin high and have an input common mode voltage that is equal to and tracks the V_{CMO} output.

Two full-scale range settings are provided with the FSR pin. A high on that pin causes an input differential full-scale range setting of 800 mV_{P-P}, while grounding that pin causes an input differential full-scale range setting of 600 mV_{P-P}.

Functional Description (Continued)

1.4 Clocking

The ADC081000 must be driven with an a.c. coupled, differential clock signal. Section 4 describes the use of the clock input pins. A differential LVDS output clock is available for use in latching the ADC output data into whatever receives that data.

To help ease data capture, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). This is chosen with the OutEdge input. A high on the OutEdge input causes the output data to transition on the rising edge of DCLK, while grounding this input causes the output to transition on the falling edge of DCLK.

1.5 The LVDS Outputs

The data outputs, the Out Of Range (OR) and DCLK are LVDS compliant outputs. Output current sources provide 3 mA of output current to a differential 100 Ohm load when the OutV input is high or 2.2 mA when the OutV input is low. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the ADC081000 is used is noisy, it may be necessary to tie the OutV pin high.

1.6 Out Of Range (OR) Indication

The input signal is out of range whenever the correct code would be above positive full-scale or below negative full scale. When the input signal for any given sample is thus out of range, the OR output is high for that word time.

1.7 Power Down

The ADC081000 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the device power consumption is reduced to a minimal level and the outputs are in a high impedance state. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

1.8 Summary of Control Pins and Convenience Outputs

Table 1 and *Table 2* are provided as a guide to the use of the various control and convenience pins of the ADC081000. Note that this table is only a guide and that the rest of this data sheet should be consulted for the full meaning and use of these pins.

TABLE 1. Digital Control Pins

PIN	DESCRIPTION	LOW	HIGH
3	OutV	440mV Outputs	600mV Outputs
4	OutEdge	Data Transition at DCLK Fall	Data Transition at DCLK Rise
14	DC_Coup	A.C. Coupled Inputs	D.C. Coupled Inputs
26	PD	Normal Operation	Power Down
30	CAL	Normal Operation	Run Calibration
35	FSR	600 mV_{P-P} Full-Scale In	800 mV_{P-P} Full-Scale In
127	CalDly	2^{24} Clock Cycles	2^{30} Clock Cycles

TABLE 2. Convenience Output Pins

PIN	DESCRIPTION	USE / INDICATION
7	V_{CMO}	Common Mode Output Voltage.
31	V_{BG}	1.25V Convenience Output.
79 80	OR+ OR–	Differential Out-Of-Range Indication; active high.
126	CalRun	Low is normal operation. High indicates Calibration is running.

Applications Information

2.0 THE REFERENCE VOLTAGE

The voltage reference for the ADC081000 is derived from a 1.254V bandgap reference which is made available at the V_{BG} output for user convenience and has an output current capability of ±100 µA. The V_{BG} output should be buffered if more current than this is required of it.

The internal bandgap-derived reference voltage causes the full-scale peak-to-peak input swing to be either 600 mV or 800 mV, as determined by the FSR pin and described in Section 1.3. There is no provision for the use of an external reference voltage.

3.0 THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. *Table 3* gives the input to output relationship with the FSR pin high. With the FSR pin grounded, the millivolt values in *Table 3* are reduced to 75% of the values indicated.

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

Applications Information (Continued)

TABLE 3. DIFFERENTIAL INPUT TO OUTPUT RELATIONSHIP (FSR High)

V_{IN}+	V_{IN}−	Output Code
V_{CM} − 200 mV	V_{CM} + 200 mV	0000 0000
V_{CM} − 99 mV	V_{CM} + 99 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 101 mV	V_{CM} − 101 mV	1100 0000
V_{CM} + 200mV	V_{CM} − 200 mV	1111 1111

Note that a precise d.c. common mode voltage must be present at the ADC inputs. This common mode voltage, V_{CMO}, is provided on-chip when DC_Coup (pin 14) is low and the input signal is a.c. coupled to the ADC through 4.7 nF capacitors. See *Figure 4*.

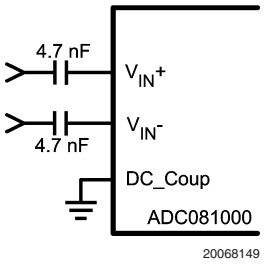


FIGURE 4. Differential Input Drive

When pin 14 is high, the analog inputs are d.c. coupled and a common mode voltage must be externally provided at the analog input pins. This common mode voltage should track the V_{CMO} output voltage. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change. Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog input pins remain within 50 mV of V_{CMO}.

If d.c. coupling is used, it is best to servo the input common mode voltage, using the V_{CMO} pin, to maintain optimum performance. An example of this type of circuit is shown in *Figure 5*. One such circuit should be used in front of the V_{IN}+ input and another in front of the V_{IN}− input. In that figure, R_{D1}, R_{D2} and R_{D3} are used to divide the V_{CMO} potential so that, after being gained up by the amplifier, the input common mode voltage is equal to V_{CMO} from the ADC. R_{D1} and R_{D2} are split to allow the bypass capacitor to isolate the input signal from V_{CMO}. R_{IN}, R_{D2} and R_{D3} will divide the input signal, if necessary. Capacitor "C" in *Figure 5* should be chosen to keep any component of the input signal from affecting V_{CMO}.

Be sure that any current drawn from the V_{CMO} output does not exceed ±1 µA.

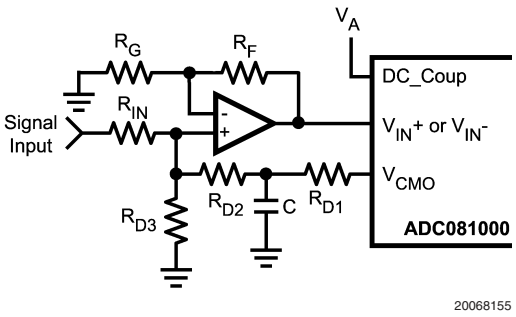


FIGURE 5. Example of Servoing the Analog Input with V_{CMO}

The Input impedance in the d.c. coupled mode (DC_Coup pin high) consists of a precision 100 Ohm resistor between V_{IN}+ and V_{IN}- and a capacitance from each of these inputs to ground. Driving the inputs beyond full scale will result in saturation or clipping of the reconstructed output.

3.1 Handling Single-Ended Analog Signals

There is no provision for the ADC081000 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-connected transformer, as shown in *Figure 6*.

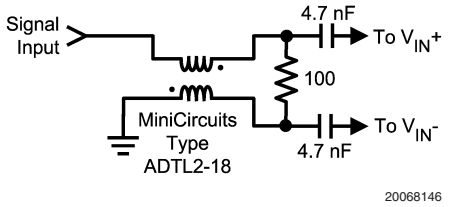


FIGURE 6. Single-Ended to Differential signal conversion with a balun-connected transformer

3.2 Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh.

3.3 Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC081000 is derived from an internal band-gap reference. The FSR pin controls the effective reference voltage of the ADC081000 such that the differential full-scale input range at the analog inputs is 800 mV_{P-P} with the FSR pin high, or is 600 mV_{P-P} with FSR pin low. Best SNR is obtained with FSR high, but better distortion and SFDR are obtained with the FSR pin low.

Applications Information (Continued)

4.0 THE CLOCK INPUTS

The ADC081000 has differential LVDS clock inputs, CLK+ and CLK-, which must be driven with an a.c. coupled, differential clock signal. Although the ADC081000 is tested and its performance is guaranteed with a differential 1.0 GHz clock, it typically will function well with clock frequencies indicated in the Electrical Characteristics Table. The clock inputs are internally terminated and biased. The clock signal must be capacitive coupled to the clock pins as indicated in *Figure 7*.

Operation up to the sample rates indicated in the Electrical Characteristics Table is typically possible if the conditions of the Operating Ratings are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management . See Section 7.2.

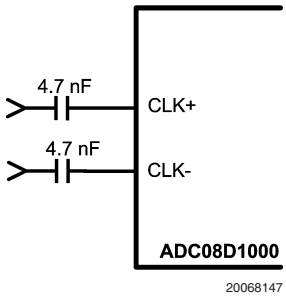


FIGURE 7. Differential (LVDS) Clock Connection

The differential Clock line pair should have a characteristic impedance of 100Ω and be terminated at the clock source in that (100Ω) characteristic impedance. The clock line should be as short and as direct as possible. The ADC081000 clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient clock levels will result in poor dynamic performance. Excessively high clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the clock level within the range specified in the Operating Ratings.

While it is specified and performance is guaranteed at 1.0 GSPS with a 50% clock duty cycle, ADC081000 performance is essentially independent of clock duty cycle. However, to ensure performance over temperature, it is recommended that the input clock duty cycle be such that the minimum clock high and low times are maintained within the range specified in the Electrical Characteristics Table.

High speed, high performance ADCs such as the ADC081000 require very stable clock signals with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the total of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)}/V_{INFSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, to the ADC analog input.

Note that the maximum jitter described above is the rms total of the jitter from all sources, including that in the ADC clock, that added by the system to the ADC clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

5.0 CONTROL PINS

Seven control pins provide a wide range of possibilities in the operation of the ADC081000 and facilitate its use. These control pins provide Full-Scale Input Range setting, Self Calibration, Calibration Delay, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down feature.

5.1 Self Calibration

The ADC081000 self-calibration must be run to achieve rated performance. This procedure is performed upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is a clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress.

5.1.1 Power-on Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, as described in Section 1.1.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until on-command calibration conditions are met. The ADC081000 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See On-Command Calibration Section 5.1.2.

The internal power-on calibration circuitry comes up in a random state. If the clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 200 mW. The power consumption will be normal after the clock starts.

5.1.2 On-Command Calibration

Calibration may be run at any time by bringing the CAL pin high for a minimum of 10 clock cycles after it has been low for a minimum of 10 clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of 10 clock clock cycles, then brought high for a minimum of another 10 clock cycles. The calibration cycle will begin 10 clock cycles after the CAL pin is thus brought high.

The minimum 10 clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in section 1.1, for best performance, a self calibration should be performed 20 seconds or more after power up and repeated when the ambient temperature changes more than 30˚C since the last self calibration was run. SINAD drops about 1.5 dB for every 30˚C change in die temperature and ENOB drops about 0.25 bit for every 30˚C change in die temperature.

Applications Information (Continued)

5.2 Calibration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration, as described in Section 1.1. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

5.3 Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these clock signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that clock signal can be used to latch the output data into the receiving circuit.

When the OutEdge pin is high, the output data is synchronized with (changes with) the rising edge of DCLK+. When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the ADC081000 is capable, slight differences in the lengths of the clock and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK edge that best suits the application circuit and layout.

5.4 Power Down Feature

The Power Down (PD) pin, when high, puts the ADC081000 into a low power mode where power consumption is greatly reduced.

The digital output pins retain the last conversion output code when the clock is stopped, but are in a high impedance state when the PD pin is high. However, upon return to normal operation (re-establishment of the clock and/or lowering of the PD pin), the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

6.0 THE DIGITAL OUTPUTS

The ADC081000 demultiplexes its output data onto two LVDS output buses.

The results of successive conversions started on the odd falling edges of the CLK+ pin are available on one of the two LVDS buses, while the results of conversions started on the even falling edges of the CLK+ pin are available on the other LVDS bus. This means that the word rate at each LVDS bus is 1/2 the ADC081000 clock rate and the two buses must be interleaved to obtain the entire 1 GSPS conversion result.

Since the minimum recommended clock rate for this device is 200 MSPS, the effective sample rate can be reduced to as low as 100 MSPS by using the results available on just one of the the two LVDS buses and a 200 MHz input clock, decimating the 200 MSPS data by two.

There is one LVDS clock pair available for use to latch the LVDS outputs on both buses. Whether the data is sent at the rising or falling edge of DCLK+ is determined by the sense of the OutEdge pin, as described in Section 5.3.

The OutV pin is used to set the LVDS differential output levels. See Section 1.5.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}– will produce an output code of all ones, a full-scale input level with V_{IN}– positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}– are equal, the output code will vary between 127 and 128.

7.0 POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance. Having power and ground planes in adjacent layers of the PC Board will provide the best supply bypass capacitance in terms of low ESL.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC081000 should be assumed to have little power supply noise rejection. Any power supply used for digital circuity in a system where a lot of digital power is being consumed should not be used to supply power to the ADC081000. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

7.1 Supply Voltage

The ADC081000 is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC081000 power pins.

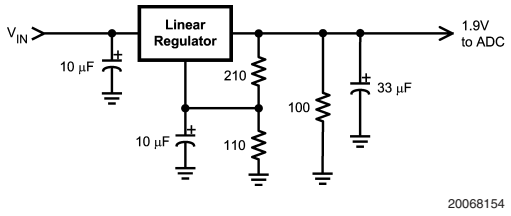


FIGURE 8. Non-Spiking Power Supply

Applications Information (Continued)

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC081000. The circuit of *Figure 8* will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC081000, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output in *Figure 8* provides a minimum output current during power-up to ensure there is no turn-on spiking.

In this circuit, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V . If a 3.3V supply is used, an LM1086 linear regulator is recommended. Also, be sure that the impedance of the power distribution system is low to minimize resistive losses and minimize noise on the power supply.

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in the Operating Ratings table. This voltage should not exceed the V_A supply voltage.

If the power is applied to the device without a clock signal present, the current drawn by the device might be below 100 mA. This is because the ADC081000 gets reset through clocked logic and its initial state is random. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the clock is established.

7.2 Thermal Management

The ADC081000 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 130˚C. That is, t_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 130˚C. This is not a problem if the ambient temperature is kept to a maximum of +85˚C, the device is soldered to a PC Board and the sample rate is at or below 1 Gsps.

Note that the following are general recommendations for mounting exposed pad devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

The package of the ADC081000 has an exposed pad on its back that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional LQFP, but the exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The exposed pad of the device must be soldered down to ensure adequate heat conduction out of the package. The land pattern for this exposed pad should be at least as large as the 5 x 5 mm of the exposed pad of the package and be located such that the exposed pad of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground. A clearance of at least 0.5 mm should separate this land pattern from the mounting pads for the package pins.

Since a large aperture opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the land pattern of *Figure 9*.

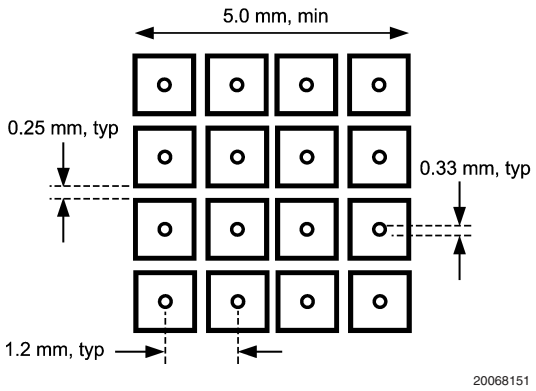


FIGURE 9. Recommended Package Land Pattern

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a minimum copper pad of 2 inches by 2 inches (5.1 cm by 5.1 cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process as this wicking could cause voids in the solder between the package exposed pad and the thermal land on the PCB. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

On a board of FR-4 material and the built in heat sink described above (4 square inch pad and 9 thermal vias), the die temperature stabilizes at about 30˚C above the ambient temperature in about 20 seconds.

If it is desired to monitor die temperature, a temperature sensor may be mounted on the heat sink area of the board near the thermal vias. Allow for a thermal gradient between the temperature sensor and the ADC081000 die of θ_{JC} times typical power consumption = 2.8 x 1.43 = 4˚C. Allowing for a 5˚C (including an extra 1˚C) temperature drop from the die to the temperature sensor, then, would mean that maintaining a maximum pad temperature reading of 125˚C will ensure that the die temperature does not exceed 130˚C, assuming that the exposed pad of the ADC081000 is properly soldered down and the thermal vias are adequate.

Applications Information (Continued)

8.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, as opposed to splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input "ground" return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90˚ to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90˚ crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC081000. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

9.0 DYNAMIC PERFORMANCE

The ADC081000 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in Section 4.0.

It is good practice to keep the ADC clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is a lower impedance than that offered by the package pins.

10.0 COMMON APPLICATION PITFALLS

Allowing loose power supply voltage tolerance. The ADC081000 is specified for operation between 1.8 Volts to 2.0 Volts. Using a 1.8 Volt power supply then implies the need for no negative tolerance. The best solution is to use an adjustable linear regulator such as the LM317 or LM1086 set for 1.9V as discussed in Section 7.1.

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, all inputs should not go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC081000. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in Sections 1.3 and 3.0, the Input common mode voltage must remain within 50 mV of the V_{CMO} output and track that output, which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO}.

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC081000 as many high speed amplifiers will have higher distortion than will the ADC081000, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage. As mentioned in Section 1.3, the reference voltage is intended to be fixed to provide one of two different full-scale values (600 mV_{P-P} and 800 mV_{P-P}). Over driving this pin will not change the full scale value, but can otherwise upset operation.

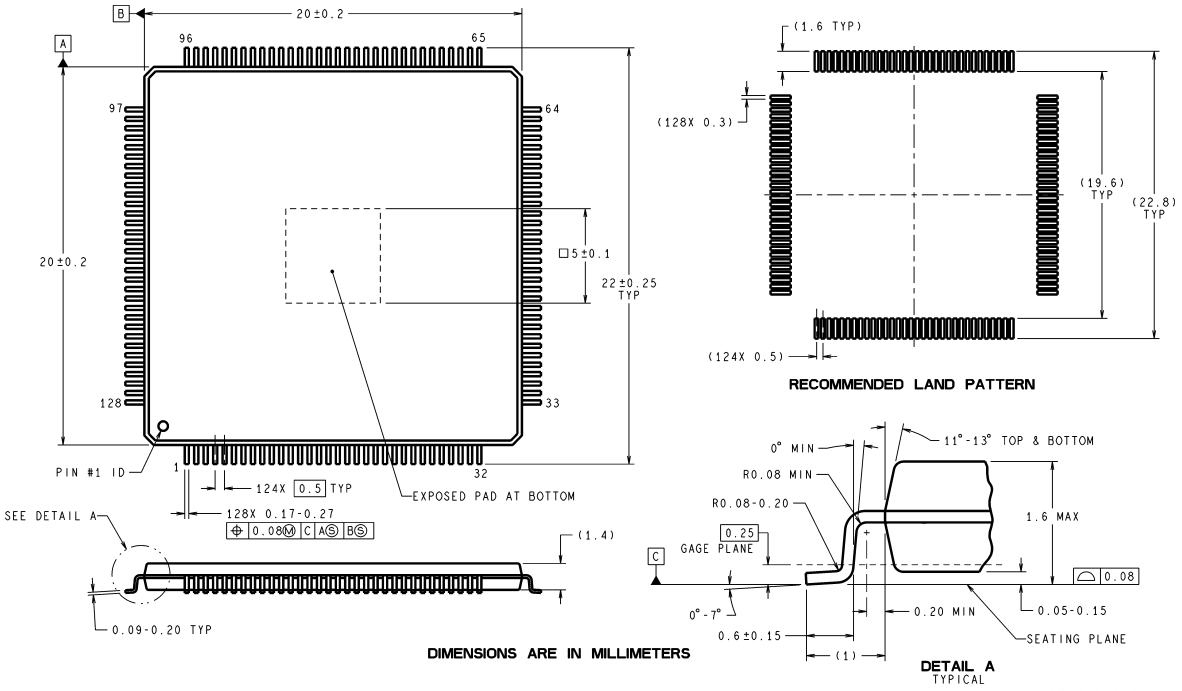
Driving the clock input with an excessively high level signal. The ADC clock level should not exceed the level described in the Operating Ratings Table or the input offset error could increase.

Inadequate clock levels. As described in Section 4.0, insufficient clock levels can result in poor performance. Excessive clock levels could result in the introduction of an input offset.

Using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in Section 7.2, it is important to provide an adequate heat removal to ensure device reliability. This can either be done with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

Physical Dimensions inches (millimeters) unless otherwise noted



VNX128A (Rev A)

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE JEDEC REGISTRATION MS-026, VARIATION BFB.

128-Lead Exposed Pad LQFP
Order Number ADC081000CIYB
NS Package Number VNX128A

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