

HIGH EFFICIENT SINGLE INDUCTOR BUCK-BOOST CONVERTER WITH 1.8-A SWITCHES

FEATURES

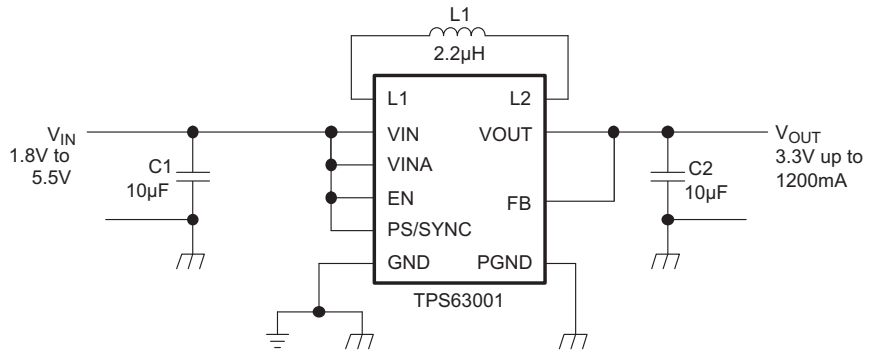
- **Up to 96% Efficiency**
- **1200-mA Output Current at 3.3V in Step Down Mode (VIN = 3.6V to 5.5V)**
- **Up to 800-mA Output Current at 3.3V in Boost Mode (VIN > 2.4V)**
- **Automatic Transition between Step Down and Boost Mode**
- **Device Quiescent Current less than 50μA**
- **Input Voltage Range: 1.8V to 5.5V**
- **Fixed and Adjustable Output Voltage Options from 1.2V to 5.5V**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **Forced Fixed Frequency Operation and Synchronization possible**
- **Load Disconnect During Shutdown**
- **Over-Temperature Protection**
- **Available in Small 3 mm × 3 mm, QFN-10 Package**

APPLICATIONS

- **All Two-Cell and Three-Cell Alkaline, NiCd or NiMH or Single-Cell Li Battery Powered Products**
- **Portable Audio Players**
- **PDAs**
- **Cellular Phones**
- **Personal Medical Products**
- **White LEDs**

DESCRIPTION

The TPS6300x devices provide a power supply solution for products powered by either a two-cell or three-cell alkaline, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. Output currents can go as high as 1200 mA while using a single-cell Li-Ion or Li-Polymer Battery, and discharge it down to 2.5V or lower. The buck-boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters Power Save mode to maintain high efficiency over a wide load current range. The Power Save mode can be disabled, forcing the converter to operate at a fixed switching frequency. The maximum average current in the switches is limited to a typical value of 1800 mA. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 10-pin QFN PowerPAD™ package measuring 3 mm × 3 mm (DRC).



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OUTPUT VOLTAGE OPTIONS(1)

T_A	OUTPUT VOLTAGE DC/DC	PACKAGE MARKING	PACKAGE	PART NUMBER(2)
–40°C to 85°C	Adjustable	BPT	10-Pin QFN	TPS63000DRC
	3.3 V	BPU		TPS63001DRC
	5.0 V	BPV		TPS63002DRC

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) The DRC package is available taped and reeled. Add R suffix to device type (e.g., TPS63000DRCR) to order quantities of 3000 devices per reel. Add T suffix to device type (e.g., TPS63000DRCT) to order quantities of 250 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	TPS6300x
Input voltage range on VIN, VINA, L1, L2, VOUT, PS/SYNC, EN, FB	–0.3 V to 7 V
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

DISSIPATION RATINGS TABLE

PACKAGE	THERMAL RESISTANCE Θ_{JA}	POWER RATING $T_A \leq 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
DRC	48.7°C/W	2054 mW	21 mW/°C

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at VIN, VINA	1.8		5.5	V
Operating free air temperature range, T_A	–40		85	°C
Operating virtual junction temperature range, T_J	–40		125	°C

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ELECTRICAL CHARACTERISTICS

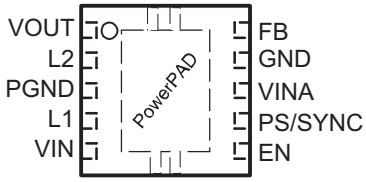
over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

DC/DC STAGE							
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range			1.8		5.5	V
V_I	Input voltage range for startup			1.9		5.5	V
V_O	TPS63000 output voltage range			1.2		5.5	V
V_{FB}	TPS63000 feedback voltage			495	500	505	mV
f	Oscillator frequency			1250		1500	kHz
	Frequency range for synchronization			1250		1800	kHz
I_{SW}	Switch current limit		V_{IN} = V_{INA} = 3.6 V, T_A = 25°C	1600	1800	2000	mA
	High side switch on resistance		V_{IN} = V_{INA} = 3.6 V		100		mΩ
	Low side switch on resistance		V_{IN} = V_{INA} = 3.6 V		100		mΩ
	Line regulation					0.5%	
	Load regulation					0.5%	
I_q	Quiescent current	VIN	I_O = 0 mA, V_{EN} = V_{IN} = V_{INA} = 3.6 V, V_{OUT} = 3.3 V		1	1.5	µA
		VINA			40	50	µA
		VOUT (adjustable output voltage)			4	6	µA
	FB input impedance (fixed output voltage)				1		MΩ
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = V_{INA} = 3.6 V		0.1	1	µA
CONTROL STAGE							
V_{UVLO}	Under voltage lockout threshold		V_{INA} voltage decreasing	1.5	1.7	1.8	V
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped on GND or VINA		0.01	0.1	µA
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

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PIN ASSIGNMENTS

DRC PACKAGE
(TOP VIEW)

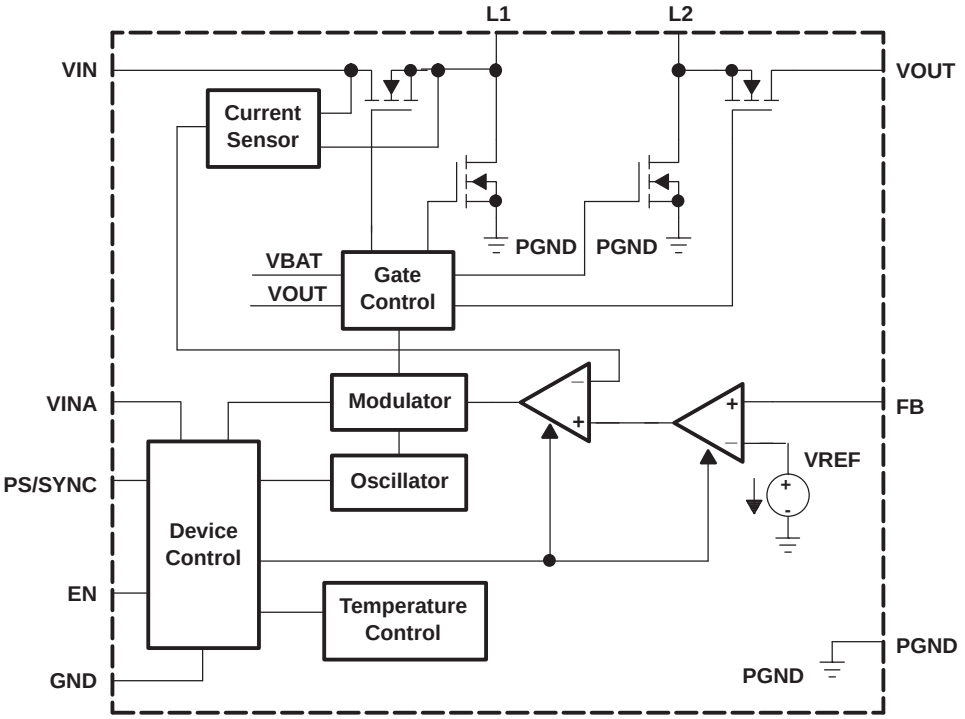


Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	6	I	Enable input. (1 enabled, 0 disabled)
FB	10	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions
GND	9		Control / logic ground
PS/SYNC	7	I	Enable / disable power save mode (1 disabled, 0 enabled, clock signal for synchronization)
L1	4	I	Connection for Inductor
L2	2	I	Connection for Inductor
PGND	3		Power ground
VIN	5	I	Supply voltage for power stage
VOUT	1	O	Buck-boost converter output
VINA	8	I	Supply voltage for control stage
PowerPAD™			Must be soldered to achieve appropriate power dissipation. Should be connected to PGND.

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FUNCTIONAL BLOCK DIAGRAM (TPS63000)



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

DESCRIPTION		FIGURE
Maximum output current	vs Input voltage	1
Efficiency	vs Output current (TPS63001)	2
	vs Output current (TPS63002)	3
	vs Input voltage (TPS63001)	4
	vs Input voltage (TPS63002)	5
Output voltage	vs Output current (TPS63001)	6
	vs Output current (TPS63002)	7
Waveforms	Output voltage in continuous current mode (TPS63001, VIN > VOUT)	8
	Output voltage in continuous current mode (TPS63001, VIN < VOUT)	9
	Output voltage in continuous current mode (TPS63001, VIN = VOUT)	10
	Output voltage in power save mode (TPS63001, VIN > VOUT)	11
	Output voltage in power save mode (TPS63001, VIN < VOUT)	12
	Load transient response (TPS63001, VIN > VOUT)	13
	Load transient response (TPS63001, VIN < VOUT)	14
	Line transient response (TPS63001, Iout = 300mA)	15
	Line transient response (TPS63001, Iout = 600mA)	16
	Startup after enable (TPS63000, VOUT = 2.5V)	17
	Startup after enable (TPS63002)	18

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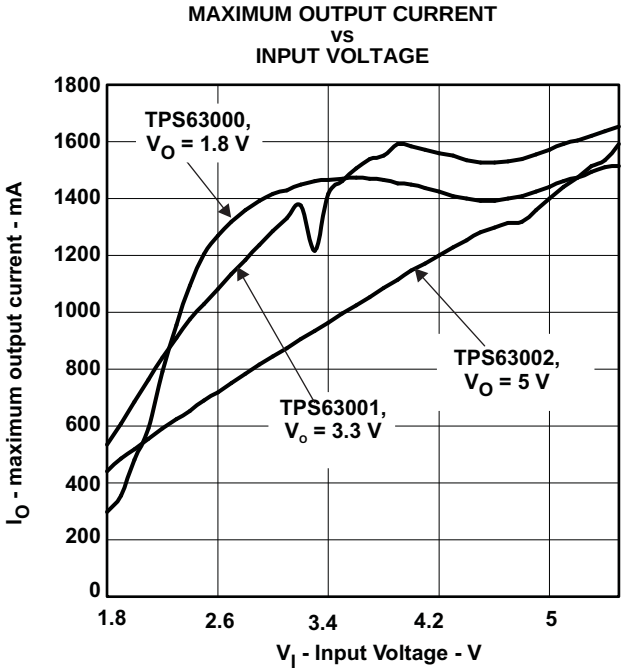


Figure 1.

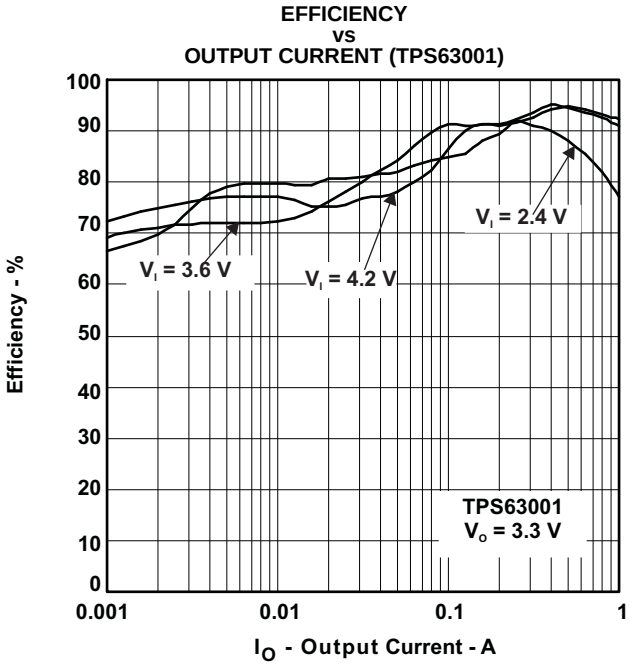


Figure 2.

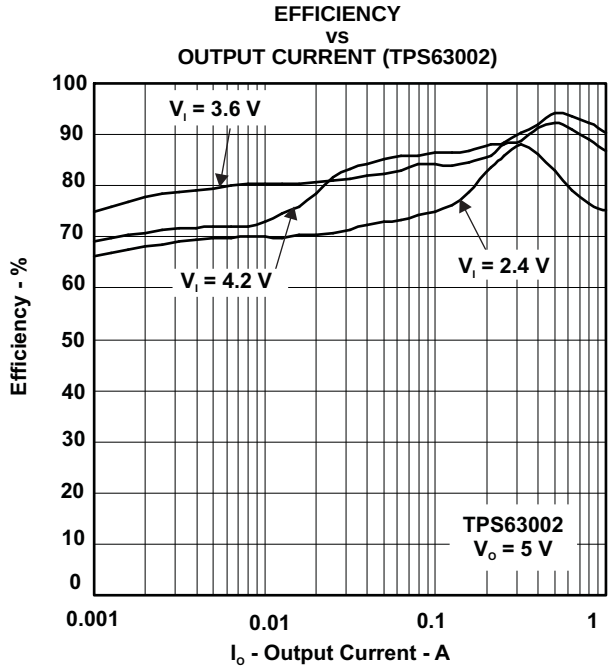


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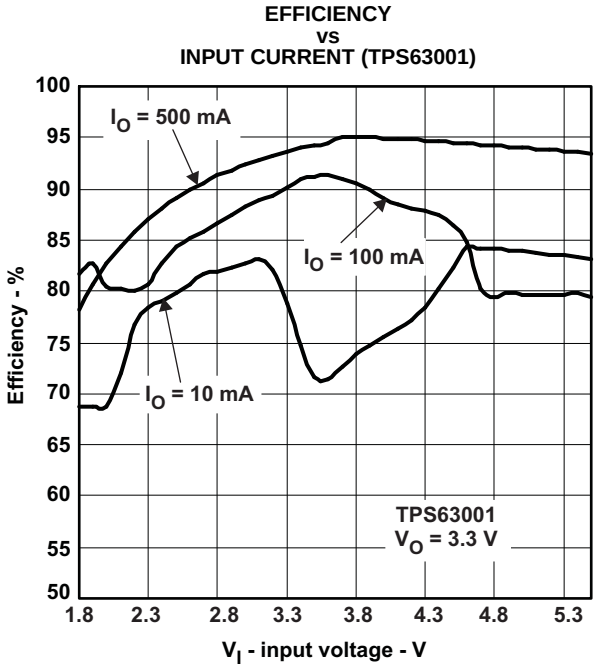


Figure 4.

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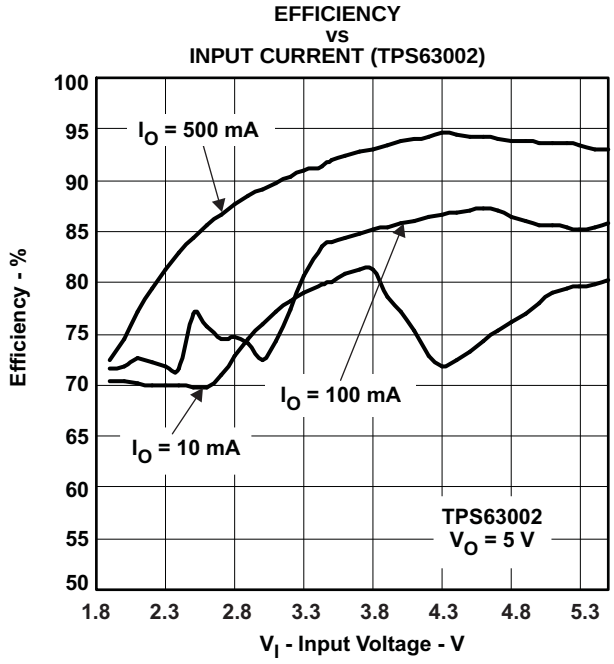


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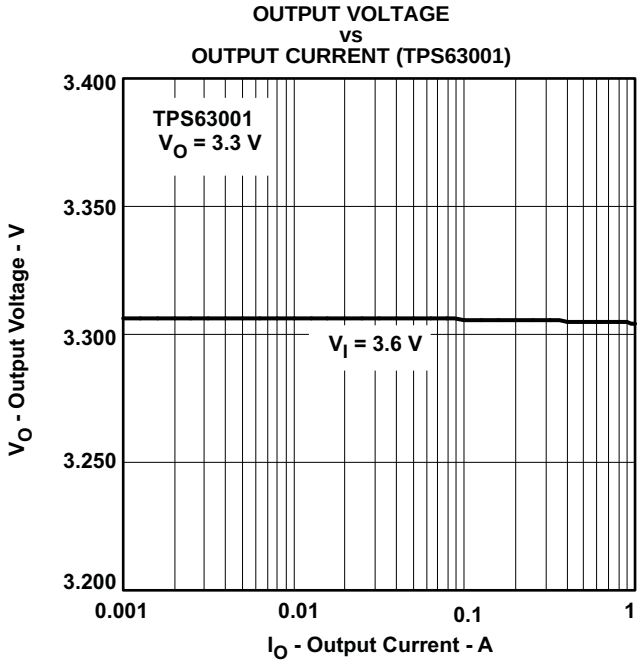


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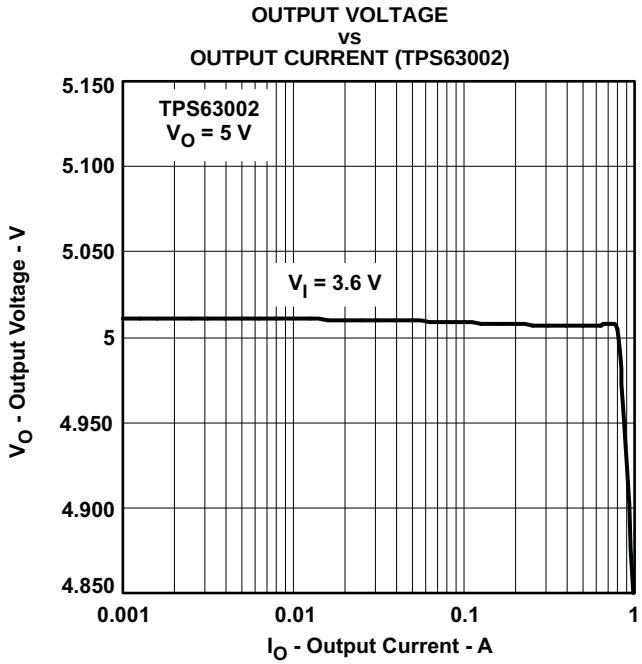


Figure 7.

OUTPUT VOLTAGE IN CONTINUOUS CURRENT MODE (TPS63001, VIN > VOUT)

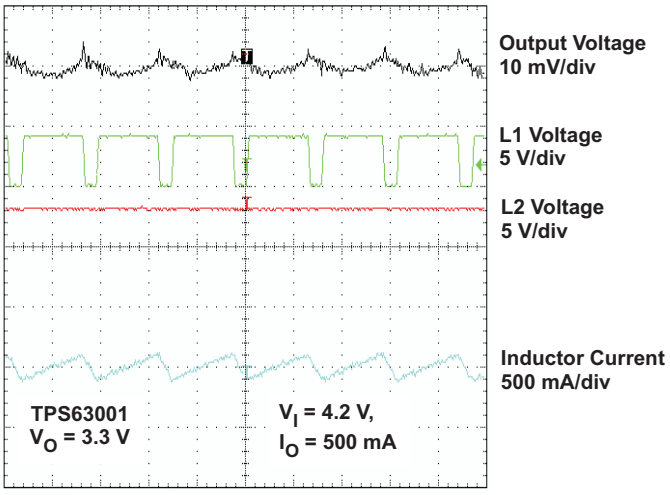


Figure 8.

OUTPUT VOLTAGE IN CONTINUOUS CURRENT MODE (TPS63001, VIN > VOUT)

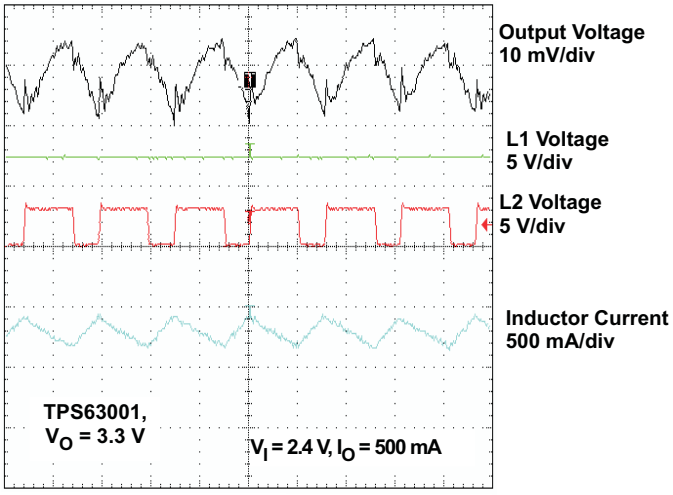


Figure 9.

OUTPUT VOLTAGE IN CONTINUOUS CURRENT MODE (TPS63001, VIN = VOUT)

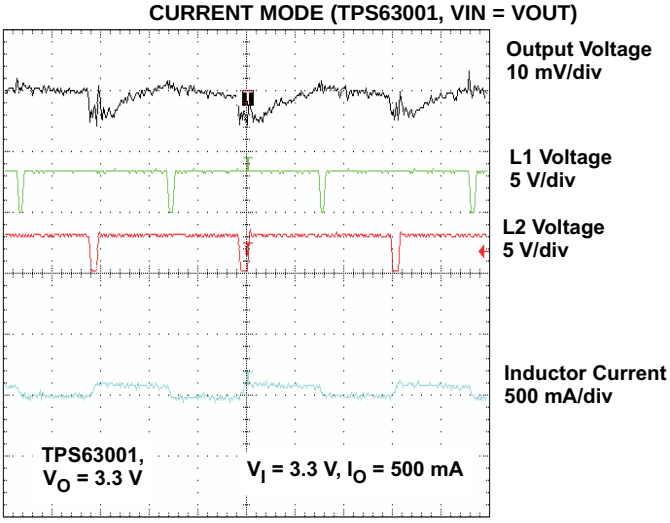


Figure 10.

OUTPUT VOLTAGE IN POWER SAVE MODE (TPS63001, VIN > VOUT)

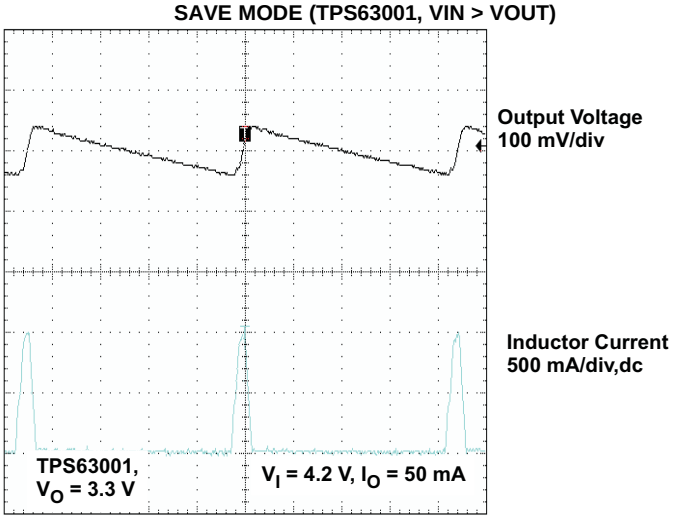


Figure 11.

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OUTPUT VOLTAGE IN POWER SAVE MODE (TPS63001, VIN < VOUT)

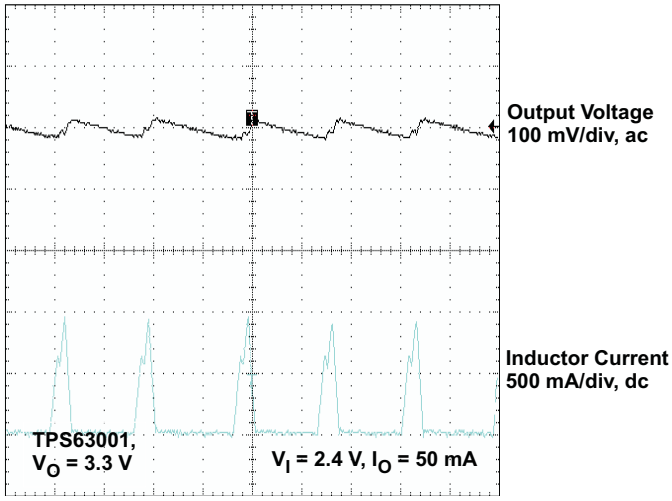


Figure 12.

LOAD TRANSIENT RESPONSE (TPS63001, VIN > VOUT)

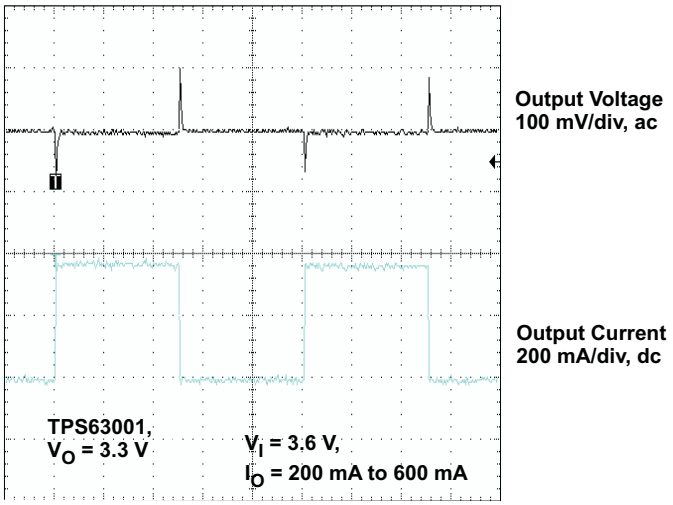


Figure 13.

LOAD TRANSIENT RESPONSE (TPS63001, VIN < VOUT)

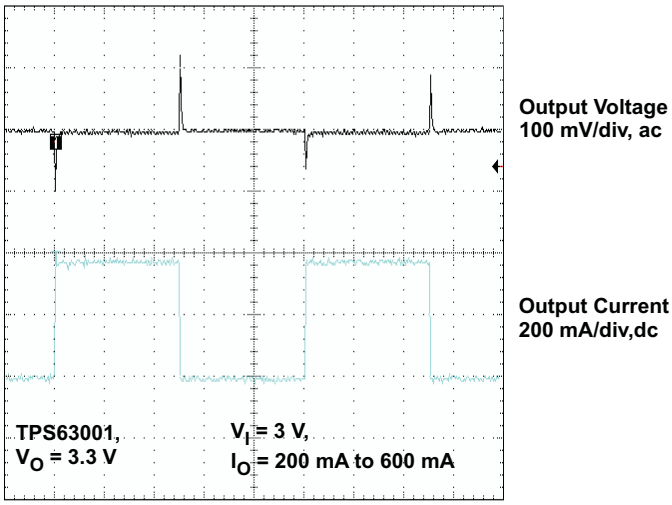


Figure 14.

LINE TRANSIENT RESPONSE (TPS63001, Iout = 300mA)

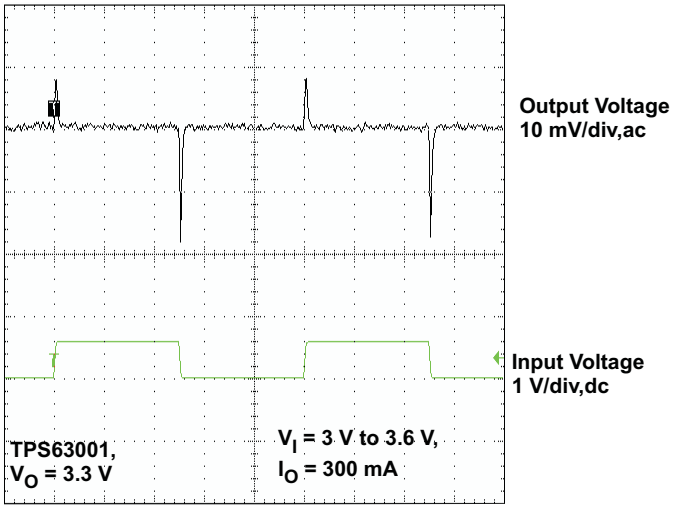


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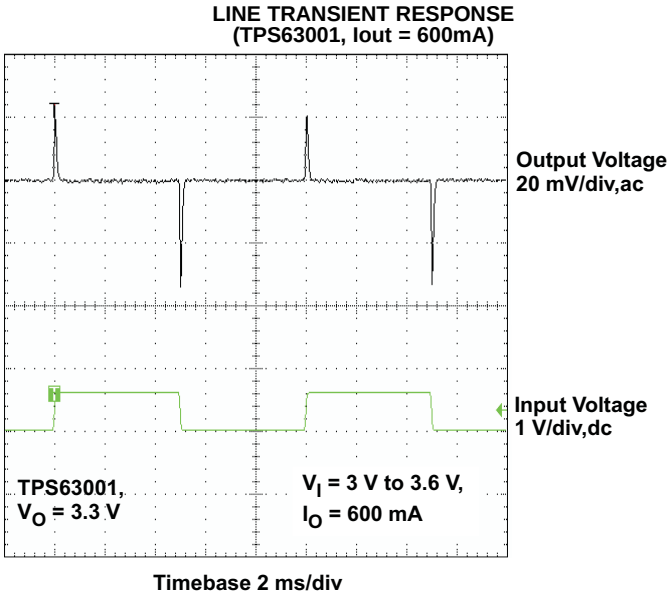


Figure 16.

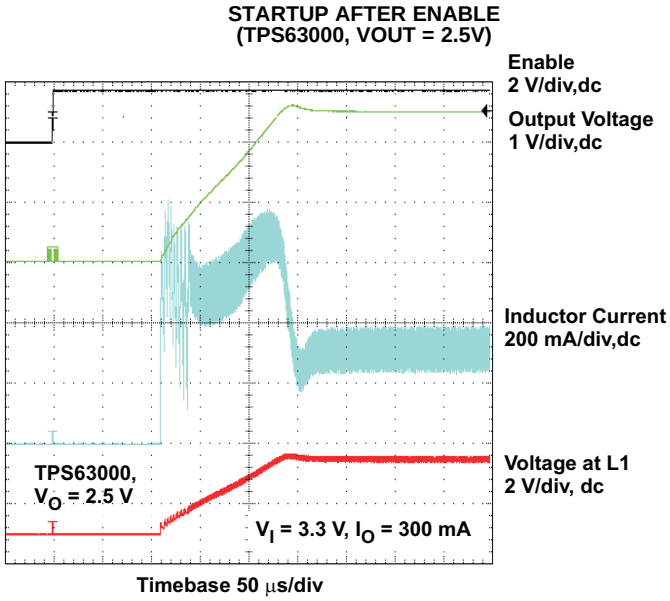


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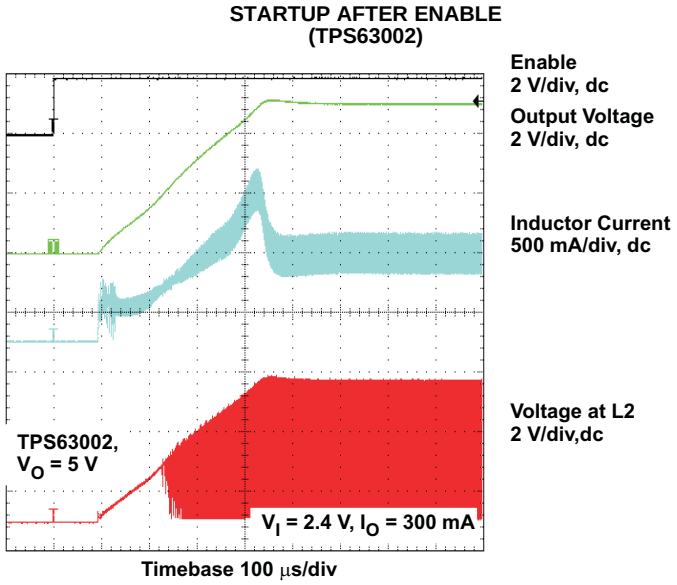
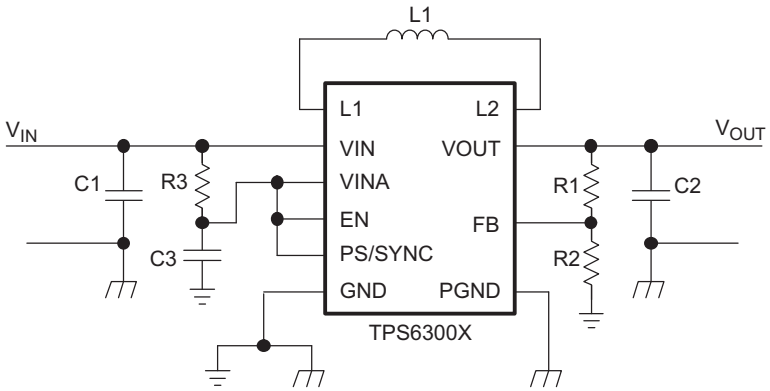


Figure 18.

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PARAMETER MEASUREMENT INFORMATION



List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS6300 0 / 1 / 2	Texas Instruments
L1	VLF4012-2R2	TDK
C1	10 µF 6.3V, 0603, X7R ceramic	
C2	2 × 10 µF 6.3V, 0603, X7R ceramic	
C3	0.1 µF, X7R ceramic	
R3	100 Ω	
R1, R2	Depending on the output voltage at TPS63000, not used at TPS6300 1 / 2	

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DETAILED DESCRIPTION

CONTROLLER CIRCUIT

The controlling circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages a resistive voltage divider must be connected to that pin. At fixed output voltages FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The controller circuit also senses the average input current as well as the peak input current. With this, maximum input power can be controlled as well as the maximum peak current to achieve a safe and stable operation under all possible conditions. To finally protect the device from overheating, an internal temperature sensor is implemented.

Synchronous Operation

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficency over a wide input voltage and output power range.

To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point ideally close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter.

Buck-Boost Operation

To be able to regulate the output voltage properly at all possible input voltage conditions, the device automatically switches from step down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation; when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Switching losses are also kept low by using only one active and one passive switch. Regarding the remaining 2 switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

Power Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. To enable power save, PS/SYNC must be set low. Power save mode is used to improve efficiency at light load. If power save mode is enabled, the converter stops operating if the average inductor current gets lower than about 300 mA and the output voltage is at or above its nominal value. If the output voltage decreases below its nominal value, the device ramps up the output voltage again by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last for one or several pulses. The converter again stops operating once the conditions for stopping operation are met again.

The power save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency. Synchronization is done by a PLL, so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

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Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

Softstart and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial 400mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will not increase. There is no timer implemented. Thus the output voltage overshoot at startup, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a very large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output and keeps the current limit low to protect itself and the application. At a short at the output during operation the current limit also will be decreased accordingly. At 0 V at the output, for example, the output current will not exceed about 400 mA.

Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VINA is lower than approximately its threshold (see electrical characteristics table). When in operation, the device automatically enters the shutdown mode if the voltage on VINA drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

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APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6300x dc/dc converters are intended for systems powered by one-cell Li-Ion or Li-Polymer battery with a typical voltage between 2.3 V and 4.5 V. They can also be used in systems powered by a double or triple cell Alkaline, NiCd, or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V . Additionally, any other voltage source with a typical output voltage between 1.8 V and 5.5 V can power systems where the TPS6300x is used.

PROGRAMMING THE OUTPUT VOLTAGE

Within the TPS6300X family there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. At the adjustable output voltage versions, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500mV. The maximum recommended value for the output voltage is 5.5V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on those two values, the recommended value for R_2 should be lower than 500kΩ, in order to set the divider current at 1µA or higher. It is recommended to keep the value for this resistor in the range of 200kΩ. From that, the value of the resistor connected between VOUT and FB, R_1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 1:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1.0 MΩ resistor should be chosen for R_1. To improve control performance using a feedforward capacitor in parallel to R_1 is recommended. The value for the feedforward capacitor can be calculated using Equation 2.

$$C_{ff} = \frac{2.2\ \mu s}{R_1} \quad (2)$$

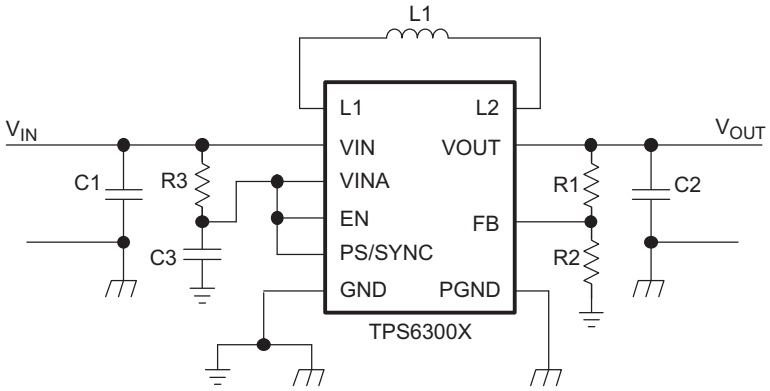


Figure 19. Typical Application Circuit for Adjustable Output Voltage Option

INDUCTOR SELECTION

To properly configure the TPS6300X devices, an inductor must be connected between pin L1 and pin L2. To estimate the inductance value Equation 3 and Equation 4 can be used.

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$$L_1 = \frac{V_{OUT} \times \left(V_{IN1} - V_{OUT}\right)}{V_{IN1} \times f \times 0.3\ A} \quad (3)$$

$$L_2 = \frac{V_{in2} \times \left(V_{OUT} - V_{IN2}\right)}{V_{OUT} \times f \times 0.3\ A} \quad (4)$$

In both equations *f* is the minimum switching frequency. In Equation 3 the minimum inductance value, L_1 for step down mode operation is calculated. V_{IN1} is the maximum input voltage. In Equation 4 the minimum inductance, L_2, for boost mode operation is calculated. V_{IN2} is the minimum input voltage. The recommended minimum inductor value is either L_1 or L_2 whichever is higher. As an example, a suitable inductor for generating 3.3V from a Li-Ion battery with a battery voltage range from 2.5V up to 4.2V is 2.2 µH. The recommended inductor value range is between 1.5 µH and 4.7 µH. In general, this means that at high voltage conversion rates, higher inductor values offer better performance.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 5 shows how to calculate the peak current I_1 in step down mode operation and Equation 6 shows how to calculate the peak current I_2 in boost mode operation.

$$I_1 = \frac{I_{OUT}}{0.8} + \frac{V_{OUT}\left(V_{IN1} - V_{OUT}\right)}{2 \times V_{IN1} \times f \times L} \quad (5)$$

$$I_2 = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN2}} + \frac{V_{IN2} \times \left(V_{OUT} - V_{IN2}\right)}{2 \times V_{OUT} \times f \times L} \quad (6)$$

The critical current value for selecting the right inductor is the higher value of I_1 and I_2. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents. This also needs to be taken into account when selecting an appropriate inductor. The following inductor series from different suppliers have been used with TPS6300x converters:

Table 1. List of Inductors

VENDOR	INDUCTOR SERIES
Coilcraft	LPS3015
	LPS4012
Murata	LQH3NP
Tajo Yuden	NR3015
TDK	VLF3215
	VLF4012

CAPACITOR SELECTION

Input Capacitor

At least a 4.7 µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC.

To get an estimate of the recommended minimum output capacitance, Equation 7 can be used.

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$$C_{OUT} = 5 \times L \times \frac{\mu F}{\mu H} \quad (7)$$

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6300x devices is 125°C. The thermal resistance of the 10-pin QFN 3 × 3 package (DRC) is $R_{\theta JA}$ = 48.7°C/W, if the PowerPAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 820mW, as calculated in Equation 8. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125°C - 85°C}{48.7\ °C/W} = 820\ mW \quad (8)$$

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS63000DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63000DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63000DRCT	ACTIVE	SON	DRC	10	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63000DRCTG4	ACTIVE	SON	DRC	10	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63001DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63001DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63001DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63001DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63002DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63002DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63002DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS63002DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TPS63000 :

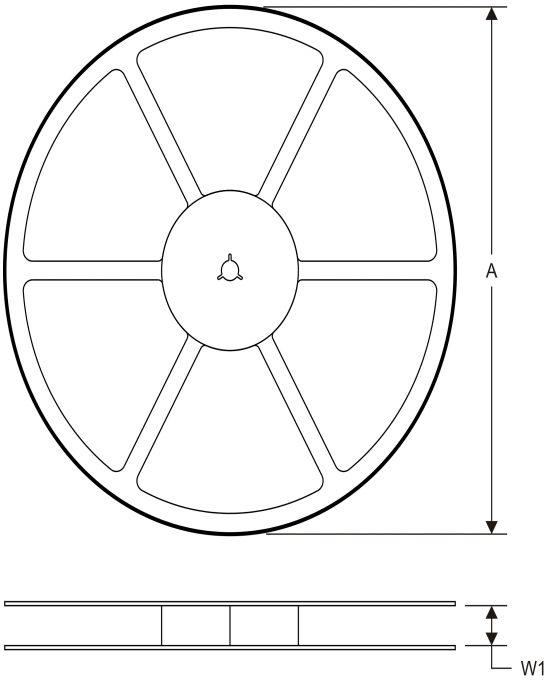
- Automotive: TPS63000-Q1

NOTE: Qualified Version Definitions:

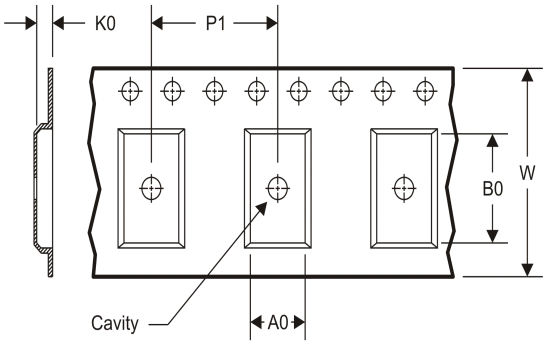
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



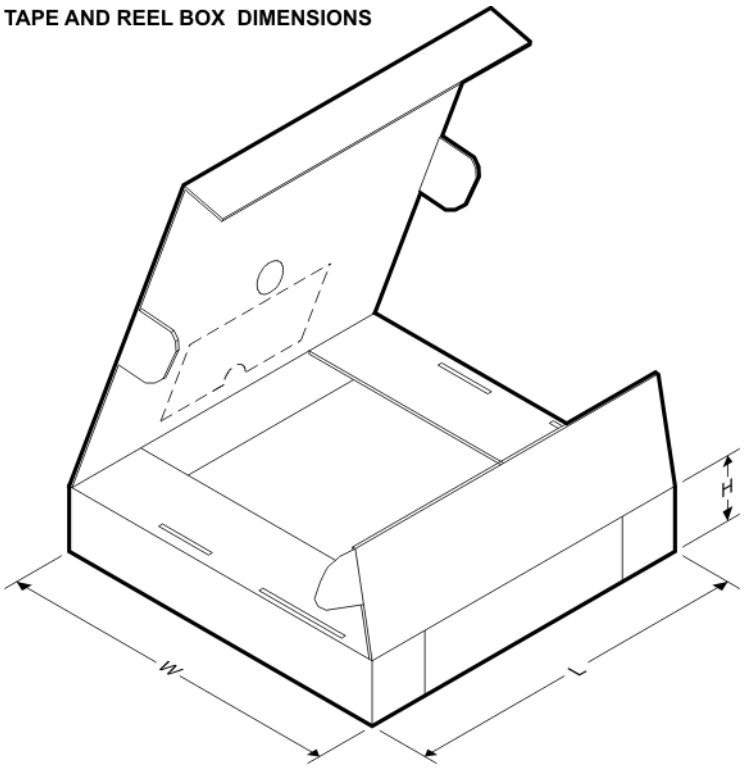
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63000DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63000DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63000DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63000DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63001DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63001DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63001DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63002DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63002DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63002DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63002DRCT	SON	DRC	10	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

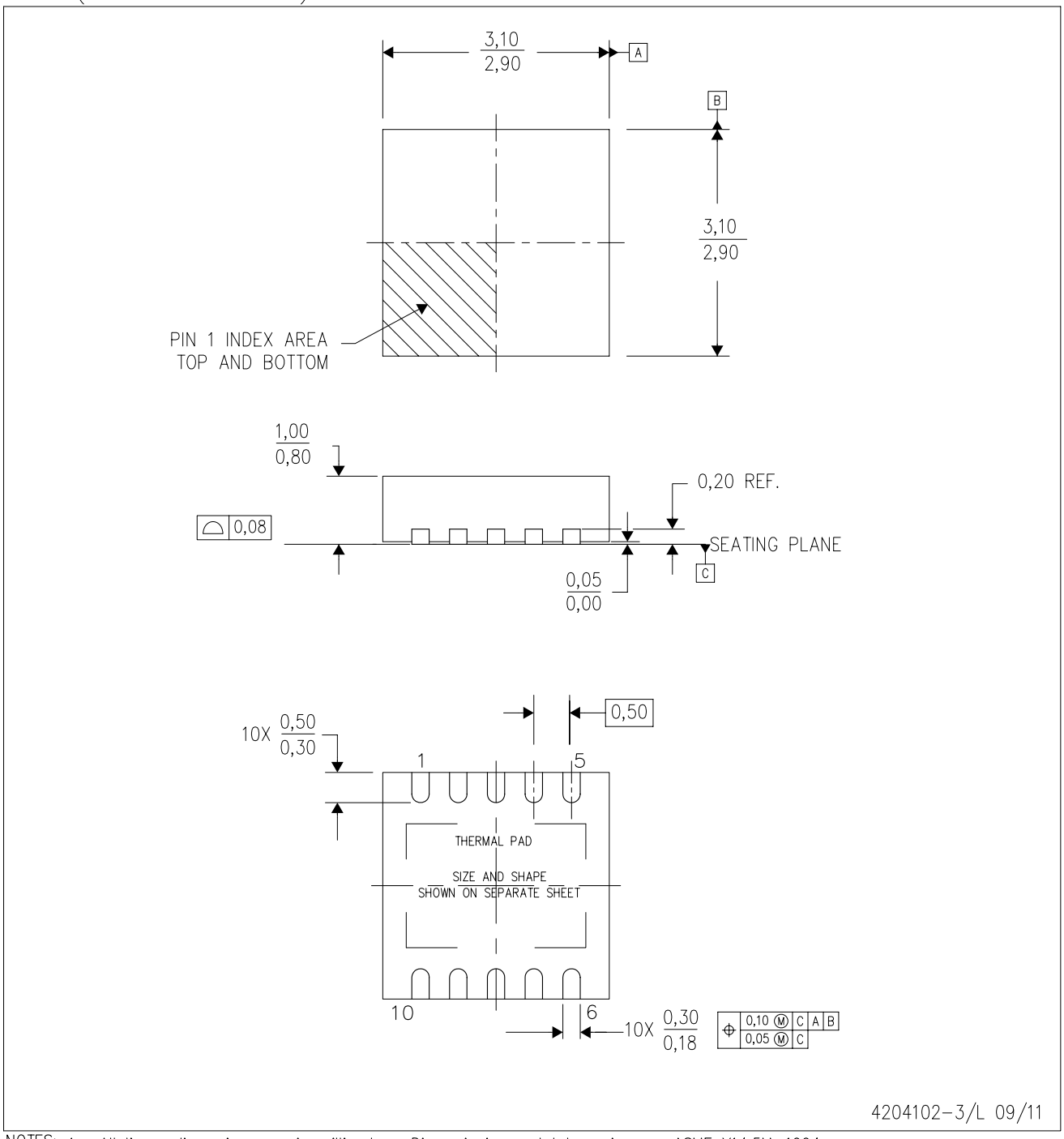
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63000DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS63000DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS63000DRCT	SON	DRC	10	250	210.0	185.0	35.0
TPS63000DRCT	SON	DRC	10	250	210.0	185.0	35.0
TPS63001DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS63001DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS63001DRCT	SON	DRC	10	250	210.0	185.0	35.0
TPS63002DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS63002DRCR	SON	DRC	10	3000	367.0	367.0	35.0
TPS63002DRCT	SON	DRC	10	250	210.0	185.0	35.0
TPS63002DRCT	SON	DRC	10	250	340.5	338.1	20.6

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

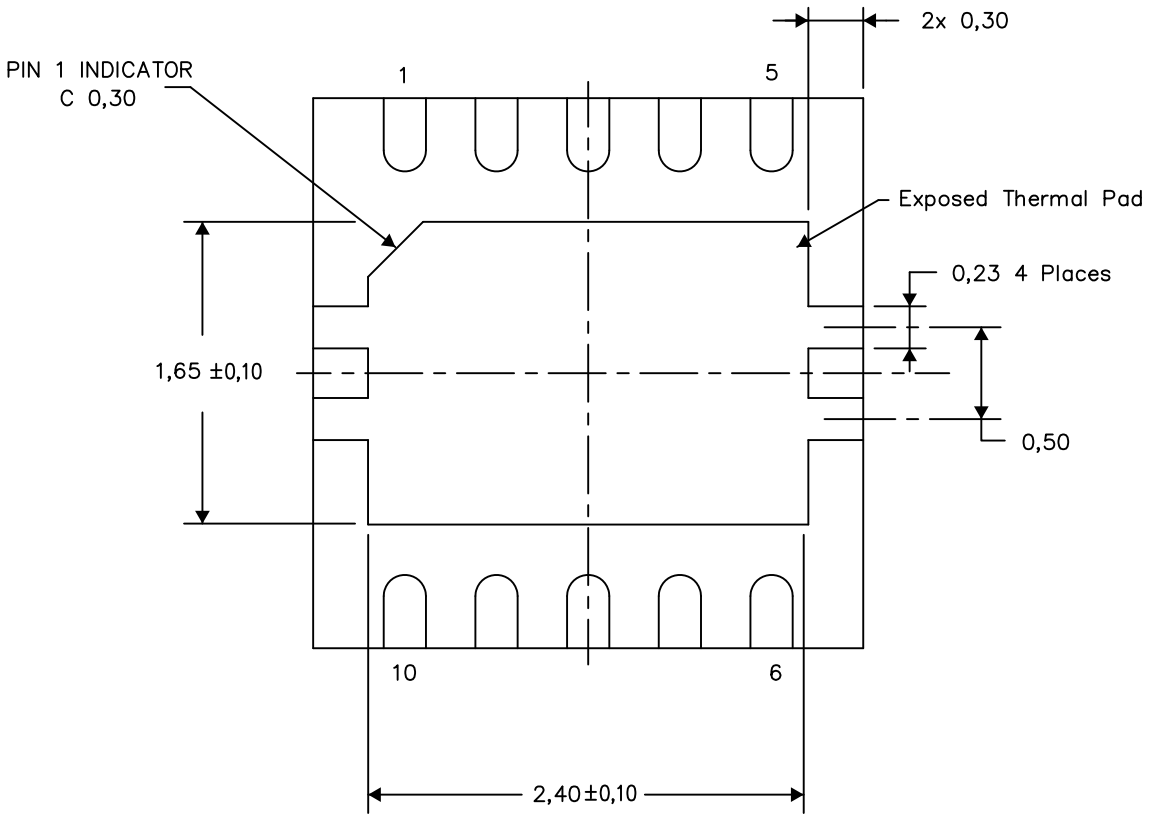
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



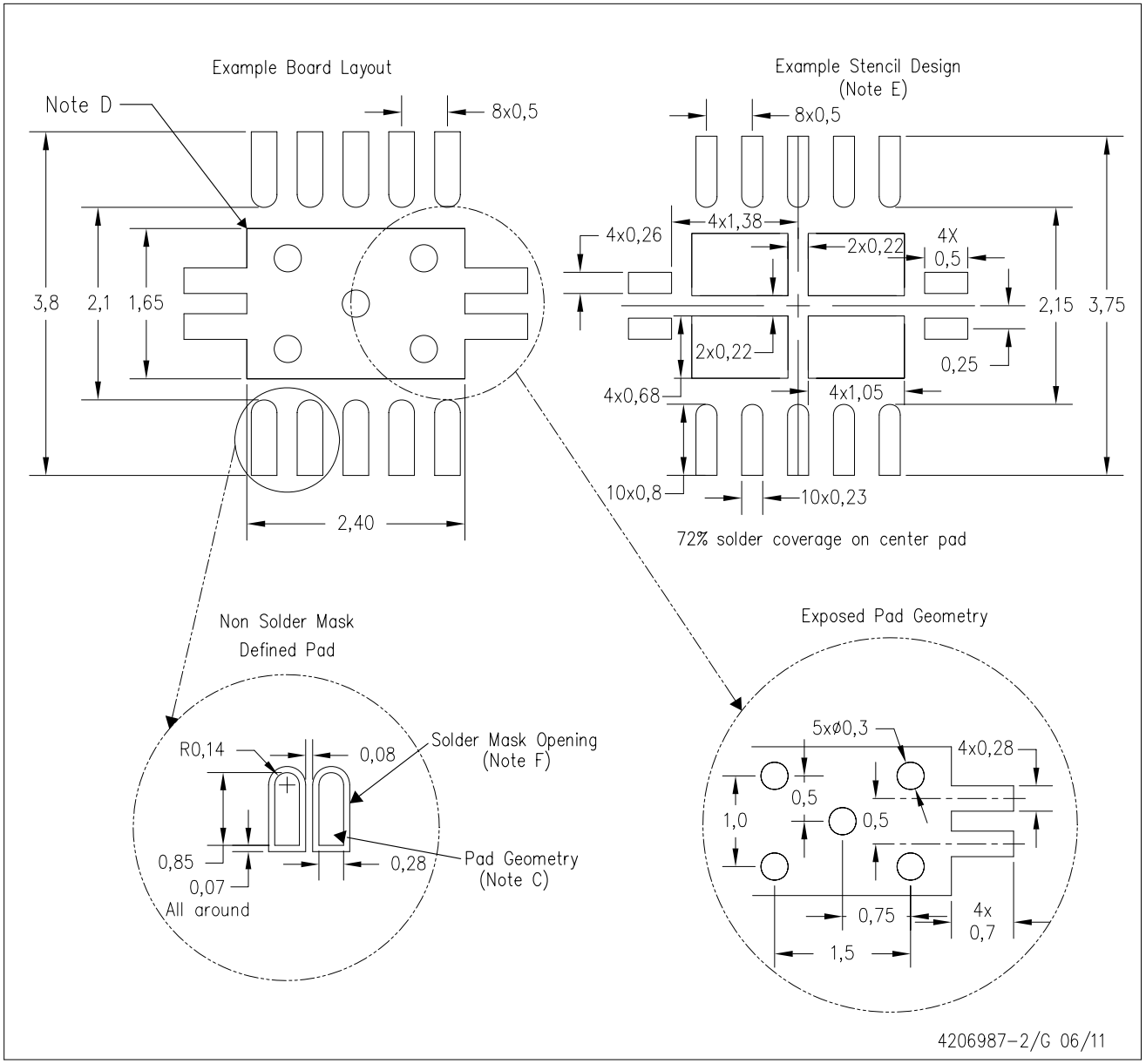
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/N 07/12

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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