DATA SHEET

GPCD6L106A

Multi-Channel Sound Controller with DC-DC Booster

Generalplus

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Version 1.0

Table of Contents

MULTI-CHANNEL SOUND CONTROLLER
WITH DC-DC BOOSTER

1.GENERAL DESCRIPTION

The GPCD6L106A features a 320KB internal ROM, 512-byte working SRAM, three 12-bit timers, 20 general I/Os with multi-channel input and one 14-bit DAC with amplifier. In audio processing, melody and speech can be mixed into one output and it is featured a maximum of two sets of software channels and a high performance SPU voice engine to perform high quality voice function with ADPCM/PCM data. To save more power in the device, GPCD6L106A features a sleep mode to make CPU enter sleep state while not is use. Although in power saving mode, it is able to wake up rapidly if any interrupt source or wakeup IO is triggered. A Serial Peripheral Interface (SPI) controller helps GPCD6L106A to communicate with other devices and components easily and efficiently.

2.FEATURES

- Input Voltage: 1.0V ~ 3.6V
- Programmable pumped voltage:
  (supports up to two sets of DC-DC booster circuits)
  One-battery option: 3.3V ~ 4.2V
  Two-battery option: 3.3V ~ 4.5V
- CPU speed: Max. 8MHz
- F_{OSC} = Max. 16MHz (2 x CPU clock)
- ROM size: Max. 320K bytes
- RAM size: Max. 512 bytes
- Three 12-bit timer/counter, TMA with capture and comparison function, TMB/ TMC with comparison function only (Programmable and Auto Reload)
- Clock sources include external ROSC, internal ROSC or XTAL (option)
- Sleep mode to reduce power consumption

- Key change wakeup function
- IRQs & NMI interrupts
- Watchdog function (option)
- 3.0V/3.3V regulator output (option)
- Low Voltage Reset
- 20-bit programmable general I/Os
- Eight I/Os with high sink current for LED application
- All general IOs with 1M pull-low function to prevent current leakage from false key touch
- One 14-bit DAC with amplifier for direct drive speaker
- SPU (Sound Processing Unit) engine outputs audio data with 14-bit resolution to perform high quality voice/melody
- IR PWM Output
- Hardware PWMIO supports four LED outputs with 256-level brightness control
- Real-time clock
- 4-channel SPU engine with ADPCM/PCM wavetable
- Maximum two sets of 14-bit software channel with noise filter to play high quality sound
- SPI master interface
- Built-in Battery Voltage Detection (BVD) / Low Voltage Detection (LVD) function

3.APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- General purpose controller
- High-end toy controller
- Intelligent education toys
- And more

4.BLOCK DIAGRAM

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┌──────────────────────────────────────────────────────────────────┐
│                                                                    │
│   ┌──────────────────────┐         ┌──────────────────────┐       │──── XI
│   │ 8-Bit controller │ SRAM │  ⇕   │        Clock         │       │
│   │                  │      │       └──────────────────────┘       │──── XO
│   └──────────────────────┘         ┌──────────────────────┐       │
│             ⇕                  ⇕   │    Timer / Counter    │       │
│   ┌──────────────────────┐         └──────────────────────┘       │
│   │        ROM           │  ⇕                                      │
│   └──────────────────────┘     ⇕   ┌──────────────────────┐       │
│   ┌──────────────────────┐         │ SPU/2 software channel│       │
RESETB─│ Regulator/LVR/Porst  │  ⇕       └──────────────────────┘       │
│   └──────────────────────┘                                        │
│   ┌──────────────────────┐     ⇕   ┌──────────────────────┐       │──── AUDP
│   │        SPI           │  ⇕       │  14-Bit Push-Pull DAC │       │
│   └──────────────────────┘         └──────────────────────┘       │──── AUDN
│   ┌──────────────────────┐  ⇕                                      │
│   │       PWMIO          │                                         │
│   └──────────────────────┘                                        │
│   ┌──────────────────────────────────────────────┐               │
│   │      20 General I/O,IOA,IOB,IOD               │               │
│   └──────────────────────────────────────────────┘               │
│          │              │              │                           │
└──────────────────────────────────────────────────────────────────┘
        IOA0~7         IOB0~7         IOD0~3
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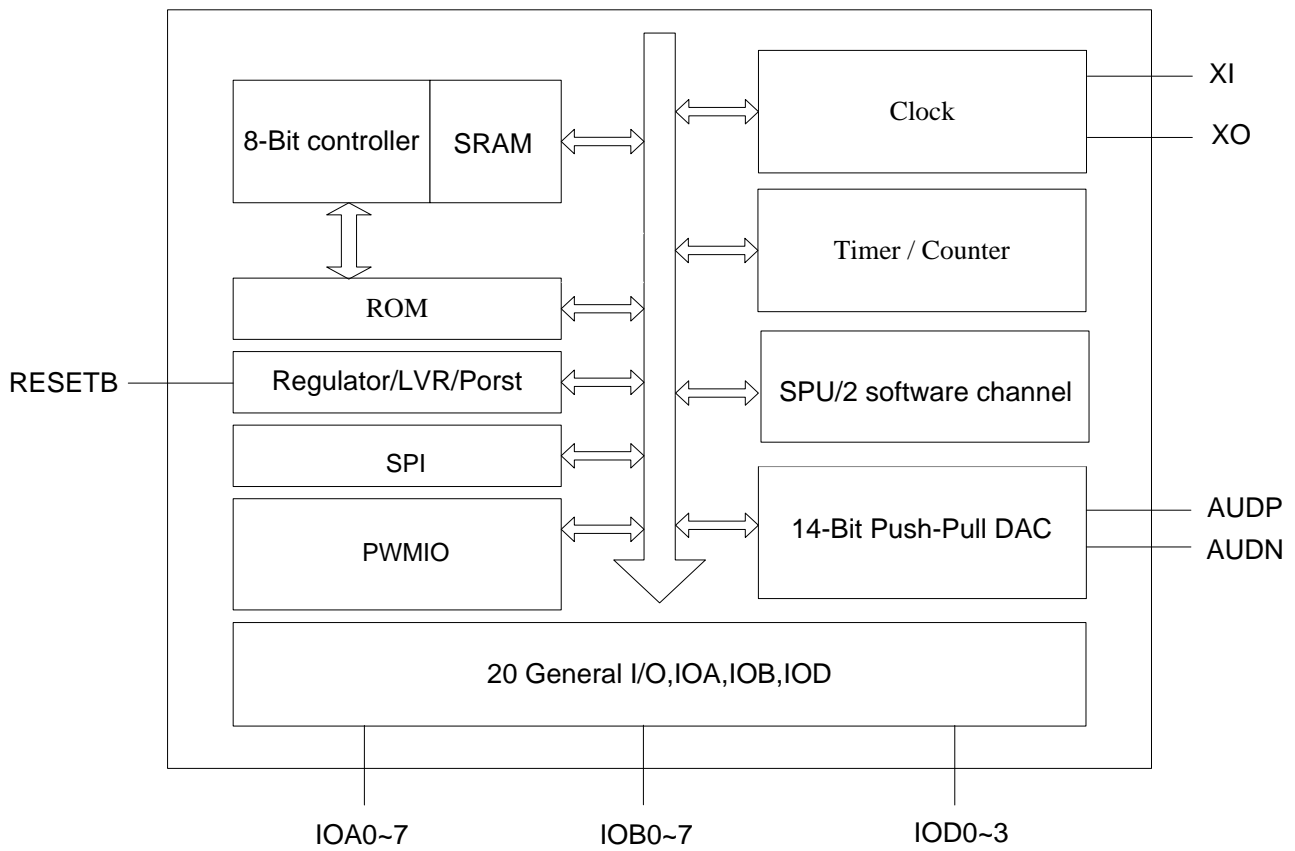
5. SIGNAL DESCRIPTION

Mnemonic	Type	Description	Note
IO PORT			
IOA7-0	I/O	Bi-direction IO port with wakeup function	IOA3-0 high sink
IOB7-0	I/O	Bi-direction IO port with wakeup function	IOB3-0 high sink
IOD3-0	I/O	Bi-direction IO port with wakeup function	
Clock related			
XO	O	Oscillator crystal output	Keep floating at ROSC mode
XI	I	Oscillator crystal input/ROSC input	
Power/Ground PAD			
VDD_IN	P	Power from battery (1.0V~3.6V)	
VSS_IN , VSS_IN2	G	Ground reference for battery	
VDD_DCO1,VDD_DCO2	P	Power output from DC-DC booster (3.3V~4.5V)	VDD_DCO1, VDD_DCO2 are shorted on PCB
VSS_DC1,VSS_DC2, VSS_DC3	G	Ground reference for DC-DC booster output	VSS_DC1, VSS_DC2, VSS_DC3 are shorted on PCB
VDD_RGO	P	Regulator power output	For core power
VDD_RGI	P	Regulator power input	Connect to VDD_DCO1/VDD_DCO2
VDDIO	P	Power for all IO ports (3.3V~4.5V)	VDD_IO cannot be lower than VDD_CORE
VSSIO	G	Ground reference for all IO ports	
VDD_CORE	P	Power for core circuit	Connected to VDD_RGO
VSS_CORE	G	Ground reference for core circuit	
VDD_DAC	P	Power for DAC	Connected to VDD_DCO1/VDD_DCO2
VSS_DAC	G	Ground reference for DAC	
VDD_AMP	P	Power for audio amplifier	Connected to VDD_DCO1/VDD_DCO2
VSS_AMP	G	Ground reference for audio amplifier	
VDD_DRV	P	Power for audio output driver	Connected to VDD_DCO1/VDD_DCO2
VSS_DRV	G	Ground reference for audio output driver	
Others			
RESETB	I	External reset pin (active low)	Internal pull-high
TEST	I	NC for normal application.	Internal pull-low
LX1	I	Inductor connection for DC-DC (1st group)	
LX2	I	Inductor connection for DC-DC (2nd group)	
AUDP	O	Audio output-P	
AUDN	O	Audio output-N	
MICIN	I	Line-In / Microphone input	

6. FUNCTION DESCRIPTIONS

6.1. SRAM

The 512-byte SRAM (including Stack) area is located in 00000h~002FFh.

6.2. ROM

GPCD6L106A is capable of accessing internal 320KB ROM. The ROM area is located in 00840h~4FFFFh.

6.3. Low Voltage Reset

With the Low Power Reset (LVR) function, a reset signal is generated to reset system when the operating voltage drops below LVR level.

6.4. Interrupt

The GPCD6L106A has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls fifteen IRQs and seven NMIs. NMI has higher priority than IRQ, meaning a NMI cannot be interrupted by any RQ.

6.5. Hardware PWMIO

Hardware PWMIO supports four LED outputs from IOB0~3 (or IOA0~3) with brightness control of 256 levels. The clock source of PWMIO can be selected by user's request.

6.6. I/O

The purpose of input and output port is to communicate with other devices. A maximum of 20 programmable I/O ports is built-in for GPCD6L106A, including PortA, PortB, and PortD. All ports are general I/Os with programmable wakeup capability. In addition, these ports also feature some special functions in certain pins. Please refer to following figure for more information about IO's special functions.

6.6.1. I/O Configuration

The following diagram is the I/O schematic.

I/O A, B, D Schematic:
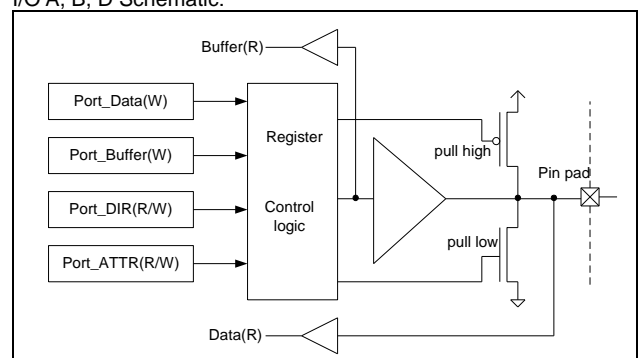
Port_Data and Port_Buffer are written into the same register but reading from different node. To activate key wakeup function, user should latch data on IOX_Data and enable the key wakeup function. Wakeup is triggered when the port's state is different from the latched data.

A summary of IO sharing is listed as follows.

IO Sharing

	IOA								IOB							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
High sink					V	V	V	V					V	V	V	V
PWMIO													V	V	V	V
IR(Output)									V							
External INT										V						
External Clock		V(TMC)	V(TMB)	V(TMA)												
RTC											V	V				
IIS out/in	V(in)	V(in)	V(in)			V(out)	V(out)	V(out)								
QD					V(qd2)	V(qd2)	V(qd1)	V(qd1)								
CC		TMC	TMB	TMA						TMC	TMB	TMA				
1M pull low	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

	IOD			
	Bit3	Bit2	Bit1	Bit0
Wake up	V	V	V	V
SPI	V(rx)	V(tx)	V(ck)	V(cs)
1M pull low	V	V	V	V

*Note: QD means quadrature decoder; CC means Capture/Comparison.

6.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are featured in GPCD6L106A: TimerA, TimerB, and TimerC. These timers are all 12-bit up-counters, a preloaded register, and programmable clock sources. Timer A/B can also be the clock source of the software channel. The clock source of each timer can be set individually. Two clock sources, including CPU clock and external clock, can be selected individual or combination to be timer's clock source. TimerA supports both capture and comparison functions; TimerB and TimerC support comparison function only.

6.8. Sleep, Wakeup, and Watchdog

6.8.1. Sleep and Wakeup

Sleep mode saves power by stopping clock while device is not in use. When entering sleep mode, system runs from operating mode to standby mode. Wakeup from sleep mode is to resume the system back to operating mode.

1) Sleep: after power-on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter sleep mode.

2) Wakeup: When a wakeup source is generated, GPCD6L106A wakes up from sleep mode. While wakeup is completed, program counter will continue to execute the next command where it left from entering the sleep mode.

6.8.2. Watchdog

If the watchdog function is enabled, a reset signal is generated to reset system when watchdog counter is overflow.

6.9. Speech and DAC

The GPCD6L106A adopts a high performance SPU voice engine to achieve 4-channel voice effect with ADPCM/PCM. A hardware multiplier is also embedded in this SPU for software use. Moreover, there is one 14-bit DAC with Class-D amplifier for direct audio output.

6.10. SPI Controller

A Serial Peripheral Interface (SPI) controller is built in GPCD6L106A to facilitate communication with other devices and components. There are four control signals on SPI: SPICSN, SPICLK (SCK), SPIRX (SDI), and SPITX (SDO); these four signals are shared with PortD0, PortD1, PortD2, and PortD3. While SPI module is enabled by corresponding control bits, these four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are presented as follows:
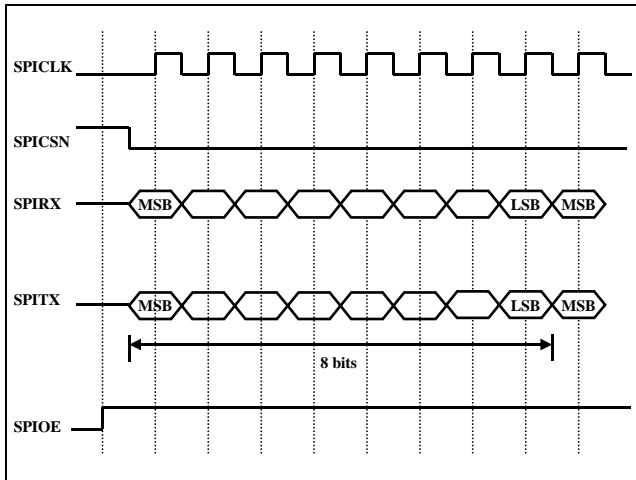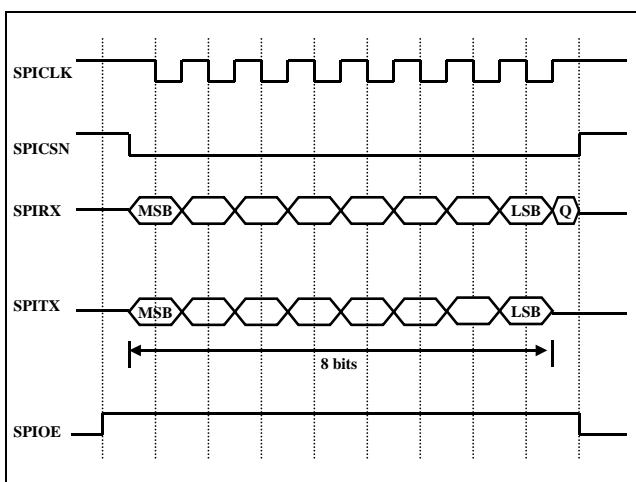
GPCD6L106A

Master Mode, SPO = 0, SPH=0
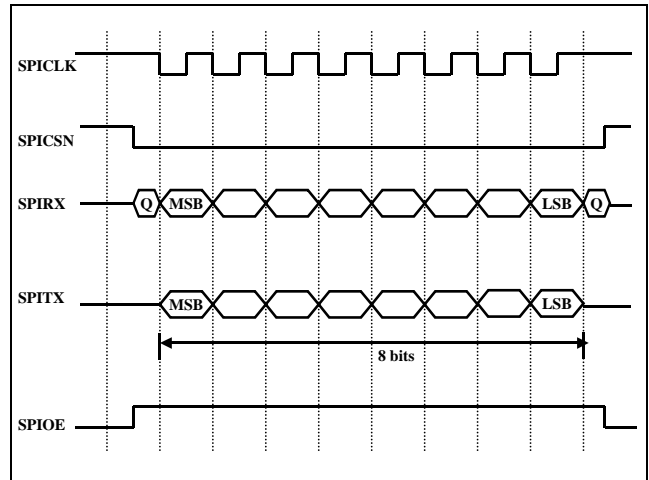
Master Mode, SPO = 1, SPH=1
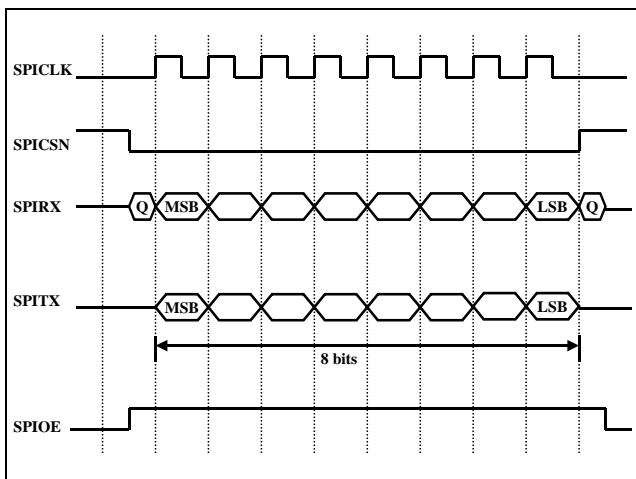
Master Mode, SPO = 0, SPH=1

Master Mode, SPO = 1, SPH=0

6.11. DC-DC Booster

The GPCD6L106A can be supplied wide input voltage (1.0V~3.6V) and work with a programmable pumped voltage. Inside the chip, up to two sets of high efficient DC-DC booster circuits are built in. The DC-DC booster circuit pumps input voltage to 3.3V~4.5 that is able to supply the power for system's working voltage.

6.12. Battery Voltage Detect / Low Voltage Detect

The GPCD6L106A features a Battery Voltage Detect (BVD) function and the battery voltage level can be read back by program. Furthermore, user can set low voltage level and obtain the Low Voltage Detect (LVD) flag by program.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device.   For normal operational conditions see DC Electrical Characteristics.

7.2. AC Characteristics (TA = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC}	-	16	-	MHz	VDD_IN = 1.0V - 3.6V
Fosc deviation by process	△F/F	-2	-	2	%	(Fosc(VDD_CORE)-16Mhz)/16MHz, VDD_CORE =3.0V, For Internal OSC
		-7	-	7	%	(Fosc(VDD_CORE)-16Mhz)/16MHz, VDD_CORE =3.0V, For external ROSC, R=33KΩ

7.3. Power Characteristics

7.3.1. One battery selected, TA = 25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VDD_IN	1.0	-	-	V	I(VDD_DCO)=80mA@VDD_DCO=3.3V I(VDD_DCO)=30mA@VDD_DCO=4.2V L=15uH/0.5W (Color Code Inductance) Under two sets DCDC condition
Input Voltage (Max.)	VDD_IN	-	-	1.8	V	
Operating Voltage** (pump voltage)	VDD_DCO	3.3	-	4.2	V	
Operating Current-1	I_{OP-1}	-	20	-	mA	VDD_IN=1.5V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC on, no load
		-	30	-	mA	VDD_IN=1.5V, VDD_DCO=4.2V F_{CPU} = 8MHz , DAC on, no load
Operating Current-2	I_{OP-2}	-	13	-	mA	VDD_IN=1.5V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC off, no load
		-	20	-	mA	VDD_IN=1.5V, VDD_DCO=4.2V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	5.0	μA	VDD_IN = 1.5V
Battery Voltage Detect	V_{BVD}	V_{BVD} -10%	V_{BVD}	V_{BVD} +10%	V	V_{BVD}.=0.9V+0.1V*N ;Nn=0~6

*As I(VDD_DCO) is greater than the value of test condition; VDD_DCO can be observed voltage drop.

**VDD_DCO is the pumped voltage.   It is greater than or equal to input voltage.   It is possible to be lower with heavy loading under operating.

7.3.2. Two battery selected, TA = 25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage (Min.) *	VDD_IN	1.3	-	-	V	I(VDD_DCO)=40mA@VDD_DCO=3.3V

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
		-	-	-		I(VDD_DCO)=15mA@VDD_DCO=4.5V L=15uH/0.5W (Color Code Inductance) Under two sets DCDC condition
Input Voltage (Max.)	VDD_IN	-	-	3.6	V	
Operating Voltage**	VDD_DCO	3.3	-	4.5		
Operating Current-1	I_{OP-1}	-	10	-	mA	VDD_IN=3.0V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC on, no load
		-	15	-	mA	VDD_IN=3.0V, VDD_DCO=4.5V F_{CPU} = 8MHz , DAC on, no load
Operating Current-2	I_{OP-2}	-	6	-	mA	VDD_IN=3.0V, VDD_DCO=3.3V F_{CPU} = 8MHz , DAC off, no load
		-	9	-	mA	VDD_IN=3.0V, VDD_DCO=4.5V F_{CPU} = 8MHz , DAC off, no load
Standby Current	I_{STBY}	-	-	10.0	μA	VDD15 = 3.0V
Battery Voltage Detect	V_{BVD}	V_{BVD} -10%	V_{BVD}	V_{BVD} +10%	V	V_{BVD}=1.8V+0.2V*N ;Nn=0~6

*As I(VDD_DCO) is larger than the value of test condition; VDD_DCO can be observed voltage drop.

**VDD_DCO is the pumped voltage.   It is greater than or equal to input voltage.   It is possible to be lower with heavy loading under operating.

7.4. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VDD_RGI	2.3	-	5.5	V	
Maximum Current Output	I_{VDD_RGO}	-	-	30	mA	VDD5V (Regulator in)= 4.5V, △VDD (Regulator out) <100mV
Output Voltage	VDD_RGO	2.7	3.0	3.3	V	VDD_REG > 3.4V and V33_REG is 3.0V
Standby Current	I_{RGES}	-	5	-	uA	VDD5V (Regulator in)= 3.0V

7.5. DC Characteristics

7.5.1. VDD_IO=3.3V, TA=25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input High Level	V_{IH}	0.7*VDD_IO	-	VDD_IO	V	-
Input Low Level	V_{IL}	VSS_IO	-	0.3*VDD_IO	V	-
Output High Current (IOA[7:0]/IOB[7:0]/IOD[7:0])	I_{OH}	-	6	-	mA	VDD_IO =3.3V, V_{OH} =0.7*VDD_IO
Output Low Sink Current (IOA[7:4]/IOB[7:4]/IOD[7:0])	I_{OL1}	-	9	14	mA	VDD_IO =3.3V, V_{OL} =0.3*VDD_IO
Output Low Sink Current (IOA[3:0]/IOB[3:0])	I_{OL2}	-	18	27	mA	VDD_IO =3.3V, V_{OL} =0.3*VDD_IO
Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL}	70	100	130	Kohm	VDD_IO =3.3V, V_{in} =VDD_IO
High Impedance Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL2}	595	850	1105	Kohm	VDD_IO =3.3V, V_{in} =VDD_IO
Input Pull-High Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PH}	70	100	130	Kohm	VDD_IO =3.3V, V_{in} =VSS_IO

7.5.2. VDD_IO =4.5V, TA=25℃

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input High Level	V_{IH}	0.7*VDD_IO	-	VDD_IO	V	-
Input Low Level	V_{IL}	VSS_IO	-	0.3*VDD_IO	V	-
Output High Current (IOA[7:0]/IOB[7:0]/IOD[7:0])	I_{OH}	-	10	-	mA	VDD_IO =4.5V, V_{OH} =0.7*VDD_IO
Output Low Sink Current (IOA[7:4]/IOB[7:4]/ IOD[7:0])	I_{OL1}	-	16	24	mA	VDD_IO =4.5V, V_{OL} =0.3*VDD_IO
Output Low Sink Current (IOA[3:0]/IOB[3:0])	I_{OL2}	-	31	47	mA	VDD_IO =4.5V, V_{OL} =0.3*VDD_IO
Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL1}	70	100	130	Kohm	VDD_IO =4.5V, V_{in} =VDD_IO
High Impedance Input Pull-Low Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PL2}	595	850	1105	Kohm	VDD_IO =4.5V, V_{in} =VDD_IO
Input Pull-High Resistor (IOA[7:0]/IOB[7:0]/IOD[7:0])	R_{PH}	70	100	130	Kohm	VDD_IO =4.5V, V_{in} =VSS_IO

7.6. DAC Characteristics

7.6.1. One battery selected, VDD_IN=1.5V VDD_DCO=3.3V, R_L=8Ω, f=1KHz, TA=25℃

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	Bit
THD+n (3.3V@0.175W)	-	-	0.4	-	%
Noise at No Signal	-	-	-84	-	dBr A
Dynamic Range(-60dB)	-	-	-78	-	dBr A

7.6.2. Two battery selected, VDD_IN=3.0V VDD_DCO=4.5V, R_L=8Ω, f=1KHz, TA=25℃

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	Bit
THD+n (4.5V@0.35W)	-	-	0.3	-	%
Noise at No Signal	-	-	-84	-	dBr A
Dynamic Range(-60dB)	-	-	-75	-	dBr A

7.7. Pump Efficiency

7.7.1. One battery selected, VDD_IN=1.5V, T_A = 25℃

a. Two sets DCDC

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency (L=15uH/0.5W)	Eff.	-	80	-	%	I(VDD_DCO)=30mA; VDD_DCO=3.3V
		-	70	-	%	I(VDD_DCO)=100mA; VDD_DCO=3.3V

*Use Color Code Inductance

b. One set DCDC

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency	Eff.	-	80	-	%	I(VDD_DCO)=30mA; VDD_DCO=3.3V
(L=15uH/0.5W)		-	70	-	%	I(VDD_DCO)=60mA; VDD_DCO=3.3V

*Use Color Code Inductance

7.7.2. Two battery selected, VDD_IN=3.0V, T$_A$ = 25℃

a. Two sets DCDC

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency	Eff.	-	81	-	%	I(VDD_DCO)=50mA; VDD_DCO=4.5V
(L=15uH/0.5W)		-	75	-	%	I(VDD_DCO)=200mA; VDD_DCO=4.5V

*Use Color Code Inductance

b. One set DCDC

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency	Eff.	-	81	-	%	I(VDD_DCO)=50mA; VDD_DCO=4.5V
(L=15uH/0.5W)		-	75	-	%	I(VDD_DCO)=100mA; VDD_DCO=4.5V

*Use Color Code Inductance

7.7.3. Two battery selected, VDD_IN=2.0V, T$_A$ = 25℃, One set DCDC

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Pump Efficiency(L=15uH/0.5W)	Eff.	-	65	-	%	I(VDD_DCO)=100mA; VDD_DCO=3.3V

*Use Color Code Inductance

7.8. VDD_IN v.s. Supplied Current (I(VDD_DCO))

7.8.1. One battery selected, TA = 25℃

a. Two sets DCDC

VDD_IN (V)	I(VDD_DCO) (mA)	Condition
1.0	80	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
1.2	130	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
1.5	200*	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)

*The max measured current of I(VDD_DCO) is 200mA only.

b. One set DCDC

VDD_IN (V)	I(VDD_DCO) (mA)	Condition
1.0	40	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
1.2	60	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
1.5	90	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)

7.8.2. Two battery selected, TA = 25℃

a. Two sets DCDC

VDD_IN (V)	I(VDD_DCO) (mA)	Condition
1.5	10	VDD_DCO=4.5V ; L=15uH/0.5W (Color Code Inductance)
2.4	200*	VDD_DCO=4.5V ; L=15uH/0.5W (Color Code Inductance)

*The max measured current of I(VDD_DCO) is 200mA only.

b. One set DCDC

VDD_IN (V)	I(VDD_DCO) (mA)	Condition
1.5	10	VDD_DCO=4.5V ; L=15uH/0.5W (Color Code Inductance)
2.4	150	VDD_DCO=4.5V ; L=15uH/0.5W (Color Code Inductance)
3.0	200*	VDD_DCO=4.5V ; L=15uH/0.5W (Color Code Inductance)

*The max measured current of I(VDD_DCO) is 200mA only.

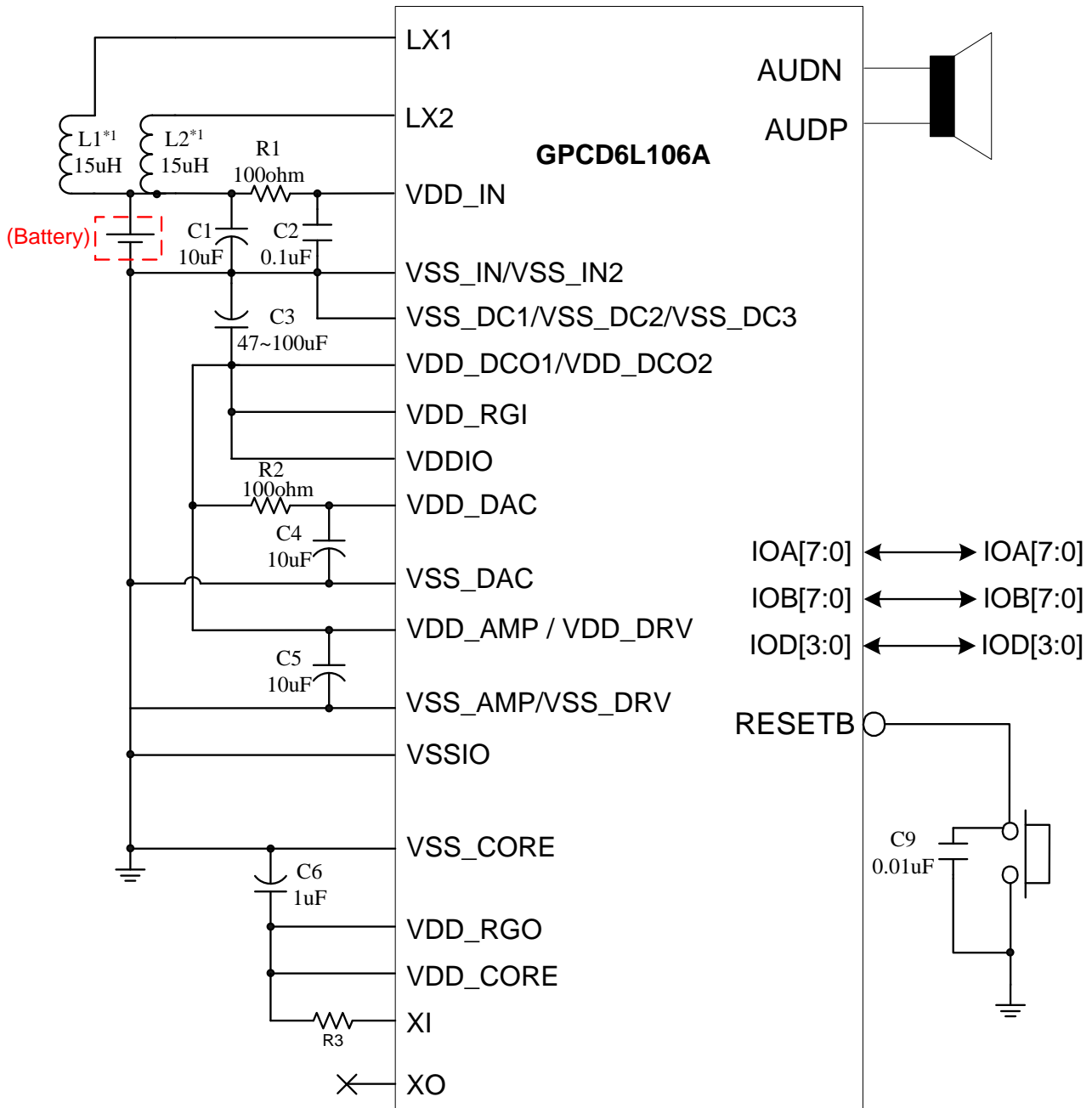| VDD_IN (V)	I(VDD_DCO) (mA)	Condition
1.5	90	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
1.8	160	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)
2.4	200*	VDD_DCO=3.3V ; L=15uH/0.5W (Color Code Inductance)

*The max measured current of I(VDD_DCO) is 200mA only.

7.9. The Relationship between R_{OSC} and F_{OSC} (TA=25℃)
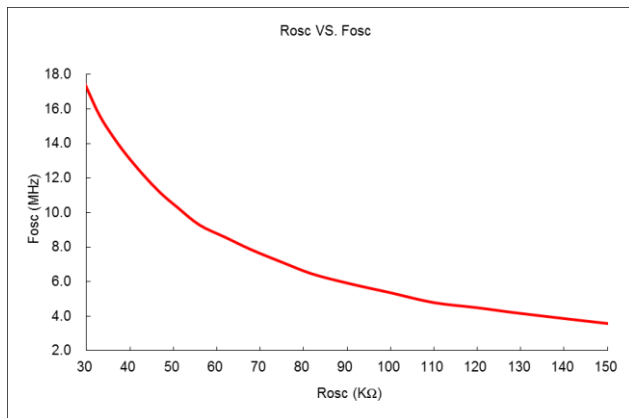
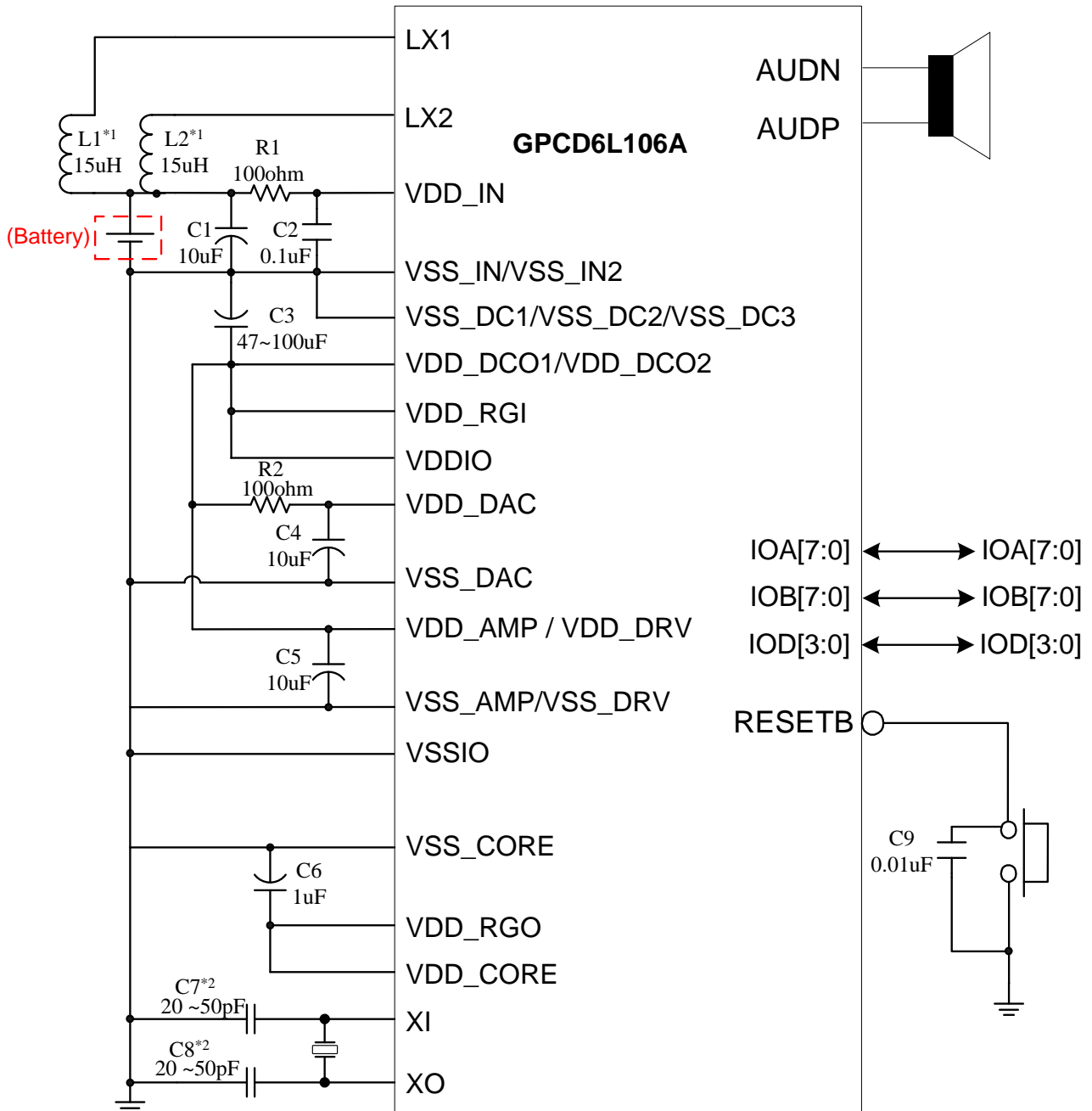## 8.APPLICATION CIRCUITS

8.1. GPCD6L106A Application Circuit with External R_{OSC}-Mode

Note:

1. L1 and L2 should be as close as to VDD_IN/LX1/LX2 as possible. Please use inductance with lower resistance to gain higher efficiency. **15uH/0.5W@IDC(max)>250mA, ESR<1.5ohm is recommended.**

2. The value of C3 is dependent on the loading of application. In general, 47uF should be enough. C3 should be as close as possible to VDD_DCO1/VDD_DCO2.

3. C4 should be as close as possible to VDD_DAC/VSS_DAC.

4. C5 should be as close as possible to VDD_AMP/VDD_DRV and VSS_AMP/VSS_DRV.

5. The capacitance of C9 cannot be large than 0.01uF.

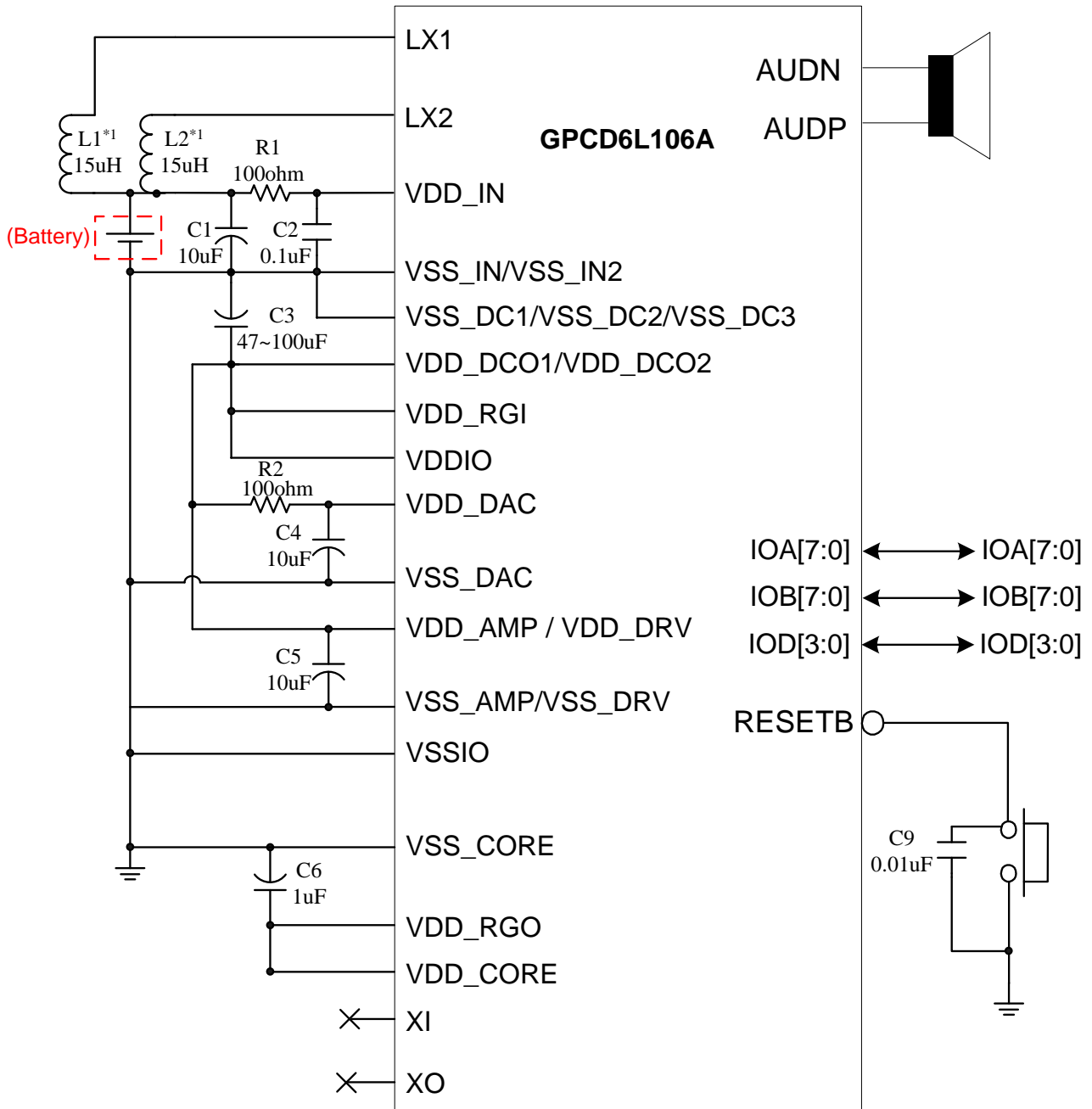## 8.2. GPCD6L106A Application Circuit with XTAL-Mode

Note:

1. L1 and L2 should be as close as to VDD_IN/LX1/LX2 as possible. Please use inductance with lower resistance to gain higher efficiency. **15uH/0.5W@IDC(max)>250mA, ESR<1.5ohm is recommended.**

2. The values of C7/C8 are for design guidance only; different values may be needed for different crystal/resonator used.

3. The value of C3 is dependent on the loading of application. In general, 47uF should be enough. C3 should be as close as possible to VDD_DCO1/VDD_DCO2.

4. C4 should be as close as possible to VDD_DAC/VSS_DAC.

5. C5 should be as close as possible to VDD_AMP/VDD_DRV and VSS_AMP/VSS_DRV.

6. The capacitance of C9 can not be large than 0.01uF.

8.3. GPCD6L106A Application Circuit with Internal R$_{OSC}$-Mode
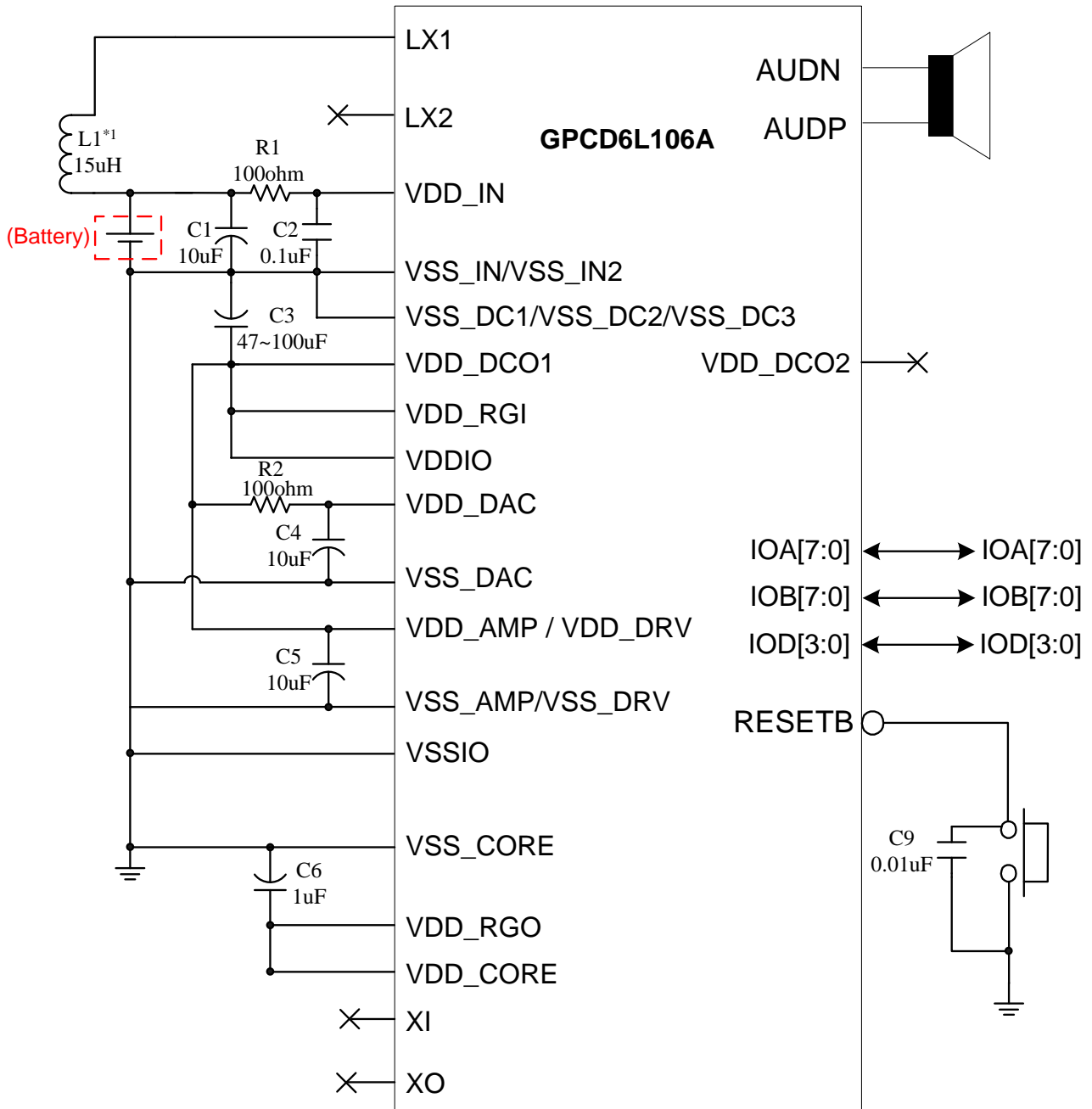

Note:

1. L1 and L2 should be as close as to VDD_IN/LX1/LX2 as possible. Please use inductance with lower resistance to gain higher efficiency. **15uH/0.5W@IDC(max)>250mA, ESR<1.5ohm is recommended.**

2. The value of C3 is dependent on the loading of application. In general, 47uF should be enough. C3 should be as close as possible to VDD_DCO1/VDD_DCO2.

3. C4 should be as close as possible to VDD_DAC/VSS_DAC.

4. C5 should be as close as possible to VDD_AMP/VDD_DRV and VSS_AMP/VSS_DRV.

5. The capacitance of C9 cannot be large than 0.01uF.

GPCD6L106A

8.4. GPCD6L106A One set DCDC Application Circuit with Internal R$_{OSC}$-Mode

Note:

1. L1 should be as close to VDD_IN/LX1 as possible. Please use inductance with lower resistance to gain higher efficiency. **15uH/0.5W@IDC(max)>250mA, ESR<1.5ohm is recommended.**
2. The value of C3 is dependent on the loading of application. In general, 47uF should be enough. C3 should be as close as possible to VDD_DCO1/VDD_DCO2. Furthermore, VDD_DCO2 does not need to be bonded.
3. C4 should be as close as possible to VDD_DAC/VSS_DAC.
4. C5 should be as close as possible to VDD_AMP/VDD_DRV and VSS_AMP/VSS_DRV.
5. The capacitance of C9 cannot be large than 0.01uF.
6. **Using one set DCDC, the driving ability is lower than two set DCDC. Users need to make sure the current consumption is enough.**

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCD6L106A-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Feb. 24, 2015	1.0	Release to 1.0	20
Dec. 08, 2014	0.1	Original	16