FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22113-3E

ASSP Communication Network
CMOS

LAN Controller with PC Card, ISA Bus, and General-purpose Bus Interfaces

MB86967

■ DESCRIPTION

The MB86967 is a highly-integrated, high-performance single-chip Ethernet LAN controller which contains a PC card interface based on the JEIDA4.2 standard, an ISA bus interface that can be connected directly to the ISA bus, a general-purpose bus interface, a Manchester encoder/decoder based on the IEEE802.3 standard, and 10BASE-T transceiver.

The LAN controller and buffer manager are software compatible with the MB86965A and MB86964. The buffer manager has functions for arbitration and buffer management of external buffer memory (SRAM) which can be expanded to 32 KB. These functions provide simultaneous access from the host and data link controller and updating of transmit and receive buffer pointers. This permits substantial reduction of software overhead in buffer management.

The Manchester encoder/decoder and 10BASE-T transceiver can be easily interfaced with twisted-pair cable just by addition of a pulse transformer and filter.

Mode pin setting allows the system interface to switch between the PC card interface, ISA bus interface, and general-purpose bus interface. When in the ISA bus interface mode, two modes can be selected: a jumperless mode allowing software setting of I/O addresses and interrupt signals, and a jumper mode allowing DIPswitch setting.

■ FEATURES

System Interface

- Allows switching between PC card interface, ISA bus interface, and general-purpose bus interface
- Allows byte swapping of word data according to host CPU (in ISA bus mode and general-purpose bus mode)

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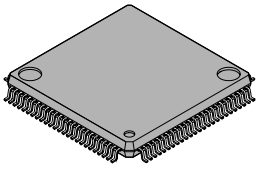
■ PACKAGE

100-pin Plastic LQFP



(FPT-100P-M05)

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- Has functions for high-speed burst DMA transfer and single DMA transfer (slave operation) (in ISA bus mode and general-purpose bus mode)
- Provides node ID EEPROM interface (in ISA bus mode)
- Allows software setting of I/O addresses and interrupt signals (in jumperless mode of ISA bus mode)
- Can be connected to 8-bit and 16-bit standard microprocessor buses (in general-purpose bus mode)
- Provides JEIDA protocol interface (in PC card mode)
- Has overlapping address window function (in PC card mode)
- Has memory control (common memory, attribute memory, I/O addresses) (in PC card mode)

LAN Interface

- Contains Manchester encoder/decoder based on IEEE802.3 standard and 10BASE-T transceiver
- Has functions for jabber control, link test, and SQE test
- Has functions for inversion detection and automatic correction
- Contains LED driver for monitoring network status (link test, collision, transmitting and receiving)
- Has function for 10BASE-T external loopback (full-duplex)

Controller

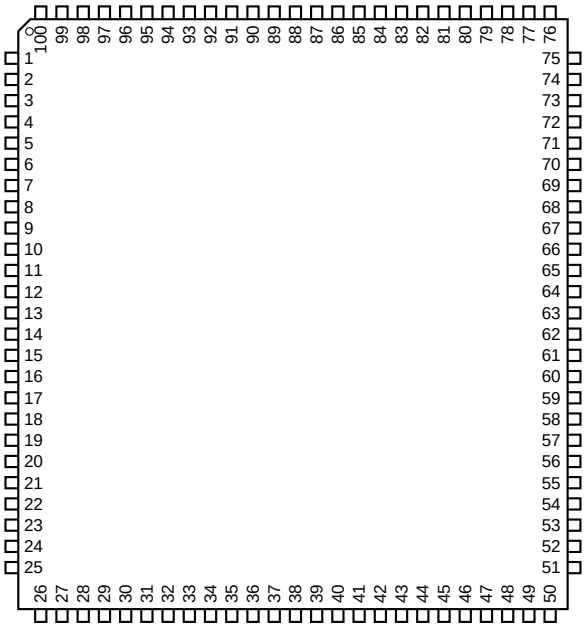
- Software compatible with MB86965A and MB86964
- Has dual-bank transmit buffer and ring receive buffer (expandable to 32 KB) set by program
- Contains 64-bit hash table for multicast address filter
- Has function for removing receive long packets (1792-byte or more receive packets)
- Has two power-down modes; standby mode (continued crystal oscillation) and shut-down mode (stopped crystal oscillation)

Others

- Aluminum two-layer wiring CMOS technology
- 100-pin LQFP package
- Power-supply voltage of 5 V ±5%

■ PIN ASSIGNMENT

(Top view)



(FPT-100P-M05)

• **PC card mode**

Pin no.	Symbol	I/O	Pin no.	Symbol	I/O	Pin no.	Symbol	I/O	Pin no.	Symbol	I/O
1	$V_{DD}1$	P	26	$V_{DD}2$	P	51	$V_{DD}3$	P	76	GNDA2	G
2	$\overline{INPACK}$	O	27	PD11	BD	52	MODE0/LEDL	IU/OD	77	TPOPB	O
3	$\overline{WAIT}$	O	28	PD4	BD	53	BA6	O	78	TPOPA	O
4	PA0	ID	29	PD3	BD	54	BA5	O	79	TPONA	O
5	PA1	ID	30	$\overline{BCS}$	O	55	BA4	O	80	TPONB	O
6	PA2	ID	31	GND3	G	56	BA3	O	81	VDDA2	P
7	PA3	ID	32	$\overline{BWE}$	O	57	GND5	G	82	$\overline{CE1}$	IU
8	PA4	ID	33	$\overline{BOE}$	O	58	BA2	O	83	$\overline{CE2}$	IU
9	PA5	ID	34	BD7	B	59	BA1	O	84	$\overline{IOIS16}$	O
10	PA6	ID	35	BD6	B	60	BA0	O	85	PD10	BD
11	PA7	ID	36	BD5	B	61	CLKO	O	86	GND6	G
12	PA8	ID	37	BD4	B	62	CLKI	I	87	PD2	BD
13	PA9	ID	38	BD3	B	63	RESET2	ISD	88	PD9	BD
14	PA10	ID	39	BD2	B	64	RESET1	ISU	89	PD1	BD
15	$\overline{IORD}$	IU	40	BD1	B	65	LEDR	OD	90	PD8	BD
16	GND1	G	41	BD0	B	66	LEDT	OD	91	PD0	BD
17	$\overline{IOWR}$	IU	42	BA14	O	67	GNDA1	G	92	$\overline{IREQ}$	O
18	PD15	BD	43	BA13	O	68	LEDC	OD	93	$\overline{REG}$	IU
19	PD14	BD	44	BA12	O	69	NC0	—	94	$V_{DD}4$	P
20	PD7	BD	45	BA11	O	70	VDDA1	P	95	$\overline{WE}$	IU
21	PD13	BD	46	GND4	G	71	TPIP	I	96	$\overline{OE}$	IU
22	PD6	BD	47	BA10	O	72	TPIN	I	97	ROMAD	O
23	PD12	BD	48	BA9	O	73	GNDM	I	98	$\overline{ROMS}$	O
24	GND2	G	49	BA8	O	74	NC1	—	99	$\overline{ROMRD}$	O
25	PD5	BD	50	BA7	O	75	NC2	—	100	GND7	G

I: Input ID: Input with pull-down resistor IS: Schmitt input P: Power supply
O: Output BD: Input/output with pull-down resistor IU: Input with pull-up resistor G: Ground
B: Input/output OD: Open-drain output

• **ISA bus mode**

Pin no.	Symbol	I/O	Pin no.	Symbol	I/O	Pin no.	Symbol	I/O	Pin no.	Symbol	I/O
1	$V_{DD}1$	P	26	$V_{DD}2$	P	51	$V_{DD}3$	P	76	GNDA2	G
2	DREQ	O	27	SD11	BD	52	LEDL	OD	77	TPOPB	O
3	IOCHRDY	OD	28	SD4	BD	53	BA6	O	78	TPOPA	O
4	SA0	ID	29	SD3	BD	54	BA5	O	79	TPONA	O
5	SA1	ID	30	$\overline{BCS}$	O	55	BA4	O	80	TPONB	O
6	SA2	ID	31	GND3	G	56	BA3	O	81	VDDA2	P
7	SA3	ID	32	$\overline{BWE}$	O	57	GND5	G	82	$\overline{SBHE}$	IU
8	SA4	ID	33	$\overline{BOE}$	O	58	BA2	O	83	$\overline{DMACK}$	IU
9	SA5	ID	34	BD7	B	59	BA1	O	84	$\overline{IOIS16}$	OD
10	SA6	ID	35	BD6	B	60	BA0	O	85	SD10	BD
11	SA7	ID	36	BD5	B	61	CLKO	O	86	GND6	G
12	SA8	ID	37	BD4	B	62	CLKI	I	87	SD2	BD
13	SA9	ID	38	BD3	B	63	AEN	ISD	88	SD9	BD
14	ALE	ID	39	BD2	B	64	CHRESET	ISU	89	SD1	BD
15	$\overline{IOR}$	IU	40	BD1	B	65	EOP	ID	90	SD8	BD
16	GND1	G	41	BD0	B	66	LEDT	OD	91	SD0	BD
17	$\overline{IOW}$	IU	42	BA14	O	67	GNDA1	G	92	IREQ0	O
18	SD15	BD	43	BA13	O	68	LEDC	OD	93	$\overline{ENHB}$	O
19	SD14	BD	44	BA12	O	69	IREQ1/IOSEL0	IU/O	94	$V_{DD}4$	P
20	SD7	BD	45	BA11	O	70	VDDA1	P	95	$\overline{ENLB}$	O
21	SD13	BD	46	GND4	G	71	TPIP	I	96	EEPDO	IU
22	SD6	BD	47	BA10	O	72	TPIN	I	97	EEPDI	O
23	SD12	BD	48	BA9	O	73	MODE/LEDR	I/OD	98	EEPCS	O
24	GND2	G	49	BA8	O	74	IREQ2/IOSEL1	IU/O	99	EEPSK	O
25	SD5	BD	50	BA7	O	75	IREQ3/IOSEL2	IU/O	100	GND7	G

I: Input ID: Input with pull-down resistor IS: Schmitt input P: Power supply
O: Output BD: Input/output with pull-down resistor IU: Input with pull-up resistor G: Ground
B: Input/output OD: Open-drain output

• **General-purpose bus mode**

Pin no.	Symbol	I/O	Pin no.	Symbol	I/O	Pin no.	Symbol	I/O	Pin no.	Symbol	I/O
1	$V_{DD}1$	P	26	$V_{DD}2$	P	51	$V_{DD}3$	P	76	GNDA2	G
2	DREQ	O	27	SD11	BD	52	MODE0	IU	77	TPOPB	O
3	READY	O	28	SD4	BD	53	BA6	O	78	TPOPA	O
4	SA0	ID	29	SD3	BD	54	BA5	O	79	TPONA	O
5	SA1	ID	30	$\overline{BCS}$	O	55	BA4	O	80	TPONB	O
6	SA2	ID	31	GND3	G	56	BA3	O	81	VDDA2	P
7	SA3	ID	32	$\overline{BWE}$	O	57	GND5	G	82	$\overline{ECS}$	I
8	MODE1	ID	33	$\overline{BOE}$	O	58	BA2	O	83	N.C	—
9	N.C	—	34	BD7	B	59	BA1	O	84	N.C	—
10	RDYPOL	ID	35	BD6	B	60	BA0	O	85	SD10	BD
11	$\overline{BHE}$	ID	36	BD5	B	61	CLKO	O	86	GND6	G
12	$\overline{DMACK}$	ID	37	BD4	B	62	CLKI	I	87	SD2	BD
13	EOP	ID	38	BD3	B	63	N.C	—	88	SD9	BD
14	N.C	—	39	BD2	B	64	HWRST	ISU	89	SD1	BD
15	$\overline{IOR}$	Iu	40	BD1	B	65	LEDR	OD	90	SD8	BD
16	GND1	G	41	BD0	B	66	N.C	—	91	SD0	BD
17	$\overline{IOW}$	Iu	42	BA14	O	67	GNDA1	G	92	$\overline{INT}$	O
18	SD15	BD	43	BA13	O	68	N.C	—	93	LEDT	OD
19	SD14	BD	44	BA12	O	69	N.C	—	94	$V_{DD}4$	P
20	SD7	BD	45	BA11	O	70	VDDA1	P	95	LEDL	OD
21	SD13	BD	46	GND4	G	71	TPIP	I	96	LEDC	OD
22	SD6	BD	47	BA10	O	72	TPIN	I	97	N.C	—
23	SD12	BD	48	BA9	O	73	GNDM	G	98	$\overline{SB}$/SW	O
24	GND2	G	49	BA8	O	74	N.C	—	99	N.C	—
25	SD5	BD	50	BA7	O	75	N.C	—	100	GND7	G

I: Input ID: Input with pull-down resistor IS: Schmitt input P: Power supply
O: Output BD: Input/output with pull-down resistor IU: Input with pull-up resistor G: Ground
B: Input/output OD: Open-drain output

■ PIN DESCRIPTION

• **System interface pins in PC card mode**

Pin no.	Symbol	Pin name	I/O	Function
18 to 23, 25, 27 to 29, 85, 87 to 91	PD0 to PD15	PC CARD DATA BUS	BD	PD15 for most significant bit and PD0 for least significant bit. A built-in 150-kΩ pull-down resistor eliminates the need for any resistor on the card.
4 to 14	PA0 to PA10	PC CARD ADDRESS BUS	ID	PA10 for most significant bit and PA0 for least significant bit. PA0 is invalid at word access. A built-in 150-kΩ pull-down resistor eliminates the need for any resistor on the card.
82	$\overline{CE1}$	CARD ENABLE 1,2	IU	$\overline{CE1}$ controls even addresses and $\overline{CE2}$ controls odd addresses. At power-on or after reset-canceling, these pins must be kept High for 20 ms to initialize the I/O card.
83	$\overline{CE2}$			
96	$\overline{OE}$	OUTPUT ENABLE	IU	This pin is used to control the output of read data from attribute memory space.
95	$\overline{WE}$	WRITE ENABLE	IU	This pin is used to control a write operation to attribute memory space.
93	$\overline{REG}$	REGISTER SELECT	IU	This pin must be kept Non-active High at access to common memory. Keeping this pin Low accesses attribute memory by $\overline{OE}$/$\overline{WE}$. The I/O area is accessed by $\overline{IORD}$/$\overline{IOWE}$. Attribute memory is allocated only to even addresses. Therefore, for word access, data signals PD0 to PD7 are valid and PD8 to PD15 are invalid. Access to odd addresses is disabled at byte access. When setting $\overline{IORD}$/$\overline{IOWE}$ Low during DMA operation, $\overline{REG}$ must be kept High to prevent illegal access.
64	RESET1	HARDWARE RESET1 (Active High)	ISU	This pin is used to clear the card configuration register (CCR), set the card to an unset state (IC card interface mode), and initialize the pointers and registers in the LAN controller and 10BASE-T transceiver. When power is applied to the card, the system must keep this pin High or high-impedance for 1 ms after the power supply has stabilized. A built-in 150-kΩ pull-down resistor eliminates the need for any resistor on the card.
63	RESET2	HARDWARE RESET2 (Active High)	ISD	This pin is internally ORed with RESET1 and contains a 50-kΩ pull-down resistor.
15	$\overline{IORD}$	I/O READ	IU	This pin is used to read data from the I/O area. The MB86967 sends no response to $\overline{IORD}$ until a write operation to the CCR sets the card to the I/O card interface mode.
17	$\overline{IOWR}$	I/O WRITE	IU	This pin is used to write data to the I/O area. The MB86967 sends no response to $\overline{IOWR}$ until a write operation to the CCR sets the card to the I/O card interface mode.
3	$\overline{WAIT}$	WAIT	O	A Low level is output to this pin to delay the end of an I/O access cycle in progress.

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Pin no.	Symbol	Pin name	I/O	Function
2	$\overline{\text{INPACK}}$	INPUT RESPONSE	O	When $\overline{\text{CE}}$,$\overline{\text{REG}}$, and $\overline{\text{IORD}}$ are 0s and the address on the address bus agrees with the I/O port in the card, a Low level is output to this pin. When I/O addresses are independent, a Low level is always output to this pin when $\overline{\text{CE}}$,$\overline{\text{REG}}$, and $\overline{\text{IORD}}$ are 0s.
84	$\overline{\text{IOIS16}}$	16-BIT I/O PORT	O	When 16-bit access (word access) to the I/O port is possible, a Low level is output to this pin. When a High level is output to this pin, the system has 8-bit access (byte access). Note: In the IC memory interface mode (no write operation to the CCR) when power is applied and a reset is canceled, this pin serves as a WP+ (write-protect) pin. Under this condition, a High level is output to this pin (write-protect). 1 should be set in the device ID tuple, WPS, in the CIS to perform a write operation to the card.
92	$\overline{\text{IREQ}}$	INTERRUPT REQUEST	O	A Low level is output to this pin to request software service from the system. For no interrupt request, a High level is output to this pin. An interrupt signal is sent to one of the interrupt request signals on the bus in the system via the socket interface. Note: In IC memory interface mode (no write operation to the CCR) when power is applied and a reset is canceled, this pin serves as a +RDY/BSY pin. Under this condition, a High level (+RDY) is output to this pin.
98	$\overline{\text{ROMS}}$	ROM SELECT	O	This pin is used for output of EEPROM OR FLASH chip select signals.
99	$\overline{\text{ROMRD}}$	ROM READ	O	This pin is used for output of EEPROM OR FLASH read signals.
97	ROMAD	ROM ADDRESS	O	This pin is used when I/O-reading the I/O number. Connection of this pin to the most significant address of EEPROM OR FLASH permits I/O-reading of address space in the upper half of ROM. For a write operation, both the write enable ($\overline{\text{WE}}$) and I/O write ($\overline{\text{IOWR}}$) pins must be enabled. If there is no need to set the ID number in the CIS for I/O-reading, this pin should be kept open.

- **System interface pins in ISA bus mode**

Pin no.	Symbol	Pin name	I/O	Function
18 to 23, 25, 27 to 29, 85, 87 to 91	SD0 to SD15	SYSTEM DATA BUS	BD	These pins are used as data buses for data exchange between the host system and the MB86967. They are also used for DMA transfer. In the 8-bit bus mode (bit 5 of DLCR6 = 1), only the 8 lower bits (SD0 to SD7) are used.
4 to 13	SA0 to SA9	SYSTEM ADDRESS BUS	ID	These pins are used for input of system address signals for selecting LAN controller registers.
64	CHRESET	CHIP RESET (Active High)	ISU	This pin is used for input of hardware reset signals.
15	$\overline{\text{IOR}}$	I/O READ (Active Low)	IU	This pin is used for input of I/O read strobe signals.
17	$\overline{\text{IOW}}$	I/O WRITE (Active Low)	IU	This pin is used for input of I/O write strobe signals.
63	AEN	ADDRESS ENABLE (Active High)	ISD	This pin is used for input of signals indicating that the DMA controller controls the system bus.
65	EOP	END OF PROCESS (Active High or Active Low)	ID	This pin is used for input of signals indicating the end of DMA transfer between the buffer memory and host system. At input of EOP, the next BREQ is not output and the handshaking cycle is terminated.
14	ALE	ADDRESS LATCH ENABLE	ID	This pin is used for input of signals indicating that the addresses of SA0 to SA9 are determined.
82	$\overline{\text{SBHE}}$	SYSTEM BUS HIGH ENABLE	IU	This pin is used for controlling byte/word transfer. In the 16-bit data bus mode (bit 5 (SB/$\overline{\text{SW}}$) of DLCR6 = 0), this pin, together with SA0, controls word transfer and the transfer of upper and lower bytes on the data bus.
2	DREQ	DMA REQUEST (Active High)	O	This pin is used for output of DMA transfer request signals.

SB/$\overline{\text{SW}}$	$\overline{\text{SBHE}}$	SA0	Function
0	0	0	Word transfer
0	0	1	Transfer of upper bytes on data bus (SD15 to SD8)
0	1	0	Transfer of lower bytes on data bus (SD7 to SD0)
0	1	1	Unused
1	×	×	Byte transfer (SD7 to SD0)

×: don't care

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<table>
<tr><th>Pin no.</th><th>Symbol</th><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td rowspan="2">69
74
75
92</td><td rowspan="2">IREQ1/IOSEL0
IREQ2/IOSEL1
IREQ3/IOSEL2
IREQ0</td><td>INTERRUPT REQUEST 0 to 3 (Active High)</td><td rowspan="2">IU/O</td><td>Jumperless Mode
These pins are used for output of IR signals. One of IREQ0 to IREQ3 is selected by configuration data in EEPROM.</td></tr>
<tr><td>I/O ADDRESS SELECT</td><td>Jumper Mode
These pins are used to select the I/O base addresses to which the LAN controller is allocated.
<table>
<tr><th>IOSEL2</th><th>IOSEL1</th><th>IOSEL0</th><th>I/O Base Address</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>260H to 27FH</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>280H to 29FH</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2A0H to 2BFH</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>240H to 25FH</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>340H to 35FH</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>320H to 33FH</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>380H to 39FH</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>300H to 31FH</td></tr>
</table></td></tr>
<tr><td>83</td><td>$\overline{\text{DMACK}}$</td><td>DMA ACKNOWLEDGE</td><td>I</td><td>This pin is used for input of DMAC acknowledge signals indicating that the DMAC is ready to transmit and receive data to and from buffer memory.</td></tr>
<tr><td>3</td><td>IOCHRDY</td><td>I/O CHANNEL READY (Active Low, open-drain output)</td><td>OD</td><td>This pin is used for output of signals indicating READY for handshaking with the host system.</td></tr>
<tr><td>84</td><td>$\overline{\text{IOCS16}}$</td><td>I/O CHANNEL SELECT 16 (Active Low, open-drain output)</td><td>OD</td><td>This pin is used for output of signals indicating that data transfer is made in a 16-bit I/O access cycle.</td></tr>
<tr><td>93</td><td>$\overline{\text{ENHB}}$</td><td>ENABLE DATA HIGH (Active Low)</td><td>O</td><td>This pin is used for output of enable signals for an external upper system data bus transceiver.</td></tr>
<tr><td>95</td><td>$\overline{\text{ENLB}}$</td><td>ENABLE DATA LOW (Active Low)</td><td>O</td><td>This pin is used for output of enable signals for an external lower system data bus transceiver.</td></tr>
<tr><td>99</td><td>EEPSK</td><td>SHIFT CLOCK</td><td>O</td><td>This pin is used for output of EEPROM shift clock pulses.</td></tr>
<tr><td>97</td><td>EEPDI</td><td>DATA IN</td><td>O</td><td>This pin is connected to DATA IN pin of EEPROM.</td></tr>
<tr><td>96</td><td>EEPDO</td><td>DATA OUT</td><td>IU</td><td>This pin is connected to DATA OUT pin of EEPROM.</td></tr>
<tr><td>98</td><td>EECS</td><td>EEPROM CHIP SELECT (Active High)</td><td>O</td><td>This pin is used for output of EEPROM chip select signals.</td></tr>
</table>

- **System interface pins in general-purpose mode**

<table>
<tr><th>Pin no.</th><th>Symbol</th><th>Pin name</th><th>I/O</th><th>Function</th></tr>
<tr><td>18 to 23,
25,
27 to 29,
85,
87 to 91</td><td>SD0 to SD15</td><td>SYSTEM DATA BUS</td><td>BD</td><td>These pins are used as a data bus for data exchange between the host system and the MB86967. They are also used for DMA transfer. In the 8-bit bus mode (bit 5 of DLCR6 = 1), only the 8 lower bits (SD0 to SD7) are used.</td></tr>
<tr><td>4 to 7</td><td>SA0 to SA3</td><td>SYSTEM ADDRESS BUS</td><td>ID</td><td>These pins are used for input of system address signals for selecting MB86967 registers, BOOT PROM, and ID PROM.</td></tr>
<tr><td>82</td><td>$\overline{\text{ECS}}$</td><td>ENABLE CHIP SELECT</td><td>IU</td><td>This pin is used for input of Active-Low chip select signals.</td></tr>
<tr><td>64</td><td>HWRST</td><td>CHIP RESET</td><td>ISU</td><td>This pin is used for input of hardware reset signals (Active High).</td></tr>
<tr><td>15</td><td>$\overline{\text{IOR}}$</td><td>I/O READ</td><td>IU</td><td>This pin is used for input of I/O read strobe signals (Active Low).</td></tr>
<tr><td>17</td><td>$\overline{\text{IOW}}$</td><td>I/O WRITE</td><td>IU</td><td>This pin is used for input of I/O write strobe signals (Active Low).</td></tr>
<tr><td>13</td><td>EOP</td><td>END OF PROCESS</td><td>ID</td><td>This pin is used for input of signals indicating the end of DMA transfer between the buffer memory and host system. At EOP input, the next DREQ is not output and the handshaking cycle is terminated. Either Active High or Active Low can be selected.</td></tr>
<tr><td>12</td><td>$\overline{\text{DMACK}}$</td><td>DMA ACKNOWLEDGE</td><td>ID</td><td>This pin is used for input of Active-Low signals and for connection of DMAC acknowledge signals indicating that the DMAC is read for transmitting and receiving data to and from buffer memory.</td></tr>
<tr><td>11</td><td>$\overline{\text{BHE}}$</td><td>SYSTEM BUS HIGH ENABLE</td><td>ID</td><td>This pin is used for input of Active-Low signals and for controlling byte/word transfer. In the 16-bit data bus mode (bit 5 (SB/$\overline{\text{SW}}$)of DLCR6 = 0), this pin, together with SA0, controls word transfer and the transfer of upper and lower bytes on the data bus.
<table>
<tr><th>SB/$\overline{\text{SW}}$</th><th>$\overline{\text{SBHE}}$</th><th>SA0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Transfer of upper bytes on data bus (SD15 to SD8)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Transfer of lower bytes on data bus (SD7 to SD0)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Unused</td></tr>
<tr><td>1</td><td>×</td><td>×</td><td>Byte transfer (SD7 to SD0)</td></tr>
</table>
×: don’t care</td></tr>
<tr><td>92</td><td>$\overline{\text{INT}}$</td><td>INTERRUPT REQUEST</td><td>O</td><td>This pin is used for output of Active-Low interrupt request signals.</td></tr>
<tr><td>2</td><td>DREQ</td><td>DMA REQUEST (Active High)</td><td>O</td><td>This pin is used for input of DMA transfer request signals.</td></tr>
</table>

(Continued)

(Continued)

Pin no.	Symbol	Pin name	I/O	Function
3	READY	READY	O	This pin is used for output of signals indicating READY for handshaking with the host system. Either Active High or Active Low can be selected.
10	RDYPOL	READY POLARITY	ID	This pin is used for selecting the polarity of the READY signal. 1: Active High 0: Active Low
98	$\overline{SB}$/SW	SYSTEM BYTE/WORD CONFIGURATION	O	This pin is used for output of signals indicating the system bus width. The value of bit 5 of the internal register DLCR6 is reversed. Low: 8-bit data bus mode High: 16-bit data bus mode
8	MODE1	MODE1	ID	This pin is used for setting to general-purpose bus mode.

- **Network interface pins in PC card mode, ISA bus mode, and general-purpose bus mode**

Pin no.	Symbol	Pin name	I/O	Function
68 (PC card mode) 68 (ISA bus mode) 96 (General-purpose bus mode)	LEDC	COLLISION LED	OD	These pins are used for driving the LED indicating the occurrence of collisions (open-drain output).
52 (PC card mode) 52 (ISA bus mode) 95 (General-purpose bus mode)	LEDL	LINK LED	OD	These pins are used for driving the LED indicating the status of the link test (open-drain output). These pins are placed in the link-passed state when the link test is enabled. A Low level is output to this pin when the link test is disabled. When in the power-down or shut-down mode, these pins enter the high-impedance state, regardless of the status of the link test.
66(PC card mode) 66 (ISA bus mode) 93 (General-purpose bus mode)	LEDT	TRANSMIT LET	OD	These pins are used for driving the LED indicating transmit-on status (open-drain output).
65 (PC card mode) 73 (ISA bus mode) 65 (General-purpose bus mode)	LEDR	RECEIVE LET	OD	These pins are used for driving the LED indicating receive-on status (open-drain output).
77 78 79 80	TPOPB TPOPA TPONA TPONB	TWISTED PAIR OUTPUT	O	These pins are used for output of differential transmit signals from the built-in 10BASE-T transceiver. Preconditioning is performed by two output pins and external filters.
71 72	TPIP TPIN	TWISTED PAIR INPUT	I	These pins are used for input of receive signals from the twisted-pair cable.

- **Buffer memory interface pins in PC card mode, ISA bus mode, and general-purpose bus mode**

Pin no.	Symbol	Pin name	I/O	Function
34 to 41	BD0 to BD7	BUFFER MEMORY DATA BUS	B	These pins are used as data buses for data exchange between the SRAM buffer memory and the MB86967.
42 to 45, 47 to 50, 53 to 56, 58 to 60	BA0 to BA14	BUFFER MEMORY ADDRESS BUS	O	These pins permit addressing of external SRAM buffer memory expandable to 32 Kbytes.
33	$\overline{\text{BOE}}$	BUFFER OUTPUT ENABLE	O	This pin is used for output of Active-Low signals and for enabling buffer memory at a read operation.
32	$\overline{\text{BWE}}$	BUFFER WRITE ENABLE	O	This pin is used for output of Active-Low signals and for enabling buffer memory at a write operation.
30	$\overline{\text{BCS}}$	BUFFER RAM CHIP SELECT	O	This pin is used for output of Active-Low signals and RAM chip select signals.

- **Other pins in PC card mode, ISA bus mode, and general-purpose bus mode**

Pin no.	Symbol	Pin name	I/O	Function
52	MODE/LEDL (PC card mode)	MODE SELECT/ LINK LED	IU/OD	This pin serves as a mode select pin or a pin for driving the LED indicating the status of the link test according to the mode used. It is pulled-up internally.
	LEDL (ISA bus mode)		OD	
	MODE (General-purpose bus mode)		IU	
73	GNDM (PC card mode)	MODE SELECT/ RECEIVE LED	G	This pin serves as a mode select pin or a pin for driving the LED indicating the receive status according to the mode used. It serves as a GND pin in the PC card mode and general-purpose bus mode.
	MODE/LEDR (ISA bus mode)		I/OD	
	GNDM (General-purpose bus mode)		G	
61 62	CLKO CLKI	CRYSTAL OSCILLATOR	O I	Connect an external 20-MHz crystal oscillator. Input external clock pulses to CLKI. The wiring between CLKO/CLKI and the crystal oscillator should be as short as possible to prevent cross-talk with other signal lines.
1, 26, 51, 94	$V_{DD}1$ to $V_{DD}4$	DIGITAL V_{DD}	—	These pins are used for power supply to the digital sections.
70 81	VDDA1 VDDA2	ANALOG V_{DD}	—	These pins are used for power supply to the encoder/decoder and 10BASE-T transceiver.
16, 24, 31, 46, 57, 86, 100	GND1 to GND7	DIGITAL GROUND	—	These pins are used for grounding the digital sections.
67 76	GNDA1 GNDA2	ANALOG GROUND	—	These pins are used for grounding the encoder/ decoder and 10BASE-T transceiver.

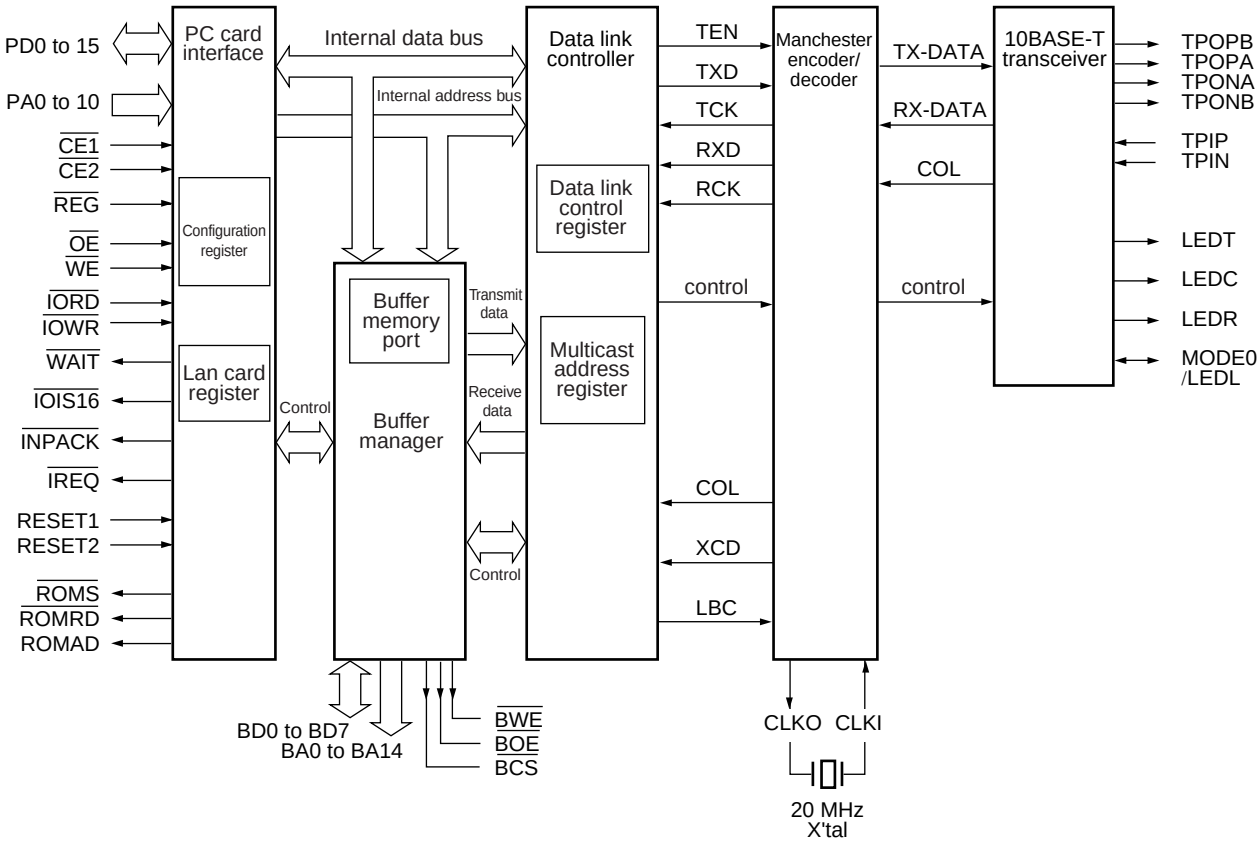
■ SETTING EACH MODE

Pin 73	Pin 52	Pin 8	Pin 41 (BD0)	Operation Mode
1	×	×	External pull-up*1	ISA bus mode (Jumperless mode)
			External pull-down*2	ISA bus mode (Jumper mode)
0	1	×	×	PC card mode*3
0	0	0	×	General-purpose bus mode

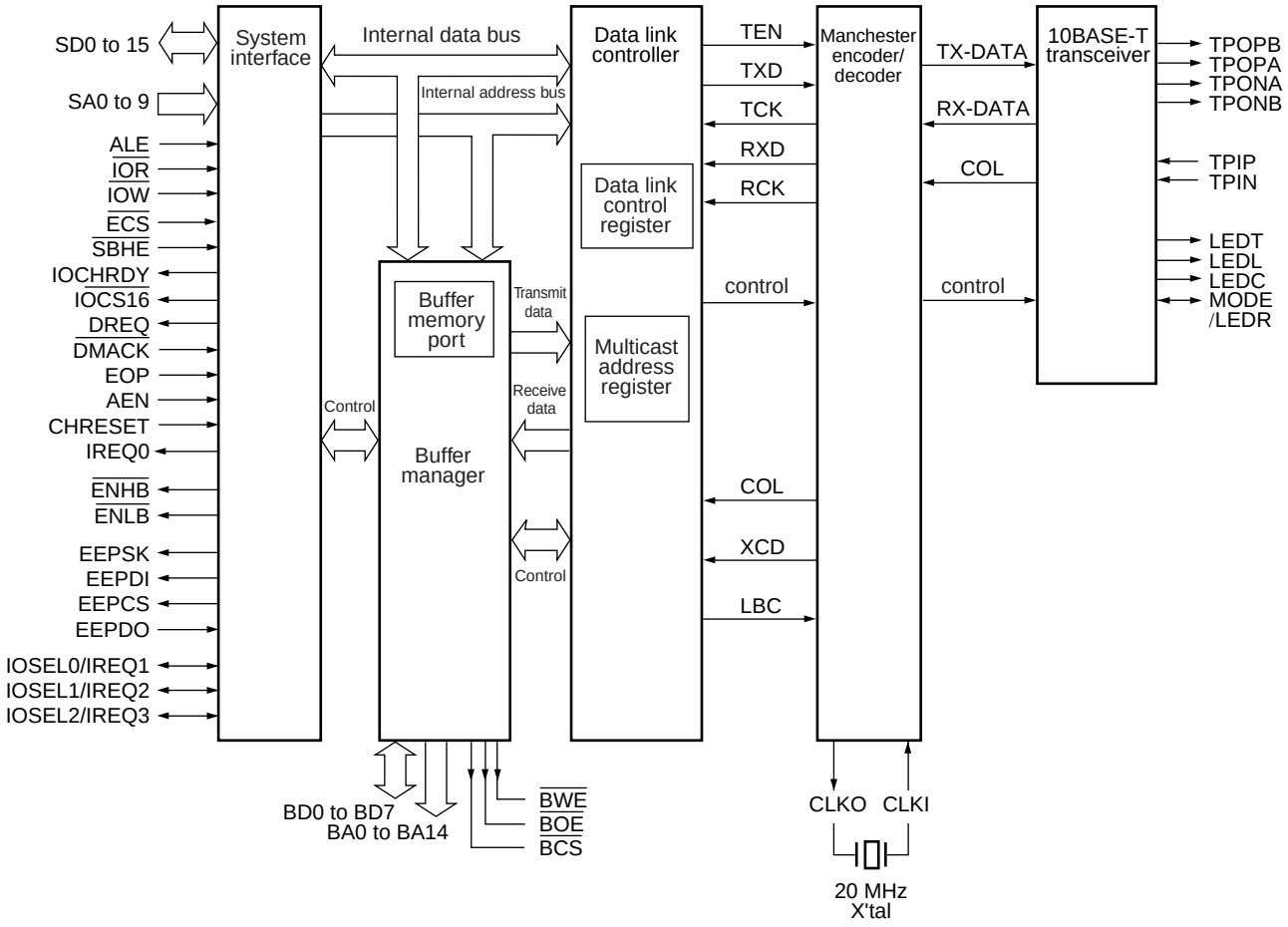
×: don't care
*1: To set the jumperless mode, pull up pin 41 (BD0) at about 50 kΩ to 150 kΩ .
*2: To set the jumper mode, pull down pin 41 (BD0) at about 50 kΩ to 150 kΩ .
*3: The PC card mode has a bug. Please refer to the Page 58 errata sheet in this document.

■ BLOCK DIAGRAM

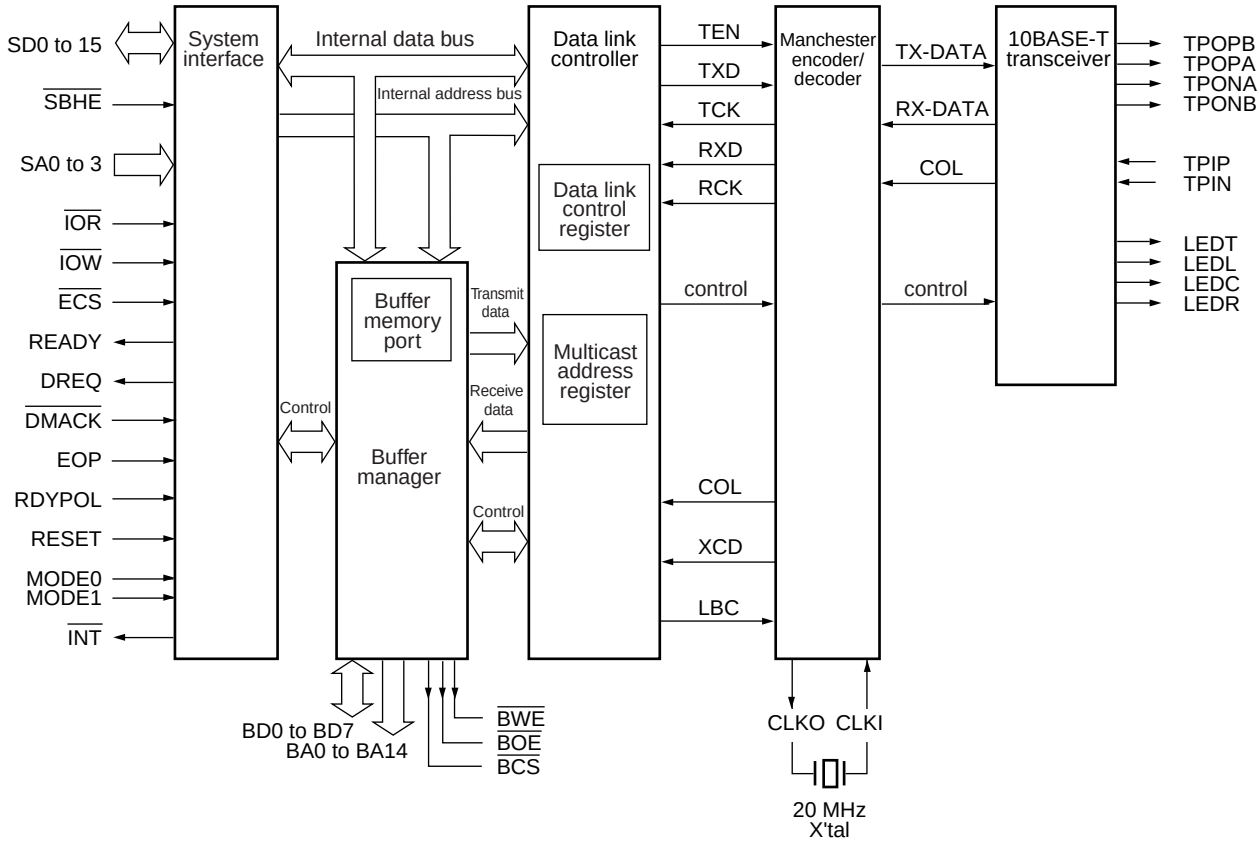
• **PC card mode**



- **ISA bus mode**


SD0 to 15
SA0 to 9
ALE
IOR
IOW
ECS
SBHE
IOCHRDY
IOCS16
DREQ
DMACK
EOP
AEN
CHRESET
IREQ0
ENHB
ENLB
EEPSK
EEPDI
EEPCS
EEPDO
IOSEL0/IREQ1
IOSEL1/IREQ2
IOSEL2/IREQ3
System interface
Internal data bus
Internal address bus
Control
Buffer memory port
Buffer manager
Transmit data
Receive data
Control
BD0 to BD7
BA0 to BA14
BWE
BOE
BCS
Data link controller
Data link control register
Multicast address register
TEN
TXD
TCK
RXD
RCK
control
COL
XCD
LBC
Manchester encoder/ decoder
CLKO
CLKI
20 MHz X'tal
TX-DATA
RX-DATA
COL
control
10BASE-T transceiver
TPOPB
TPOPA
TPONA
TPONB
TPIP
TPIN
LEDT
LEDL
LEDC
MODE /LEDR

- **General-purpose bus mode**



■ BLOCK DESCRIPTION

The MB86967 has five functional blocks. The functions of each block in the PC card mode, ISA mode, and general-purpose bus mode is explained below.

1. 10BASE-T Transceiver

The 10BASE-T transceiver pre-distorts transmit packets from the Manchester encoder/decoder to be suitable for use in the 10BASE-T jitter template. Filtering is performed by an external active filter. The transceiver passes the received packets through an internal receive filter and transfers them to the encoder/decoder.

2. Manchester Encoder/Decoder

The Manchester encoder/decoder converts NRZ-formatted transmit packets from the data link controller into Manchester code and transfers them to the 10BASE-T transceiver. The encoder/decoder converters the receive packets from the transceiver from Manchester code to NRZ format and transfers them to the data link controller.

3. Data Link Controller

The data link controller performs the function of the data link layer specified in the IEEE802.3 standard. At transmitting, the controller attaches the preamble and CRC code to transmit data from buffer memory and transmits it as serial data to the Manchester encoder/decoder. In the event of a collision, the controller automatically executes the back-off algorithm for re-transmission.

At receiving, the data link controller performs address-matching and error checks for receive packets from the Manchester encoder/decoder, removes the preamble and CRC code from the packets, and converts them to serial data before writing to buffer memory.

The data link controller has a multicast address filter to recognize up to 64 groups of multicast addresses.

4. Buffer Manager

The MB86967 needs external SRAM (expandable to 32 Kbytes) for buffering transmit and receive data. Buffer memory is divided into a dual-bank transmit buffer and ring receive buffer where all processing such as arbitration of access from the system and network and updating of buffer pointers is performed automatically by the buffer manager. The transmit buffer has a packet chain function for continuously transmitting the packets of data stored in it using one transmit-start instruction.

5. System Interface

Like the MB86965B and MB86964, the mode pin setting allows the system interface to switch between the general-purpose interface, ISA bus interface enabling direct interface with the ISA bus, and PC card interface based on the JEIDA4.2 standard.

When in the ISA bus interface mode, a serial EEPROM can be connected for storing node IDs and two modes can be selected: a jumperless mode allowing software setting of I/O addresses and interrupt signals for the LAN controller, and a jumper mode allowing DIP-switch setting.

■ FUNCTIONAL DESCRIPTION

1. Local Buffer Configurations

The MB86967 is designed to operate with local buffer which holds packets received from the host processor prior to transmission and assembles packets received from the network before they are delivered to the host processor. The buffer is implemented by using a single byte-wide SRAM whose size is selected via DLCR6<1> as 8 kbytes (DLCR6<1> = 0) or 32 kbytes DLCR6<1> = 1).

See Buffer Access section for information on how the host accesses the buffer memory.

2. Crystal Oscillator

The clock rate of 10 Mbits/s specified by the international LAN standard, ISO/ANSI/IEEE 8802-3, is derived from an on-chip oscillator that is controlled by a 20 MHz crystal connected across pins 61 and 62 (CLKO and CLKI). Capacitance specified by the crystal manufacturer must be connected as shown in Figure 1 to stabilize the effects of stray capacitance that may vary crystal frequency. The 20 MHz clock also serves as an internal phase-locked loop (PLL) reference for decoder clock recovery.

Use a crystal with the following specifications: quartz (AT-cut); 20-MHz; frequency acurracy of ±50ppm at 25°C and ±100ppm at 0°C to 70°C; parallel resonant with 20 pF-load in fundamental mode.

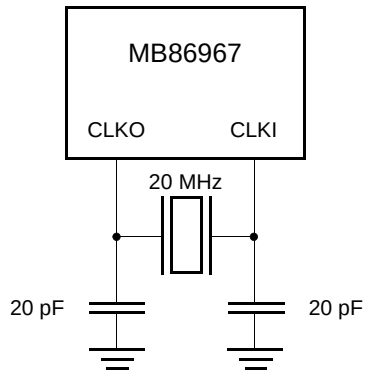


Figure 1 Crystal Oscillator Connection

3. Byte-Order Control

Byte-order control provided by BYTESWEAP bit, DLCR7<0>, provides compatibility with various higher-level protocols, such as TCP/IP and XNS. These protocols may have a different order for transmission of the bytes within a word. When BYTESWEAP is low, the least-significant byte of the word transmits first, followed by the most-significant. When BYTESWEAP is set high, the byte order reverses. This feature applies only when the system bus operates in 16-bit (word) mode.

The byte-order control works by reversing, or not reversing, the bytes of all words as they pass between the buffer memory and the system bus. Thus all data stored in the transmit buffer or retrieved from the receive buffer is affected, including nontransmitted headers. This control bit does not affect the MB86967 registers other than the Buffer Memory Port registers, BMPR8 and BMPR9. When using this feature, ensure the reversal of header information as well as packet data in the software driver code. See Table 1 for examples of using least..most and most..least byte ordering.

4. Register Access

The MB86967 includes four sets of user-accessible registers, all of which are accessible as bytes or words. Each register set contains eight registers.

Direct access is available to two sets of registers in the device's register set at a time, via register addresses 00H through 0FH. The Data Link Control Registers set (DLCR0 - DLCR7) is always accessible via addresses 00H to 07H. Access to one of the remaining three sets is accomplished by programming the register bank select bits, DLCR7<3:2>. This selects the register set accessible via addresses 08H to 0FH. The bank-switched registers are the Node ID set , DLCR7 - DLCR15, (for setting the Ethernet Address and performing TDR diagnostics), the Hash Table set, HT8 - HT15, (for setting up multicast address filtering) and the Buffer Memory Port set, BMPR7 - BMPR15. During operation (excluding initialization or diagnostics), the Buffer Memory Port set should normally be selected.

Table 1 Byte Ordering

Data<15:8>	Data<7:0>
FOR TRANSMIT PACKET	
LEAST....MOST	
Transmit Length, high byte	Transmit Length, low byte
Destination Address, 2nd byte	Destination Address, 1st byte
Source Address, 2nd byte	Source Address, 1st byte
Length Field, low byte*	Length Field, high byte*
Data Field, 2nd byte	Data Field, 1st byte
MOST....LEAST	
Transmit Length, low byte*	Transmit Length, high byte*
Destination Addr, 1st byte	Destination Addr, 2nd byte
Source Addr, 1st byte	Source Addr, 2nd byte
Length Field, high byte	Length Field, low byte
Data Field, 1st byte	Data Field, 2nd byte
FOR RECEIVE PACKET	
LEAST....MOST	
Unused, reserved	Receive Packet Status
Receive Length, high byte	Receive Length, low byte
Destination Address, 2nd byte	Destination Address, 1st byte
Source Address, 2nd byte	Source Address, 1st byte
Length Field, low byte*	Length Field, high byte*
Data Field, 2nd byte	Data Field, 1st byte
MOST....LEAST	
Receive Packet Status	Unused; reserved
Receive Length, low byte*	Receive Length, high byte*
Destination Addr, 1st byte	Destination Addr, 2nd byte
Source Addr, 1st byte	Source Addr, 2nd byte
Length Field, high byte	Length Field, low byte
Data Field, 1st byte	Data Field, 2nd byte

Items shown with an asterisk are in numerically reversed byte order

5. Buffer Access

The Buffer Memory Port register pair BMPR8 and BMPR9 provide 8- or 16-bit data access to the receive and transmit buffers through on-chip FIFOs. To eliminate the need for complicated directional control, FIFOs are dedicated to each direction of data transfer. Writing to the transmit buffer can be interleaved with reading from the receive buffer, with the MB86967 automatically maintaining buffer memory pointers, thus relieving the host of that task. The Buffer Memory port register pair is at address 08H when DLCR7<3:2> are programmed to '10' to select the Buffer Memory Port register set. When using DMA, the buffer memory port is automatically selected when the DMA Acknowledge input, DMACK, is asserted. The host accesses are byte-wide when the system is configured for byte-wide operation and word-wide when the system interface is configured for word-wide operation. In the latter mode, byte-wide access to the buffer memory port is not supported.

Data can transfer from the host memory to the transmit buffer, or from the receive buffer to host memory by using string moves, single-transfer programmed I/O moves, or DMA. Select the method that yields the highest system-level efficiency. A rapid transfer process results in best performance. Slow transfer can result in poor throughput and performance, and cause the receive buffer to overflow and lose packets.

6. DMA Operation (ISA, Generic Mode Only)

The MB86967 supports single-cycle and burst DMA operation for data transfers between the host and the packet buffer. Hand-shaking between the MB86967 and the external DMA controller is accomplished by the DREQ and DMACK signals. The end of process input, when asserted by the system DMA controller during a transfer cycle, terminates DMA activity after completion of the current cycle. If a DMA interrupt (DLCR3<5>) is enabled, the MB86967 generates an interrupt after completion of DMA activity.

Usually only one DMA operation will be run at a time, although the MB86967 could run two interleaving operations, one reading and one writing. There is only one DMA EOP bit, and only one DREQ pin and one DMACK pin, so most hosts could not support more than one DMA operation at a time.

6.1 DMA Write (Transmit) ISA, Generic Mode Only

Setting the TX DMA Enable bit, BMPR12<0>, enables DMA transfer of data packets from the host memory to the MB86967 transmit buffer. The DMA burst control bits, BMPR13<1:0>, set the maximum number of data transfer cycles (bytes or words) in a single bus acquisition to be 1, 4, 8, or 12. The MB86967, when ready to accept data from the host, sets the DMA request output, DREQ, and the host responds by asserting DMA acknowledge, DMACK, followed by Write Strobe, WR, and placing data on the data bus. The MB86967 asserts the RDY(RDY) output when ready to complete the current data-transfer cycle. (The assertive states of the RDY(RDY) output and the EOP(EOP) input are independently programmable.) The MB86967 accepts the data byte/word into its bus write FIFO and later moves it into buffer memory. At the close of a transfer cycle, the host negates WR. In burst mode and depending on the value of the DREQ EXTND bit, DLCR4<2>, the MB86967 negates DREQ at the next-to-last or last transfer cycle of the burst. The host DMA then completes the last one or two transfer cycles and negates DACK to terminate the burst. To start another burst, the MB86967 reasserts DREQ.

The DMA controller asserts the end of process input, EOP(EOP), concurrent with the last required data-transfer cycle to indicate completion of the entire transfer process. This action sets the DMA EOP status bit, DLCR1<5>, and discontinues further data requests from the MB86967. The MB86967 will also generate an interrupt if the DMA EOP interrupt enable bit, DLCR3<5>, is high. The host can use this interrupt to begin action to close the process. The host should reset the MB86967 DMA logic and clear the interrupt by writing 00H to BMPR12.

Note: DMA EOP, DLCR1<5> must be cleared to close the transmit DMA process before attempting another DMA process. This is accomplished by writing 00H to BMPR12. When this is done, the DMA EOP bit will clear automatically, clearing the EOP status and interrupt, (if enabled) so it is not necessary to clear the interrupt separately.

After finishing the loading of packets into the buffer, the host initiates packet transmission. This is done by loading the number of packets to be transmitted into the Transmit Start Register, BMPR10<6:0>, and asserting the Transmit Start bit, TXST, of the same register, BMPR10<7>.

6.2 DMA Read (Receive) ISA, Generic Mode Only

The MB86967 indicates that it has received packets and stored them in the packet buffer with status bits or interrupts. Before attempting to transfer a packet from the buffer, the host processor should read the RX BUF EMPTY bit, DLCR5<6>. If this bit is 0, there are one or more packets ready for transfer in the receive buffer. After reading each packet, the host will check this bit again to see if there are more.

Prior to beginning the transfer of a packet from the receive buffer to host memory via DMA, the host must first read the four-byte receive packet header from the buffer to obtain the packet status and the length of the packet in bytes. Calculating from the packet length the number of DMA cycles needed to read the packet, the host will load that number into the cycle counter of the host DMA controller. Next, RX DMA EN, BMPR12<1>, is set to high to enable DMA read operation to transfer the packet to host memory. The DMA burst control bits, BMPR13<1:0>, set the maximum number of data transfer cycles (bytes or words) in a single bus acquisition to be 1, 4, 8, or 12. When it is ready to begin, the MB86967 asserts its DMA Request output, DREQ. The host responds by asserting DMA Acknowledge, DMACK, followed by the Read Strobe, RD. The MB86967 will assert its RDY(RDY) output when it has placed the byte/word on the data bus and is ready to complete the data transfer cycle. The system memory will accept the data, then the host negates RD. The MB86967 shifts the data down in its bus read FIFO, then moves its internal read pointer to point to the next byte/word in the buffer, moving it into the FIFO.

In burst mode and depending on the value of the DREQ EXTND bit, DLCR4<2>, the MB86967 negates DREQ at the next-to-last or last transfer cycle of the burst. The host DMA then completes the last one or two transfer cycles and negates DMACK to terminate the burst. The MB86967 reasserts DREQ to repeat the process if it can transfer more data after the host negates DMACK. The DMA controller asserts the end of process input, EOP(EOP) concurrent with the last byte/word data transfer to indicate completion of the entire process. The MB86967 then stops requesting more DMA cycles.

When EOP(EOP) is asserted by the host DMA controller, the DMA EOP bit, DLCR1<5>, will be set high, and an interrupt will also be generated, provided it is enabled by a high in the associated interrupt enable bit, DLCR3<5>. This interrupt can be used by the host to initiate the final actions to close the DMA process. The interrupt is cleared and the DMA is disabled and reset by writing 00H to the DMA Enable Register, BMPR12.

Note: Clearing RX DMA EN must be done to close the receive DMA process before attempting another DMA process. This is accomplished by writing 00H to BMPR12. When this is done, the DMA EOP bit will clear automatically, clearing the EOP status and interrupt, so it is not necessary to clear the interrupt separately.

After completion of the DMA process, RX DMA EN must be reasserted when the host wants to begin reading another packet from the receive buffer by using DMA.

7. Buffer Controller

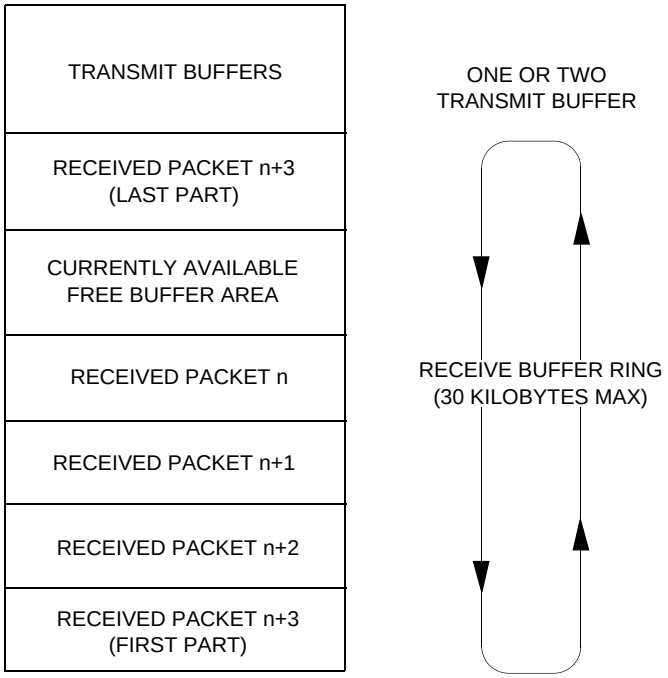


Figure 2 Buffer Memory Organization

7.1 General

The MB86967 uses a dedicated buffer memory, organized as shown in Figure 2, for intermediate storage of packets to be transmitted, and of packets received from the network. The MB86967 can operate with 8 or 32 kilobytes of total buffer memory, including both transmit and receive spaces. Memory partitioning into transmit and receive sections is controlled by the system software. The total size of the transmit buffer space can be up to 16 kilobytes. The buffer memory not used for the transmitter is used for the receiver, and is automatically configured as a ring buffer. Packets are stored head-to-toe in the receive buffer, as they are in the transmit buffer. However, each packet in the receive buffer is aligned on an eight-byte boundary. As packets are being stored in the receive buffer, as the end of the linear addressing space is reached, the chip's receive write pointer automatically wraps around to the top of the receive addressing range to make a seamless ring. The receive read pointer does the same as the packets are read out to the system. By programming the sizes allocated to transmit and receive buffers, an optimum usage of the memory can be selected according to the demands of a particular application.

The buffer controller keeps track of buffer memory partitioning and allocation and updates internal address pointers automatically for the tasks of transmit, retransmit, receive, rejection of packets with errors and data transfers to and from the host. The host and its drivers are thus relieved of buffer management functions, making the MB86967 easy to operate and substantially reducing software requirements. Packets with errors are normally automatically rejected by the MB86967 as are packets shorter than the IEEE minimum length packet of 60 bytes, excluding Preamble and CRC. Since these tasks can be done faster in hardware than in software, this not only

off-loads the host system, but it also speeds up the communication processes, yielding higher throughput. As a result, the MB86967 can typically win benchmark performance tests over competing controllers.

7.2 Arbitration of Buffer Access

The buffer controller automatically prioritizes and services requests for access to memory from the transmitter, receiver and host system. The MB86967's arbitration mechanism, illustrated in Figure 3, interleaves accesses to the buffer memory so that the operation appears to be simultaneous: data can be written to or read from the buffer memory by the host via Buffer Memory Port Register 8 (BMPR8), while data is being read from the buffer by the transmitter and/or written in for storage by the receiver. Each interface, whether host system or network access, appears to be served independently by the controller. Each interface has an associated FIFO to provide time for the buffer interleaving. Thus, packet data is pipelined through the system for highest performance and throughput, and the buffer controller supports all the cases of simultaneous access to the buffer memory as follows:

1. Data from the network is stored in the receive buffer.
2. The host retreives packets from the receive buffer.
3. The host loads packet data into the transmit buffer.
4. The transmitter obtains data for transmission from the transmit buffer.
5. Any combination of the above can occur concurrently.

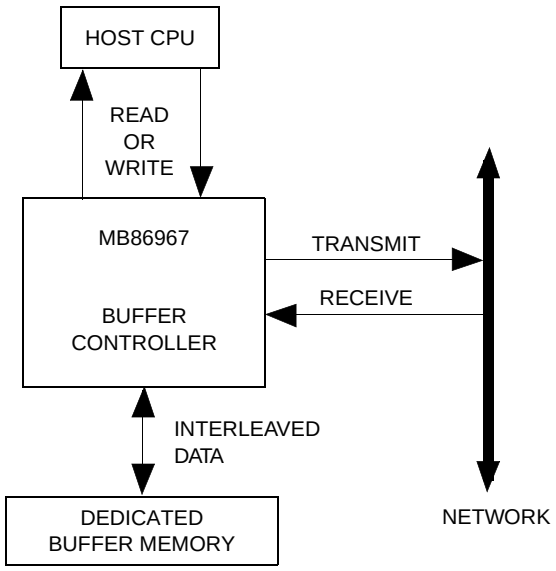


Figure 3 Simultaneous Access to Buffer Memory

7.3 Transmit Buffer

The section of the memory used by the transmitter can be configured by programming the Transmitter Buffer Size control bits, DLCR6<3:2>. Configurations include a single buffer 2 kilobytes long, or a pair of banks, each either 2, 4 or 8 kilobytes long, as illustrated in Figure 4. Within each buffer or bank, one or more packets can be written by the system until the available space is too small for another packet. When a single transmit buffer is used, the system and the transmitter time-share the use of the buffer. When two buffers are used, the system can load packets into one of the buffers while the contents of the other are being transmitted. Using dual buffers and loading multiple packets for 'packet chaining' gives the highest rate of transmission.

At reset, internal pointers are initialized to point to the beginning of one of the transmit buffers. Each time the host writes data to the buffer via the Buffer Memory Port Register, an internal pointer is advanced to the next memory location within the transmit buffer. Once a data byte/word is written, it cannot be read and the internal pointer cannot be reversed.

When the host completes loading the transmit buffer, it writes the number of packets it has loaded into TX PKT CNT, BMPR10<6:0> and sets the transmit start bit, BMPR10<7>. When this occurs, the MB86967 will switch banks and will start transmitting at the earliest opportunity. Another automatically-managed pointer, the transmit read pointer, sequences through the bank being transmitted to read the packet data into the transmitter through its FIFO. If a collision occurs, the packet will be automatically retransmitted after a pseudo-random waiting interval called the backoff interval. If there are multiple packets in the buffer, the MB86967 will continue down the list until all are transmitted. Upon reaching the end of the list or chain of packets, the transmitter will stop, update its status bits and, if enabled, generate an interrupt. The details of this operation are described in the section on packet transmission.

7.4 Transmit Packet Header

As shown in Figure 5, each packet within one transmit bank is separated by a non-transmitted, two-byte header containing an 11-bit value which specifies the length of the associated packet in bytes. The length specification includes only what is stored in the buffer (shown in the figure as ‘DATA’), which are the Destination ID, Source ID, Length, and Data fields of the packet. It does not include the Preamble and CRC fields which are generated by the MB86967 as it transmits the packet, and therefore are not stored in the buffer.

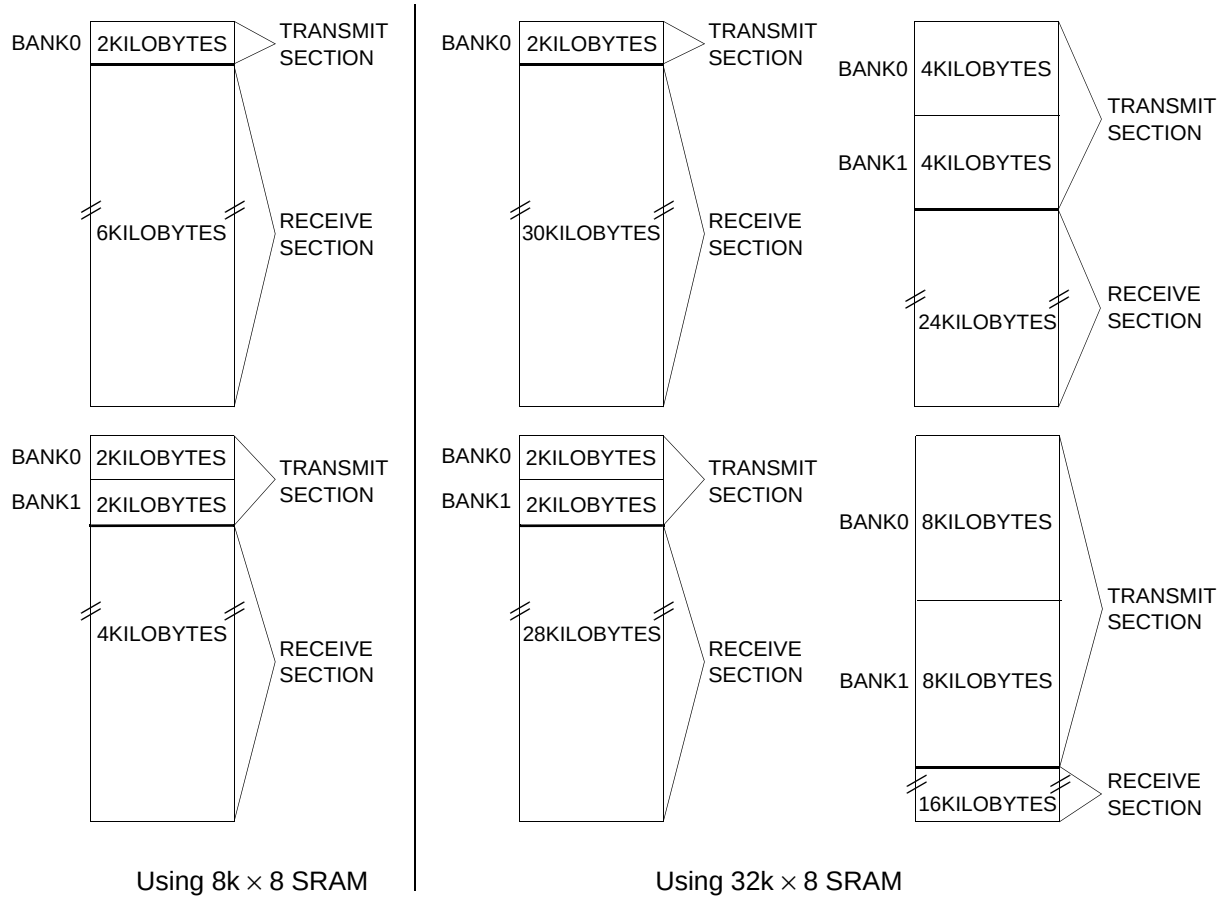


Figure 4 Transmit Buffer Configurations

7.5 Receive Buffer

Once initialized and enabled, the receiver will automatically load any error-free incoming packets which pass the address filter into the receive buffer through an on-chip FIFO. An interrupt can be provided to alert the host processor that a packet is available in the buffer. The host processor can read out received packets as they become available. Continuous reception can continue as long as the receive buffer does not become full. If the host processor reads the receive packets from the buffer promptly, the buffer will not fill up. If overflow does occur, the receiver will stop and an interrupt will be generated to indicate the problem. If this occurs, the buffer should be emptied so that reception can resume. As soon as space becomes available in the receive buffer, the receiver will automatically resume reception.

The receive buffer size can vary between a maximum of 30 kilobytes when 2 kilobytes are allocated for the transmit section and a 32 kilobyte SRAM is used, to a minimum of 4 kilobytes if 4 kilobytes are allocated for the transmit section and an 8 kilobyte SRAM is used. The receive section dynamically allocates space for each individual incoming data packet, aligning each at an eight-byte ‘page’ boundary. Each received packet is preceded by a four byte header which provides packet status and the length of that data packet. The data packets are linked or chained by internal pointers which use the length value in the packet header to calculate the starting address of the next packet. This buffer format is shown in Figure 6. Since the MB86967 controls its dedicated

buffer memory, FIFO size and depth are unimportant in this architecture, and need not be considered in system timing considerations.

A status bit in one of the MB86967's internal registers informs the host when one or more packets are resident in the receive buffer and available to be read. The host retrieves these packets from the buffer memory by successive reads of BMPR8. Once a data byte/word is read from the buffer memory, internal pointers are advanced to the next byte/word. As data is thus read by the system, that memory becomes available for reception of new packets. The MB86967 automatically rejects an incoming packet if there is not enough buffer space to fully receive that packet. Therefore, there is no chance for packets already received to be 'overrun' by incoming packets.

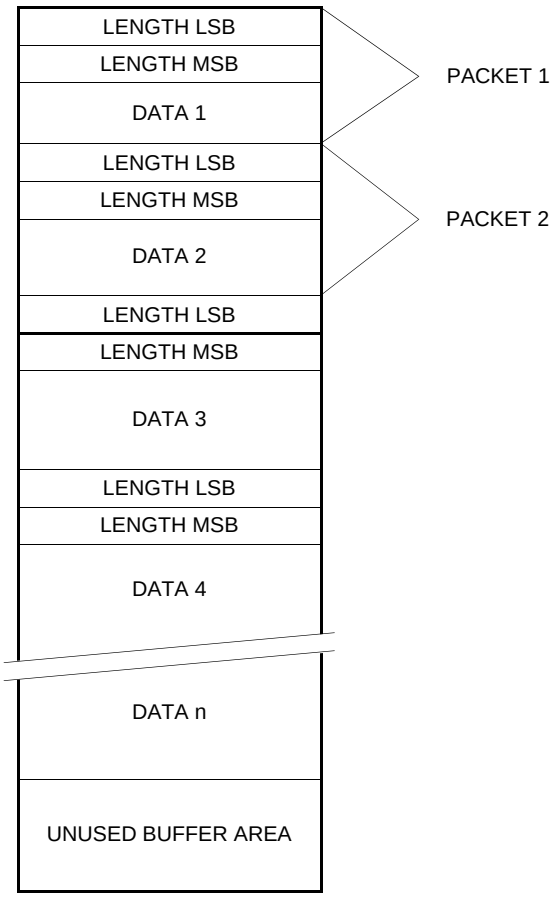


Figure 5 Transmit Buffer Detail

When DLCR5<5>, the ACPT BAD PKTS bit, is set to a '0' (disabled), detection of a bad incoming packet causes the MB86967 to release the buffer space in which that packet is contained and to reset its internal pointers so as to use that space for the next incoming packet. If this bit is set to a '1', a packet with a CRC or alignment error will be accepted and the appropriate error bits in the status field of its header will be set. The same applies to DLCR5<3>, ACPT SHORT PKTS, which when high allows retention of packets below 60 bytes in length, excluding Preamble and CRC (which is shorter than IEEE 802.3 minimum packet size).

7.6 Skip Packet

Writing a '1' to BMPR14<2> commands the buffer controller to skip the balance of the current receive packet in memory. The bit can then be read to determine completion of the skip process is complete (within 300 ns). If there is another packet, the bit returns to 0 when the chip is ready to read the next packet.

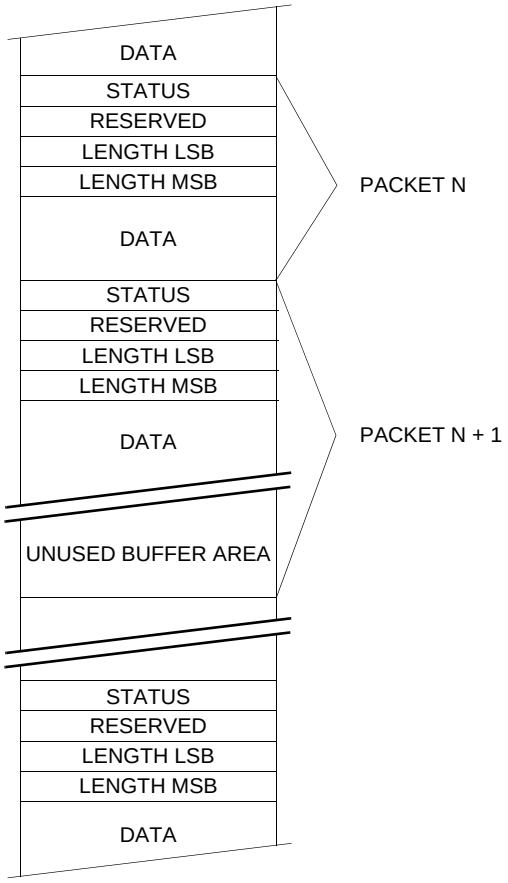


Figure 6 Receive Buffer Detail

7.7 Receive Packet Header

The receive packet header contains four bytes and is stored in the receive buffer preceding each packet. The receive packet header comprises one byte of packet status, an unused byte and two bytes (11 bits) for packet length. Bits 1 through 4 of the status byte are an image of the same bits in the Receive Status Register, DLCR1, with respect to the packet that follows. Bit 5 is the GOOD PKT bit, which when set to 1 indicates that no errors were detected in the packet. Bits 0, 6 and 7 are unused and are always set to 0. See Table 2.

The length stored in bytes 3 and 4 of the header specifies the length of the portion of the packet stored in the buffer. This length specification is in bytes, regardless of whether the system interface is programmed for byte or word mode. During reception, the MB86967 strips the Preamble field and checks and strips the CRC field, so, as is the case for the transmit buffer, those fields of the packet are not stored in the buffer. The length specification thus includes only the Destination ID, Source ID, Length, and Data fields of the incoming packet.

Table 2 Receive Packet Header Status Indications

Condition	N/A (Bit 7)	N/A (Bit 6)	Good PKT (Bit 5)	RMT 0900H (Bit 4)	SHORT PKT ERR (Bit 3)	ALIGN ERR (Bit 2)	CRC ERR (Bit 1)	N/A (Bit 0)
GOOD PACKET	0	0	1	0/1	X	X	X	X
PACKET WITH ERROR	0	0	0	0/1	0/1	0/1	0/1	X

0/1 indicates that the value of the bit will be 0 or 1 depending on the condition of the packet. An ‘X’ indicates that the value should be ignored.

8. Transmitter Circuits

Circuits within the transmitter include a transmitter state machine, a small FIFO for pipelining the packet data, preamble generator, CRC generator, parallel to serial converter, backoff generator, interpacket gap timer and time domain reflectometer (TDR) counter. Additional circuits involved in packet transmission are described in the Transceiver section of this document.

The transmitter state machine provides sequencing of events for the transmitter, including idle, preamble, data, CRC, interpacket gap, jam and backoff. It detects various transmit error conditions and sets appropriate bits within the DLCR registers.

The pipeline FIFO provides elastic buffering that the buffer controller can load with data to be transmitted. The chip’s CRC generator calculates the 32-bit CRC on the destination and source address, the length field and the data field as specified by the ISO/ANSI/IEEE 8802-3 specification for Ethernet. This value is appended to the end of the packet when it is transmitted.

8.1 Media Access Control

The MB86967 transmitter state machine implements the Carrier Sense, Multiple Access with Collision Detection (CSMA/ CD) network media-access protocol. The MB86967 monitors the network for any other node’s carrier, and defers transmission (collision avoidance) while other nodes are transmitting, except when DSC, DLCR4<0>, is high. Collision detection handles collisions that may still occur when two nodes separated on the network begin transmitting at nearly the same time. All nodes monitor the network for collisions and, when involved in one, transmit a 32-bit jam signal to reinforce the collision and then terminate transmission. After waiting a pseudo-random backoff interval, generated as described below, the node automatically retries transmission of the packet.

Packets on the network must be separated by at least 9.6 microseconds, the ‘interpacket gap’ (IPG) during which the network medium is specified to be idle. The MB86967 transmitter state machine measures this IPG starting from the end of a packet on the network, and does not attempt to transmit until the end of the IPG. If carrier reappears on the network during the first two-thirds of the IPG, the MB86967 resets the timer to re–time the IPG from the end of the new transmission. Such an event can occur during a collision, since data and carrier indications can be corrupted by the superimposition of the two packets. During the last one-third of the IPG, the MB86967 ignores the occurrence of a carrier indication, in accordance with 8802-3, to ensure fairness and equality in access to the network. Thus, if one station begins transmission slightly ahead of another, there is no advantage to the earlier start. Both nodes transmit, a collision occurs, and backoff interval differentials resolve the media-access contention.

8.2 Transmit Packet Processing

To transmit one or more packets, the host system first loads the packet(s), preceded by a two-byte header giving their lengths, into a transmit buffer by writing the data to the Buffer Memory Port Register, BMPR8. Only the destination address, source address, length and data fields of the packets are loaded by the system. After the

packets are loaded into the transmit buffer, the system turns the transmitter on to initiate transmission. Observing the media access protocol, the MB86967 defers transmitting to carrier from other nodes, minimum interpacket gap intervals and backoff intervals, if any, and then begins to serialize the data. It generates the Preamble field at the beginning, and calculates and appends the CRC field at the end. Figure 7 illustrates the standard packet format. The serialized signal is routed to the transceiver section which encodes the data into the required Manchester code, appends an end-of-packet delimiter.

The transmitter transmits the packets in the transmit buffer in the order in which they were loaded. If a collision is detected by the transceiver, the transmitter automatically retransmits the packet until successful or until 16 consecutive attempts have ended in collision. In the latter case, depending on the mode selection made at initialization time, the transmitter continues to try to transmit the same packet starting again with a collision count of zero, skips the current packet and tries to transmit the next packet starting with a collision count of zero, or halts and waits for instruction from the host. In the last case, the host can elect to terminate transmission attempts by setting ENADLC, DLCR6<7> to one, continue to attempt to transmit the same packet (collision counter reset), or skip the current packet and try to transmit the next packet(collision count is zero).

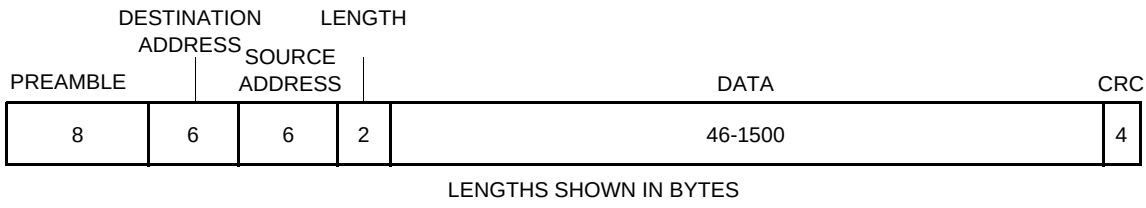


Figure 7 Packet Format

8.3 Backoff Generator

A 17-bit pseudo-random number generator clocked at the 10 MHz bit rate provides the collision backoff function. Distances between stations become part of the randomizing function. The number generator is sampled at the time of collision, masking all but the appropriate number of bits specified by the 8802-3 backoff algorithm. This value is then counted down at the slot-time rate (512 bit times) to generate the backoff interval. For a first collision, only one bit is used, giving a backoff of either 51.2 microseconds or 0. For a second consecutive collision, two bits are used, and so forth, up to ten bits. From the tenth to the 16th collisions, 10 bits are used. This generates a pseudo-random backoff interval of from 0 to 52.38 ms, the so-called ‘binary exponential backoff’ for collisions per the 8802-3 standard.

8.4 Transmit Error Processing

The MB86967 provides four transmit error status bits in its Transmit Status Register (DLCR0) for reporting the four possible transmit errors. The errors are: 1) loss of carrier during transmission, which usually indicates a medium fault or a collision, 2) collision, 3) 16 consecutive collisions and 4) jabber error, which occurs if the length of a single transmission substantially exceeds the time required to transmit a maximum length packet conforming to the standard. The latter three can be enabled separately to generate interrupts.

A status bit in the Transmit Status Register is set in case a collision terminates transmission. Collision counter DLCR4<7:4>, automatically increments after each collision up to the sixteenth collision, at which time it rolls over to zero. Another status bit indicates that sixteen consecutive attempts to transmit a packet have been made and all have been terminated by collision. The occurrence of 16 collisions may indicate a network problem, such as a disconnected cable or terminator, that produces false collisions. While rare, 16 collisions may normally occur.

8.5 Time Domain Reflectometry

When a node transmits, a short or open on the network causes a reflected signal to the node receiver, which can sometimes be detected. The reflection causes failure of the carrier sense or detection of a false collision. An open on the network may cause a false collision, whereas a short usually causes loss of carrier sense. Time domain reflectometry (TDR) allows estimates of the distance along the network cable from the node to the fault.

The MB86967 is equipped with a special counter to perform the TDR function. The contents of the counter after any transmission can be determined by reading the Time Domain Reflectometry registers, DLCR14 (the least-significant byte) and DLCR15 (the most-significant byte). Only the lower 14 bits of the counter are equipped, which is more than is needed for an IEEE or Ethernet LAN. The top two bits, DLCR15<7:6>, are always 0. The TDR counter counts the actual number of bits transmitted for each packet before a collision indication, carrier loss indication or completion of transmission, whichever comes first. A complete transmission with no error indications clears the TDR counter. The elapsed time represents twice the signal delay from node to fault.

To perform the TDR fault test, first enable interrupts for TMT OK, by setting DLCR2<7> high. An alternative to using the interrupt is to poll the TMT OK bit, looking for a high level. Set the 16 Collisions Register, BMPR11, to 07H for this test (no halt, skip-failed packet). Clear status bits by writing 0FF86H to the Receive and Transmit Status registers. Next, try to transmit a packet length of 600 or more bits. Up to 16 attempts may be made automatically, if collisions are indicated. Upon completion of the transmission attempts, TMT OK goes high, generating an interrupt if so enabled. When this occurs, read the Transmit Status register and the TDR register.

8.6 Interpreting the Results

If the count is zero, no fault was detected. If the count is greater than zero, but smaller than the packet length, a cable fault may exist. If the count is less than 525, a real collision may have occurred during the test. Real collisions normally occur within the first 65 bytes of the packet, including preamble. Note the error status bits, COL and CR LOST. COL high suggests a cable open, whereas CR LOST suggests a short. Repeat the measurement several times, discarding any anomalous values, and average the rest. A cluster of readings at about the same value is a strong indicator of a valid fault measurement. If such a cluster of readings occurs, multiply the average of the cluster by 39 feet to estimate the distance from the node to the fault. [39 feet = (100 ns $\times$ 0.8 $\times$ 186,282 miles/second $\times$ 5280 feet/mile)/2; this assumes the network is mostly coaxial cable with signal propagation speed of approximately 0.8 $\times$ C, the speed of light.]

9. Receiver Circuits

The receiver includes a receive state machine, serial-to-parallel conversion, pipe-line FIFO, preamble recognition, bit and byte-framing, address filtering, CRC and other error checking. Additional circuits involved in packet reception are described in the Transceiver section of this document.

The receiver state machine provides sequencing of events for the receiver, including idle, busy, address filtering, and data storage, detects receive error conditions and sets appropriate bits within the DLC registers. A small data FIFO provides elastic buffering for synchronization with the buffer controller timing and buffering of data while the buffer controller is servicing other buffer memory access requests.

9.1 Monitoring the Network

Whenever the data link section is enabled (ENA DLC bit, DLCR6<7>, is set to zero), the MB86967 constantly monitors the network for carrier. Signals that exceed the AC and DC squelch thresholds of the transceiver cause the internal carrier sense line to assert, which in turn causes the receiver to attempt to receive a packet. (The transmitter also uses the carrier sense function to defer to transmissions from other nodes.)

The receiver monitors the serial data stream from the transceiver for the end-of-preamble bit pattern, a four-bit pattern of 1011 ending the preamble's pattern of alternating ones and zeros. This pattern also provides byte

and field synchronization for the receiver; the bit immediately following the end of preamble is the first bit of the first byte of the packet's destination address field.

When packet transmission is unflawed, carrier sense remains asserted for the duration of the packet, negating just after the last bit of the CRC field is received, when the transceiver detects the end-of-packet symbol at the end of the packet. Loss of carrier sense at any other time may also result from a collision or other network problems.

9.2 Address Filtering

A receive packet can be filtered by applying selectable criteria to the contents of its Destination Address field, which is the first data-bearing field following immediately after the Preamble. There are several control bits in the MB86967's registers which provide programmablility of the filter criteria. The contents of the Destination Address field can be of three basic types. The first data type which can occur in this 48-bit field is a single node address, the unique, single-node address, globally registered with the IEEE. This data type is indicated by a "0" in the first bit position of the address. The second type is the multicast address, an address for a pre-defined group of nodes. The multicast address is indicated by a "1" in the first bit position of the address. The MB86967 filters multicast addresses using a hash function and a 64-bit hash table. Thirdly, a broadcast address is defined as a special case of the multicast address which addresses all nodes on the local network. This address value consists of all "1"s. The MB86967 provides programmable address filtering logic for each of these address types.

Among the address filtering selections possible with the MB86967 are the following examples:

1. All Pass (no filtering)
2. Node address and broadcast packets only
3. Node address xxx.xxx, multicast addresses yyy.yyy and zzz.zzz and broadcast packets only

9.3 Hash Table

The Hash Table provides a way to filter incoming multicast packets so the host processor need not process packets that are not of interest. The principle behind this filtering process is based on the arrangement of a large number of elements of an array, or database, to facilitate searching for elements associated with a given key or datum. The hash function is a mathematical or logical function that maps all elements in a domain onto a smaller domain called the hash table.

Assume this hashing function as an example: treat the multicast address as a nonnegative 48-bit integer, divide this number by 64 and take the remainder. This function maps all multicast addresses into a 64-element hash table because the remainder must be an integer between 0 and 63. Applying this hashing function results in taking the least-significant six bits of the multicast address as an integer. In the hash table, for each element, 0 through 63, a single bit is stored to indicate if the address is accepted (1) or rejected (0). If, for example, the node belongs to three multicast groups, only three or fewer of the hash table elements store ones, and the rest store zeroes. The scheme allows the acceptance of any number of addresses, including all of them. However, while this filters out most nonspecific addresses, there may be addresses not of interest used on the network that also fall into the accept elements, so filtering may be imperfect.

The actual hashing function used in the MB86967 is to calculate the CRC on the multicast address and to store the most-significant six bits of this calculation in a register . The six bits are used to address the elements of the hash table: the three MSBs are used as the Hash Table register address, and the three LSBs are used as the bit address within a register byte. If the addressed Hash Table element yields a '1' and the packet is a multicast packet (first bit of destination address equals 1), and it passes the error filters, the packet will be accepted. The hash filter criteria are only used on multicast addresses, which all start with a one. Node IDs that start with a zero are not filtered by the hash filter. The broadcast address, a special case of the multicast set wherein all the bits are ones, is accepted anyway unless the Reject All Packets mode is selected.

The hash filter is used only when the Address Filter mode select bit AF1 is 1 and mode select bit AF0 is 0, selecting the Node ID, Broadcast, Multicast + Hash Table mode. Hash Table registers should only be accessed when the Receiver is disabled, i.e., when ENA DLC is high, to avoid interaction with the Receiver. There are eight bytes of registers in the Hash Table containing 64 one-bit elements, as shown in the Table 7.

9.4 Receive Packet Processing

As a packet arrives from the network, its destination address field is tested for the various address filter criteria selected by the Address Filter Mode bits, DLCR5<1:0>, and the Hash Table. Only if the address meets the filter criteria selected will the packet be accepted for storage in the receive buffer. In addition, the packet must be error-free, unless the chip has been enabled to receive flawed packets for diagnostic purposes. If these conditions are met, the packet reception results in the packet being stored in the buffer, its 4-byte header being updated at the end of reception, the BUF EMPTY status bit, DLCR5<6>, being cleared, the RX PKT status bit, DLCR1<7>, being set high and an interrupt being generated if so enabled. The last four bytes of the packet are the CRC field and are checked for correct CRC. The CRC bytes are not transferred to the Receive Buffer. If the packet has an error and reception of such packets has not been enabled, it will be discarded and pointers will be reset to reuse the same portion of the receive buffer for the next packet to arrive. If a flawed packet is accepted for storage for diagnostic purposes, its error(s) will be reported in the status byte of its header (see Receive Packet Header section).

9.5 Receive Error Processing

Status bits in the receive status register are set to indicate errors associated with packet reception. These errors are: 1) bus read error, which occurs if the host system attempts to read from an empty receive buffer (this need never occur if the RX BUF EMPTY bit is checked), 2) short packet error, 3) alignment error (incomplete byte fragment at end of packet), 4) CRC error and 5) buffer overflow, which occurs if the receive buffer space is insufficient to hold the entire received packet (the receive controller automatically removes such packets from the receive buffer and packets already stored in the buffer are not lost). Each of these receive error conditions may optionally generate an interrupt. None of these errors requires special host processing or intervention, other than optional tallying of the error for network management purposes.

10. 10BASE-T Transceiver

The MB86967's transceiver section provides the electrical interface for RJ45 (10BASE-T) connections to the Ethernet local area network. Its functions include Manchester encoding and decoding of serial data streams to the transmitter and from the receiver, level conversion, collision detection, signal quality error (SQE) and link integrity testing, jabber control, loopback, and automatic correction of polarity reversal on the twisted-pair input. Also provided are outputs for transmit, collision and link test pass LEDs, and compatibility with unshielded twisted-pair cables. Receive threshold can be reduced to allow an extended range between nodes in low-noise environments. Programmable functions are controlled via BMPR13. Transceiver status is presented in BMPR15.

10.1 Data Encoder

The encoder converts the serialized NRZ data from the transmitter to Manchester code, the format used on the network medium. In Manchester code a one is represented as a bit cell (nominally 100-nanoseconds) starting with a low, ending with a high, with a low-to-high transition at the midpoint; Manchester code for a zero is the inverse.

The encoder also monitors the state of the internal transmit enable signal from the transmitter section and appends an end-of-packet symbol (illegal Manchester code) to the data stream when that signal is negated at the end of the CRC field of the transmitted packet.

10.2 Transmitter Circuits

The transceiver's transmitter section receives the encoded data from the Manchester encoder and the twisted-pair network via the TPO circuit. Advanced integrated pulse-shaping produces an output signal that is predistorted and prefiltered to meet the 10BASE-T jitter template on the TPON and TPOP pins.

During idle periods, the MB86967 transmits link integrity test pulses on the TPO circuit if LINK TEST EN, BMPR13<5>, is asserted.

10.3 Jabber Control

An on-chip watchdog timer prevents the chip from locking into a continuous transmit mode. When a transmission exceeds the maximum time limit (specified for the MB86967 as 20 to 150 msec), the watchdog timer disables the transmit and loopback functions and asserts the JABBER error status bit, DLCR0<3>, generating an interrupt if so enabled. Before the MB86967 can exit the jabber state, the transmit data circuit must remain idle for between 0.25 and 0.75 seconds.

10.4 SQE Test

The transceiver supports the signal quality error (SQE) test function specified in the standard. After every successful transmission on the 10BASE-T network, the MB86967 transceiver section transmits the SQE signal to the controller for 10±5 bit times over the internal CI circuit. BMPR15<1> reflects the status of this SQE test.

10.5 Receive Input Circuits

Valid received signals from the twisted-pair network connection (the TPI circuit) pass through on-chip filters to the data decoder.

An internal intelligent squelch function discriminates noise from link test pulses and valid data streams. The receiver is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the receiver enters the idle state.

10.6 Data Decoder

The data decoder section performs three functions on the received data: clock recovery, carrier detection, and Manchester data decoding. Carrier detection is indicated to the receiver section by assertion of the internal carrier sense signal, which occurs shortly after the received data signals appear. Carrier sense status can be monitored via DLCR0<6>. Clock recovery and data separation are accomplished by an internal phase-locked loop. The recovered clock is supplied to the receiver together with the recovered NRZ serial data stream.

10.7 Reverse Polarity

The transceiver polarity reverse circuit uses link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the transceiver enters the link fail state and no valid data or link pulses are received within 96 to 128 milliseconds, polarity resets to the default uninverted condition. If Link Integrity testing is disabled, polarity detection is based only on received data.

The transceiver automatically corrects reversed polarity. Polarity reversal is reported via BMPR15<3>.

10.8 Collision Detection

The collision detection function operates on the twisted-pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The transceiver reports collisions to the back-end via an internal signal. If the TPI circuit is active while there is activity on the TPO circuit, the TPI data passes to the back-end as received data, disabling normal loopback.

10.9 Loopback

The MB86967 provides the automatic local loopback function specified by the 10BASE-T standard for the twisted-pair port. This function is in effect except when the LBC bit, DLCR4<1>, is asserted. Data transmitted by the transmitter is passed through the data encoder, internally looped back within the MB86967 before the TPO drivers to the data decoder and returned to the receiver. This local loopback function is disabled when a data collision occurs, clearing the received data circuit in the transceiver for the data arriving at the twisted-pair inputs. The local loopback is also disabled during the link fail and jabber states.

The MB86967 provides additional loopback testing functions controlled by LBC. When the twisted-pair port is selected and LBC is asserted, the loopback is forced regardless of the state of the TPI inputs or link test failure.

During loopback, data is routed from the transmit buffer to the transmit section of the data link controller, through the Manchester encoder, back through the Manchester decoder, through the receiver section of the data link controller, and is then stored in the receive buffer. Software can then read and check the received packet that has traveled through the MB86967 transmit and receive sections. Receipt of the loopback data into the receive buffer can be disabled by asserting FILTER SELF RX, BMPR14<0>. The transmitted data is blocked from appearing at the network outputs while the MB86967 is in forced loopback mode (LBC asserted).

10.10 Link Integrity Test

The link integrity test determines the status of the receive side twisted-pair cable. Link integrity testing is enabled when LINK TEST EN, BMPR13<5>, is set low. When enabled, the receiver recognizes the link integrity pulses transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 to 150 milliseconds, the MB86967 enters a link-fail state and disables the transmit and automatic local loopback functions. The MB86967 ignores any link integrity pulse with an interval less than 2 to 7 milliseconds. The MB86967 remains in the link-fail state until it detects either a serial data packet or two or more link integrity pulses.

■ CONTROL REGISTERS IN LAN CONTROLLER

These control registers are used in all modes (PC card mode, ISA bus mode, and general-purpose bus mode).

The I/O address space between the base and 0 to F addresses has 32 control registers in the LAN controller for two address-extended bits (RBS1 and RBS0). The two address-extended bits (RBS1 and RBS0) are at bits 3 and 2 of the control register DLCR7 in the LAN controller (base address +7).

Notes:1. At reset, the LAN controller defaults to the 8-bit system interface. However, in the PC card mode, the 8-bit or 16-bit interface is set by bit 5 (IOIS8) of CCR1 at switching from the IC memory interface to the I/O card interface according to the CCR setting condition.
2. The PC card mode does not support DMA.

1. Arrangement of Registers

Register name	Symbol	System address				Register bank	
		SA3/PA3	SA2/PA2	SA1/PA1	SA0/PA0	RBS1	RBS0
Transmit status	DLCR0	0	0	0	0	×	×
Receive status	DLCR1	0	0	0	1	×	×
Transmit interrupt enable	DLCR2	0	0	1	0	×	×
Receive interrupt enable	DLCR3	0	0	1	1	×	×
Transmit mode	DLCR4	0	1	0	0	×	×
Receive mode	DLCR5	0	1	0	1	×	×
Control 1	DLCR6	0	1	1	0	×	×
Control 2	DLCR7	0	1	1	1	×	×
Node ID 0	DLCR8	1	0	0	0	0	0
Node ID 1	DLCR9	1	0	0	1	0	0
Node ID 2	DLCR10	1	0	1	0	0	0
Node ID 3	DLCR11	1	0	1	1	0	0
Node ID 4	DLCR12	1	1	0	0	0	0
Node ID 5	DLCR13	1	1	0	1	0	0
TDR0	DLCR14	1	1	1	0	0	0
TDR1	DLCR15	1	1	1	1	0	0
Multicast address 0	MAR8	1	0	0	0	0	1
Multicast address 1	MAR9	1	0	0	1	0	1
Multicast address 2	MAR10	1	0	1	0	0	1
Multicast address 3	MAR11	1	0	1	1	0	1
Multicast address 4	MAR12	1	1	0	0	0	1
Multicast address 5	MAR13	1	1	0	1	0	1
Multicast address 6	MAR14	1	1	1	0	0	1
Multicast address 7	MAR15	1	1	1	1	0	1
Buffer memory port	BMPR8	1	0	0	0	1	0
Transmit packet count	BMPR10	1	0	1	0	1	0
16 collision	BMPR11	1	0	1	1	1	0
DMA enable	BMPR12	1	1	0	0	1	0
DMA burst/transceiver mode	BMPR13	1	1	0	1	1	0
Receive control/transceiver interrupt	BMPR14	1	1	1	0	1	0
Transceiver status/control	BMPR15	1	1	1	1	1	0

2. Explanation of Control Registers in LAN Controller

2.1 Data Link Controller Register

(1) DLCR0: Transmit Status Register

DLCR0 indicates the transmit status of the data link controller. The external interrupt $\overline{INT}$ is asserted by setting the bits of DLCR2 corresponding to the status bits, bit 7 and bit 3 to 0.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	TMT OK	NET BSY	TMT REC	SRT RKT	JABBER	COL	16 COL	BUS WR ERR
Write	BIT CLR	—	—	—	BIT CLR	BIT CLR	BIT CLR	BIT CLR
Initial Value	0	Undefined	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7	TMT OK (Transmit O.K)	Read	0	Indicates transmission in progress
			1	This bit is set automatically when transmission of all packets in the transmitter buffer is completed. In the single buffer mode, the next transmit data can be transferred from the host system. In the dual buffer mode, transmission of data from the second bank can be started (Bit 7 (TMST) of the BMR10 is set). The dual buffer mode permits transfer of the next transmit data from the host system to one buffer, while the other buffer is transmitting packets.
		Write	0	Not affected
			1	This bit is cleared.
6	NET BSY (Net Busy)	Read	0	Indicates network empty (no carrier detected)
			1	Indicates network in use (carrier detected)
		Write	—	Not affected
5	TMT REC (Transmit Packet Receive)	Read	0	Indicates packets transmitted by this register not received normally. This bit is cleared automatically at the start of transmission of each packet.
			1	Indicates packets transmitted by this register received normally. This bit must not be used in normal operation.
		Write	—	Not affected
4	SRT PKT (Short Packet)	Read	0	No short packet error. This bit is cleared automatically at the start of transmission of each packet.
			1	Indicates network carrier detect disappeared during packet transmission. This bit is usually set in the event of a packet collision or physical damage to the cable.
		Write	—	Not affected

(Continued)

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Bit no.	Bit name	Operation	Value	Function
3	JABBER	Read	0	No jabber
			1	Indicates transmission suspension with continuous transmission over specified time detected by internal watchdog timer
		Write	0	Not affected
			1	This bit is cleared.
2	COL (Collision Error)	Read	0	No collision error
			1	Indicates occurrence of packet collision on network during packet transmission. The data link controller performs retransmission automatically until 16 collisions occur. The count of collision can be checked by reading bits 7 to 4 of the collision counter register DLCR4.
		Write	0	Not affected
			1	This bit is cleared.
1	16COL (16 Collision Error)	Read	0	No 16 collision error
			1	Indicates collisions occurred 16 times continuously during packet transmission. The operation after 16 collision errors can be set using bits 2 and 1 of the 16 collision control register BMPR11.
		Write	0	Not affected
			1	This bit is cleared.
0	BUS WR ERR (Bus Write Error)	Read	0	No bus write error
			1	Indicates LSI failed to assert RDY signal within 2.15 μs at writing transmit data from system to transmitter buffer. In other words, transmit data could not be written because the transmitter buffer is full. This bit is never set at transmitting based on the normal operation flow.
		Write	0	Not affected
			1	This bit is cleared.

(2) DLCR1: Receive Status Register

DLCR1 indicates the receive status of the data link controller. The external interrupt $\overline{INT}$ is asserted by setting the bits of DLCR3 corresponding to the status bits, bit 7 to 0.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	PKT RDY	BUS RD ERR	DMA EOP	RMT RST	RX SRT PKT	ALG ERR	CRC ERR	OVRFLO
Write	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR	BIT CLR
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function	
7	PKT RDY (Packet Ready)	Read	0	No received packet is in the receiver buffer.	
			1	Indicates packets from self office received normally and transferred completely to receiver buffer. In other words, at least one packet of receive data is in the receiver buffer.	
		Write	0	Not affected	
			1	This bit is cleared. If there are still received packets in the receiver buffer even after the host system has read one packet of receive data from the receiver buffer, this bit is automatically reset.	
6	BUS RD ERR (Bus Read Error)	Read	0	No bus read error	
			1	Indicates LSI failed to assert RDY signal within 2.15 µs at reading data in receiver buffer from host system. In other words, the host system attempted to read data from the receiver buffer, although the buffer has no data to read.	
		Write	0	Not affected	
			1	This bit is cleared.	
5	DMA EOP	Read	0	Indicates DMA transfer not yet completed during DMA transfer. This bit is cleared when both the DMA RENA and DMA TENA bits of the BMPR12 are cleared.	* : This bit is invalid in the PC card mode.
			1	Indicates DMA transfer completed and EOP signal asserted by external DMA controller	
		Write	0	Not affected	
			1	This bit is cleared. This clearing should be done by clearing both the DMA RENA and DMA TENA bits of the BMPR12.	

(Continued)

(Continued)

Bit no.	Bit name	Operation	Value	Function
4	RMT RST (Remote Reset)	Read	0	The received packet is not a remote reset packet.
			1	Indicates value of data length field in received packet is 0900_H. This bit is set only when the ENA RMT RST bit of DLCR5 is set and a physical address match occurs; it is not set for the multicast address and broadcast address. It is also not set when the ENA SRT PKT bit of DLCR5 is set.
		Write	0	Not affected
			1	This bit is cleared. It is also cleared automatically at the start of receiving the next packet.
3	RX SRT PKT (Short Packet)	Read*	0	No short packet error
			1	Indicates data length (address + data length + data) of received packet not more than minimum data length (60 bytes). This bit is set for not more than 6 bytes when the ENA SRT PKT bit of DLCR5 is set. It is not set when a collision occurs at the self-TXPKT.
		Write	0	Not affected
			1	This bit is cleared.
2	ALG ERR (Alignment Error)	Read*	0	No alignment error
			1	Indicates CRC of received packet incorrect and bit count of received data not multiple of 8
		Write	0	Not affected
			1	This bit is cleared.
1	CRC ERR (CRC Error)	Read*	0	No CRC error
			1	Indicates CRC of received packet incorrect. This bit is not set when a collision occurs at the self-TXPKT.
		Write	0	Not affected
			1	This bit is cleared.
0	OVRFLO (Overflow Error)	Read*	0	No overflow error
			1	Indicates that data erased because data length of received packet larger than free capacity of receiver buffer memory. Even when this bit is set, data is received normally when the data length of the next packet is smaller than the free capacity of the receiver buffer memory. This bit is set to indicate that the receiver buffer memory is almost full; transfer data immediately from the buffer to the host system. This bit is not set in the loopback mode.
		Write	0	Not affected
			1	This bit is cleared.

* : The bit 3 to bit 0 are cleared when the new packet is received.

(3) DLCR2: Transmit Interrupt Enable Register

The DLCR2 register enables a transmit interrupt. When the bit corresponding to the status bit of DLCR0 is set to 1, the external interrupt $\overline{INT}$ is asserted when the status bit is set.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	ENA TMT OK	0	0	0	ENA JABBER	ENA COL	ENA 16COL	ENA BUS WR ERR
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7	ENA TMT OK	Read/Write	0	Disables TMT OK interrupt
			1	Enables TMT OK interrupt
6 to 4	Not used	Read/Write	—	The read value is always 0. Write 0 to these bits at writing.
3	ENA JABBER	Read/Write	0	Disables JABBER interrupt
			1	Enables JABBER interrupt
2	ENA COL	Read/Write	0	Disables COL interrupt
			1	Enables COL interrupt
1	ENA 16COL	Read/Write	0	Disables 16COL interrupt
			1	Enables 16COL interrupt
0	ENA BUS RD ERR	Read/Write	0	Disables BUS RD ERR interrupt
			1	Enables BUS RD ERR interrupt

(4) DLCR3: Receive Interrupt Enable Register

The DLCR3 register enables a receive interrupt. When the bit corresponding to the status bit of DLCR1 is set to 1, the external interrupt $\overline{INT}$ is asserted when the status bit is set.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	ENA PKT RDY	ENA BUS RD ERR	ENA DMA EOP	ENA RMT RST	ENA RX SRT PKT	ENA ALG ERR	ENA CRC ERR	ENA OVRFLO
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function	
7	ENA PKT RDY	Read/Write	0	Disables PKT RDY interrupt	
			1	Enables TMT OK interrupt	
6	ENA BUS RD ERR	Read/Write	0	Disables BUS RD ERR interrupt	
			1	Enables BUS RD ERR interrupt	
5	ENA DMA EOP	Read/Write	0	Disables DMA EOP interrupt	* : This bit is invalid in the PC card mode.
			1	Enables DMA EOP interrupt	
4	ENA RMT RST	Read/Write	0	Disables RMT RST interrupt	
			1	Enables RMT RST interrupt	
3	ENA RX SRT ERR	Read/Write	0	Disables RX SRT ERR interrupt	
			1	Enables RX SRT ERR interrupt	
2	ENA ALG ERR	Read/Write	0	Disables ALG ERR interrupt	
			1	Enables ALG ERR interrupt	
1	ENA CRC ERR	Read/Write	0	Disables CRC ERR interrupt	
			1	Enables CRC ERR interrupt	
0	ENA OVRFLO	Read/Write	0	Disables OVRFLO interrupt	
			1	Enables OVRFLO interrupt	

(5) DLCR4: Transmit Mode Register

DLCR4 sets the transmitter operation modes, and displays the count of collision occurrence.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	COL3	COL2	COL1	COL0	TST1	$\overline{\text{CNTRL}}$	$\overline{\text{LBC}}$	DSC
Write	—	—	—	—	0			
Initial Value	0*	0*	0*	0*	0	1	1	0

Bit no.	Bit name	Operation	Value	Function	
7 to 4	COL3 to COL0 (Collision Count)	Read	—	Displays count of collision until transmission completed. These bits are cleared at the completion of transmission.	
3	TST1 (Chip Test 1)	Read/Write	—	This is a chip test bit. Always write 0 to this bit at writing to DLCR4. 1 cannot be written to this bit during normal operation.	
2	$\overline{\text{CNTRL}}$ (DREQ Control)	Read/Write	0	The DREQ signal is negated in the last cycle of DMA transfer.	* : This bit is invalid in the PC card mode.
			1	The DREQ signal is negated two cycles before the last cycle of DMA transfer.	
1	$\overline{\text{LBC}}$ (Loopback Control)	Read/Write	0	Forced to enter loopback mode. The loopback is not canceled even when a collision is detected. Transmit data is not output from the TPOP*/TPON* pin.	
			1	Enters standard loopback mode specified in 10BASE-T standard. The loopback function works only at data transmission. The transmit data is loopbacked to the receiver by the encoder/decoder. If the MB86967 is in the link fail and jabber states when a collision is detected, the loopback mode is canceled and signals are accepted from the twisted-pair board.	
0	DSC (Disable Carrier Detec)	Read/Write	—	When this bit is set to 1, the MB86967 is enabled for duplex transmission. In this case, data can be transmitted irrespective of the state of the receiver, enabling external loopback operation.	

* : These bits are undefined until the first packet is completely transmitted after power-on.

(6) DLCR5: Receive Mode Register

DLCR5 sets the receiver operation mode, and displays the status of the receiver buffer memory.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	TST2	BUF EMP	ACPT BAD PKT	ADD SIZE	ENA SRT PKT	ENA RMT RST	AM1	AM0
Write	0	—						
Initial Value	0	1	0	0	0	0	0	1

Bit no.	Bit name	Operation	Value	Function
7	TST2 (Chip Test 2)	Read/Write	—	This is a chip test bit. Always write 0 to this bit at writing to DLCR5. Writing 1 to this bit is prohibited during normal operation.
6	BUF EMP (Buffer Empty)	Read	0	Indicates valid data remaining in receiver buffer memory
			1	Indicates no valid data in receiver buffer memory
		Write	—	Not affected
5	ACPT BAD PKT (Bad Packet Receive)	Read/Write	0	If the received packet has short packet, alignment, and CRC errors, it is discarded and is not transferred to the receiver buffer.
			1	A packet with short packet, alignment, and CRC errors is transferred to the receiver buffer like a normally-received packet.
4	ADD SIZE (Address Size)	Read/Write	0	Compares destination addresses of receive packet and ID addresses of node for match at all 6 bytes (48 bits)
			1	Compares destination addresses of received packet and ID addresses of node for match only at upper byte and 5 bytes (40 bits)
3	ENA SRT PKT (Enable Short Packet Receive)	Read/Write	0	A packet of more than 60 bytes and less than 2 Kbytes can be received.
			1	A packet of more than 6 bytes and less than 2 Kbytes can be received. The value of this bit is ignored when bit 5 (ACPT BAD PKT) is set.
2	ENA RMT RST (Enable Remote Reset)	Read/Write	0	The remote reset packet is not detected.
			1	Checks whether value of data length field in receive packet is 0900_H
1 and 0	AM1, AM0 (Address Match Mode)	Read/Write	—	Selects node ID address match detect mode at packet receiving (Tables 3 and 4)

Table 3 Receiving Packets from Other Nodes

AM1 DLCR5 Bit 1	AM0 DLCR5 Bit 0	$\overline{\text{LBC}}$ DLCR4 Bit 1	SELF RX BMPR14 Bit 0	Physical Packet		Broadcast Packet	Multicast Packet	
				ID Match	ID Mismatch		Lower ID Match*1	Address Filter*2
0	0	×	×	Discarded	Discarded	Discarded	Discarded	Discarded
0	1	0	×	Discarded	Discarded	Discarded	Discarded	Discarded
0	1	1	×	Received	Discarded	Received	Received	Discarded
1	0	0	×	Discarded	Discarded	Discarded	Discarded	Discarded
1	0	1	×	Received	Discarded	Received	Discarded	Discarded
1	1	0	×	Discarded	Discarded	Discarded	Discarded	Discarded
1	1	1	×	Received	Received	Received	Received	Received

Table 4 Receiving Packets Transmitted from Self Office

AM1 DLCR5 Bit 1	AM0 DLCR5 Bit 0	$\overline{\text{LBC}}$ DLCR4 Bit 1	SELF RX BMPR14 Bit 0	Physical Packet		Broadcast Packet	Multicast Packet	
				ID Match	ID Mismatch		Lower ID Match*1	Address Filter*2
0	0	×	×	Discarded	Discarded	Discarded	Discarded	Discarded
0	1	0	×	Received	Discarded	Received	Received	Discarded
0	1	1	×	Received	Discarded	Discarded	Discarded	Discarded
1	0	0	×	Received	Discarded	Received	Discarded	Received
1	0	1	×	Received	Discarded	Discarded	Discarded	Discarded
1	1	0	×	Received	Received	Received	Received	Received
1	1	1	0	Received	Received	Received	Received	Received
1	1	1	1	Discarded	Discarded	Discarded	Discarded	Discarded

*1: Lower ID Match: Receive the packets because a match occurs at the 24 lower bits of the node ID and bit 0 of the node ID register is 1.

*2: Address Filter: Receive the packets because bit 0 of the node ID register is 1 and the CRC value of the node ID register is selected by the multicast address register.

(7) DLCR6: Control Register 1

DLCR6 sets the MB86966 operation modes.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	$\overline{\text{ENA}}$ DLC	100NS/ $\overline{\text{150NS}}$	SB/$\overline{\text{SW}}$	BB/$\overline{\text{BW}}$	TX BUF SIZE 1	TX BUF SIZE 0	BUF SIZE 1	BUF SIZE 0
Initial Value	1	0	1	1	0	1	1	0

Bit no.	Bit name	Operation	Value	Function
7	$\overline{\text{ENA}}$ DLC (Enable Data Link Controller)	Read/Write	0	When 0 is written to this bit, the MB86967 is ready for transmitting and receiving. When this bit is 0, the node ID register and multicast address register cannot be accessed.
			1	The data link controller and buffer manager in the MB86967 are initialized and both the transmitter and receiver buffers are also initialized.
6	100NS/$\overline{\text{150NS}}$ (SRAM Cycle Time Select)	Read/Write	0	Sets cycle time of external SRAM to 150 ns
			1	Sets cycle time of external SRAM to 100 ns. In this case, use SRAM with an access time of 80 ns or less.
5	SB/$\overline{\text{SW}}$ (System Bus Width Select)	Read/Write	—	Selects width of system data bus **SB/$\overline{\text{SW}}$ / System Data Bus** 0 / 16 bit 1 / 8 bit • PC Card Mode When 1 is written to bit 5 (IOIS8) of the CCR1, the SB/-SW bit is set to 1, placing the system data bus in the byte transfer mode. When 0 is written, the SB/-SW bit is set to 0, placing the system data bus in the word transfer mode. In the PC card mode, writing to the SB/-SW bit is performed by CCR1. Writing from DLCR6 does not affect bit 5. • General-purpose Bus Mode The reversed value of the SB/$\overline{\text{SW}}$ bit is output to the external pin SB/$\overline{\text{SW}}$.
4	BB/$\overline{\text{BW}}$ (Buffer Memory Bus Width)	Read	1	The width of the buffer memory data bus is fixed to 8 bits. The read value of this bit is always 1.
		Write	—	Not affected
3 and 2	TX BUF SIZE 1 TX BUF SIZE 0 (Transmitter Buffer Size)	Read/Write	—	Sets size of transmitter buffer. **TX BUF SIZE 1 / TX BUF SIZE 0 / Bank Capacity / Bank Count / Buffer Capacity** 0 / 0 / 2 Kbyte / 1 / 2 Kbyte 0 / 1 / 2 Kbyte / 2 / 4 Kbyte 1 / 0 / 4 Kbyte / 2 / 8 Kbyte 1 / 1 / 8 Kbyte / 2 / 16 Kbyte

(Continued)

* : This register is accessible only for the device initialization.

(Continued)

Bit no.	Bit name	Operation	Value	Function
1	BUF SIZE 1	Read/Write	—	Sets size of external buffer memory (transmitter buffer size + receiver buffer size) BUF SIZE 1: 0 → Buffer Size: 8 Kbyte; 1 → 32 Kbyte
0	BUF SIZE 0	Read	0	The read value of this bit is fixed at 0.
		Write	—	Not affected

(8) DLCR7: Control Register 2

DLCR7 sets the MB86967 operation modes.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	IDENT1	IDENT0	$\overline{\text{STBY}}$	RDYPOL	RBS1	RBS0	EOP/$\overline{\text{EOP}}$	BYTE SWAP
Write				—				
Initial Value	1	0	1	×	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7 and 6	IDENT1 IDENT0	Read	—	Reading the initial values of these bits permits checking the type of controller used in software. Read values 10: MB86967 Read values 11: MB86965A Read values 01: MB86964 Read values 00: MB86960A Writing to these bits is invalid.
5	$\overline{\text{STBY}}$	Read/Write	0	The LAN controller is placed in the standby mode. In the standby mode, the clock stops, reducing current consumption to about 10%. When 1 is prewritten to bit 4 of BMPR14, the MB86967 enters the shutdown mode. In this mode, the crystal oscillator stops, reducing the current consumption to about 1%. In the PC card mode, when the PwrDwn bit of CCR1 is set to 1, this bit is set to 0. Writing from DLCR7 to this bit is prohibited.
			1	Operating state (not standby state). In the PC card mode, when the PwrDwn bit of CCR1 is set to 0, this bit is set to 1. Writing from DLCR7 to this bit is prohibited. Return from the shutdown mode by resetting.
4	RDYPOL	Read	—	The value of the external pin RDYPOL can be read. In the PC card mode, the read value is always 1. In the ISA bus mode, the read value of this bit is always 0.
		Write	—	Not affected

(Continued)

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Bit no.	Bit name	Operation	Value	Function
3 and 2	RBS1 RBS0	Read/Write	—	The MB86967 has three internal register sets. Bank switching by these bits allows the system to access each register set. DLCR0 to DLCR7 can always be accessed irrespective of the conditions of register banks.

RBS1	RBS2	Address 00_H to 07_H	Address 08_H to $0F_H$
0	0	DLCR0 to DLCR7	DLCR8 to DLCR15
0	1	DLCR0 to DLCR7	MAR8 to MAR15
1	0	DLCR0 to DLCR7	BMPR8 to BMPR15
1	1	DLCR0 to DLCR7	Reserved

Bit no.	Bit name	Operation	Value	Function	
1	EOP/$\overline{EOP}$	Read/Write	0	Sets DMA end signal (EOP) input pin Active Low	* : This bit is invalid in the PCMCIA mode.
			1	Sets DMA end signal (EOP) input pin Active High	
0	BYTE SWAP	Read/Write	0	When the system bus is the 16-bit mode, byte swapping is not performed for access to BMPR8. The bus is an Intel 16-bit bus.	* : Writing 1 to this bit is prohibited in the PC card mode. Always write 0 to this bit.
			1	When the system bus is the 16-bit mode, byte swapping is performed for access to BMPR8, switching between upper and lower data. The bus is a Motorola 16-bit bus.	

(9) DLCR8 to DLCR13: Node ID Registers

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLCR8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
DLCR9	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
DLCR10	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
DLCR11	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
DLCR12	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
DLCR13	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40

DLCR8 to DLCR13 store the node ID of the self office. After comparing the destination addresses in the receive packet with the values of the node ID registers, the matching packets are received according to the setting conditions of the Address Match Mode bits of DLCR5.

Usually, set bit 0 (ID 0) of DLCR8 to 0 (When bit 0 of the destination address is 1, the received data serve as the multicast address and the packet is received according to the setting conditions of the Address Match Mode bits of DLCR5, irrespective of their values).

The initial values of the node ID registers are undefined. Reading and writing are possible only when bit 7 ($\overline{ENA}$ DLC) of DLCR6 is 1.

(10) DLCR14 and DLCR15: TDR Registers

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLCR14	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
DLCR15	0	0	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

DLCR14 and DLCR15 are 14-bit counters that are reset at the start of transmission to count the transmit bits until a collision occurs or the carrier is dropped.

They are read-only registers. The read values of bits 7 and 6 of DLCR15 is always 0.

2.2 Multicast Address Registers

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MAR8	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
MAR9	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
MAR10	MID23	MID22	MID21	MID20	MID19	MID18	MID17	MID16
MAR11	MID31	MID30	MID29	MID28	MID27	MID26	MID25	MID24
MAR12	MID39	MID38	MID37	MID36	MID35	MID34	MID33	MID32
MAR13	MID47	MID46	MID45	MID44	MID43	MID42	MID41	MID40
MAR14	MID55	MID54	MID53	MID52	MID51	MID50	MID49	MID48
MAR15	MID63	MID62	MID61	MID60	MID59	MID58	MID57	MID56

The multicast address registers select the multicast address packet to receive when the Address Match Mode bits of DLCR5 are set to 1 and 0, respectively. Multicast addresses are input to a 32-bit CRC circuit and grouped into 64 by the six rightmost bits of the calculated CRC. Packets with multicast addresses of groups in which set the bits corresponding to the multicast address registers are received.

The initial values of the multicast address registers are undefined. Reading and writing are possible only when bit 7 ($\overline{\text{ENA}}$ DLC) of DLCR6 is 1.

2.3 Buffer Memory Port Registers

(1) BMPR8: Buffer Memory Port

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BMPR8	BMP7	BMP6	BMP5	BMP4	BMP3	BMP2	BMP1	BMP0
	BMP15	BMP14	BMP13	BMP12	BMP11	BMP10	BMP9	BMP8

BMPR8 is a data port for transferring transmit and receive data between the host system and buffer memory. When the system interface is in the byte mode, BMPR8 serves as an 8-bit I/O port. When the system interface is in the 16-bit bus mode, BMPR8 serves as a 16-bit I/O port. In the 16-bit bus mode, other registers can be accessed in both bytes and words, but this register can be accessed only in words.

In the 16-bit bus mode, setting bit 0 (BYTE SWAP) of DLCR7 permits order swapping between MSB and LSB, allowing this register to work with both Intel and Motorola processors.

(2) BMPR10: Transmit Packet Count Register

BMPR10 sets the transmit start bit and transmit packet count.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	0	TX PKT CNT 6	TX PKT CNT 5	TX PKT CNT 4	TX PKT CNT 3	TX PKT CNT 2	TX PKT CNT 1	TX PKT CNT 0
Write	TMST							
Initial Value	0	×	×	×	×	×	×	×

Bit no.	Bit name	Operation	Value	Function
7	TMST	Read	0	The read value of this bit is always 0.
		Write	0	Not affected
			1	Starts transmitting packet. When the transmitter buffer is in the single buffer mode, set this bit after transferring the transmit packet from the host to the transmit buffer. When the transmitter buffer is in the dual buffer mode, set this bit after transferring the transmit packet to the transmitter buffer and completing transmission of the packet to the second bank (after the TMT OK bit of DLCR0 is set).
6 to 0	TX PKT CNT 6 to 0	Read	—	These bits are decremented each time transmission of one packet is completed, and display the count of packets that have not been transmitted yet. They are set to 00H after all packets have been transmitted.
		Write	—	The MB86967 can start transmitting more than one packet using one transmit command. Set the TMST bit and write the transmit packet count (the count of packet transferred to buffer memory).

(3) BMPR11: 16 Collision Control Register

BMPR11 controls operation of the data link controller after a 16 collisions occur.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	0	0	0	0	0	16COL CNTL 2	16COL CNTL 1	16COL CNTL 0
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7 to 3	Not used	Read	0	The read values of these bits is always 0.
		Write	0	Writing 1 is prohibited. Always write 0 at writing.
2 to 0	16COL CNTL 2 to 0	Read/ Write	—	See tables below.

16COL CNTL			Operation after 16COLs Occur
2	1	0	
1	1	0	Similar to ordinary collisions, the transmit packet causing 16COLs is retransmitted automatically (Auto Mode).
1	1	1	The next packet is transmitted automatically after skipping the transmit packet causing the 16COLs (Auto Mode).
0	1	×	When 16COLs occur, stop the transmitted data link controller temporarily. To resume transmission, write the values listed in the table below to this register. These values are valid only when written. Write them to this register each time transmission stops after 16COLs occur (Manual Mode).

16COL CNTL			Operation when Resuming Transmission in Manual Mode
2	1	0	
0	1	0	Similar to ordinary collisions, the transmit packet causing 16COLs is retransmitted.
0	1	1	The next packet is transmitted after skipping the transmit packet causing the 16COLs.

(4) BMPR12: DAM Enable Register

The BMPR12 controls DMA transfer between the host system and the MB86967.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	×	×	×	×	LONGPKT RCV DIS	0	DMA RENA	DMA TENA
Write	0	0	0	0				
Initial Value	×	×	×	×	0	0	0	0

Bit no.	Bit name	Operation	Value	Function	
7 to 4	Not used	Read	—	The read values of these bits are always undefined.	
		Write	0	Writing 1 is prohibited. Always write 0 at writing.	
3	LONGPKT RCV DIS	Read/Write	0	The receive long packet removal function is enabled. Packets with a length of 1792 bytes or more are not received.	
			1	The receive long packet removal function is disabled. Packets with a length of up to 2047 bytes cannot be received normally.	
2	Not used	Read/Write	—	The read value of this bit is always 0. Writing 1 is prohibited. Always write 0 at writing.	
1	DMA RENA	Read/Write	0 (*1)	DMA read operation is disabled.	* : Writing 1 to this bit is prohibited in the PC card mode. Always write 0 to this bit.
			1 (*2)	DMA read operation (reading from receiver buffer) is enabled.	
0	DMA TENA	Read/Write	0 (*1)	The DMA write operation is disabled.	
			1 (*2)	The DMA write operation (writing to receiver buffer) is enabled.	

*1: The DLCR1 DMAEOP bit is cleared if the DMA RENA bit and DMA TENA bit are set to “00”.
*2: Writing “11” to both DMA RENA bit and DMA TENA bit is prohibited.

(5) BMPR13: DMA Burst/Transceiver Mode Control Register

The BMPR13 sets the DMA transfer cycle count between the host system and MB86967 and the operation modes of the 10BASE-T transceiver.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read / **Write**	I/O BASE UNLOCK	0	LINK TEST ENA	0	0	0	DMA BRST 1	DMA BRST 0
Initial Value	1	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7	I/O BASE UNLOCK	Read/Write	0	The I/O base address is not changed even after an I/O-read operation to address X12H.
			1	An I/O-read operation to address X12H increments the values of the I/O base address select signals (IOSEL0 to IOSEL2), causing a change in the I/O base address (This is valid only in the jumperless ISA bus mode).
6	Not used	Read/Write	—	The read value of this bit is always 0. Writing 1 is prohibited. Always write 0 to this bit at writing.
5	LINK TEST ENA	Read/Write	0	The link test on the 10BASE-T transceiver is enabled.
			1	The link test on the 10BASE-T transceiver is disabled.
4 to 2	Not used	Read/Write	—	The read values of these bits is always 0. Writing 1 is prohibited. Always write 0 to these bits at writing.
1 and 0	DMA BRST 1 and 0	Read/Write	—	The DMA transfer cycle count is set by one bus request (These bits are invalid in the PC card mode).

BRST1	BRST0	DAM Transfer Cycle Count (Max.)
0	0	1 (single DMA)
0	1	4
1	0	18
1	1	12

(6) BMPR14: Receiver Control/Transceiver Interrupt Enable/Shutdown Register

BMPR14 controls interrupts from the receiver buffer pointer and 10BASE-T transceiver.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	0	ENA LKF INT	0	SHUT DWN MODE	TST3	SKIP RX PKT	ENA SQE INT	ENA FILTER
Write					0			
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7	Not used	Read/Write	—	The read value of this bit is always 0. Always write 0 to this bit at writing.
6	ENA LKF INT	Read/Write	0	The link fail interrupt is disabled.
			1	The link fail interrupt is enabled.
5	Not used	Read/Write	—	The read value of this bit is always 0. Always write 0 to this bit at writing.
4	SHUT DWN MODE	Read/Write	0	When bit 5 ($\overline{\text{STBY}}$) of DLCR7 is set, the MB86967 enters the standby state (oscillation continues).
			1	When bit 5 ($\overline{\text{STBY}}$) of DLCR7 is set, the MB86967 enters the shutdown state (oscillation stops).
3	TST3 (Chip Test 3)	Read/Write	—	This a chip test bit. Always write 0 to this bit at writing to the BMPR14. Writing 1 to this bit during normal operation is prohibited.
2	SKIP RX PKT	Read/Write	0	Skipping the receiver buffer pointer is completed.
			1	The receiver buffer pointer is being skipped (updated), indicating the transient state from when 1 is written to this bit until skipping the pointer is completed (about 200 ns).
			0	Not affected. The receiver buffer pointer is not skipped.
			1	When 1 is written to this bit, the receiver buffer pointer is skipped up to the beginning of the next packet. This bit is cleared automatically when skipping is completed. If the packet to be skipped is the last one in the receiver buffer, the BUF EMP bit of DLCR5 is set after the receiver buffer pointer is skipped. This function works only after reading the receive packet header (4 bytes). And, it is prohibited to write “1” when the remainder of the packet becomes 8-byte.
1	ENA SQE INT	Read/Write	0	The signal quality error interrupt is disabled.
			1	The signal quality error interrupt is enabled.
0	FILTER SELF RX	Read/Write	0	When the Address Match Mode bits AM1 and AM0 are 11, the packet transmitted from the self office is also received.
			1	When the Address Match Mode bits AM1 and AM0 are 11, the packet transmitted from the self office is not received.

(7) BMPR15: Transceiver Status Control Register

BMPR15 indicates the status of the 10BASE-T transceiver.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	0	LKF	0	0	POL REV	0	SQE	0
Write		BIT CLR			BIT CLR		BIT CLR	
Initial Value	0	×	0	0	×	0	0	0

Bit no.	Bit name	Operation	Value	Function	
7	Not used	Read/Write	—	The read value of this bit is always 0. Writing 1 is prohibited. Always write 0 to this bit at writing.	
6	LKF	Read	0	No link fail is detected.	
			1	A link fail is detected.	
		Write	0	Not affected	
			1	This bit is cleared.	
5 and 4	Not used	Read/Write	—	The read value of this bit is always 0. Writing 1 is prohibited. Always write 0 to this bit at writing.	
3	POL REV	Read	0	Polarity reversal is not detected.	
			1	Polarity reversal is detected.	
		Write	0	Not affected	
			1	This bit is cleared.	
2	Not used	Read/Write	—	The read value of this bit is always 0. Writing 1 is prohibited. Always write 0 to this bit at writing.	
1	SQE	Read	0	An SQE error is not detected.	* : The read value of this bit is always 0 when bit 0 of DLCR4(DSC: Disable Carrier Detect) is enabled (1).
			1	An SQE error is detected.	
		Write	0	Not affected	
			1	This bit is cleared.	
0	Not used	Read/Write	—	The read value of this bit is always 0. Writing 1 is prohibited. Always write 0 to this bit at writing.	

■ EXPLANATION OF ISA BUS MODE

1. Jumperless ISA Mode

In this mode, the LAN controller reads the I/O addresses and interrupt outputs from initialization data in external E²PROM after the hardware reset at power-on, and initializes them. It takes about 50 µs until initialization is completed.

This eliminates the need for on-board DIP switches for address decode selection. The initialization data can be changed because the E²PROM can be read and written. Utilities for changing initialization data allow an inexperienced user to retrieve contentions between I/O addresses and mount a LAN interface card in any personal computer.

Only one byte is used for the initialization data in the E²PROM. Second and later bytes should be used to store node ID. Data (node ID) at the second and later bytes should be read bit-by-bit, converted to parallel data, and then written to the node ID registers (DLCR8 to DLCR15).

1.1 Setting at E²PROM

The initial values should be prewritten to the first byte in the E²PROM as shown in Figure 8; the node ID should be prewritten to the second and later bytes.

After a hardware reset, the LAN controller reads the initialization data at the first one byte in E²PROM automatically, and sets it at the BMPR19 internal register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTSEL1	INTSEL0	Not used			IOSEL2	IOSEL1	IOSEL0

Setting Interrupt Channels

INTSEL1	INTSEL0	Interrupt Channel (Pin)
0	0	IRQ0
0	1	IRQ1
1	0	IRQ2
1	1	IRQ3

Setting I/O Addresses

IOMSEL2	IOMSEL1	IOMSEL0	I/O Base Address
0	0	0	260H to 27FH
0	0	1	280H to 29FH
0	1	0	2A0H to 2BFH
0	1	1	240H to 25FH
1	0	0	340H to 35FH
1	0	1	320H to 33FH
1	1	0	380H to 39FH
1	1	1	300H to 31FH

Figure 8 Configuration of Bits at First One Byte in E²PROM

1.2 Setting I/O Base Addresses

After completing jumperless initialization, read 8 bytes (DLCR0 to DLCR7) of the registers in the LAN controller using the system software and check that the initial values in these registers have been read correctly. If they are not read correctly, the I/O addresses are assumed to overlap other I/O addresses, and must be changed. To make a change, read BMPR18 (the read value is meaningless). Each time BMPR18 is read, the values of IOSEL2 to IOSEL0 are incremented from 000 to 111 and the updated values become valid in BMPR19.

When the I/O addresses are updated until the values of DLCR0 to DLCR7 can be read properly, the LAN controller is located at the correct I/O addresses. After the I/O addresses have been defined, to prevent them being updated in error when BMPR18 is read, clear bit 7 (I/O BASE UNLOCK) of BMPR13.

When the I/O address values found by the above operation are prewritten to E^2PROM, the above operation is not needed at the next system startup, which reduces the system startup overhead. Consequently, the above retrieval of I/O addresses is required only when the LAN interface board is first installed in a personal computer.

1.3 Setting Interrupt Signals

The LAN controller has four interrupt output pins. The interrupt output pin from which interrupt signals should be output can be specified by initialization data in E^2PROM. If contention occurs between the interrupt signals and other I/O devices, the address decoder cannot be updated like the I/O addresses. Write another address decode value to E^2PROM and then restart the system. Repeat the above process until interrupt signals are allocated to the correct address area.

1.4 Restarting System

To restart the system, perform a hardware reset or a write operation to the reset registers RESET0 to RESET7 (any data can be written to any of RESET0 to RESET7). The write operation provides the same condition as the hardware reset except that BMPR16 and BMPR17 are not initialized.

Initialization takes about 50 μs after canceling a hardware reset, or completing a write operation at the reset registers.

2. Jumper + E^2PROM ISA Mode

This mode is the jumperless ISA mode without automatic initialization function. The I/O addresses are set by external pins. The interrupt output pin is fixed at IRQ0. The E^2PROM interface functions only to store node ID. Read and write operations from and to E^2PROM are performed by the system software. After converting read serial data to parallel data, write the data to the node ID registers (DLCR8 to DLCR15).

3. Performance Comparison between Jumperless ISA Mode and Jumper + E^2PROM ISA Mode

	Jumperless ISA Mode	Jumper + E^2PROM ISA Mode
Automatic initialization	○	×
E^2PROM interface	○ (Required)	○ (Option)
Interrupt output selection	○	×

4. Register Arrangement

Registers accessible only in the ISA mode are listed below.

Register Name	Symbol	System Address					Register Bank	
		SA4	SA3	SA2	SA1	SA0	RBS1	RBS0
E^2PROM control	BMPR16	1	0	0	0	0	×	×
E^2PROM data	BMPR17	1	0	0	0	1	×	×
I/O base address	BMPR18	1	0	0	1	0	×	×
Jumperless setting	BMPR19	1	0	0	1	1	×	×
Reserved	—	1	0	1	0	0	×	×
Reserved	—	1	0	1	0	1	×	×
Reserved	—	1	0	1	1	0	×	×
Reserved	—	1	0	1	1	1	×	×
Reset 0	RES0	1	1	0	0	0	×	×
Reset 1	RES1	1	1	0	0	1	×	×
Reset 2	RES2	1	1	0	1	0	×	×
Reset 3	RES3	1	1	0	1	1	×	×
Reset 4	RES4	1	1	1	0	0	×	×
Reset 5	RES5	1	1	1	0	1	×	×
Reset 6	RES6	1	1	1	1	0	×	×
Reset 7	RES7	1	1	1	1	1	×	×

5. BMPR16: E^2PROM Control Register

BMPR16 controls external E^2PROM.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	×	×	×	×	×	×	×	×
Write	0	ESK	ECS	0	0	0	0	0
Initial Value	×	0	0	×	×	×	×	×

Bit no.	Bit name	Operation	Value	Function
7	Not used	Read	—	The read value of this bit is undefined.
		Write	0	Always write 0 to this bit at writing.
6	ESK	Read	—	The read value of this bit is undefined.
		Write	—	Shift clocks to E^2PROM are generated by repeatedly writing 1 or 0 to this bit.
5	ECS	Read	—	The read value of this bit is undefined.
		Write	—	When 1 is written to this bit, the E^2PROM chip select signal is asserted. When 0 is written to this bit, the E^2PROM chip select signal is negated.
4 to 0	Not used	Read	—	The read values of these bits are undefined.
		Write	0	Always write 0s to these bits at writing.

6. BMPR17: E²PROM Data Register

BMPR17 is an external E²PROM data port.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	EDIO	×	×	×	×	×	×	×
Write		0	0	0	0	0	0	0
Initial Value	0	×	×	×	×	×	×	×

Bit no.	Bit name	Operation	Value	Function
7	EDIO	Read	—	Port for reading output data from E²PROM
		Write	—	Port for writing input data to E²PROM
6 to 0	Not used	Read	—	The read values of these bits are undefined.
		Write	0	Always write 0s to these bits at writing.

7. BMPR18: I/O Base Address Register

BMPR18 updates and displays the I/O base addresses (valid only in jumperless mode).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	IOBA7	IOBA6	IOBA5	IOBA4	IOBA3	IOBA2	IOBA1	IOBA0
Write	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7 to 0	IOBA7 to IOBA0	Read	—	Each time this register is read, the I/O base address select signals (IOSEL2 to IOSEL0) are incremented to update the I/O base addresses. The updated values can be read from bits 2 to 0 of BMPR19. The read values of this register have no meaning.

8. BMPR19: Jumperless Setting Register

BMPR19 displays the initialization value in the jumperless mode (valid only in jumperless mode).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	INTSEL1	INTSEL1	×	×	×	IOSEL2	IOSEL1	IOSEL0
Write	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7 to 6	INTSEL1 INTSEL0	Read	—	Display the interrupt channels. **INTSEL1** / **INTSEL0** / **Interrupt Channel (Pin)** 0 / 0 / IRQ0 0 / 1 / IRQ1 1 / 0 / IRQ2 1 / 1 / IRQ3
5 to 3	Not used	Read	—	The read values of these bits are undefined.
2 to 0	IOSEL2 IOSEL1 IOSEL0	Read	—	Display the boot ROM addresses. **IOSEL2** / **IOSEL1** / **IOSEL0** / **I/O Base Address** 0 / 0 / 0 / 260_H to $27F_H$ 0 / 0 / 1 / 280_H to $29F_H$ 0 / 1 / 0 / $2A0_H$ to $2BF_H$ 0 / 1 / 1 / 240_H to $25F_H$ 1 / 0 / 0 / 340_H to $35F_H$ 1 / 0 / 1 / 320_H to $33F_H$ 1 / 1 / 0 / 380_H to $39F_H$ 1 / 1 / 1 / 300_H to $31F_H$

9. RES0 to RES7: Reset Registers

These 8-byte reset registers are valid only in the ISA bus mode. Writing to these registers (any data can be written to any of RES0 to RES7) allows initialization of the buffer manager, data link controller, Manchester encoder/decoder, and 10BASE-T transceiver. This writing also allows the internal registers to be initialized by a reset, but prohibits initialization of BMPR18 and BMPR19.

■ EXPLANATION OF PC CARD MODE

1. E²PROM/FLASH Interface

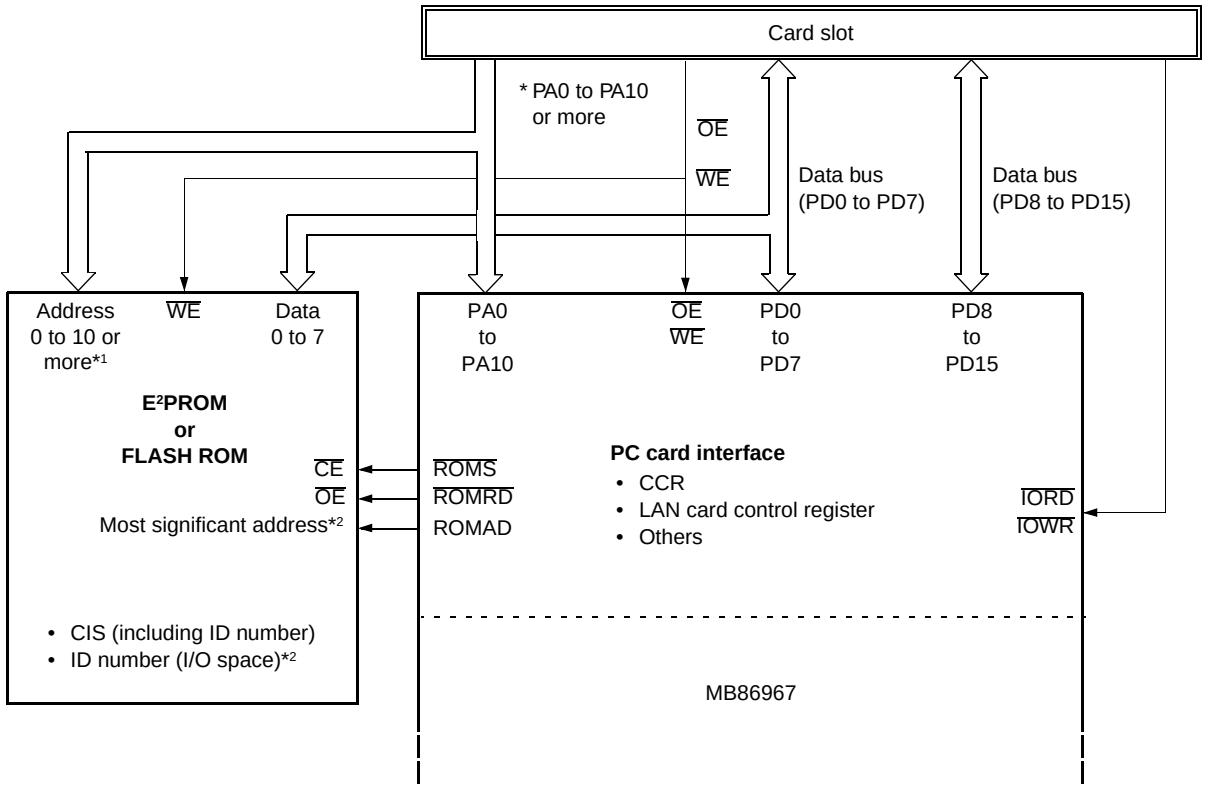


Figure 9 Example of E²PROM/FLASH Interface

*1: Changed depending on size of E²PROM or flash ROM
[Example]
PA0 to PA16 for 128-KB flash ROM

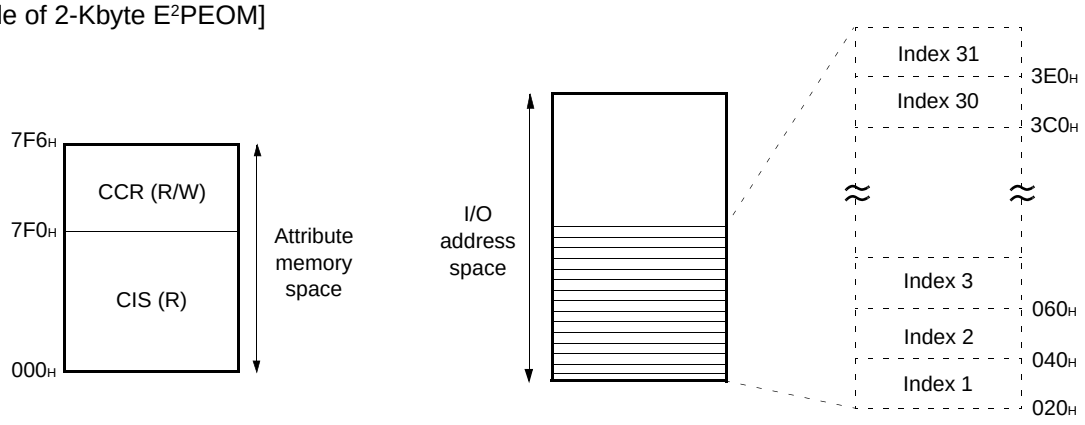
*2: To I/O-read the ID number, connect the ROMAD pin to the most significant bit of ROM. If I/O-read is not required, leave the ROMAD pin open to set the ID number in the CIS.

2. Use of E²PROM and Flash ROM

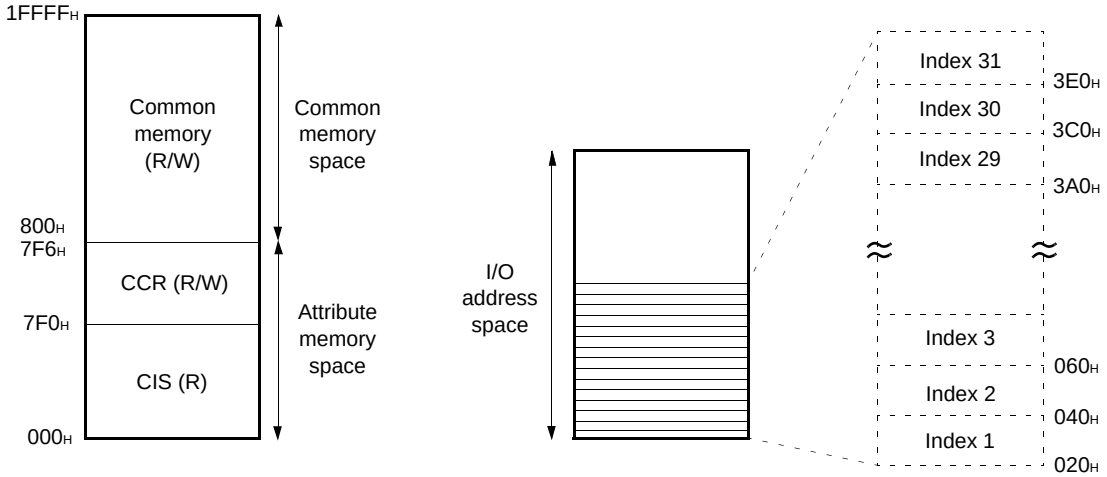
2.1 Setting ID Number in CIS

ROM Size	CIS Space	Common Memory Space	CCR Location	Address Pin from System to ROM	Address Pin from System to MB86966
128-Kbyte flash ROM	2 Kbytes	126 Kbytes	7F0H to 7F6H	A0 to A16	A0 to A10
2-Kbyte E²PROM	2 Kbytes	—	7F0H to 7F6H	A0 to A10	

[Example of 2-Kbyte E²PEOM]



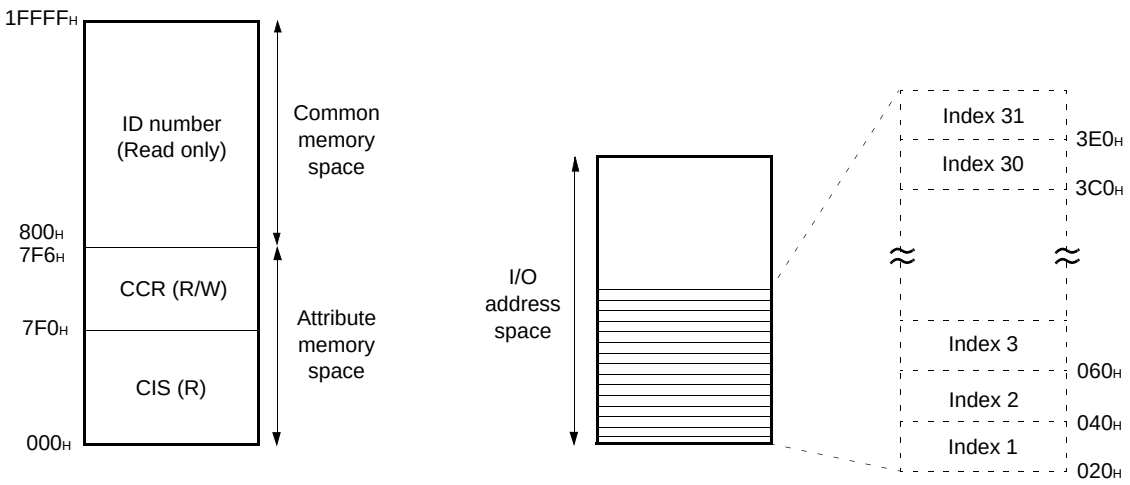
[Example of 128-Kbyte Flash ROM]



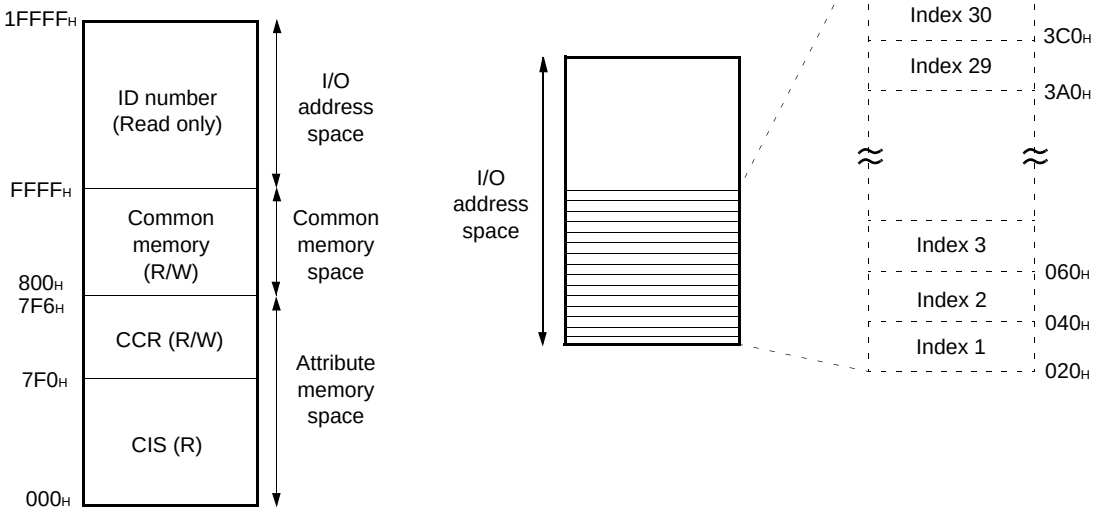
2.2 I/O-reading ID Number

ROM Size	CIS Space	Common Memory Space	I/O Space	CCR Location	Address Pin from System to ROM	Address Pin from System to MB86966	Address Pin from MB86966 to ROM
128-Kbyte flash ROM	2 Kbytes	62 Kbytes	62 Kbytes	7F0H to 7F6H	A0 to A10	A0 to A10	Connect ROMAD pin to A16.
4-Kbyte E²PROM	2 Kbytes	—	2 Kbytes	7F0H to 7F6H	A0 to A10	A0 to A10	Connect ROMAD pin to A11.

[Example of 4-Kbyte E²PEOM]



[Example of 128-Kbyte Flash ROM]



3. Address Space

The configuration of the LAN PC card in the MB86967 (in PC card mode) has up to three address spaces (for common memory, I/O memory, and attribute memory).

Table 5 gives the common memory space, I/O memory space, and attribute memory space of the MB86967.

Table 5 Memory Map for PC Card

Common Memory Space*1	I/O Memory Space	Attribute Memory Space
(E^2PROM or FLASH)	• Control registers in LAN controller (Core of LAN controller) • LAN card control register (PC card interface) • ID number (E^2PROM or FLASH)*2	• Card attribute data register (CIS) (E^2PROM or FLASH) • LAN card configuration register (CCR) (PC card interface)

Note: Parts in parentheses are the blocks where each item is located.

*1: Common memory space cannot allocated if the E^2PROM or flash ROM to be selected is less than 2 Kbytes.
*2: Connecting P97 (ROMAD) to the most significant address bit of ROM allows I/O-reading of the ID number. To write to this space, both the $\overline{IOWR}$ and $\overline{WE}$ pins must be enabled.

4. Common Memory Space

Common memory space can be used if the capacity of E²PROM or flash ROM to be selected is large. The address space is located higher than the CIS (card attribute data register) of attribute memory space (See examples of E²PROM and flash ROM in 2).

Only even addresses are used in the CIS, but both common memory space even and odd addresses can be used in common memory space. Only byte access (8 bits) is available.

Writing to common memory space is possible. Efficient writing is performed by data-polling the selected E²PROM or flash ROM. However, in this case, the PwrDwn bit of CCR1 must be not set for the power-down state without ending writing.

Batch erase should not be selected for flash ROM. When erasing common memory in blocks, take care not to erase attribute memory space.

(1) Read from Common Memory

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	1	1	0	0	1	0	Invalid	Even byte	L	L	L
						1	Invalid	Odd byte	L	L	L
Word access (16 bits)	1	0	0	0	1	×	Invalid	Invalid	H	H	L
High byte only	1	0	1	0	1	×	Invalid	Invalid	H	H	L

(2) Write to Common Memory

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	1	1	0	0	1	0	Don't care	Even byte	L	H	L
						1	Don't care	Odd byte	L	H	L
Word access (16 bits)	1	0	0	0	1	×	Don't care	Don't care	H	H	L
High byte only	1	0	1	0	1	×	Don't care	Don't care	H	H	L

5. Attribute Memory Space

Attribute memory space has the card attribute data register (CIS) and card configuration register (CCR). It can be accessed in 8 bits from even addresses; odd addresses are invalid.

The MB86967 can have access to both 8-bit and 16-bit data. When attribute memory space is accessed in the 16-bit mode, only the data signals D0 to D7 are valid, and D8 to D15 are invalid.

CIS is located at 000H to 7EEH, starting with address 0. CCR has four registers, located at 7F0H, 7F2H, 7F4H, and 7F6H.

Address	Symbol	Register
7F0H	CCR0	Card configuration option register
7F2H	CCR1	Card configuration status register
7F4H	CCR2	Pin replacement register
7F6H	CCR3	Socket/copy register

[Reference]
CIS: In E²PROM or flash ROM
CCR: In MB86967

(1) Read from CIS

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{IORD}$	$\overline{WE}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	0	1	0	0	1	1	0	Invalid	Even byte	L	L	L
							1	Invalid	Invalid	H	H	L
Word access (16 bits)	0	0	0	0	1	1	×	Invalid	Even byte	L	L	L

(2) Write to CIS

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{IOWR}$	$\overline{WE}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	0	1	0	1	1	0	0	Don't care	Even byte	L	H	L
							1	Don't care	Don't care	H	H	L
Word access (16 bits)	0	0	0	1	1	0	×	Don't care	Even byte	L	H	L

(3) Read from CCR

Mode	Address	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{IORD}$	$\overline{WE}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	7F0H to 7F6H	0	1	0	0	1	1	0	Invalid	Even byte	H	H	L
								1	Invalid	Invalid	H	H	L
Word access (16 bits)		0	0	0	0	1	1	×	Invalid	Even byte	H	H	L

(4) Write to CCR

Mode	Address	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{IOWR}$	$\overline{WE}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	7F0H to 7F6H	0	1	0	1	1	0	0	Don't care	Even byte	H	H	L
								1	Don't care	Don't care	H	H	L
Word access (16 bits)		0	0	0	1	1	0	×	Don't care	Even byte	H	H	L

6. LAN Card Configuration Register

(1) CCR0: Card Configuration Option Register (00007F0H)

The card configuration option register (CCR0) sets a software reset, interrupt signal, and configuration index.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	SRESET	LevIREQ	Configuration index					
Write		—						
Initial Value	0	1	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7	SRESET (Software Reset)	Read/Write	0	When 0 is written to this bit, the MB86967 enters the hardware reset state or the same state as that after hardware reset.
			1	Reset state; this is the same as the hardware reset state except that this bit is not cleared. When this bit is set, the pointers and registers in the LAN controller are also reset.
6	LevIREQ (Level Interrupt Request)	Read	—	Since the MB86967 is in the level interrupt request mode, 1 is always read in the I/O interface card mode. This bit is not affected by writing.
5 to 0	CONF INDX (Configuration Index)	Read/Write	—	These bits are used to select 32 configuration indexes provided for the card.

(2) CCR1: Card Configuration Status Register (00007F2H)

This register indicates the configuration status of the card.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	Changed	0	IOis8	0	0	PwrDwn	0	0
Write	—	—		—	—		—	—
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7	Changed (State Change)	Read	—	This bit is 1, indicating that the bit value (bit 5) of the pin replacement register is 1. The value of bit 5 of the pin replacement register, indicating that this bit becomes 0. This is a read-only bit and it is not affected by writing.
6	Not used	Read	—	The read value of this bit is always 0 and this bit is not affected by writing.
5	IOIS8 (8-bit I/O)	Read/Write	0	The MB86967 enters the word transfer mode (PD0 to PD15). In this case, bit 5 (SB/$\overline{SW}$) of the control register (DLCR6) in the LAN controller is set to 0.
			1	The MB86967 enters the byte transfer mode (PD0 to PD7). In this case, SB/-SW (bit 5) of DLCR6 in the LAN controller is set to 1. The system must set $\overline{CE2}$ Non-active.
4 and 3	Not used	Read	—	The read value is always 0. These bits are not affected by writing.
2	PwrDwn	Read/Write	0	This bit clears the power-down mode. When this bit is cleared, bit 5 ($\overline{STBY}$) of DLCR7 in the LAN controller is also cleared to 1.
			1	The power-down mode is set. When this bit is set, bit 5 ($\overline{STBY}$) of DLCR7 is set to 0, making it possible to place the LAN controller and 10BASE-T transceiver in the standby state. Presetting bit 4 of BMPR14 in the LAN controller causes the MB86967 to enter the shutdown mode (oscillation stopped). This bit should be set after initializing the LAN controller. Return from the shutdown mode should be made by reset. See 4. Operation Sequence in PC Card Mode.
1 and 0	Not used	Read	—	The read values of these bits is always 0. These bits are not affected by writing.

(3) CCR2: Pin Replacement Register (00007F4H)

This register indicates the card ready or busy state.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	0	0	CRdy/$\overline{\text{Bsy}}$	0	1	1	RRdy/$\overline{\text{Bsy}}$	0
Write	—	—		—	—	—		—
Initial Value	0	0	0	0	1	1	0	0

Bit no.	Bit name	Operation	Value	Function
7 and 6	Not used	Read	—	The read values of these bits is always 0. These bits are not affected by writing.
5	CRdy/$\overline{\text{Bsy}}$ (Ready/Busy State Change)	Read/Write	0	Indicates that Ready/Busy bit (bit 1) not changed (from 1 to 0 or from 0 to 1) 0 can be written to this bit only when this bit is 1 with bit 1 set to 1.
			1	Indicates that Ready/Busy changed (from 1 to 0 or from 0 to 1) 0 can be written to this bit only when this bit is 1 with bit 1 set to 1.
4	Not used	Read	—	The read value of this bit is always 0. This bit is not affected by writing.
3 and 2	Not used	Read	—	The read values of these bits is always 1. These bits are not affected by writing.
1	RRdy/$\overline{\text{Bsy}}$ (Ready/Busy)	Read/Write	0	Indicates card in busy state
			1	Indicates card in ready state In the IC memory card interface mode, such as power-on and reset a High level is output (when a write operation to the CCR is not performed).
0	Not used	Read	—	The read value of this bit is always 0. This bit is not affected by writing.

(4) CCR3: Socket/Copy Register (00007F6H)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	0	0	0	0	0	0	0	0
Write	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
0 to 7	Not used	Read	—	The read values of these bits is always 0. These bits are not affected by writing.

7. I/O Address Space

I/O address space has control registers in the LAN controller and the LAN card control register; in some cases, it has ID numbers. The MB86967 supports both the independent I/O addressing mode, and overlapping I/O addressing mode. Index 0 of the 32 I/O indexes is used to address the independent I/O, and index 31 is used to address the overlapping I/O. One index has 32 bytes of address space. In the independent I/O addressing mode, the I/O address pins A4 to A0 are used.

When using the overlapping I/O addressing mode in the ISA and EISA buses, I/O address space is allocated to any one of the 31 indexes. The system can select any I/O base address by writing different indexes to bits 0 to 5 of the card configuration option register. In this mode, all I/O address pins A0 to A10 are used.

If 32 bytes of I/O address space are allocated to the control registers in the LAN controller, the LAN card control register, and ID numbers are as follows:

Base Address	Register
+0 to F	Control registers in LAN controller
+10	LAN card control register
+12, 14, 16, 18, 1A, 1C, 1E	For setting ID numbers (only read value valid) A read value that is not used as the ID number is undefined.
+11, 13, 15, 17, 19, 1B, 1D, 1F	Reserved (The read value is undefined and writing is invalid.)

The configuration indexes and I/O base addresses to be assigned are as follows:

Index	CCR 7F0$_H$ Bit 0 to 5	I/O Address Space	Index	CCR 7F0$_H$ Bit 0 to 5	I/O Address Space
	0 0 0 0 0 0	I/O function in non-active	16	1 1 0 0 0 0	200H to 21F$_H$
0	1 0 0 0 0 0	Independent I/O addressing	17	1 1 0 0 0 1	220$_H$ to 23F$_H$
1	1 0 0 0 0 1	020$_H$ to 03F$_H$	18	1 1 0 0 1 0	240$_H$ to 25F$_H$
2	1 0 0 0 1 0	040$_H$ to 05F$_H$	19	1 1 0 0 1 1	260$_H$ to 27F$_H$
3	1 0 0 0 1 1	060$_H$ to 07F$_H$	20	1 1 0 1 0 0	280$_H$ to 29F$_H$
4	1 0 0 1 0 0	080$_H$ to 09F$_H$	21	1 1 0 1 0 1	2A0$_H$ to 2BF$_H$
5	1 0 0 1 0 1	0A0$_H$ to 0BF$_H$	22	1 1 0 1 1 0	2C0$_H$ to 2DF$_H$
6	1 0 0 1 1 0	0C0$_H$ to 0DF$_H$	23	1 1 0 1 1 1	2E0$_H$ to 2FF$_H$
7	1 0 0 1 1 1	0E0$_H$ to 0FF$_H$	24	1 1 1 0 0 0	300$_H$ to 31F$_H$
8	1 0 1 0 0 0	100$_H$ to 11F$_H$	25	1 1 1 0 0 1	320$_H$ to 33F$_H$
9	1 0 1 0 0 1	120$_H$ to 13F$_H$	26	1 1 1 0 1 0	340$_H$ to 35F$_H$
10	1 0 1 0 1 0	140$_H$ to 15F$_H$	27	1 1 1 0 1 1	360$_H$ to 37F$_H$
11	1 0 1 0 1 1	160$_H$ to 17F$_H$	28	1 1 1 1 0 0	380$_H$ to 39F$_H$
12	1 0 1 1 0 0	180$_H$ to 19F$_H$	29	1 1 1 1 0 1	3A0$_H$ to 3BF$_H$
13	1 0 1 1 0 1	1A0$_H$ to 1BF$_H$	30	1 1 1 1 1 0	3B0$_H$ to 3DF$_H$
14	1 0 1 1 1 0	1C0$_H$ to 1DF$_H$	31	1 1 1 1 1 1	3E0$_H$ to 3FF$_H$
15	1 0 1 1 1 1	1E0$_H$ to 1FF$_H$			

(1) I/O-read (+0 to +10)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{IORD}$	$\overline{OE}$	$\overline{IOWR}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	0	1	0	0	1	1	0	Invalid	Even byte	H	H	L
							1	Invalid	Odd byte	H	H	L
Word access (16 bits)	0	0	0	0	1	1	0	Odd byte	Even byte	H	H	L
High byte only	0	0	1	0	1	1	×	Even byte	Invalid	H	H	L

(2) I/O-read (+12, +14, +16, +18, 1A, 1C, 1E: ID number)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{IORD}$	$\overline{OE}$	$\overline{IOWR}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	0	1	0	0	1	1	0	Invalid	Even byte	L	L	H
Word access (16 bits)	0	0	0	0	1	1	0	Odd byte	Even byte	L	L	H

(3) I/O-write (+0 to +10)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{IORD}$	$\overline{IOWR}$	$\overline{WE}$	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	0	1	0	1	0	1	0	Don't care	Even byte	H	H	L
							1	Don't care	Odd byte	H	H	L
Word access (16 bits)	0	0	0	1	0	1	0	Odd byte	Even byte	H	H	L
High byte only	0	0	1	1	0	1	×	Even byte	Don't care	H	H	L

(4) I/O-write (+12, +14, +16, +18, 1A, 1C, 1E: ID number)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{IORD}$	$\overline{IOWR}$*	$\overline{WE}$*	PA0	PD8 to PD15	PD0 to PD7	$\overline{ROMS}$	$\overline{ROMRD}$	ROMAD
Byte access (8 bits)	0	1	0	1	0	0	0	Don't care	Even byte	L	H	H
Word access (16 bits)	0	0	0	1	0	0	0	Odd byte	Even byte	L	H	H

* : To write the ID number, both the $\overline{IOWR}$ and $\overline{WE}$ pins must be set Active.

(5) CARDCR: LAN Card Control Register (Base address +10)

This is an external ROM control register that can be accessed only in the PC card mode.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	CIS WR ENA	COMMON WR ENA	ID NUMBER WR ENA	0	0	0	0	0
Write				—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

Bit no.	Bit name	Operation	Value	Function
7	CIS WRITE ENABLE (CIS Write Enable)	Read/Write	0	The system cannot write data to CIS in E^2PROM or flash ROM.
			1	The system can write data to CIS in E^2PROM or flash ROM.
6	COMMON WR ENABLE (Common Memory Write Enable)	Read/Write	0	The system cannot write data to common memory in E^2PROM or flash ROM.
			1	The system can write data to common memory in E^2PROM or flash ROM.
5	ID NUMBER WR ENABLE (ID Number Write Enable)	Read/Write	0	The system cannot write data to I/O space (for ID number) in E^2PROM or flash ROM.
			1	The system can write data to I/O space (for ID number) in E^2PROM or flash ROM.
0 to 4	Not used	Read	—	The read values of these bits are always 0s. These bits are not affected by writing.

8. Initializing Card (Using MB86967 in PC Card)

Immediately after the card is installed in the system, the IC memory card interface (memory card) is selected.

The following instructions describe how to switch to the I/O card interface:

a. The system reads card attribute data (CIS) for setting operating environments.
b. The data is written to the card configuration register (CCR).
   At this time, the LAN controller is set to the 8-bit interface or 16-bit interface by setting the bit 5 (IOIS8) of CCR1.
c. The Ethernet ID numbers read from CIS or I/O space are written.

Note: Switch from the I/O card interface to IC memory card interface by setting the external RESET pin or the SRESET bit of CCR0.

■ RESET, STANDBY, AND SHUTDOWN MODES

1. PC Card Mode

Interface	LAN Controller		Operation
Input of 1 to external reset register			• The CCR is initialized. • The I/O card interface is switched to the IC memory interface. • The LAN controller and 10BASE-T transceiver are also initialized.
CCR0 Bit 7 SRESET = 1			Same as above, except this bit not cleared • The CCR is initialized. • The I/O card interface is switched to the IC memory interface. • The LAN controller and 10BASE-T transceiver are also initialized.
	DLCR6 Bit 7 $\overline{\text{ENA}}$ DLC = 1		• The LAN controller is initialized. The previous values of the control registers (DLCR, MAR, and BMPR) in the LAN controller are retained. • The TP or AUI transceiver is in the power-down mode.
CCR1 Bit 2 PwrDwn = 1	DLCR7 Bit 5 $\overline{\text{STBY}}$ = 0*	BMPR14 Bit 4 SHUT DWN MODE = 0	• Standby mode The clock stops and current consumption is reduced to about 10%.
		BMPR14 Bit 4 SHUT DWN MODE = 1	• Shutdown mode Crystal oscillation stops and current consumption is reduced to about 1%.

* : The $\overline{\text{STBY}}$ bit of the DLCR7 is set automatically.

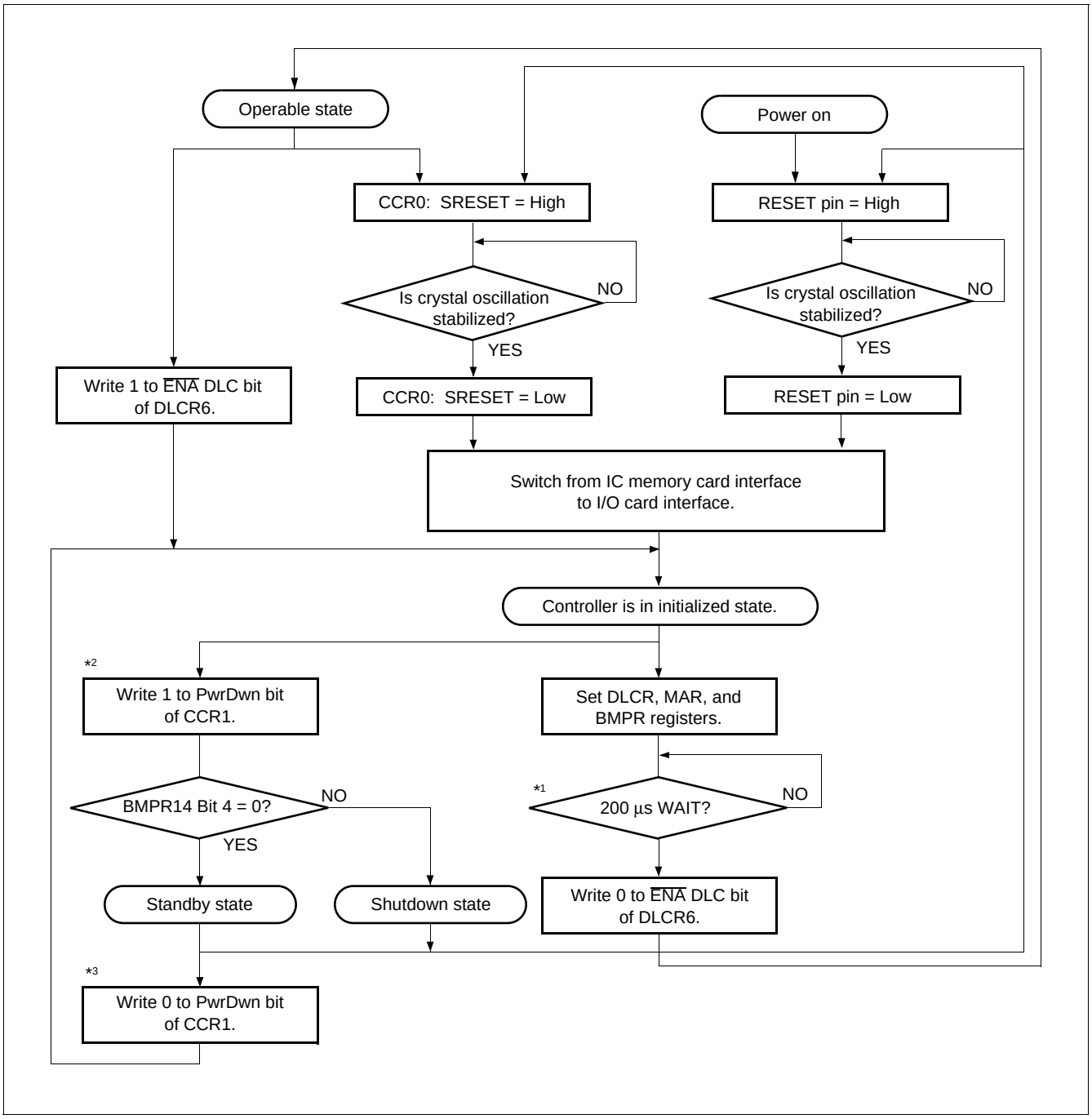
2. ISA Bus Mode

		Operation
Input of 1 to external reset register		• The LAN controller and 10BASE-T transceiver are initialized.
Write to reset registers: RES0 to RES7 (any values)		• The LAN controller and 10BASE-T transceiver are initialized but BMPR16 and BMPR17 are not.
DLCR6 Bit 7 $\overline{\text{ENA}}$ DLC = 1		• The LAN controller is initialized. The previous values of the control registers (DLCR, MAR, and BMPR) in the LAN controller are retained. • The TP transceiver is in the power-down mode.
DLCR7 Bit 5 $\overline{\text{STBY}}$ = 0	BMPR14 Bit 4 SHUT DWN MODE = 0	• Standby mode The clock stops and current consumption is reduced to about 10%.
	BMPR14 Bit 4 SHUT DWN MODE = 1	• Shutdown mode Crystal oscillation stops and current consumption is reduced to about 1%.

3. General-purpose Bus Mode

		Operation
Input of 1 to external reset register		• The LAN controller and 10BASE-T transceiver are initialized.
DLCR6 Bit 7 $\overline{\text{ENA}}$ DLC = 1		• The LAN controller is initialized. The previous values of the control registers (DLCR, MAR, and BMPR) in the LAN controller are retained. • The TP transceiver is in the power-down mode.
DLCR7 Bit 5 $\overline{\text{STBY}}$ = 0	BMPR14 Bit 4 SHUT DWN MODE = 0	• Standby mode The clock stops and current consumption is reduced to about 10%.
	BMPR14 Bit 4 SHUT DWN MODE = 1	• Shutdown mode Crystal oscillation stops and current consumption is reduced to about 1%.

4. Operation Sequence in PC Card Mode

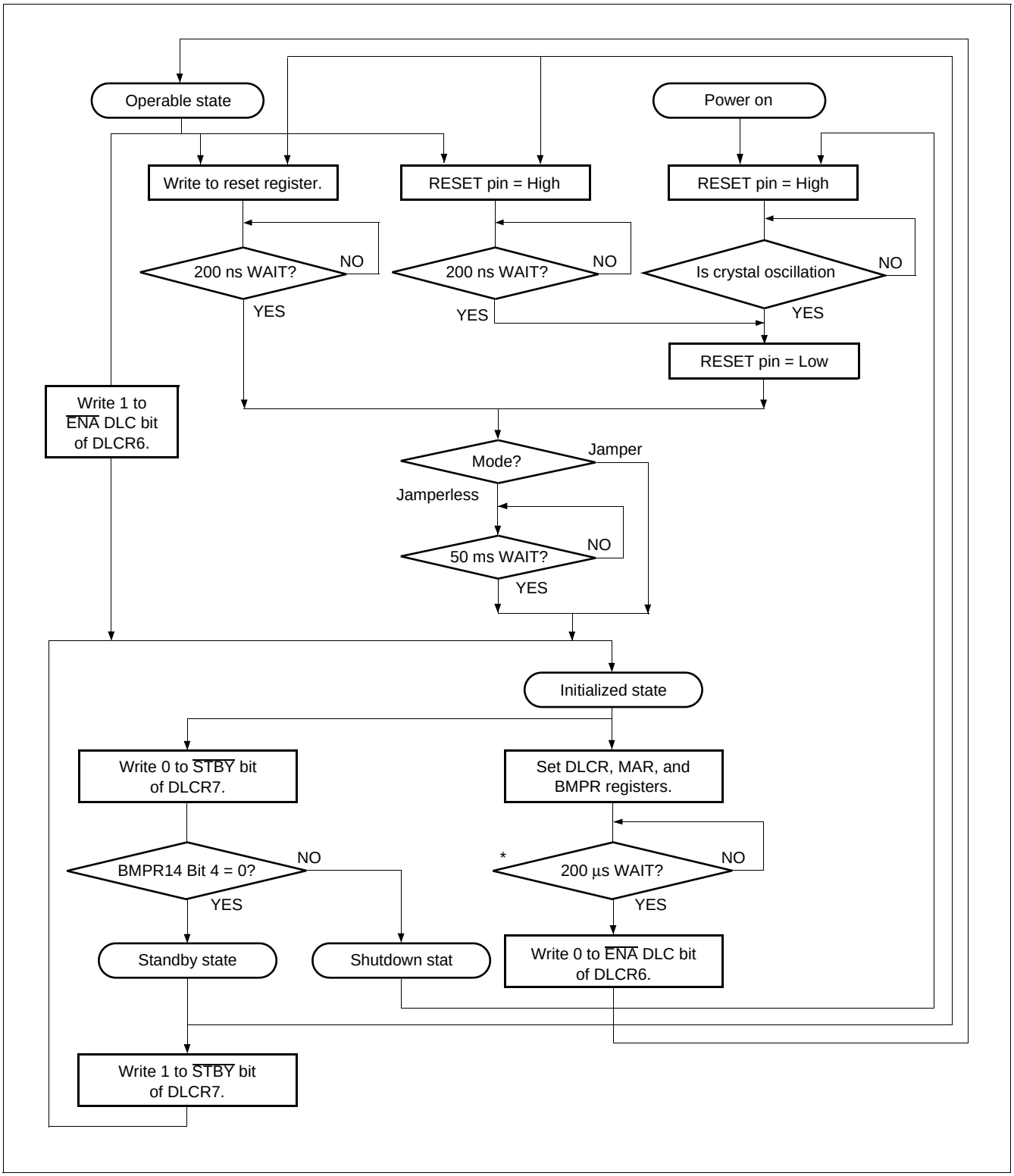


*1: The time for setting the DLCR, MAR, and BMPR registers may be included in the waiting time of 200 µs.
*2: The $\overline{\text{STBY}}$ bit of DLCR7 is automatically set to 0.
*3: The $\overline{\text{STBY}}$ bit of DLCR7 is automatically set to 1.

In the PC card mode, the $\overline{\text{STBY}}$ bit of DLCR7 is set from the PwrDwn bit of CCR1 to as shown in *2 and *3. Direct change (from 0 to 1 or from 1 to 0) is not allowed.

- Standby state: The clock to each circuit stops but crystal oscillation does not.
- Shutdown state: Crystal oscillation stops.

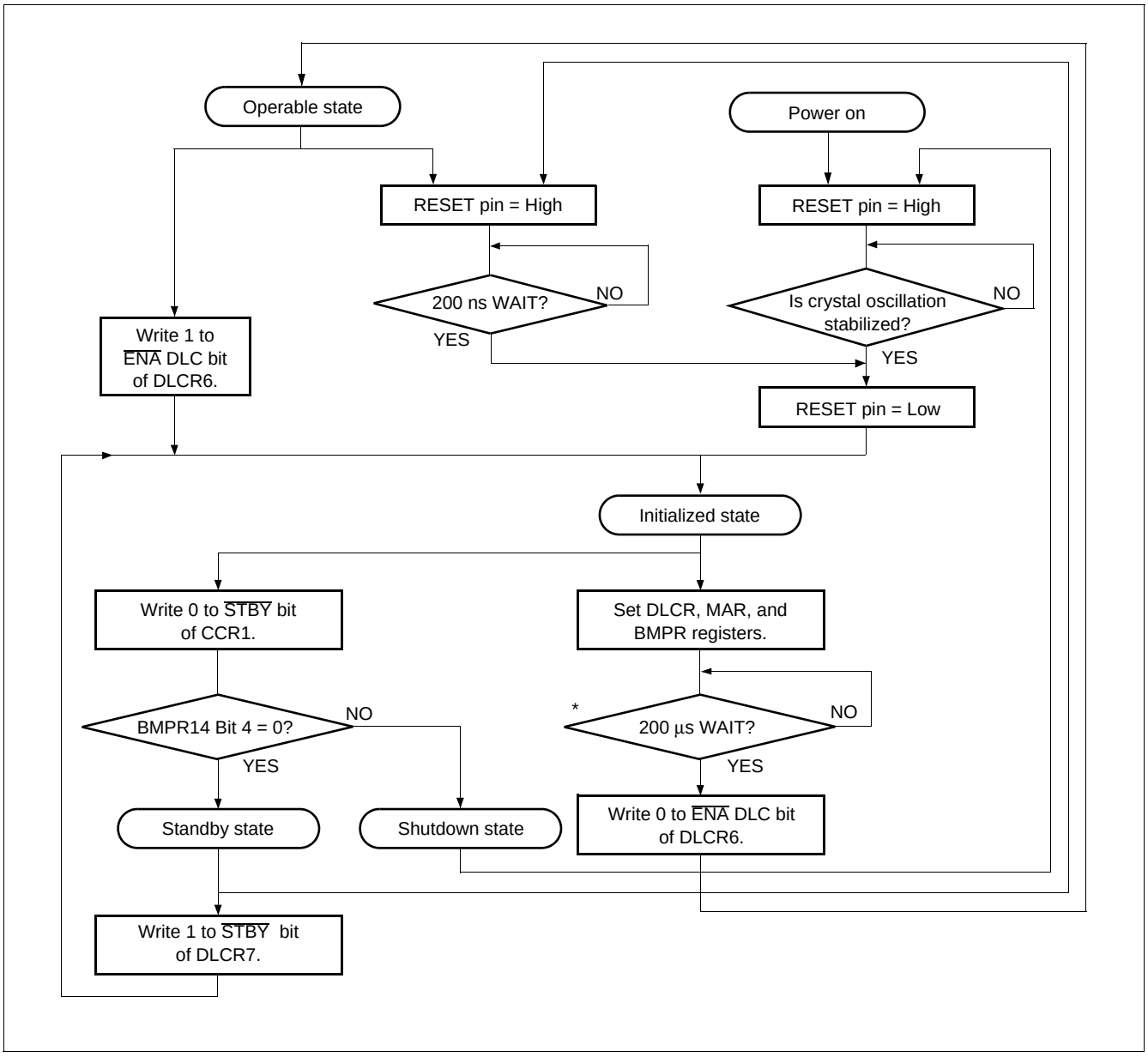
5. Operation Sequence in ISA Bus Mode



* : The time for setting the DLCR, MAR, and BMPR registers may be included in the waiting time of 200 µs.

- Standby state: The clock to each circuit stops but crystal oscillation does not.
- Shutdown state: Crystal oscillation stops.

6. Operation Sequence in General-purpose Bus Mode



* : The time for setting the DLCR, MAR, and BMPR registers may be included in the waiting time of 200 µs.

- Standby state: The clock to each circuit stops but crystal oscillation does not.
- Shutdown state: Crystal oscillation stops.

■ SOFTWARE SUPPORT FOR POPULAR NETWORK OPERATING SYSTEMS

1. LAN Node Drivers

The so-called driver is the hardware-dependent portion of the software complement for a network node. It's purpose is to marry a specific hardware configuration to a more-or-less generic interface provided by the networking software. Network software suppliers provide such generic interfaces for drivers to encourage universal support from a variety of hardware products. By partitioning or layering the software into a stack of components with standardized interfaces between the layers, the job of integrating various hardware and software offerings with a particular network operating system becomes easier. More drivers will become available, and everyone benefits.

As seen in Figure 9, which depicts a model of LAN node components, the driver sits between the generic network software and the hardware, and acts as a bridge between the system and the node hardware. The interface of the driver to the network software and its applications is a generic interface and virtually the same for all drivers running on a given operating system. But the driver comprehends the configuration and nuances of the hardware, and optimizes it's performance in the system. A good, well-written driver is a positive advantage to the system, allowing it to achieve its performance potential; whereas a poor driver will limit the performance and reliability of the system.

The best drivers have a certain intimacy with the hardware, which allows them to take full advantage of its features. High data throughput, data integrity, and reliable operation are the key goals for which every node-driver writer should strive. In addition, the final driver should be efficient, by requiring minimum host execution time. These are all things the end user will and should take for granted; if they are not supplied with the design, there will be no customer satisfaction.

Most network software suppliers offer technical support for third-party driver development. This often comes in the form of a developer's kit that includes a manual and software examples. Some suppliers also offer test suites and certification testing to verify the driver product, because they know that good drivers benefit both users and suppliers.

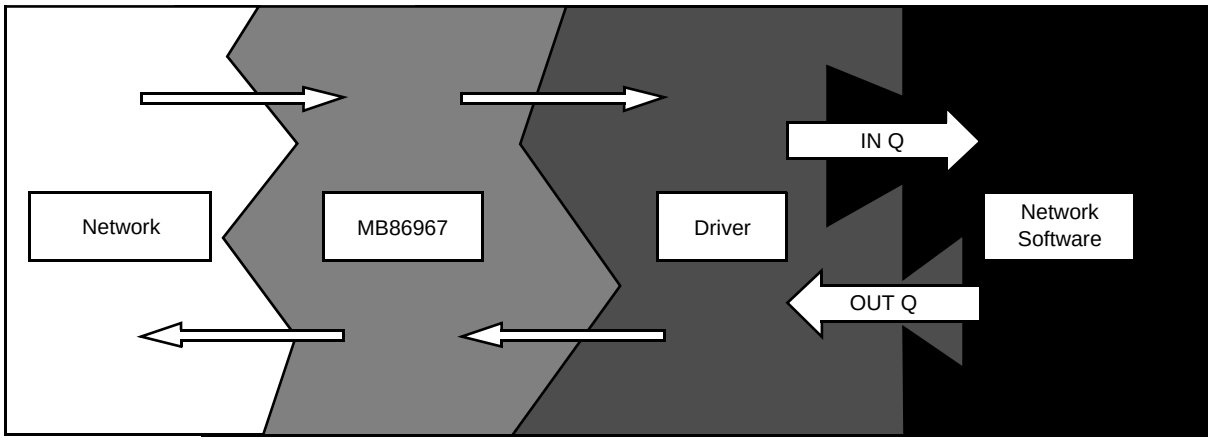


Figure 9 Model of LAN Node

2. What's in a Driver?

Typical node drivers manage the movement of packet data between system memory and the network, and vice versa, as well as providing diagnostic testing, error processing, and error statistics on-demand for the system.

The first thing a driver does when the system is powered up is system check-out, which may include buffer memory testing, and loopback testing of the transmit and receive circuits. If the network supports it, as does Ethernet, for example, the testing may include sending and receiving test packets on the network to verify the ability to communicate.

As shown in Figure 10, the driver provides control of the initialization, interrupt and branch control processes, supporting both the transmit and the receive functions.

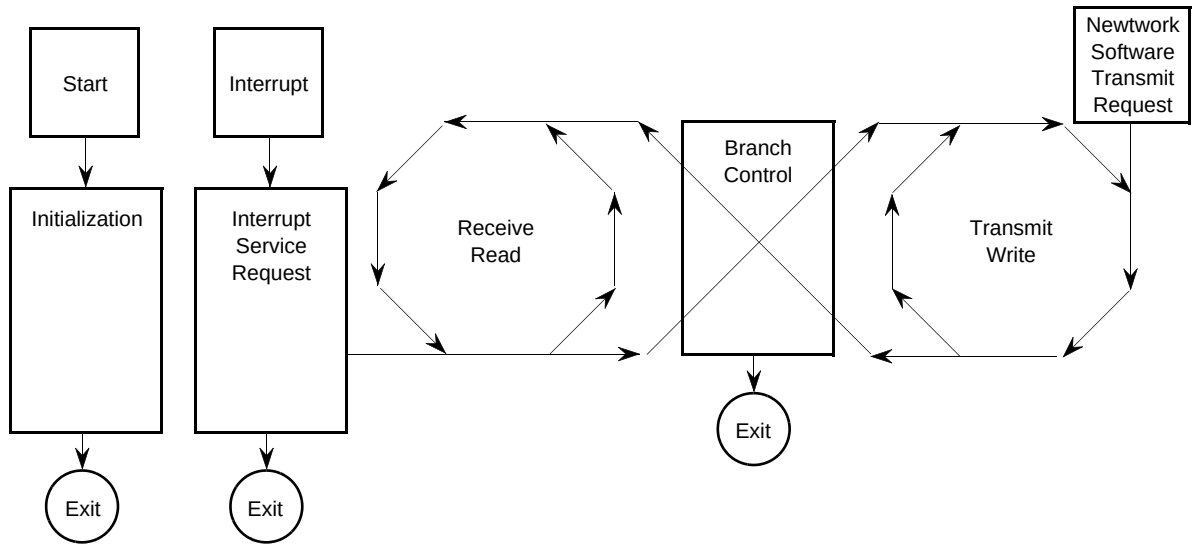


Figure 10 Software Driver Model

Figure 11 shows an example in flow chart form of a check-out routine written for the Fujitsu MB86967 Controller. The driver first initializes the control and status registers in the controller for memory and loopback testing. Loopback and memory testing are conducted simultaneously by transmitting memory test patterns from the transmit buffer area of memory to the receive buffer area using loopback. This test sequence simultaneously exercises and tests the transmitter, the receiver and the buffer memory.

The loopback/memory startup test is performed by first loading a test pattern in the form of several packets into the controller chip's transmit buffer, then transmitting the packets in loopback mode. The loopback transmission path through the chip exercises the data link controller as well as the encoder and decoder circuitry, but does not affect the network.

The MB86967 controller has a unique buffer memory architecture which pipelines packets through the system in both directions, optimizing data through-put. MB86967's buffer controller provides all the pointer management for accessing the buffer automatically, greatly reducing the complexity of the driver and minimizing the software overhead. Receive packets with errors are automatically purged by MB86967. When a collision occurs, MB86967 automatically re-transmits without host interaction. These features provide high data throughput while minimizing the host and memory overhead. At the successful conclusion of the tests, the driver starts up the MB86967 chip for regular service on the network.

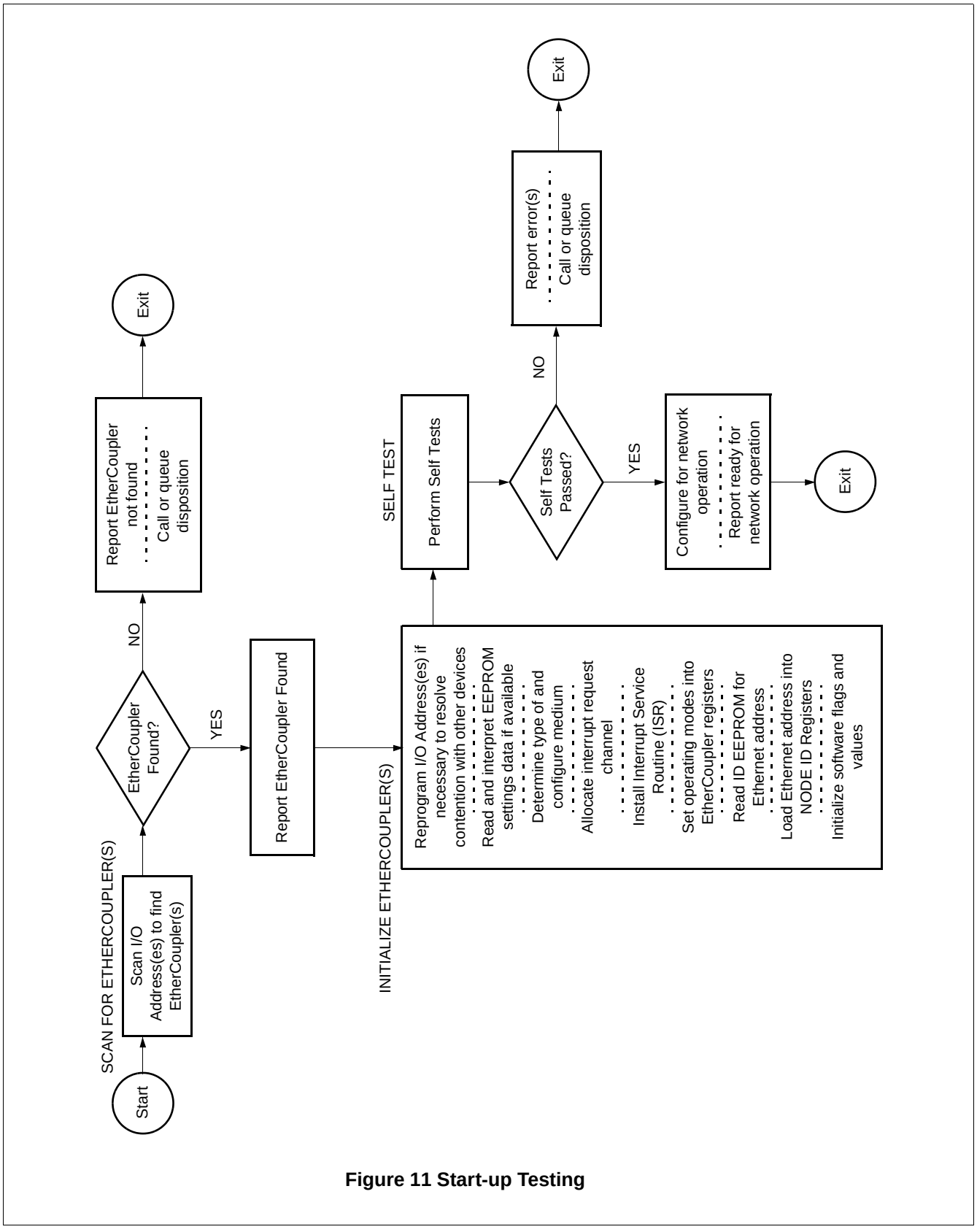


Figure 11 Start-up Testing

3. Operating on the Network

Driver code for operating on the network might be partitioned into three main modules as shown in the example for the MB86967 controller in this section. The modules, shown in Figures 12, 13, and 14 are Transmit Packet Write, in which packets to be transmitted are moved from host memory to the point marked TX PKT WRITE.

Transmission takes place in two steps. First, packets to be transmitted are loaded into the transmit buffer. Secondly, when the transmitter is not busy, it will be started to transmit the stored packets. Each of these steps may have to wait for resources. The packets cannot be loaded unless there is buffer space available. MB86967 provides the option of a single or two independent transmit buffers. With two buffers there is usually no waiting. The transmitter cannot transmit but one buffer full of packets at a time. To manage these resources, two software flags are used, TBUF STAT and TX STAT, the status of the transmit buffer and the transmitter respectively. TBUF STAT refers to the current buffer which might be available to the driver for loading. Its status can be Busy if no buffer is available, Loading when in the process of being loaded, in Standby if ready to transmit, but not full, ready and Full or Empty. The transmitter status can be either Busy or Idle.

Packet length is checked during the loading process to assure that the ISO/ANSI/IEEE 8802-3 length requirements are met. Packets ready to be loaded can be loaded into an Empty or Standby buffer, the latter being a buffer with packets waiting for the transmitter to become idle. If a standby buffer has more room for packets, additional packets can be loaded until it is full. The Empty buffer is available for loading and has no packets. The driver takes ownership of an Empty or Standby buffer by changing its status to Loading.

After the packets are loaded, the transmit status flag is checked for an idle transmitter. If idle, it can be immediately started to transmit the contents of either a Full or Standby buffer. When the transmitter of the MB86967 chip is started, buffer status also changes. In single buffer mode, starting the transmitter makes the single buffer unavailable to the system. In dual buffer mode, starting the transmitter re-allocates its previously-transmitted buffer as an empty buffer, available for loading. If the transmitter is busy, the routine will suspend execution at that point pending an idle transmitter.

Two key interrupts used in this example are the receive packet interrupt (RX PKT), indicating that one or more packets has been received since the interrupt was last enabled, and the transmitter done interrupt (TX DONE), indicating that the transmitter has finished transmitting the contents of its current buffer. The interrupt service routine for network operation, illustrated in Figure 13, is short and sweet. If the receive packet interrupt has occurred, it calls or queues the routine for reading packets (RX PKT READ). Further receive interrupts are masked until the driver has emptied the receive buffer. This prevents redundant interrupts which would otherwise occur if packets come in during the read sequence. If the transmitter done interrupt has occurred, the status flags are updated, and appropriate action is taken to satisfy pending activity, if any, with the newly available buffer and/or transmitter resource.

The driver is structured to read all receive packets in the buffer whenever one or more packets arrive. A status bit in MB86967 (BUF EMPTY) indicates whether the receive buffer is empty or not (indicating whole packets only). The packet read routine, shown in Figure 14, starts by masking further receive interrupts until it has emptied the buffer and suspended execution. This prevents redundant interrupts which would otherwise occur if packets come in during the read sequence. As each packet is read, it can be read in parts. If after reading the first part the packet is not of interest, the rest can be discarded without being moved to host memory using MB86967's Skip Packet feature. Reading will continue until the buffer is empty, as indicated by RBUF EMPTY bit.

The Transmit Packet Write Routine, shown in Figure 12, and the Receive Packet Read Routine, shown in Figure 14, together comprise the driver core, which can be called by the network software or from the Network Interrupt Service Routine, shown in Figure 13. Once called, this core routine transfers both transmit and receive packets until there are no more to be transferred, then exits or returns. If packets are transferring, this core routine avoids locking out either the transmitter or the receiver while the other is very busy, by alternating between the two after a fixed number of packets, set by TX MAX and RX MAX. While in operation, the core routine polls key status bits. Interrupts are disabled to prevent unnecessary interrupts while the core is executing.

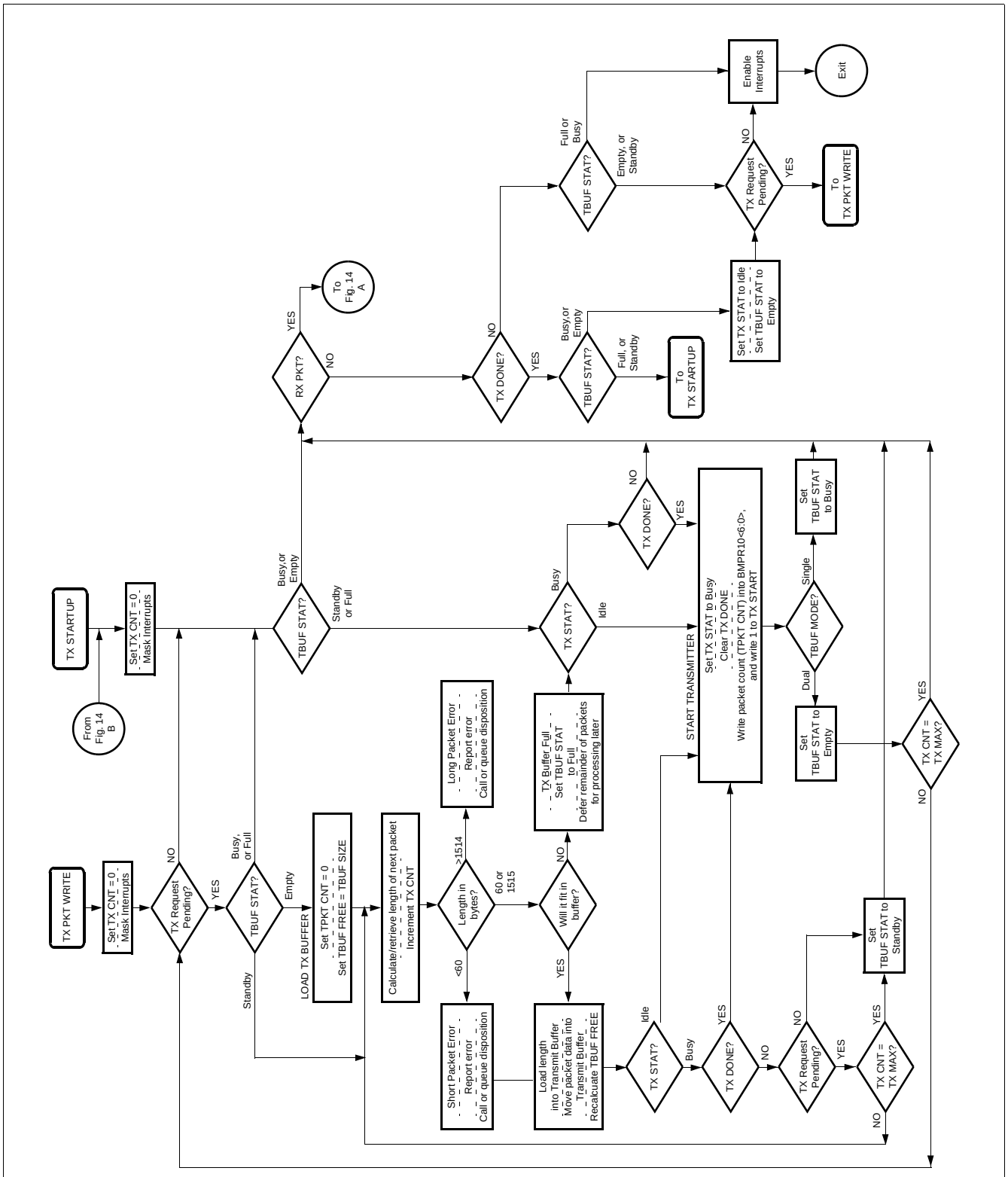


Figure 12 Transmit Packet Write Routine

A driver such as the one illustrated in this section might typically occupy 4 to 6 kilobytes on its distribution diskette. The host-resident portion, when loaded for network operation, might use typically 2 to 3 kilobytes of host memory. A set of quality software drivers bundled with the hardware is well worth providing to LAN equipment customers. By providing better performance and reliability, good drivers will enhance both customer satisfaction and sales, while reducing customer service calls.

Table 6 represents typical control and status parameter used in MB86967 Network Drivers.

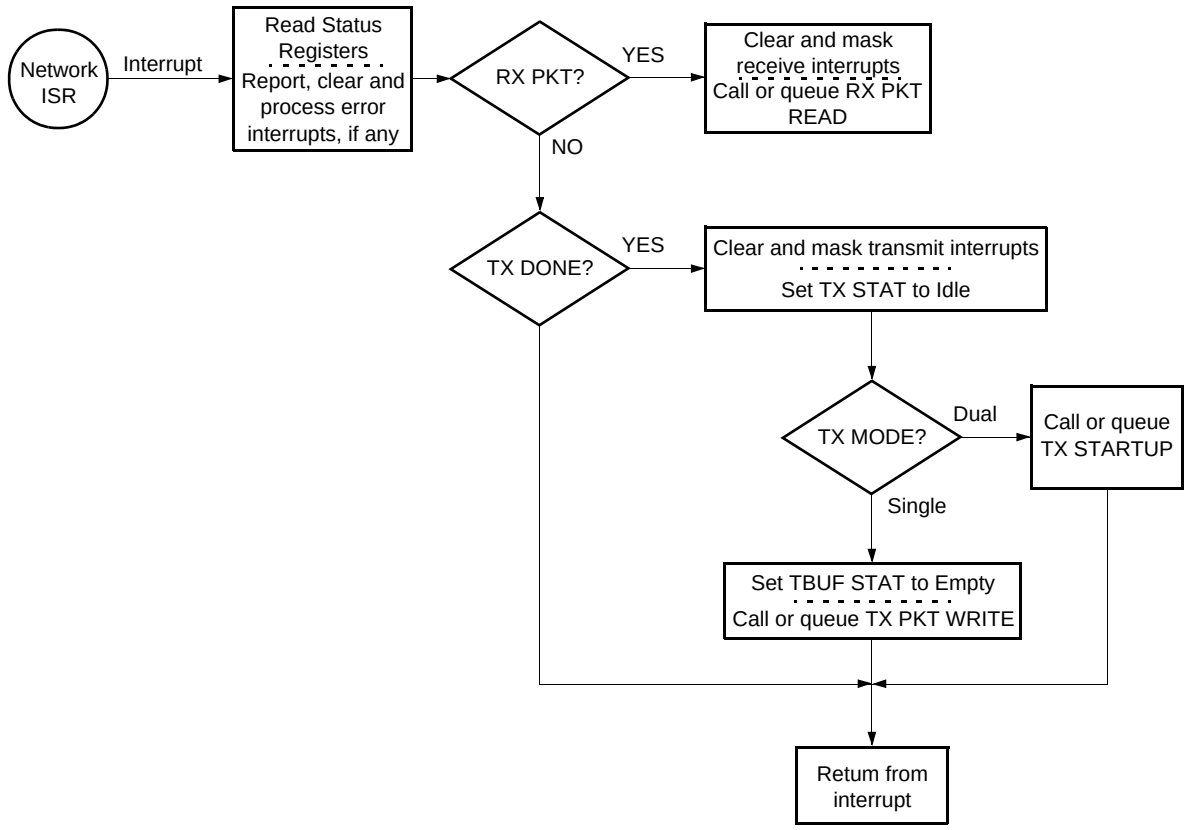


Figure 13 Network Interrupt Service Routine

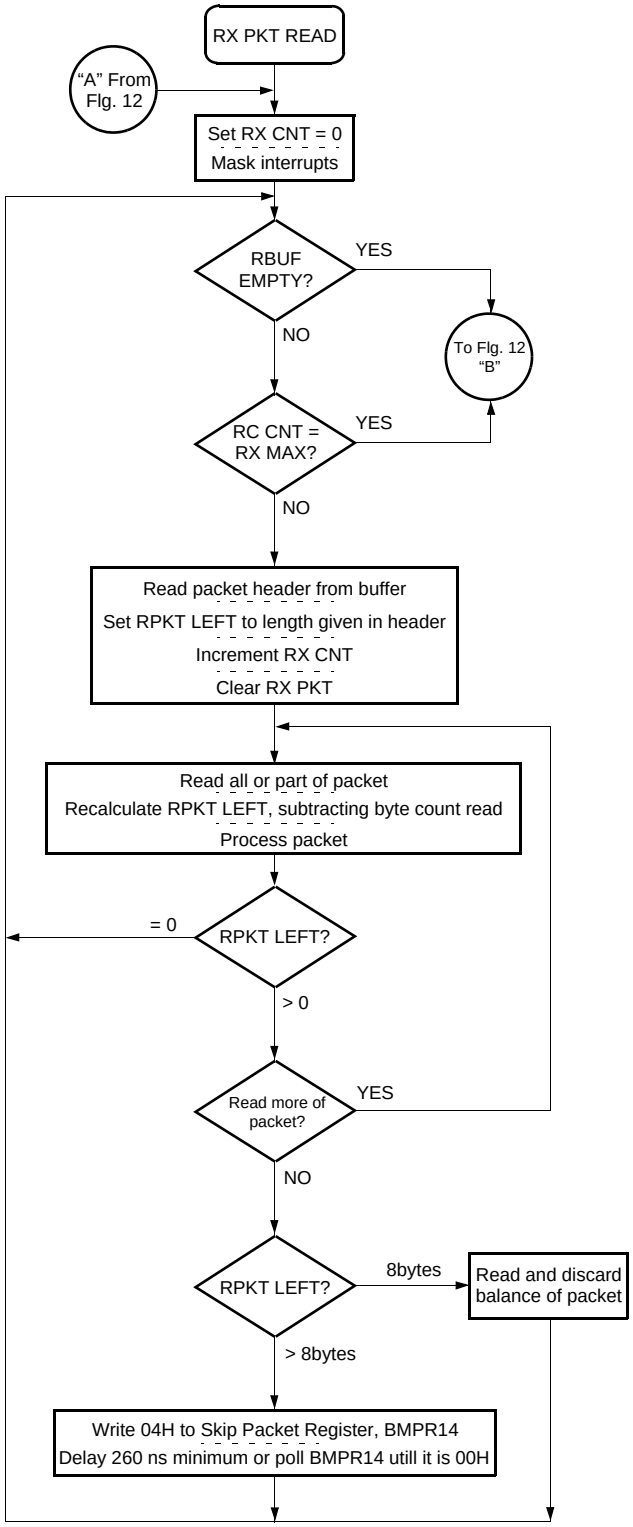


Figure 14 Receive Packet Read Routine

Table 6 Control and Status Parameters

Symbol	Type	Name	Description
DLC EN	Register Bit	DATA LINK CONTROL ENABLE	When high, resets all buffer memory pointers and disables both the transmitter and the receiver circuits. When low, enables buffer memory, transmitter and receiver.
LBC	Register Bit	LOOPBACK CONTROL	When set low, places MB86967 in internal loopback mode.
RBUF EMPTY	Register Bit	RECEIVE BUFFER EMPTY	When high, indicates that there is at least one complete packet stored in the receive buffer, ready to read. When low, indicates there are no packets ready to read in the receive buffer.
RPKT LEFT	Software Value	RECEIVE PACKET LENGTH LEFT	The number of bytes remaining in the receive packet being read from the buffer. Calculated by the driver from the original length given by MB86967 in the 3rd and 4th bytes of the receive packet header, less the number of bytes already read out.
RX CNT	Software Value	RECEIVE TRANSFER COUNT	A running count of the number of packets transferred from the receive buffer to system memory since entering the Receive Packet Read Routine. This parameter can share the same memory location with TX CNT, because both are not used concurrently in the same subroutine.
RX MAX	Software Value	MAXIMUM VALUE FOR RX CNT	The maximum number of packets that may be processed in the Receive Packet Read Routine.before passing control to the Transmit Packet Write Routine. This parameter can be fixed or allowed to vary according to need. Typical range for this parameter is 15 - 32.
TBUF FREE	Software Value	TRANSMIT BUFFER FREE SPACE	The number of available bytes remaining in the transmit buffer being loaded with packets by the driver. Calculated by driver.
TBUF MODE	Register Bits	TRANSMIT BUFFER MODE	The configuration of the transmit buffer space, SINGLE buffer or DUAL buffers.
TBUF SIZE	Software Value	TRANSMIT BUFFER SIZE	The size in bytes of each transmit buffer, which depends on initial configuration parameters for the buffer memory.
TBUF STAT	Software Value	TRANSMIT BUFFER STATUS	Current status of the transmit buffer available for loading packets. Maintained by the driver.

TBUF STAT	Value Description
Empty	Current transmit buffer available to system bus is completely empty.
Busy	No buffer is currently available to the system bus because a) MB86967 is in single-buffer mode and b) the transmitter is using the buffer.
Standby	The buffer currently available to the system bus has one or more packets in it, but may still have room for additional packet(s).
Full	The buffer currently available to the system bus has one or more packets in it, and does not have room for the next packet presented to the driver from the transmit queue.

Symbol	Type	Name	Description
TPKT CNT	Software Value	TRANSMIT PACKET COUNT	The number of packets loaded into the current transmit buffer by the driver. Value is counted by driver. This value is written into MB86967 register BMPR10<6:0> at the time transmitter is started.
TX CNT	Software Value	TRANSMIT TRANSFER COUNT	A running count of the number of packets transferred from system memory to the transmit buffer since entering the Transmit Packet Write Routine. This parameter can share the same memory location with RX CNT, because both are not used concurrently in the same subroutine.
TX DONE	Register Bit	TRANSMITTER DONE	When transmitter finishes transmitting, MB86967 sets this bit high. Normally cleared by driver prior to starting transmitter. Hardware reset or DLC EN being set high also clears this bit.
TX MAX	Software Value	MAXIMUM VALUE FOR TX CNT	The maximum number of packets that may be processed in the Transmit Packet Write Routine before passing control to Receive Packet Read Routine. This parameter can be fixed or allowed to vary according to need. Typical range for this parameter is 15-32.
TX START	Register Bit	START TRANSMITTER	When set high, activates transmitter to transmit all packets in the current transmit buffer. See also TPKT CNT.
TX STAT	Software Value	TRANSMIT BUFFER STATUS	Current status of the transmitter, maintained by driver.

TX STAT	Value Description
Busy	Transmitter has not finished transmitting packets previously given to it to transmit.
Idle	Transmitter has finished transmitting all packets in its buffer.

■ ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_{DD}	V_{SS} – 0.5	+6.0	V
Input voltage	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature	Tstg	–55	+125	°C
Operating temperature	Top	–40	+85	°C
Output current	I_O	–40	+40	mA

* : Duration of voltage applied is within 1 sec per terminal.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Ta	0	—	+70	°C
TTL “H” level output current	I_{OH}	—	–2.0	—	mA
		—	–4.0*1	—	mA
		—	–8.0*3	—	mA
TTL “L” level output current	I_{OL}	—	3.2	—	mA
		—	12.0*2	—	mA
		—	24.0*3	—	mA
Crystal oscillator frequency	f_{Xtal}	20.000 ± 0.005%			MHz

*1: Applies to P92 ($\overline{IREQ}$, IREQ0, $\overline{INT}$)
*2: Applies to LED terminal (open-drain output) and P92 ($\overline{IREQ}$, IREQ0, $\overline{INT}$)
*3: Applies to P3 ($\overline{WAIT}$, IOCHRDY, READY) and P84 ($\overline{IOIS16}$)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply current	I_{DD}	Operation state*1	—	70	100	mA
	I_{DDP}	Power down*2	—	10	15	mA
	I_{DDS}	Shut down*3	—	0.1	0.5	mA
TTL “H” level output voltage	V_{OH}	I_{OH} = –2 mA, –4 mA, –8 mA	4.0	—	V_{DD}	V
TTL “L” level output voltage	V_{OL}	I_{OL} = 3.2 mA, 12 mA	V_{SS}	—	0.4	V
		I_{OL} = 24 mA	V_{SS}	—	0.5	V
TTL “H” level input voltage	V_{IH}	TTL standard cell	2.2	—	V_{DD}	V
		TTL schmitt trigger cell	2.4	—	V_{DD}	V
TTL “L” level input voltage	V_{IL}	TTL standard cell	V_{SS}	—	0.8	V
		TTL schmitt trigger cell	V_{SS}	—	0.6	V
TTL input leak current	I_{LI}	V_I = 0 to V_{DD}	–10	—	10	µA
TTL HI-Z leak current*4	I_{LZ}		–10	—	10	µA
Input pull-up/pull-down resistor	R_{PUPD}	V_I = 0 V to V_{DD}	100	—	—	kΩ

*1: For TP in operation.
*2: With the use of register settings, enable power saving mode, including RESET=Low, TP input/input with pull-up resistor = OPEN, other input terminal = Low or High, All output terminals = OPEN
*3: With the use of register settings, enable shut-down mode, including RESET=Low, TP input/input with pull-up resistor = OPEN, other input terminal = Low or High, All output terminals = OPEN
*4: Leak current when the TTL I/O terminal is in a high-impedance state.

2. TP Interface DC Characteristics

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

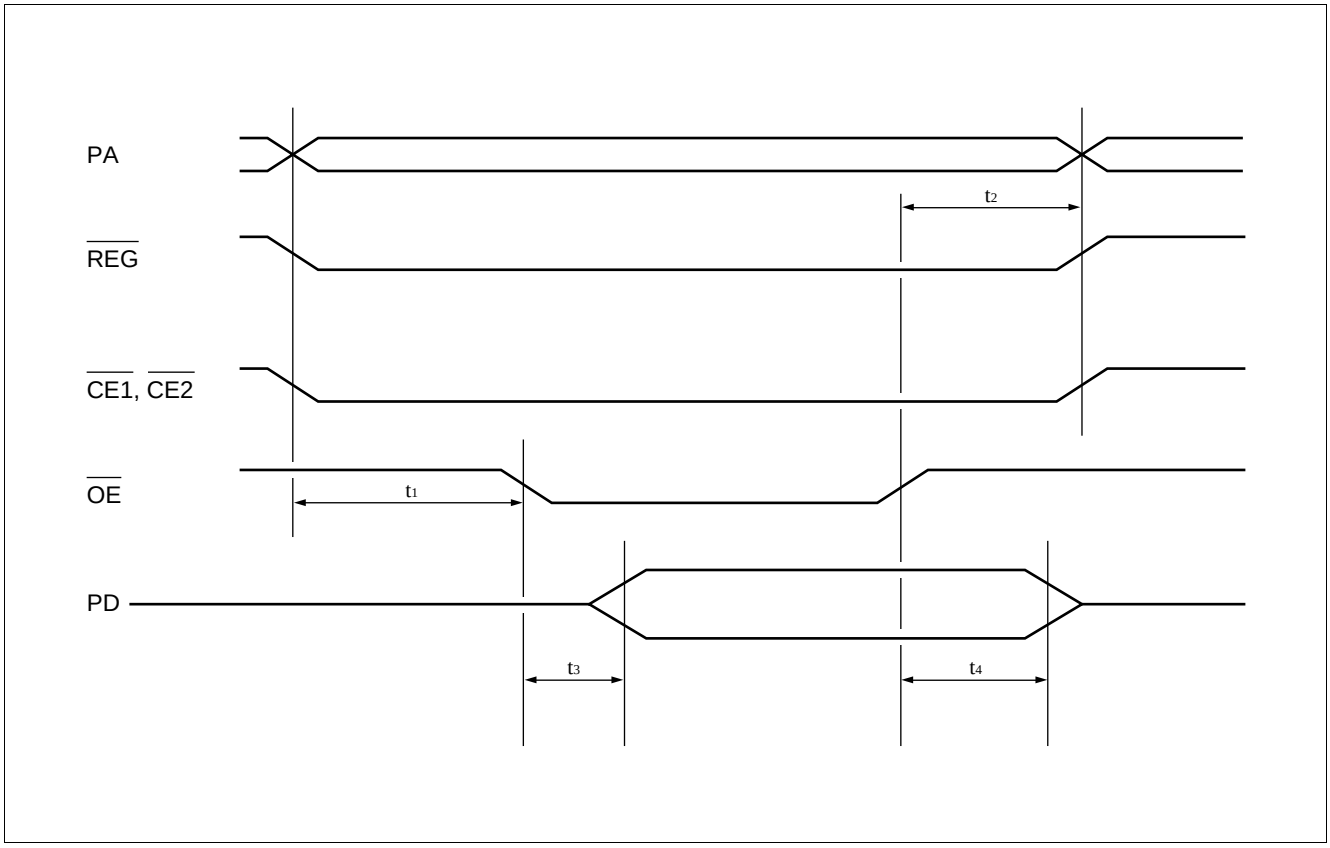
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
TPO "H" level output voltage	V_{TOH}	I_{TOH} = 24 mA	V_{DD} – 0.5	—	V_{DD}	V
TPO "L" level output voltage	V_{TOL}	I_{TOL} = 24 mA	V_{SS}	—	0.4	V
TPO "H" level output current	I_{TOH}	—	—	24.0	—	mA
TPO "L" level output current	I_{TOL}	—	—	24.0	—	mA
TPO output impedance	Z_{TO}	—	—	10.0	—	Ω
TPI input impedance	Z_{TI}	—	—	10.0	—	kΩ
TPI input bias voltage	V_{TI}BIAS	—	—	3.3	—	V
TPI differential input voltage	V_{TI}D	—	±0.58	—	±3.1	V
TPI differential input squelch threshold voltage	V_{TI}DSH	—	—	–420	—	mV
TPI differential input non-squelch threshold voltage	V_{TI}DNSH	—	–80	0	+80	mV

3. AC Characteristics

(1) Bus Timing (PC card mode, CCR read cycle)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

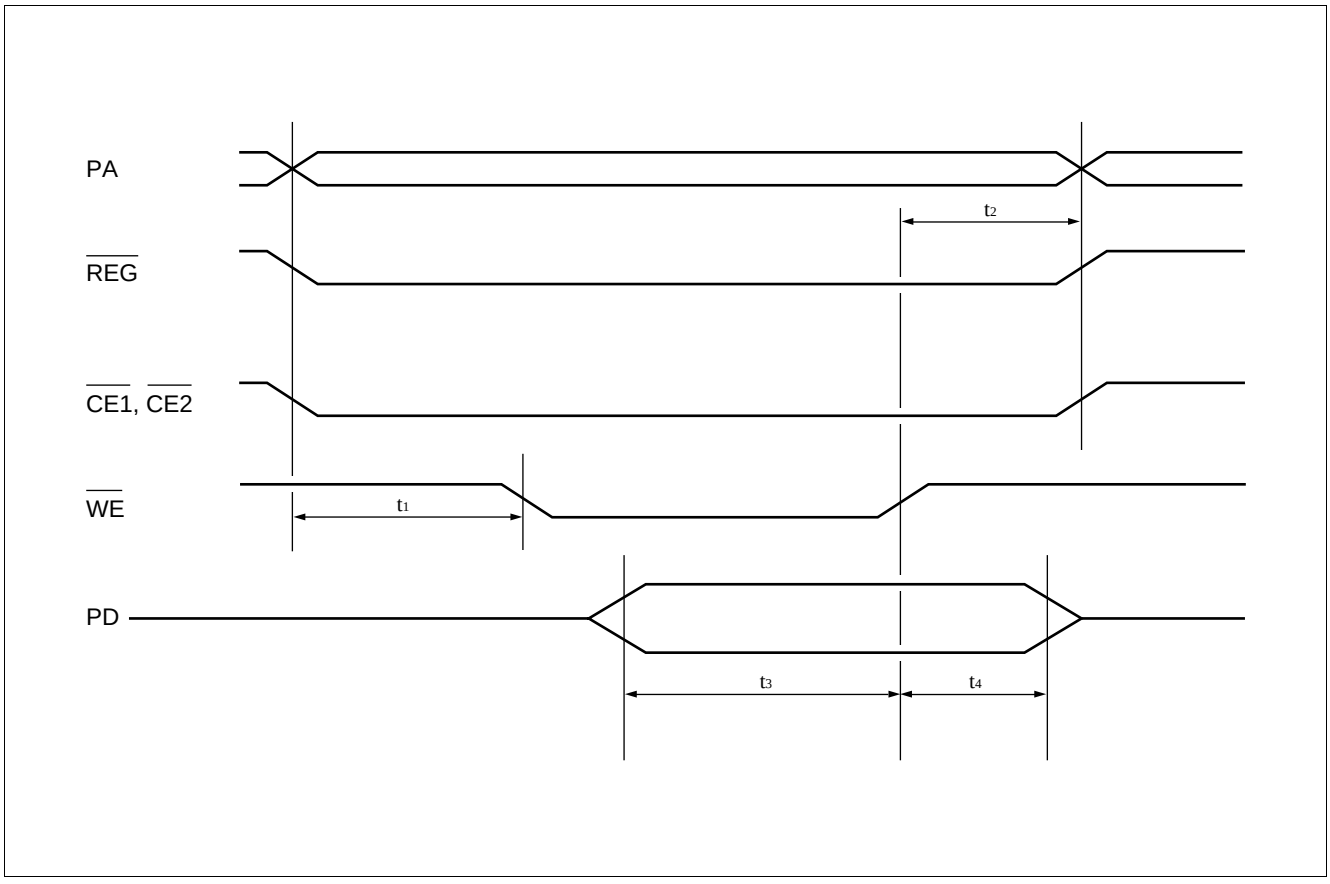
Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{OE}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ after $\overline{OE}$ negate	t_2	5	—	ns
Output delay time for read data	t_3	—	40	ns
Output hold time for read data	t_4	5	—	ns



(2) Bus Timing (PC card mode, CCR write cycle)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

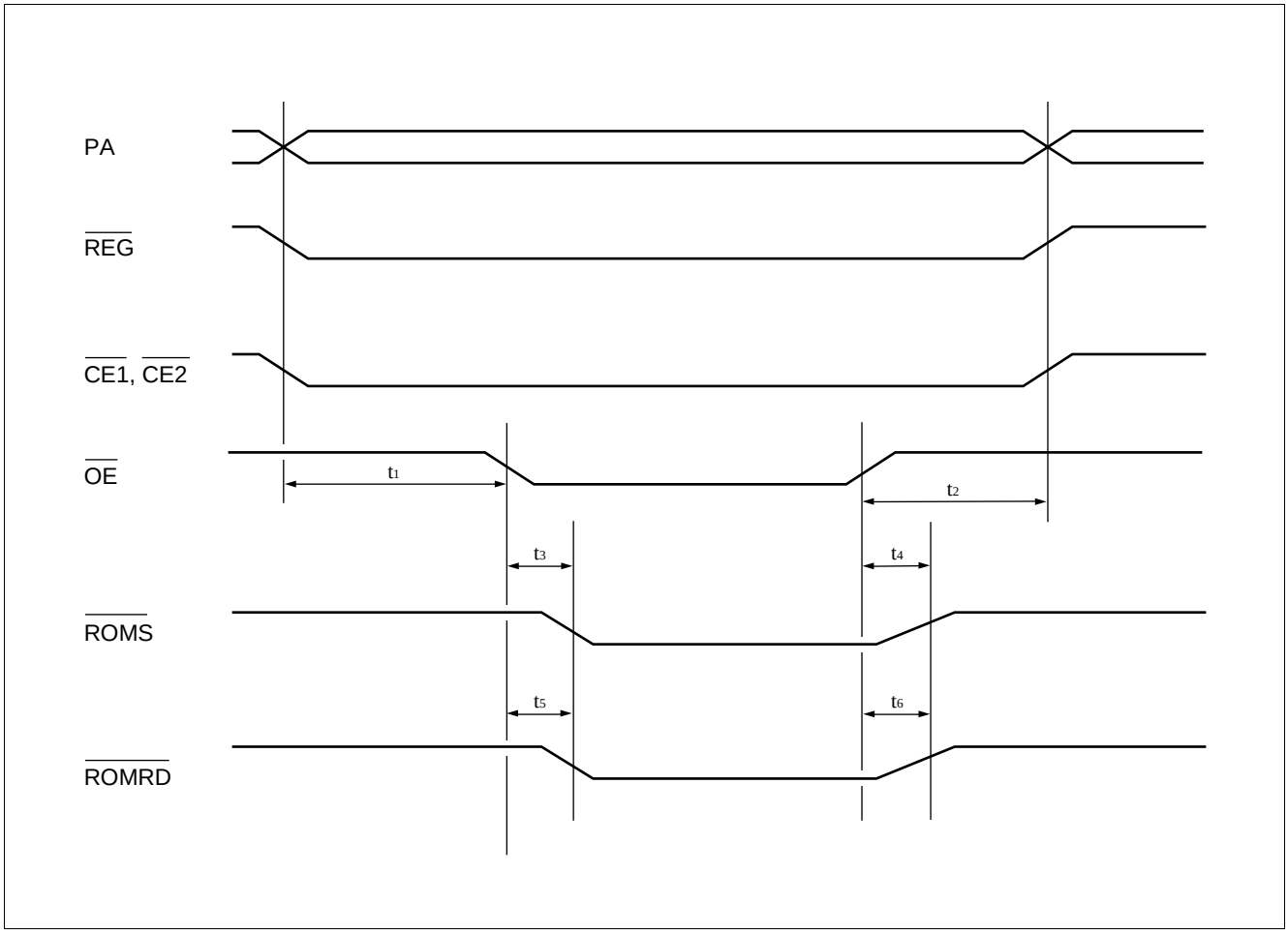
Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{WE}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ after $\overline{WE}$ negate	t_2	5	—	ns
Setup time for write data input	t_3	10	—	ns
Hold time for write data input	t_4	5	—	ns



(3) Bus Timing (PC card mode, CIS read)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

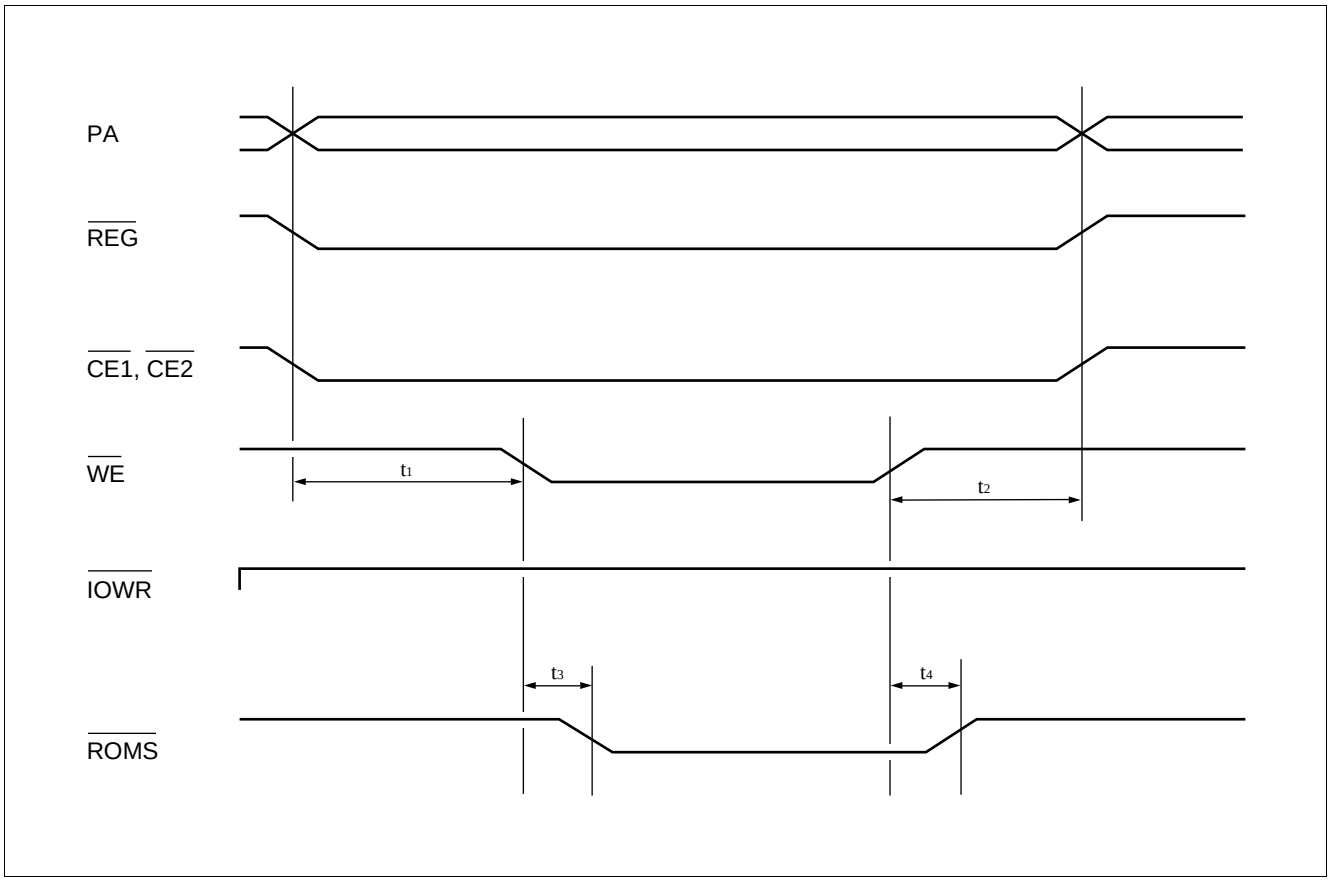
Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{OE}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ after $\overline{OE}$ negate	t_2	5	—	ns
$\overline{ROMS}$ assert output delay after $\overline{OE}$ assert	t_3	—	30	ns
$\overline{ROMS}$ negate output delay after $\overline{OE}$ negate	t_4	—	30	ns
$\overline{ROMRD}$ assert output delay after $\overline{OE}$ assert	t_5	—	30	ns
$\overline{ROMRD}$ negate output delay after $\overline{OE}$ negate	t_6	—	30	ns



(4) Bus Timing (PC card mode, CIS write)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

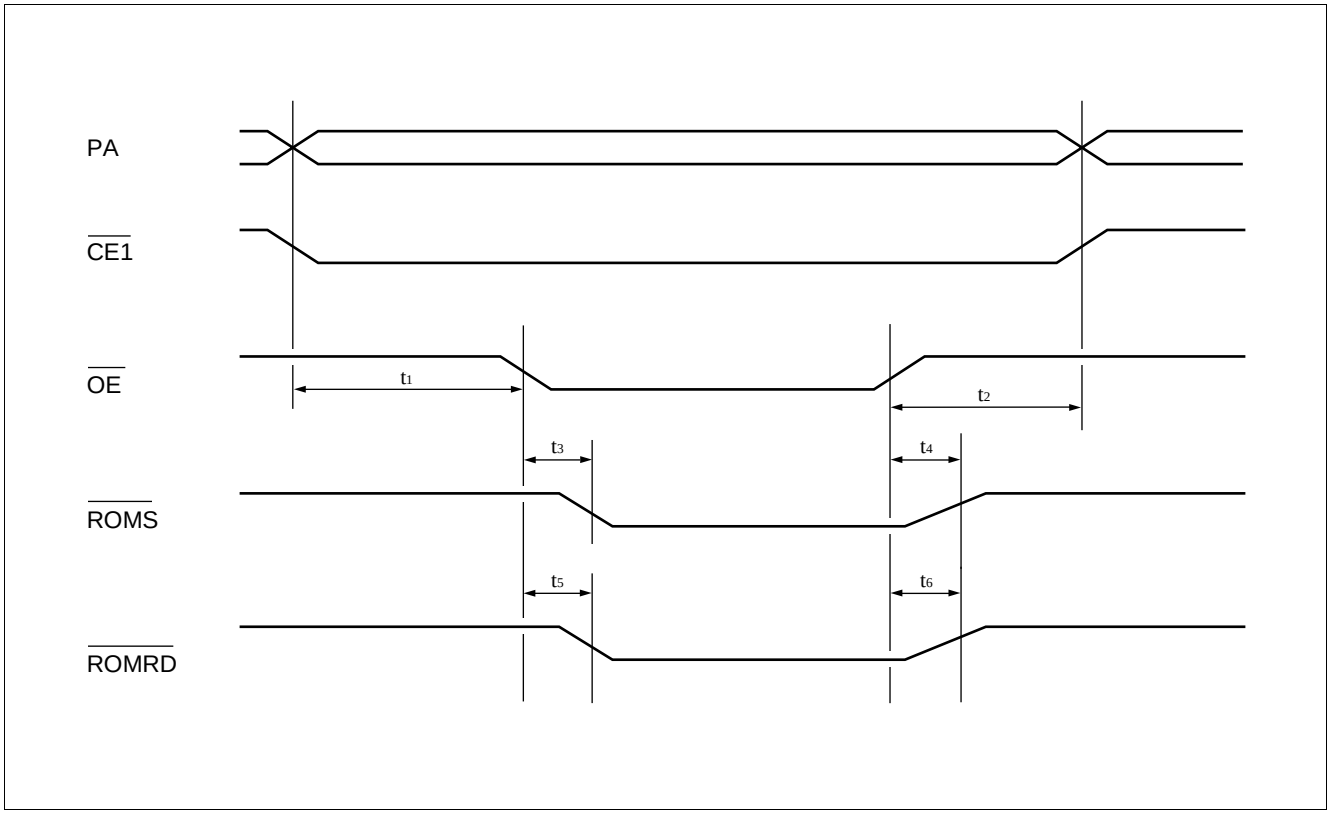
Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{WE}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ after $\overline{WE}$ negate	t_2	5	—	ns
$\overline{ROMS}$ assert output delay after $\overline{WE}$ assert	t_3	—	30	ns
$\overline{ROMS}$ negate output delay after $\overline{WE}$ negate	t_4	—	30	ns



(5) Bus Timing (PC card mode, common memory read)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

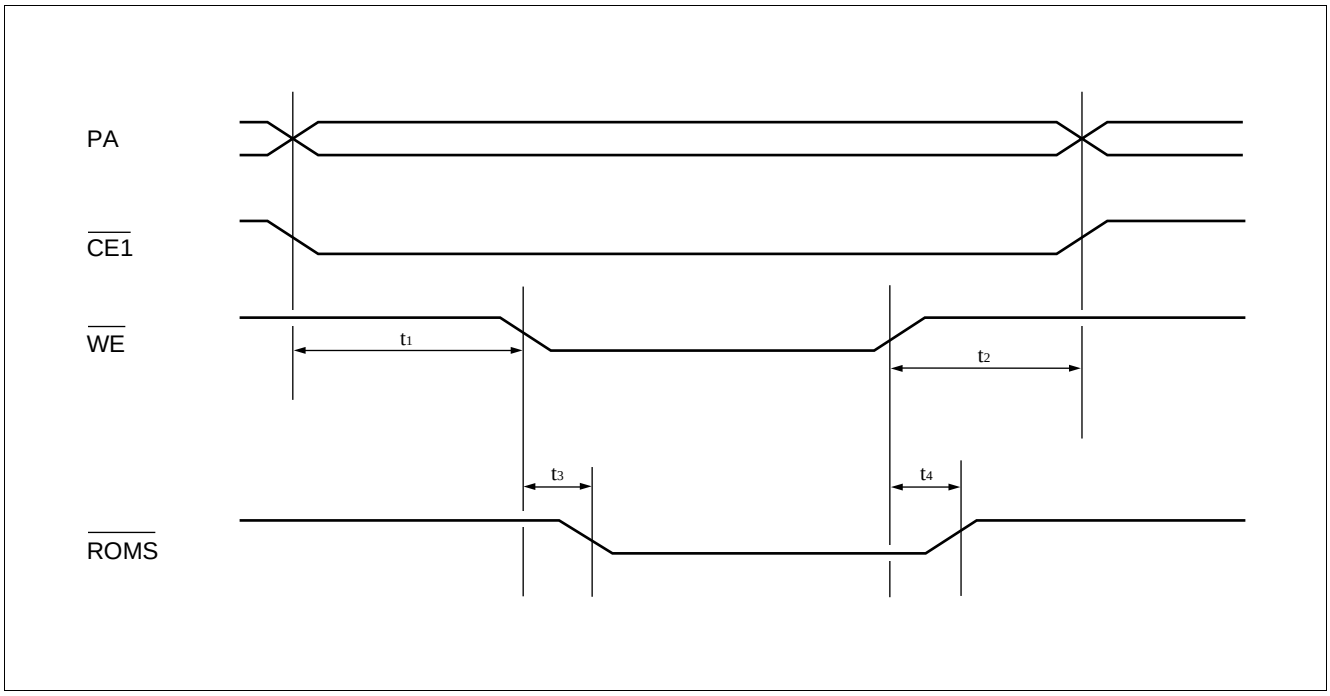
Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$ prior to $\overline{OE}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$ after $\overline{OE}$ negate	t_2	5	—	ns
$\overline{ROMS}$ assert output delay after $\overline{OE}$ assert	t_3	—	30	ns
$\overline{ROMS}$ negate output delay after $\overline{OE}$ negate	t_4	—	30	ns
$\overline{ROMRD}$ assert output delay after $\overline{OE}$ assert	t_5	—	30	ns
$\overline{ROMRD}$ negate output delay after $\overline{OE}$ negate	t_6	—	30	ns



(6) Bus Timing (PC card mode, common memory write)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$ prior to $\overline{WE}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$ after $\overline{WE}$ negate	t_2	5	—	ns
$\overline{ROMS}$ assert output delay after $\overline{WE}$ assert	t_3	—	30	ns
$\overline{ROMS}$ negate output delay after $\overline{WE}$ negate	t_4	—	30	ns



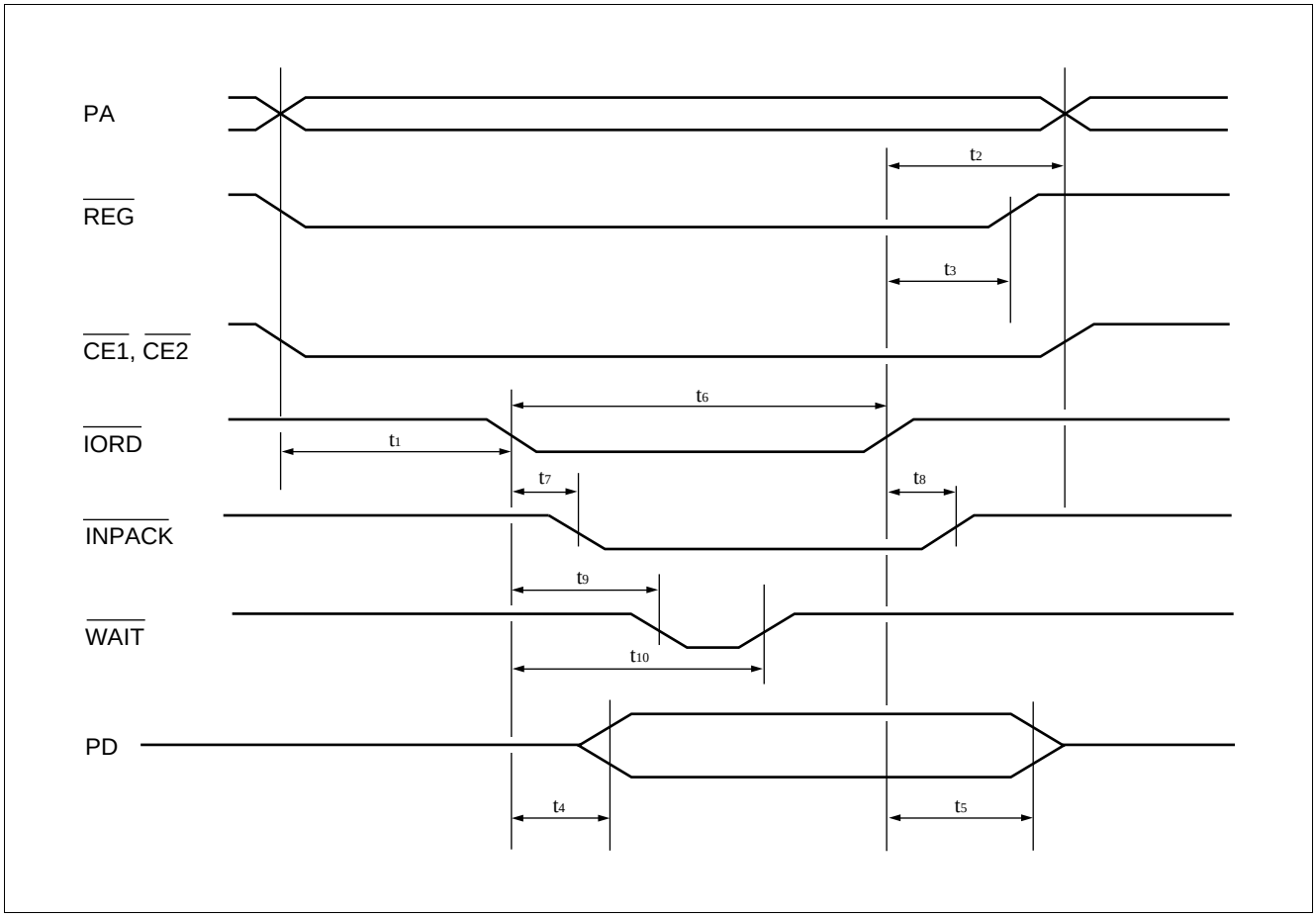
(7) Bus Timing (PC card mode, I/O read cycle)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{IORD}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$ after $\overline{IORD}$ negate	t_2	5	—	ns
Hold time for $\overline{REG}$ after $\overline{IORD}$ negate	t_3	0	—	ns
Output delay for read data after $\overline{IORD}$ assert	t_4	—	44	ns
Output hold for read data after $\overline{IORD}$ negate	t_5	10	—	ns
Read pulse width	t_6	30	—	ns
Output delay for $\overline{INPACK}$ assert after $\overline{IORD}$ assert	t_7	—	45	ns
Output delay for $\overline{INPACK}$ negate after $\overline{IORD}$ negate	t_8	—	45	ns
Output delay time of $\overline{WAIT}$ assert from $\overline{IORD}$ assert	t_9	5*1	35*1	ns
Output delay time of $\overline{WAIT}$ negate from $\overline{IORD}$ assert	t_{10}	—	175*2	ns

*1: $\overline{WAIT}$ is asserted only when the write access conflicts with that of the network on reading the buffer memory port (BMPR8).

*2: $\overline{WAIT}$ is asserted only when the write access conflicts with that of the network on reading the buffer memory port (BMPR8).
This value will be 2.15 µs when the bus write error occurs on reading the buffer memory port.



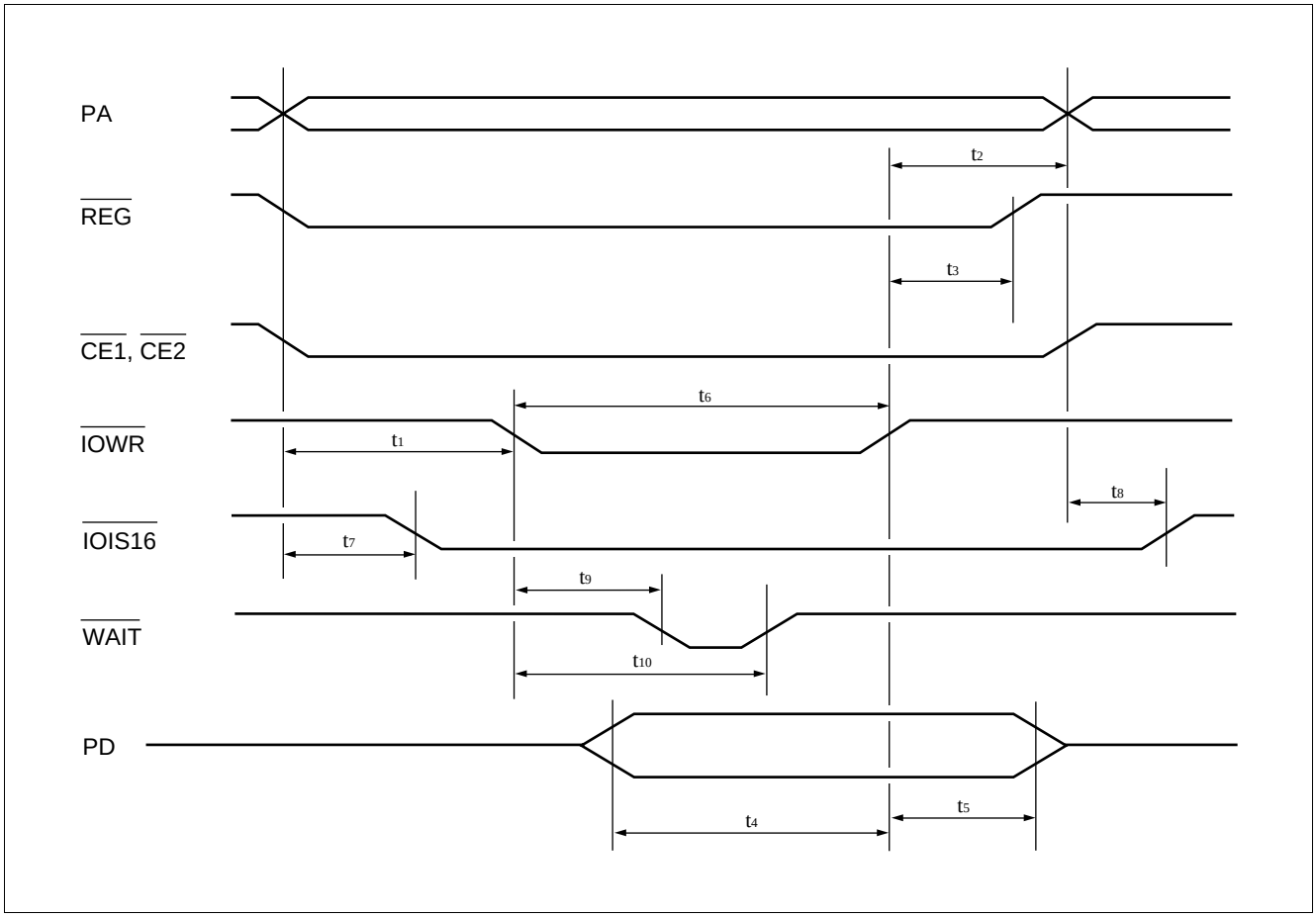
(8) Bus Timing (PC card mode, I/O write cycle)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{IOWR}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$ after $\overline{IOWR}$ negate	t_2	5	—	ns
Hold time for $\overline{REG}$ after $\overline{IOWR}$ negate	t_3	0	—	ns
Setup time for write data input	t_4	10	—	ns
Hold time for write data input	t_5	5	—	ns
Write pulse width	t_6	36	—	ns
Output delay time for $\overline{IOIS16}$ assert from address	t_7	—	35	ns
Output delay time for $\overline{IOIS16}$ negate from address	t_8	—	35	ns
Output delay time for $\overline{WAIT}$ assert from $\overline{IOWR}$ assert	t_9	5*1	35*1	ns
Output delay time for $\overline{WAIT}$ negate from $\overline{IOWR}$ assert	t_{10}	—	175*2	ns

*1: $\overline{WAIT}$ is asserted only when the write access conflicts with that of the network on writing the buffer memory port (BMPR8).

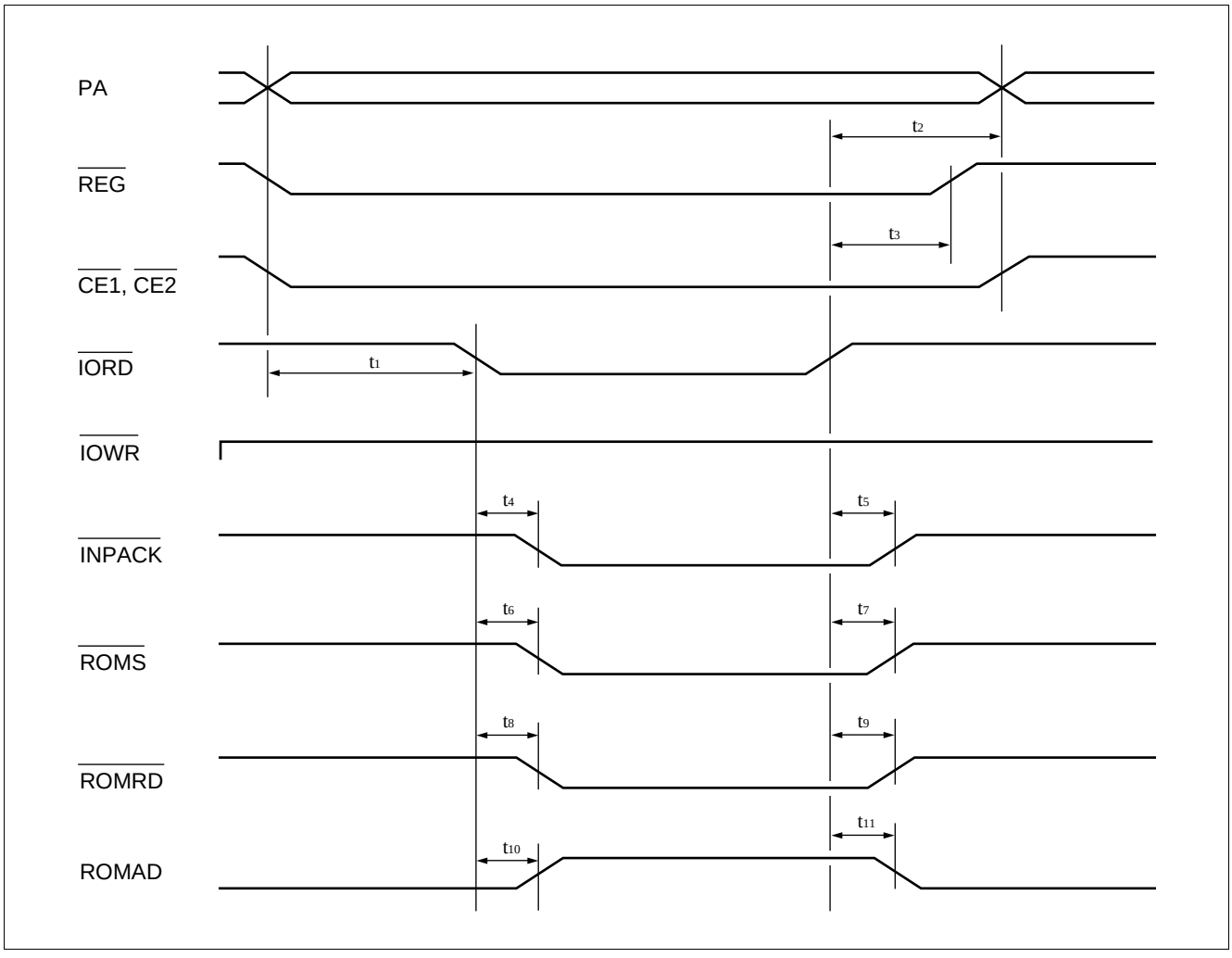
*2: $\overline{WAIT}$ is asserted only when the write access conflicts with that of the network on writing the buffer memory port (BMPR8).
This value will be 2.15 µs when the bus write error occurs on writing the buffer memory port.



(9) Bus Timing (PC card mode, ID number read from EEPROM: I/O access)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

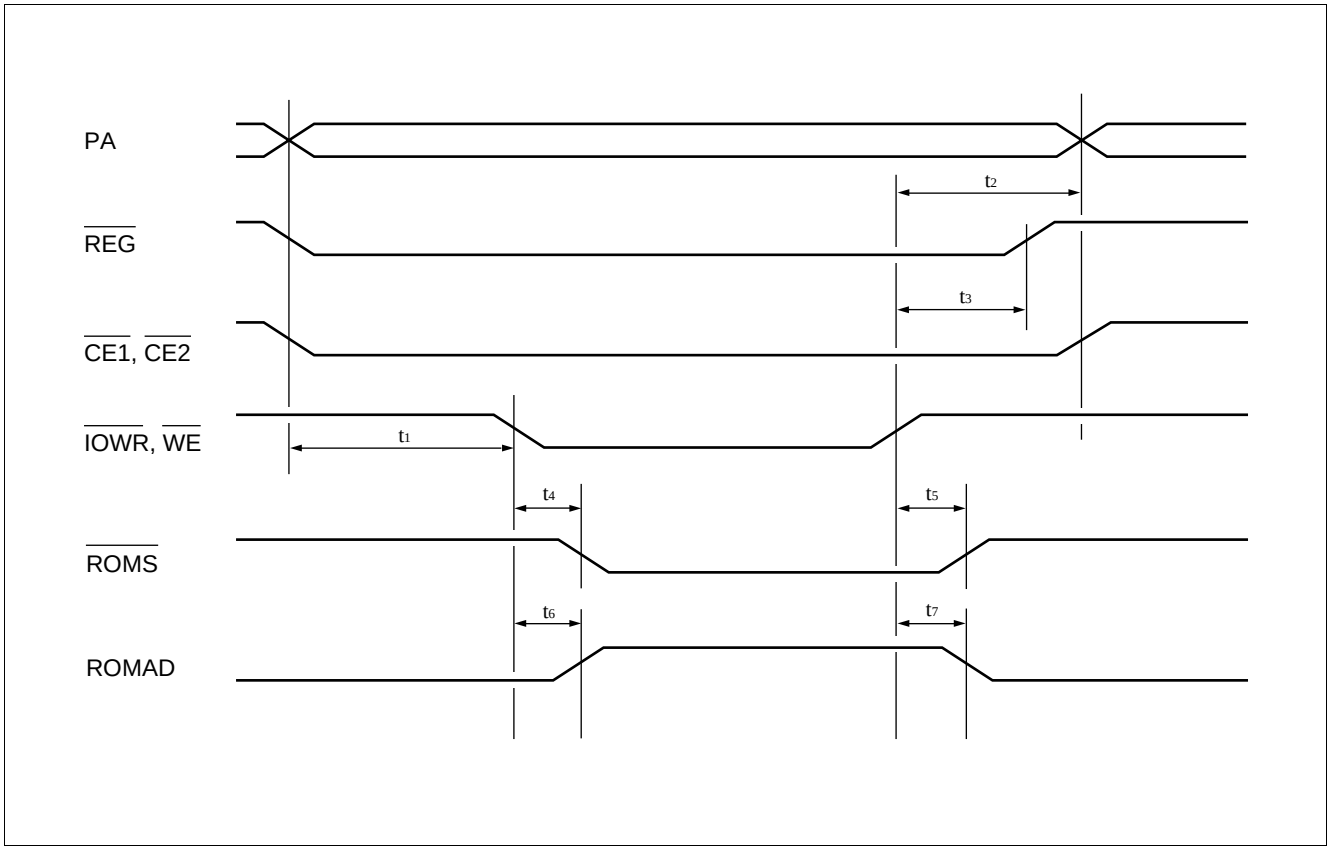
Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{IORD}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$ after $\overline{IORD}$ negate	t_2	5	—	ns
Hold time for $\overline{REG}$ after $\overline{IORD}$ negate	t_3	0	—	ns
Output delay for $\overline{INPACK}$ assert after $\overline{IORD}$ assert	t_4	—	45	ns
Output delay for $\overline{INPACK}$ negate after $\overline{IORD}$ negate	t_5	—	45	ns
Output delay for $\overline{ROMS}$ assert after $\overline{IORD}$ assert	t_6	—	35	ns
Output delay for $\overline{ROMS}$ negate after $\overline{IORD}$ negate	t_7	—	35	ns
Output delay for $\overline{ROMRD}$ assert after $\overline{IORD}$ assert	t_8	—	30	ns
Output delay for $\overline{ROMRD}$ negate after $\overline{IORD}$ negate	t_9	—	30	ns
Output delay for ROMAD assert after $\overline{IORD}$ assert	t_{10}	—	30	ns
Output delay for ROMAD negate after $\overline{IORD}$ negate	t_{11}	—	30	ns



(10)Bus Timing (PC card mode, ID number write from EEPROM: I/O access)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

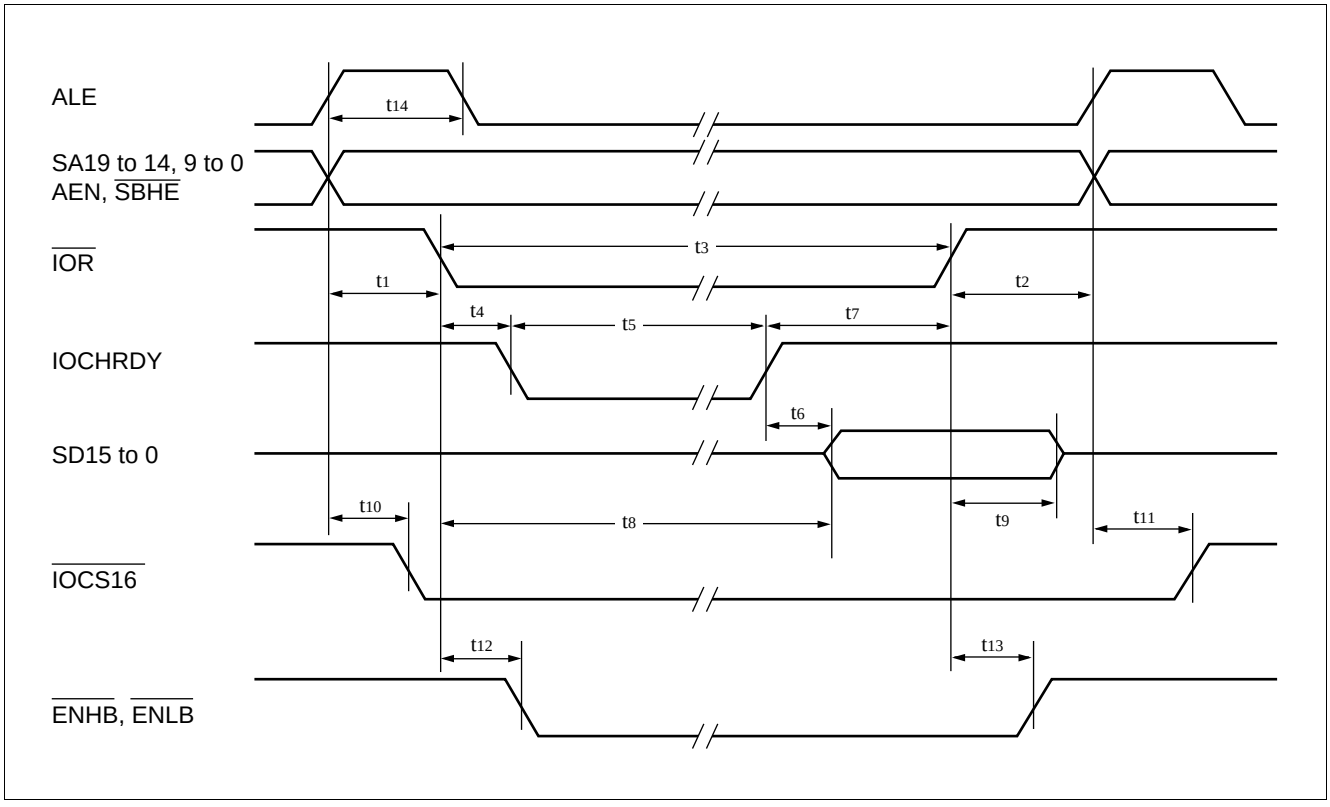
Parameter	Symbol	Value		Unit
		Min.	Max.	
Setup time for address, $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$ prior to $\overline{IOWR}$ assert	t_1	5	—	ns
Hold time for address, $\overline{CE1}$, $\overline{CE2}$ after $\overline{IOWR}$ negate	t_2	5	—	ns
Hold time for $\overline{REG}$ after $\overline{IOWR}$ negate	t_3	0	—	ns
Output delay for $\overline{ROMS}$ assert after $\overline{IOWR}$ assert	t_4	—	35	ns
Output delay for $\overline{ROMS}$ negate after $\overline{IOWR}$ negate	t_5	—	35	ns
Output delay for ROMAD assert after $\overline{IOWR}$ assert	t_6	—	30	ns
Output delay for ROMAD negate after $\overline{IOWR}$ negate	t_7	—	30	ns



(11)ISA Bus Mode Read Cycle

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

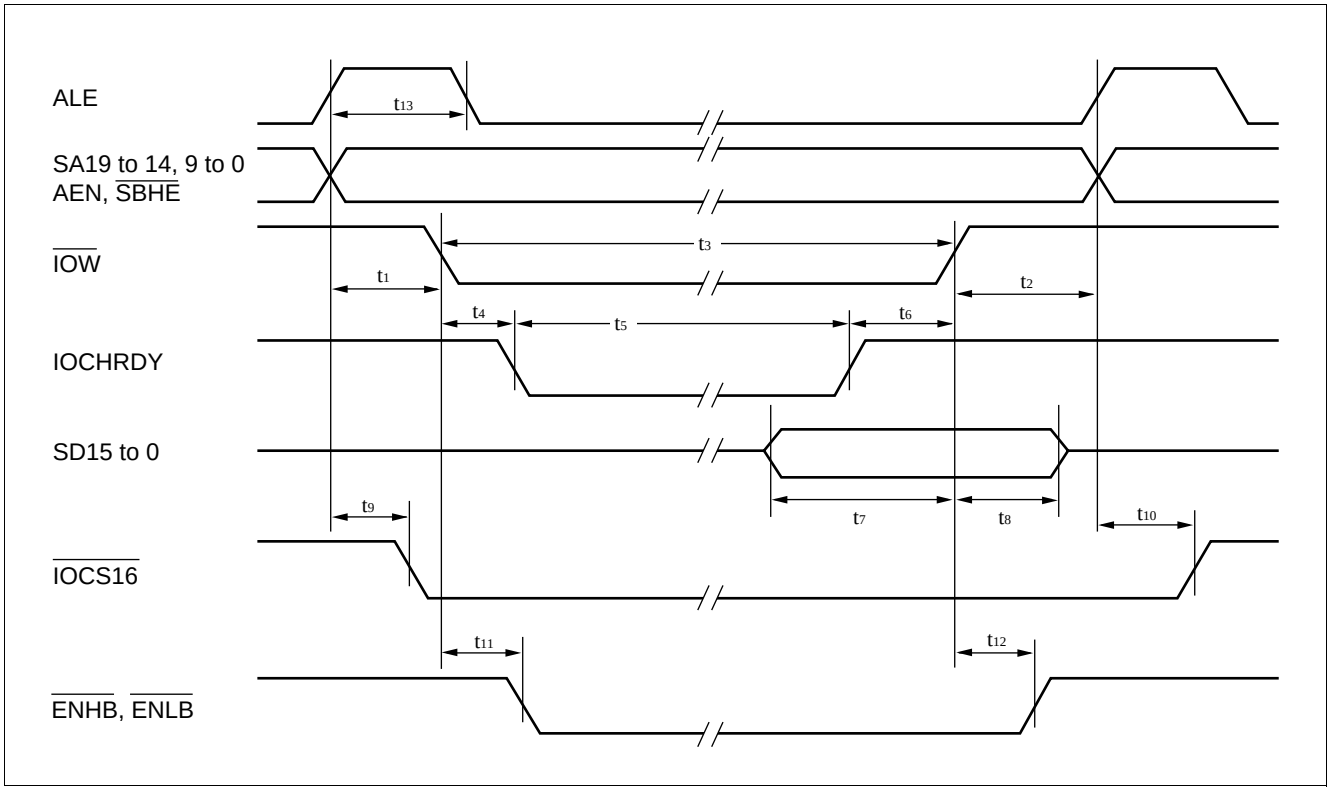
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
From the rising edge of SA19 to SA14, SA9 to SA0, and ALE or establishment of AEN or $\overline{SBHE}$ until $\overline{IOR}$ assert	t_1	15	—	—	ns
Hold time of SA19 to SA14, SA9 to SA0, AEN, $\overline{SBHE}$ from $\overline{IOR}$ negate	t_2	21	—	—	ns
$\overline{IOR}$ pulse width	t_3	50	—	—	ns
From $\overline{IOR}$ negate to IOCHRDY negate	t_4	—	—	20	ns
IOCHRDY pulse width (on conflict at the time of BMPR8 access)	t_5	—	—	175	ns
From IOCHRDY assert to SD15 to 0 enabled	t_6	—	—	30	ns
From IOCHRDY assert to IOR hold time	t_7	20	—	—	ns
From $\overline{IOR}$ assert to SD15 to 0 enabled (no conflict on bus access)	t_8	—	—	38	ns
From $\overline{IOR}$ negate to SD15 to SD0 high impedance	t_9	—	—	38	ns
From SA19 to SA14, SA9 to SA0, ALE rising edge, AEN or $\overline{SBHE}$ rising edge up to $\overline{IOCS16}$ assert	t_{10}	—	—	28	ns
From SA19 to SA14, SA9 to SA0, ALE rising edge, AEN or $\overline{SBHE}$ rising edge up to $\overline{IOCS16}$ negate	t_{11}	—	—	71	ns
From $\overline{IOR}$ assert to $\overline{ENHB}$, or $\overline{ENLB}$ assert	t_{12}	—	—	46	ns
From $\overline{IOR}$ negate to ENHB or ENLB negate	t_{13}	—	—	24	ns
ALE pulse width	t_{14}	30	—	—	ns



(12)ISA Bus Mode Write Cycle

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
From the rising edge of SA19 to SA14, SA9 to SA0, and ALE or establishment of AEN or $\overline{SBHE}$ until $\overline{IOW}$ assert	t_1	15	—	—	ns
Hold time of SA19 to SA14, SA9 to SA0, AEN, $\overline{SBHE}$ from $\overline{IOW}$ negate	t_2	21	—	—	ns
$\overline{IOW}$ pulse width	t_3	50	—	—	ns
From $\overline{IOW}$ negate to IOCHRDY negate	t_4	—	—	20	ns
IOCHRDY pulse width (on conflict at the time of BMPR8 access)	t_5	—	—	175	ns
From IOCHRDY assert to IOW hold time	t_6	20	—	—	ns
$\overline{IOW}$ to SD15 to 0 setup time	t_7	5	—	—	ns
$\overline{IOW}$ to SD15 to SD0 hold time	t_8	33	—	—	ns
From SA19 to SA14, SA9 to SA0, ALE rising edge, AEN or $\overline{SBHE}$ rising edge up to $\overline{IOCS16}$ assert	t_9	—	—	38	ns
From SA19 to SA14, SA9 to SA0, ALE rising edge, AEN or $\overline{SBHE}$ rising edge up to $\overline{IOCS16}$ negate	t_{10}	—	—	71	ns
From $\overline{IOW}$ assert to $\overline{ENHB}$, or $\overline{ENLB}$ assert	t_{11}	—	—	46	ns
From $\overline{IOW}$ negate to ENHB or ENLB negate	t_{12}	—	—	24	ns
ALE pulse width	t_{13}	30	—	—	ns



(13)General-purpose Bus Mode Read Cycle

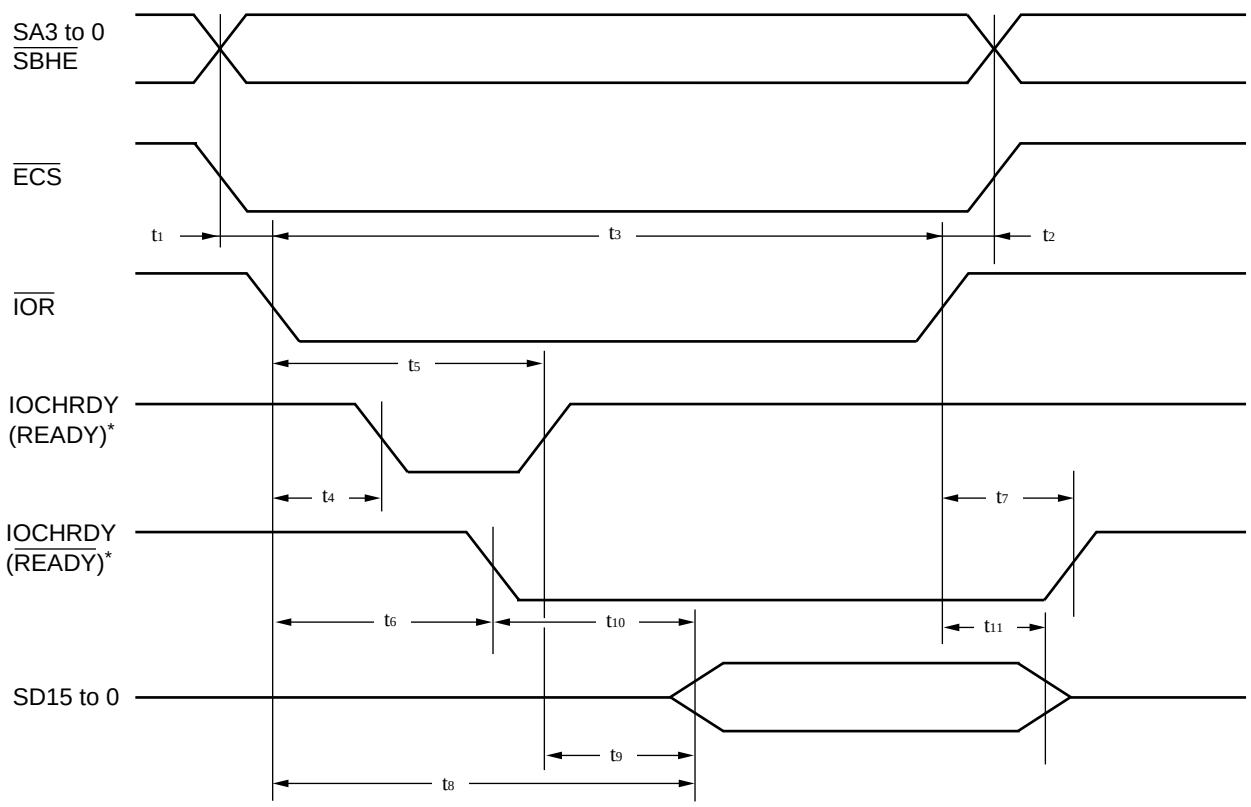
(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Address setup time (from $\overline{IOR}$ assert)	t_1	3	—	—	ns
Address hold time (from $\overline{IOR}$ negate)	t_2	3	—	—	ns
$\overline{IOR}$ pulse width	t_3	30	—	—	ns
Output delay time for READY negate	t_4	7*2	—	26*2	ns
Output delay time for READY assert	t_5	—	—	175*1	ns
Output delay time for $\overline{READY}$ assert	t_6	—	—	28/175*3	ns
Output delay time for $\overline{READY}$ negate	t_7	—	—	28	ns
Output delay time for read data (from $\overline{IOR}$ assert)	t_8	—	—	44	ns
Output delay time for read data (from READY assert)	t_9	—	—	8	ns
Output delay time for read data (from $\overline{READY}$ assert)	t_{10}	—	—	18	ns
Output hold time for read data	t_{11}	10	—	80	ns

*1: READY is negated only when the read access is conflicted with that of the network on reading the buffer memory port (BMR8).
This value would be 2.15 µs when the bus read error occurs on reading the buffer memory port.

*2: READY is negated only when the read access is conflicted with that of the network on reading the buffer memory port (BMR8).

*3: Max time is 28 ns for normal read. Max time is 175 ns only when the read access is conflicted with that of the network on reading the buffer memory port (BMR8).
This value would be 2.15 µs when the bus read error occurs on reading the buffer memory port.



* : The IOCHRDY output terminal allows the RDYPNSEL terminal to toggle between READY (active high) and READY (active low).

(14)General-purpose Bus Mode Write Cycle

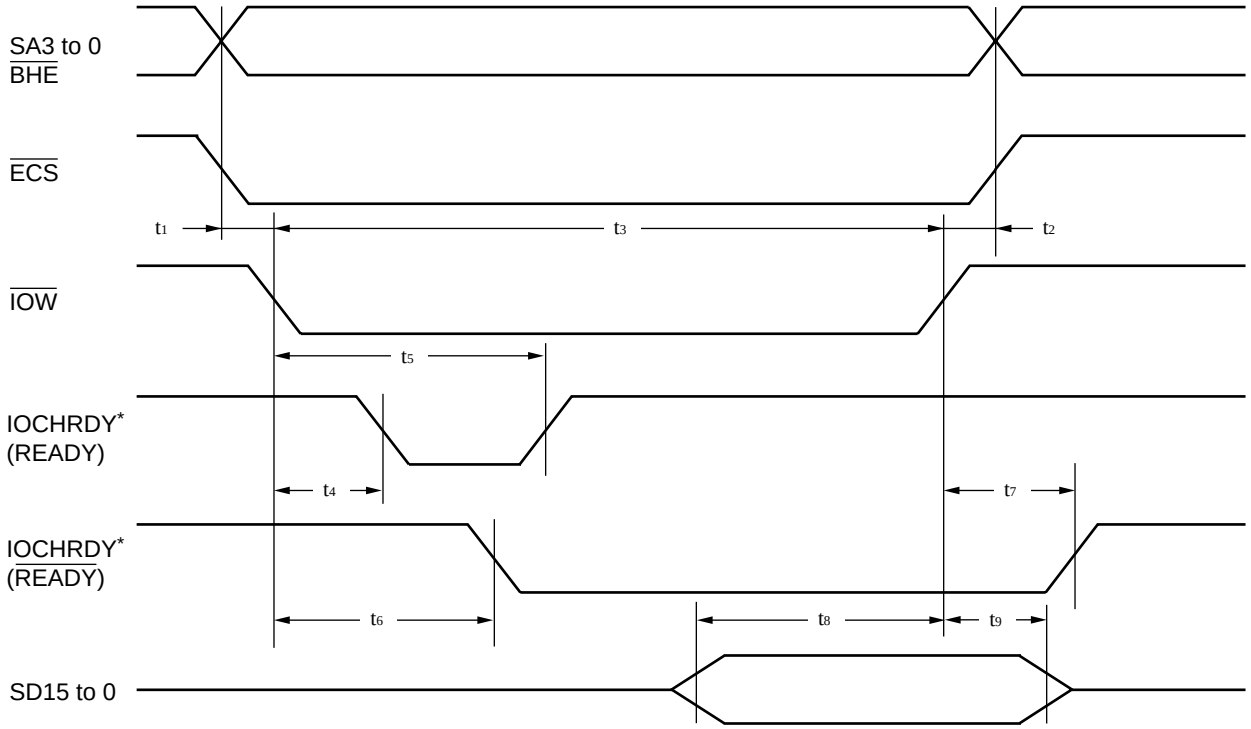
(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Address setup time (from $\overline{IOW}$ assert)	t_1	3	—	—	ns
Address hold time (from $\overline{IOW}$ negate)	t_2	3	—	—	ns
$\overline{IOW}$ pulse width	t_3	36	—	—	ns
Delay time for READY negate output	t_4	7*2	—	26*2	ns
Delay time for READY assert output	t_5	—	—	175*1	ns
Delay time for $\overline{READY}$ assert output	t_6	—	—	28/175*3	ns
Delay time for $\overline{READY}$ negate output	t_7	—	—	28	ns
Setup time for write data input	t_8	5	—	—	ns
Hold time for write data input	t_9	6	—	—	ns

*1: READY is negated only when the write access is conflicted with that of the network on writing the buffer memory port (BMR8).
This value would be 2.15 µs when the bus write error occurs on writing the buffer memory port.

*2: READY is negated only when the write access is conflicted with that of the network on writing the buffer memory port (BMR8).

*3: Max time is 28 ns for normal write. Max time is 175 ns only when the write access is conflicted with that of the network on writing the buffer memory port (BMR8). This value would be 2.15 µs when the bus write error occurs on writing the buffer memory port.

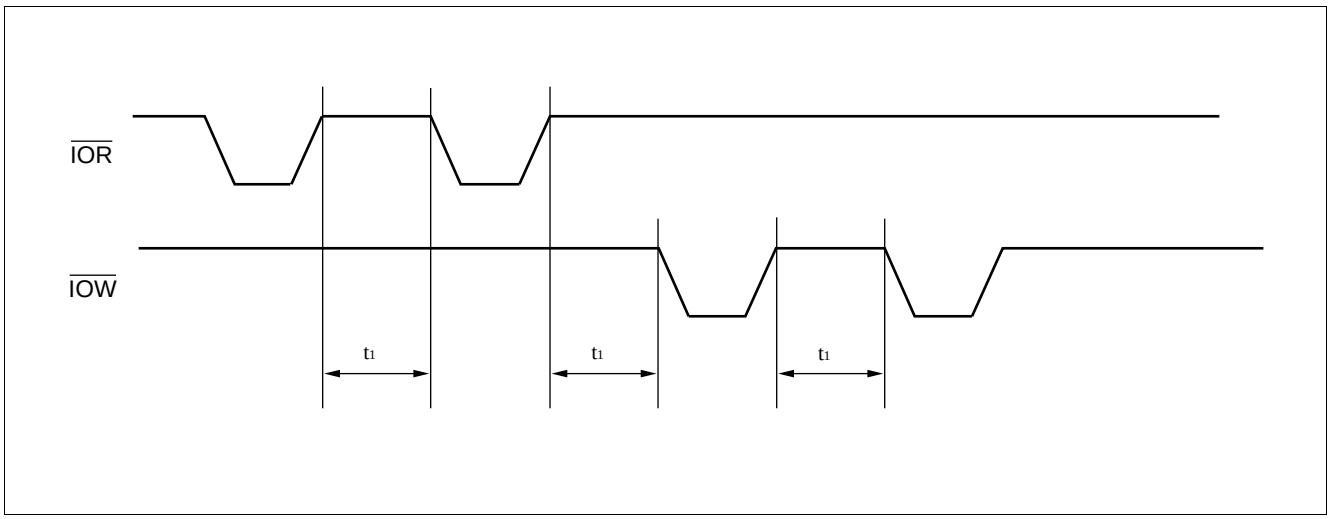


* : The IOCHRDY output terminal allows the RDYPNSEL terminal to toggle between READY (active high) and $\overline{READY}$ (active low).

(15)General-purpose Bus Mode Write Input Inhibit Period

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

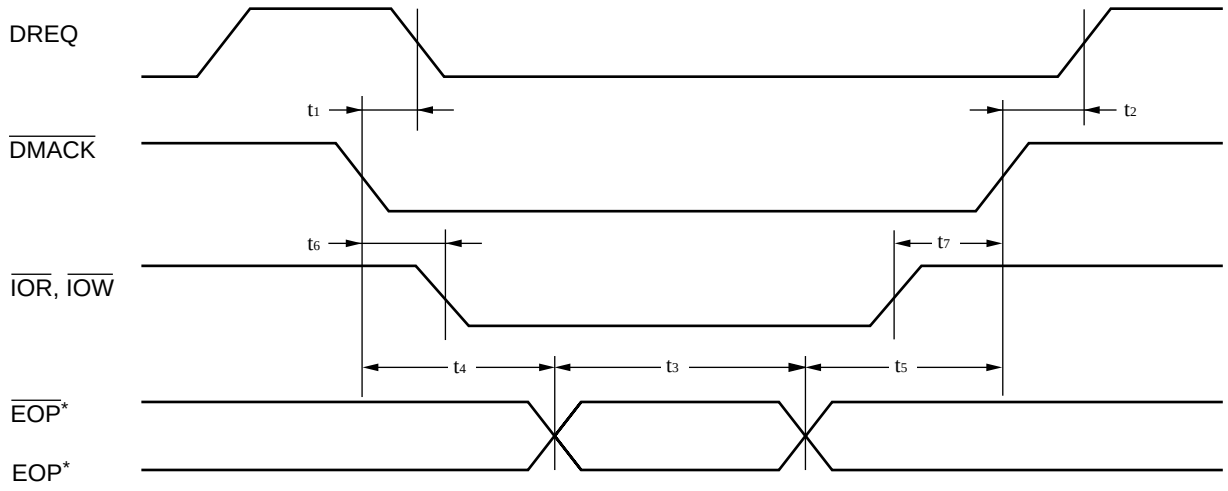
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Input inhibit period for $\overline{IOR}$ and $\overline{IOW}$.	t_1	50	—	—	ns



(16)Single DMA Access Timing

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Delay time for DREQ negate output (from $\overline{DMACK}$ assert)	t_1	—	—	21	ns
Delay time for DREQ assert output (from $\overline{DMACK}$ negate)	t_2	—	—	19	ns
EOP pulse width	t_3	10	—	—	ns
Delay time for EOP assert input	t_4	3	—	—	ns
Setup time for EOP negate	t_5	3	—	—	ns
Setup time for $\overline{DMACK}$	t_6	0	—	—	ns
Hold time for $\overline{DMACK}$ input	t_7	3	—	—	ns



* : EOP input allows the values of EOP/$\overline{EOP}$ register values for bit 1 of DLCR7 to toggle between EOP (active high) and $\overline{EOP}$ (active low).

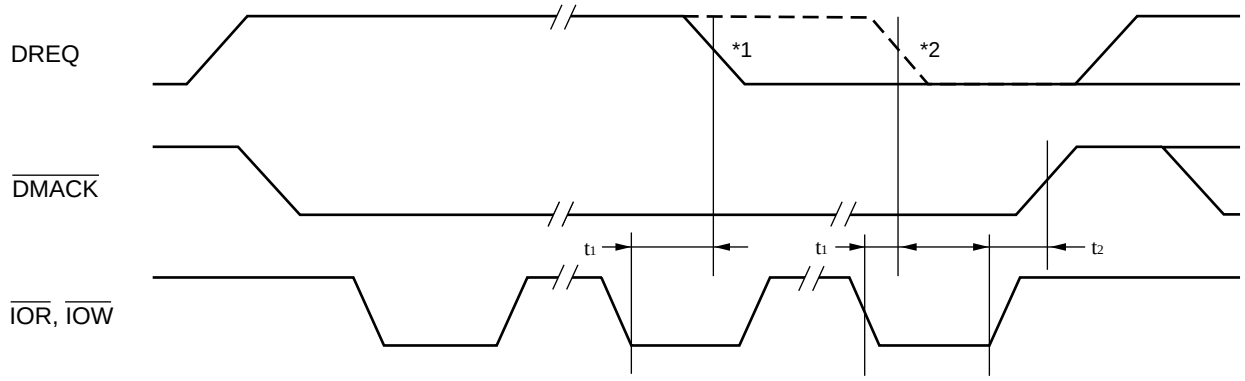
Note: IOCHRDY signal timing is identical as that of bus timing.

(17)Burst DMA Access Timing

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

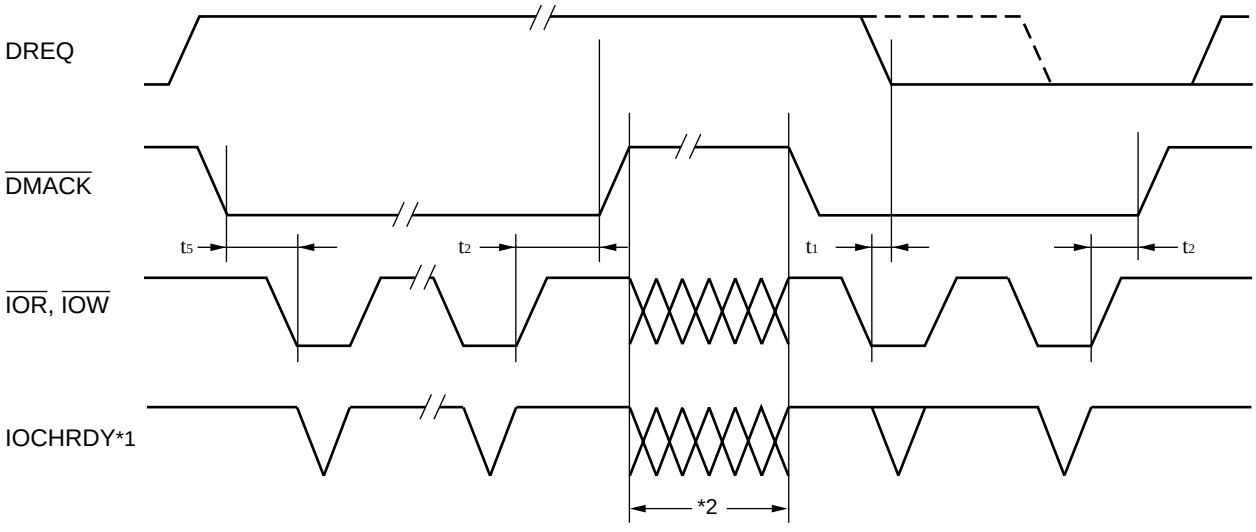
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Hold time for DREQ output	t_1	—	—	32	ns
Hold time for $\overline{DMACK}$ input (from $\overline{IOR}$, $\overline{IOW}$ negate)	t_2	3	—	—	ns
Hold time for DREQ output	t_3	4	—	28	ns
Hold time for $\overline{DMACK}$ input (from EOP/$\overline{EOP}$ negate)	t_4	3	—	—	ns
Setup time for $\overline{DMACK}$ input	t_5	0	—	—	ns

- **Burst DMA access timing (Exiting DMA from the MB86967)**



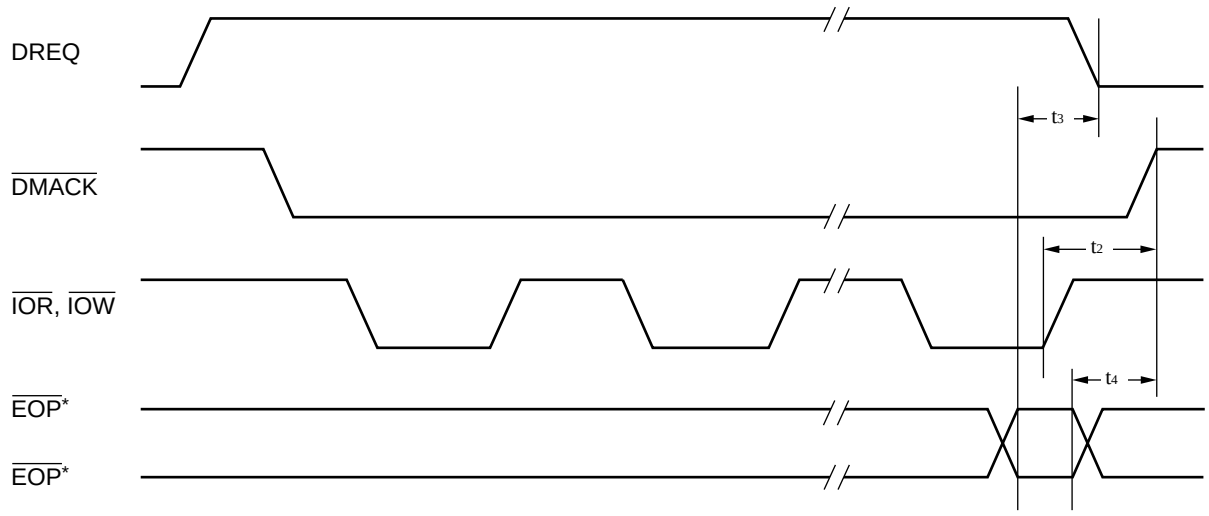
*1: This transition goes low at a single cycle before the last DMA when DLCR4 bit 2 is 1.
*2: This transition goes low at the last cycle of DMA when DLCR4 bit 2 is 0.

- **Burst DMA access timing (When DMA is interrupted by $\overline{DMACK}$ input)**



*1: IOCHRDY signal timing is identical as that of bus timing.
*2: Interrupt period for DMA transfer

- **Burst DMA access timing (When DMA is exited with the EOP input)**



* : EOP input allows the values of EOP/$\overline{EOP}$ register values for bit 1 of DLCR7 to toggle between EOP (active high) and $\overline{EOP}$ (active low).

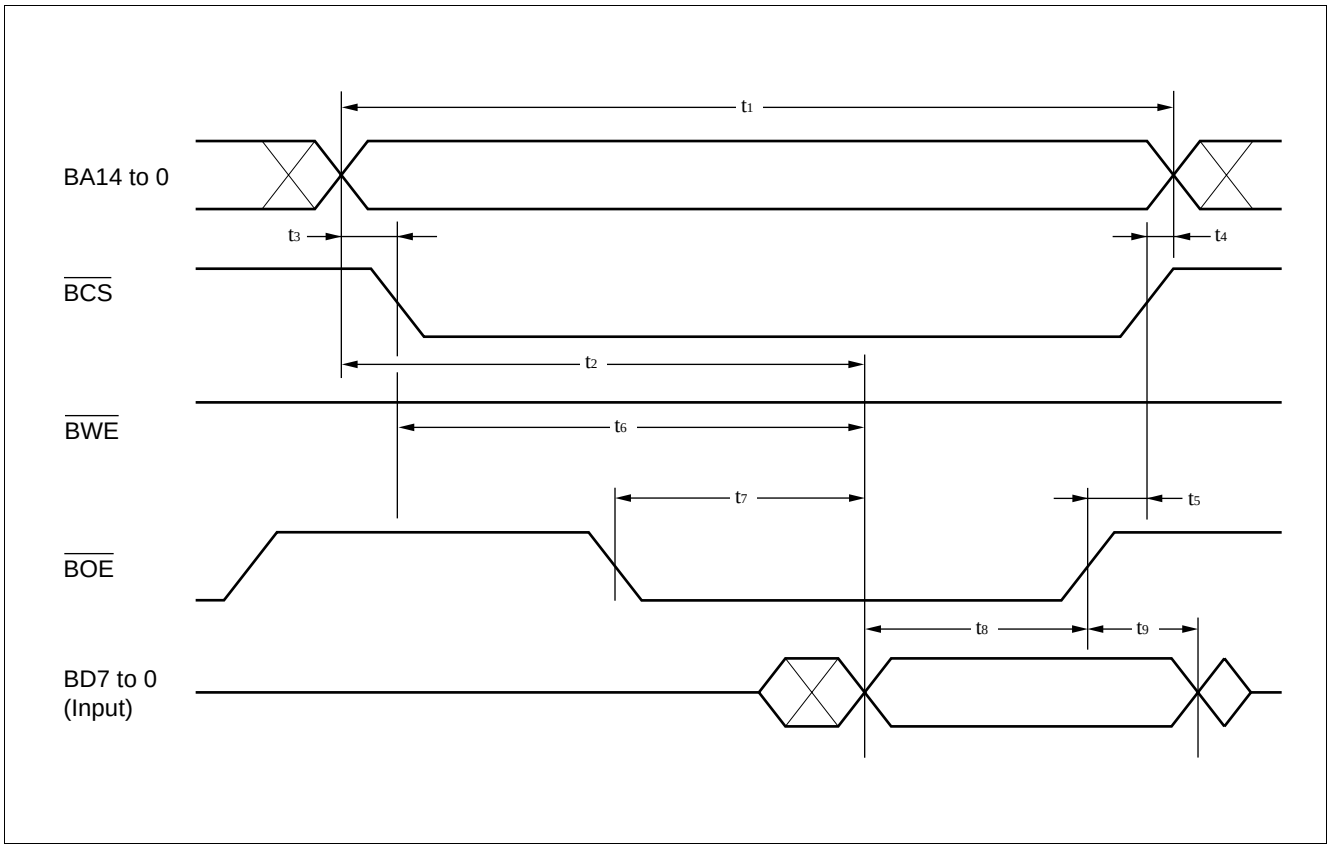
Note: IOCHRDY signal timing is identical as that of bus timing.

(18)Buffer Memory Read Timing

- **100 ns cycle access**

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

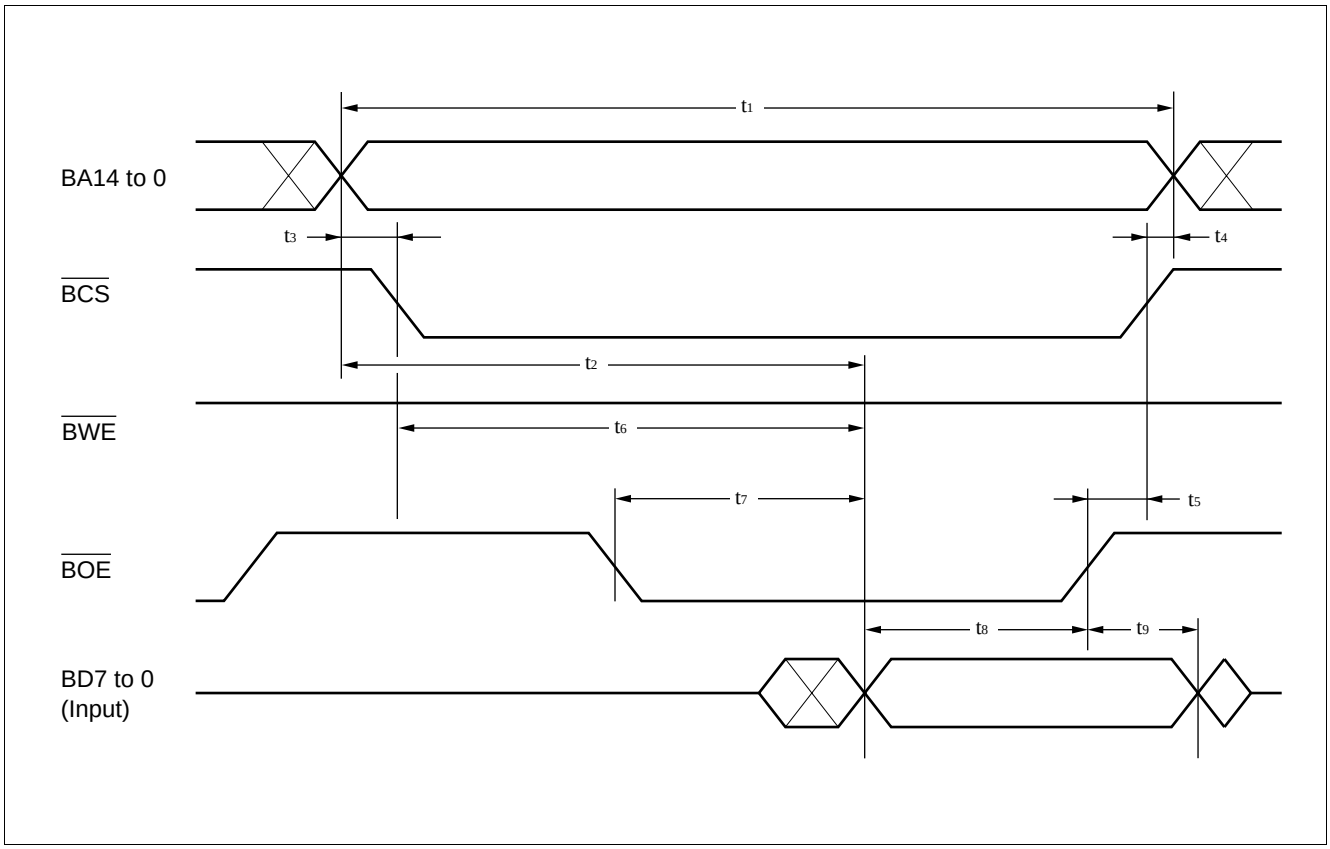
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Read cycle time (100 ns cycle mode)	t_1	—	100	—	ns
Address access time	t_2	—	—	81	ns
Address setup time (from $\overline{BCS}$ Low)	t_3	0	—	8	ns
Address hold time (from $\overline{BCS}$ High)	t_4	0	—	—	ns
Setup time for $\overline{BOE}$ output (from $\overline{BCS}$ High)	t_5	—	—	5	ns
Access time for chip select	t_6	—	—	81	ns
Access time for output enable	t_7	—	—	49	ns
Setup time for data	t_8	15	—	—	ns
Hold time for data	t_9	0	—	—	ns



- **150 ns cycle access**

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Read cycle time (150 ns cycle mode)	t_1	—	150	—	ns
Address access time	t_2	—	—	81	ns
Address setup time (from $\overline{BCS}$ Low)	t_3	0	—	8	ns
Address hold time (from $\overline{BCS}$ High)	t_4	0	—	—	ns
Setup time for $\overline{BOE}$ output (from $\overline{BCS}$ High)	t_5	—	—	5	ns
Access time for chip select	t_6	—	—	81	ns
Access time for output enable	t_7	—	—	49	ns
Setup time for data	t_8	15	—	—	ns
Hold time for data	t_9	0	—	—	ns

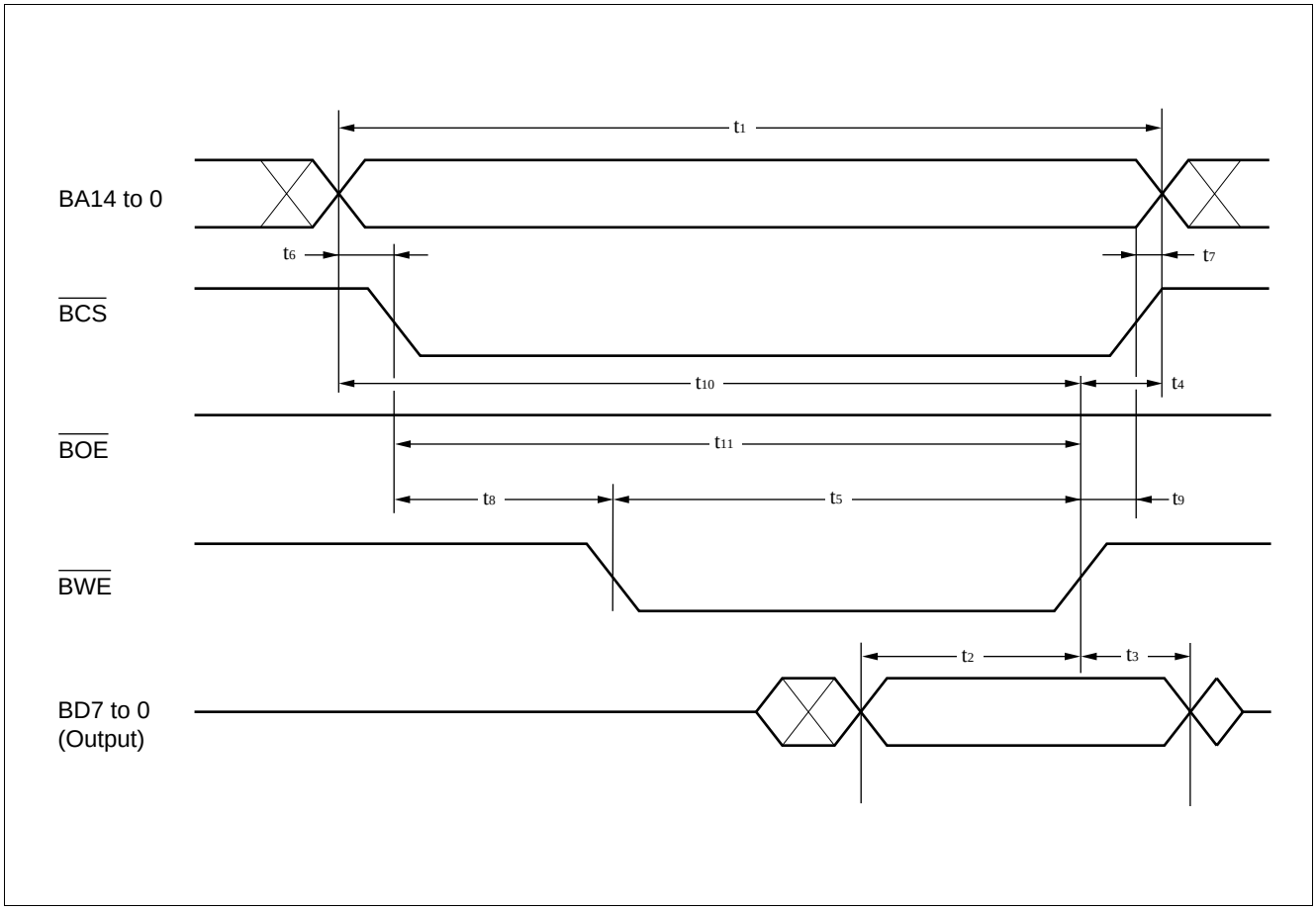


(19)Buffer Memory Write Timing

- **100 ns cycle access**

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

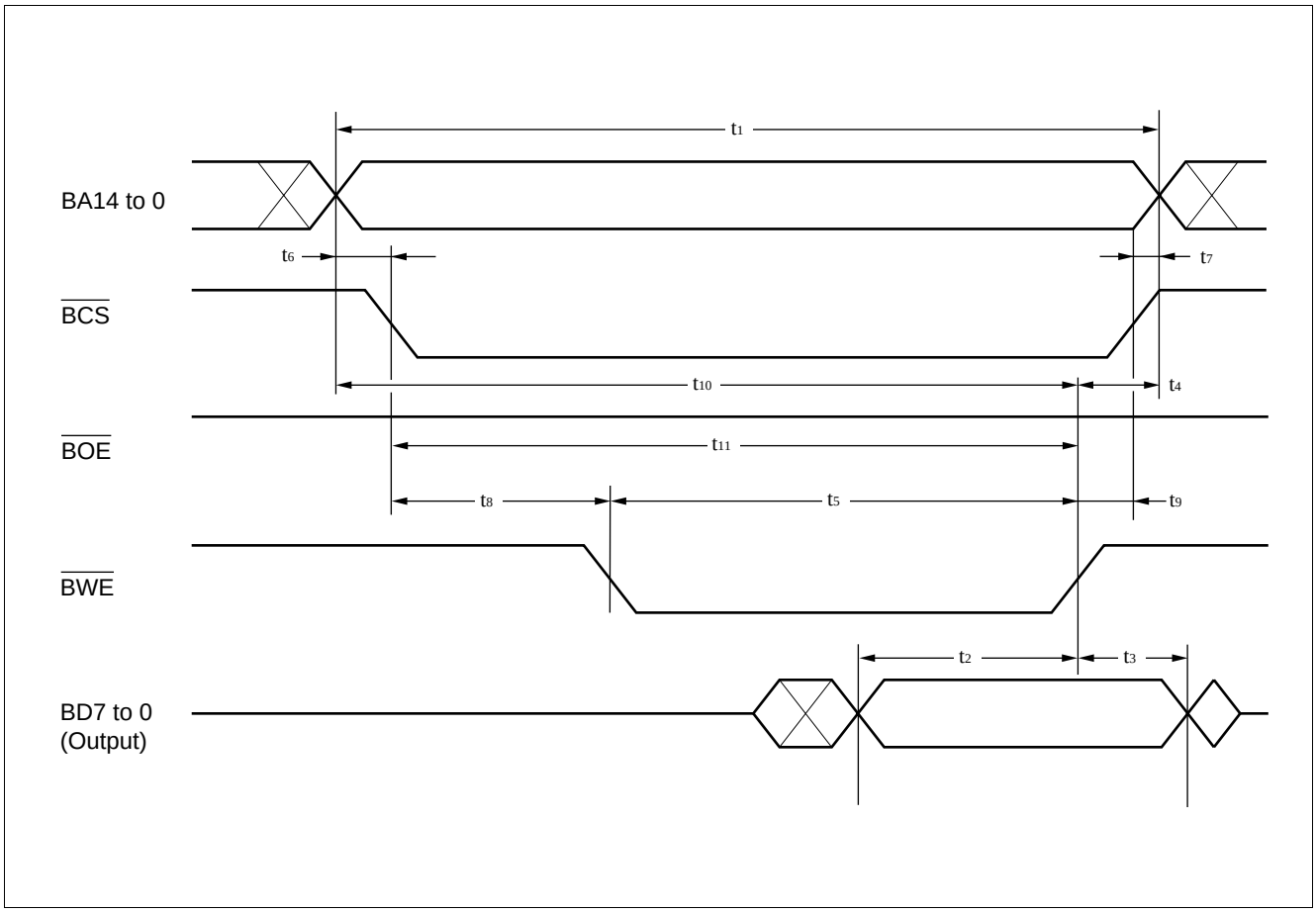
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Write cycle time (100 ns cycle mode)	t_1	—	100	—	ns
Setup time for data	t_2	40	—	—	ns
Hold time for data	t_3	10	—	—	ns
Address hold time (from $\overline{WE}$ High)	t_4	12	—	—	ns
$\overline{WE}$ pulse width	t_5	60	—	—	ns
Address setup time (from $\overline{BCS}$ Low)	t_6	2	—	8	ns
Address hold time (from $\overline{BCS}$ High)	t_7	0	—	—	ns
Delay time for $\overline{WE}$ output (from $\overline{BCS}$ Low)	t_8	0	—	—	ns
Setup time for $\overline{WE}$ output (from $\overline{BCS}$ High)	t_9	0	—	—	ns
Address determination time	t_{10}	71	—	—	ns
Chip select determination time	t_{11}	62	—	—	ns



- **150 ns cycle access**

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

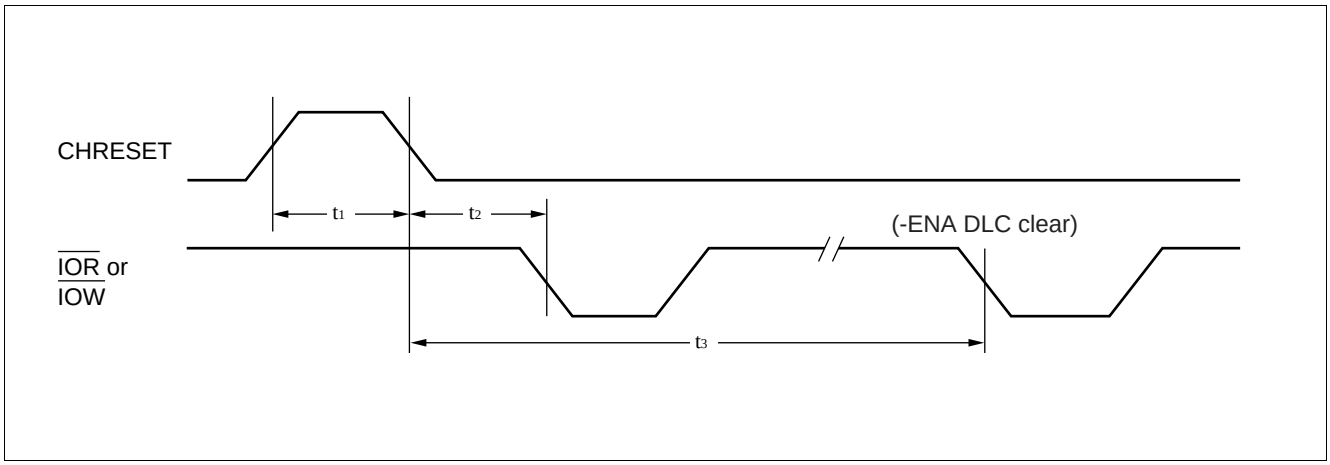
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Write cycle time (150 ns cycle mode)	t_1	—	150	—	ns
Setup time for data	t_2	40	—	—	ns
Hold time for data	t_3	10	—	—	ns
Address hold time (from $\overline{WE}$ High)	t_4	12	—	—	ns
$\overline{WE}$ pulse width	t_5	100	—	—	ns
Address setup time (from $\overline{BCS}$ Low)	t_6	2	—	8	ns
Address hold time (from $\overline{BCS}$ High)	t_7	0	—	—	ns
Delay time for $\overline{WE}$ output (from $\overline{BCS}$ Low)	t_8	0	—	—	ns
Setup time for $\overline{WE}$ output (from $\overline{BCS}$ High)	t_9	0	—	—	ns
Address determination time	t_{10}	110	—	—	ns
Chip select determination time	t_{11}	100	—	—	ns



(20)Reset Timing

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

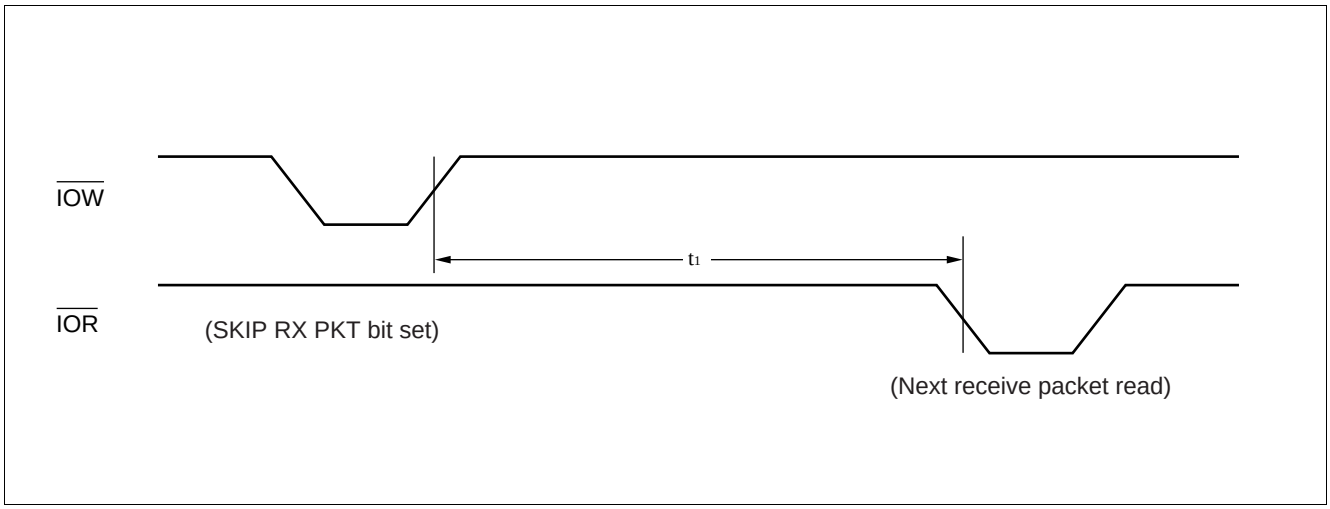
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Reset pulse width	t_1	200	—	—	ns
Register access enable start time	t_2	300	—	—	ns
Start time for transmit & receive operation	t_3	200	—	—	µs



(21)Skip Packet Timing

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

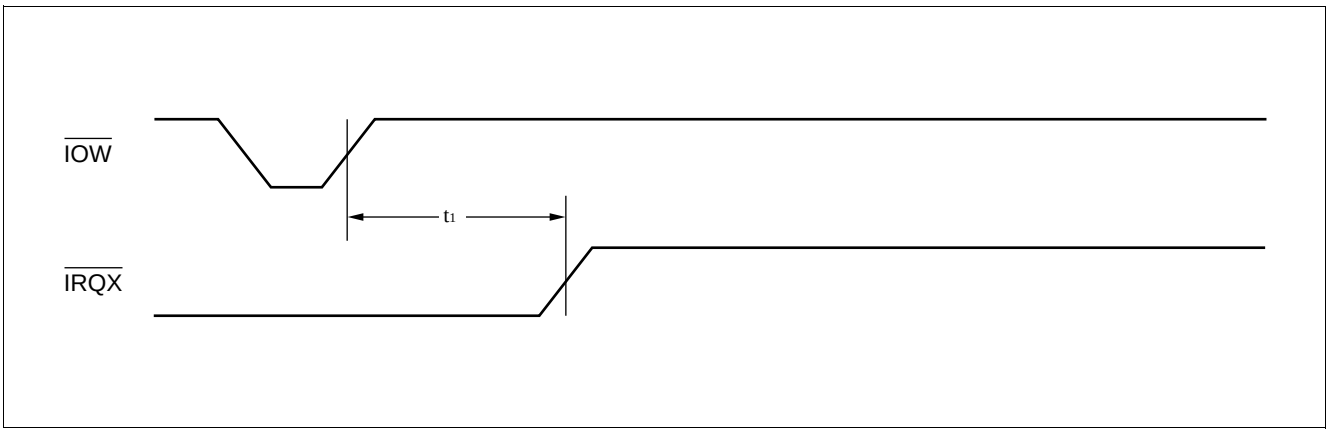
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Skip end time	t_1	300	—	—	ns



(22)Interrupt Output Timing

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Delay time for interrupt output clear	t_1	5	—	40	ns



(23)Jabber Timing

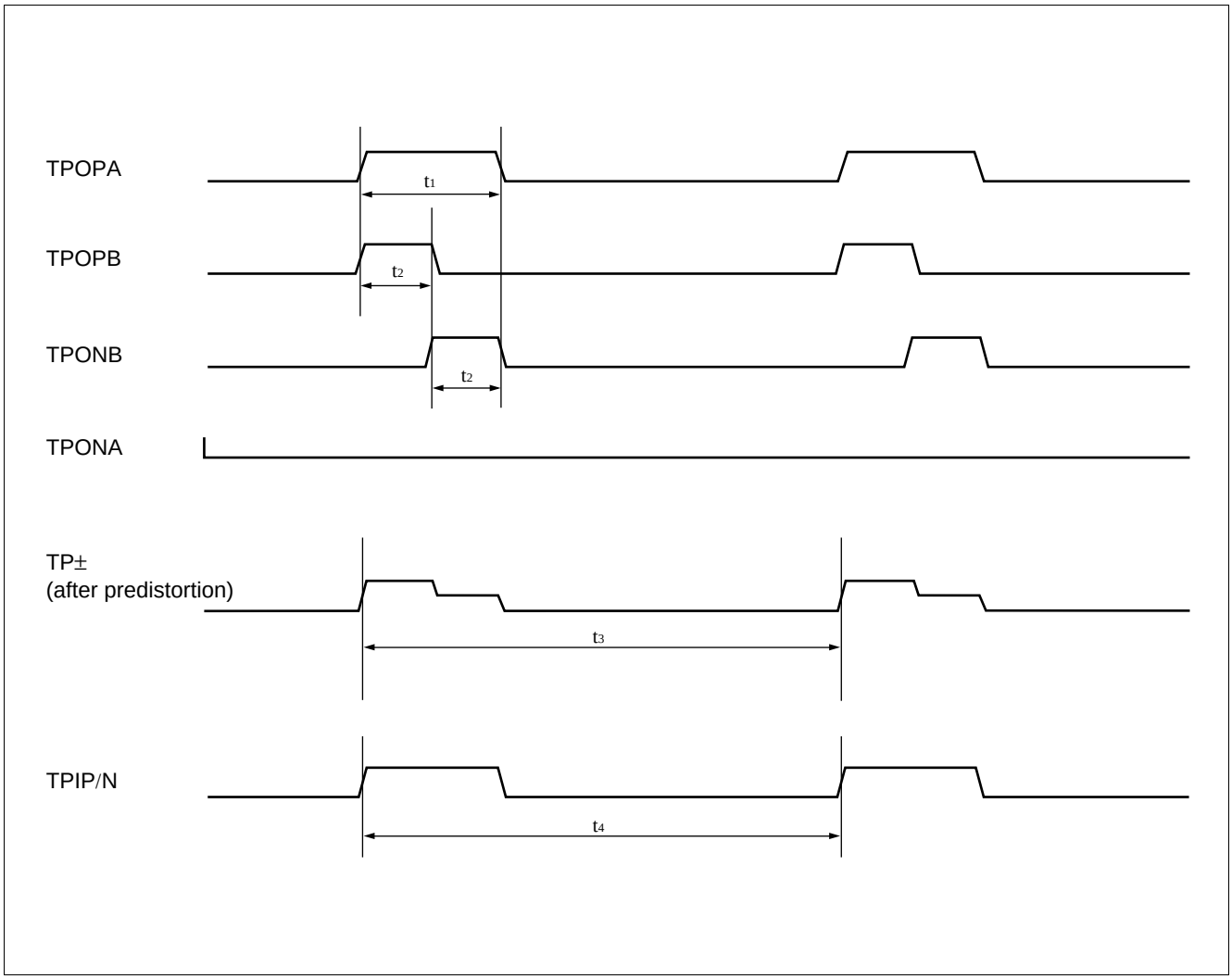
(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Max transmit time	—	—	64	96	128	ns
Jabber stop timer	—	—	480	512	544	ns

(24)Link Test Timing

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

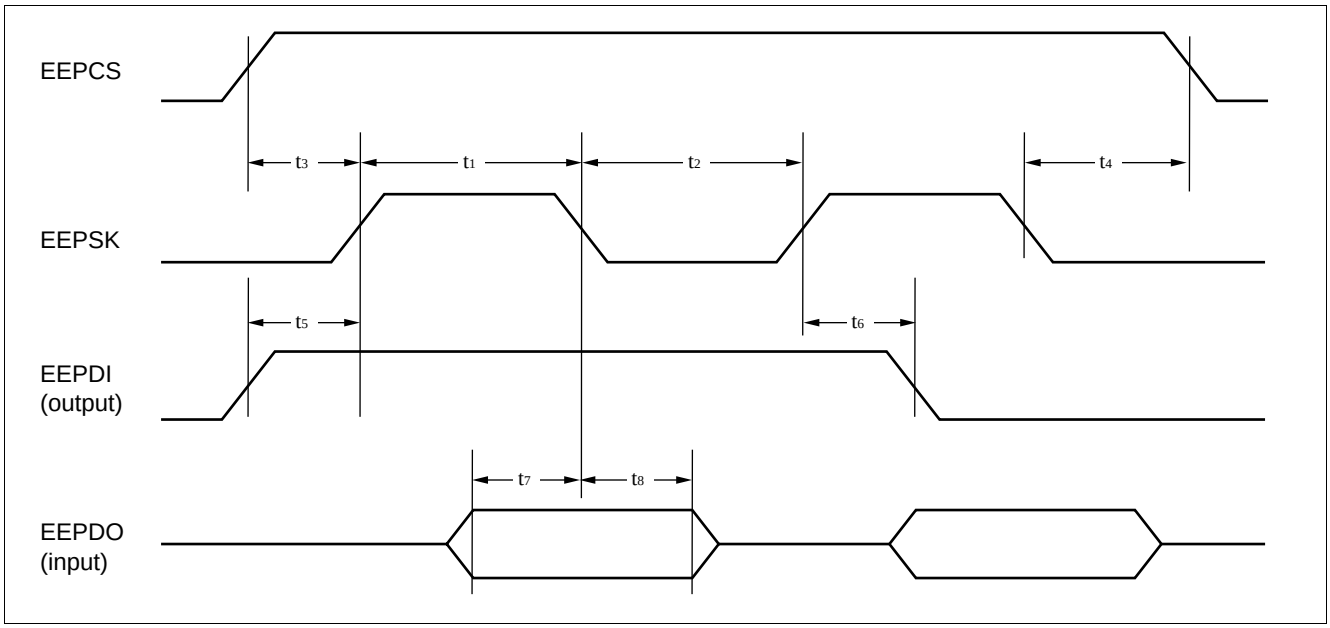
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Link pulse width for TPOPA	t_1	—	100	—	ns
Link pulse width for TPOPB and TPONB	t_2	—	50	—	ns
Link pulse transmit interval	t_3	15	16	17	ms
Effective link pulse receive interval	t_4	4.0	—	65	ms

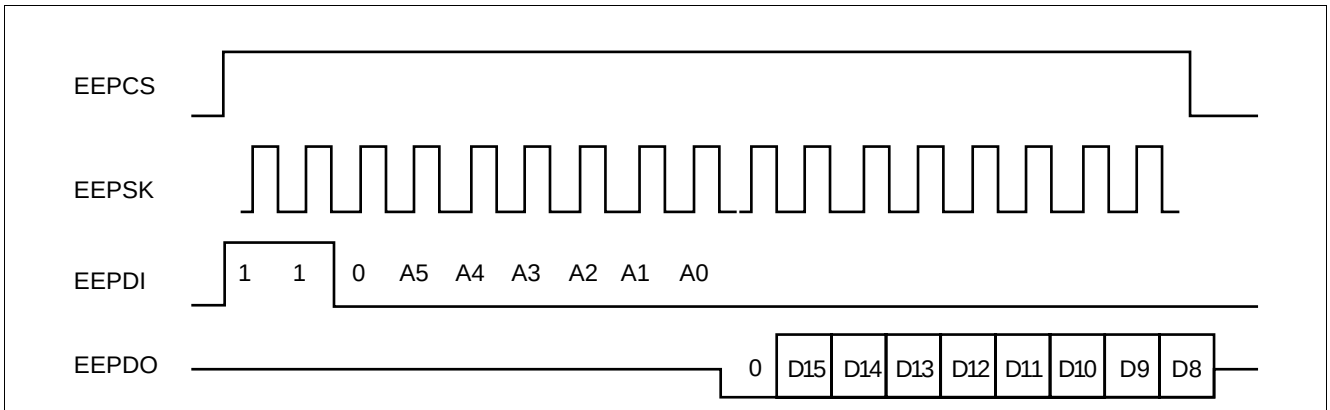


(25)Timing for reading the EEPROM default setting information (jumperless ISA mode)

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Shift clock “H” pulse width	t_1	—	600	—	ns
Shift clock “L” pulse width	t_2	—	600	—	ns
Chip select setup time	t_3	—	400	—	ns
Chip select hold time	t_4	—	200	—	ns
DI data setup time	t_5	—	200	—	ns
DI data hold time	t_6	—	200	—	ns
DO data setup time	t_7	100	—	—	ns
DO data hold time	t_8	100	—	—	ns





Notes:
- Use the NMC93C06 or NMC93C46 for EEPROM by National Semiconductor or its equivalent.
- Control signal or data for EEPROM requires control through software when writing data or reading the node ID data. It is to be controlled so that it meets the AC timing requirements for EEPROM.

(26)SQE Test Timing

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
SQE test wait timer	—	800	1000	1200	ns
SQE test timer	—	800	1000	1200	ns

(27)LED Turn-on Time

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Receive LED turn-on time	—	—	128	—	ms
Transmit LED turn-on time	—	—	128	—	ms
Collision turn-on time	—	—	128	—	ms

(28)Loopback Test

(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

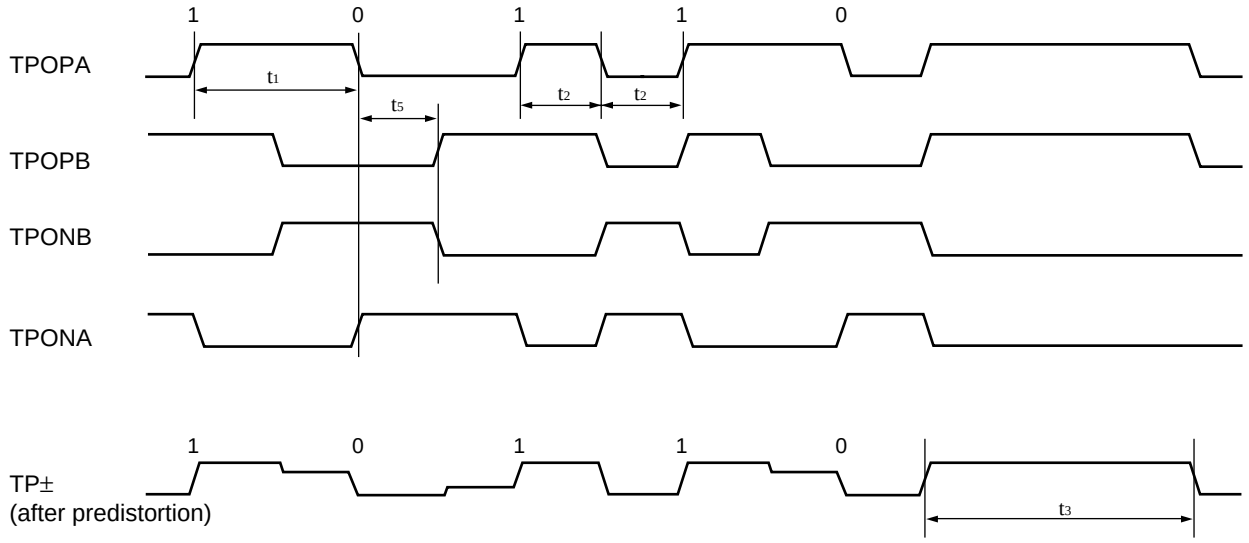
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Setup time for loopback signal (DLCR4, bit 1) prior to starting to transmit	—	100	—	—	ns
Hold time for loopback signal (DLCR4, bit1) after transmit.	—	100	—	—	ns

(29)Timing for transmitting TP

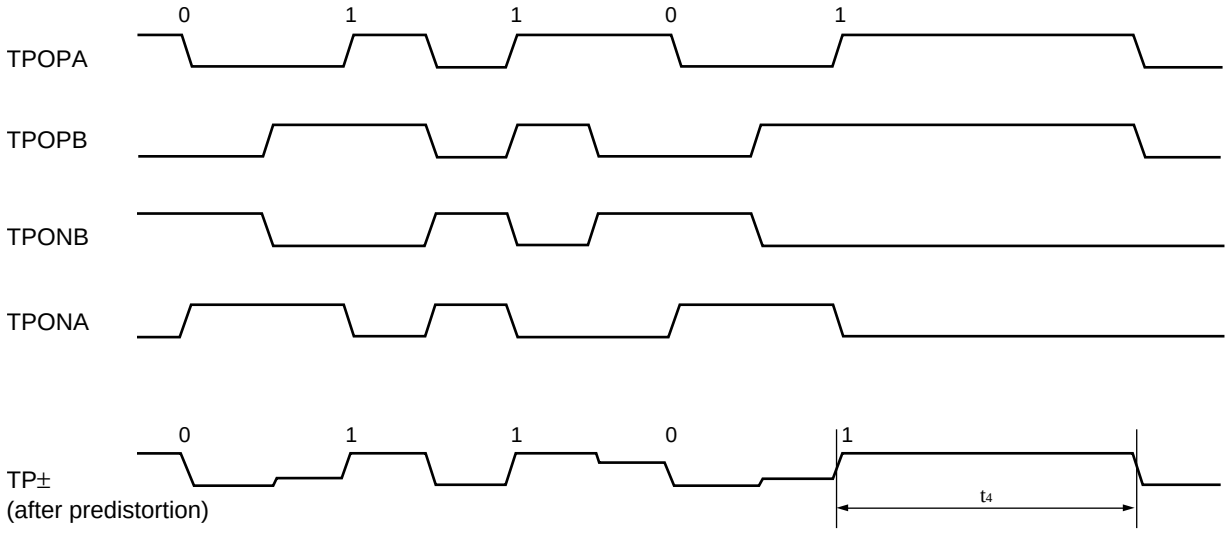
(V_{DD} = +5 V ± 5%, GND = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Data width for transmitting TP (1, 0, 1, 0···)	t_1	—	100	—	ns
Data with for transmitting TP (1, 1, 1, 1, ··· or 0, 0, 0, 0, ···)	t_2	—	50	—	ns
Data width for end of packet (the last data: “0”)	t_3	—	250	—	ns
Data width for end of packet (the last data: “1”)	t_4	—	300	—	ns
Delay time from TPOPA to TPOPB or from TPONA to TPONB.	t_5	—	50	—	ns

- **When the last data is “0”**

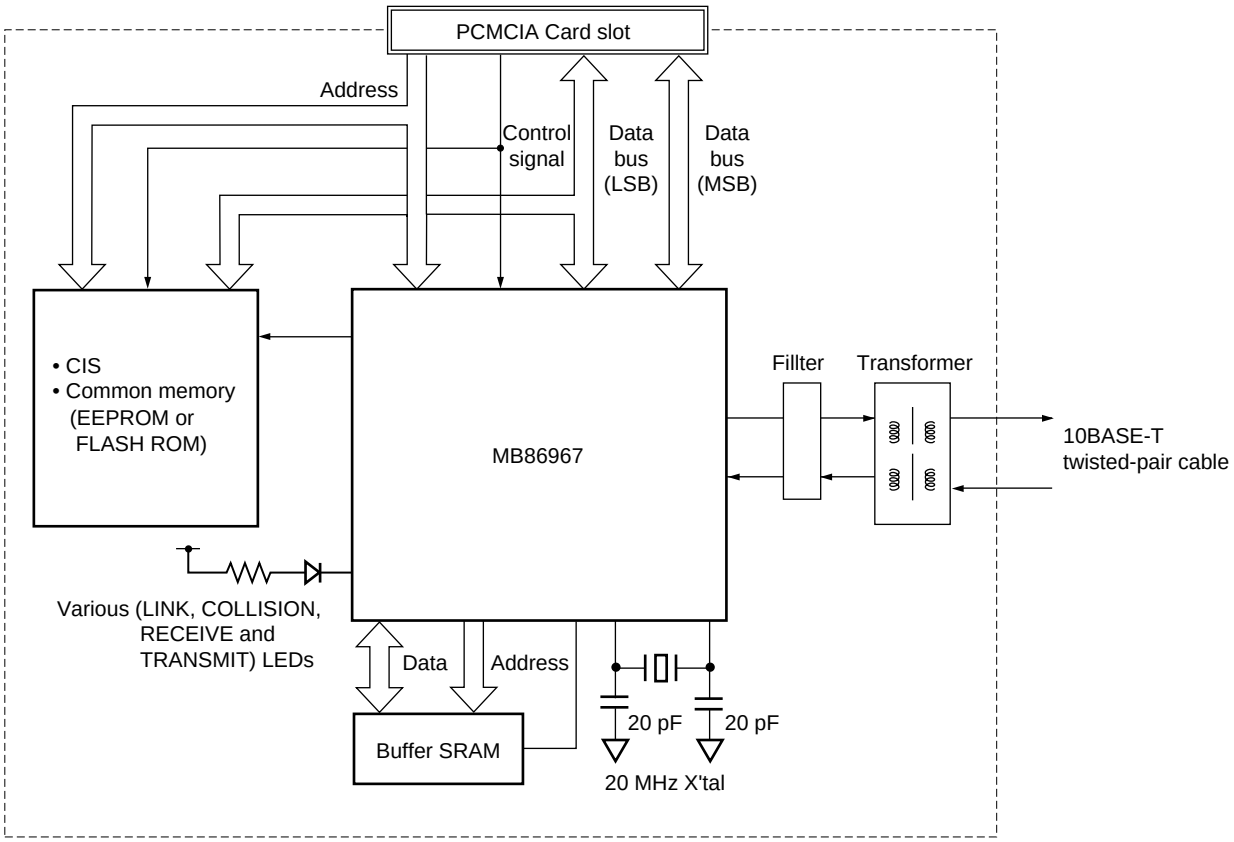


- **When the last data is “1”**

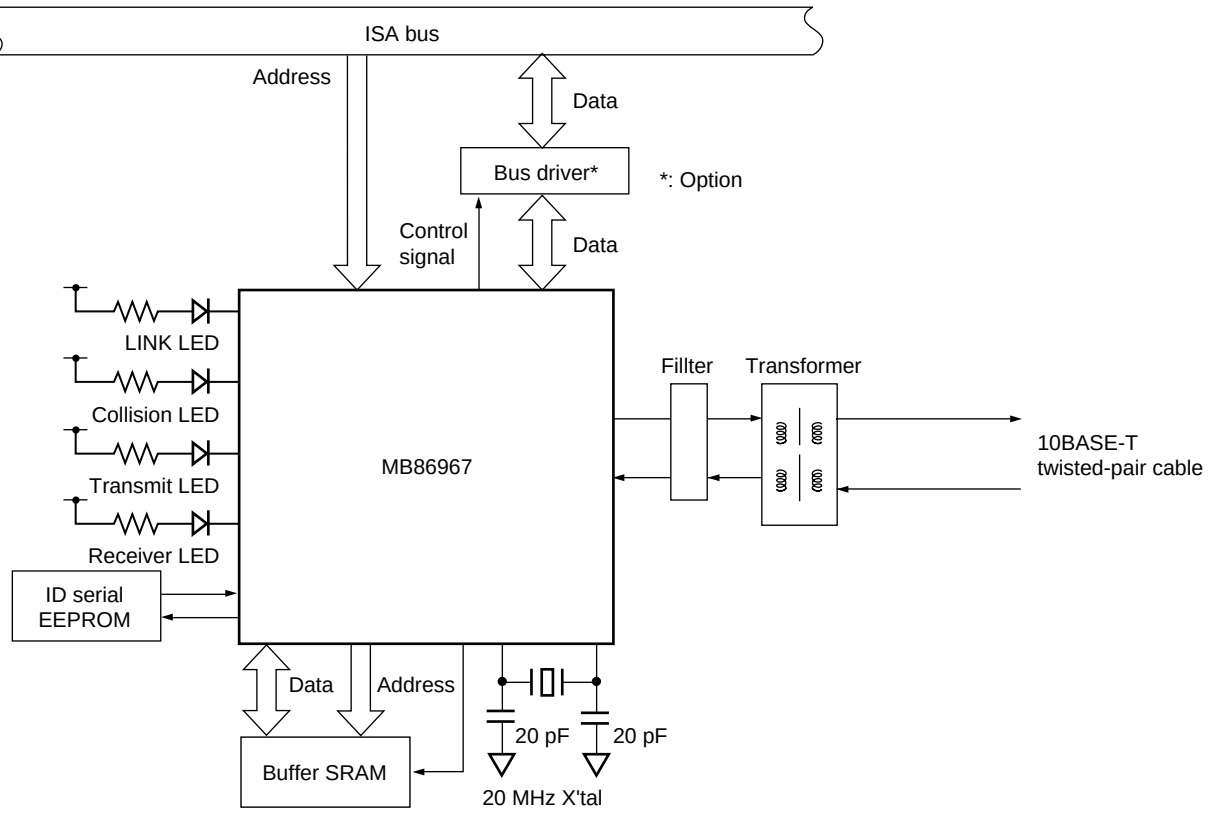


■ SYSTEM CONFIGURATION EXAMPLE

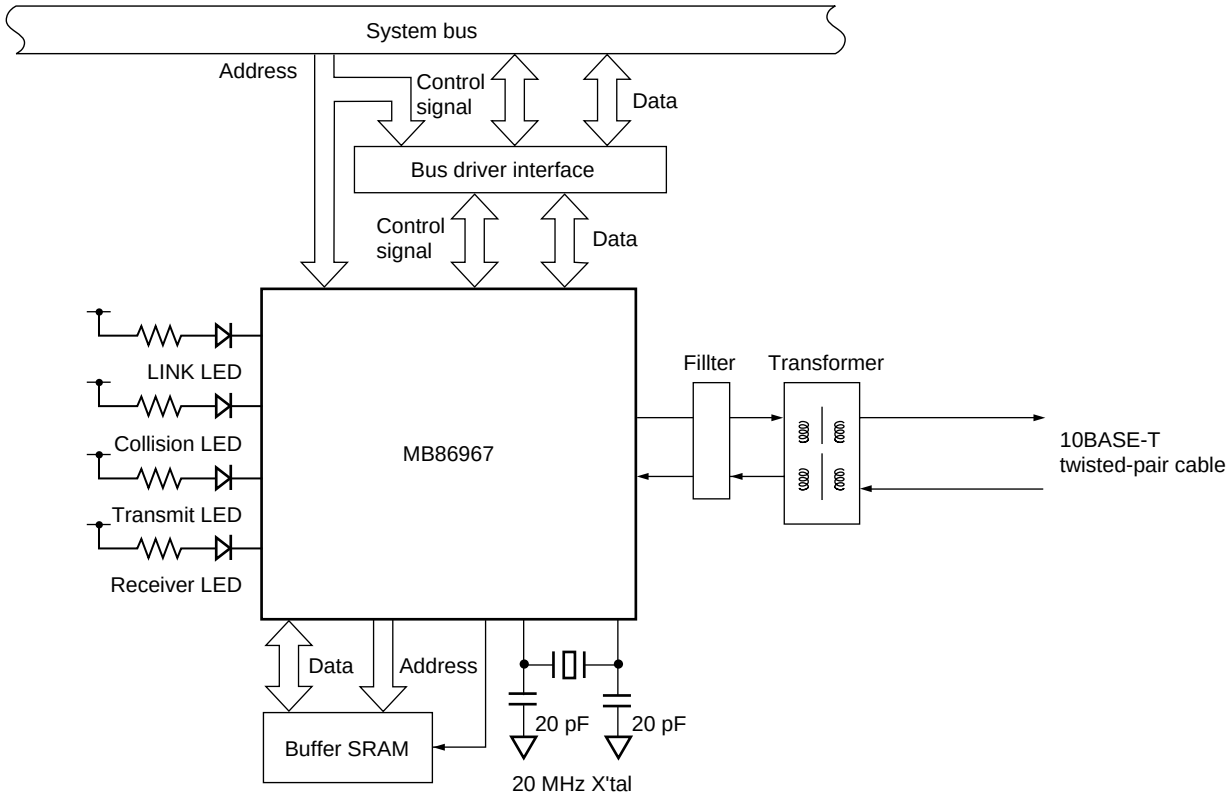
• **PC card mode**



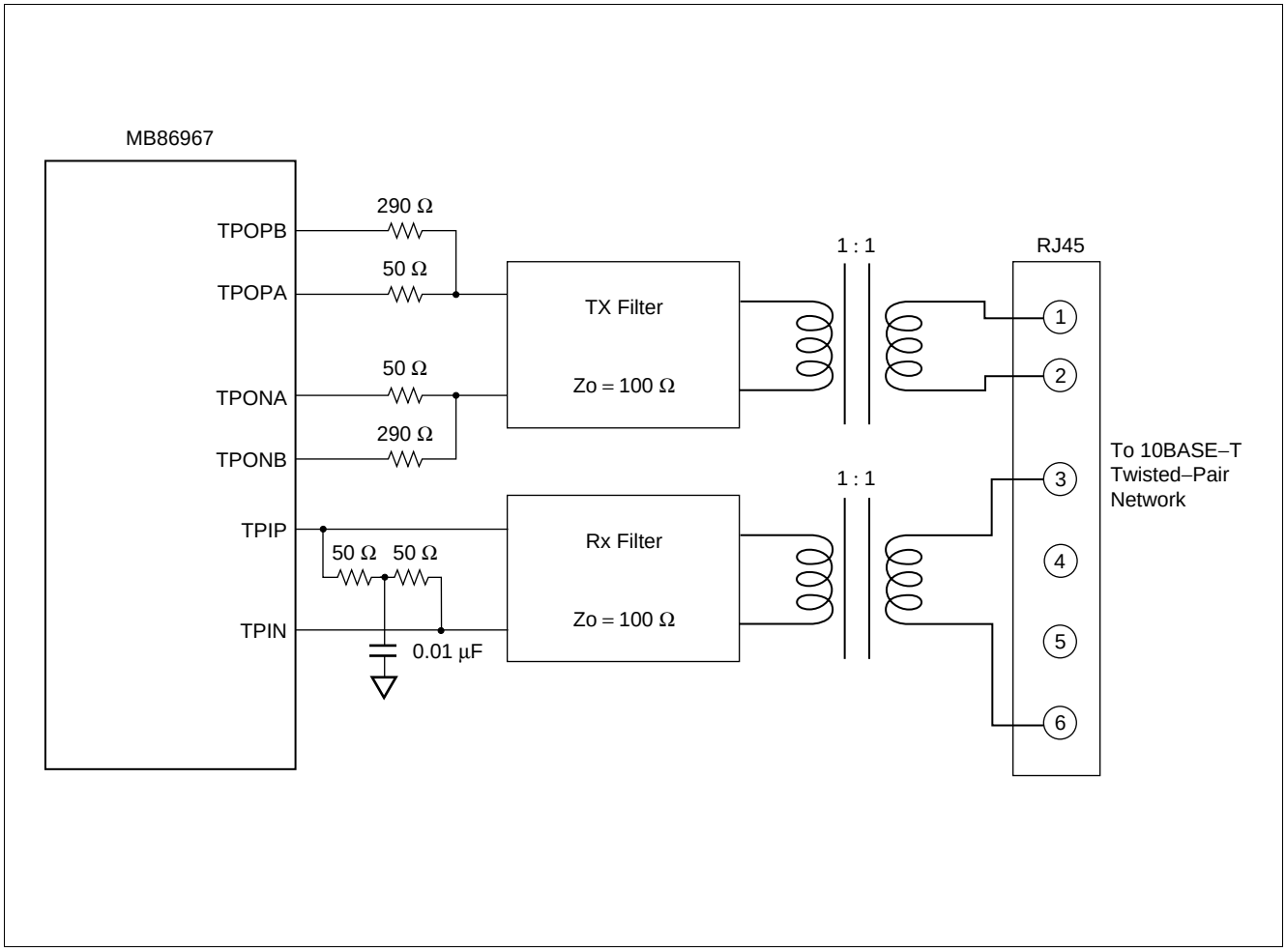
- **ISA bus mode**


ISA bus
Address
Data
Bus driver*
*: Option
Control signal
Data
LINK LED
Collision LED
Transmit LED
Receiver LED
ID serial EEPROM
MB86967
Fillter
Transformer
10BASE-T twisted-pair cable
Data
Address
Buffer SRAM
20 pF
20 pF
20 MHz X'tal

- **General-purpose bus mode**



■ 10 BASE-T INTERFACE CIRCUIT



- **Recommended pulse transformer**

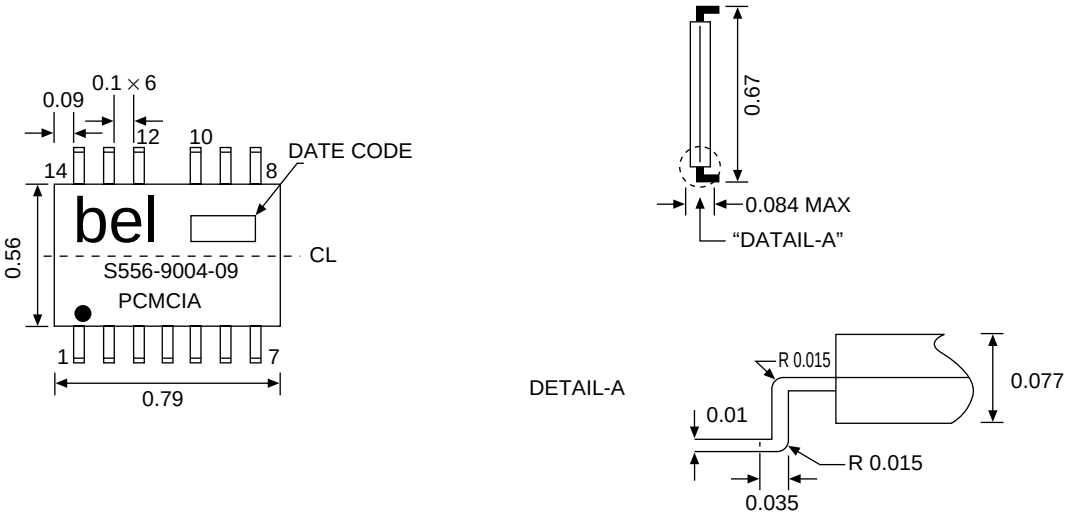
Recommended transformer for the MB86967 is as follows:

Model: S556-9004-09

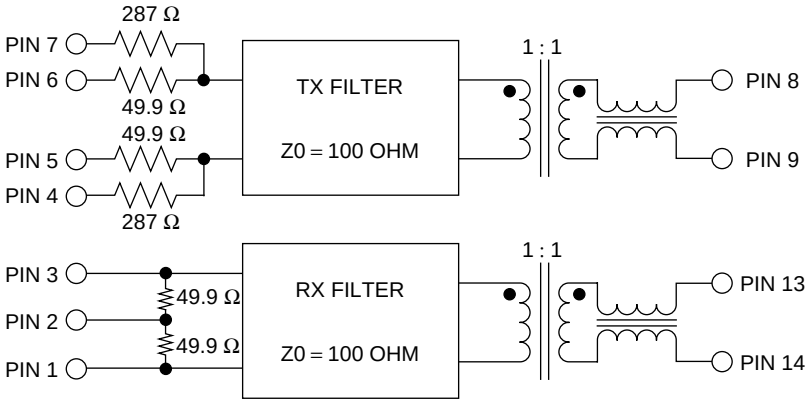
Manufacturer: Bel Fuse Ltd.

- **Overview of S556-9004-09**

[External view units in inches]

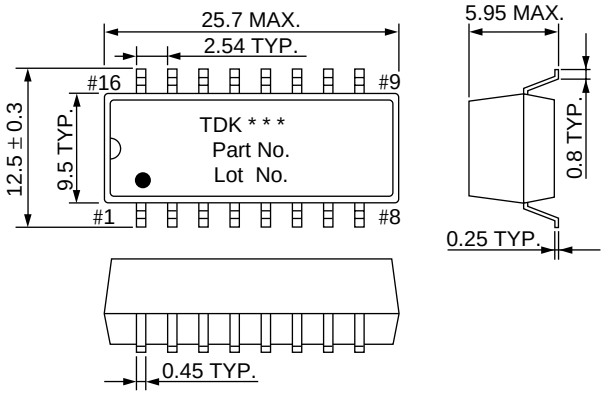


[Internal circuit]



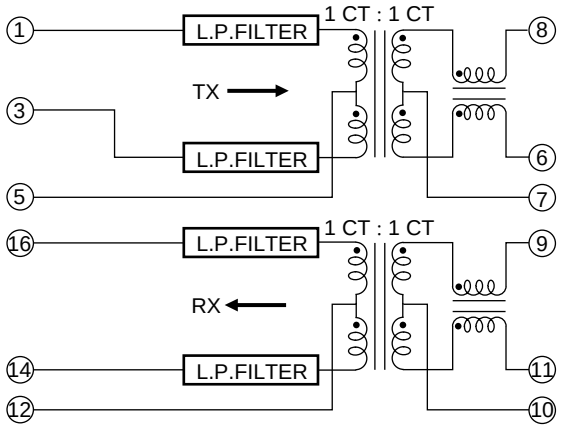
Model: TLA-3M103
Manufacturer · Distributor: TDK Co.

- **Overview of TLA-3M103**
  [External view units in mm]



* * * : COUNTRY OF ORIGIN

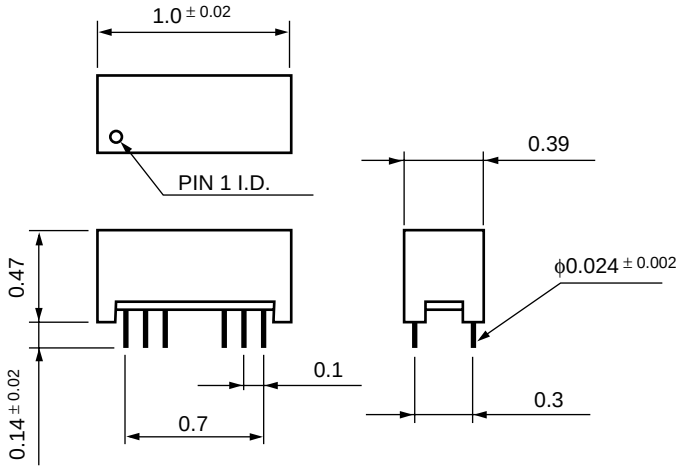
[Internal circuit]



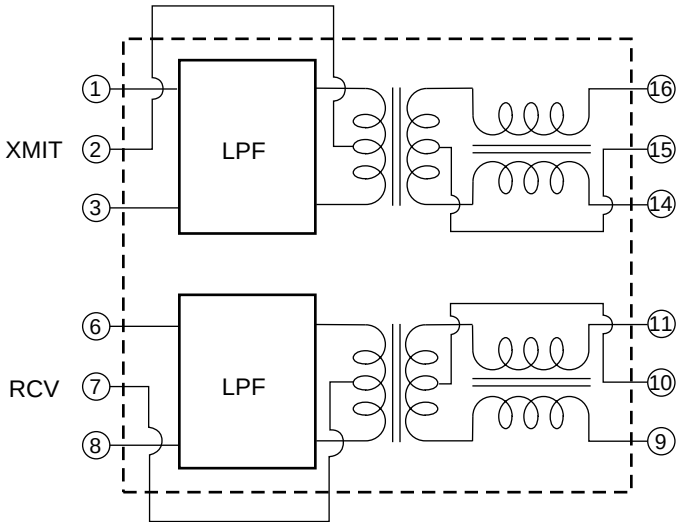
N.C. pin: ②④⑬⑮

Model: 851C2N-0005
Manufacturer · Distributor: Toko Co.

- **Overview of 851C2N-0005**
  [External view units in inches]



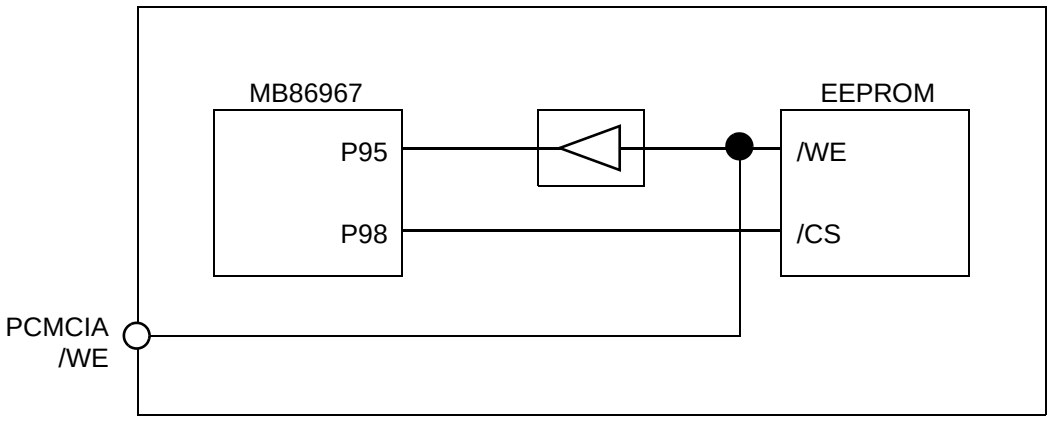
[Internal circuit]



		MB86965B	MB86964-R	MB86967	Notes
Package		QFP160	SQFP100	SQFP100	
Supply voltage		5 V ± 5%	5 V ± 5%	5 V ± 5%	
Operation mode		Jumperless +ISA I/F Jumper+E²PROM+ISA I/F Jumper+PROM+ISA I/F General-purpose I/F	General-purpose bus I/F	PC card I/F General-purpose bus I/F Jumperless +ISA I/F Jumper + E²PROM + ISA I/F	
Network interface		TP/AUI	TP/AUI	TP	
Max buffer memory size		64 Kbytes	32 Kbytes	32 Kbytes	
Buffer memory bus width		8/16 bits	8 bits	8 bits	
ROM interface for boot program		Internal	No	No	
ROM type for boot program		PROM or Flash ROM			Writable by selecting Flash ROM
LED for monitoring network status	ISA bus mode	Test for transmit, receive, collision, link		Test for transmit, receive, collision, link	
	PC card mode			Test for transmit, receive, collision, link	
	General-purpose bus mode	Test for transmit, receive, collision, link	Test for transmit, receive, collision, link	Test for transmit, receive, collision, link	
Device ID		1, 1	0, 1	1, 0	DLCR7 bit 6, 7
Internal register	ISA bus mode	DLCR 0 to 15, MAR 8 to 15, BMPR 8, 10 to 19, IDRB 0 to 7		DLCR 0 to 15, MAR 8 to 15, BMPR 8, 10 to 19, (IDRB 0 to 7)*	*: Change name to RES0 to 7
	PC card mode			DLCR 0 to 15, MAR 8 to 15, BMPR 8, 10 to 15, CARDCR, (ID), CCR 0 to 3	
	General-purpose bus mode	DLCR 0 to 15, MAR 8 to 15, BMPR 8, 10 to 15	DLCR 0 to 15, MAR 8 to 15, BMPR 8, 10 to 15	DLCR 0 to 15, MAR 8 to 15, BMPR 8, 10 to 15	
Full duplex operation		Yes	No	Yes	DLCR4 bit 0
Jumperless mode default setting		External reset or writing IDRB0 to 7		External reset or writing IDRB 0-7	
Shutdown mode		No	No	Yes (crystal oscillation stop)	BMPR14 bit 4 × DLCR7 bit 5
TP transceiver filter		Internal	Internal	External	
Winding ratio for TP transmit pulse transformer		1:$\sqrt{2}$	1:$\sqrt{2}$	1 : 1	
Remote signalling		Yes	Yes	No	BMPR14 bit 5, 7 BMPR15 bit 4, 5, 7
100 Ω/150 Ω termination resistor		Selectable	Selectable	100 Ω	BMPR13 bit 2
Deleting receive long packet		No	No	Yes	BMPR12 bit 3
Lower Squelch		Yes	Yes	No	BMPR13 bit 6

■ ERRATA SHEET

Category	Power supply OFF sequence in PC card mode,.
Summary	Whin the CIS area is prepared with an EEPROM device, MB86967 mulfunctions with mis-writing occasionally for the CIS area (This error depends on the type of PC.)
Recommendation	Please insert the OR-gate between MB86967 and EEPROM. As a result. even if Pin 95 is driven to Low, it does not influence EEPROM.

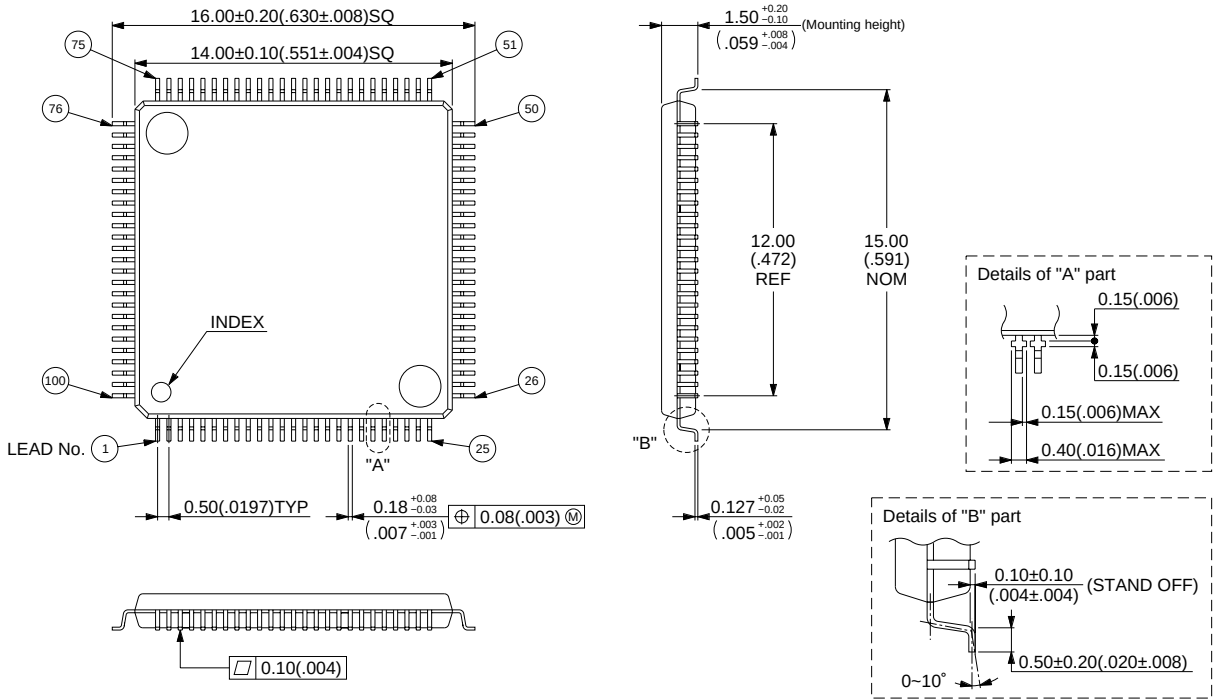


■ ORDERING INFORMATION

Part number	Package	Remarks
MB86967PFV	100-pin Plastic LQFP (FPT-100P-M05)	

■ PACKAGE DIMENSION

100-pin Plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches)

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