# MIC4123/4124/4125

## Dual 3A-Peak Low-Side MOSFET Driver

## Bipolar/CMOS/DMOS Process

## General Description

The MIC4123/4124/4125 family are highly reliable BiCMOS/DMOS buffer/driver/MOSFET drivers. They are higher output current versions of the MIC4126/4127/4128, which are improved versions of the MIC4426/4427/4428. All three families are pin-compatible. The MIC4123/4124/4125 drivers are capable of giving reliable service in more demanding electrical environments than their predecessors. They will not latch under any conditions within their power and voltage ratings. They can survive up to 5V of noise spiking, of either polarity, on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (either polarity) forced back into their outputs.

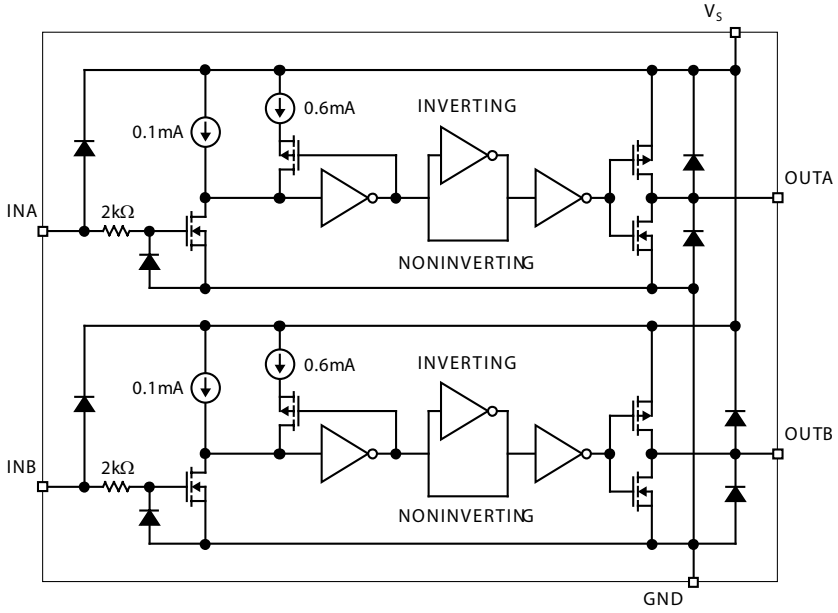
The MIC4123/4124/4125 series drivers are easier to use, more flexible in operation, and more forgiving than other CMOS or bipolar drivers currently available. Their BiCMOS/DMOS construction dissipates minimum power and provides rail-to-rail voltage swings.

Primarily intended for driving power MOSFETs, the MIC4123/4124/4125 drivers are suitable for driving other loads (capacitive, resistive, or inductive) which require low-impedance, high peak currents, and fast switching times. Heavily loaded clock lines, coaxial cables, or piezoelectric transducers are some examples. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

## Features

- Reliable, low-power bipolar/CMOS/DMOS construction
- Latch-up protected to >200mA reverse current
- Logic input withstands swing to –5V
- High 3A-peak output current
- Wide 4.5V to 20V operating range
- Drives 1800pF capacitance in 25ns
- Short <50ns typical delay time
- Delay times consistent with in supply voltage change
- Matched rise and fall times
- TTL logic input independent of supply voltage
- Low equivalent 6pF input capacitance
- Low supply current
  - 3.5mA with logic-1 input
  - 350µA with logic-0 input
- Low 2.3Ω typical output impedance
- Output voltage swings within 25mV of ground or $V_S$.
- ‘426/7/8-, ‘1426/7/8-, ‘4426/7/8-compatible pinout
- Inverting, noninverting, and differential configurations
- Exposed backside pad packaging reduces heat
  - ePAD SOIC-8L ($\theta_{JA}$ = 58°C/W)
  - 4mm x 4mm MLF™-8L ($\theta_{JA}$ = 45°C/W)

## Functional Diagram




Integrated Component Count:
4 Resistors
4 Capacitors
52 Transistors

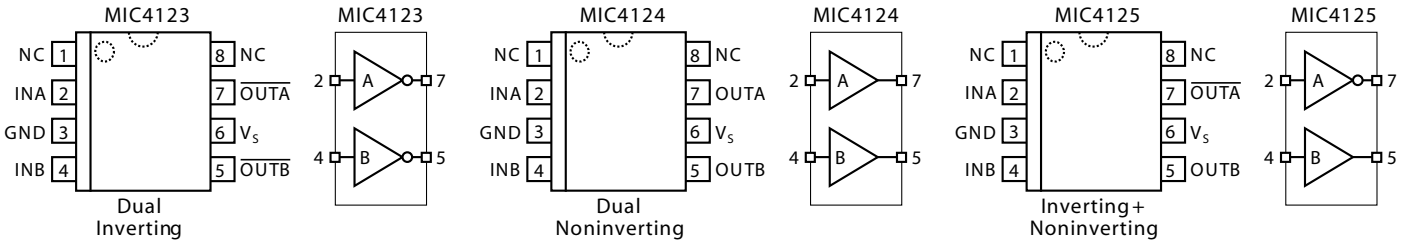
**Ground Unused Inputs**

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## Ordering Information

| Part Number | Package | Configuration | Lead Finish |
|---|---|---|---|
| MIC4123YME | EPAD 8-Lead SOIC | Dual Inverting | Pb-Free |
| MIC4123YML | 8-Lead MLF | Dual Inverting | Pb-Free |
| MIC4124YME | EPAD 8-Lead SOIC | Dual Non-Inverting | Pb-Free |
| MIC4124YML | 8-Lead MLF | Dual Non-Inverting | Pb-Free |
| MIC4125YME | EPAD 8-Lead SOIC | Inverting + Non-Inverting | Pb-Free |
| MIC4125YML | 8-Lead MLF | Inverting + Non-Inverting | Pb-Free |

## Pin & Driver Configuration




## Pin Description

| Pin Number | Pin Name | Function |
|---|---|---|
| 2 / 4 | INA / B | Control Input |
| 3 | GND | Ground: Duplicate pins must be externally connected together |
| 6 | $V_S$ | Supply Input: Duplicate pins must be externally connected together |
| 7 / 5 | OUTA / B | Output: Duplicate pins must be externally connected together |
| 1, 8 | NC | Not connected |
| EP | GND | Ground: Backside Pad |

## Absolute Maximum Ratings (Note 1)

Supply Voltage ..... +24V
Input Voltage ..... $V_S$ + 0.3V to GND – 5V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (10 sec.) ..... 300°C
ESD Susceptability, **Note 3**

## Operating Ratings (Note 2)

Supply Voltage ($V_S$) ..... +4.5V to +20V
Junction Temperature Range ..... –40°C to 125°C
Package Thermal Resistance
4mm X 4mm MLF $\theta_{JA}$ ..... 45°C/W
EPAD SOIC-8L $\theta_{JA}$ ..... 58°C/W

## MIC4123/4124/4125 Electrical Characteristics (Note 4)

4.5V ≤ $V_S$ ≤ 20V; $T_A$ = 25°C, **bold** values indicate –40°C ≤ $T_J$ ≤ +125°C; unless noted. Input Voltage slew rate >2.5V/µs.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| **$V_{IH}$** | **Logic 1 Input Voltage** | | **2.4** | 1.5 | | V |
| $V_{IL}$ | Logic 0 Input Voltage | | | 1.3 | **0.8** | V |
| $I_{IN}$ | Input Current | 0V ≤ $V_{IN}$ ≤ $V_S$ | –1<br>**–10** | | 1<br>**10** | µA<br>µA |
| **Output** | | | | | | |
| $V_{OH}$ | High Output Voltage | $I_{OUT}$ = 100µA | **$V_S$–0.025** | | | V |
| $V_{OL}$ | Low Output Voltage | $I_{OUT}$ = –100µA | | | **0.025** | **V** |
| $R_O$ | Output Resistance HI State | $I_{OUT}$ = 10mA, $V_S$ = 20V | | 2.3 | 5 | Ω |
| | | | | | **8** | **Ω** |
| | Output Resistance LO State | $I_{OUT}$ = 10mA, $V_S$ = 20V | | 2.2 | 5 | Ω |
| | | | | | **8** | Ω |
| $I_{PK}$ | Peak Output Current | | | 3 | | A |
| I | Latch-Up Protection Withstand Reverse Current | | >200 | | | mA |
| **Switching Time** | | | | | | |
| $t_R$ | Rise Time | test Figure 1, $C_L$ = 1800pF | | 11 | 35<br>**60** | ns<br>ns |
| $t_F$ | Fall Time | test Figure 1, $C_L$ = 1800pF | | 11 | 35<br>**60** | ns<br>ns |
| $t_{D1}$ | Delay TIme | test Ffigure 1, $C_L$ = 1800pF | | 44 | 75<br>**100** | ns<br>ns |
| $t_{D2}$ | Delay Time | test Figure 1, $C_L$ = 1800pF | | 59 | 75<br>**100** | ns<br>ns |
| **Power Supply** | | | | | | |
| $I_S$ | Power Supply Current | $V_{IN}$ = 3.0V (both inputs) | | 1.5 | 2.5<br>**3.5** | mA<br>mA |
| $I_S$ | Power Supply Current | $V_{IN}$ = 0.0V (both inputs) | | 0.15 | 0.25<br>**0.3** | mA<br>mA |

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating rating.

**Note 3.** Devices are ESD sensitive. Handling precautions recommended. ESD tested to human body model, 1.5k in series with 100pF.

**Note 4.** Specification for packaged product only.

## Test Circuit

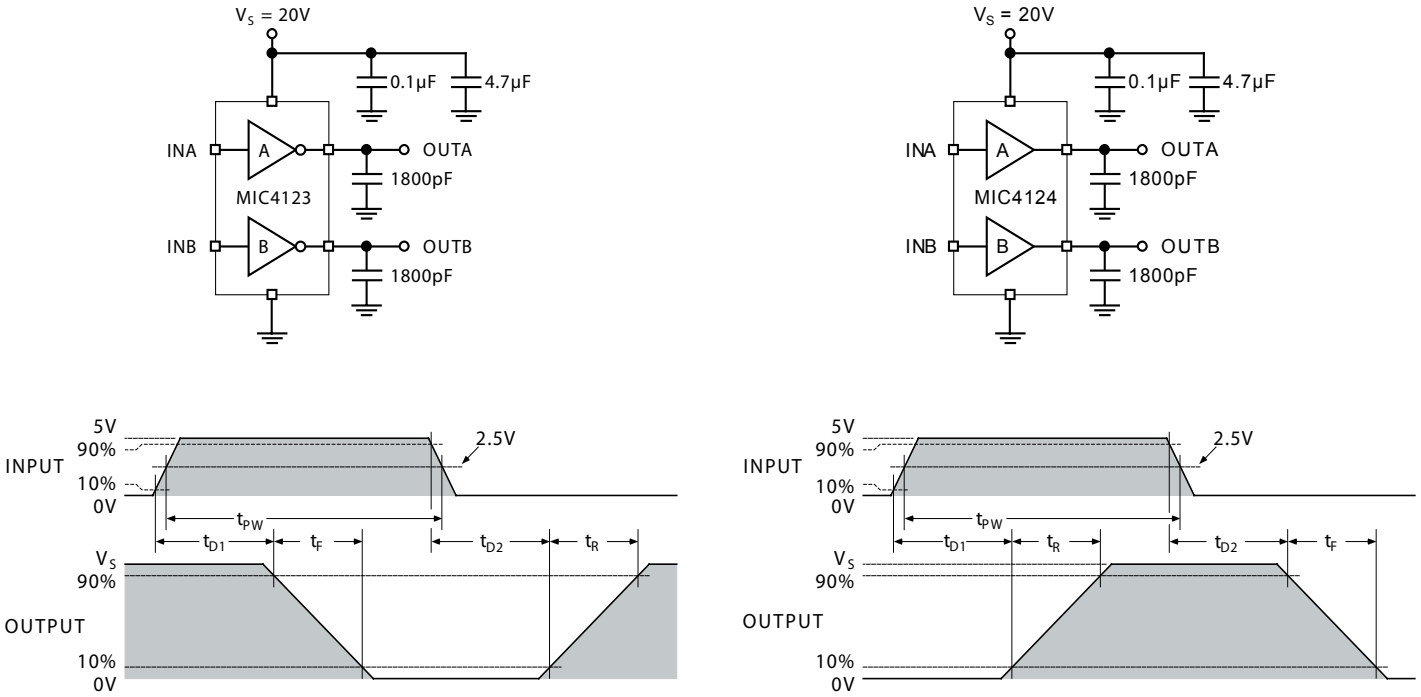
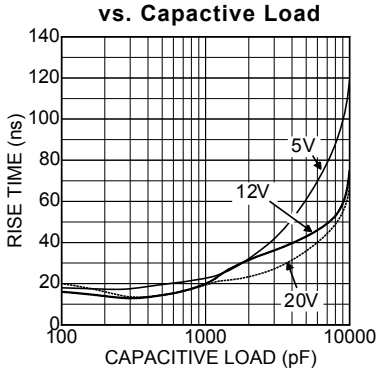



**Figure 1a. Inverting Driver Switching Time**

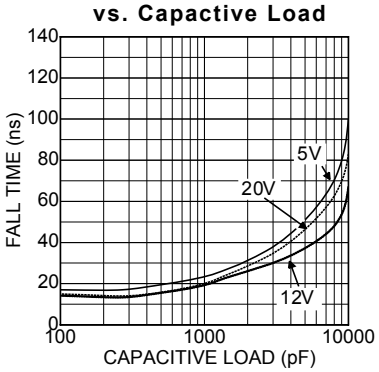
**Figure 1b. Non-inverting Driver Switching Time**

## Typical Characteristic Curves

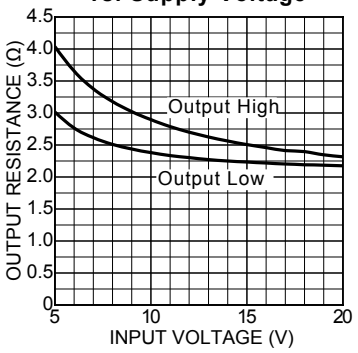
**Rise Time vs. Capactive Load**



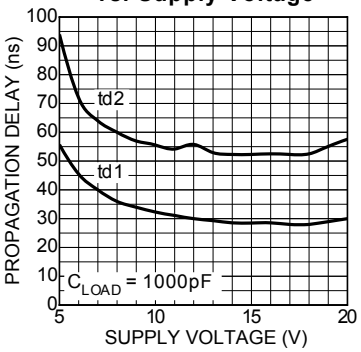

**Fall Time vs. Capactive Load**



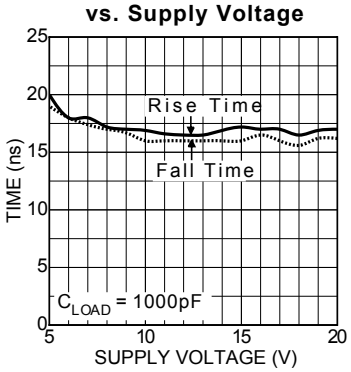

**Output Resistance vs. Supply Voltage**




**Propagation Delay vs. Supply Voltage**




**Rise and Fall Time vs. Supply Voltage**



## Application Information

Although the MIC4123/24/25 drivers have been specifically constructed to operate reliably under any practical circumstances, there are nonetheless details of usage which will provide better operation of the device.

### Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 2000pF from 0 to 15 volts in 20ns requires a constant current of 1.5A. In practice, the charging current is not constant, and will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that as far as the driver is concerned, the system power supply, as seen by the driver, must have a **VERY** low impedance.

As a practical matter, this means that the power supply bus must be capacitively bypassed at the driver with at least 100X the load capacitance in order to achieve optimum driving speed. It also implies that the bypassing capacitor must have very low internal inductance and resistance at all frequencies of interest. Generally, this means using two capacitors, one a high-performance low ESR film, the other a low internal resistance ceramic, as together the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. PLEASE NOTE that many film capacitors can be sufficiently inductive as to be useless for this service. Likewise, many multilayer ceramic capacitors have unacceptably high internal resistance. Use capacitors intended for high pulse current service (in-house we use WIMA™ film capacitors and AVX Ramguard™ ceramics; several other manufacturers of equivalent devices also exist). The high pulse current demands of capacitive drivers also mean that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PCB land inductance from nullifying what you are trying to accomplish. For optimum results the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 2.5cm or less.

Bypass capacitance, and its close mounting to the driver serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large Δ I) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. ***Good bypassing practice is essential to proper operation of high speed driver ICs.***

### Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load ON. Eventually (except in rare circumstances) it is also necessary to turn the load OFF. This requires attention to the ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: The adequacy of the grounding available for the driver, and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

The E-Pad and MLF packages have an exposed pad under the package. It's important for good thermal performance that this pad is connected to a ground plane.

Best practice for a ground path is obviously a well laid out ground plane. However, this is not always practical, and a poorly-laid out ground plane can be worse than none. Attention to the paths taken by return currents even in a ground plane is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to whatever is driving it should all be as low in resistance and inductance as possible. Of the three paths, the ground lead from the driver to the logic driving it is most sensitive to resistance or inductance, and ground current from the load are what is most likely to cause disruption. Thus, these ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

To illustrate what can happen, consider the following: The inductance of a 2cm long land, 1.59mm (0.062") wide on a PCB with no ground plane is approximately 45nH. Assuming a dI/dt of 0.3A/ns (which will allow a current of 3A to flow after 10ns, and is thus slightly slow for our purposes) a voltage of 13.5 Volts will develop along this land in response to our postulated $\Delta I$. For a 1cm land, (approximately 15nH) 4.5 Volts is developed. Either way, anyone using TTL-level input signals to the driver will find that the response of their driver has been seriously degraded by a common ground path for input to and output from the driver of the given dimensions. Note that this is before accounting for any resistive drops in the circuit. The resistive drop in a 1.59mm (0.062") land of 2oz. Copper carrying 3A will be about 4mV/cm (10mV/in) at DC, and the resistance will increase with frequency as skin effect comes into play.

The problem is most obvious in inverting drivers where the input and output currents are in phase so that any attempt to raise the driver's input voltage (in order to turn the driver's load off) is countered by the voltage developed on the common ground path as the driver attempts to do what it was supposed to. It takes very little common ground path, under these circumstances, to alter circuit operation drastically.

### Output Lead Inductance

The same descriptions just given for PCB land inductance apply equally well for the output leads from a driver to its load, except that commonly the load is located much further away from the driver than the driver's ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4cm (2") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are at least an order of magnitude lower than the impedance of common coax, using coax is seldom a cost-effective solution. A twisted pair works about as well, is generally lower in cost, and allows use of a

wider variety of connectors. The second wire of the twisted pair should carry common from as close as possible to the ground pin of the driver directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver, as this will not provide a complete current path for either driver. Likewise, do not use a twisted triad with two outputs and a common return unless both of the loads to be driver are mounted extremely close to each other, and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines: i.e., minimize sharp bends, or narrowings in the land, as these will cause ringing. For a rough estimate, on a 1.59mm (0.062") thick G-10 PCB a pair of opposing lands each 2.36mm (0.093") wide translates to a characteristic impedance of about 50Ω. Half that width suffices on a 0.787mm (0.031") thick board. For accurate impedance matching with a MIC4123/24/25 driver, on a 1.59mm (0.062") board a land width of 42.75mm (1.683") would be required, due to the low impedance of the driver and (usually) its load. This is obviously impractical under most circumstances. Generally the tradeoff point between lands and wires comes when lands narrower than 3.18mm (0.125") would be required on a 1.59mm (0.062") board.

To obtain minimum delay between the driver and the load, it is considered best to locate the driver as close as possible to the load (using adequate bypassing). Using matching transformers at both ends of a piece of coax, or several matched lengths of coax between the driver and the load, works in theory, but is not optimum.

**Driving at Controlled Rates**

Occasionally there are situations where a controlled rise or fall time (which may be considerably longer than the normal rise or fall time of the driver's output) is desired for a load. In such cases it is still prudent to employ best possible practice in terms of bypassing, grounding and PCB layout, and then reduce the switching speed of the load (NOT the driver) by adding a noninductive series resistor of appropriate value between the output of the driver and the load. For situations where only rise or only fall should be slowed, the resistor can be paralleled with a fast diode so that switching in the other direction remains fast. Due to the Schmitt-trigger action of the driver's input it is not possible to slow the rate of rise (or fall) of the driver's input signal to achieve slowing of the output.

**Input Stage**

The input stage of the MIC4123/24/25 consists of a single-MOSFET class A stage with an input capacitance of <8pF. This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is a –2mA current source. Thus, the quiescent current drawn by the driver varies, depending upon the logic state of the input.

Following the input stage is a buffer stage which provides ~400mV of hysteresis for the input, to prevent oscillations when slowly-changing input signals are used or when noise is present on the input. Input voltage switching threshold is approximately 1.5V which makes the driver directly compatible with TTL signals, or with CMOS powered from any supply voltage between 3V and 15V.

The MIC4123/24/25 drivers can also be driven directly by the MIC9130, MIC3808, MIC38C42, and similar switch mode power supply ICs. By relocating the main switch drive function into the driver rather than using the somewhat limited drive capabilities of a PWM IC. The PWM IC runs cooler, which generally improves its performance and longevity, and the main switches switch faster, which reduces switching losses and increase system efficiency.

The input protection circuitry of the MIC4123/24/25, in addition to providing 2kV or more of ESD protection, also works to prevent latchup or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed or rendered inoperable until the power supply is cycled OFF and ON. The MIC4123/24/25 drivers have been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC. Because the excess voltage is simply conducted to the power terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30mA can be conducted through the driver from the input terminal to its power supply terminal. This may overload the output of whatever is driving the driver, and may cause other devices that share the driver's power supply, as well as the driver, to operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the drivers. $T_{D2}$, for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver so that line spiking and ringing are minimized, will always result in faster and more reliable operation of the device, leave less EMI to be filtered elsewhere, be less stressful to other components in the circuit, and leave less chance of unintended modes of operation.

**Power Dissipation**

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 series and 74Cxxx have outputs which can only source or sink a few milliamps of current, and even shorting the output of the device to ground or $V_{CC}$ may not damage the device. CMOS drivers, on the other hand, are intended to source or sink several Amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver ICs can easily be exceeded when driving large loads at high frequencies. Care must therefore be paid to device dissipation when operating in this domain.

The Supply Current vs Frequency and Supply Current vs Load characteristic curves furnished with this data sheet aid in estimating power dissipation in the driver. Operating frequency, power supply voltage, and load all affect power dissipation.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin E-Pas SOIC package, from the datasheet, is 58°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 2.16W.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load power dissipation ($P_L$)
- Quiescent power dissipation ($P_Q$)
- Transition power dissipation ($P_T$)

Calculation of load power dissipation differs depending upon whether the load is capacitive, resistive or inductive.

### *Resistive Load Power Dissipation*

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load
$R_O$ = the output resistance of the driver when the output is high, at the power supply voltage used (See characteristic curves)
D = fraction of time the load is conducting (duty cycle)

### *Capacitive Load Power Dissipation*

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = f\ C\ (V_S)^2$$

where:

f = Operating Frequency
C = Load Capacitance
$V_S$ = Driver Supply Voltage

### *Inductive Load Power Dissipation*

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the $R_O$ required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending upon how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I\ V_D\ (1 - D)$$

where $V_D$ is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce $P_L$

$$P_L = P_{L1} + P_{L2}$$

### *Quiescent Power Dissipation*

Quiescent power dissipation ($P_Q$, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2mA; a logic high will result in a current drain of ≤2.0mA. Quiescent power can therefore be found from:

$$P_Q = V_S\ [D\ I_H + (1 - D)\ I_L]$$

where:

$I_H$ = quiescent current with input high
$I_L$ = quiescent current with input low
D = fraction of time input is high (duty cycle)
$V_S$ = power supply voltage

### *Transition Power Dissipation*

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from $V_S$ to ground. The transition power dissipation is approximately:

$$P_T = f\ V_S\ (A \bullet s)$$

where (A•s) is a time-current factor derived from Figure 2.

Total power (PD) then, as previously described is just

$$P_D = P_L + P_Q + P_T$$

Examples show the relative magnitude for each term.

EXAMPLE 1: A MIC4123 operating on a 12V supply driving two capacitive loads of 3000pF each, operating at 250kHz, with a duty cycle of 50%, in a maximum ambient of 60°C.

First calculate load power loss:

$$P_L = f \times C \times (V_S)^2$$
$$P_L = 250{,}000 \times (3 \times 10^{-9} + 3 \times 10^{-9}) \times 12^2$$
$$= 0.2160W$$

Then transition power loss:

$$P_T = f \times V_S \times (A \bullet s)$$
$$= 250{,}000 \bullet 12 \bullet 2.2 \times 10^{-9} = 6.6mW$$

Then quiescent power loss:

$P_Q = V_S \times [D \times I_H + (1 - D) \times I_L]$
$= 12 \times [(0.5 \times 0.0035) + (0.5 \times 0.0003)]$
$= 0.0228W$

Total power dissipation, then, is:

$P_D = 0.2160 + 0.0066 + 0.0228$
$= 0.2454W$

Assuming an E-Pad SOIC package, with an $\theta_{JA}$ of 58°C/W, this will result in the junction running at:

$0.2454 \times 58 = 14.2°C$

above ambient, which, given a maximum ambient temperature of 60°C, will result in a maximum junction temperature of 89.4°C.

EXAMPLE 2: A MIC4124 operating on a 15V input, with one driver driving a 50Ω resistive load at 1MHz, with a duty cycle of 67%, and the other driver quiescent, in a maximum ambient temperature of 40°C:

$P_L = I^2 \times R_O \times D$

First, $I_O$ must be determined.

$I_O = V_S / (R_O + R_{LOAD})$

Given $R_O$ from the characteristic curves then,

$I_O = 15 / (3.3 + 50)$

$I_O = 0.281A$

and:

$P_L = (0.281)^2 \times 3.3 \times 0.67$
$= 0.174W$
$P_T = F \times V_S \times (A \cdot s)/2$

(because only one side is operating)

$= (1{,}000{,}000 \times 15 \times 3.3 \times 10^{-9}) / 2$
$= 0.025 W$

and:

$P_Q = 15 \times [(0.67 \times 0.00125) + (0.33 \times 0.000125) + (1 \times 0.000125)]$

(this assumes that the unused side of the driver has its input grounded, which is more efficient)

$= 0.015W$

then:

$P_D = 0.174 + 0.025 + 0.0150$
$= 0.213W$

In a MLF with an $\theta_{JA}$ of 60°C/W, this amount of power results in a junction temperature given the maximum 40°C ambient of:

$(0.213 \times 100) + 40 = 52.8°C$

The actual junction temperature will be lower than calculated both because duty cycle is less than 100% and because the graph lists $R_{DS(on)}$ at a $T_J$ of 125°C and the $R_{DS(on)}$ at 52.8°C $T_J$ will be somewhat lower.

***Definitions***

$C_L$ = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz.

$I_H$ = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

$I_L$ = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

$I_D$ = Output current from a driver in Amps.

$P_D$ = Total power dissipated in a driver in Watts.

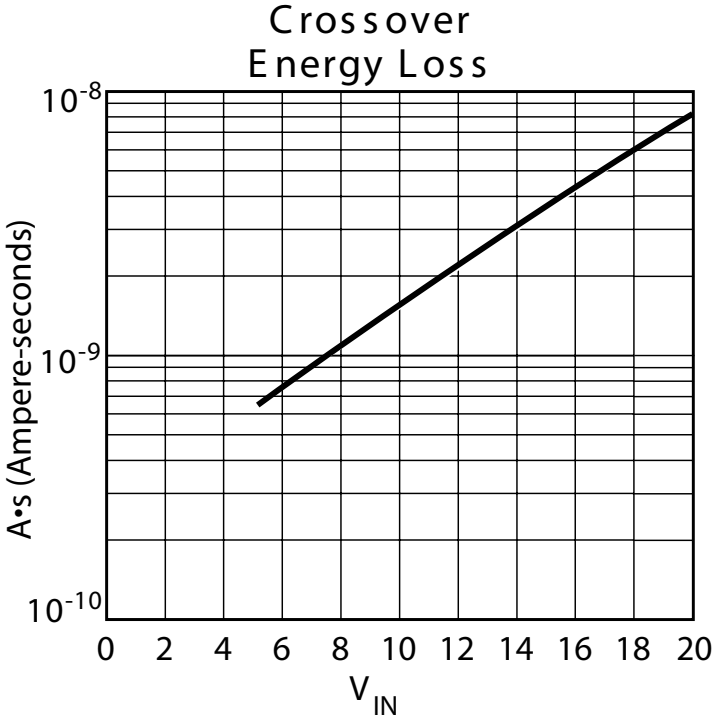
$P_L$ = Power dissipated in the driver due to the driver's load in Watts.

$P_Q$ = Power dissipated in a quiescent driver in Watts.

$P_T$ = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in the graph on the following page in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency to find Watts).

$R_O$ = Output resistance of a driver in Ohms.

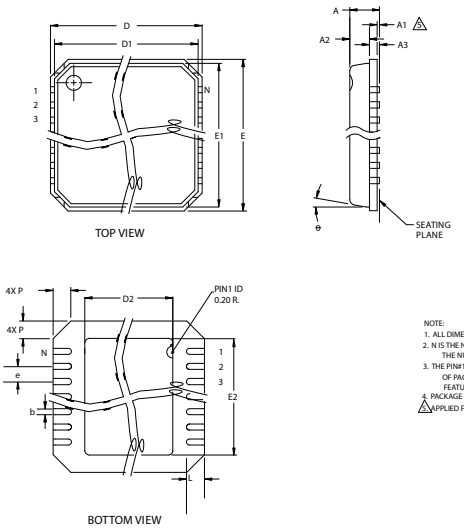
$V_S$ = Power supply voltage to the IC in Volts.




**NOTE:** THE VALUES ON THIS GRAPH REPRESENT THE LOSS SEEN BY BOTH DRIVERS IN A PACKAGE DURING ONE COMPLETE CYCLE. FOR A SINGLE DRIVER DIVIDE THE STATED VALUES BY 2. FOR A SINGLE TRANSITION OF A SINGLE DRIVER, DIVIDE THE STATED VALUE BY 4.

**Figure 2.**

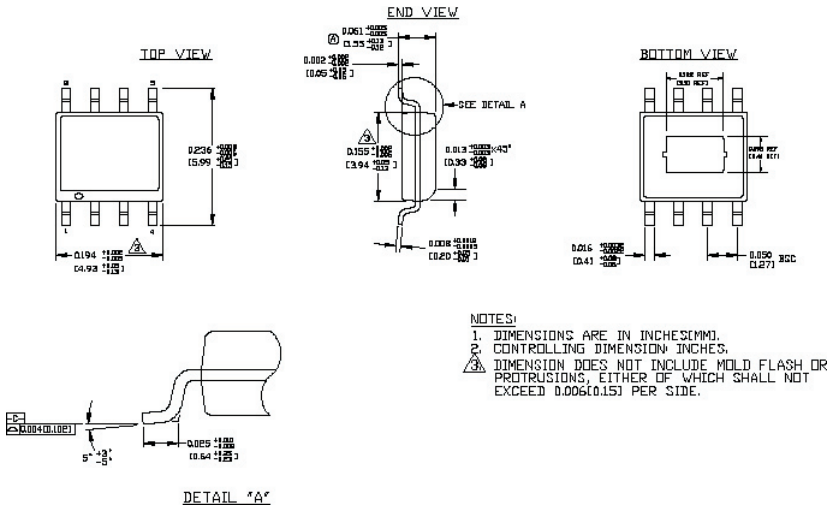
## Package Information




| DIMENSION (mm) | | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | 0.85 | 1.00 |
| A1 | 0.00 | 0.01 | 0.05 |
| A2 | - | 0.65 | 0.80 |
| A3 | | 0.20 REF. | |
| D | | 4.00 BSC | |
| D1 | | 3.75 BSC | |
| D2 | 2.25 | 2.40 | 2.55 |
| E | | 4.00 BSC | |
| E1 | | 3.75 BSC | |
| E2 | 3.05 | 3.20 | 3.35 |
| θ | | | 12° |
| P | 0.24 | 0.42 | 0.60 |
| e | | 0.65 BSC | |
| N | | 8 | |
| L | 0.30 | 0.45 | 0.60 |
| b | 0.23 | 0.28 | 0.35 |

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE NUMBER OF TERMINALS. THE NUMBER OF TERMINALS PER SIDE IS N/4.
3. THE PIN#1 IDENTIFIRE MUST BE EXISTED ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. PACKAGE WARPAGE MAX 0.05mm.
⚠ APPLIED FOR EXPOSED PAD AND TERMINALS.

**8-Pin 4x4 MLF (ML)**




**8-Pin Exposed Pad SOIC (ME)**

**MICREL INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

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