Features

General

- High-performance, Low-power secureAVR® Core RISC Architecture
  - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 6000V on contact pins, ± 2000V on RF pins
- Operating Ranges: from 2.7V to 5.5V
- Compliant with EMV 2000 Specifications; PC Industry Compatible
- Power-saving Wait and Very Low-power Stop Modes
- Power-up Detection
- Available in Wafers, Modules, Contactless Module or Inlay and Industry-standard Packages
- Compliant with VISA / Master Card PayPassT Specifications

Contactless Mode

- Contactless Interface Controller (CIC) with Full Support for ISO/IEC 14443 Type A and B Protocol
- Supply Voltage Clamp and Regulation
- Full-bridge Power Rectification
- On-chip Tuning Capacitance: 20pF or 120pF
- 13.56 MHz Clock Extraction
- 6.78 MHz Internal Bus Frequency
- Reader-to-card:
  - ISO/IEC Type A: 100% ASK Modulation and Modified Miller Bit Coding
  - ISO/IEC Type B: 10% ASK Modulation and NRZ Bit Coding
  - Baud Rates: 106Kbps, 212Kbps and 424Kbps
- Card-to-reader:
  - ISO/IEC Type A: Generation of 847.5KHz Subcarrier with OOK Modulation and Manchester Bit Coding
  - ISO/IEC Type B: Modulation of Incoming RF Carrier by Resistive Load Switching / Generation of 847.5KHz Subcarrier with BPSK Modulation / NRZ data Encoding
  - Baud Rates: 106Kbps, 212Kbps and 424Kbps

Memory

- 64K Bytes of ROM Program Memory
- 8K Bytes of EEPROM, Including 64 OTP Bytes and 192 Bit-addressable Bytes
  - 1 to 64-byte Program/Erase
  - 2 ms Program, 2 ms Erase
  - Endurance: 500,000 Write/Erase Cycles at 25°C
  - 10 Years Data Retention
  - EEPROM Erase Only Mode
  - Write EEPROM without or with Auto-Erase
- 1K Bytes of RAM + 256 Bytes of DMA dedicated RAM

Peripherals

- One ISO 7816 controller
  - Up to 625 kbps at 5 MHz
  - Compliant with T = 0 and T = 1 Protocols
- One I/O Port (Can be Configured to Support 7816-3)
- Programmable Internal Oscillator (Up to 20 MHz for internal CPU Clock)
- Three 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 8-vector Interrupt Controller
- Hardware DES and Triple DES DPA, SPA and DEMA Resistant
- Checksum Accelerator
- CRC 16 & 32 Engine (Compliant with ISO/IEC 3309)
- DMA Controller (Used to Speed-Up Data Transfers when Communicating via the Contactless Interface)

Secure Microcontrollers for Smart Cards

AT90SC6408RFT

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Note: This a summary and preliminary document. For more information, please contact your local Atmel sales office.

Security

- **Dedicated Hardware for Protection Against SPA/DPA/DEMA Attacks**
- **Advanced Protection Against Physical Attack, Including Active Shield**
- **Environmental Protection Systems**
- **Voltage Monitor**
- **Frequency Monitor**
- **Temperature Monitor**
- **Light Protection**
- **Secure Memory Management/Access Protection (Supervisor Mode)**
- **Security Certification Targeted: Common Criteria EAL4+, VISA, CAST**

Development Tools

- **Voyager Emulation Platform (ATV4 Advanced) to Support Software Development**
- **IAR Embedded Workbench® V3.20c Debugger or Atmel's AVR Studio® Version 4.07 or Above**
- **Software Libraries and Application Notes**

Description

The AT90SC6408RFT is a low-power, high-performance, 8-/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR enhanced RISC architecture and with a dual interface (contact+contactless). The contactless interface fully supports the ISO/IEC 14443 Type A and Type B standard.

By executing powerful instructions in a single clock cycle, the AT90SC6408RFT achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The AT90SC6408RFT uses the secureAVR architecture that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data as well as a number of new functional and security features.

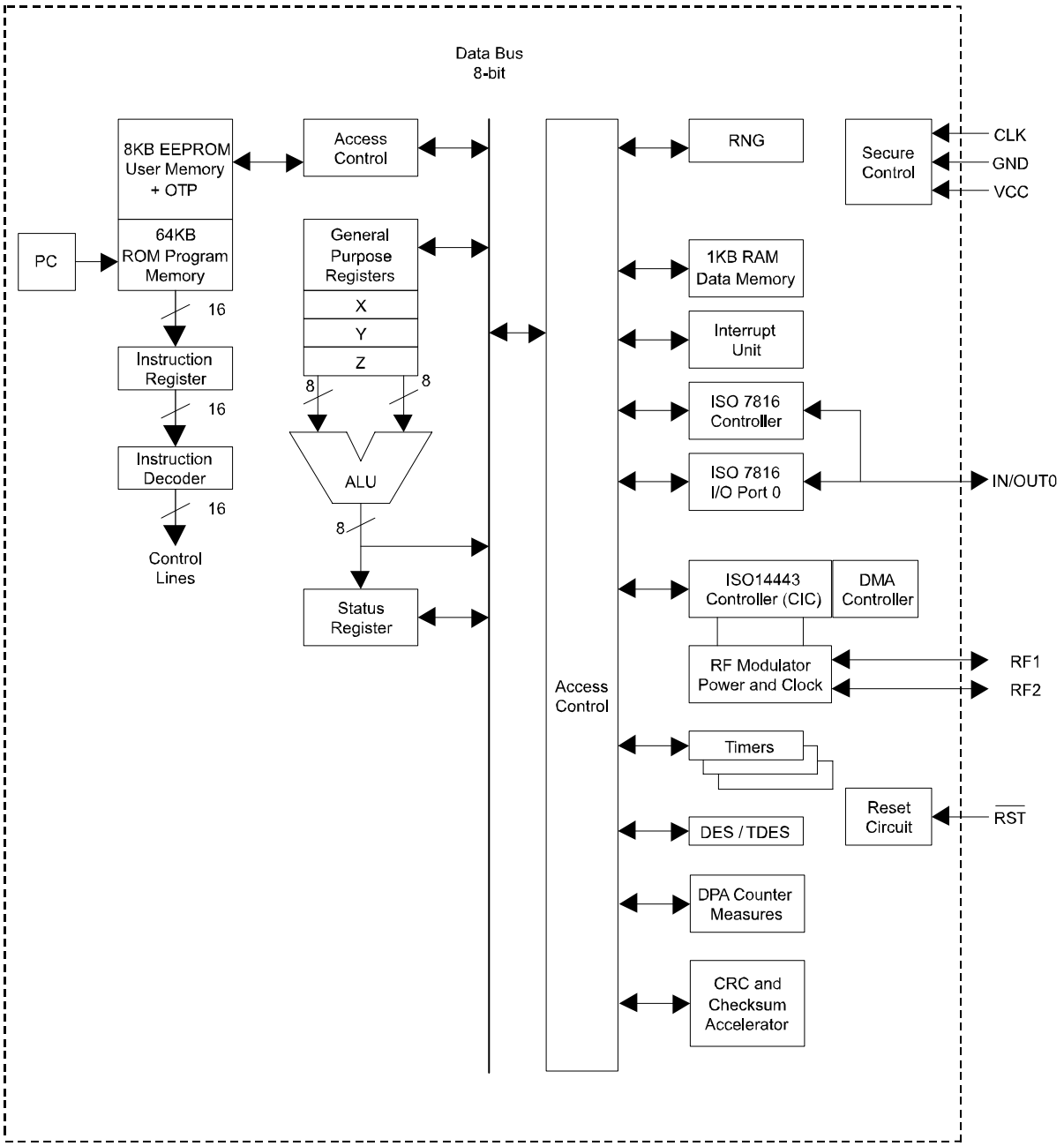
The AT90SC6408RFT features 8K bytes of high-performance EEPROM (fast erase/write time, high endurance). The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system.

Additional security features include power, frequency and temperature protection logic, logical scrambling on program data and addresses, power analysis countermeasures, and memory accesses controlled by a supervisor mode.

This product is specifically designed for Dual Interface Smart Cards and targets, Banking, Transportation, Access Control and e-identity applications.

A block diagram of the AT90SC6408RFT is shown in Figure 1.

Figure 1. AT90SC6408RFT Contact / Contactless secureAVR Enhanced Architecture



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