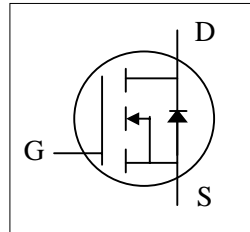
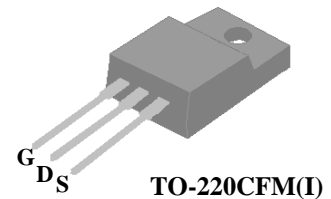




- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristics
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	600V
$R_{DS(ON)}$	5 Ω
I_D	2A



Description

AP4002 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.

Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^4$	2	A
I_{DM}	Pulsed Drain Current ¹	8	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	20	W
	Linear Derating Factor	0.16	W/ $^\circ\text{C}$
E_{AS}	Single Pulse Avalanche Energy ²	20	mJ
I_{AR}	Avalanche Current	2	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	6.25	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ\text{C}/\text{W}$



Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =1mA	600	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ³	V _{GS} =10V, I _D =1.0A	-	-	5	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =2.0A	-	1.5	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =600V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±30V, V _{DS} =0V	-	-	±1	uA
Q _g	Total Gate Charge ³	I _D =2A	-	12	19	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	2	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	5.5	-	nC
t _{d(on)}	Turn-on Delay Time ³	V _{DD} =200V	-	10	-	ns
t _r	Rise Time	I _D =1A	-	12	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =50Ω	-	52	-	ns
t _f	Fall Time	V _{GS} =10V	-	19	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	375	600	pF
C _{oss}	Output Capacitance	V _{DS} =10V	-	170	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	45	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ³	T _j =25°C, I _S =2A, V _{GS} =0V	-	-	1.5	V
t _{rr}	Reverse Recovery Time ³	I _S =2A, V _{GS} =0V,	-	340	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	2.2	-	uC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Starting T_j=25°C , V_{DD}=50V , L=10mH , R_G=25Ω
- 3.Pulse test
- 4.Ensure that the junction temperature does not exceed T_{Jmax}.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

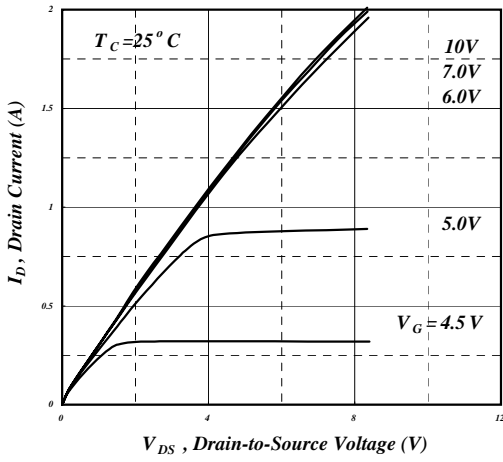


Fig 1. Typical Output Characteristics

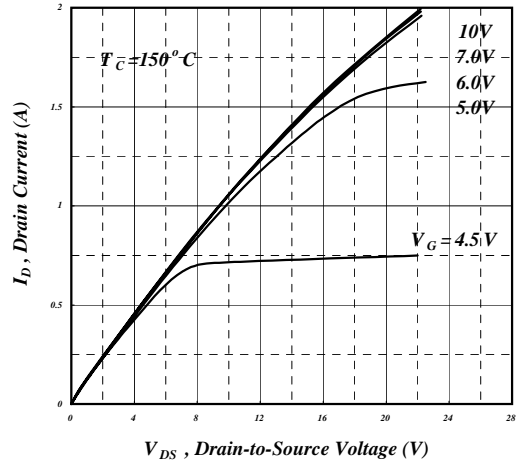


Fig 2. Typical Output Characteristics

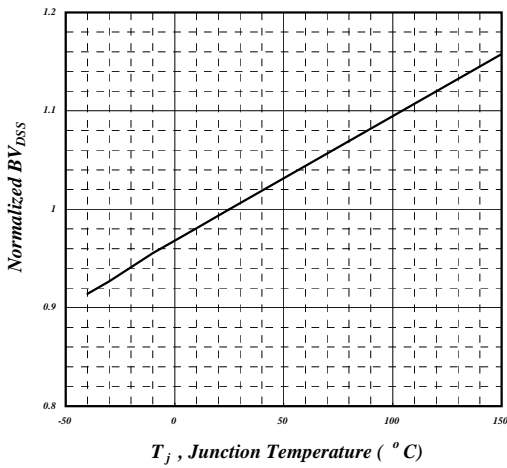


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

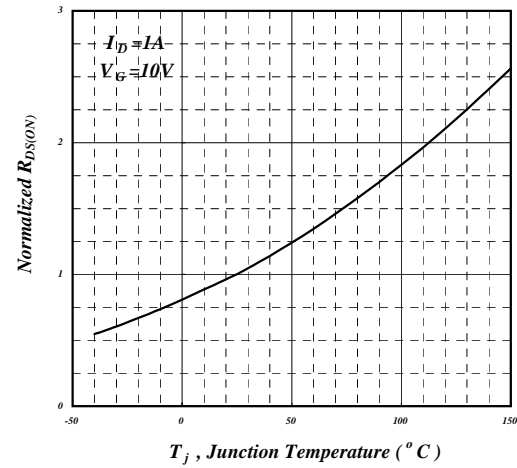


Fig 4. Normalized On-Resistance v.s. Junction Temperature

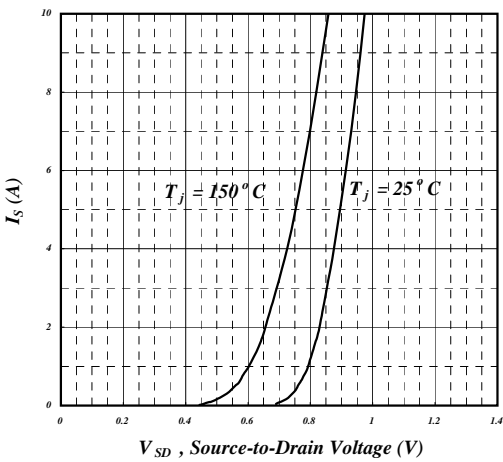


Fig 5. Forward Characteristic of Reverse Diode

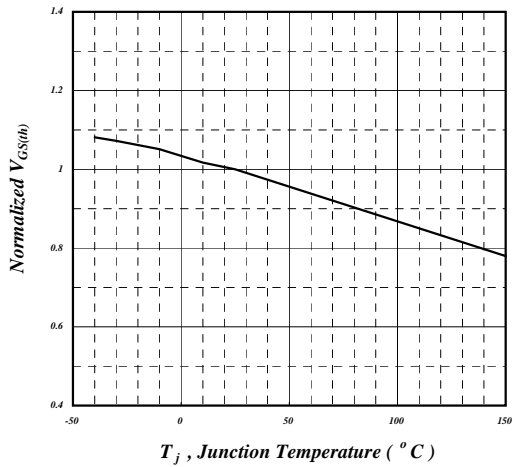


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

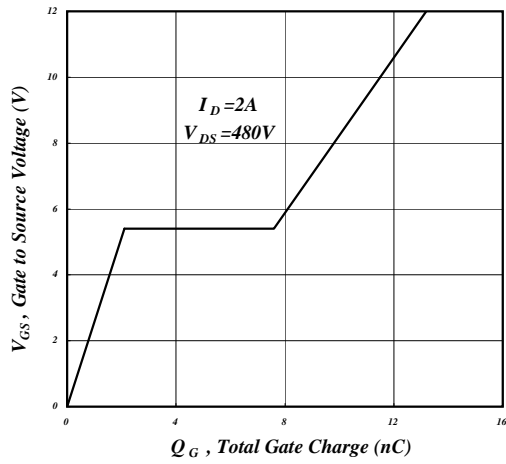


Fig 7. Gate Charge Characteristics

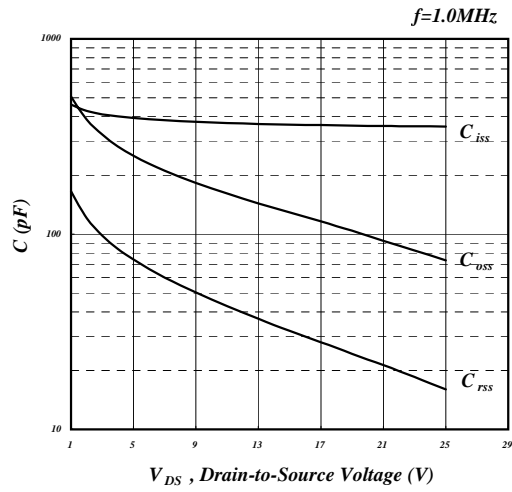


Fig 8. Typical Capacitance Characteristics

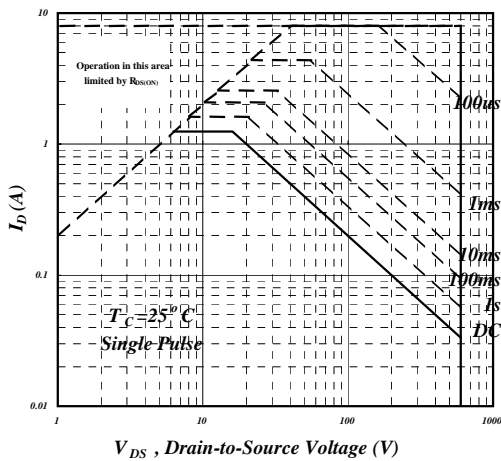


Fig 9. Maximum Safe Operating Area

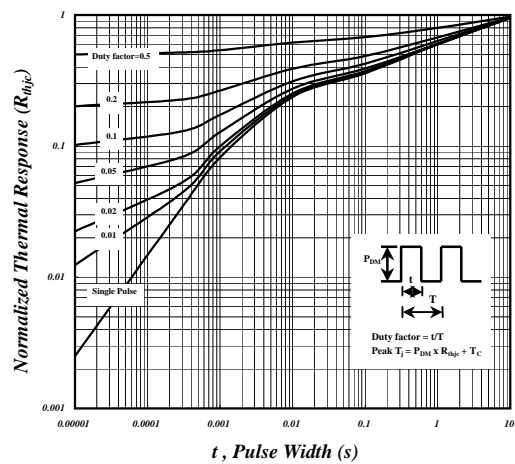


Fig 10. Effective Transient Thermal Impedance



Fig 11. Switching Time Waveform

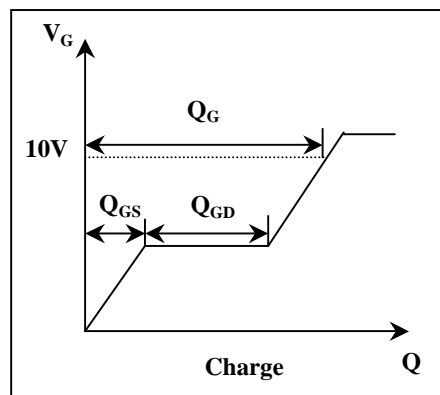


Fig 12. Gate Charge Waveform



MARKING INFORMATION

