TPS22916xx 1 V–5.5-V, 2-A, 60-mΩ Ultra-Low Leakage Load Switch

1 Features

- Input Operating Voltage Range (V_{IN}): 1 V–5.5 V
- Maximum Continuous Current (I_{MAX}): 2 A
- Low ON-Resistance (R_{ON}):
  - 5 V_{IN} = 60 mΩ (typ), 100 mΩ (85°C max)
  - 1.8 V_{IN} = 100 mΩ (typ), 150 mΩ (85°C max)
  - 1 V_{IN} = 200 mΩ (typ), 325 mΩ (85°C max)
- Ultra-Low Power Consumption:
  - ON State (I_Q): 0.5 µA (typ), 1.1 µA (85°C max)
  - OFF State (I_{SD}): 15 nA (typ), 150 nA (85°C max)
  - TPS22916CL OFF State (I_{SD}): 100 nA (typ), 270 nA (85°C max)
- Slow Timing in C Version Reduces Inrush Current (typical):
  - 5-V Turnon time (t_{ON}): 1400 µs at 5 mV/µs
  - 1.8-V Turnon time (t_{ON}): 3000 µs at 1 mV/µs
  - 1-V Turnon time (t_{ON}): 6500 µs at 0.3 mV/µs
- Fast Timing in B Version Reduces Wait Time (typ):
  - 5-V Turnon time (t_{ON}): 105 µs at 38 mV/µs
  - 1.8-V Turnon time (t_{ON}): 225 µs at 14 mV/µs
  - 1-V Turnon time (t_{ON}): 470 µs at 3.8 mV/µs
- Always-ON True Reverse Current Blocking (RCB):
  - ON State Activation Current (I_{RCB}): –500 mA (typ)
  - OFF State Leakage ($I_{IN,RCB}$): –300 nA (85°C max)
- Quick Output Discharge (QOD): 150 Ω (typ) (TPS22916B, TPS22916C, TPS22916CL only)
- Active Low Enable Option (TPS22916CL)

2 Applications

- Wearables
- Smartphones
- Tablets
- Portable Speakers

3 Description

The TPS22916xx is a small, single channel load switch utilizing a low leakage P-Channel MOSFET for minimum power loss. Advanced gate control design supports operating voltages as low as 1 V with minimal increase in ON-Resistance and power loss.

Multiple timing options are available to support various system loading conditions. For heavy capacitive loads, the slow turnon timing in the C version minimizes the inrush current. In cases with light capacitive loads, the fast timing in the B version reduces required wait time.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. Both Active High and Active Low (L) versions are available. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven high (>V_{IH}), the Smart Pull Down is disconnected to prevent unnecessary power loss.

The TPS22916xx is available in a small, space saving 0.78-mm × 0.78-mm, 0.4-mm pitch, 0.5-mm height 4-pin Wafer-Chip-Scale (WCSP) package (YFP). The device is characterized for operation over a temperature range of –40°C to +85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22916xx	WCSP (4)	0.78 mm × 0.78 mm

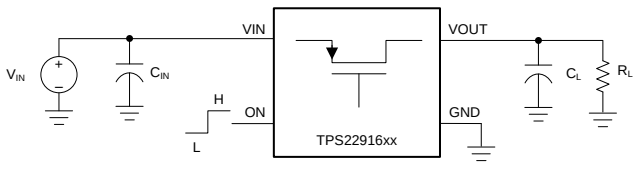
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Comparison Table

VERSION	TIMING	QOD	ENABLE (ON)
TPS22916B	Fast	Yes	Active High
TPS22916C	Slow	Yes	Active High
TPS22916CN	Slow	No	Active High
TPS22916CL	Slow	Yes	Active Low

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Simplified Schematic



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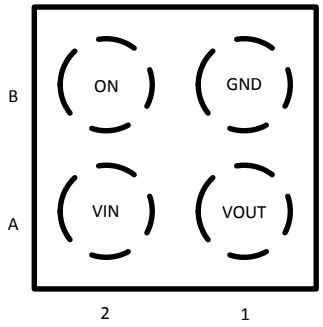
4 Revision History

DATE	REVISION	NOTES
July 2017	*	Initial release.

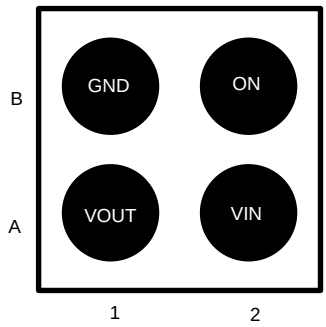
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5 Pin Configuration and Functions

YFP Package
4-Pin WSON
Laser Marking View



YFP Package
4-Pin WSON
Bump View



TPS22916xx Pin Functions

NO.	NAME	TYPE	DESCRIPTION
A1	VOUT	Power	Switch output
A2	VIN	Power	Switch input
B1	GND	Ground	Device ground
B2	ON	Digital input	Device enable

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	Enable voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		2.5	A
$T_{J,MAX}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead temperature (10-s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1	5.5	V
V_{OUT}	Output voltage	0	5.5	V
V_{IH}	High-level input voltage, ON	1	5.5	V
V_{IL}	Low-level input voltage, ON	0	0.35	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

Thermal Parameters(1)		TPS22916xx YFP (WCSP) 4 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	193	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	2.3	°C/W
θ_{JB}	Junction-to-board thermal resistance	36	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the recommended power supply voltage range of 1 V to 5.5 V. Typical Values are at 25°C.

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)								
$I_{Q,VIN}$	V_{IN} Quiescent current	Enabled, V_{OUT} = Open		25°C		0.5	1	µA
				–40°C to +85°C			1.1	
$I_{SD,VIN}$	V_{IN} Shutdown current	Disabled, V_{OUT} = GND or Open (TPS22916B/C/CN)		25°C		15	100	nA
				–40°C to +85°C			150	
		Disabled, V_{OUT} = GND or Open (TPS22916CL)		25°C		100	200	
				–40°C to +85°C			270	
ON-RESISTANCE (R_{ON})								
R_{ON}	On-state resistance	I_{OUT} = 200 mA	V_{IN} = 5 V	25°C		60	80	mΩ
				–40°C to +85°C			100	
				–40°C to +105°C			120	
			V_{IN} = 3.6 V	25°C		70	90	
				–40°C to +85°C			120	
				–40°C to +105°C			140	
			V_{IN} = 1.8 V	25°C		100	125	
				–40°C to +85°C			150	
				–40°C to +105°C			175	
			V_{IN} = 1.2 V	25°C		150	200	
				–40°C to +85°C			250	
				–40°C to +105°C			300	
			V_{IN} = 1 V	25°C		200	275	
				–40°C to +85°C			325	
				–40°C to +105°C			375	
ENABLE PIN (ON)								
I_{ON}	ON Pin leakage			–40°C to +85°C	–100	1	100	nA
R_{PD}	Smart pull down resistance	Disabled		–40°C to +85°C		1		MΩ
REVERSE CURRENT BLOCKING (RCB)								
I_{RCB}	Reverse activation current	Enabled		–40°C to +85°C		-500		mA
t_{RCB}	RCB Activation time	Enabled $I_{IN} > I_{RCB}$		–40°C to +85°C		10		µs
V_{RCB}	Release voltage	Enabled		–40°C to +85°C		25		mV
$I_{IN,RCB}$	V_{IN} Leakage current in RCB	0 V ≤ V_{IN} ≤ V_{OUT} ≤ 5.5 V		–40°C to +85°C	–300			nA
QUICK OUTPUT DISCHARGE (QOD)								
QOD (1)	Output discharge resistance	Disabled (Not in TPS22916CN)		–40°C to +85°C		150		Ω

(1) For more information on which devices include quick output discharge, see the *Device Functional Modes* section.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916B						
Rising slew rate	SR_{ON}	VIN = 1 V		3.8		mV/µs
		VIN = 1.2 V		6.4		
		VIN = 1.8 V		14		
		VIN = 3.6 V		44		
		VIN = 5 V		38		
Turnon delay	t_D	VIN = 1 V		260		µs
		VIN = 1.2 V		200		
		VIN = 1.8 V		125		
		VIN = 3.6 V		65		
		VIN = 5 V		45		
Rise time	t_R	VIN = 1 V		210		
		VIN = 1.2 V		150		
		VIN = 1.8 V		100		
		VIN = 3.6 V		65		
		VIN = 5 V		60		
Turnon time	t_{ON}	VIN = 1 V		470		
		VIN = 1.2 V		350		
		VIN = 1.8 V		225		
		VIN = 3.6 V		130		
		VIN = 5 V		105		
Turnoff time	t_{OFF}	VIN = 1 V		25		
		VIN = 1.2 V		15		
		VIN = 1.8 V		10		
		VIN = 3.6 V		5		
		VIN = 5 V		5		
Fall time	t_F	Depends on R_L and C_L				

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Switching Characteristics (continued)

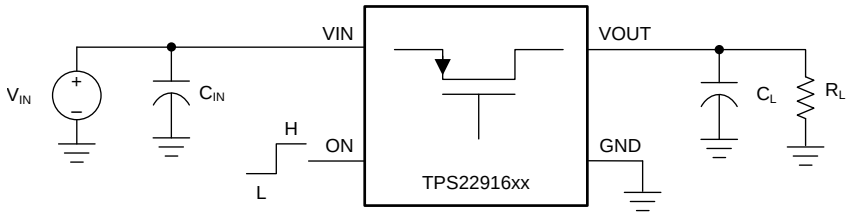
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916C, TPS22916CN, TPS22916CL						
Rising slew rate	SR_{ON}	VIN = 1 V		0.3		mV/µs
		VIN = 1.2 V		0.4		
		VIN = 1.8 V		1		
		VIN = 3.6 V		3.2		
		VIN = 5 V		5		
Turnon delay	t_D	VIN = 1 V		3500		µs
		VIN = 1.2 V		2700		
		VIN = 1.8 V		1600		
		VIN = 3.6 V		800		
		VIN = 5 V		600		
Rise time	t_R	VIN = 1 V		3000		
		VIN = 1.2 V		2300		
		VIN = 1.8 V		1400		
		VIN = 3.6 V		900		
		VIN = 5 V		800		
Turnon time	t_{ON}	VIN = 1 V		6500		
		VIN = 1.2 V		5000		
		VIN = 1.8 V		3000		
		VIN = 3.6 V		1700		
		VIN = 5 V		1400		
Turnoff time	t_{OFF}	VIN = 1 V		25		
		VIN = 1.2 V		15		
		VIN = 1.8 V		10		
		VIN = 3.6 V		5		
		VIN = 5 V		5		
Fall time	t_F	Depends on R_L and C_L (1)				

(1) See the *Quick Output Discharge (QOD)* section for information on how R_L and C_L affect Fall Time.

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7 Parameter Measurement Information



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Figure 1. TPS22916 Test Circuit

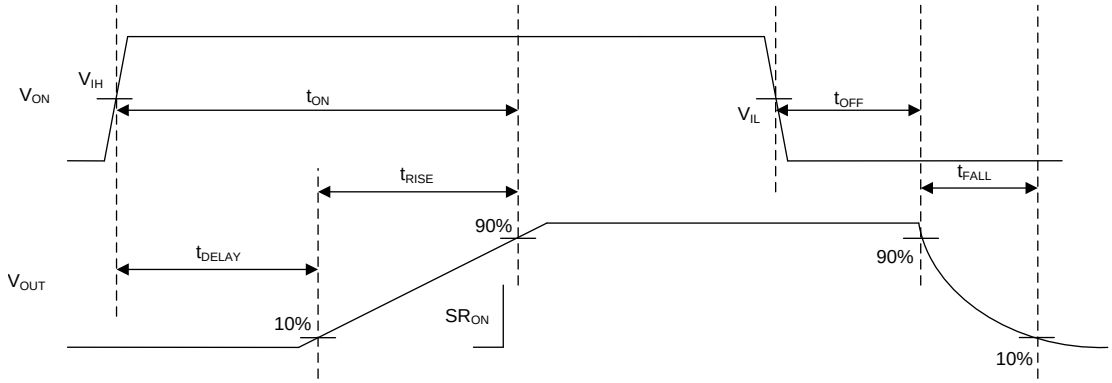


Figure 2. TPS22916 Timing Waveform

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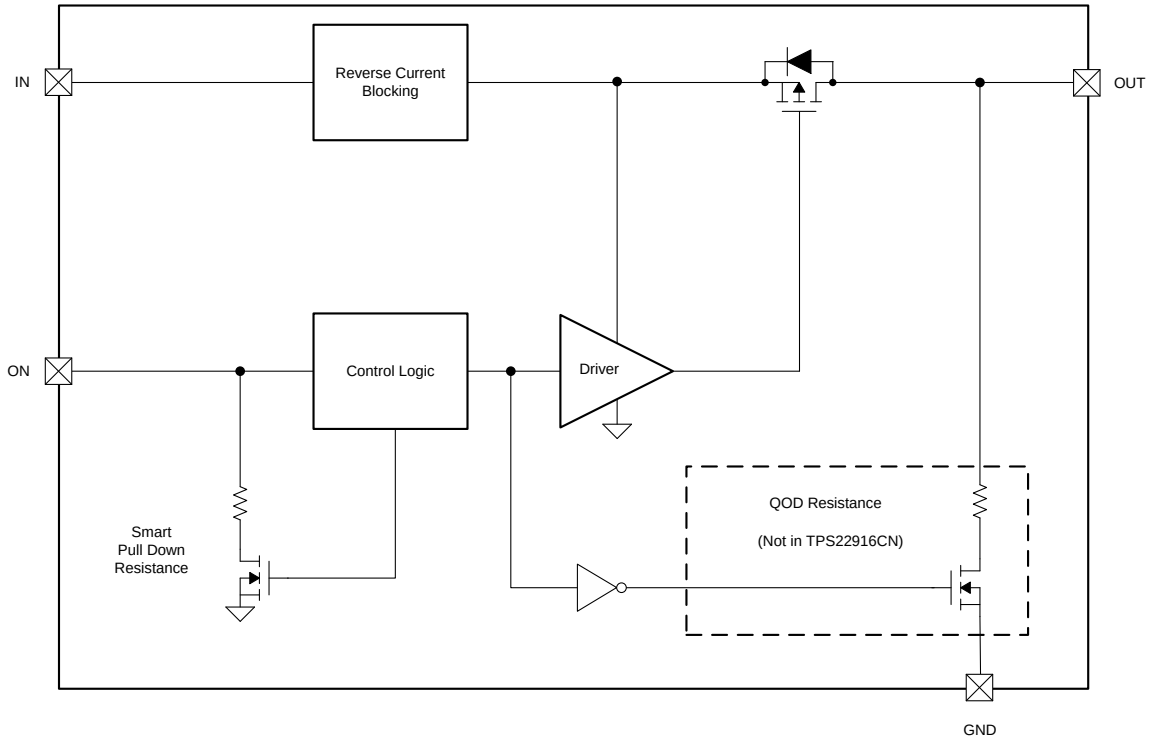
8 Detailed Description

8.1 Overview

This family of devices are single channel, 2-A load switches in ultra-small, space saving 4-pin WCSP package. These devices implement a low resistance P-channel MOSFET with a controlled rise time for applications that need to limit inrush current.

These devices are designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and BOM count.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, 3.3-V, or 5.5-V GPIO.

8.3.2 Quick Output Discharge (QOD)

The TPS22916B/C/CL include a Quick Output Discharge feature. The TPS22916CN does not include a Quick Output Discharge Feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of QOD and prevents the output from floating while the switch is disabled.

As load capacitance and load resistance increase: t_{FALL} increases. The larger the load resistance or load capacitance is, the longer it takes to discharge the capacitor, resulting in a longer fall time.

Capacitance discharge follows Equation 1.

$$t_{FALL} = -R_L \times C_L \times \ln(V_{10\%}/V_{90\%})$$

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Feature Description (continued)

Where

- $V_{10\%}$ is 10% of the initial output voltage
- $V_{90\%}$ is 90% of the initial output voltage
- R_L is the load resistance
- C_L is the load capacitance (1)

With the Quick Output Discharge feature, the QOD resistance is in parallel with R_L. This provides a lower total load resistance as seen from the load capacitance which discharges the capacitance faster resulting in a smaller t_{FALL}.

8.3.3 Full-Time Reverse Current Blocking

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN} there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold (I_{RCB}) is exceeded, the switch is disabled within t_{RCB}. See Figure 3.

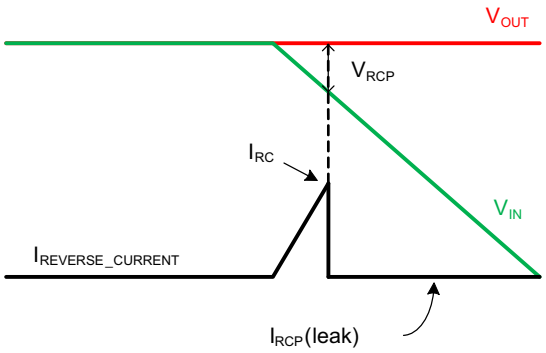


Figure 3. Reverse Current

8.4 Device Functional Modes

Table 1 describes what the V_{OUT} pin is connected to for a particular device as determined by the ON pin

Table 1. Device Function Table

ON	TPS22916B	TPS22916C	TPS22916CN	TPS22916CL
Below V_{IL}	Disabled	Disabled	Disabled	Enabled
Above V_{IH}	Enabled	Enabled	Enabled	Disabled

Table 2 shows the QOD functions.

Table 2. QOD Function Table

Device	TPS22916B	TPS22916C	TPS22916CN	TPS22916CL
Enabled	No	No	No	No
Disabled	Yes	Yes	No	Yes

Table 3 shows the Smart-ON functions.

Table 3. Smart-ON Functional Modes

ON	ON Pin
Below V_{IL}	Pull down active
Above V_{IH}	No pull down

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Thermal Considerations

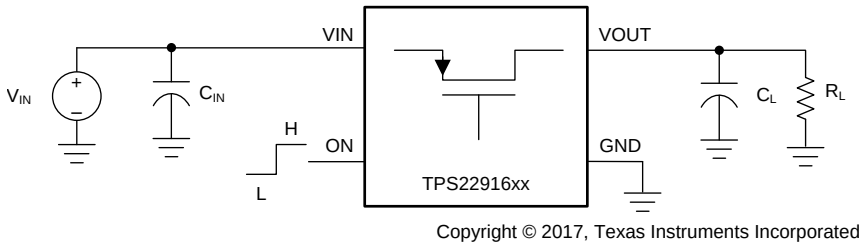
The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 2 as a guideline:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (2)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

9.2 Typical Application



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Figure 4. Typical Application

9.2.1 Design Requirements

For this design example, below, use the input parameters shown in Table 4.

Table 4. Design Parameters

Design Parameter	Example Value
V_{IN}	1.8 V
I_{LOAD}	500 mA
Maximum Voltage Drop	5%

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Voltage Drop and On-Resistance

At 1.8-V input voltage, with a maximum voltage drop tolerance of 5%, the TPS22916 has a typical RON of 100 mΩ. The rail is supplying 500 mA of current; the voltage drop for a rail is calculated based on Equation 3 and Equation 4.

$$V_{DROP} = R_{ON} \times I_{LOAD} \quad (3)$$

$$V_{DROP} = 50\ mV \quad (4)$$

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The maximum voltage drop is 5% which is 90 mV. The voltage drop caused by the load current across the on resistance is 50 mV.

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10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

Figure 5 shows an example for these devices. Notice the connection to system ground between the V_{OUT} Bypass Capacitor ground and the GND pin of the load switch, this creates a ground barrier which helps to reduce the ground noise seen by the device.

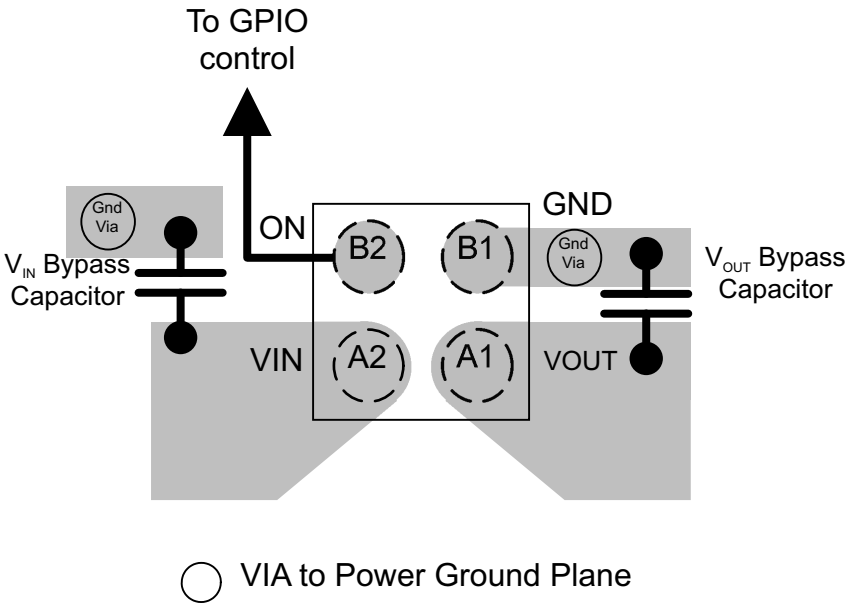


Figure 5. TPS22916xx Layout

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TPS22916 Load Switch Evaluation Module

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS22916BYFPT	ACTIVE	DSBGA	YFP	4	250	TBD	Call TI	Call TI	-40 to 85		Samples
PTPS22916CYFPT	ACTIVE	DSBGA	YFP	4	250	TBD	Call TI	Call TI	-40 to 85		Samples
TPS22916BYFPR	PREVIEW	DSBGA	YFP	4	3000	TBD	Call TI	Call TI	-40 to 85		
TPS22916BYFPT	PREVIEW	DSBGA	YFP	4	250	TBD	Call TI	Call TI	-40 to 85		
TPS22916CYFPR	PREVIEW	DSBGA	YFP	4	3000	TBD	Call TI	Call TI	-40 to 85		
TPS22916CYFPT	PREVIEW	DSBGA	YFP	4	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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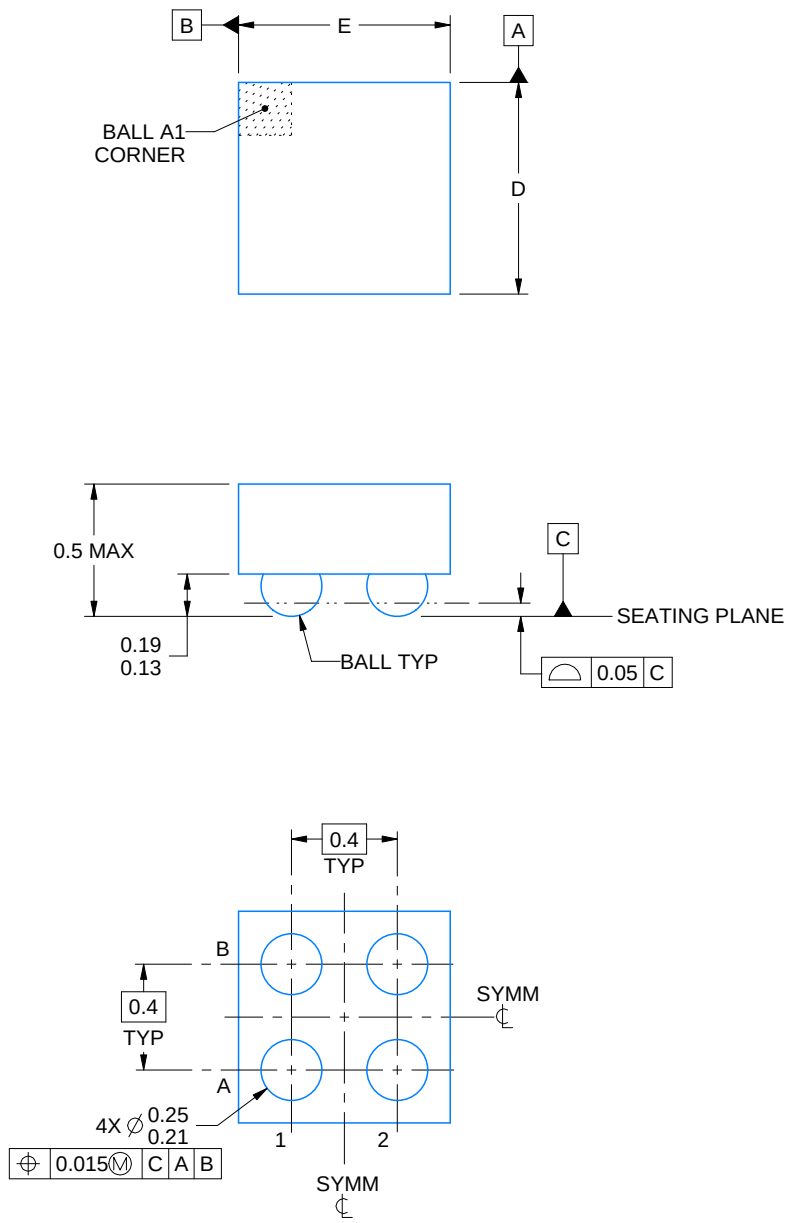
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

YFP0004

DSBGA - 0.5 mm max height

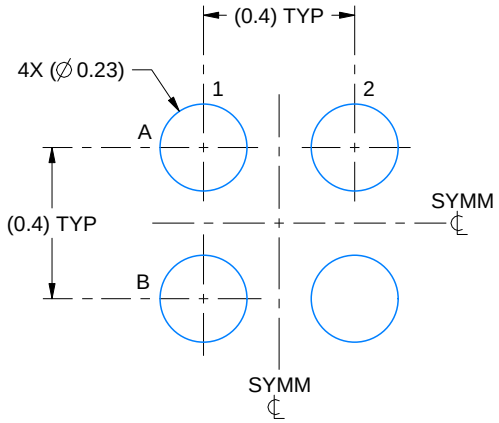
DIE SIZE BALL GRID ARRAY



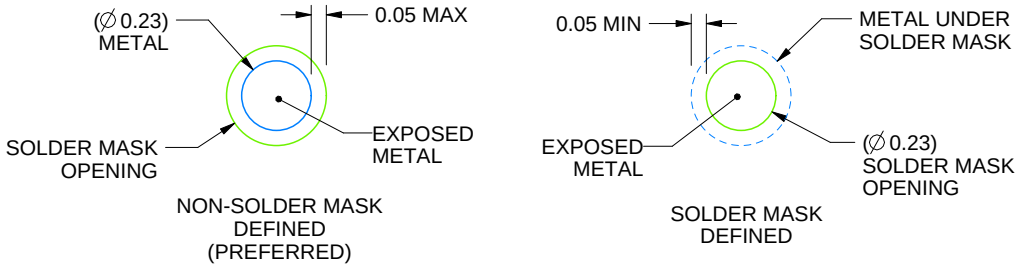
4223507/A 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

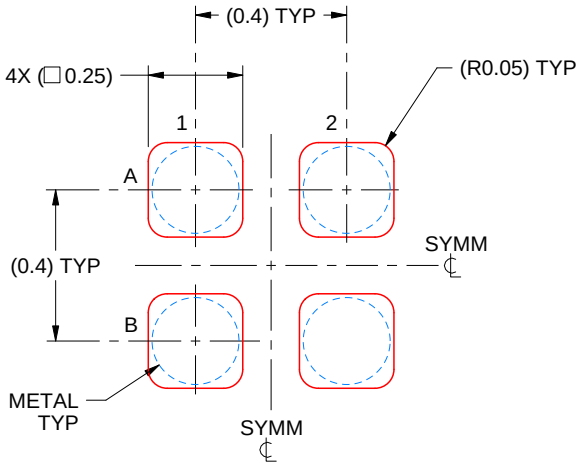
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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