Future Technology Devices International Ltd.

FT240X

(USB 8-BIT FIFO IC)



The FT240X is a USB to parallel FIFO interface with the following advanced features:

- Single chip USB to parallel FIFO bidirectional data transfer interface.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Fully integrated 2048 byte multi-time-programmable (MTP) memory, storing device descriptors and FIFO I/O configuration.
- Fully integrated clock generation with no external crystal required plus optional clock output selection enabling glue-less interface to external MCU or FPGA.
- Data transfer rates up to 1Mbyte / second.
- 512 byte receive buffer and 512 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Configurable FIFO interface I/O pins.
- Synchronous and asynchronous bit bang interface options.
- USB Battery Charger Detection. Allows for USB peripheral devices to detect the presence of a higher power source to enable improved charging.
- Device supplied pre-programmed with unique USB serial number.
- USB Power Configurations; supports bus- powered, self-powered and bus-powered with power switching.
- Integrated +3.3V level converter for USB I/O.
- True 3.3V CMOS drive output and TTL input; operates down to 1V8 with external pull-ups. Tolerant of 5V input.
- Configurable I/O pin output drive strength; 4 mA(min) and 16 mA(max).
- Integrated power-on-reset circuit.
- Fully integrated AVCC supply filtering - no external filtering required.
- +5V Single Supply Operation.
- Internal 3V3/1V8 LDO regulators
- Low operating and USB suspend current; 8mA (active-typ) and 125uA (suspend-typ).
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed capable.
- Extended operating temperature range; -40 to 85ºC.
- Available in compact Pb-free 24 Pin SSOP and QFN-24 packages (both RoHS compliant).

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1 Typical Applications

- Upgrading Legacy Peripherals to USB
- Utilising USB to add system modularity
- Incorporate USB interface to enable PC transfers for development system communication
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU/PLD/FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- USB Smart Card Readers
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader and Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Software and Hardware Encryption Dongles
- USB Instrumentation
- USB dongle implementations for Software/ Hardware Encryption and Wireless Modules
- Provides detection of dedicated charging ports for charging batteries in portable devices.

1.1 Driver Support

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows XP Embedded
- Server 2003, XP and Server 2008
- Windows CE 4.2, 5.0 and 6.0
- Mac OS-X
- Linux 3.2 and greater
- Android

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows XP Embedded
- Server 2003, XP and Server 2008
- Windows CE 4.2, 5.0 and 6.0
- Mac OS-X
- Linux 2.6 and greater
- Android

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details. For driver installation, please refer to the application note AN232B-10.

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

1.2 Part Numbers

Part Number	Package
FT240XQ-x	24 Pin QFN
FT240XS-x	24 Pin SSOP

Note: Packaging codes for x is:

-R: Taped and Reel, (SSOP is 3,000pcs per reel, QFN is 5,000pcs per reel).

- U: Tube packing, 58pcs per tube (SSOP only)

- T: Tray packing, 490pcs per tray (QFN only)

For example: FT240XQ-R is 5,000pcs taped and reel packing

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1.3 USB Compliant

The FT240X is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40001466 (Rev D).



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2 FT240X Block Diagram

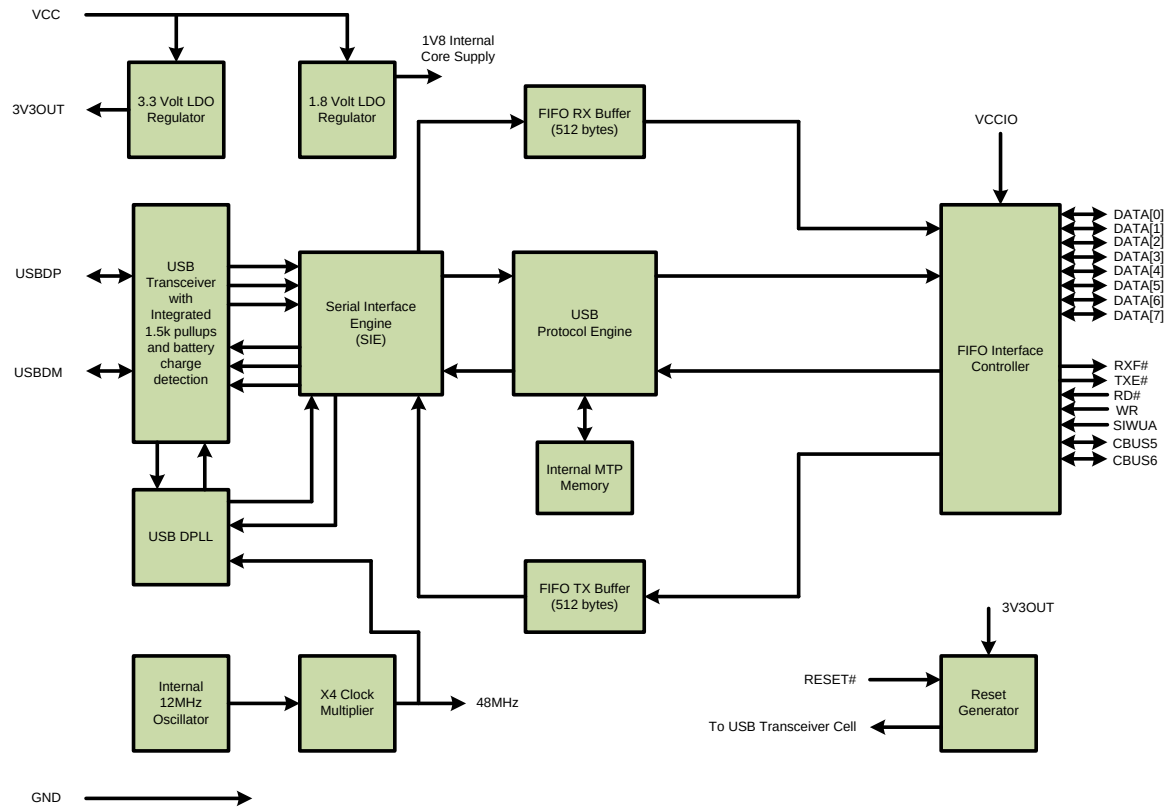


Figure 2.1 FT240X Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 24-LD SSOP Package

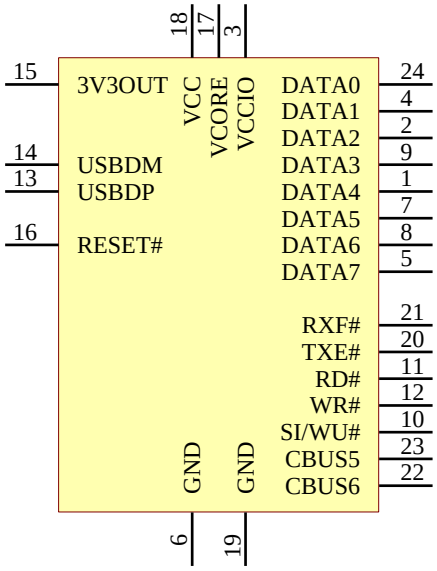


Figure 3.1 SSOP Package Pin Out and Schematic Symbol

3.2 SSOP Package Pin Out Description

Note: The convention used throughout this document for active low signals is the signal name followed by a #

Pin No.	Name	Type	Description
13	USBDP	I/O	USB Data Signal Plus, incorporating 1.5kΩ pull up resistor to 3.3V.
14	USBDM	I/O	USB Data Signal Minus.

Table 3.1 USB Interface Group

Pin No.	Name	Type	Description
3	VCCIO	PWR	1V8 - 3V3 supply for the IO cells
6, 19	GND	PWR	Device ground supply pins
15	** 3V3OUT	Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 15 is an input pin and should be connected to pin 18.
18	** VCC	PWR	+5V (or 3V3) supply to the device core.
17	VCORE	PWR	+1V8 Output. May be left unterminated

Table 3.2 Power and Ground Group

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

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Pin No.	Name	Type	Description
16	RESET#	Input	Active low reset pin. This can be used by an external device to reset the FT240X. If not required can be left unconnected, or pulled up to VCC.
10	SIWU#	Input	Active low input. May be used to flush the IC buffer back to the PC (Send Immediate) or if the PC is in suspend mode it can be used as a Wake Up signal.
23	CBUS5	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.9.
22	CBUS6	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.9.

Table 3.3 Miscellaneous Signal Group

Pin No.	Name	Type	Description
24	D0	I/O	FIFO Data Bus Bit 0
4	D1	I/O	FIFO Data Bus Bit 1
2	D2	I/O	FIFO Data Bus Bit 2
9	D3	I/O	FIFO Data Bus Bit 3
1	D4	I/O	FIFO Data Bus Bit 4
7	D5	I/O	FIFO Data Bus Bit 5
8	D6	I/O	FIFO Data Bus Bit 6
5	D7	I/O	FIFO Data Bus Bit 7
11	RD#	Input	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low. See Section 3.6 for timing diagram.
12	WR	Input	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low. See Section 3.7 for timing diagram.
20	TXE#	Output	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. During reset this signal pin is tri-state. See Section 3.7 for timing diagram.
21	RXF#	Output	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again. During reset this signal pin is tri-state. See Section 3.6 for timing diagram. If the Remote Wakeup option is enabled in the internal MTP memory, during USB suspend mode (PWREN# = 1) RXF# becomes an input. This can be used to wake up the USB host from suspend mode by strobing this pin low for a minimum of 20ms which will cause the device to request a resume on the USB bus.

Table 3.4 FIFO Interface Group (see note 2)

Notes:

When used in Input Mode, the input pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal MTP memory.

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3.3 QFN-24 Package

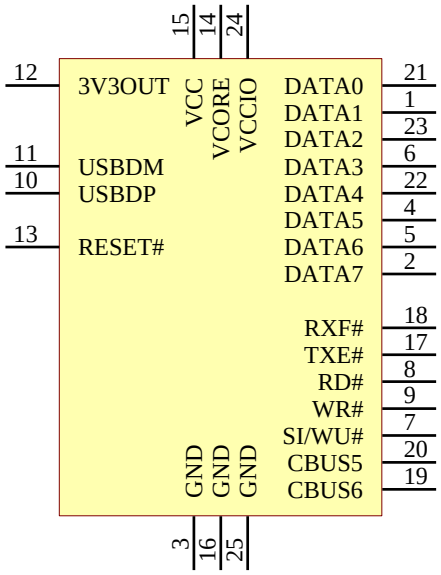


Figure 3.2 QFN-24 Package Pin Out and schematic symbol

3.4 QFN-24 Package Signal Description

Note: The convention used throughout this document for active low signals is the signal name followed by a #

Pin No.	Name	Type	Description
10	USBDP	I/O	USB Data Signal Plus, incorporating 1.5kΩ pull up resistor to 3.3V.
11	USBDM	I/O	USB Data Signal Minus.

Table 3.5 USB Interface Group

Pin No.	Name	Type	Description
24	VCCIO	PWR	1V8 - 3V3 supply for the IO cells
3, 16	GND	PWR	Device ground supply pins
12	** 3V3OUT	Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 12 is an input pin and should be connected to pin 15.
15	** VCC	PWR	+5V (or 3V3) supply to the device core.
14	VCORE	PWR	+1V8 Output. May be left unterminated

Table 3.6 Power and Ground Group

*Pin 25 is the centre pad on package base. Connect to GND.

**If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

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Pin No.	Name	Type	Description
13	RESET#	Input	Active low reset pin. This can be used by an external device to reset the FT240X. If not required can be left unconnected, or pulled up to VCC.
7	SIWU#	Input	Active low input. May be used to flush the IC buffer back to the PC (Send Immediate) or if the PC is in suspend mode it can be used as a Wake Up signal.
20	CBUS5	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.9.
19	CBUS6	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.9.

Table 3.7 Miscellaneous Signal Group

Pin No.	Name	Type	Description
21	D0	I/O	FIFO Data Bus Bit 0
1	D1	I/O	FIFO Data Bus Bit 1
23	D2	I/O	FIFO Data Bus Bit 2
6	D3	I/O	FIFO Data Bus Bit 3
22	D4	I/O	FIFO Data Bus Bit 4
4	D5	I/O	FIFO Data Bus Bit 5
5	D6	I/O	FIFO Data Bus Bit 6
2	D7	I/O	FIFO Data Bus Bit 7
8	RD#	Input	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low. See Section 3.6 for timing diagram.
9	WR	Input	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low. See Section 3.7 for timing diagram.
17	TXE#	Output	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. During reset this signal pin is tri-state. See Section 3.7 for timing diagram.
18	RXF#	Output	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again. During reset this signal pin is tri-state. See Section 3.6 for timing diagram. If the Remote Wakeup option is enabled in the internal MTP memory, during USB suspend mode (PWREN# = 1) RXF# becomes an input. This can be used to wake up the USB host from suspend mode by strobing this pin low for a minimum of 20ms which will cause the device to request a resume on the USB bus.

Table 3.8 FIFO Interface Group (see note 2)

Notes:

When used in Input Mode, the input pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal MTP memory.

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3.5 CBUS Signal Options

The following options can be configured on the CBUS I/O pins. CBUS signal options are common to both package versions of the FT240X. These options can be configured in the internal MTP memory using the software utility FT_PPROG, which can be downloaded from the FTDI Utilities (www.ftdichip.com). The default configuration is described in Section 8.

CBUS Signal Option	Available On CBUS Pin	Description
TRI-STATE	CBUS5, CBUS6	IO Pad is tri-stated
DRIVE 1	CBUS5, CBUS6	Output a constant 1
DRIVE 0	CBUS5, CBUS6	Output a constant 0
PWREN#	CBUS5, CBUS6	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.
SLEEP#	CBUS5, CBUS6	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
CLK24MHz	CBUS5, CBUS6	24 MHz Clock output.*
CLK12MHz	CBUS5, CBUS6	12 MHz Clock output.*
CLK6MHz	CBUS5, CBUS6	6 MHz Clock output.*
BCD Charger	CBUS5, CBUS6	Battery charge Detect, indicates when the device is connected to a dedicated battery charger host. Active high output.
BCD Charger#	CBUS5, CBUS6	Inverse of BCD Charger
BitBang_WR#	CBUS5, CBUS6	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBang_RD#	CBUS5, CBUS6	Synchronous and asynchronous bit bang mode RD# strobe output.
VBUS Sense	CBUS5, CBUS6	Input to detect when VBUS is present.
Time Stamp	CBUS5, CBUS6	Toggle signal which changes state each time a USB SOF is received
Keep_Awake#	CBUS5, CBUS6	Prevents the device from entering suspend state when unplugged.

Table 3.9 CBUS Configuration Control

*When in USB suspend mode the outputs clocks are also suspended.

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3.6 FT240X FIFO READ Timing Diagrams

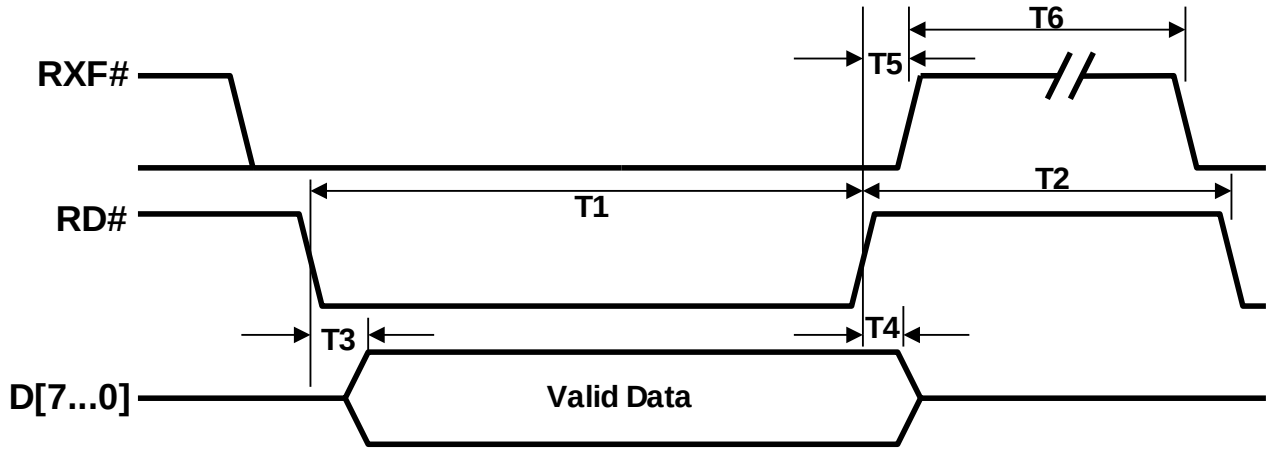


Figure 3.3 FIFO Read Cycle

Time	Description	Minimum	Maximum	Unit
T1	RD# Active Pulse Width	50	-	ns
T2	RD# to RD# Pre-Charge Time	50 + T6	-	ns
T3	RD# Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD# Inactive*	0	-	ns
T5	RD# Inactive to RXF#	0	25	ns
T6	RXF# Inactive After RD Cycle	80	-	ns

Table 3.10 FIFO Read Cycle Timings

*Load = 30pF

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3.7 FT240X FIFO WRITE Timing Diagrams

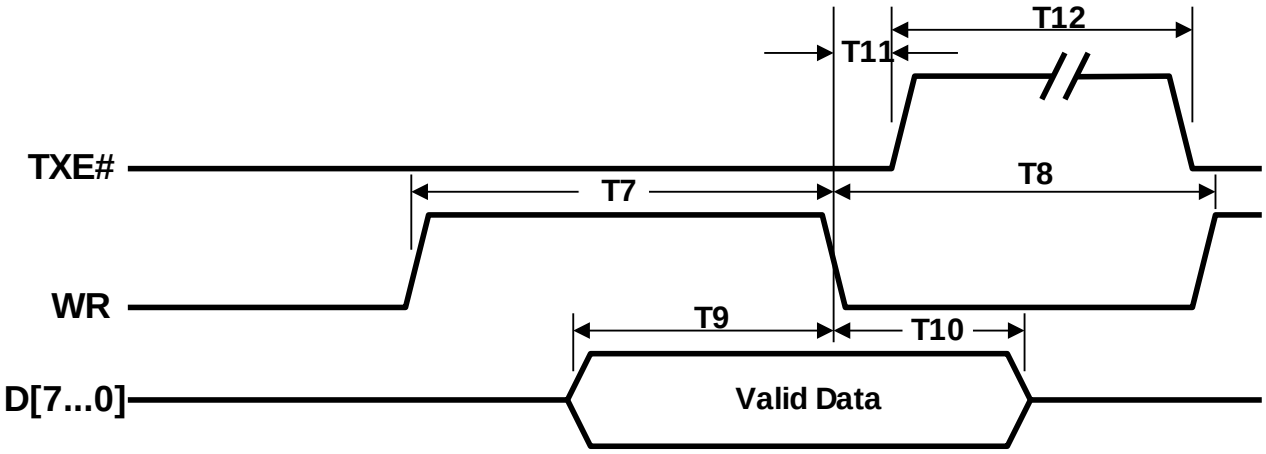


Figure 3.4 FIFO Write Cycle

Time	Description	Minimum	Maximum	Unit
T7	WR Active Pulse Width	50	-	ns
T8	WR to WR Pre-Charge Time	50	-	ns
T9	Valid data setup to WR falling edge*	20	-	ns
T10	Valid Data Hold Time from WR Inactive*	0	-	ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE# Inactive After WR Cycle	80	-	ns

Table 3.11 FIFO Write Cycle

*Load = 30pF

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4 Function Description

The FT240X is a USB to parallel FIFO interface device which simplifies USB implementations and reduces external component count by fully integrating into the device an MTP memory and an integrated clock circuit which requires no external crystal. It has been designed to operate efficiently with USB host controllers by using as little bandwidth as possible when compared to the total USB bandwidth available.

4.1 Key Features

Functional Integration. Fully integrated MTP memory, clock generation, AVCC filtering, power-on-reset (POR) and LDO regulator.

Configurable CBUS I/O Pin Options. The fully integrated MTP memory allows configuration of the Control Bus (CBUS) functionality and drive strength selection. There are 2 configurable CBUS I/O options. The configurable options are defined in section 3.5.

The CBUS lines can be configured with any one of these output options by setting bits in the internal MTP memory. The device is shipped with the most commonly used pin definitions pre-programmed - see Section 8 for details.

Asynchronous Bit Bang Mode. In asynchronous bit-bang mode, the eight FIFO lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate pre-scaler. This option will be described more fully in a separate application note available from FTDI website (www.ftdichip.com).

Synchronous Bit Bang Mode. The FT240X supports synchronous bit bang mode. This mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

High Output Drive Option. The parallel FIFO interface and the four FIFO handshake pins can be made to drive out at three times the standard signal drive level thus allowing multiple devices to be driven, or devices that require a greater signal drive strength to be interfaced to the FT240X. This option is configured in the internal MTP memory.

Programmable FIFO RX Buffer Timeout. The FIFO RX buffer timeout is used to flush remaining data from the receive buffer. This timeout defaults to 16ms, but is programmable over USB in 1ms increments from 2ms to 255ms, thus allowing the device to be optimised for protocols that require fast response times from short data packets.

Wake Up Function. If USB is in suspend mode, and remote wake up has been enabled in the internal MTP memory (it is enabled by default). Strobing the SIWU# pin low for a minimum of 20ms will cause the FT240X to request a resume from suspend on the USB bus. Normally this can be used to wake up the host PC from suspend.

Source Power and Power Consumption. The FT240X is capable of operating at a voltage supply between +3.3V and +5.25V with a nominal operational mode current of 8mA and a nominal USB suspend mode current of 125µA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within allows the FT240X to interface to logic running at +1.8V to +3.3V (5V tolerant).

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4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT240X. Please refer to the block diagram shown in Figure 2.1.

Internal MTP Memory. The internal MTP memory in the FT240X is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. The FT240X is supplied with the internal MTP memory pre-programmed as described in Section 8. A user area of the internal MTP memory is available to system designers to allow storing additional data from the user application over USB. The internal MTP memory descriptors can be programmed in circuit, over USB without any additional voltage requirement. The descriptors can be programmed using the FTDI utility software called FT_PROG, which can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com).

+1.8V LDO Regulator. The +1.8 LDO regulator generates the +1.8V reference voltage for driving the internal core of the IC.

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides +3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of the LDO is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, it can be used to supply external circuitry requiring a +3.3V nominal supply with a maximum current of 50mA.

USB Transceiver. The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide +3.3V level slew rate control signalling, whilst a differential input receiver and two single ended input receivers provide USB data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. This function also incorporates a 1.5kΩ pull up resistor on USBDP. The block also detects when connected to a USB power supply which will not enumerate the device but still supply power and may be used for battery charging.

USB DPLL. The USB DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals for the Serial Interface Engine (SIE) block.

Internal 12MHz Oscillator. The Internal 12MHz Oscillator cell generates a 12MHz reference clock. This provides an input to the x4 Clock Multiplier function. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and FIFO controller blocks.

Clock Multiplier / Divider. The Clock Multiplier / Divider takes the 12MHz input from the Internal Oscillator function and generates the 48MHz. The 48Mz clock reference is used by the USB DPLL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also verifies the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the FIFO in accordance with the USB 2.0 specification Section 9.

FIFO RX Buffer (512 bytes). Data sent from the USB host controller to the FIFO via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer and is removed from the buffer by reading the contents of the FIFO using the RD# pin. (Rx relative to the USB interface).

FIFO TX Buffer (512 bytes). Data written into the FIFO using the WR pin is stored in the FIFO TX (transmit) Buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (Tx relative to the USB interface).

FIFO Controller with Programmable High Drive. The FIFO Controller handles the transfer of data between the FIFO RX, the FIFO TX buffers and the external FIFO interface pins (D0 - D7).

Additionally, the FIFO signals have a configurable high drive strength capability which is configurable in the MTP memory.

RESET Generator. The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT240X.

RESET# can be tied to VCC or left unconnected if not being used.

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5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT240X devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-65°C to 150°C	Degrees C	
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours	
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C	
MTTF FT240XS	TBD	Hours	
MTTF FT240XQ	TBD	Hours	
VCC Supply Voltage	-0.3 to +5.5	V	
VCCIO IO Voltage	-0.3 to +4.0	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	
DC Input Voltage – High Impedance Bi-directionals (powered from VCCIO)	-0.3 to +5.8	V	
DC Output Current – Outputs	22	mA	

Table 5.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 ESD and Latch-up Specifications

Description	Specification
Human Body Mode (HBM)	**> ± 2kV**
Machine mode (MM)	**> ± 200V**
Charged Device Mode (CDM)	**> ± 500V**
Latch-up	**> ± 200mA**

Table 5.2 ESD and Latch-Up Specifications

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5.3 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC	VCC Operating Supply Voltage	2.97	5	5.5	V	Normal Operation
VCC2	VCCIO Operating Supply Voltage	1.62	---	3.63	V	
Icc1	Operating Supply Current	8	8	8.4	mA	Normal Operation
Icc2	Operating Supply Current		125		µA	USB Suspend
3V3	3.3v regulator output	2.97	3.3	3.63	V	VCC must be greater than 3V3 otherwise 3V3OUT is an input which must be driven with 3.3V

Table 5.3 Operating Voltage and Current

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.97	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	2.0			V	LVTTL
Vt	Switching Threshold		1.49		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		1.15		V	
Vt+	Schmitt trigger positive going threshold voltage		1.64		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 5.4 FIFO I/O Pin Characteristics VCCIO = +3.3V, (except USB PHY pins)
* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.25	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	0.8			V	LVTTL
Vt	Switching Threshold		1.1		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.8		V	
Vt+	Schmitt trigger positive going threshold voltage		1.2		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 5.5 FIFO I/O Pin Characteristics VCCIO = +2.5V, (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.62	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.77	V	LVTTL
Vih	Input High Switching Threshold	1.6			V	LVTTL
Vt	Switching Threshold		0.77		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.557		V	
Vt+	Schmitt trigger positive going threshold voltage		0.893		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 5.6 FIFO I/O Pin Characteristics VCCIO = +1.8V (except USB PHY pins)
* The I/O drive strength and slow slew-rate are configurable in the MTP memory

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Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCC-0.2			V	
Vol	Output Voltage Low			0.2	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 5.7 USB I/O Pin (USBDP, USBDM) Characteristics

5.4 MTP Memory Reliability Characteristics

The internal 2048 Byte MTP memory has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Write Cycle	2,000	Cycles
Read Cycle	Unlimited	Cycles

Table 5.8 MTP Memory Characteristics

5.5 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 5.9 Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm

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6 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT240X. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT240XS and FT240XQ package options.

All USB power configurations illustrated apply to both package options for the FT240X device. Please refer to Section 0 for the package option pin-out and signal descriptions.

6.1 USB Bus Powered Configuration

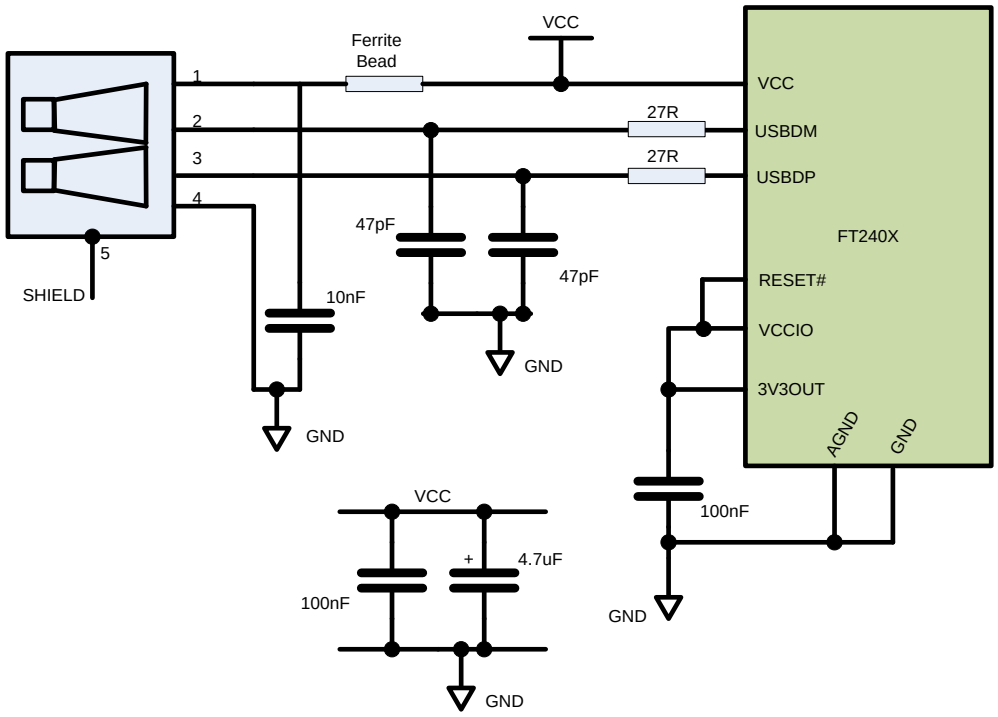


Figure 6.1 Bus Powered Configuration

Figure 6.1 illustrates the FT240X in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. Basic rules for USB bus power devices are as follows –

i) On plug-in to USB, the device should draw no more current than 100mA.
ii) In USB Suspend mode the device should draw no more than 2.5mA.
iii) A bus powered high power USB device (one that draws more than 100mA) should use the PWREN# to keep the current below 100mA on plug-in and 2.5mA on USB suspend.
iv) A device that consumes more than 100mA cannot be plugged into a USB bus powered hub.
v) No device can draw more than 500mA from the USB bus.

The power descriptors in the internal MTP memory of the FT240X should be programmed to match the current drawn by the device.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT240X and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application. A suitable range of Ferrite Beads is available from Steward (www.steward.com), for example Steward Part # MI0805K601R-10.

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6.2 Self Powered Configuration

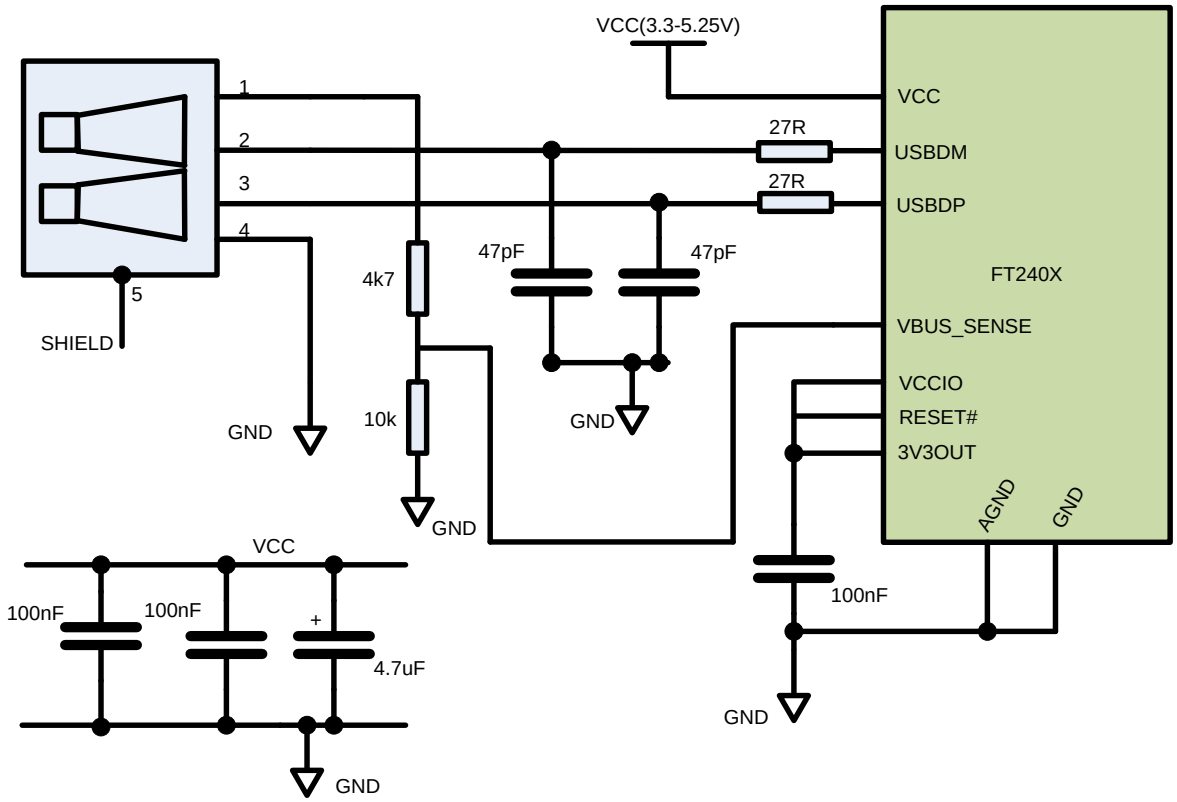


Figure 6.2 Self Powered Configuration

Figure 6.2 illustrates the FT240X in a typical USB self powered configuration. A USB self powered device gets its power from its own power supply, VCC, and does not draw current from the USB bus. The basic rules for USB self powered devices are as follows –

i) A self powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii) A self powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii) A self powered device can be used with any USB host, a bus powered USB hub or a self powered USB hub.

The power descriptor in the internal MTP memory of the FT240X should be programmed to a value of zero (self powered).

In order to comply with the first requirement above, the USB bus power (pin 1) is used to control the VBUS_Sense pin of the FT240X device. When the USB host or hub is powered up an internal 1.5kΩ resistor on USBDP is pulled up to +3.3V, thus identifying the device as a full speed device to the USB host or hub. When the USB host or hub is powered off, VBUS_Sense pin will be low and the FT240X is held in a suspend state. In this state the internal 1.5kΩ resistor is not pulled up to any power supply (hub or host is powered down), so no current flows down USBDP via the 1.5kΩ pull-up resistor. Failure to do this may cause some USB host or hub controllers to power up erratically.

Figure 6.3 illustrates a self powered design which has a +3.3V to +5.25V supply.

Note:

1. When the FT240X is in reset, the interface I/O pins are tri-stated. Input pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

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6.3 USB Bus Powered with Power Switching Configuration

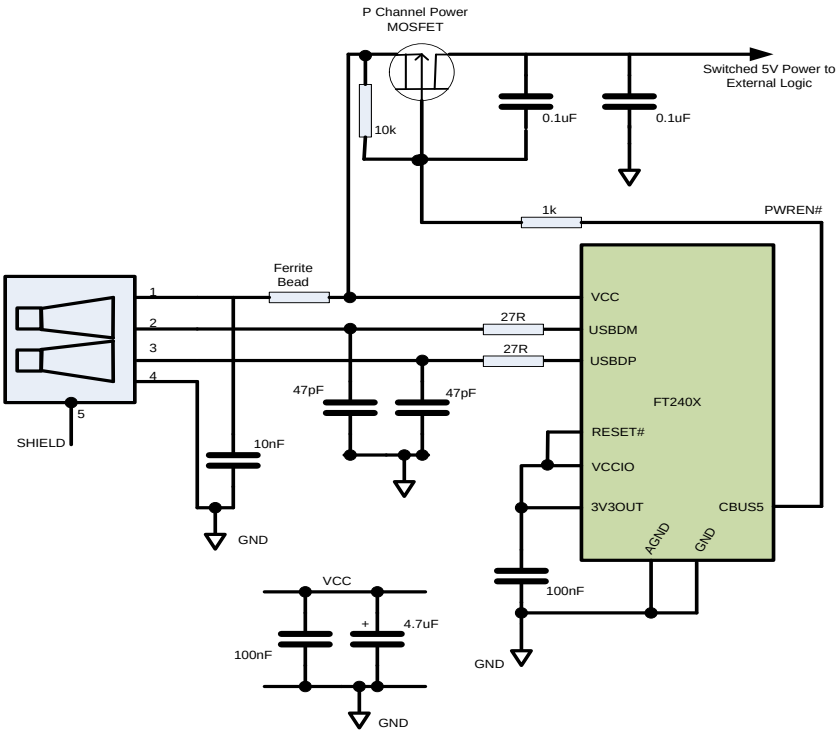


Figure 6.4 Bus Powered with Power Switching Configuration

A requirement of USB bus powered applications, is when in USB suspend mode the application draws a total current of less than 2.5mA. This requirement includes external logic. Some external logic has the ability to power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT240X provides a simple but effective method of turning off power during the USB suspend mode.

Figure 6.4 shows an example of using a discrete P-Channel MOSFET to control the power to external logic. A suitable device to do this is an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1kΩ series resistor and a 0.1µF capacitor is used to limit the current surge when the MOSFET turns on. Without the soft start circuit it is possible that the transient power surge, caused when the MOSFET switches on, will reset the FT240X or the USB host/hub controller. The soft start circuit example shown in Figure 6.4 powers up with a slew rate of approximaely12.5V/ms. Thus supply voltage to external logic transitions from GND to +5V in approximately 400 microseconds.

As an alternative to the MOSFET, a dedicated power switch IC with inbuilt "soft-start" can be used. A suitable power switch IC for such an application is the Micrel (www.micrel.com) MIC2025-2BM or equivalent.

With power switching controlled designs the following should be noted:

i) The external logic to which the power is being switched should have its own reset circuitry to automatically reset the logic when power is re-applied when moving out of suspend mode.

ii) Set the Pull-down on Suspend option in the internal FT240X MTP memory.

iii) The PWREN# pin should be used to switch the power to the external circuitry.

iv) For USB high-power bus powered applications (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the application must be set in the Max Power field in the internal FT240X MTP memory. A high-power bus powered application uses the descriptor in the internal FT240X MTP memory to inform the system of its power requirements.

v) PWREN# gets its VCC from VCCIO. For designs using 3V3 logic, ensure VCCIO is not powered down using the external logic. In this case use the +3V3OUT.

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7 Application Examples

The following sections illustrate possible applications of the FT240X. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT240XS and FT240XQ package options.

7.1 USB to MCU FIFO Interface

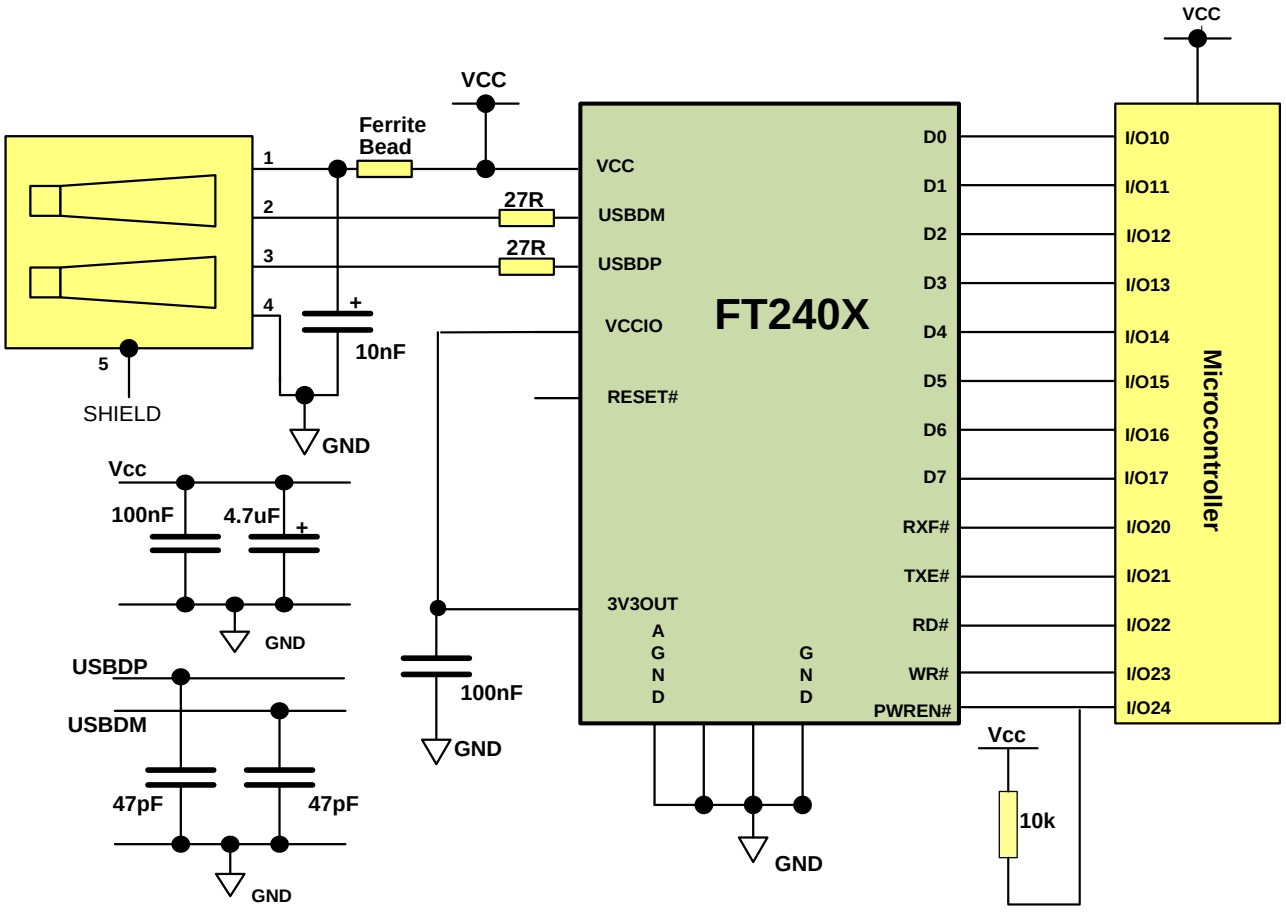


Figure 7.1 USB to MCU FIFO Interface

A typical example of using the FT240X as a USB to Microcontroller (MCU) FIFO interface is illustrated in Figure 7.1. This example uses two MCU I/O ports: one port (8 bits) to transfer data and the other port (4 or 5 bits) to monitor the TXE# and RXF# status bits and generate the RD# and WR strobes to the FT240X, when required.

Using PWREN# for this function is optional.

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7.2 Battery Charge Detection

A recent addition to the USB specification (http://www.usb.org/developers/devclass_docs/BCv1.2_011912.zip) is to allow for additional charging profiles to be used for charging batteries in portable devices. These charging profiles do not enumerate the USB port of the peripheral. The FT240X device will detect that a USB compliant dedicated charging port (DCP) is connected. Once detected while in suspend mode a battery charge detection signal is provided to allow external logic to switch to charging mode as opposed to operation mode.

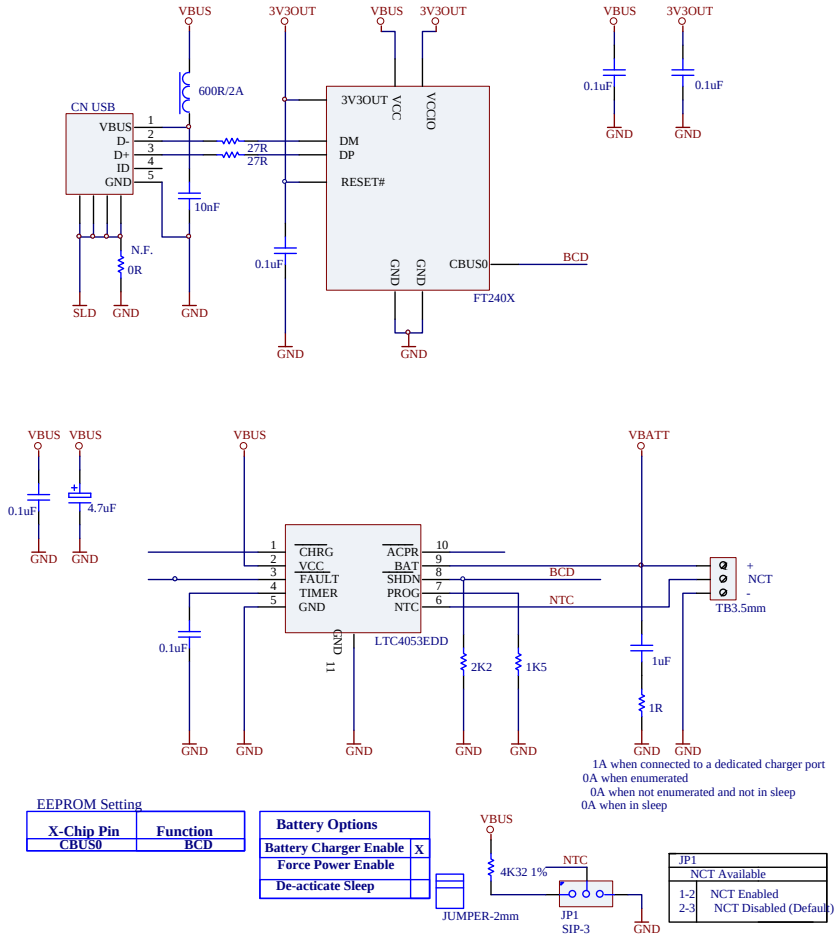


Figure 7.2 USB Battery Charging Detection (1 pin)

To use the FT240X with battery charging detection the CBUS pins must be reprogrammed to allow for the BCD Charger output to switch the external charger circuitry on. The CBUS pins are configured in the internal MTP memory with the free utility FTPROG. If the charging circuitry requires an active low signal to enable it, the CBUS pin can be programmed to BCD Charger# as an alternative.

When connected to a USB compliant dedicated charging port (DCP, as opposed to a standard USB host) the device USB signals will be shorted together and the device suspended. The BCD charger signal will bring the LTC4053 out of suspend and allow battery charging to start. The charge current in the example above is 1A as defined by the resistance on the PROG pin.

Alternatively the PWREN# And SLEEP pins may be used to control the LTC4053 such that a battery may be charged from a standard host (low current) or from a dedicated charging port (high current). In such a design as shown above the charge current would need to be limited to 0.4A to ensure that the USB host power limit is not exceeded.

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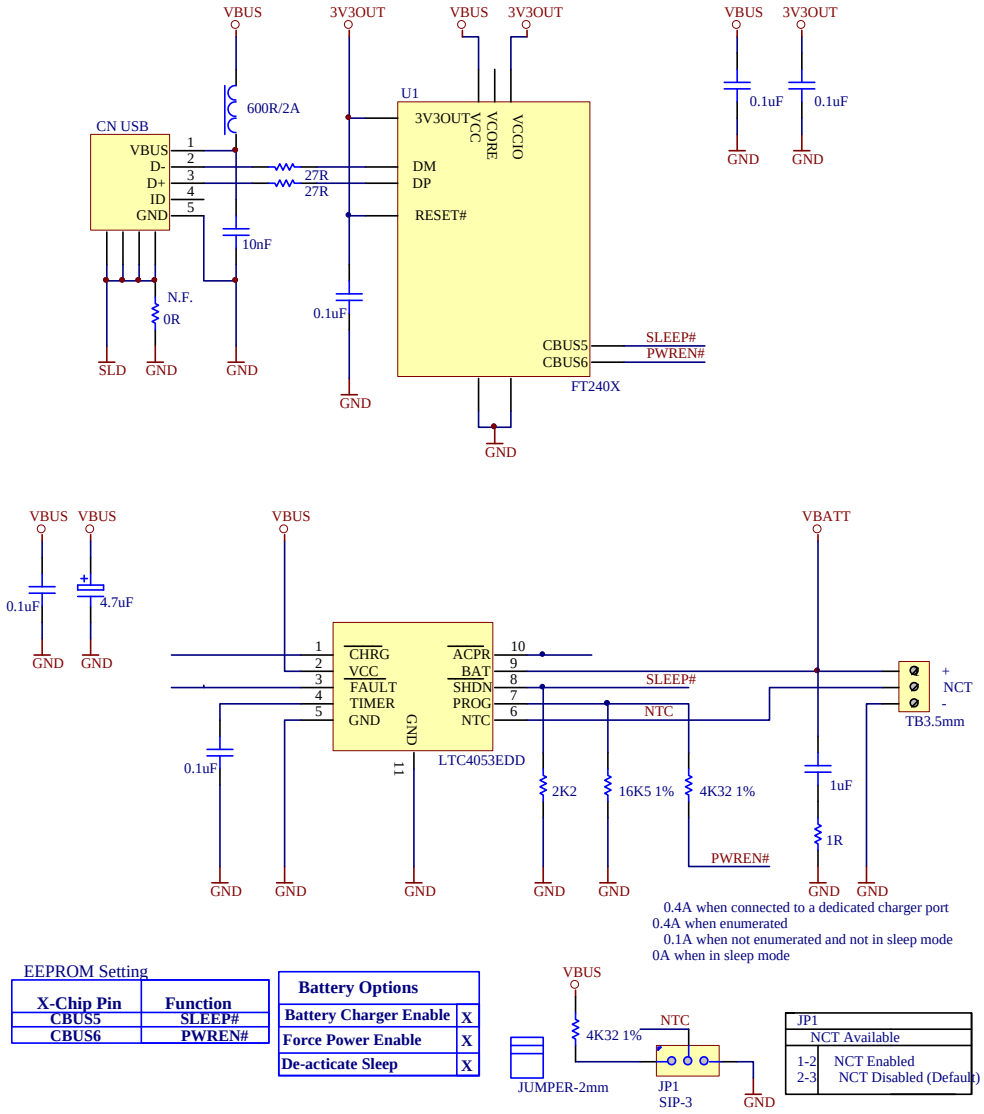


Figure 7.3 USB Battery Charging Detection (2 pin)

In the example above the FT240X SLEEP pin is used to enable/disable the LTC4053, while the PWREN# signal alters the charging current by altering the resistance on the LTC4053 PROG pin.

To calculate the equivalent resistance on the LTC4053 PROG pin select a charge current, then Res = $1500V/I_{chg}$

For more configuration options of the LTC4053 refer to:

AN_175_Battery Charging Over USB

Note: If the FT240X is connected to a standard host port such that the device is enumerated the battery charge detection signal is inactive as the device will not be in suspend.

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8 Internal MTP Memory Configuration

The FT240X includes an internal MTP memory which holds the USB configuration descriptors, other configuration data for the chip and also user data areas. Following a power-on reset or a USB reset the FT240X will scan its internal MTP memory and read the USB configuration descriptors stored there.

In many cases, the default values programmed into the MTP memory will be suitable and no re-programming will be necessary. The defaults can be found in Section 8.1.

The MTP memory in the FT240X can be programmed over USB if the values need to be changed for a particular application. Further details of this are provided from section 8.2 onwards.

Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. See TN_100 – USB Vendor ID/Product ID Guidelines for more details.

8.1 Default Values

The default factory programmed values of the internal MTP memory are shown in Table 8.1.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6015h	FTDI default PID (hex)
Serial Number Enabled	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the MTP memory during device final test.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the FIFO interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	FT240X USB FIFO	
Max Bus Power Current	90mA	
Power Source	Bus Powered	
Device Type	FT240X	
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake Up	Disabled	Taking SIWU# low will wake up the USB host controller from suspend in approximately 20 ms. When enabled.
DBUS Drive Current Strength	4mA	Options are 4mA, 8mA, 12mA, 16mA
DBUS slew rate	Slow	Options are slow or fast

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Parameter	Value	Notes
DBUS Schmitt Trigger Enable	Normal	Options are normal or Schmitt
CBUS Drive Current Strength	4mA	Options are 4mA, 8mA, 12mA, 16mA
CBUS slew rate	Slow	Options are slow or fast
CBUS Schmitt Trigger Enable	Normal	Options are normal or Schmitt
High Current I/Os	Disabled	Enables the high drive level on the FIFO data bus and control I/O pins.
Load VCP Driver	Disabled	Enabling this will load the VCP driver interface for the device.
CBUS5	VBUS_Sense	Used to detect when the device is connected to a USB host and power is available.
CBUS6	Keep_Awake#	Prevents the device from entering suspend state when unplugged.

Table 8.1 Default Internal MTP Memory Configuration

8.2 Methods of Programming the MTP Memory

8.2.1 Programming the MTP memory over USB

The MTP memory on all FT-X devices can be programmed over USB. This method is the same as for the EEPROM on other FTDI devices such as the FT232R. No additional hardware, connections or programming voltages are required. The device is simply connected to the host computer in the same way that it would be for normal applications, and the FT_Prog utility is used to set the required options and program the device.

The FT_Prog utility is provided free-of-charge from the FTDI website, and can be found at the link below. The user guide is also available at this link. Note that the FT-X devices require FT_Prog version 2.5 or later.

http://www.ftdichip.com/Support/Utilities.htm#FT_Prog

Additionally, D2XX commands can be used to program the MTP memory from within user applications. For more information on the commands available, please see the D2XX Programmers Guide below.

http://www.ftdichip.com/Support/Documents/ProgramGuides/D2XX_Programmer's_Guide(FT_000071).pdf

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8.3 Memory Map

The FT-X family MTP memory has various areas which come under three main categories:

- User Memory Area
- Configuration Memory Area (writable)
- Configuration Memory Area (non-writable)

Memory Area Description	Word Address
User Memory Area 2 Accessible via USB	0x3FF - 0x80
Configuration Memory Area Accessible via USB	0x7E - 0x50
Configuration Memory Area Cannot be written	0x4E - 0x40
User Memory Area 1 Accessible via USB	0x3E - 0x12
Configuration Memory Area Accessible via USB	0x10 - 0x00

Figure 8.1: Simplified memory map for the FT-X

User Memory Area

The User Memory Areas are highlighted in Green on the memory map. They can be read and written via USB on the FT240X. All locations within this range are freely programmable; no areas have special functions and there is no checksum for the user area.

Note that the application should take into account the specification for the number of write cycles in Section 5.4 if it will be writing to the MTP memory multiple times.

Configuration Memory Area (writable)

This area stores the configuration data for the device, including the data which is returned to the host in the configuration descriptors (e.g. the VID, PID and string descriptions) and also values which set the hardware configuration (the signal assigned to each CBUS pin for example).

These values can have a significant effect on the behaviour of the device. Steps must be taken to ensure that these locations are not written to un-intentionally by an application which is intended to access only the user area.

This area is included in a checksum which covers configuration areas of the memory, and so changing any value can also cause this checksum to fail.

Configuration Memory Area (non-writable)

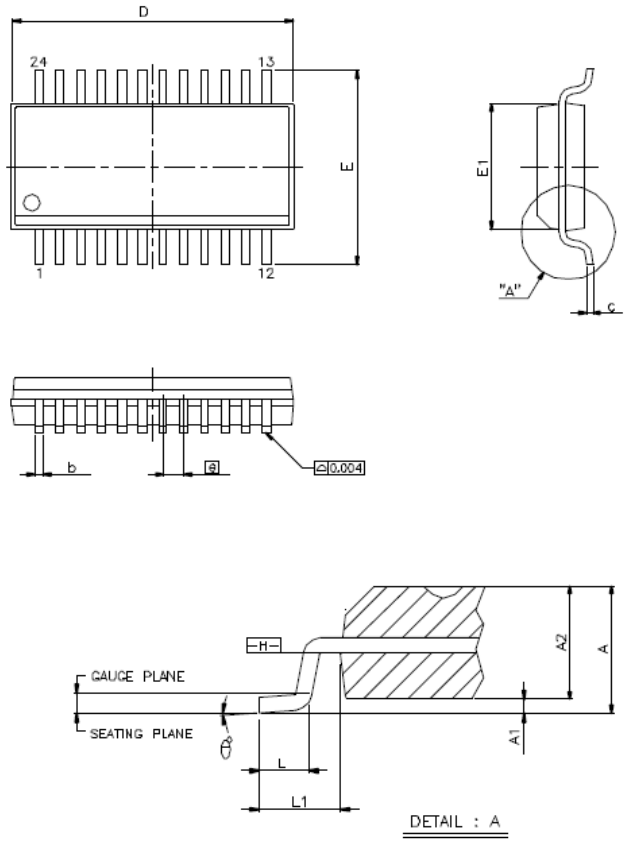
This is a reserved area and the application should not write to this area of memory. Any attempt to write these locations will fail.

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9 Package Parameters

The FT240X is available in two different packages. The FT240XS is the SSOP-24 option and the FT240XQ is the QFN-24 package option. The solder reflow profile for both packages is described in Section 9.5.

9.1 SSOP-24 Package Mechanical Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
b	0.008	–	0.012
C	0.007	–	0.010
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

NOTES:

1.JEDEC OUTLINE : MO-137 AE

2.DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST.

Figure 9.1 SSOP-24 Package Dimensions

The FT240XS is supplied in a RoHS compliant 24 pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 8.66mm x 3.91 mm body (8.66mm x 5.99mm including pins). The pins are on a 0.635 mm pitch. The above mechanical drawing shows the SSOP-24 package.

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

The code **XXXXXXXXXXXX** is the manufacturing LOT code.

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9.2 SSOP-24 Package Markings

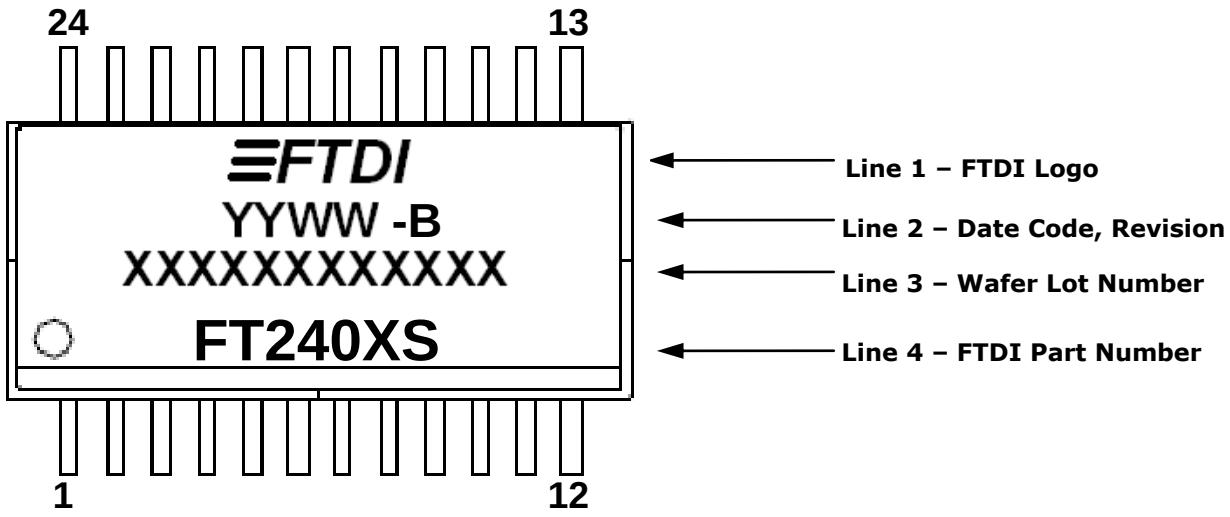


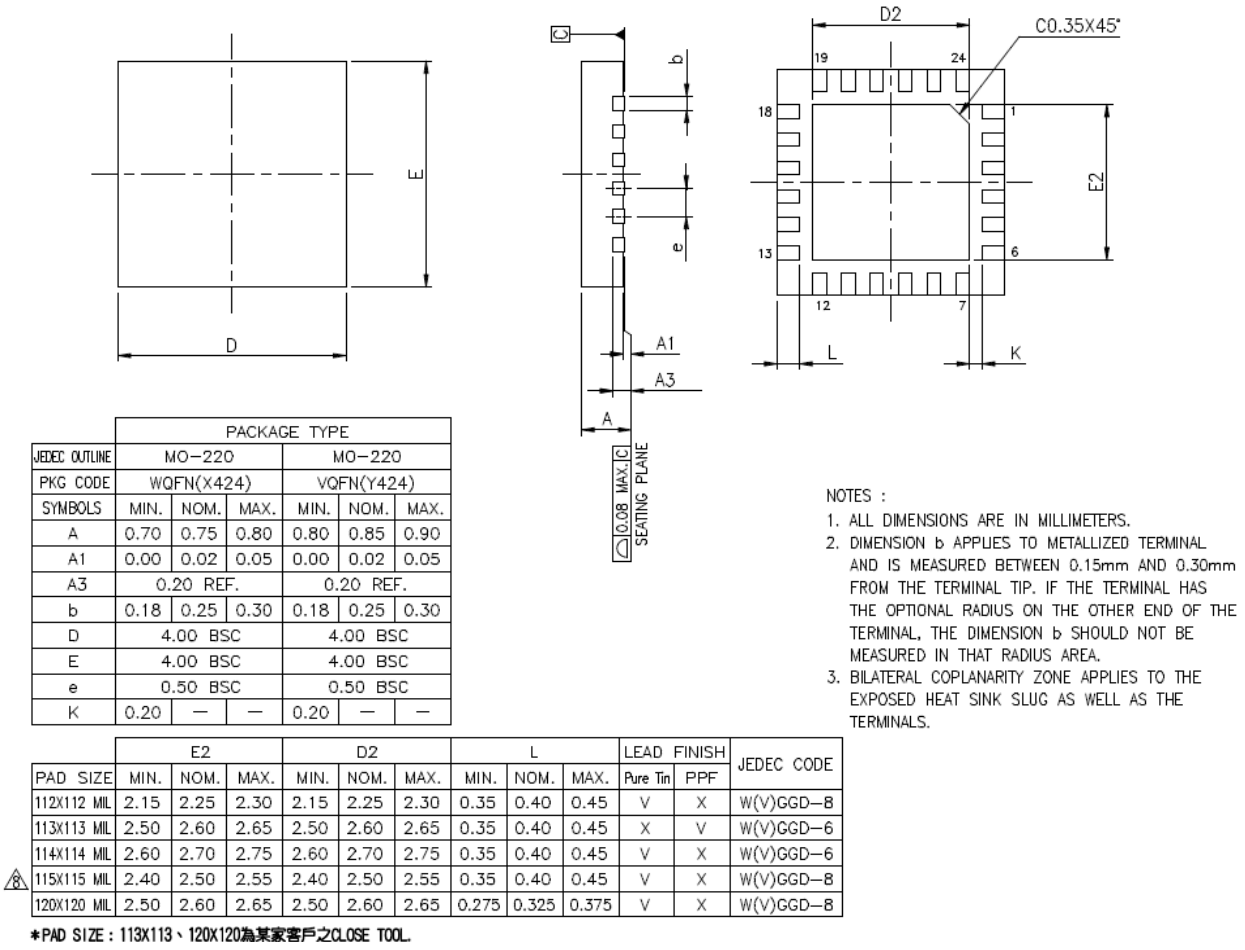
Figure 9.2 SSOP-24 Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using Greatek standard font (Roman Simplex)

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9.3 QFN-24 Package Mechanical Dimensions



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X424)			VQFN(Y424)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.18	0.25	0.30	0.18	0.25	0.30
D	4.00 BSC			4.00 BSC		
E	4.00 BSC			4.00 BSC		
e	0.50 BSC			0.50 BSC		
K	0.20	—	—	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
112X112 MIL	2.15	2.25	2.30	2.15	2.25	2.30	0.35	0.40	0.45	V	X	W(V)GGD-8
113X113 MIL	2.50	2.60	2.65	2.50	2.60	2.65	0.35	0.40	0.45	X	V	W(V)GGD-6
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75	0.35	0.40	0.45	V	X	W(V)GGD-6
115X115 MIL	2.40	2.50	2.55	2.40	2.50	2.55	0.35	0.40	0.45	V	X	W(V)GGD-8
120X120 MIL	2.50	2.60	2.65	2.50	2.60	2.65	0.275	0.325	0.375	V	X	W(V)GGD-8

*PAD SIZE : 113X113、120X120為某家客戶之CLOSE TOOL.

Figure 9.3 QFN-24 Package Dimensions

The FT240XQ is supplied in a RoHS compliant leadless QFN-24 package - WQFN(X424), with pad size 114x114. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.
This package is nominally 4.0mm x 4.0mm. The solder pads are on a 0.50mm pitch. The above mechanical drawing shows the QFN-24 package. All dimensions are in millimetres.
The centre pad on the base of the FT240XQ is internally connected to GND, and the PCB should not have tracking on the top layer in this area.

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

The code **XXXXXXX** is the manufacturing LOT code.

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9.4 QFN-24 Package Markings

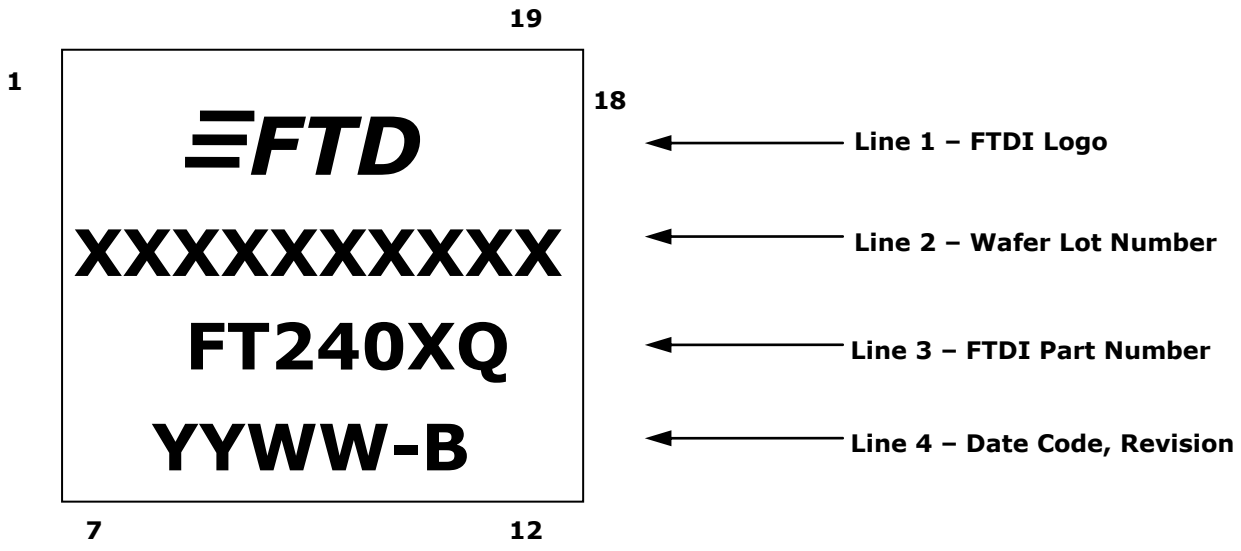


Figure 9.4 QFN-24 Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using Greatek standard font (Roman Simplex)

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9.5 Solder Reflow Profile

The FT240X is supplied in Pb free 24 LD SSOP and QFN-24 packages. The recommended solder reflow profile for both package options is shown in 9.5.

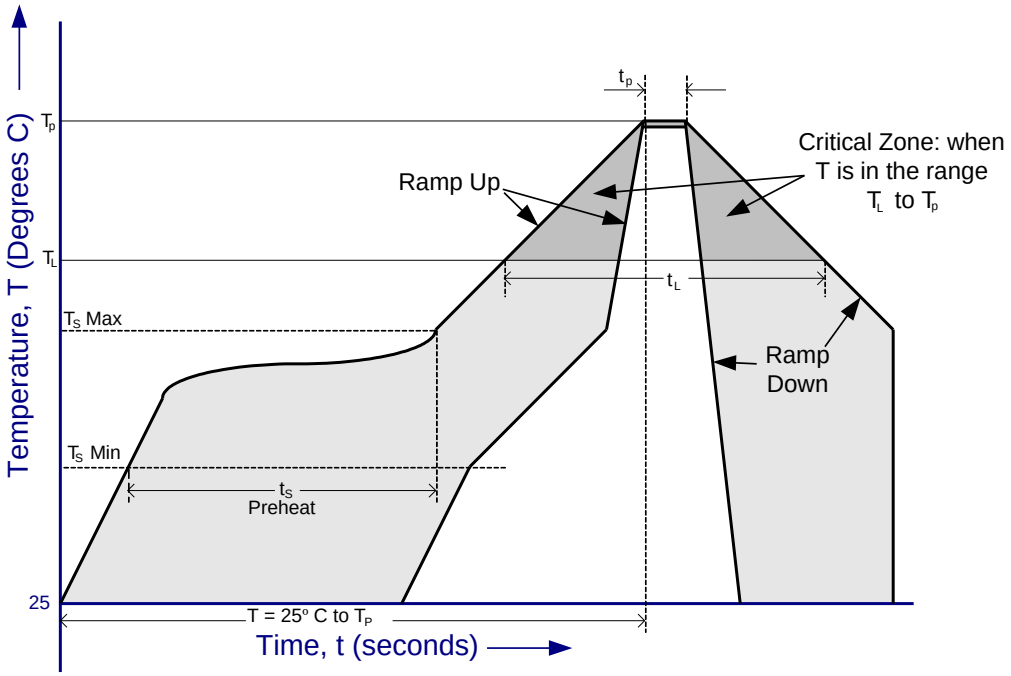


Figure 9.5 FT240X Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 9.1. Values are shown for both a completely Pb free solder process (i.e. the FT240X is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT240X is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	150°C 200°C 60 to 120 seconds	100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	217°C 60 to 150 seconds	183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 9.1 Reflow Profile Parameter Values

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Appendix A - References

Useful Application Notes

http://www.ftdichip.com/Documents/AppNotes/AN232R-01_FT232RBitBangModes.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_107_AdvancedDriverOptions_AN_000073.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_121_FTDI_Device_EEPROM_User_Area_Usage.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_120_Aliasing_VCP_Baud_Rates.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_100_Using_The_FT232_245R_With_External_Osc(FT_000067).pdf

http://www.ftdichip.com/Resources/Utilities/AN_126_User_Guide_For_FT232_Factory%20test%20utility.pdf

http://www.ftdichip.com/Documents/AppNotes/AN232B-05_BaudRates.pdf

http://www.ftdichip.com/Documents/InstallGuides.htm

http://www.ftdichip.com/Support/Documents/TechnicalNotes/TN_100_USB_VID-PID_Guidelines.pdf

http://www.ftdichip.com/Support/Documents/AppNotes/AN_175_Battery%20Charging%20Over%20USB%20with%20FTEX%20Devices.pdf

http://www.usb.org/developers/devclass_docs/BCv1.2_011912.zip

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Appendix C - Revision History

Document Title:	USB 8-BIT FIFO IC FT240X
Document Reference No.:	FT_000626
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Product Page:	http://www.ftdichip.com/FT-X.htm
Document Feedback:	Send Feedback

Version 1.0	Initial Datasheet Created	07/02/12
Version 1.1	Replaced VCC_CORE with VCORE	
	Updated 24 pin SSOP dimensions	22/02/12
Version 1.2	Clarified MTP Reliability in table 5.8	17/04/12
	Edited Table 8.1, changed "Load VCP Driver" to Disabled	
Version 1.2	Removed references to LED signals on the CBUS pins in table 3.9 as these are not available on the FT240X.	24/09/2012
Version 1.3	updated fron t page to clarify 5V tolerant	14/02/2013
	Updated TID	
	Updated US address	

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