Description

The VX-722 is a dual frequency voltage controlled crystal oscillator, VCXO, based upon Vectron's HPLL high performance phase locked loop frequency multiplier ASIC that combines key digital synthesis techniques with VI's proven core analog technology blocks. A standard low frequency crystal provides the reference to the fractional-n synthesizer so that virtually any frequency between 10MHz and 1200 MHz can be factory programmed allowing quick turn manufacturing.

Features

- Industry Standard Package, 5.0 x 7.0 x 1.8 mm
- HPLL High Performance PLL ASIC
- Jitter < 500 fs-rms (12 kHz to 20 MHz)
- Output Frequencies from 10 MHz to 1200 MHz
- Spurious Suppression, 70 dBc Typical
- 2.5V or 3.3V Supply Voltage
- LVCMOS, LVPECL or LVDS Output Configurations
- Output Enable
- Compliant to EC RoHS Directive

Applications

PLL circuits for clock smoothing and frequency translation

Description	Standard
1-2-4 Gigabit Fibre Channel	INCITS 352-2002
10 Gigabit Fibre Channel	INCITS 364-2003
10GbE LAN / WAN	IEEE 802.3ae
Synchronous Ethernet	ITU-T G.8262
OC-192	ITU-T G.709
SONET / SDH	GR-253-CORE Issue4

Block Diagram

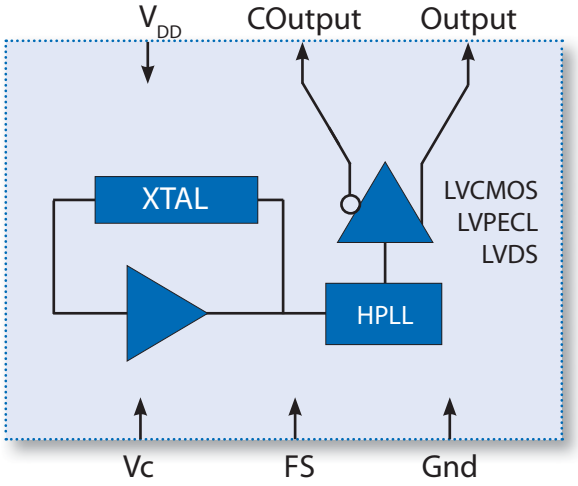

Figure 1 - Block Diagram

Performance Specifications

Electrical Performance

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Supply						
Voltage[1]	3.3V Option 2.5V Option	V_{DD}	2.97 2.25	3.3 2.5	3.63 2.75	V
Current	LVCMOS LVDS LVPECL	I_{DD}	- - -	90 99 120	98 108 130	mA
Operating Temperature [1, 3]		T_{OP}	-40	-	+85	°C
Output Enable (OE)	V_{IH}		0.75 x V_{DD}	-	-	V
	V_{IL}		-	-	0.5	
Frequency Select (FS)	V_{IH}		0.75 x V_{DD}	-	-	V
	V_{IL}		-	-	0.5	
Frequency						
Nominal Frequency[1]	LVPECL/LVDS LVCMOS	f_N	10 10	- -	1200 160	MHz
Absolute Pull Range [1, 2, 3]	V_C = 0.1xV_{DD} to 0.9xV_{DD}	APR	±50	-	-	ppm
Linearity [2, 4]	20% to 80% full output	Lin	-	-	±10	%
Gain Transfer [2,]	10 to 90% of V_{DD}	K_V	-	+100	-	ppm/V
Temperature Stability [1, 6]	T_A = -40 to +85°C	f_{STAB}	-	±20	-	ppm
Outputs						
LVPECL Output	mid-level	V_O	V_{DD}-1.42	-	V_{DD}-1.25	V
	swing (diff)	V_{OD}	1.1	-	1.9	V_{PP}
LVDS Output	mid-level	V_O	1.4	1.6	1.8	V
	swing (diff)	V_{OD}	300	450	600	mV_{PP}
LVCMOS Output		V_{OH}	0.9 x V_{DD}	-	V_{DD}	V
		V_{OL}	-	-	0.1 x V_{DD}	V
Rise/Fall Time (20/80%)[2,5]	LVPECL/LVDS LVCMOS with C_L = 15	t_R/t_f	- -	- -	350 1.2	ps ns
Symmetry [2,3]	LVPECL: V_{DD}-1.3 V (diff) LVDS: 1.6 V (diff) LVCMOS: V_{DD}/2	SYM	45	50	55	%
Spurious Suppression [6]			65	70	-	dBc
Jitter [6] (Performance Option N)	12 kHz to 20 MHz	ϕJ	-	-	1000	fs-rms
Jitter [6] (Performance Option A)	12 kHz to 20 MHz	ϕJ	-	-	500	fs-rms
Control Voltage						
Input Impedance (Output Enabled) [6]		Z_C	500	-	-	kΩ
Modulation Bandwidth		BW	-	10.0	-	kHz
Control Voltage Tuning Range		V_C	0	-	V_{DD}	V

1] See Standard Frequencies and Ordering Information (Pg 8).
2] Parameters are tested with production test circuit (See Figure 2 for LVCMOS, Figure 3 for LVPECL and figure 4 for LVDS).
3] Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4] Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5] Parameters are described with waveform diagram below (Figure 5).
6] Not tested in production, guaranteed by design, verified at qualification.

Test Circuits & Output Waveform

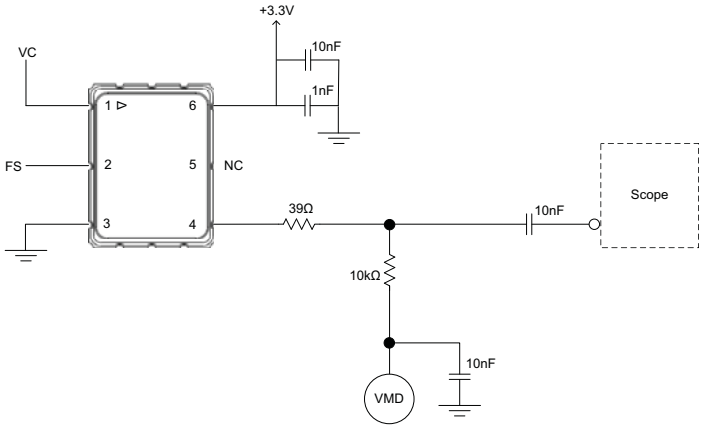

Figure 2 - LVCMOS Production Test Circuit

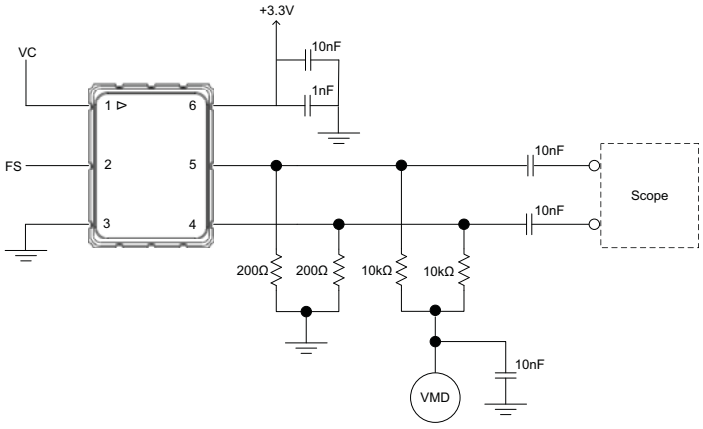

Figure 3 - LVPECL Production Test Circuit

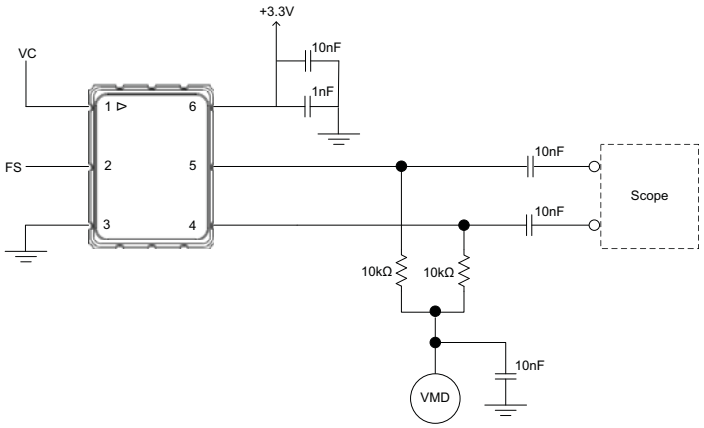

Figure 4 - LVDS Production Test Circuit

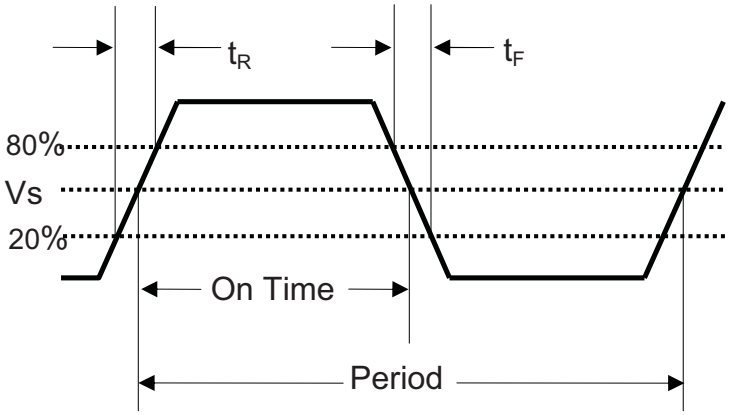

Figure 5 - Waveform Diagram

Absolute Maximum Ratings			
Parameter	**Symbol**	**Ratings**	**Unit**
Power Supply	V_{DD}	0 to 3.8	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{DD}	V
Output Enable	OE	0 to V_{DD}	V
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature / Duration	T_{PEAK} / t_P	260 / 40	°C / sec

LVPECL Application Diagrams

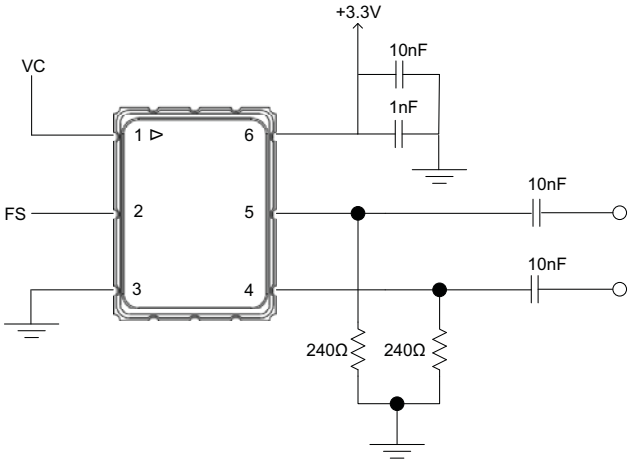

Figure 6 - Single Resistor Termination Scheme

Resistor values are typically 120 to 240 ohms for 3.3V operation and 82 to 120 ohms for 2.5V operation.

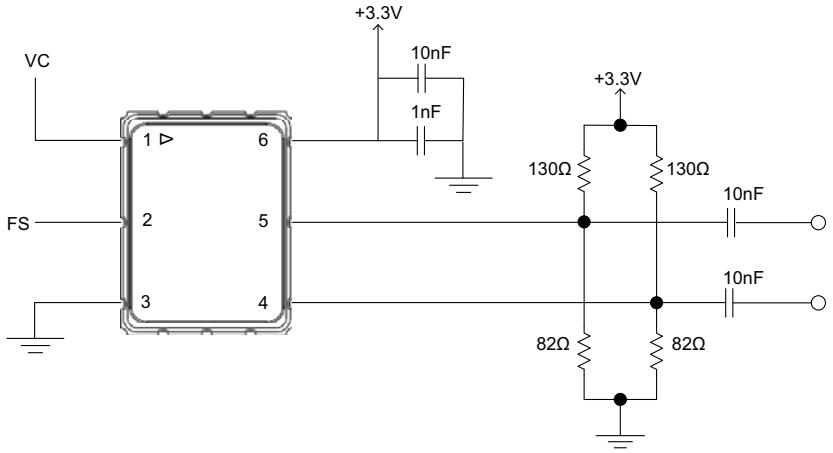

Figure 7 - Pull Up Pull Down Termination

Resistor values are typically for 3.3V operation
For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 240 ohms

There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 6, and a pull-up/pull-down scheme as shown in Figure 7. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

LVDS Application Diagrams

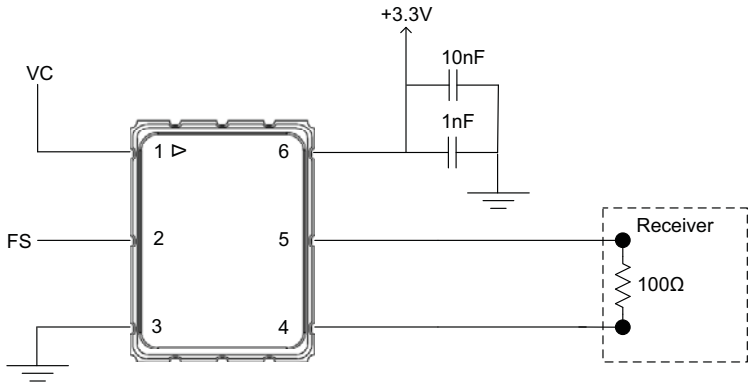

Figure 8 - LVDS to LVDS, internal 100Ω

Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.

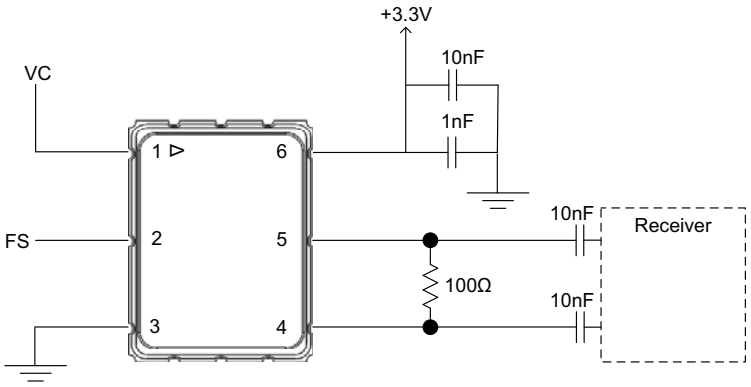

Figure 9 - LVDS to LVDS, External 100Ω and AC block ing caps

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

Typical Characteristics

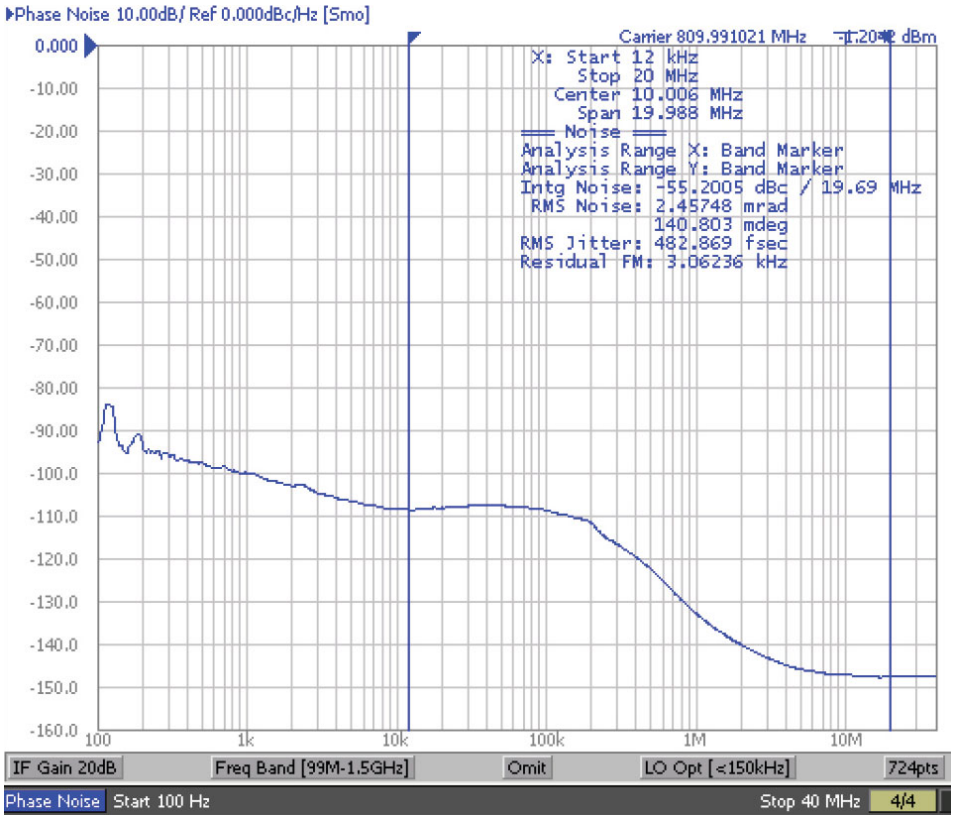

Figure 10 - Typical Phase Noise/Jitter Performance - INTEGER Mode

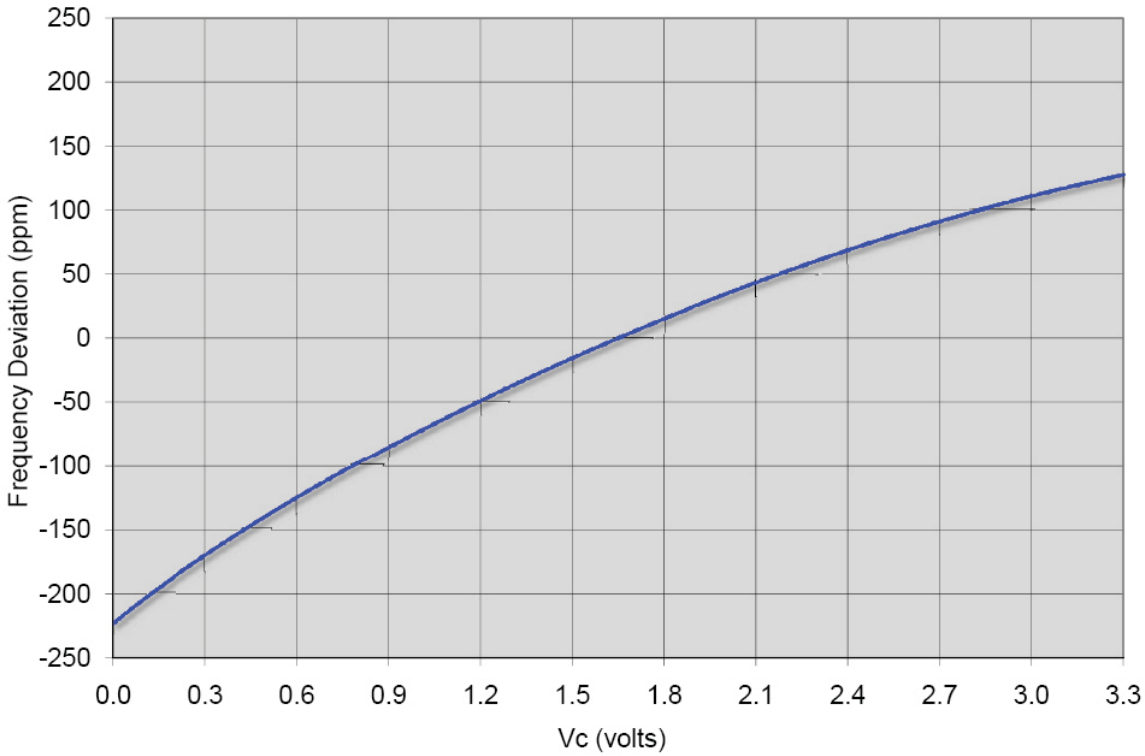

Figure 11 - Typical VC Pull

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Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VX-722 family is capable of meeting the following qualification tests:

Environmental Compliance	
Parameter	**Conditions**
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/JEDEC J-STD-020, MSL1

Handling Precautions

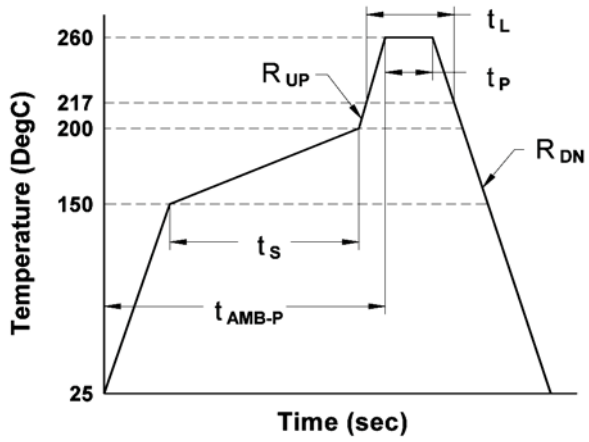
Although ESD protection circuitry has been designed into the VX-722 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	**Minimum**	**Conditions**
Human Body Model	1000V	MIL-STD-883, Method 3015
Charged Device Model	900V	JEDEC, JESD22-C101
Machine Model	200 V	JEDEC, JESD22-A115-A

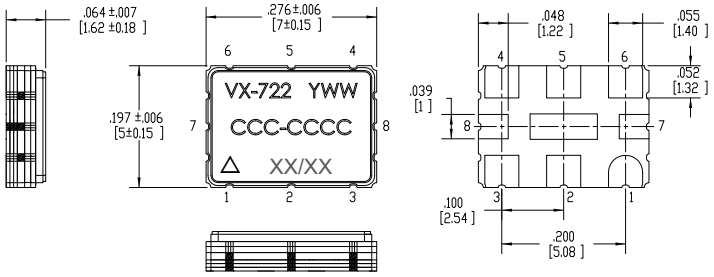
Reflow Profile (IPC/JEDEC J-STD-020)		
Parameter	**Symbol**	**Value**
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VX-722 device is hermetically sealed so an aqueous wash is not an issue.

Terminal Plating: Electrolytic Ni > 1.9µm
Electrolytic Au > 0.7µm



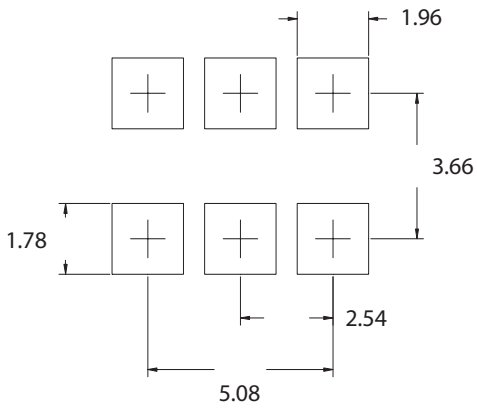
Outline & Marking Diagram



Y = Year
WW = Week
C = Option Codes
XX/XX = Frequency1/Frequency2
(See Ordering Info)

mm
[inch]

Suggested Pad Layout

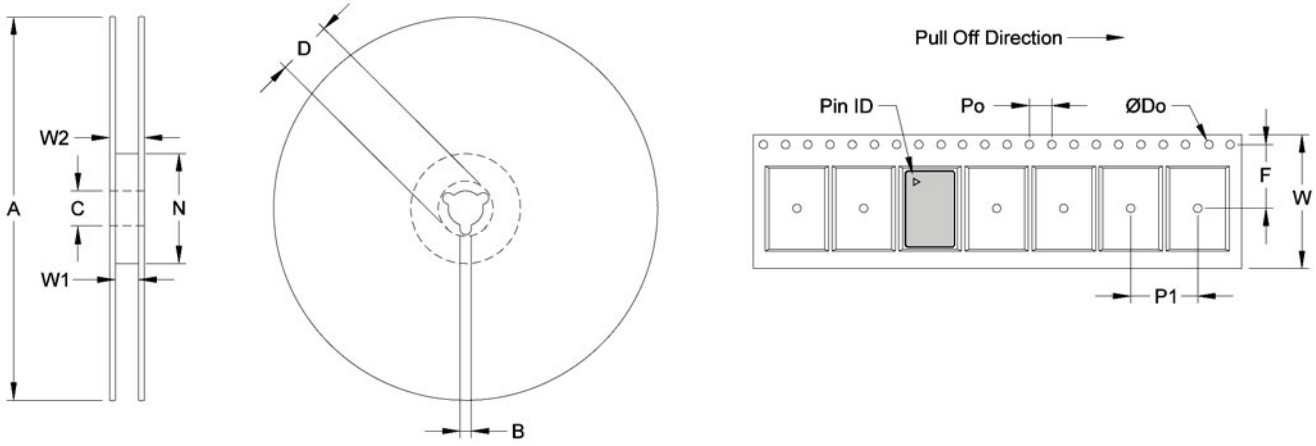


Pin Out		
Pin	**Symbol**	**Function**
1	V_C	Control Voltage
2	FS	Frequency Select[1]
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput (N/A for LVCMOS)	Complementary Output (N/C for LVCMOS)
6	V_{DD}	Power Supply Voltage

1: Frequency Select is internally pulled to V_{DD} with a 30 kΩ resistor.

Frequency Select		
FS	**Voltage Range**	**Result**
H	$(5V_{CC} / 6)$ to V_{CC}	F2
M	$(V_{CC}/2)$ ±15% $(V_{CC}/2)$	Output Disable
L	Gnd to $(V_{CC}/6)$	F1

Tape & Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# Per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	
VX-722	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Standard Frequency Table

Standard Factory Configurable Frequencies (MHz)											
18.7500000	EE	39.0625000	HH	73.7280000	K8	173.370748	ND	622.080000	P2	781.250000	T9
19.2000000	DD	39.3216000	HD	74.1250000	K1	173.437500	NP	624.693800	PD	796.875000	TB
19.3926580	DX	39.8437500	HJ	74.1758000	KA	176.838175	NA	624.704800	P6	800.000000	TK
19.4400000	D6	40.0000000	JF	74.2500000	K7	182.016000	N8	625.000000	P3	805.664100	TA
19.5312500	DZ	40.2830630	KK	75.0000000	KH	182.857142	NM	627.329600	P7	809.063500	TE
19.6608000	DB	40.9600000	J1	76.8000000	K4	184.000000	NG	629.987800	PA	819.200000	TH
19.6989680	DK	41.0888870	KM	77.7600000	K2	184.320000	NH	637.500000	PG	821.777300	TF
19.7190000	DH	41.6571440	KP	78.0000000	LH	187.500000	N5	640.000000	PN	850.000000	TJ
19.9218750	ED	41.6600000	LM	78.1250000	K3	195.000000	N7	644.531250	P4	983.400000	TU
20.0000000	E2	41.8329130	KT	78.6432000	K5	200.000000	NE	645.120000	RJ	1,000.0000	TM
20.1416000	E3	42.0000000	JB	79.6875000	KG	200.192000	N6	647.239400	PE		
20.4800000	E4	42.0101690	KV	80.0000000	K9	201.416020	N1	647.250800	PK	Recent Adds:	
20.5444340	EF	42.5000000	JC	80.5664130	KJ	212.500000	NF	649.970300	PF	174.703083	NX
20.7135000	E1	42.6600000	JZ	82.1777380	KL	219.429571	NL	657.421875	PB	175.000000	W2
20.8285720	EG	44.2095440	KX	82.9440000	K6	240.000000	NR	665.625600	PC	698.812330	VC
20.8286000	EB	44.4343000	LF	83.3142880	KN	243.000000	NC	666.514286	P5		
20.9165460	EH	44.6218000	JW	83.6658250	KR	245.760000	N9	669.128100	R2		
21.0050840	EJ	44.7360000	J3	84.0203380	KU	250.000000	NT	669.326582	R3		
22.0000000	E9	44.9280000	JE	86.6853740	LJ	252.571428	NJ	669.642900	R1		
22.1047720	EK	45.1584000	JG	88.4190880	KW	256.000000	NK	670.838600	R7		
22.2171000	E5	45.8240000	JM	95.7000000	LK	262.144000	NB	672.000000	RT		
22.5792000	E8	46.0379460	LG	97.5000000	KE	292.571429	NN	672.156250	TX		
24.0000000	EC	46.7200000	JK	100.000000	L8	300.000000	PT	672.162712	R5		
24.5760000	E6	46.8750000	JY	105.000000	L6	307.200000	RX	673.456600	RA		
24.7040000	E7	48.0000000	JV	106.250000	L9	311.040000	P1	684.255400	R9		
25.0000000	F7	49.1520000	J7	108.000000	LA	312.500000	PU	687.700000	TV		
25.1658000	F8	49.4080000	J2	110.000000	L1	318.750000	PV	690.569196	R4		
25.6000000	F6	50.0000000	JD	112.000000	L2	320.000000	PP	693.468750	RV		
25.9200000	F2	50.0480000	KD	114.000000	L3	322.265650	PW	693.482991	R6		
26.0000000	F3	51.2000000	LL	120.000000	LC	328.710950	PX	693.750000	R8		
27.0000000	F4	51.8400000	J4	122.880000	LB	333.257150	PY	696.390625	RW		
27.6480000	FB	52.0000000	JP	124.416000	L7	334.663300	RB	696.421478	V1		
28.7040000	F1	53.3300000	JU	125.000000	L4	336.081350	RC	696.421875	TY		
29.4912000	F5	54.7460000	JL	130.000000	LD	353.676350	RD	704.380600	TG		
29.5000000	F9	55.0000000	JX	131.072000	LN	368.640000	RY	707.352700	TC		
30.0000000	HE	60.0000000	JR	139.264000	L5	375.000000	RF	707.500000	V2		
30.7200000	H1	61.3800000	KY	150.000000	M8	382.800000	RU	710.948600	T2		
30.8800000	HF	61.4400000	J5	150.144000	M6	400.000000	RR	712.520000	TW		
31.2500000	H8	62.2080000	J8	153.600000	MA	409.600000	RE	716.573200	T1		
32.0000000	H2	62.5000000	J9	155.520000	M2	491.520000	PM	718.750000	T5		
32.7680000	H3	62.9145000	LE	156.250000	M3	500.000000	RK	719.734400	T3		
33.0000000	H7	63.3600000	JJ	159.375000	M7	505.000000	V3	737.280000	TL		
33.3330000	HC	63.8976000	JN	160.000000	M1	531.000000	PH	739.200000	TT		
34.3680000	H6	64.0000000	JT	161.132813	M4	531.250000	P8	742.500000	V4		
34.5600000	HB	64.1520000	JH	164.355475	M9	568.928600	PJ	748.070900	T6		
36.8640000	HG	65.5360000	J6	166.628572	M5	569.196400	P9	750.000000	T7		
37.0560000	H4	66.0000000	JA	167.331646	N2	588.000000	RH	768.000000	TN		
37.1250000	H9	70.0000000	KB	168.040678	N3	595.056000	PL	777.600000	T4		
37.5000000	HK	70.6560000	KC	170.000000	N4	600.000000	PR	779.568600	T8		
38.8800000	H5	71.6100000	KF	172.500000	NU	614.400000	RG	780.881000	TD		

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Rev2: 14 November 2012

Ordering Information

VX - 722 - E C E - K E N A - F1/F2

Product Family
VX: VCXO

Package
722: 5 x 7 x 1.8 mm
Dual

Supply
E: 3.3 V
H: 2.5 V

Output
A: LVCMOS
C: LVPECL
D: LVDS

Operating Temperature
T: 0/70°C
E: -40/85 °C

Frequency (See Table)
F1, F2

Performance Options
N: Standard
A: < 500 fs-rms Jitter

Future
N: N/A

Stability
X: Standard
E: ±20ppm Temperature Stability

Absolute Pull Range
K: ± 50 ppm

Example: VX-722-ECE-KXCN-PH/T6

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