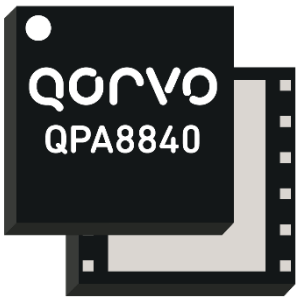
QPA8840

75 Ω 22dB CATV Amplifier (50 – 1800 MHz)

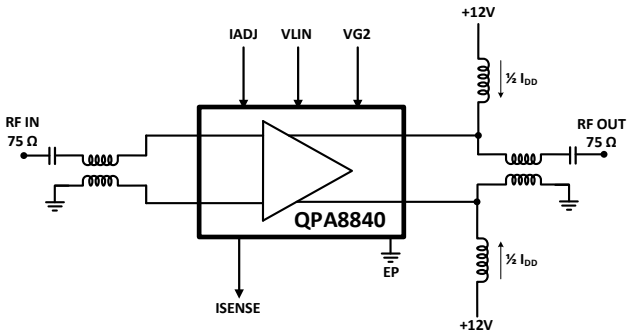
Product Overview

The QPA8840 is a an ultra-linear, 22dB Gain, GaAs amplifier, intended for mid or output stage amplification in CATV infrastructure applications. The QPA8840 operates off a 12 Volt, 425 mA supply. The device features a push-pull cascode design which provides flat gain along with ultra-low distortion from 50MHz to 1.8GHz.



12 pin 6 x 6 Laminate Module

Functional Block Diagram



Key Features

- 50 MHz to 1800 MHz Operation
- 12 V Operation
- Gain: 22 dB Typical
- OP1dB: 32 dBm Typical
- Noise Figure: 3.1 dB Typical
- RoHS Compliant

Applications

- DOCSIS 4.0 Amplifiers
- DOCSIS 4.0 Optical Nodes
- Broadband Hybrid CATV Modules

Ordering Information

Part Number	Description
QPA8840EVB-01	Evaluation Board
QPA8840SB	Sample bag with 5 pieces
QPA8840SR	7” Reel with 100 pieces
QPA8840TR13	13” Reel with 2500 pieces

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Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	+16 V
Supply Current (I_{DD})	550 mA
Maximum Input Level	+70 dBmV
Operating Temperature Range	-40 to +100 °C
Storage Temperature Range	−65 to +150 °C
Maximum Junction Temperature	+150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Electrical Specifications at 12 V

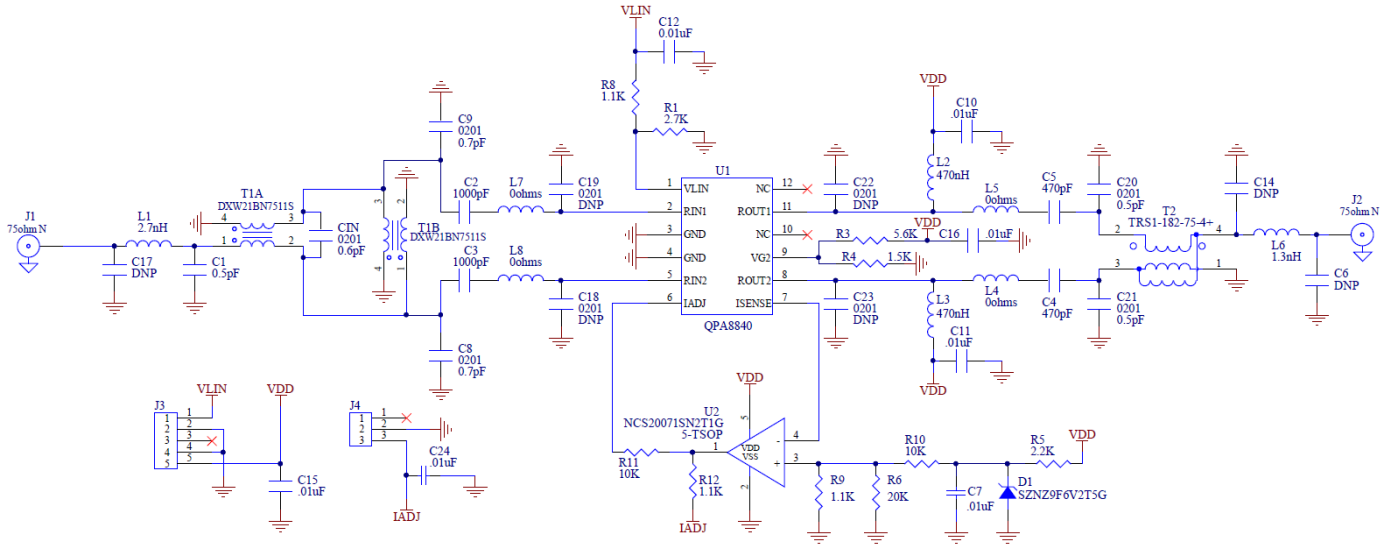
Parameter	Condition [1]	Min	Typ	Max	Unit
Supply Voltage (V_{DD})			12		V
Supply Current (I_{DD})			425		mA
Frequency Range		50		1800	MHz
Gain			22		dB
Gain Slope			1		dB
Reverse Isolation			25		dB
Input Return Loss			20		dB
Output Return Loss			18		dB
P_{OUT}	45dB MER, Source Corrected		68.6		dBmV Total Composite Power
	42dB MER, Source Corrected		69.3		
Noise Figure	50 – 250 MHz		2.8		dB
	250 – 1250 MHz		3.1		
	1250 – 1800 MHz		4.2		
OIP2L[2]	50 – 250 MHz		82		dBm
	250 – 1250 MHz		75		
	1250 – 1800 MHz		81		
OIP2U[2]	50 – 250 MHz		81		dBm
	250 – 1250 MHz		67		
	1250 – 1800 MHz		73		
OIP3[2]	50 – 250 MHz		48		dBm
	250 – 1250 MHz		47.7		
	1250 – 1800 MHz		42.3		
OP1dB	50 – 1250 MHz		32.1		dBm
	1250 – 1800 MHz		30.0		
Thermal Resistance	Θ_{JC}		8		˚C/W

Notes:

1) Typical performance at these conditions: Temp = +25 °C, V_{DD} = +12V, 75 Ω system, Full band unless otherwise noted.
2) 15dBm/tone output.
3) 108MHz to 1791MHz, 20dB tilt, 280 Ch. SC-QAM, ITU-T J.83, Annex B

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Evaluation Board Schematic 50 MHz – 1800 MHz

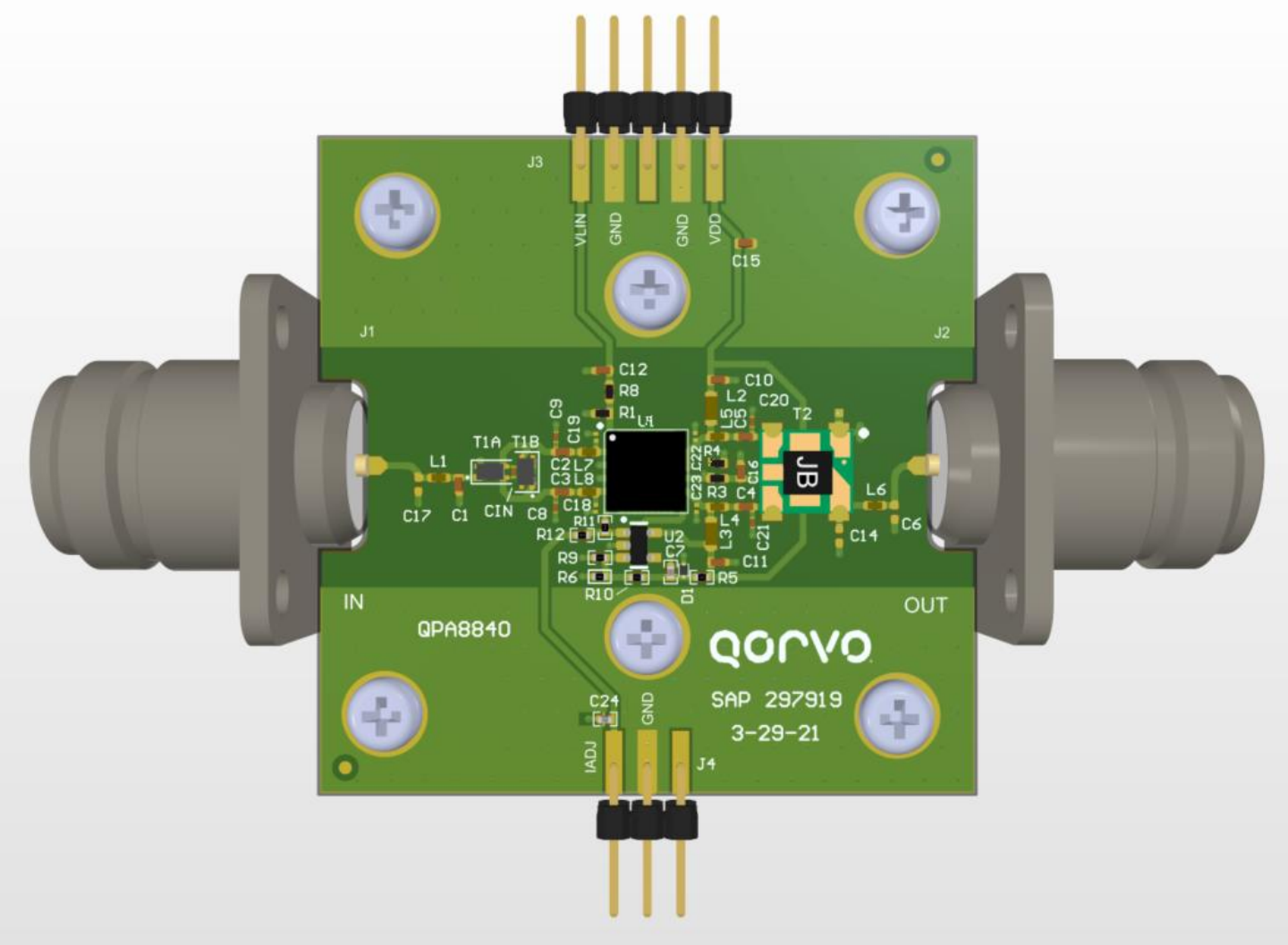


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Reference Designator	Description	Manufacturer	Part Number
U1	1.8GHz 12 V Power Doubler MMIC 22dB Gain	Qorvo	QPA8840
U2	IC, OP AMP, GP, 1-CIR, 2.7-36V, 5TSOP	On Semi	NCS20071SN2T1G
PCB	QPA8840 Evaluation Board Assembly	TTM Technologies	QPA8840-4000(A)
C1	CAP, 0.5pF, +/-0.25pF, 50V, HI-Q, 0402	Murata	GJM1555C1HR50CB01D
CIN	CAP, 0.6pF, +/-0.1pF, 25V, HI-Q, 0201	Murata	GJM0335C1ER60BB01D
C8, C9	CAP, 0.7pF,+/-0.1pF,25V,HI-Q,0201	Murata	GJM0335C1ER70BB01D
C20, C21	CAP, 0.5pF, +/-0.1pF, 25V, C0G, 0201	Murata	GRM0335C1ER50BA01D
C7, C10, C11, C12, C15, C16, C24	CAP, 0.01uF, 10%, 50V, X7R, 0402	Murata	GCM155R71H103KA55D
C2, C3	CAP, 1000pF, 10%, 50V, X7R, 0402	TDK	CGA2B2X7R1H102K050BA
C4, C5	CAP, 470pF, 10%, 0402, X7R, 50V, NISN	Murata	GCM155R71H471KA37D
L4, L5, L7, L8	RES, 0 OHM, 5%, 1/10W, 0402	Kamaya	RMC1/16SJPTH
R4	RES, 1.5K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-152JTH
R5	RES, 2.2K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-222JTH
R1	RES, 2.7K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-272JTH
R3	RES, 5.6K, 5%, 1/10W, 0402	Kamaya	RMC1/16S-562JTH
R10, R11	RES, 10K, 5%, 1/16W, 0402	Kamaya	RMC1/16S-103JTH
R6	RES, 20K, 1%, 1/16W, 0402	Vishay	CRCW040220K0FKED
R8, R9, R12	RES, 1.1K, 5%, 1/16W, 0402	Panasonic	ERJ-2GEJ112
D1	DIO, ZENR, 6.2V, 5mA ,250mW, SOD-923, SD	On Semi	SZNZ9F6V2T5G
L1	IND, 2.7nH, +/-0.3nH, M/L, 0402	Murata	LQG15HS2N7S02D
L6	IND, 1.3nH, ±0.1nH, 1000mA, M/L, 0402	Murata	LQG15HS1N3B02D
L2, L3	IND, 470nH, 5%, 0.42A, W/W, 0603	Coilcraft	0603LS-471XJLC
T1A, T1B	BALUN, 1.8GHz, 75 / 75 OHM, 0805	Murata	DXW21BN7511SL
T2	XFMR, 1:1, 10 – 1800 MHz, 75 OHM, SMD	Minicircuits	TRS1-182-75-4+
J1, J2	CONN, COAXIAL, SKT, 75 OHM, 1.8GHz, SMD	Huber + Suhner	23_N-75-0-1/133_NE
J3	CONN, HDR, ST, 5-PIN, 0.100”	Molex	22-28-4053
J4	CONN, HDR, ST, 3-PIN, 0.100”	Samtec	TSW-103-07-G-S
Heat Sink	Heatsink 50 x 50 x 40	Alpha Novatech	S08EFV03-A
Indium Foil	INDIUM, 1”x1”, .004” THK, PURE	Indium Corp	KITEA-85350
Screws	SCREW, M3 x 6mm, SHCS, SS, Qty 10	McMaster - Carr	91292A111
C6, C14, C17, C18, C19, C22, C23	Not Populated		

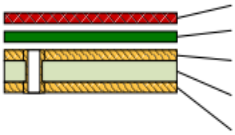
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Evaluation Board Assembly Drawing



QPA8840 Evaluation Board

LAYER STACK LEGEND

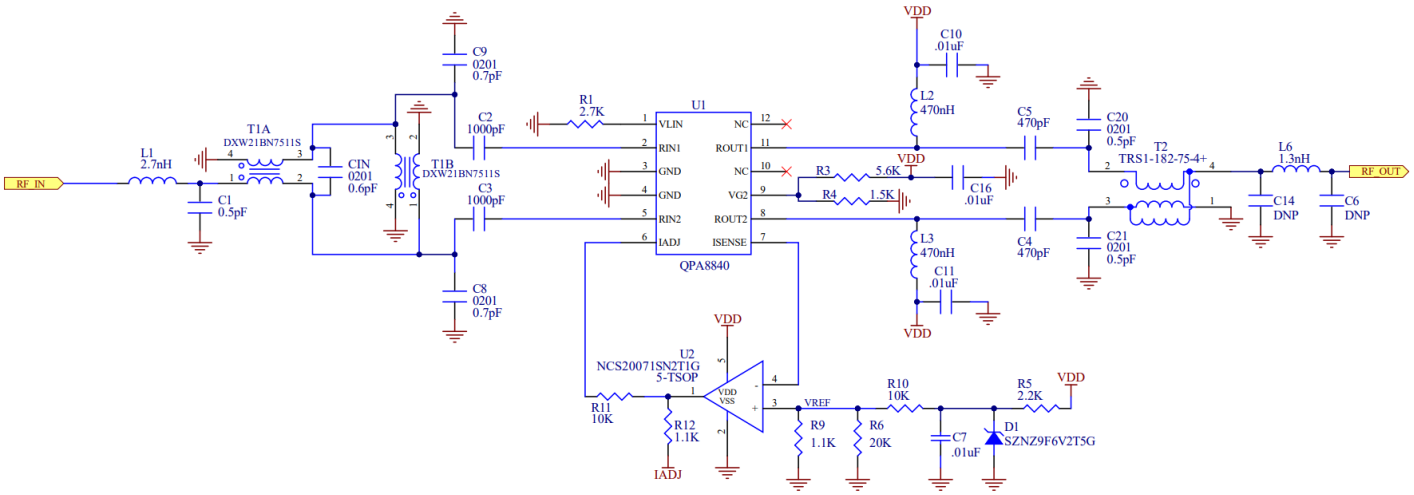


Material	Layer	Thickness	Dielectric Material	Type	Comment
	Top Overlay			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
Surface Material	Top Solder	0.0004in	SM-001	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE), OR LDI (LASER DIRECT IMAGEABLE), GREEN.
CF-004	Top Layer	0.0014in		Signal	
Core		*0.0200in*	*RO4003*	*Dielectric*	
CF-004	Bottom Layer	0.0014in		Signal	

Finished board thickness: 0.0232

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Typical Application Schematic

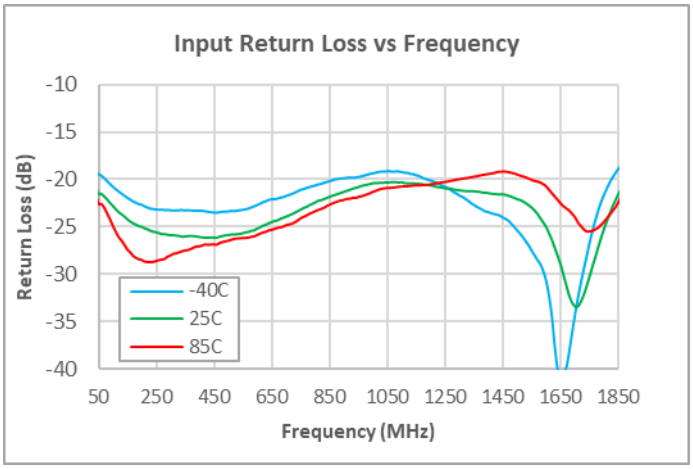


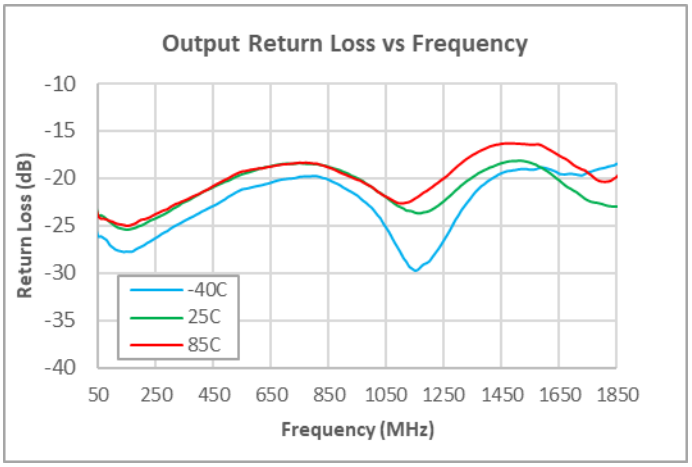
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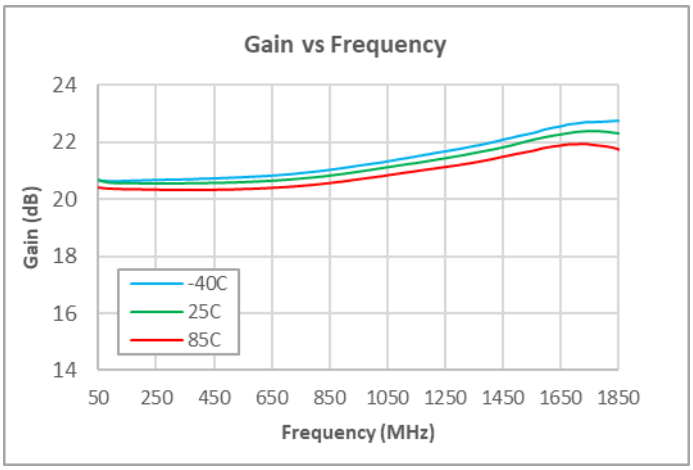
1) L1/C1 provide control for input matching with additional trim provided by C8, C9, and CIN. C2/C3 are for DC blocking and not typically adjusted for input matching.
2) L6 is used for output matching with additional trimming provided at C20/C21. C4/C5 provide DC blocking and also adds low frequency series impedance for output matching. Depending on the application load impendance, C6 and C14 may be helpful for output matching.
3) DC bias is provided through L2/L3 with sufficient local bypassing at C10/C11. Additional bypassing may be needed depending on the ambient noise environment of the application.
4) R3/R4 sets the gate bias, VG2, of the cascode and is only adjusted for operating with alternate VDD bias.
5) R1 sets the bias current for the internal linearizer which provides a small amount of fixed predistortion at the input proportional to the device current, I_{DD}, to improve the MER capability. The linearizer current is optimized for 12V, 425mA. For other operating bias points, it may be beneficial to reoptimize R1 to peak MER across the full bandwidth of the desired composite load condition.
6) U2 is an active bias current control formed by using the ISENSE output and comparing to the reference voltage on U1, Pin 3 (VREF). The output from U2 is fed back into the IADJ pin to keep the current tightly controlled. For most conditions, IDD = VREF/1.4.

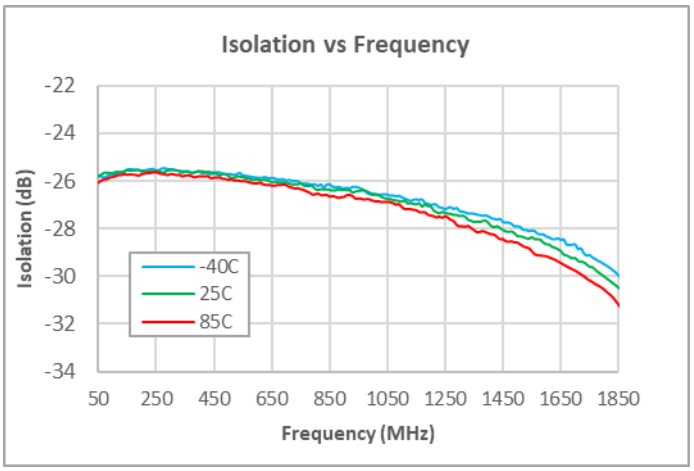
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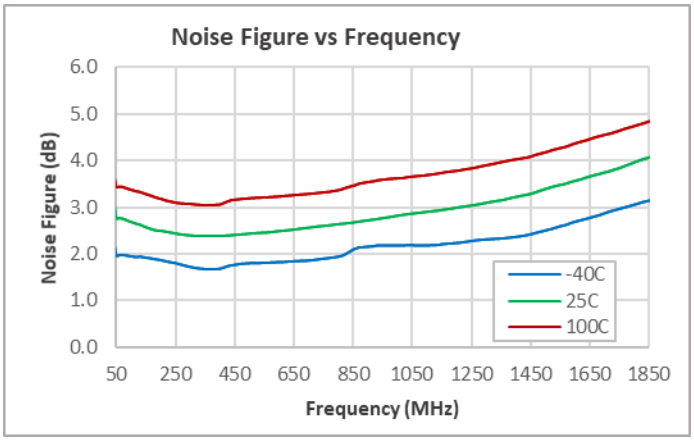
Performance Data









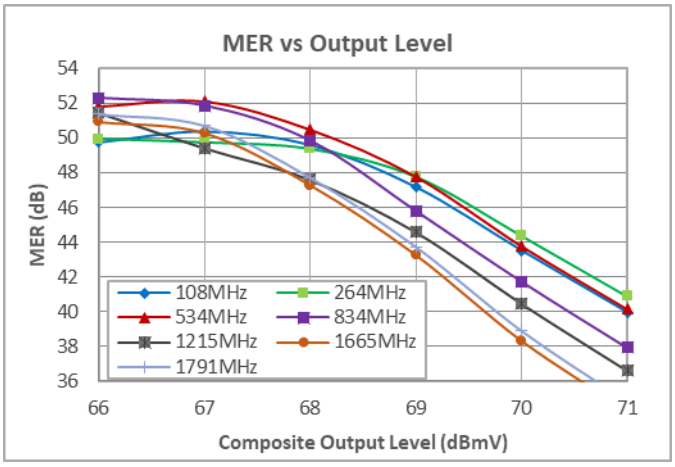


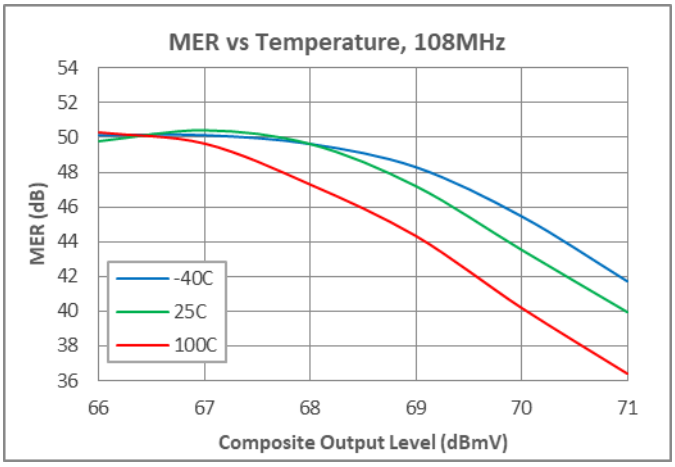
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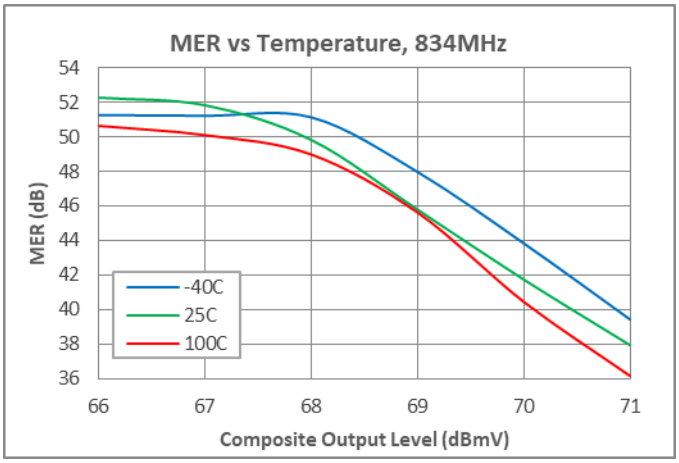
1. Test conditions unless otherwise noted: VDD = +12V, Z_o = 75Ω

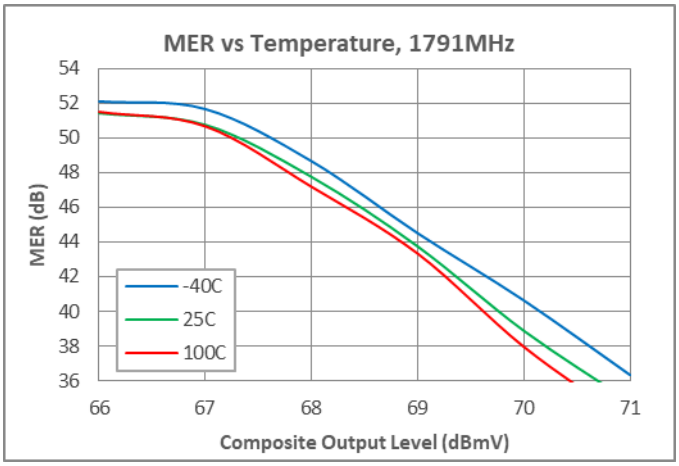
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Performance Data







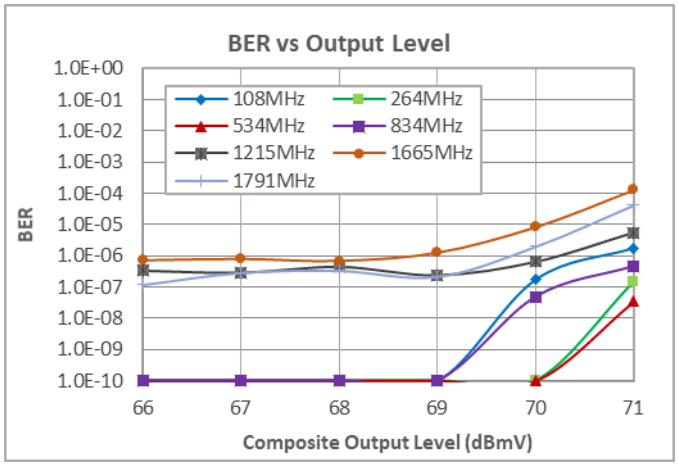


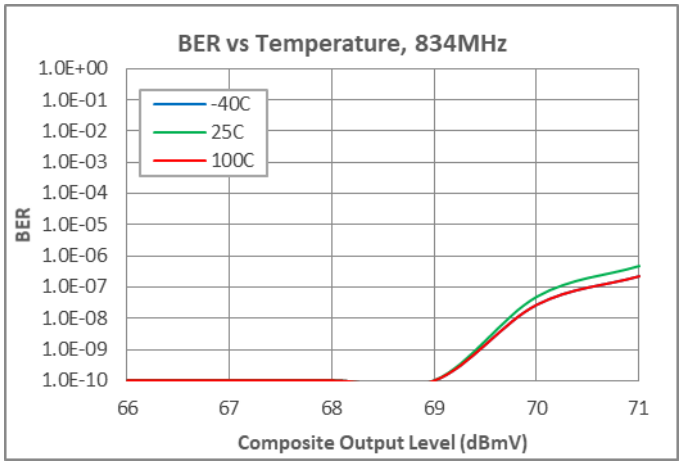
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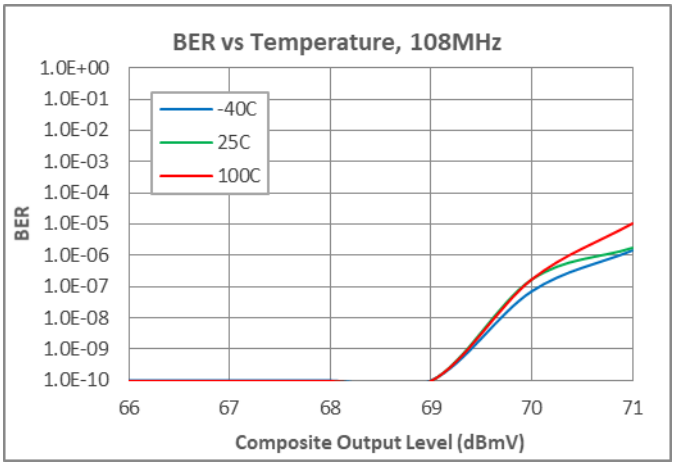
1. Test conditions unless otherwise noted: VDD = +12V, Z_o = 75Ω
2. 108 – 1794 MHz, 280 Ch. SC-QAM, Tilt = 20dB
3. MER Source Corrected. Maximum Correction, 4.3dB

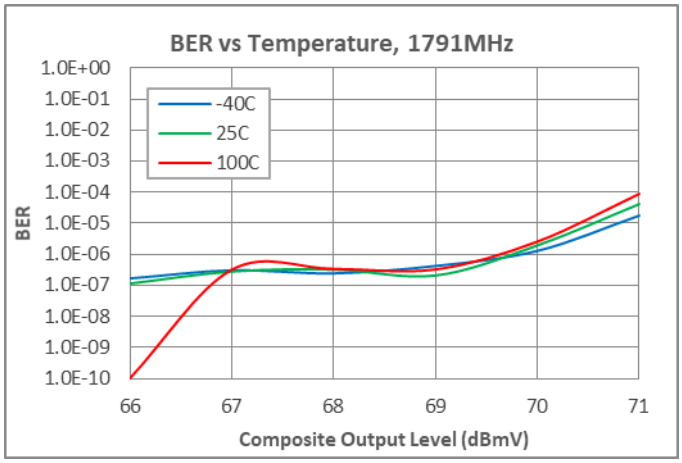
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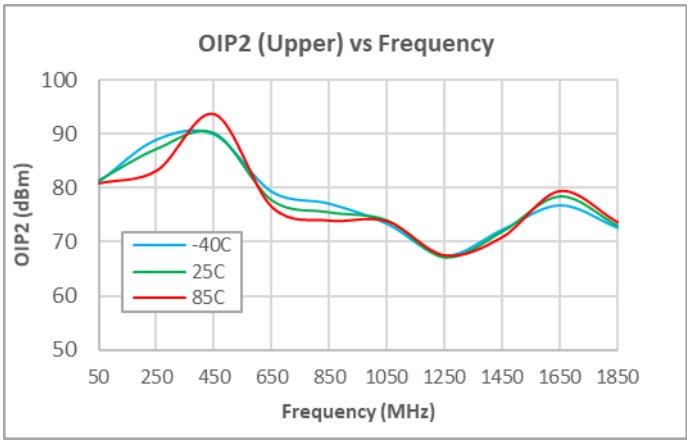


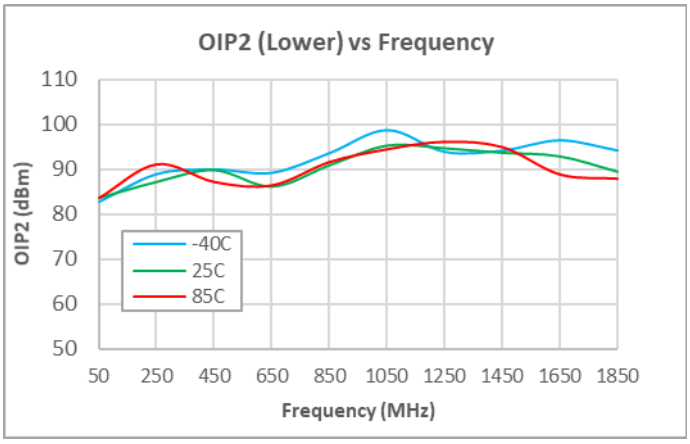
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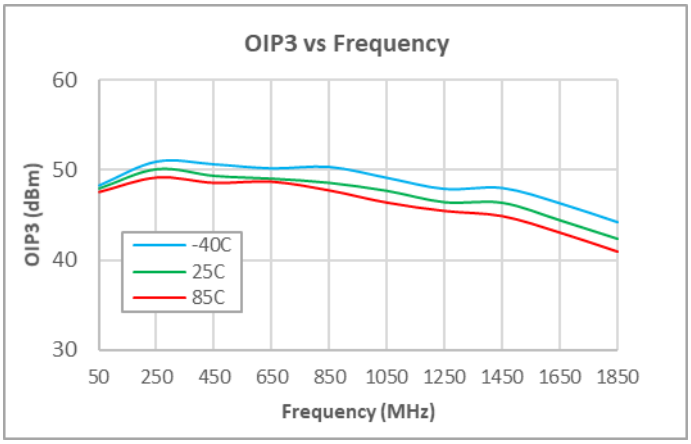
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2. 108 – 1794 MHz, 280 Ch. SC-QAM, Tilt = 20dB
3. BER Pre-Correction

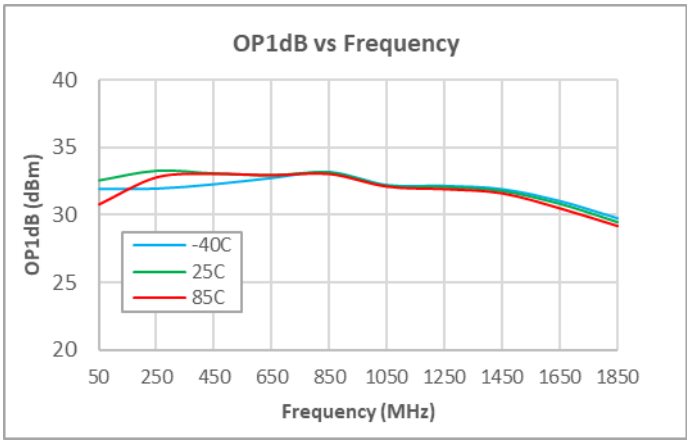
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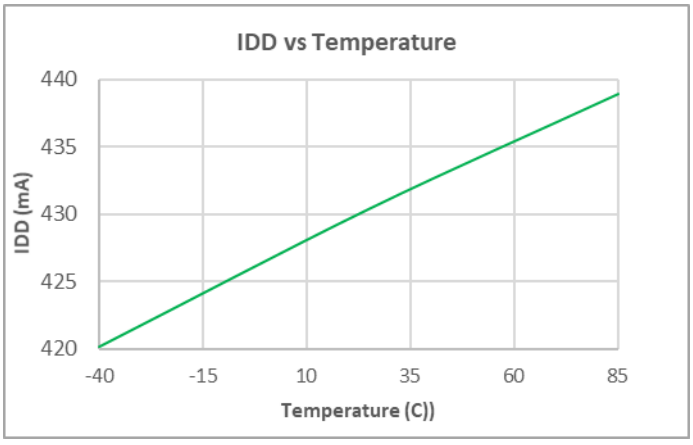
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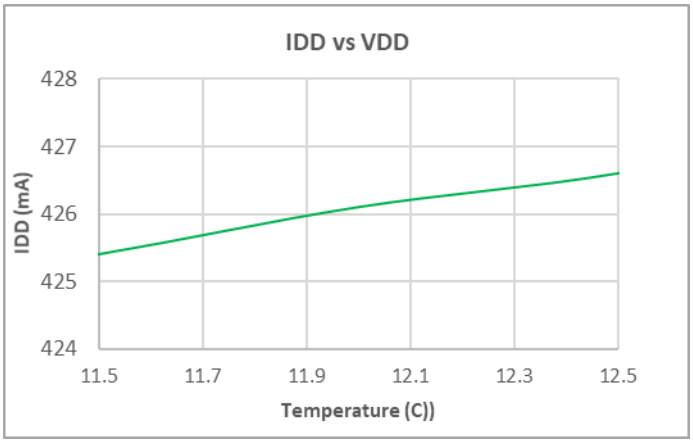










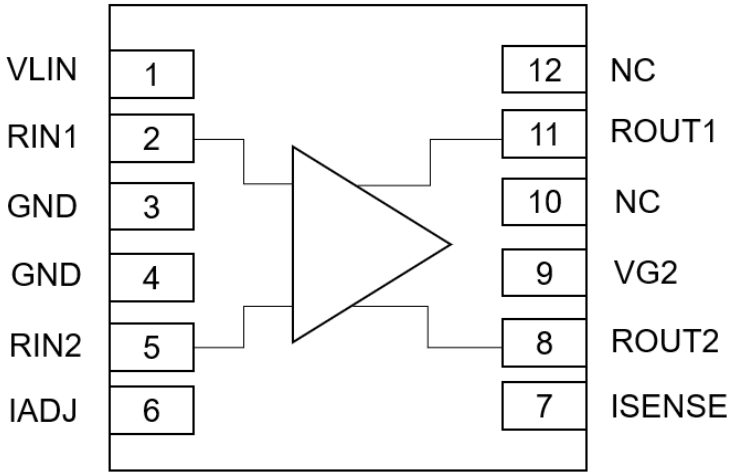


Test Conditions:

1. Test conditions unless otherwise noted: VDD = +12V, Z_o = 75Ω
2. OIP2: +12dBm/Tone, Δf = 30MHz, Full Band
3. OIP3: +12dBm/Tone, Δf = 6MHz, Full Band
4. IDD measurements include active bias circuit shown on EVB Schematic on Pg. 3

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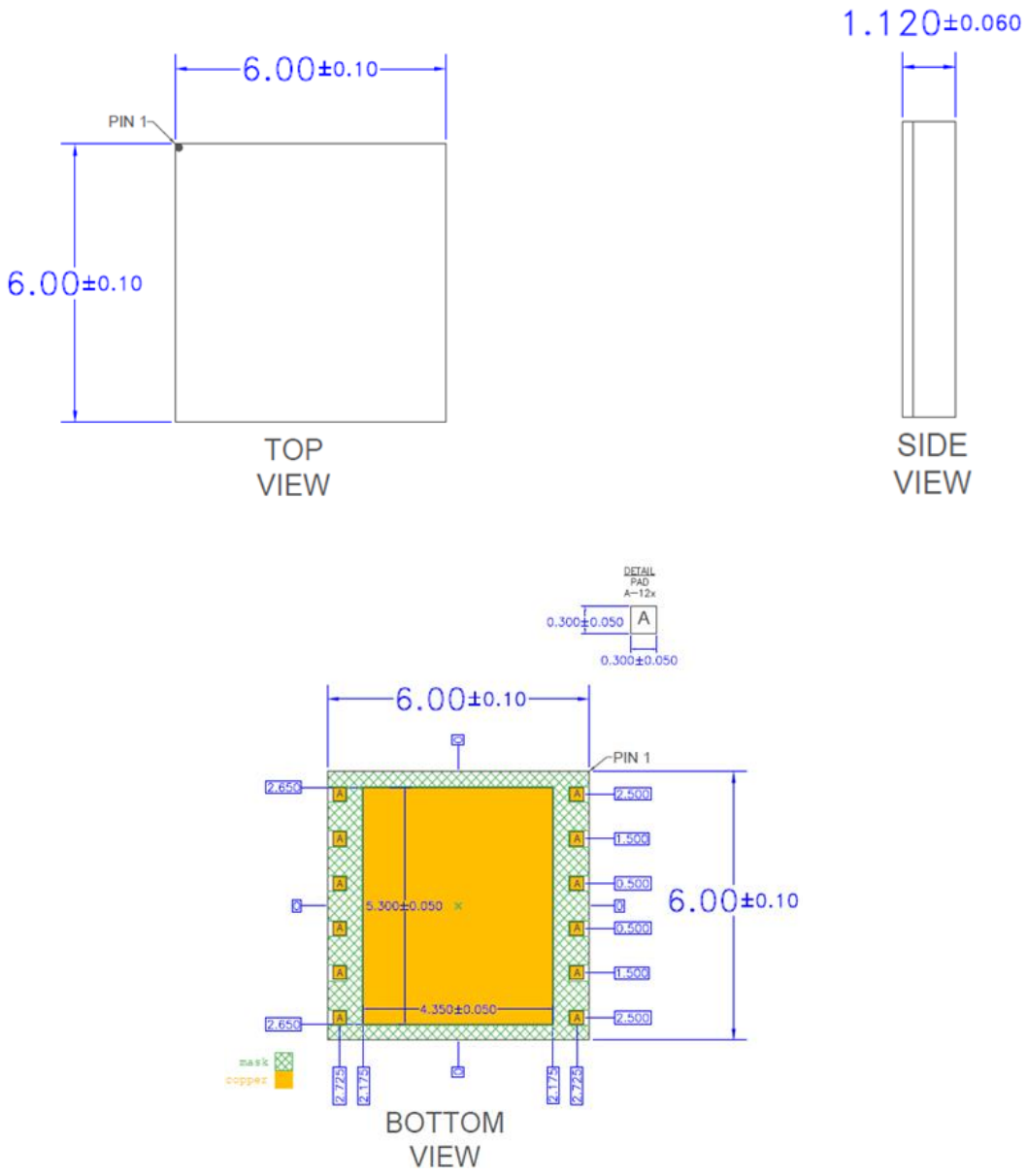
Pin Configuration and Description



Pin Number	Label	Description
1	VLIN	Linearizer Current Set
2	RIN1	RF Input +
3	GND	Ground
4	GND	Ground
5	RIN2	RF input -
6	IADJ	IDD Current Set
7	ISENSE	Current Sense Connection for Active Bias Circuit
8	ROUT2	RF Output -
9	VG2	2nd Stage Gate Bias
10	NC	No Connection
11	ROUT2	RF Output +
12	NC	No Connection
Paddle	GND	DC/RF/Thermal Ground (maximize vias in this area)

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Package Outline



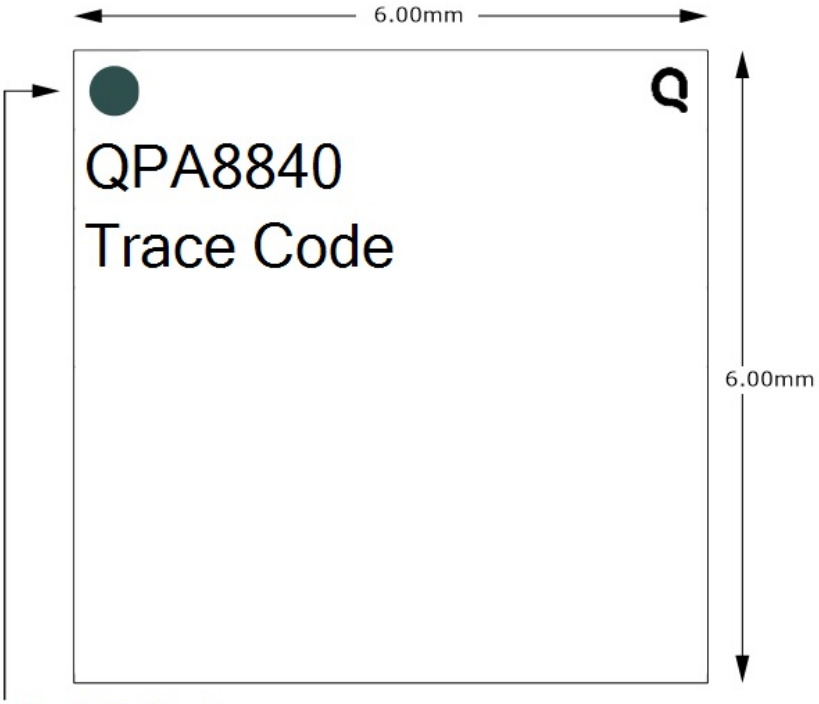
12-Pin 6x6 mm² Laminate Module

Notes:

1. Dimensions in millimeters

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Package Marking



Pin 1 Indicator
Qorvo Logo - Use Q5D
Trace Code to be assigned by subcon

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Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B (500V)	ANSI/ESDA/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3 (1000V)	ANSI/ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- PFOS Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) and tin / lead (245 °C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: ENEPIG

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: **www.qorvo.com**

Email: **customer.support@qorvo.com**

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