Phase-Locked Loop Clock Driver

Product Features

- High-Performance Phase-Locked-Loop Clock Distribution for Networking,
- Synchronous DRAM modules for server/workstation/ PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero Input-to-Output delay
- Low jitter: Cycle-to-Cycle jitter ±100ps max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Wide range of Clock Frequencies up to 80 MHz
- Package: Plastic 8-pin SOIC Package (W)

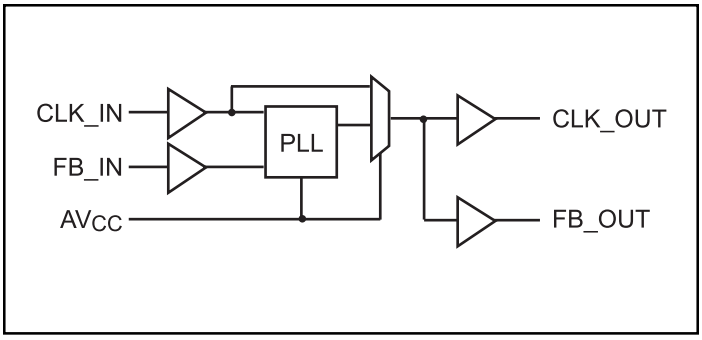
Product Description

The PI6C2502 features a low-skew, low-jitter, phase-locked loop (PLL) clock driver. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero.

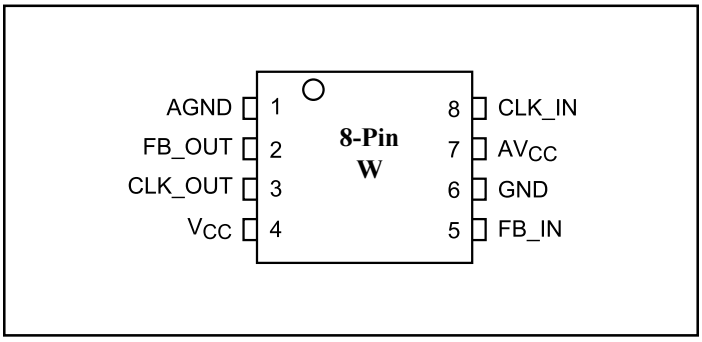
Application

If a system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers such as PI6C2509Q, and PI6C2510Q, is likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends the use of a zero-delay buffer and an eighteen output non-zero-delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

Logic Block Diagram



Product Pin Configuration



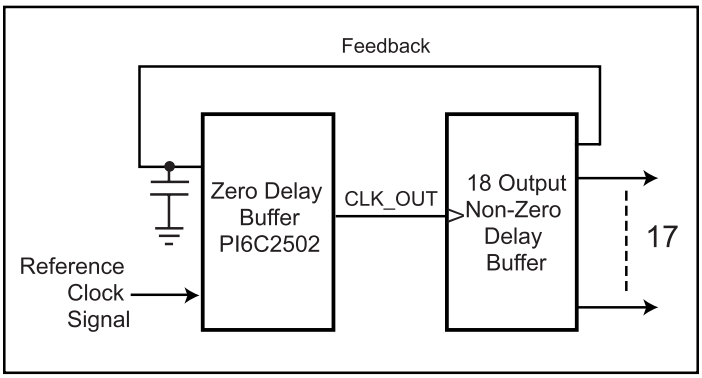


Figure 1. This Combination Provides Zero-Delay Between the Reference Clocks Signal and 17 Outputs

Pin Functions

Pin Name	Pin Number	Type	Description
CLK_IN	8	I	Reference Clock input. CLK_IN allows spread spectrum clock input.
FB_IN	5	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
FB_OUT	2	O	Feedback output FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs CLK_OUT.
CLK_OUT	3	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
AV_{CC}	7	Power	Analog power supply. AV_{CC} can be also used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	4	Power	Power supply.
GND	6	Ground	Ground.

DC Specifications (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_I	Input voltage range	–0.5	V_{CC} +0.5	V
V_O	Output voltage range			
I_{O_DC}	DC output current		100	mA
Power	Maximum power dissipation at T_A = 55°C in still air		1.0	W
T_{STG}	Storage temperature	–65	150	°C

Note: Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	V_{CC}	Min.	Typ.	Max.	Units
I_{CC}	V_I = V_{CC} or GND; I_O = 0(1)	3.6V			10	µA
C_I	V_I = V_{CC} or GND	3.3V		4		pF
C_O	V_O =V_{CC} or GND			6		

Note: 1. Continuous Output Current

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply voltage	3.0	3.6	V
V_{IH}	High level input voltage	2.0		
V_{IL}	Low level input voltage		0.8	
V_I	Input voltage	0	V_{CC}	
T_A	Operating free-air temperature	0	70	°C

Electrical Characteristics

(Over recommended operating free-air temperature range Pull Up/Down Currents, V_{CC} = 3.0V)

Symbol	Parameter	Condition	Min.	Max.	Units
I_{OH}	Pull-up current	V_{OUT} = 2.4V		–18	mA
		V_{OUT} = 2.0V		–30	
I_{OL}	Pull-down current	V_{OUT} = 0.8V	25		
		V_{OUT} = 0.55V	17		

AC Specifications Timing Requirements

(Over recommended ranges of supply voltage and operating free-air temperature)

Symbol	Parameter	Min.	Max.	Units
F_{CLK}	Clock frequency	25	80	MHz
D_{CYI}	Input clock duty cycle	40	60	%
	Stabilization Time after power up		1	ms

Switching Characteristics

(Over recommended ranges of supply voltage and operating free-air temperature, C_L=30pF)

Parameter	From (Input)	To (Output)	V_{CC} = 3.3V ±0.3V, 0-70°C			Units
			Min.	Typ.	Max.	
tphase error without jitter	CLK_IN↑ at 100MHz and 66MHz	FB_IN↑	–150		+150	ps
Jitter, cycle-to-cycle	At 100 MHz and 66 MHz	CLK_OUT	–100		+100	
Skew at 100 MHz and 66 MHz	CLK_OUT or FB_OUT	CLK_OUT or FB_OUT			200	
Duty cycle		CLK_OUT or FB_OUT	45		55	%
tr, rise-time, 0.4V to 2.0V				1.0		ns
tf, fall-time, 2.0V to 0.4V				1.1		

Note: These switching parameters are guaranteed by design.

Application Note

Layout and Schematic Guidelines

Introduction

Because of today's high-speed design demands, board designers must have extensive knowledge concerning transmission line effect, EMI, and crosstalk. They also need to understand board materials, signal and power stacking, connectors, cables, vias, and trace dimensions. Pericom Semiconductor Corporation offers an extensive line of high-speed clock products for desktop, notebook, set top boxes, information device, servers, and workstations. To make high-speed chips function properly, a designer needs to rely on accurate schematics and layout guidelines.

This application note focuses on Pericom's PI6C2502 Zero- Delay Clock Buffer, presenting schematics and layout guidelines for the chip. Also listed are some decoupling guidelines that are important for this chip's varied applications.

Decoupling Capacitors

Every printed circuit board needs large bypass capacitors to balance the inductance of the power-supply wiring. These capacitors have some lead inductance that increase as the frequency goes higher, which is why it is very important to place the capacitors as close as possible to the ***V_{CC} and Ground Pins on the Chip***.

To reduce the series lead inductance effect, avoid the following:

1. Long traces larger than 0.01 inch between capacitor pad and via
2. Use of capacitors other than surface mount
3. Via holes less than 0.035-inch diameter

Pericom's clocks use high-precision, integrated analog PLL that can be effected by the power supply and ground pins. Noise on these two pins can dramatically increase skew and output jitter.

To minimize these problems, connect a 4.7µF, a 220nF , and a 2.2nF capacitor to the digital supply pin. Also use one 4.7µF , one 220nF, and one 2.2nF capacitor on the analog supply pin. Connect the other side to the analog ground pin.

Place a 10µF capacitor from the main power island to the power plane that is supplied to the clock chip.

Use high-quality, low ESR, ceramic surface-mount capacitors.

Stacking

At low speeds, currents follow the least resistance path, but at high speeds current follows the least inductance path. The lowest inductance return path lies directly under the signal conductor. This location minimizes the total loops needed between the outgoing and returning paths. That is why it is important to separate the signal layers by ground planes if possible. Also avoid totally cutting part of the ground plane to be used for a signal's path. That is totally unacceptable, because it will increase crosstalk considerably and does not provide a clean return to those signals. Also use lower trace impedance because it lowers undershoot and overshoot. Always use FR-4 material for board fabrication. Use 4- layer stack-up arrangement. Make sure you have a signal layer that is followed by the ground layer, then a power layer, and finally the second signal layer. Please see Figure 1 below.

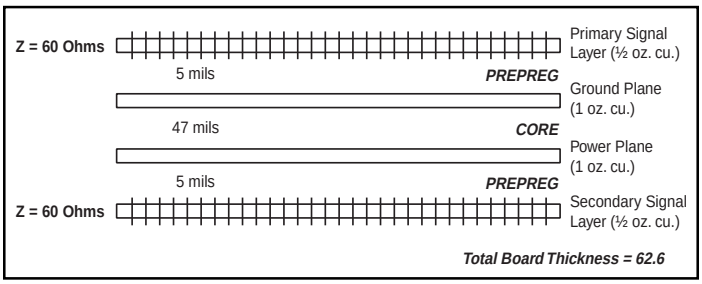


Figure 1: Four-Layer Board Stack-up

Clock routing and spacing

To minimize crosstalk on the clock signals, use a minimum of 0.014-inch spacing between clock traces and others. If you have to use serpentine to match trace lengths on similar chips, make sure that you have at least 0.018-inch spacing for serpentines. Please see Figure 2 below.

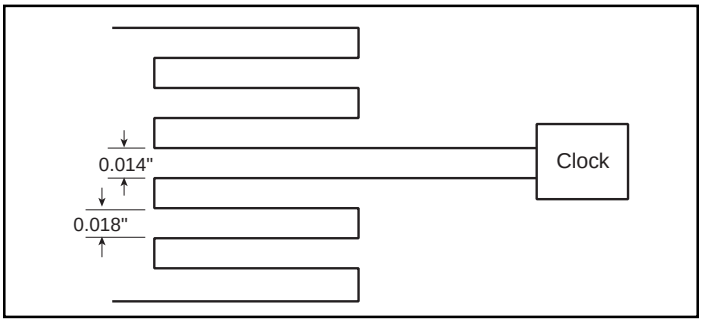
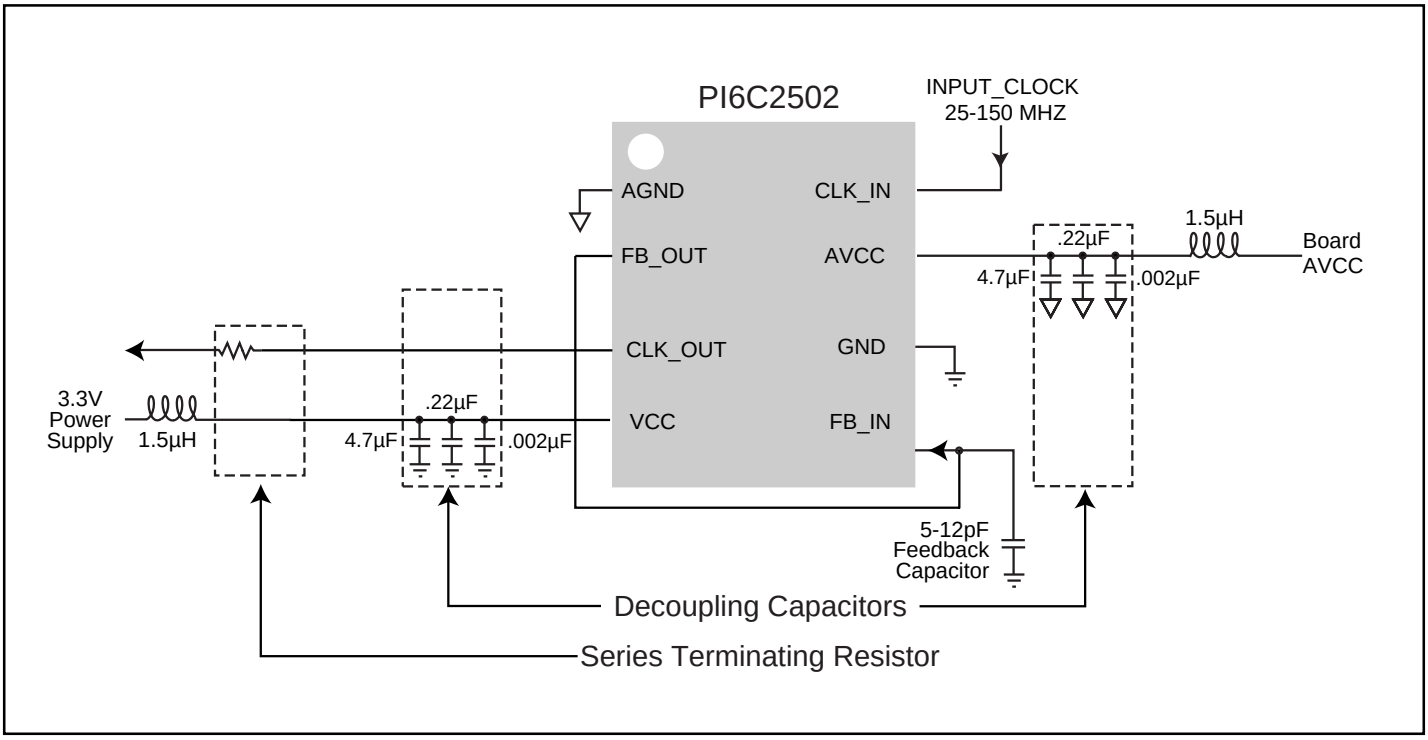
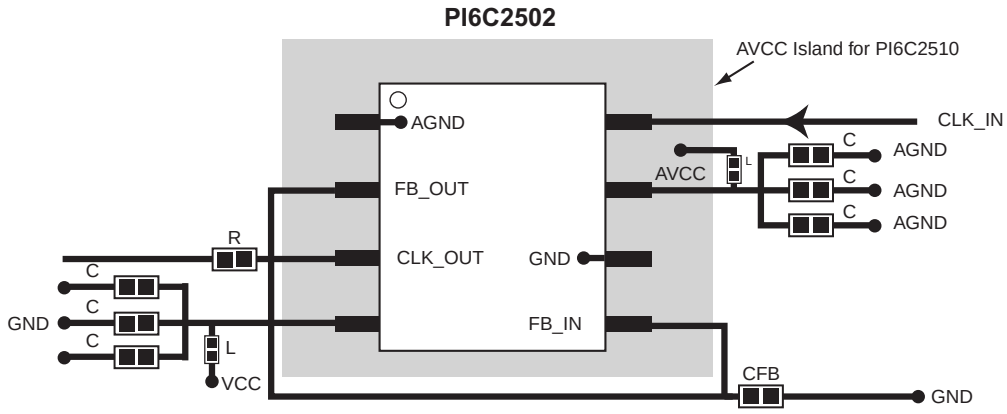


Figure 2: Clock Trace Spacing Guidelines

Schematic Drawing



Clock Chip Layout



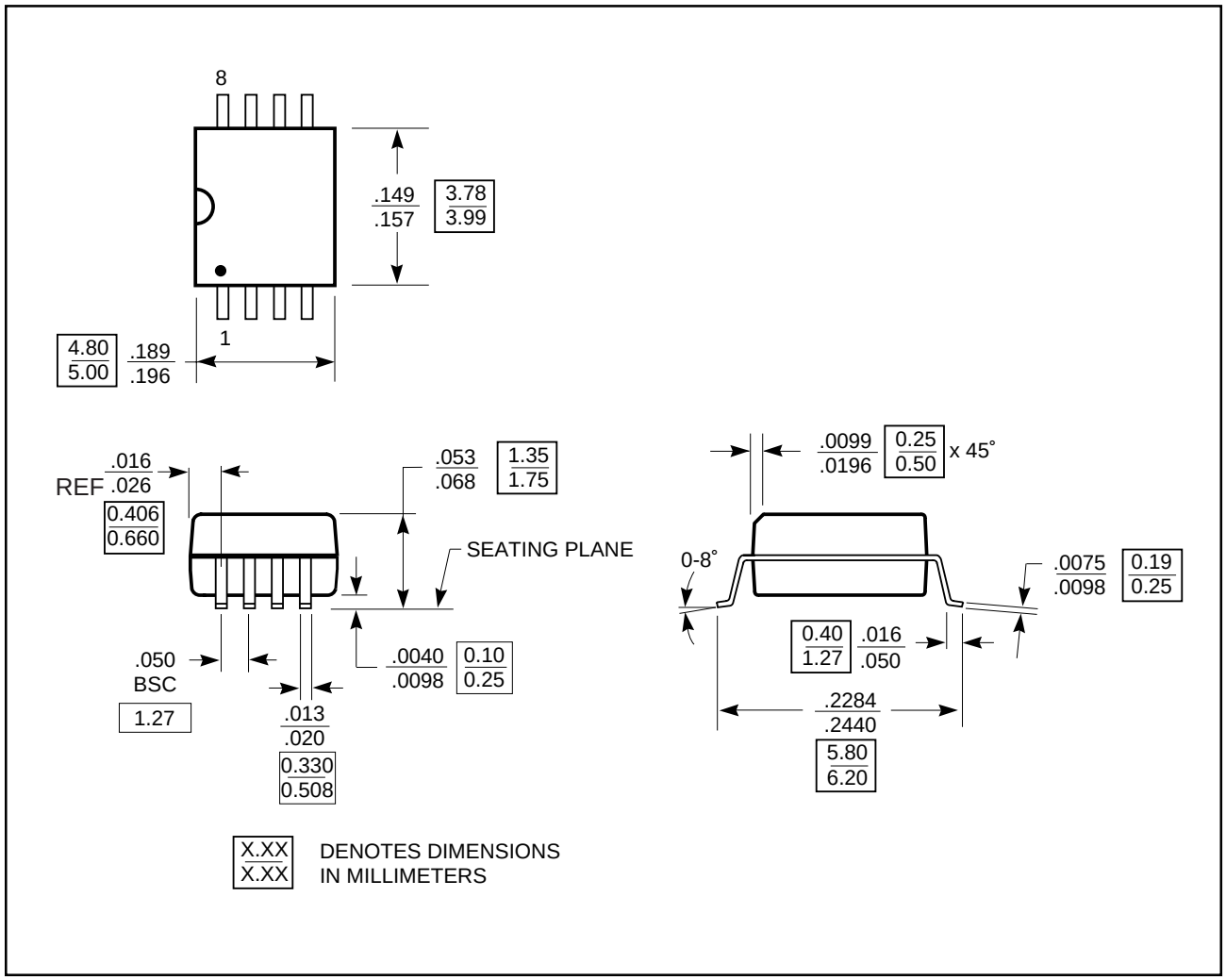
Use Wider Traces for Ground and Power
(0.034-inch width, 0.1-inch pitch)

Legend:

GND	=	Via to Digital Ground
AGND	=	Via to Analog Ground
VCC	=	Via to 3.3V Digital Power
AVCC	=	Via to 3.3V Analog Power
R	=	Termination Resistor 12-32Ω
C	=	Decoupling Capacitor
L	=	Inductor
CFB	=	Feedback Capacitor

Package Mechanical Information

Plastic 8-pin SOIC Package



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI6C2502W	W8	8-pin 150-mil SOIC	Commercial