



Features

- ESD protection for one line with bi-directional
- Provide transient protection for one line to
IEC 61000-4-2 (ESD) $\pm 17\text{kV}$ (air), $\pm 15\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
Cable Discharge Event (CDE)
- **0201 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- For low operating voltage applications: 5V maximum
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green part**

Applications

- Mobile phones
- Handheld portable applications
- Computer interfaces protection
- Microprocessors protection
- Serial and parallel ports protection
- Control signal lines protection
- Power lines on PCB protection
- Latch-up protection

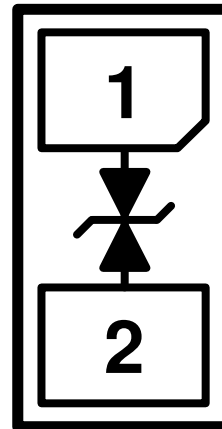
Description

AZ5A75-01F is a design which includes one bi-directional ESD rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ5A75-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ5A75-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5A75-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge)

Circuit Diagram / Pin Configuration



DFN0603P2Y (Bottom View)
(0.6mm x 0.3mm x 0.3mm)



SPECIFICATIONS

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise specified) | | | |
|--|-------------|---------------|------------------|
| PARAMETER | SYMBOL | RATING | UNIT |
| Operating Supply Voltage | V_{DC} | ± 5.5 | V |
| ESD per IEC 61000-4-2 (Air) | V_{ESD-1} | ± 17 | kV |
| ESD per IEC 61000-4-2 (Contact) | V_{ESD-2} | ± 15 | |
| Lead Soldering Temperature | T_{SOL} | 260 (10 sec.) | $^\circ\text{C}$ |
| Operating Temperature | T_{OP} | -55 to +85 | $^\circ\text{C}$ |
| Storage Temperature | T_{STO} | -55 to +150 | $^\circ\text{C}$ |

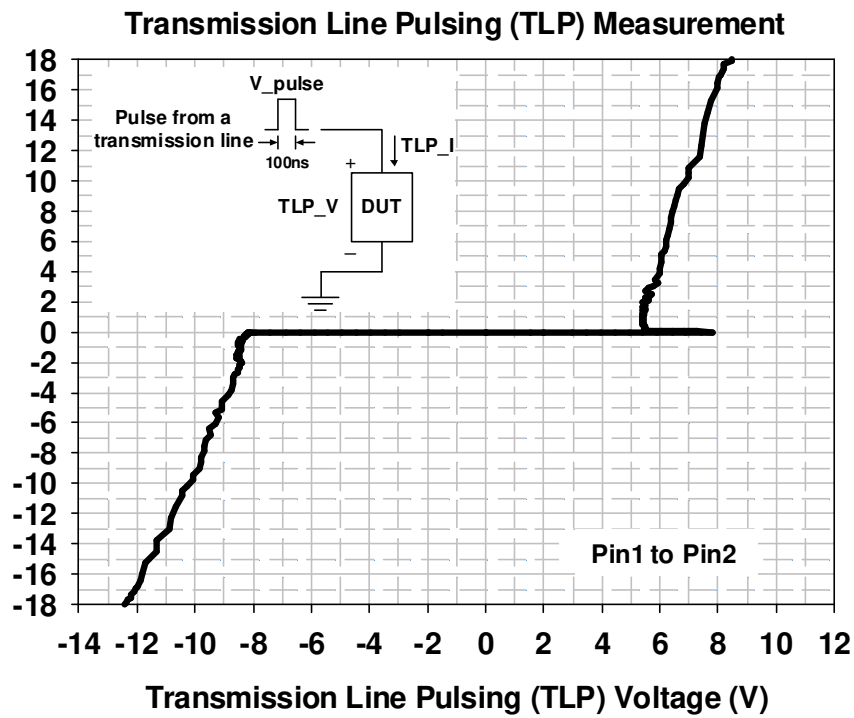
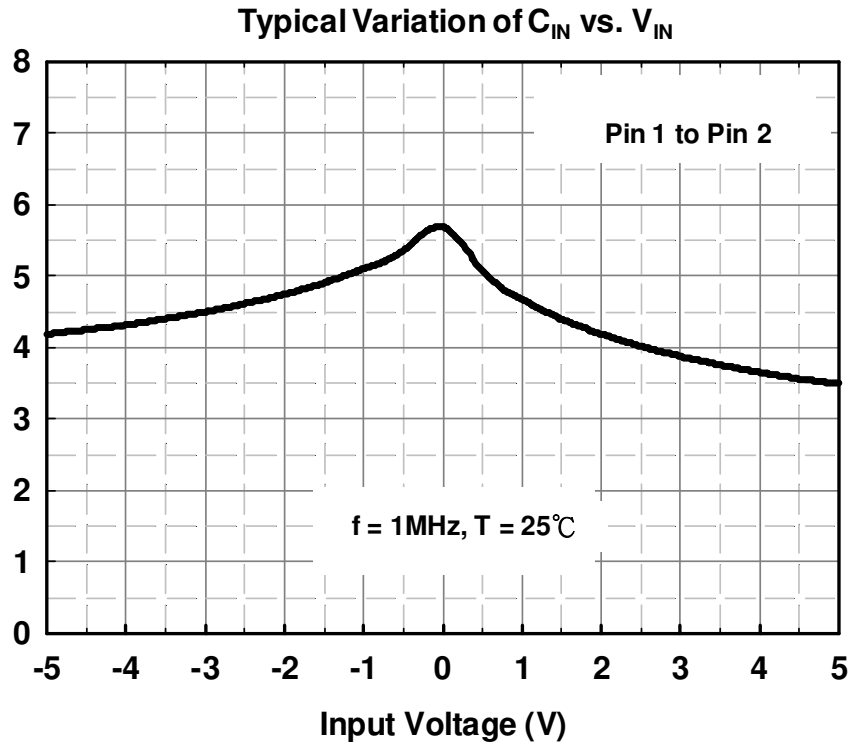
| ELECTRICAL CHARACTERISTICS | | | | | | |
|-----------------------------------|---------------|---|-----|------|-----|----------|
| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNIT |
| Reverse Stand-Off Voltage | V_{RWM} | $T = 25^\circ\text{C}$. | -5 | | 5 | V |
| Reverse Leakage Current | I_{Leak} | $V_{RWM} = \pm 5\text{V}$, $T = 25^\circ\text{C}$. | | | 100 | nA |
| Reverse Breakdown Voltage | V_{BV} | $I_{BV} = 1\text{mA}$, $T = 25^\circ\text{C}$. | 5.6 | | 9 | V |
| ESD Clamping Voltage (Note 1) | V_{CL-ESD} | IEC 61000-4-2 +8kV ($I_{TLP} = 16\text{A}$), Contact mode, $T = 25^\circ\text{C}$. | | 12 | | V |
| ESD Dynamic Turn-on Resistance | $R_{dynamic}$ | IEC 61000-4-2, 0~+8kV, $T = 25^\circ\text{C}$, Contact mode. | | 0.25 | | Ω |
| Channel Input Capacitance | C_{IN} | $V_R = 0\text{V}$, $f = 1\text{MHz}$, $T = 25^\circ\text{C}$. | | 5.5 | 7 | pF |

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: $Z_0 = 50\Omega$, $t_p = 100\text{ns}$, $t_r = 1\text{ns}$.



Typical Characteristics



Application Information

The AZ5A75-01F is designed to protect one line against system ESD/EFT/Cable Discharge pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5A75-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5A75-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5A75-01F.
- Place the AZ5A75-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

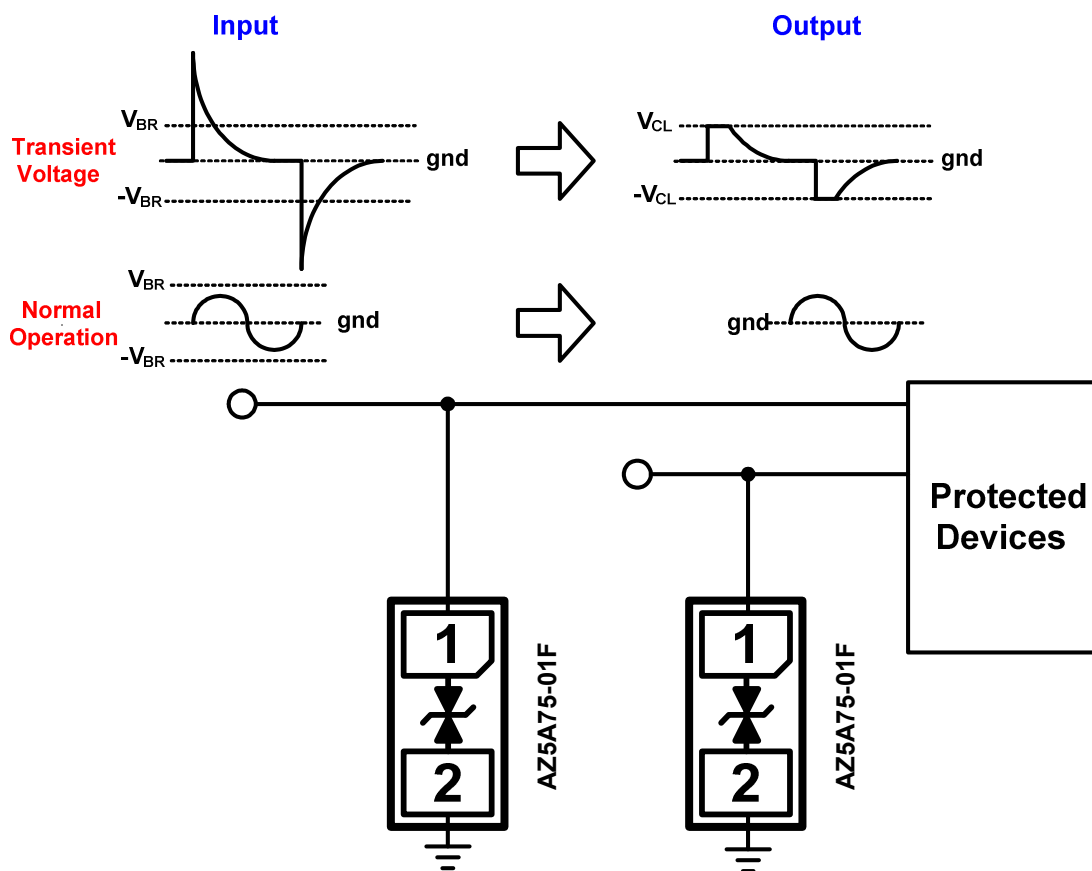


Fig. 1



Fig. 2 shows another simplified example of using low-speed data line, and power line from ESD AZ5A75-01F to protect the control line, transient stress.

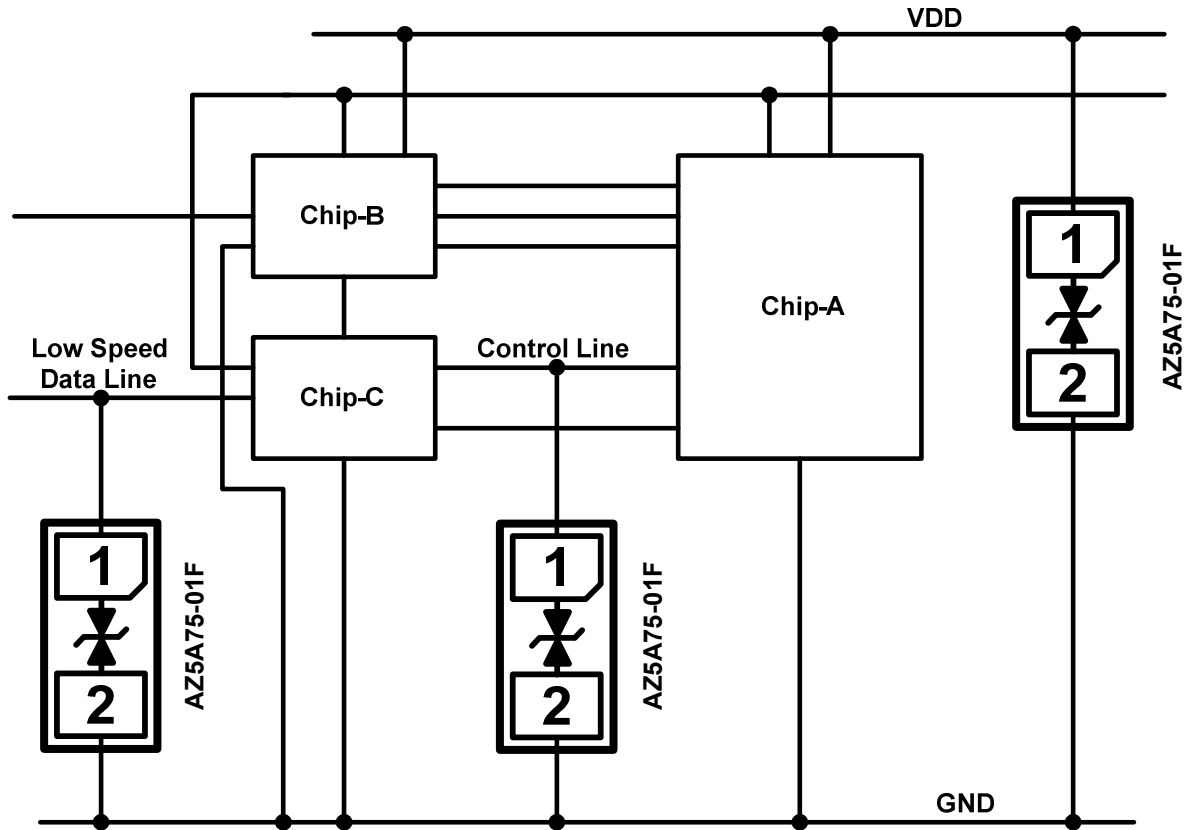
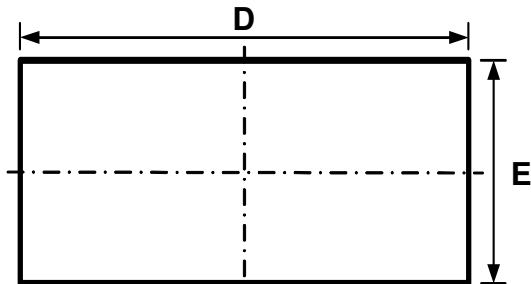


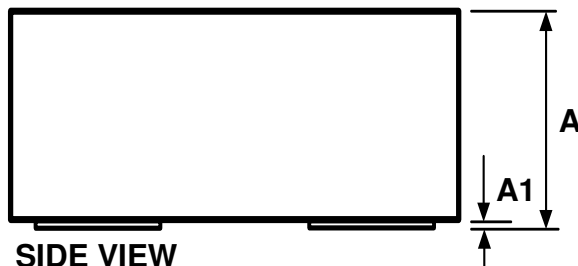
Fig. 2

Mechanical Details

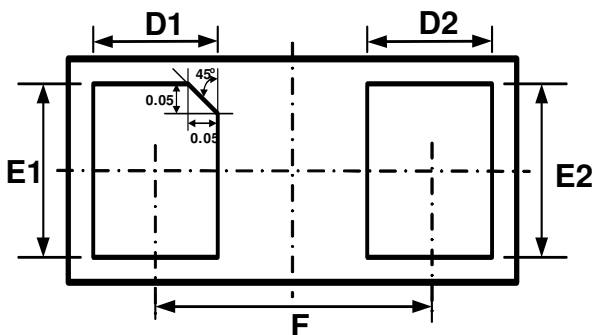
DFN0603P2Y PACKAGE DIAGRAMS



TOP VIEW



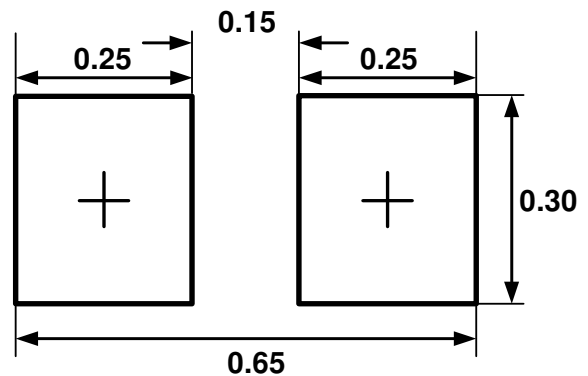
SIDE VIEW



BOTTOM VIEW

| SYMBOL | Millimeters | | |
|--------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| D | 0.55 | 0.60 | 0.65 |
| E | 0.25 | 0.30 | 0.35 |
| A | 0.28 | 0.30 | 0.32 |
| A1 | 0.00 | 0.02 | 0.05 |
| D1 | 0.13 | 0.18 | 0.23 |
| D2 | 0.14 | 0.19 | 0.24 |
| E1/E2 | 0.20 | 0.25 | 0.30 |
| F | 0.35 | | |

LAND LAYOUT

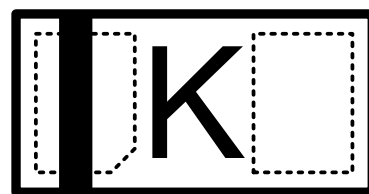


(Unit: mm)

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



K = Device Code

| Part Number | Marking Code |
|--------------------------------|--------------|
| AZ5A75-01F.R7G (Green Part) | K |

Note. Green means Pb-free, RoHS, and Halogen free compliant.



Ordering Information

| PN# | Material | Type | Reel size | MOQ | MOQ/internal box | MOQ/carton |
|----------------|----------|------|-----------|-------------|---------------------|-------------------------|
| AZ5A75-01F.R7G | Green | T/R | 7 inch | 12,000/reel | 4 reels= 48,000/box | 6 boxes =288,000/carton |

Revision History

| Revision | Modification Description |
|---------------------|--------------------------|
| Revision 2017/03/24 | Preliminary Release. |
| Revision 2018/03/19 | Formal Release. |
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