Active Clamp Forward PWM Controller

ISL6726

The ISL6726 is a highly featured single-ended PWM controller intended for applications using the active clamp forward converter topology in either n- or p-channel active clamp configurations, the asymmetric half-bridge topology, and the standard forward topologies with synchronous rectification. It is a current-mode PWM controller with many features designed to simplify its use. Among its many features are a precision oscillator which allows accurate control of the deadtime and maximum duty cycle, bi-directional synchronization with 180° phase shift for interleaving applications, adjustable soft-start and soft-stop, a low power disable mode, and average current limit for “brick-wall” overcurrent protection.

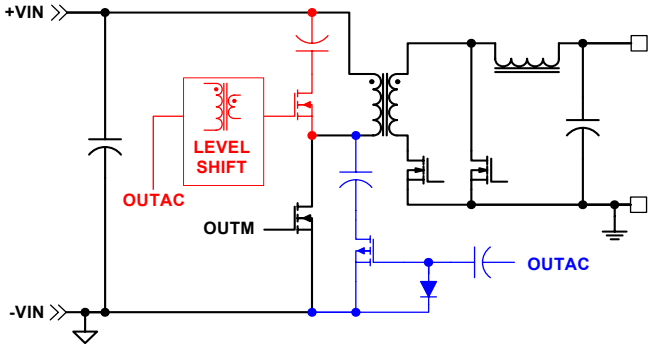
This advanced BiCMOS design features low start-up and operating currents, adjustable switching frequency to greater than 1MHz, high current FET drivers, and very low propagation delays for a fast response to overcurrent faults.

Applications

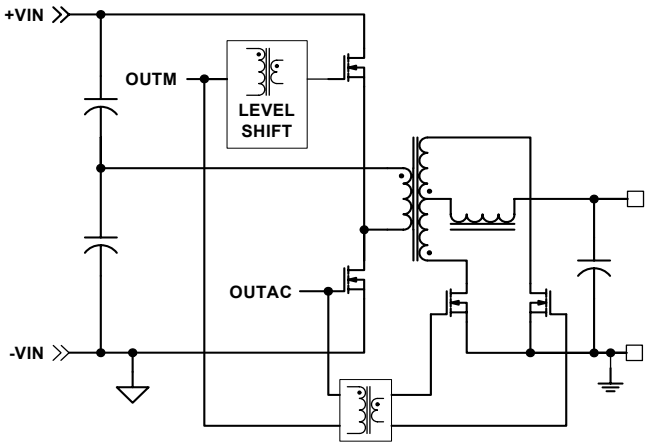
- Telecom and Datacom Power Supplies
- AC/DC Power Supplies
- Battery Chargers

Features

- Precision Maximum Duty Cycle and Deadtime Control
- 125µA Typical Start-up Current
- Adjustable Peak and Average Current Limit Protection
- Programmable Oscillator Frequency
- Bi-Directional Synchronization with 180° Phase Shift for Interleaved Converter Applications
- Adjustable Soft-Start and Selectable Soft-Stop
- Selectable Minimum Duty Cycle Clamp for Synchronous Rectifier Applications
- Programmable Slope Compensation
- Supports N- and P-Channel Active Clamp FETs
- Programmable Switch Timing Between Main and Active Clamp Outputs
- Programmable Undervoltage Lock-Out (UV)
- Input Voltage Dependent Duty Cycle Clamp
- ENABLE Input with Low Power Disable
- Internal Over-Temperature Protection
- Pb-Free (RoHS Compliant)



N- or P- CHANNEL ACTIVE CLAMP FORWARD

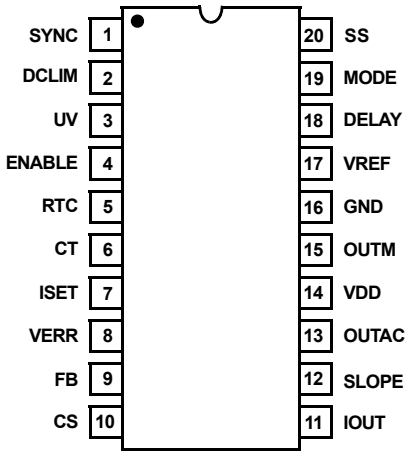


ASYMMETRIC HALF-BRIDGE

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Copyright Intersil Americas Inc. 2011. All Rights Reserved
Intersil (and design) is a trademark owned by Intersil Corporation or one of its subsidiaries.
All other trademarks mentioned are the property of their respective owners.

Pin Configuration

ISL6726
(20 LD QSOP)
TOP VIEW



Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	SYNC	A bi-directional edge-sensitive signal used to synchronize multiple devices together. If the SYNC pins of two units are connected, they will synchronize 180 degrees out of phase with each other. This feature facilitates the design of interleaved topologies. If more than two units are connected, one will be the master unit and the rest will be slave units. All of the slave units will synchronize 180 degrees out-of-phase with the master. The master designation is not fixed or predetermined and is self-arbitrating. The master is determined by the fastest running oscillator on a dynamic basis. SYNC may also be used to synchronize to an external clock.
2	DCLIM	Used in conjunction with UV, DCLIM creates a duty cycle clamp that is dependent on the input voltage. As the input voltage increases, the maximum allowed duty cycle decreases. This feature is necessary in the active clamp forward to help prevent transformer core saturation during transients. A resistor divider from VREF sets the threshold of DCLIM.
3	UV	Sets the user programmable undervoltage threshold. Placing a resistor divider from the input voltage to ground and set to 1.00V determines the minimum operating voltage. The amount of hysteresis is determined by an internal current source and set by the external impedance of the divider. The current source is active when UV is below 1V.
4	ENABLE	A logic level signal used to enable the IC. When the input is open, the IC is enabled and a soft-start cycle begins if no fault conditions are present. When pulled low, the outputs are disabled and the IC enters a low power sleep state. If soft-stop is enabled, a logic “0” on ENABLE forces a soft-stop prior to entering the low power sleep state.
5	RTC	The oscillator timing capacitor charge/discharge current control pin. A resistor is connected between this pin and GND and determines the magnitude of the charge and discharge current. The charge current is nominally 2x the current flowing into the resistor. The discharge current is nominally 8x the current flowing into the resistor. The ratio of the charge to discharge current is fixed and sets the maximum duty cycle at 80%.
6	CT	The oscillator timing capacitor is connected between this pin and GND.
7	ISET	Controls the peak and average current limit thresholds. A voltage up to 1.0V may be applied to ISET.
8	VERR	The error voltage input to the PWM comparator and the compensation connection for the average current loop control. VERR requires an external pull-up resistor to VREF. A typical application connects the photo-transistor output of an opto-coupler between VERR and GND.
9	FB	FB is the inverting input to the average current error amplifier (IEA). The amplifier is used as the error amplifier for the average current limit control loop. If the amplifier is not used, FB should be grounded. The amplifier is normally configured as an integrator.
10	CS	The current sense input to the IC. Provides information to the PWM, the peak overcurrent protection comparators, and the average current limit circuitry. The CS pin is shorted to GND when the PWM output pulse terminates. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal logic and the turn off of the external power switch.
11	IOUT	Output of the sample and hold buffer amplifier that captures and averages the CS signal. With a nominal 4x multiplier and the ability to scale the signal externally with a resistor divider, the average current limit can be set independently of the peak current limit.

Pin Descriptions (Continued)

PIN #	SYMBOL	DESCRIPTION
12	SLOPE	A slope compensation capacitor is connected between SLOPE and GND. A current source of 100µA charges the capacitor during the On time and discharges it during the Off time. The amplitude of the signal is multiplied by a gain of 0.2 and summed with the CS input.
13	OUTAC	The Active Clamp output for driving an external power switch. OUTAC is capable of driving either a p- or n- channel clamp device and is configured by DELAY.
14	VDD	VDD is the power connection for the IC. To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible. VDD is monitored for undervoltage (UVLO). When VDD is below the UVLO threshold, the IC is disabled and the reference voltage, VREF, is turned off.
15	OUTM	The main PWM output for driving an external power switch.
16	GND	Logic and power ground for this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.
17	VREF	The 5.00V reference voltage output having a -2/+1.5% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 2.2µF low ESR capacitor. VREF can source up to 10mA.
18	DELAY	The DELAY pin configures OUTAC for either n-channel or p-channel drive compatibility by setting the phase and the duration when both the main and active clamp outputs are off. A resistor from DELAY to VREF sets an out-of-phase (non-overlap) relationship for an n-channel clamp device with adjustable deadtime. A resistor from DELAY to GND sets an in-phase (overlap) relationship for a p-channel clamp device with an adjustable symmetric non-overlap duration between OUTM and OUTAC.
19	MODE	The MODE pin configures the IC for standard or synchronous rectification operation. If MODE is connected to VREF, standard rectification operation is selected. Soft-stop and the minimum duty cycle clamp are disabled. If MODE is connected to GND, synchronous rectification operation is enabled allowing soft-stop and the minimum duty cycle clamp to function.
20	SS	Connect the soft-start timing capacitor between this pin and GND to control the duration of soft-start and soft-stop. The value of the SS capacitor determines the rate of increase and decrease of the duty cycle during start-up and soft-stop. Soft-stop is enabled/disabled by MODE.

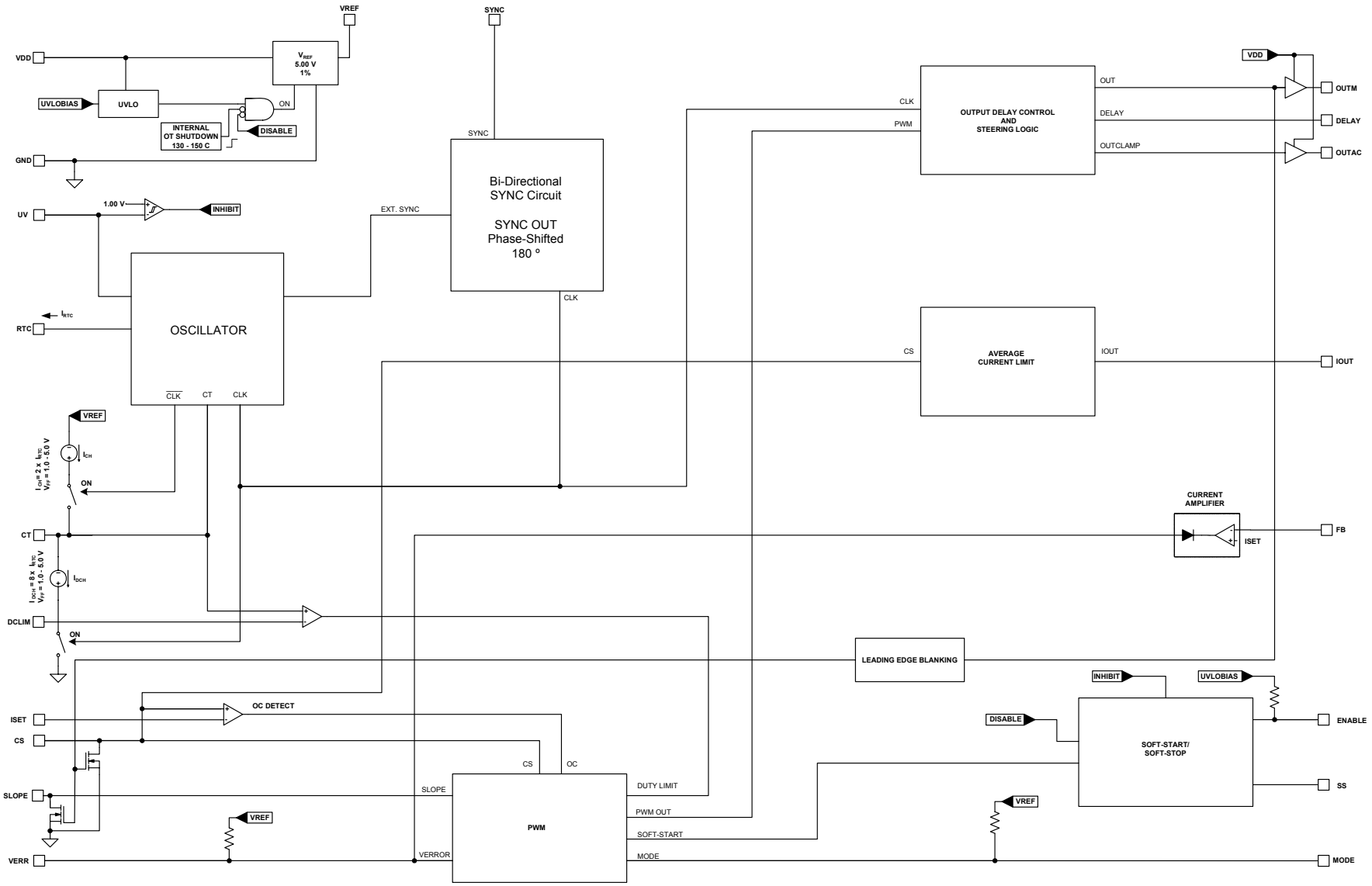
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6726AAZ	ISL6726 AAZ	-40 to +105	20 Ld QSOP	M20.15

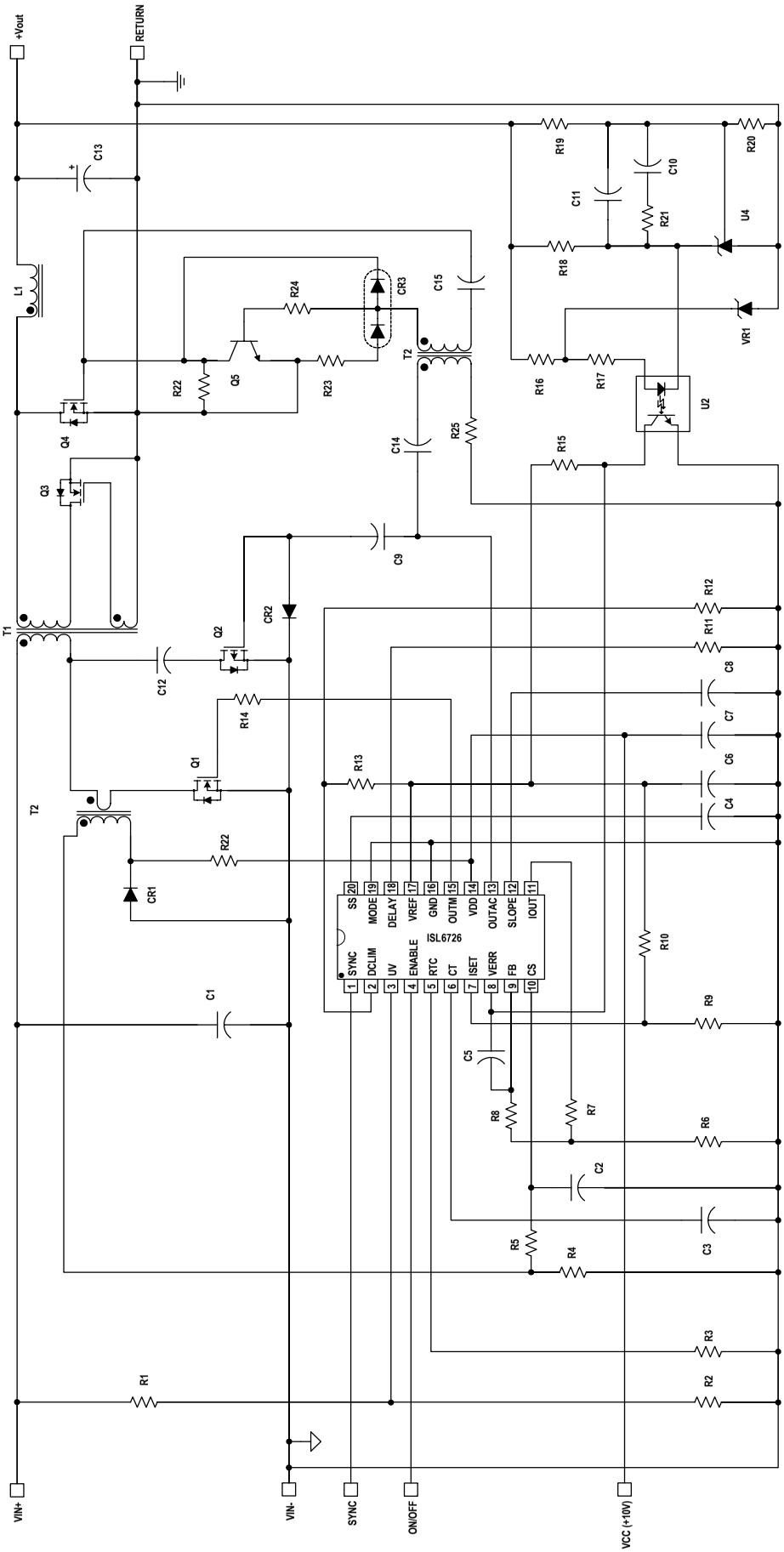
NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6726. For more information on MSL, please see Technical Brief TB363.

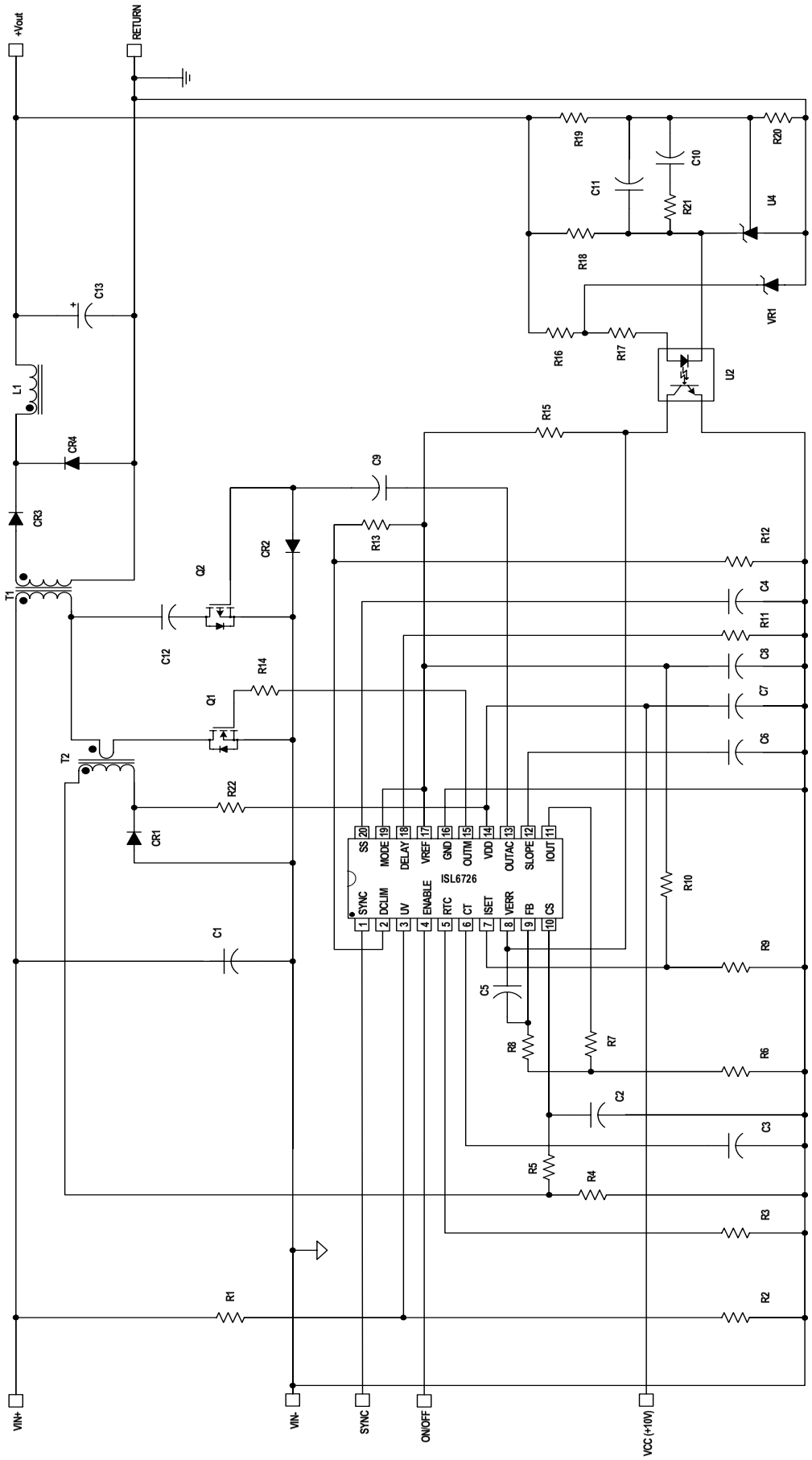
Internal Architecture



Typical Application Using ISL6726 - Active Clamp Forward with Synchronous Rectification



Typical Application Using ISL6726 - Active Clamp Forward with Diode Rectification



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +22.0V
OUTM, OUTAC . . . . . GND - 0.3V to V_{DD}
Signal Pins. . . . . GND - 0.3V to 5V
Peak GATE Current, OUTM. 3A
Peak GATE Current, OUTAC 2A
ESD Rating
Human Body Model (Tested per JESD22-A114) 3kV
Machine Model (Tested per JESD22-A115). 250V
Charged Device Model (Tested per JESD-C101E) 1.5kV
Latch Up (Tested per JESD-78B; Class2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Lead QSOP (Notes 4, 5)	86	38

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range
ISL6726Axx. . . . . -40°C to +105°C
Supply Voltage Range (Typical). . . . . 9VDC to 16VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. All voltages are to be measured with respect to GND, unless otherwise specified.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and the Typical Application schematics on pages 5 and 6. 8V < V_D < 20V, R_{TC} = 10.0kΩ, C_T = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SUPPLY VOLTAGE					
Supply Voltage			12	**20**	V
Start-Up Current, I_{DD}	V_{DD} < START Threshold	**50**	125	**400**	µA
Operating Current, I_{DD}	$C_{OUTM, OUTAC}$ = 0nF, V_{DD} = 12V		10	**11**	mA
	$C_{OUTM, OUTAC}$ = 0nF, V_{DD} = 20V		12	**13**	
	$C_{OUTM, OUTAC}$ = 1nF, V_{DD} = 12V		18	**20**	mA
UVLO START Threshold		**7.40**	7.65	**8.00**	V
UVLO STOP Threshold		**6.00**	6.23	**7.00**	V
Hysteresis		**1.00**	1.40	**2.00**	V
VOLTAGE REFERENCE					
Overall Accuracy	I_{VREF} = 0 to -10mA	**4.900**	5.00	**5.075**	V
Long Term Stability	T_A = +125°C, 1000 hours		3		mV
Operational Current (Source)		**-10**			mA
Current Limit		**-25**		**-100**	mA
CURRENT SENSE					
Current Limit Threshold, ISET Minimum				**0.35**	V
Current Limit Threshold, ISET Maximum		**1.000**	1.125		V
CS to OUT Delay			100		ns
CS to PWM Comparator Offset	V_{SLOPE} = 0V	**90**	100	**110**	mV
CS Discharge Device, $r_{DS(ON)}$			15	**31**	Ω
CS Input Bias Current		**-1**		**1**	µA
ISET Input Bias Current		**-1**		**1**	µA
Leading Edge Blanking (LEB) Duration		**75**	100	**130**	ns

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and the Typical Application schematics on pages 5 and 6. 8V < V_D < 20V, R_{TC} = 10.0kΩ, C_T = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
IOUT Buffer Gain	T_A = +25°C	3.90	4.00	4.12	V/V
IOUT VOH	Δ_{VOH}, ($VOH_{ILOAD=0\mu A}$ - $VOH_{ILOAD=-300\mu A}$), CS = 0.5V, ISET = 1.00V		0.05	**0.2**	V
IOUT VOL	I_{LOAD} = 100µA, CS = 0V, ISET = 1.00V	**0.05**	0.1	**0.15**	V
SLOPE COMPENSATION					
Charge Current	SLOPE = 2V	**-90**	-100	**-110**	µA
Slope Compensation Gain	Fraction of slope voltage added to CS	**0.190**	0.200	**0.210**	V/V
SLOPE Discharge Device, $r_{DS(ON)}$				**50**	Ω
SLOPE Range, Linear Response		**0**		**2.5**	V
PULSE WIDTH MODULATOR					
Minimum Duty Cycle	MODE = 5V, VERR < 0.6V			**0**	ns
	MODE = 0V, VERR < 0.6V	**270**	300	**350**	ns
Maximum Duty Cycle	4.8 < VERR < VREF, UV = 4.2V, DCLIM > 4.0V	**76**	80	**84**	%
	RTC = 25.5kΩ, CT = 220pF		80		%
SS to PWM Comparator Input Gain		**0.23**	0.25	**0.27**	V/V
VERR to PWM Comparator Input Gain		**0.28**	0.30	**0.32**	V/V
VERR to PWM Comparator Input Offset		**0.60**	0.80	**1.00**	V
OUTM TO OUTAC DELAY TIMING					
DELAY Gain	Overlap, T_A = +25°C	1.54	1.83	2.11	ns/kΩ
	Non-Overlap, T_A = +25°C	1.54	1.79	2.11	ns/kΩ
DELAY Range		**50**		**500**	ns
DELAY Disable, High		**4.9**			V
DELAY Disable, Low				**0.100**	V
OSCILLATOR					
Frequency Accuracy	T_A = +25°C	326	338	349	kHz
Frequency Variation with VDD	T_A = +105°C, $\lvert(F_{20V} - F_{8V})/F_{8V}\rvert$, UV = 2.00V (Note 7)		0.1	0.3	%
	T_A = +25°C, $\lvert(F_{20V} - F_{8V})/F_{8V}\rvert$, UV = 2.00V		0.2	0.6	%
	T_A = -40°C, $\lvert(F_{20V} - F_{8V})/F_{8V}\rvert$, UV = 2.00V (Note 7)		0.6	8.0	%
Frequency Variation with UV	T_A = +25°C, $\lvert(F_{4.25V} - F_{2.00V})/F_{2.00V}\rvert$ VDD = 8V		0.1	1.5	%
	VDD = 20V		0.3	5.2	%
Temperature Stability	UV = 2.0V, VDD = 8V		0.5	**1.5**	%
Charge Current Gain	RTC = 10.0kΩ, 100kΩ	**1.88**	2.0	**2.12**	µA/µA
Discharge Current Gain	RTC = 10.0kΩ, 100kΩ	**6.0**	7.2	**8.2**	µA/µA
CT Valley Voltage	Static operation	**0.75**	0.80	**0.85**	V
CT Peak Voltage	Static operation UV = 2.00V	**2.30**	2.40	**2.50**	V
	UV = 4.00V	**3.80**	4.00	**4.20**	V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and the Typical Application schematics on pages 5 and 6. 8V < V_D < 20V, R_{TC} = 10.0kΩ, C_T = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
RTC Voltage	R_{LOAD} = Open UV = 2.00V	**1.55**	1.60	**1.65**	V
	UV = 4.00V	**3.10**	3.20	**3.30**	V
SOFT-START					
ISS Charge Current	SS = 2V	**-45**	-55	**-65**	µA
ISS Discharge Current, Absolute Value	MODE = 0V, SS = 2V	**-45**	-55	**-65**	µA
SS Clamp Voltage		**4.5**	4.6	**4.7**	V
Reset Threshold Voltage	SS decreasing	**0.15**	0.20	**0.25**	V
SS Discharge Current	MODE = 5V, SS = 2V		10.0		mA
UV UNDERVOLTAGE					
Input Voltage Low/Inhibit Threshold		**0.97**	1.00	**1.03**	V
Hysteresis, Switched Current Amplitude		**6.2**	10	**14**	µA
Input High Clamp Voltage		**4.8**			V
Input Impedance		**1**			MΩ
Maximum Control Voltage		**4.20**		**VREF**	V
OUTPUT OUTM, OUTAC					
High Level Output Voltage (VOH) OUTM	VDD - V_{OUTM} or V_{OUTAC}			**0.5**	V
OUTAC	I_{OUT} = -100mA			**1.0**	V
Low Level Output Voltage (VOL) OUTM	I_{OUT} = 100mA			**0.5**	V
OUTAC				**1.0**	V
Rise Time OUTM	C_{GATE} = 1nF, V_{DD} = 8V		15	**30**	ns
OUTAC			30	**60**	ns
Fall Time OUTM	C_{GATE} = 1nF, V_{DD} = 8V		10	**20**	ns
OUTAC			20	**40**	ns
UVLO Output Voltage Clamp	VDD = 5V OUTM, OUTAC I_{LOAD} = 1mA			**1.5**	V
DCLIM					
Input Bias Current		**-1**		**1**	µA
Maximum Control Voltage		**4.00**		**VREF**	V
MODE					
High Level Input Voltage (VIH)		**2**			V
Low Level Input Voltage (VIL)				**0.8**	V
Pull-up Resistance, Internal			100		kΩ

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to the Block Diagram on page 4 and the Typical Application schematics on pages 5 and 6. 8V < V_D < 20V, R_{TC} = 10.0kΩ, C_T = 470pF, T_A = -40°C to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
ENABLE					
High Level Input Voltage (VIH)		**2**			V
Low Level Input Voltage (VIL)				**0.8**	V
Pull-up Resistance, Internal			275		kΩ
ERROR AMPLIFIER					
Operating Input Range	VERR = FB, ISET = 0V, 4V	**0**		**4.00**	V
Unity Gain Band-Width Product			8		MHz
FB Bias Current		**-1**		**1**	µA
VERR VOL	I_{LOAD} = 5mA, FB = VREF, ISET = 1V			**0.40**	V
VERR Pull-up Current Source	VERR = FB = 0V, ISET = 1V		100		µA
SYNCHRONIZATION					
VIL				**0.8**	V
VIH		**2.0**			V
VOL	I_{LOAD} = 10µA			**100**	mV
VOH	I_{LOAD} = -1.0mA	**4.0**	4.5		V
Source Current	VOH > 2.0V		-10		mA
Sink Current	VOL < 2.5V		10		mA
Output Duration		**200**		**575**	ns
Input Duration, Minimum		**100**			ns
Maximum Frequency, Input		**2**			MHz
THERMAL PROTECTION					
Thermal Shutdown			145		°C
Thermal Shutdown Clear			130		°C
Hysteresis, Internal Protection			15		°C

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

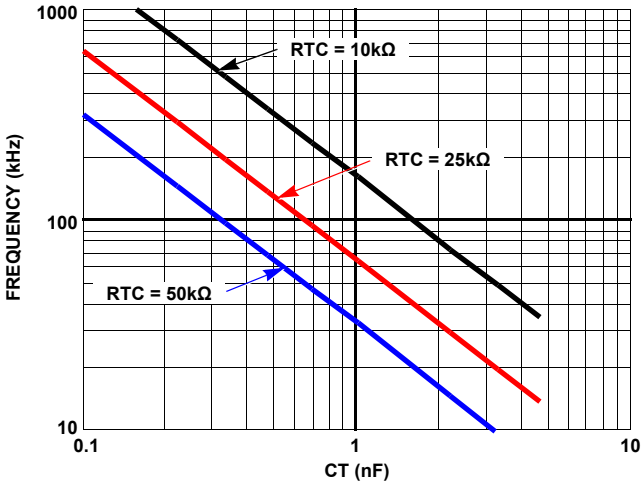


FIGURE 1. OSCILLATOR FREQUENCY vs CT and RTC

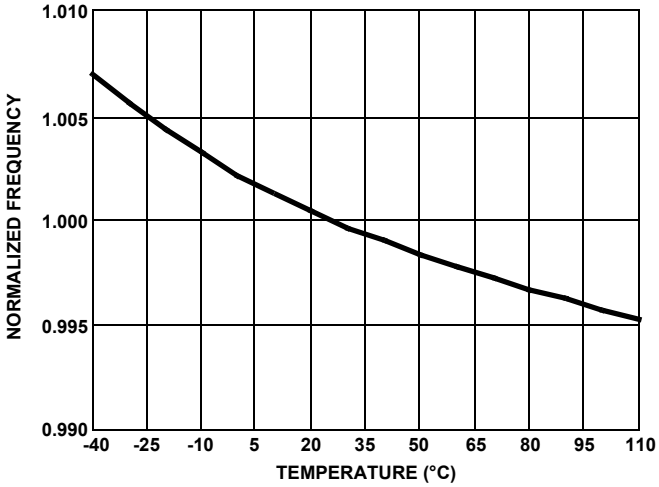


FIGURE 2. OSCILLATOR FREQUENCY vs TEMPERATURE

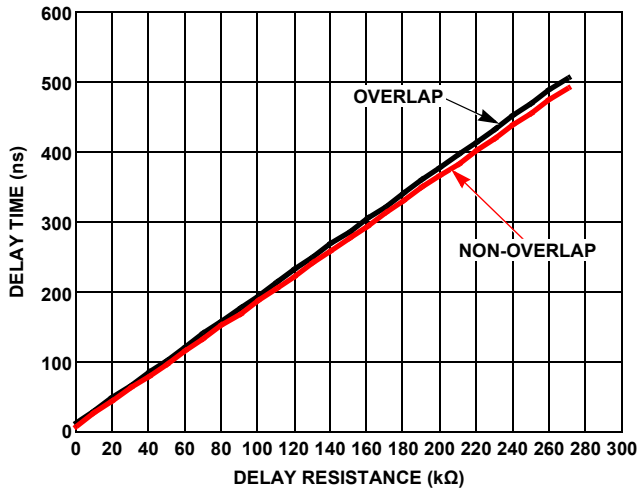


FIGURE 3. DELAY TIME vs RESISTANCE

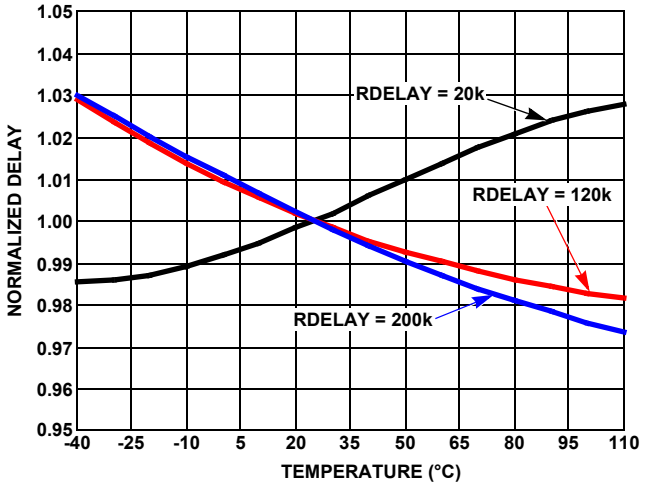


FIGURE 4. DELAY TIME vs TEMPERATURE (OVERLAP)

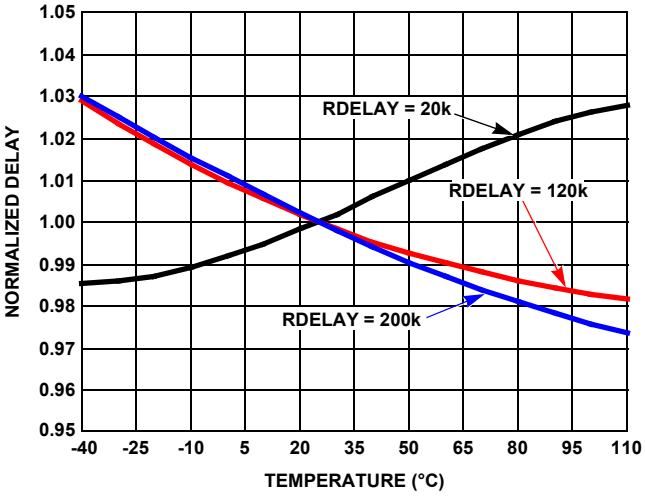


FIGURE 5. DELAY TIME vs TEMPERATURE (NON-OVERLAP)

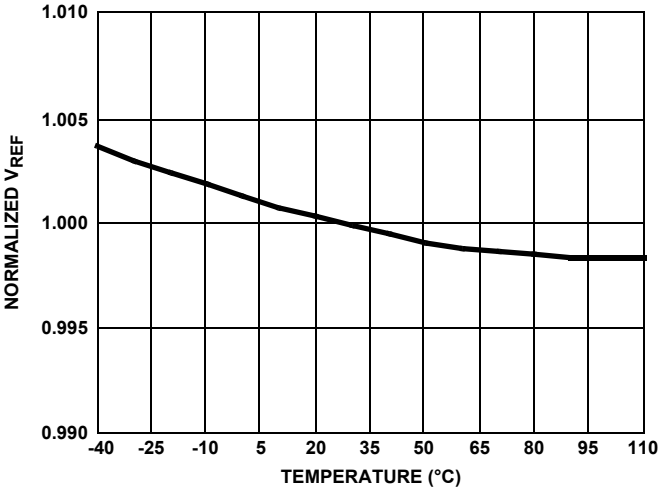


FIGURE 6. VREF vs TEMPERATURE

Functional Description

Features

The ISL6726 PWM is an excellent choice for low cost high performance applications requiring D (duty cycle) and 1-D control signals. This includes active clamp forward, asymmetric half-bridge, and synchronous rectified (SR) standard forward and flyback topologies. Among its many features are:

- High current FET drivers
- Adjustable soft-start and soft-stop
- Slope compensation
- Programmable deadtime control
- Overlapping and non-overlapping output configuration for both n-channel and p-channel clamp configurations
- Peak and average overcurrent protection
- Internal thermal protection
- Minimum duty cycle clamp
- Input voltage dependent maximum duty cycle clamp

Supply Currents

The total supply current, IDD, will be dependent on the load applied to outputs OUTM and OUTAC. Total IDD current is the sum of the quiescent current and the average output current. Knowing the operating frequency (F_{SW}) and the output loading capacitance charge (Q) per output, the average output current can be calculated from Equation 1:

$$I_{OUT} = 2 \bullet Q \bullet F_{SW} \quad \text{(EQ. 1)}$$

Oscillator

The ISL6726 oscillator has a programmable frequency range to 2MHz, and can be set with one resistor and one capacitor. The use of two timing elements, RTC, and CT allow great flexibility and precision when setting the oscillator frequency.

The switching period is the sum of the timing capacitor charge and discharge durations. The charge and discharge duration is determined by RTC and CT.

$$t_C \approx 0.5 \bullet RTC \bullet CT \quad S \quad \text{(EQ. 2)}$$

$$t_D \approx 0.125 \bullet RTC \bullet CT \quad S \quad \text{(EQ. 3)}$$

$$t_{SW} = T_C + T_D = \frac{1}{F_{SW}} \quad S \quad \text{(EQ. 4)}$$

Where t_C and t_D are the charge and discharge times, respectively, t_{SW} is the oscillator free running period, and F_{SW} is the oscillator frequency. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 10ns/transition. This delay adds directly to the switching duration, but also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very low charge and discharge currents are used, there will be increased error due to the input impedance of the CT pin.

The timing component tolerance directly effects the oscillator accuracy. A NPO/COG dielectric ceramic capacitor or better is suggested for CT. RTC should be 1% tolerance or better.

Figure 1 graphically portrays the oscillator frequency as function of the timing components. The minimum deadtime is fixed at 20% of the period allowing an 80% maximum duty cycle. This limits the maximum voltage stress on the power MOSFETs to 5x the input voltage. For applications that cannot tolerate this voltage stress, the maximum duty cycle can be reduced using the DCLIM feature. The peak voltage stress for an active clamp topology is approximately $V_{IN}/(1\text{-}D)$.

Soft-Start/Soft-Stop Operation

The ISL6726 features a soft-start using an external capacitor in conjunction with an internal current source. Soft-start reduces stresses and surge currents during start-up. Soft-stop reduces electrical stresses during shutdown when synchronous rectifiers (SRs) are used and prevents polarity reversal of the converter output. Soft-stop may be inhibited with MODE for applications not using SRs.

The soft-start feature clamps the duty cycle for the duration of soft-start. The duty cycle is initially forced to zero and allowed to linearly increase until the control loop takes control. At the beginning of a soft-start cycle, the SS capacitor is discharged. If ENABLE is open and there is no UVLO fault on VDD, a current source charges the soft-start capacitor. Taking into account the internal gains and offsets of VERR and SS, soft-start limits the peak current amplitude as long as it remains below VERR. As the SS voltage increases, the peak current amplitude is allowed to increase. The output pulse width increases accordingly, until the SS voltage exceeds VERR and the control loop takes over. The SS voltage will continue to increase until it reaches its clamp voltage of 4.6V even though soft-start is actually finished when the control loop takes over. The duty cycle increases from zero to its steady state operating point during the soft-start period. The soft-start waveform is shown in Figure 7 for the non-overlap configuration, appropriate for the active clamp forward with a n-channel clamp FET or the asymmetric half-bridge topology. For the active clamp topology using a p-channel clamp FET, the overlap configuration is required and the OUTAC waveform shown in Figure 7 would be inverted. The non-overlap configuration is shown for clarity.

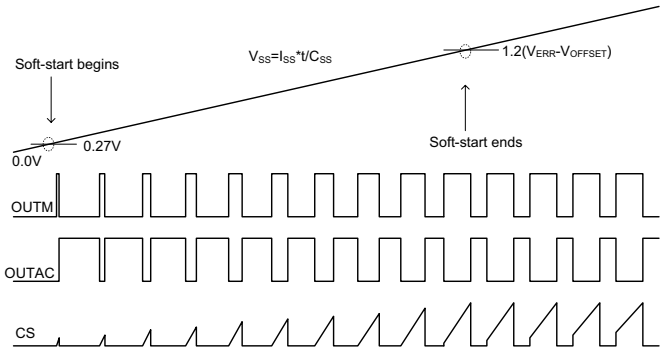


FIGURE 7. SOFT-START FUNCTION (I_{DELAY} POSITIVE)

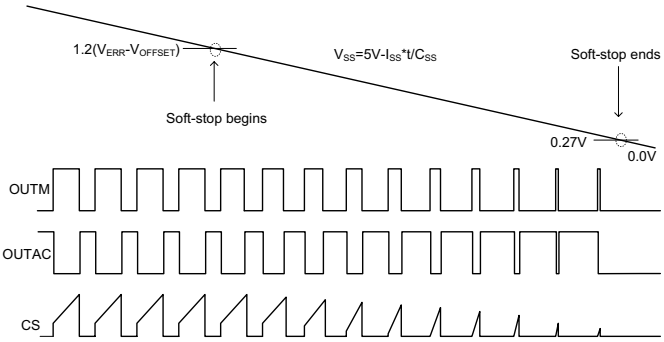


FIGURE 8. SOFT-STOP FUNCTION (I_{DELAY} POSITIVE)

The soft-stop function is enabled when MODE=0. The ISL6726 enables a soft-stop when UV falls below 1V or when ENABLE is pulled low (disable), causing a controlled discharge of the SS capacitor at the rate equal to and opposite of soft-start. Soft-stop will not occur for a UVLO fault on VDD regardless of the MODE setting. Soft-stop continues until the SS pin voltage drops below ~0.25V, even if the fault condition is removed before the threshold is reached.

Using soft-stop forces an orderly shutdown of a converter that uses synchronous rectification (SR). It prevents the output voltage from going negative by controlling the rate at which the output voltage is discharged through the output inductor. It also prevents the SRs from being avalanched if SR operation is stopped when the inductor current is negative.

If a self-driven SR method is used, the behavior during turn-off is improved as well. During soft-stop, the forward rectifier pulse width is slowly decreased to its minimum while the free-wheeling rectifier pulse width is slowly increased to its maximum. The active clamp capacitor voltage, $V_{IN}/(1-D)$, approaches V_{IN} as the duty cycle approaches zero. The freewheeling rectifier gate voltage is V_{IN} D/n(1-D), where n is the transformer turns ratio Np/Ns, and decreases with decreasing duty cycle. At some point the voltage applied to the gate is insufficient to turn on the SR FET and negative inductor current is prevented.

A hard-stop with self-driven SRs results in oscillation of the SRs because the output voltage can provide gate voltage through the output inductor and secondary winding.

Minimum Duty Cycle Clamp

In addition to soft-stop when MODE=0, the minimum pulse width of OUTM is clamped to ~300ns independent of the PWM modulator. Higher duty cycles are obviously allowed depending on the operating conditions, but shorter duty cycles are not. In SR applications, this feature prevents excessive negative output inductor current if the output should experience a large and sudden reduction in load, such as occurs during a 100% to 0% load transient. A sudden load dump can cause the control loop error voltage to drop sufficiently to command 0% duty cycle. This sets the forward rectifier to 0% duty cycle and the free-wheeling rectifier to 100% duty cycle. This condition allows the inductor current to ramp to a large negative amplitude until the duty cycle again becomes non-zero. Due to the normal deadtime allowed for proper switching of the SRs, the forward rectifier will avalanche when the duty cycle becomes non-zero. When the forward SR turns on, the inductor current will reflect to the primary and stress the components there as well. With the minimum duty cycle clamp feature, the forward rectifier turns on for ~300ns each cycle and prevents the large negative current in the output inductor.

Gate Drive

The ISL6726 has two outputs, OUTM and OUTAC. OUTM is capable of sourcing 1A and sinking 1.5A peak current, and OUTAC is capable of sourcing 0.5A and sinking 0.75A peak current. OUTAC is configured using the DELAY input for either overlap or non-overlap phasing relative to OUTM. When configured for non-overlap phasing, OUTAC operates at 1-D with deadtime, where D is the duty cycle of OUTM. This configuration is useful for the n-channel active clamp and asymmetric half-bridge topologies. When configured for overlap phasing, OUTAC has symmetric rising edge advance and falling edge delays relative to OUTM. This configuration is useful for the p-channel active clamp topology.

Two typical active clamp converter configurations are shown in Figures 9 and 10, with overlap or non-overlap delay time accurately set by a programming resistor. The rising edge overlap and the falling edge overlap time (or rising edge deadtime, and falling edge deadtime) are equal and independent of the operating frequency or duty cycle.

To limit the peak current through the IC, an external resistor may be placed in series between an output and the gate of the MOSFET. The resistor also dampens any oscillation caused by the resonant tank of the parasitic inductance of the PWB traces and the FET gate input capacitance. The overlap/non-overlap delay between OUTAC and OUTM prevents simultaneous conduction of the main and clamp switches in an active clamp converter, or the upper and lower switches in an asymmetric half- bridge converter.

Table 1 shows the combinations of the settings with the corresponding features for different topologies.

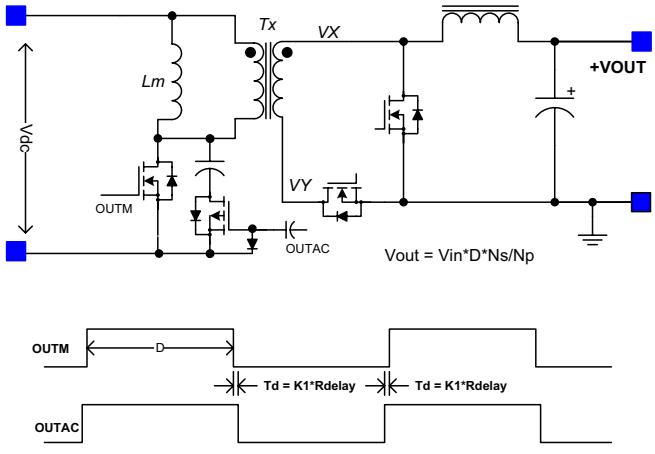


FIGURE 9. OUTPUT TIMING DIAGRAM FOR P-CHANNEL ACTIVE CLAMP

TABLE 1. MODE AND DELAY SETTINGS FOR TYPICAL TOPOLOGIES

TOPOLOGY	MODE	DELAY	PHASING	SOFT-STOP	MINIMUM D CLAMP
N-FET Active Clamp with Diode Rectification	HIGH	R to VREF	Non-OverLap	Disabled	Disabled
P-FET Active Clamp with Diode Rectification	HIGH	R to GND	OverLap	Disabled	Disabled
N-FET Active Clamp with SR Rectification	LOW	R to VREF	Non-OverLap	Enabled	Enabled
P-FET Active Clamp with SR Rectification	LOW	R to GND	OverLap	Enabled	Enabled
Standard Forward with Diode Rectification	HIGH	= 0V, = VREF	OverLap, Non-Overlap	Disabled	Disabled
Asymmetric Half-Bridge	LOW	R to VREF	Non-OverLap	Enabled	Enabled

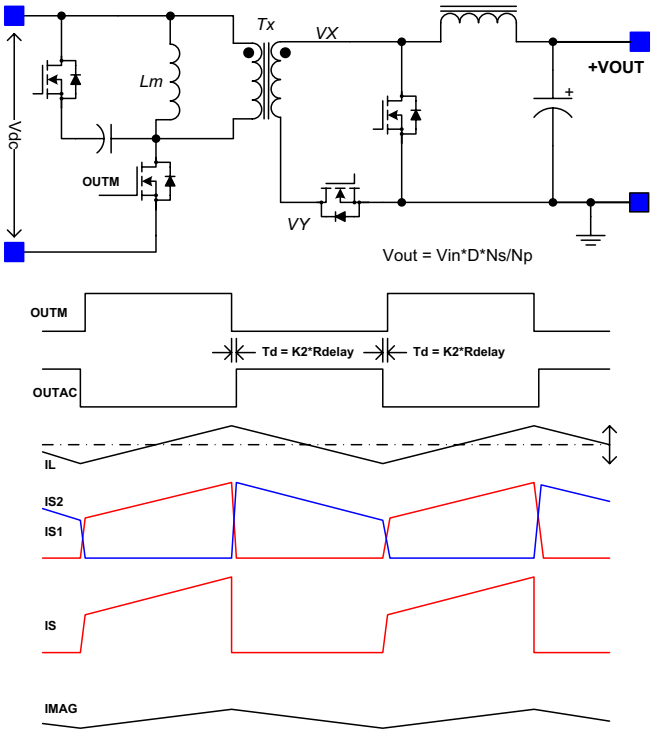


FIGURE 10. OUTPUT TIMING DIAGRAM FOR N-CHANNEL ACTIVE CLAMP

Overlap phasing results when a resistor is connected between DELAY and GND. Non-overlap phasing results when a resistor is connected between DELAY and VREF. The resistor value determines the magnitude of the delay. The delay feature may be disabled by connecting DELAY directly to GND or VREF, depending on which configuration is desired, overlap or non-overlap. The non-overlap time in the overlap mode can be calculated using Equation 5.

$$t_{DELAY} = 1.83\frac{ns}{k\Omega} \cdot R_{DELAY}(k\Omega) + 13ns \quad \text{(EQ. 5)}$$

The deadtime in non-overlapping mode can be calculated using Equation 6.

$$t_{DELAY} = 1.79\frac{ns}{k\Omega} \cdot R_{DELAY}(k\Omega) + 9ns \quad \text{(EQ. 6)}$$

See Figure 3 for typical DELAY gain curves.

Overcurrent Operation

The ISL6726 has two mechanisms for current limit. The peak current limit function provides cycle-by-cycle overcurrent protection. The protection threshold is set by a voltage applied to ISET. If the peak current at CS exceeds ISET, the OUTM pulse is terminated for the remainder of the switching cycle.

Peak current limit has some shortcomings that discourage its use as the only current limit mechanism. First, there is the slope compensation ramp that adds to the current feedback signal. Its contribution to the CS signal varies with duty cycle, and at high duty cycles it has a larger contribution than at lower duty cycles. As an overload condition causes the duty cycle to decrease, the portion of the current feedback contributed by the slope compensation decreases and the amount contributed by the current feedback increases. The result is that the maximum output current will increase as the output voltage decreases.

Another phenomenon occurs when the duty cycle is reduced to the minimum pulse width the IC controller is capable of producing. If the output voltage is reduced below the value corresponding to this duty cycle, current tail-out occurs. There is a certain amount of energy delivered to the output on each switching cycle that must correspond to voltage and current at the load. If the voltage is very low due to a shorted output, large currents can result.

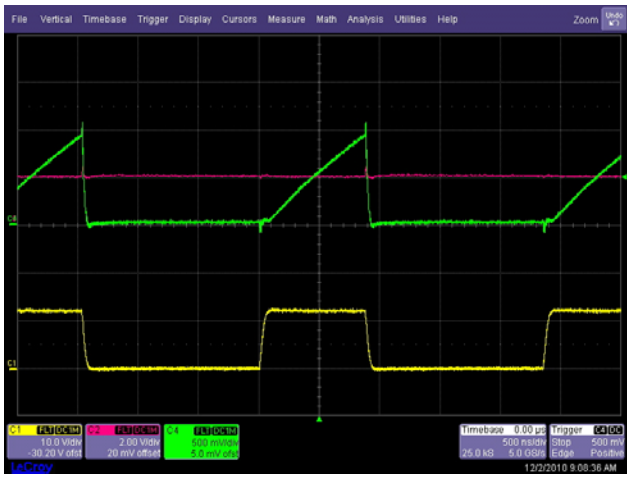
Some controllers solve the problem by allowing the converter to cycle on and off (hic-cup operation) to lower the average short circuit current. This works acceptably for some applications, but not when redundancy or parallel operation is required. Such behavior can prevent a successful fault recovery when the short is removed. The paralleled or redundant units will not hic-cup in unison, and each will experience an overload condition each time a restart is attempted.

An ideal current limiting method requires a constant value regardless of the output voltage, the so-called “brick-wall” current limit. The output current remains constant from current limit inception to a short circuit. The ISL6726 provides this behavior with the average current limit function.

The average current limit feature uses a patented circuit that samples the current feedback signal and creates a signal proportional to the average value of the output inductor current. The signal, analogous to the voltage feedback signal of voltage control loop, becomes the feedback signal for the current error amplifier and produces a current error signal. The voltage feedback and current feedback share a common control node

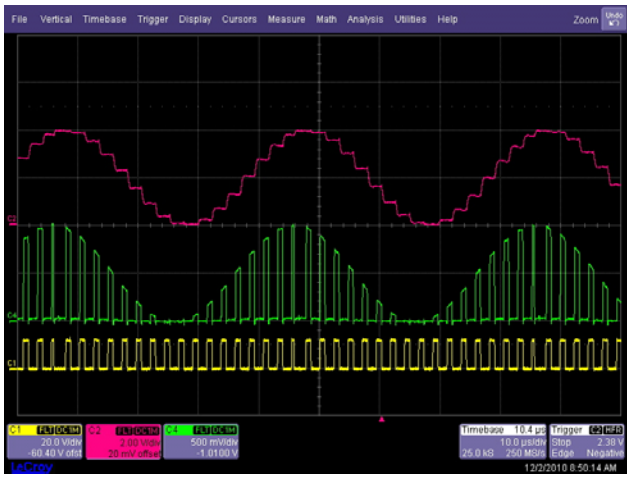
(VERR) used by the pulse width modulator. Whichever error signal, voltage or current, that commands the lower duty cycle is in control. If the average current is lower than the average current limit threshold, the current error amplifier has no impact on VERR and the voltage loop is in control. If the average current limit threshold is exceeded, however, the current error amplifier will lower VERR to regulate the output current. The voltage loop loses control as it must increase the duty cycle to maintain the output voltage in regulation.

After a 100ns leading edge blanking (LEB) delay, the current sense signal is sampled for the duration of the on time, the average current is determined, and the result is amplified by 4x and output to the IOUT pin at the termination of the OUTM pulse. Due to the sampling algorithm used, if an RC filter is placed on the CS input, its time constant should not exceed ~30ns or error may be introduced on IOUT.



Channel 1: OUTM Channel 2: IOUT Channel 4: CS

FIGURE 11. CS INPUT vs IOUT



Channel 1: OUTM Channel 2: IOUT Channel 4: CS

FIGURE 12. DYNAMIC BEHAVIOR OF CS AND IOUT

The average current signal on IOUT produces an accurate representation of the output current provided the converter operates in continuous conduction mode (CCM). Once the inductor current becomes discontinuous (DCM operation), IOUT represents one half of the peak inductor current rather than the average current. This occurs because the sample and hold circuitry is active only during the on time of the switching cycle and cannot determine when the inductor current becomes discontinuous. It is unable to detect when the inductor current reaches zero during the off time. This behavior does not affect the average current limit function, but does have an impact if IOUT is used for current monitoring functions.

IOUT may be used with the available error amplifier (EA) of the ISL6726 as shown in Figure 13. The error amplifier is typically configured as an integrator. As shown in Figure 13, IOUT is attenuated by resistors R_1 and R_2 so that the average current limit threshold can be set independently of the peak current limit threshold. The integrator bandwidth is determined by R and C. The current error amplifier is similar to the voltage EA found in most PWM controllers, except it cannot source current. VERR requires an external pull-up resistor.

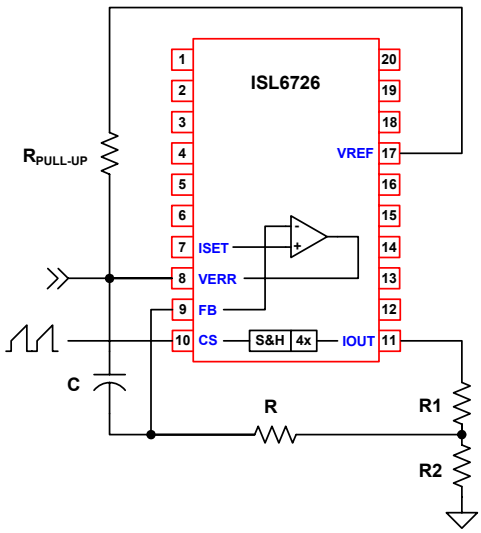


FIGURE 13. AVERAGE CURRENT CONFIGURATION

The IEA is configured as an integrating (Type I) amplifier using ISET as the reference. The voltage applied at FB is integrated against the ISET reference. The resulting signal, VERR, is applied to the PWM comparator where it is compared to the current signal CS. If FB is less than ISET, the IEA will be open loop (can't source current), VERR will be at a level determined by the voltage loop, and the duty cycle is unaffected. As the output load increases, IOUT will increase, and the voltage applied to FB will increase until it reaches ISET. At this point the IEA will control VERR as required to maintain the output current at the level that corresponds to the ISET reference. When the output current again drops below the average current limit threshold, the IEA returns to an open loop condition, and the duty cycle is again controlled by the voltage loop. The average current control loop behaves much the same as the voltage control loop found in typical power supplies except it regulates current rather than voltage.

The average current loop bandwidth is normally set much lower than the switching frequency, typically less than 5kHz and maybe as slow as a few hundred hertz, depending on the application requirements. This is especially useful if the application experiences large surges. The average current loop can be set to the steady state overcurrent threshold and have a time response that is longer than the required transient.

Under some conditions it will be necessary to clamp the FB pin with a Schottky diode to signal ground. If the voltage loop causes a fast decreasing transient on VERR, the feedback capacitor between VERR and FB can cause a negative voltage on FB and violate the absolute maximum rating.

Duty Cycle Clamp

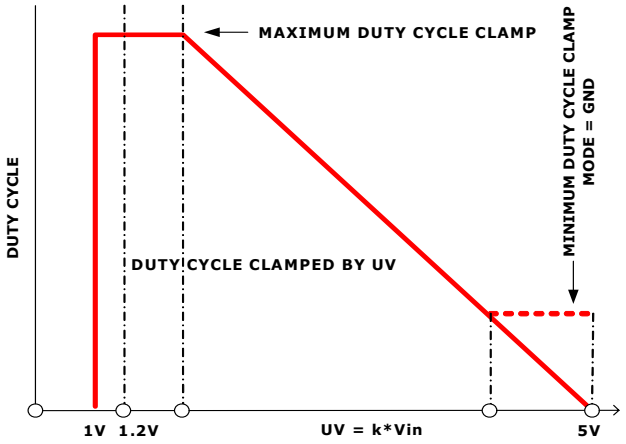


FIGURE 14. DUTY CYCLE CLAMP

It is very important to control the maximum duty cycle of an active clamp reset forward converter. The clamp capacitor and drain-source voltage of the main switch is related to the duty cycle D by Equation 7. If the duty cycle is not clamped, the FET drain-source voltage can become quite high and overstress the FET.

$$Vds = \frac{Vin}{(1-D)} \quad \text{(EQ. 7)}$$

Without the input voltage dependent maximum duty cycle clamp it is possible to have both high input voltage and high duty cycle during input voltage or load transients. The duty cycle clamp reduces the maximum duty cycle as the input voltage increases. Whereas the maximum duty cycle at minimum input voltage is large, it is not necessary, nor is it advantageous, to have the same maximum duty cycle at maximum input voltage. The duty cycle clamp allows the designer to provide a constant margin of duty cycle headroom above the steady state operating point to allow for adequate dynamic response without allowing so much headroom that it can result in excessive voltage stress on the FET.

During transients the situation is particularly bad, not only because of the voltage stress on the power FETs, but also because the clamp capacitor voltage is not at the steady state voltage required to properly reset the transformer. The active clamp forward topology is also know as the optimum reset topology because the steady state clamp capacitor voltage is exactly the value required to reset the core during the off time. However, it can take many switching cycles before the clamp capacitor voltage reaches a new steady state value after a change in operating point. If the clamp capacitor voltage is lower than required, the transformer core is not reset completely and can lead to transformer saturation after a few switching cycles.

This condition occurs when the input voltage is rapidly decreased, or when the output load is rapidly increased. Both of these conditions result in a rapidly increasing duty cycle. If the duty cycle can increase more quickly than the clamp capacitor voltage can respond, the core will not be properly reset. One or the other of these transients can be mitigated by the sizing of the clamp capacitor value. Smaller values favor input voltage transient behavior whereas larger values favor load transient behavior. Most designs favor load transient behavior. In either case, the maximum duty cycle clamp prevents large duty cycle increases and limits transformer flux density and FET voltage stress.

The main output PWM is controlled by the current and voltage feedback signals. When the feedback loop demands maximum duty cycle, the duty cycle is limited by the lesser of the input voltage-dependent duty cycle limiter or the maximum duty cycle limit of the controller, which is 80% by design.

The input voltage dependent duty cycle limit is inversely proportional to the input voltage, as shown in Figure 15. The voltage applied to UV determines the amplitude of the CT sawtooth waveform, where CT_{PEAK} = 0.8 + 0.8 * UV. Since the UV turn-on threshold is 1.00V, the minimum amplitude of CT is 1.60V. At UV = 4.00V, the amplitude of CT is 4.00V. The maximum duty cycle clamp is determined by the voltage applied to DCLIM and the amplitude of CT. If DCLIM is set to 1.60V or greater, the maximum duty cycle is 80%. The maximum duty cycle as a function of UV and DCLIM is:

$$D_{MAX} \begin{cases} = 0.8, DCLIM > 0.8 \cdot UV + 0.8 \\ = \frac{DCLIM - 0.8}{UV}, DCLIM \leq 0.8 \cdot UV + 0.8 \end{cases} \quad \text{(EQ. 8)}$$

For most applications the maximum duty cycle will be set for the minimum operating input voltage, and for which UV is set to 1.00V.

Consequently, the actual duty cycle of the main output, OUTM, is the minimum of the current mode PWM comparator, the maximum 80% duty cycle clamp of the controller, or the input voltage dependent duty cycle clamp.

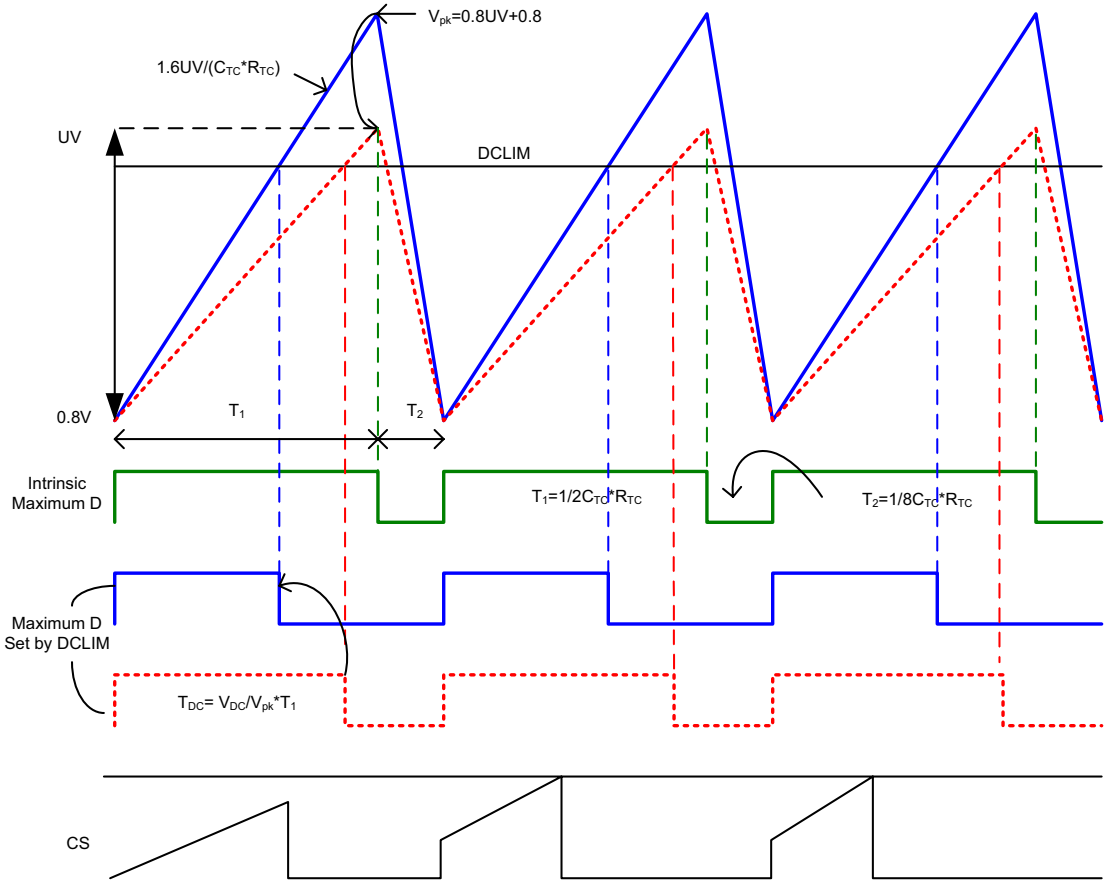


FIGURE 15. MAXIMUM DUTY CYCLE CLAMP USING DCLIM

Synchronization

ISL6726 provides a single I/O pin synchronization function that allows synchronization to an external clock or to self-synchronize to another unit at ~180 degrees out-of-phase for interleaved applications. When using an external clock, the clock pulse width must be a minimum of 100ns. The clock frequency must be higher than the free running frequency of the oscillator.

Multiple units may be synchronized together simply by connecting the SYNC pins together as shown in Figure 16. In this configuration all of the devices will synchronize out-of-phase with the master. The master is usually the unit with the fastest free-running oscillator, but may not be due to intentional hysteresis within the arbitration circuitry. Synchronization occurs on the leading edge of the SYNC signal. However, no unit will accept a SYNC pulse while its oscillator ramp voltage is less than 3/8 of the timing capacitor voltage peak voltage. This prevents short cycling of the period.

If the SYNC pins of multiple devices are connected together, the first SYNC signal that asserts will reset the oscillator RAMP of all other devices. Further arbitration may occur if there is a higher frequency unit present. All slave controllers will operate out-of-phase with the master. Multiple devices may be synchronized in this fashion, but the number will depend on the distance and capacitance of the SYNC signal path. Care should be taken to ensure the ground potential difference between devices is minimized. In most cases an external clock is used to synchronize more than two units.

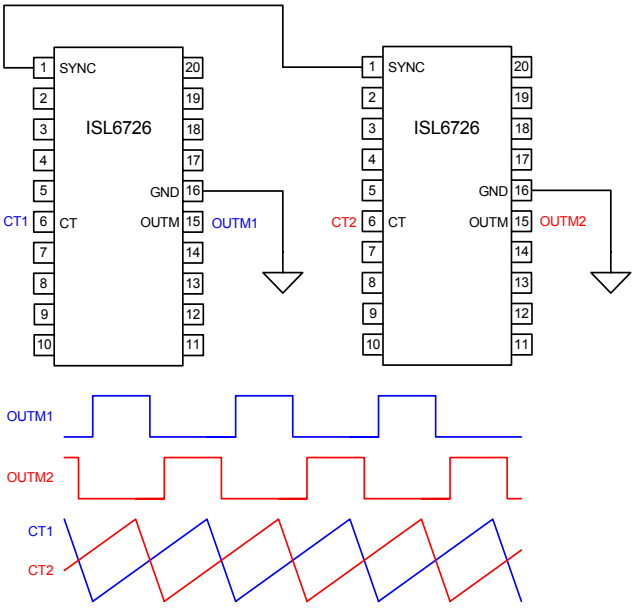


FIGURE 16. SYNCHRONIZING TWO UNITS

Configuring UV

The UV input is used for input source undervoltage lockout. If the UV node voltage falls below 1.00V, a UV shutdown fault occurs. This may be caused by low source voltage or by intentional grounding of the pin to disable the outputs. There is a nominal 10µA switched current source used to create hysteresis. The current source is active only during an UV/Inhibit fault; otherwise, it is inactive and does not affect the UV threshold voltage. The magnitude of the hysteresis is a function of the external resistor divider impedance. If the resistor divider impedance results in too little hysteresis, a series resistor between the UV pin and the divider may be used to increase the hysteresis. A soft-start cycle begins when the UV/Inhibit fault clears. The voltage hysteresis created by the switched current source and the external impedance is generally small due to the large resistor divider ratio required to scale the input voltage down to the UV threshold level.

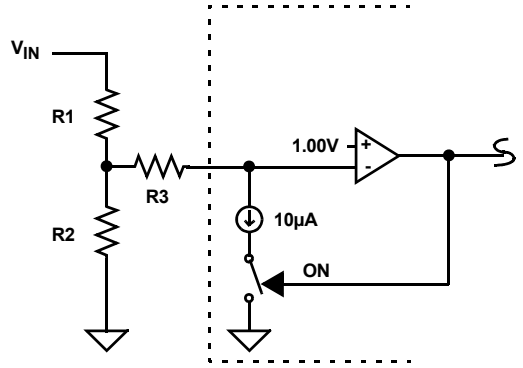


FIGURE 17. UV HYSTERESIS

Referring to Figure 17, as V_{IN} decreases to a UV condition, the threshold level is:

$$V_{IN(DOWN)} = \frac{R1 + R2}{R2} \quad V \qquad \text{(EQ. 9)}$$

The hysteresis voltage, ΔV, is:

$$\Delta V = 10^{-5} \bullet \left\langle R1 + R3 \bullet \left(\frac{R1 + R2}{R2}\right)\right\rangle \quad V \qquad \text{(EQ. 10)}$$

Setting R3 equal to zero results in the minimum hysteresis, and yields:

$$\Delta V = 10^{-5} \bullet R1 \quad V \qquad \text{(EQ. 11)}$$

As V_{IN} increases from a UV condition, the threshold level is:

$$V_{IN(UP)} = V_{IN(DOWN)} + \Delta V \quad V \qquad \text{(EQ. 12)}$$

Although the current hysteresis provides great flexibility in setting the magnitude of the hysteresis voltage, it is susceptible to noise on the signal. If the hysteresis was implemented as a fixed voltage instead, the signal could be filtered with a small capacitor placed between the UV pin and signal ground. This technique does not work well when the hysteresis is a current source because a current source takes time to charge the filter capacitor. There is no instantaneous change in the threshold level thereby rendering the current hysteresis ineffective. To remedy the situation the filter capacitor must be separated from the UV pin by a resistor. Referring to Figure 17, the filter capacitor must be placed in parallel with R2, and the capacitor and R3 must be physically close to the UV pin.

UV may also be used as an inhibit signal by externally pulling it below the 1V threshold. However, caution must be exercised as the maximum duty cycle limit controlled by DCLIM will be defeated. The peak amplitude of CT will be reduced to ~1.6V when UV decreases below the 1V turn-off threshold, and the maximum duty cycle allowed will increase to 80%.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal.

For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability, referred to as sub-harmonic oscillation. Slope compensation is a technique in which the current feedback signal is modified by adding slope, that is, adding a linearly increasing voltage as a function of time. The minimum amount of slope compensation required corresponds to 1/2 the inductor downslope, as it would appear referred to the CS input. See Figure 18. More may be added, but increasing the slope compensation arbitrarily results in a control loop that transitions into voltage mode as the slope compensation begins to dominate the current feedback signal.

The minimum amount of capacitance to place at the SLOPE pin is:

$$C_{SLOPE} = 18 \bullet \frac{t_{ON}}{V_{SLOPE}} \quad \mu F \qquad \text{(EQ. 13)}$$

Where t_{ON} is the maximum ON time in seconds, and V_{SLOPE} is the amount of voltage to be added as slope compensation to the current feedback signal at the CS pin. In general, the amount of slope compensation added is 2 to 3 times the minimum required.

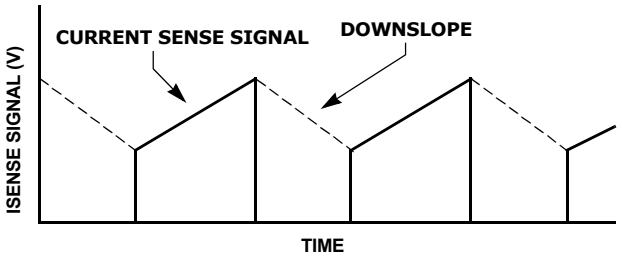


FIGURE 18. DOWNSLOPE

It should be noted that the power transformer magnetizing inductance contributes to slope compensation and should be considered when determining the amount of slope compensation required.

Example:

Assume the inductor current signal presented at the CS pin decreases 125mV during the Off period, and:

Switching Frequency, F_{sw} = 250kHz

Duty Cycle, D = 60%

$t_{ON} = D/F_{sw} = 0.6/250E3 = 2.4\mu s$

$t_{OFF} = (1 - D)/Fsw = 1.6\mu s$

Determine the downslope:

Downslope = 0.125V/1.6µs = 78mV/µs. Now determine the amount of voltage that must be added to the current sense signal by the end of the On time.

$$V_{SLOPE} = \frac{1}{2} \bullet 0.078 \bullet 2.4 = 94mV \quad \text{(EQ. 14)}$$

Therefore,

$$C_{SLOPE(MIN)} = 18 \times 10^{-6} \bullet \frac{2.4 \times 10^{-6}}{0.094} \approx 470pF \quad \text{(EQ. 15)}$$

An appropriate slope compensation capacitance for this example would be 1/2 to 1/3 the calculated value, or between 150pF and 220pF.

Using MODE

The MODE pin configures the IC for standard or synchronous rectification compatibility. If MODE is connected to VREF, standard rectification compatibility is selected. Soft-stop and the minimum duty cycle clamp are disabled. If MODE is connected to GND, synchronous rectification compatibility is selected, and soft-stop and the minimum duty cycle clamp are enabled.

Thermal Protection

An internal temperature sensor protects the device should the junction temperature exceed +145°C. There is approximately +15°C of hysteresis.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. Use a ground layer if possible. The power ground should be connected to the control ground at one point. VDD should be bypassed directly to GND with good high frequency capacitance, such as a ceramic capacitor. A small ceramic capacitor is also recommended for DCLIM.

The OUTM, and OUTAC of ISL6726 are very fast signals, and should have very short direct paths to the power MOSFETs in order to minimize inductance in the PC board traces. The return path should be as short as possible. The components at the Pins of SS, DCLIM, UV, DELAY, CT, and RTC should be as physically close as possible to the IC. Proximity to high di/dt loops and high dv/dt nodes should be avoided.

The CS signal requires proper filtering and the PWB layout is critical for normal operation of the current related functions. A RC filter may be required. The time constant should be no greater than 25ns to prevent incorrect average current information. If a current sense transformer is used, both leads of the secondary winding should be routed to the CS filter components and to the IC pins. The transformer return should be connected via a dedicated PC board trace to the GND pin rather than through the ground plane.

If a current sense resistor in series with the switching FET source is used, a low inductance resistor is recommended. The low level signals must avoid the high current path.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
January 31, 2011	FN7654.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL6726

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/sear

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

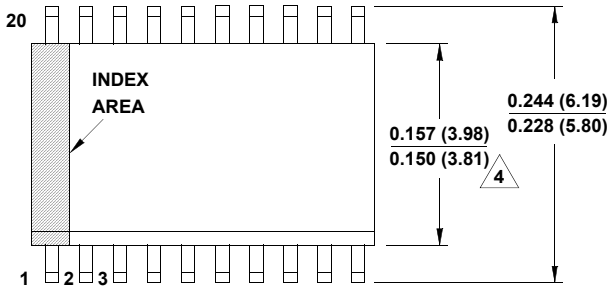
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

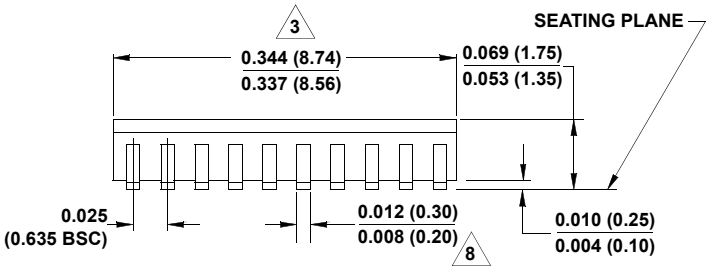
M20.15

20 LEAD QUARTER SIZE OUTLINE PLASTIC PACKAGE (QSOP)

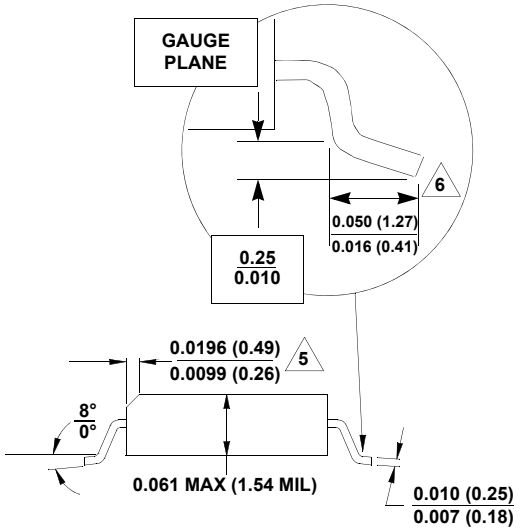
Rev 2, 1/11



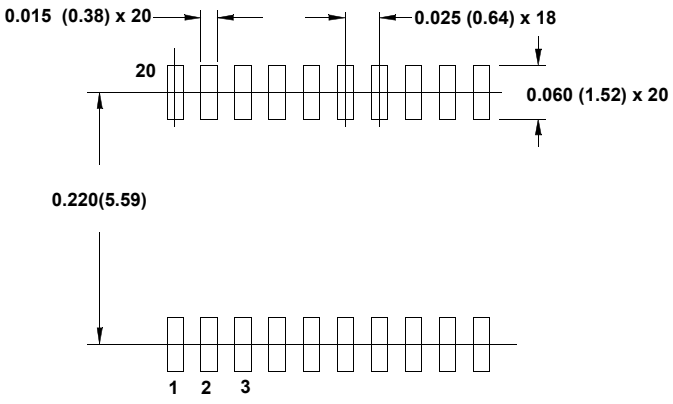
TOP VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Length of terminal for soldering to a substrate.
7. Terminal numbers are shown for reference only.
8. Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of dimension at maximum material condition.
9. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.