Features

- ESD Protect for 4 Lines with Uni-directional
- Provide Transient protection for each line directly to
  IEC 61000-4-2 (ESD) ±20kV (air), ±20kV (contact)
  IEC 61000-4-4 (EFT) 60A (5/50ns)
  IEC 61000-4-5 (Lightning) 5A (8/20μs)
- For low operating voltage applications: 3.3V maximum
- Fast turn-on and Low clamping voltage
- Array of surge rated equivalent TVS diodes
- **DFN2116P8X** package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green Part***

Applications

- Cellular Handsets and Accessories
- Small Panel Modules
- PDA's
- Portable Devices
- Digital Cameras
- Touch Panels
- Notebooks and Handhelds
- MP3 Players

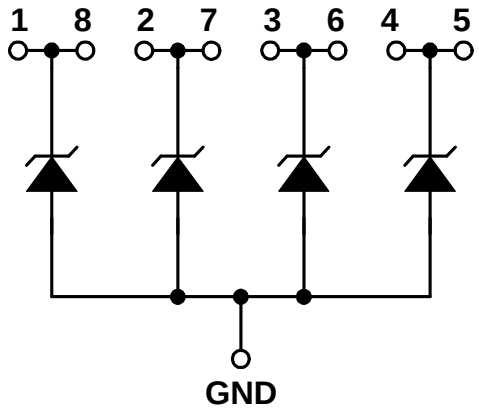
Description

AZ2113-04F is a design which includes surge rated clamping cell arrays to protect the power lines or data/control lines in an electronic systems. The AZ2113-04F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

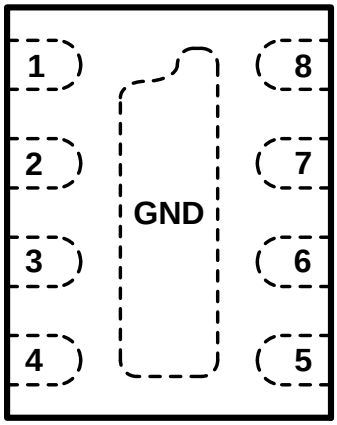
AZ2113-04F is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control lines, protecting any downstream components.

AZ2113-04F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



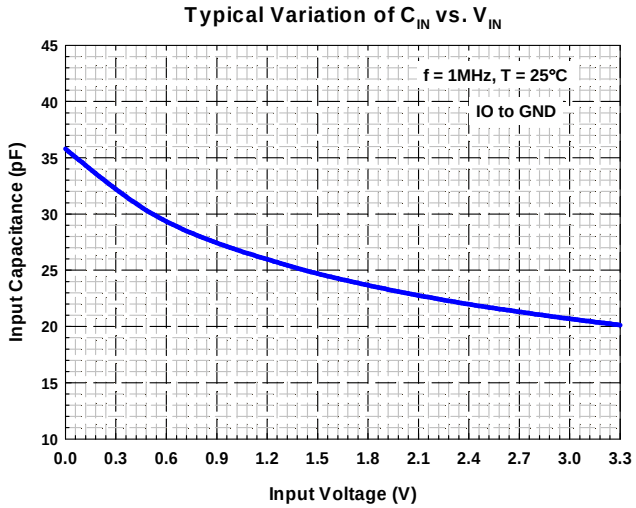
DFN2116P8X (Top View)

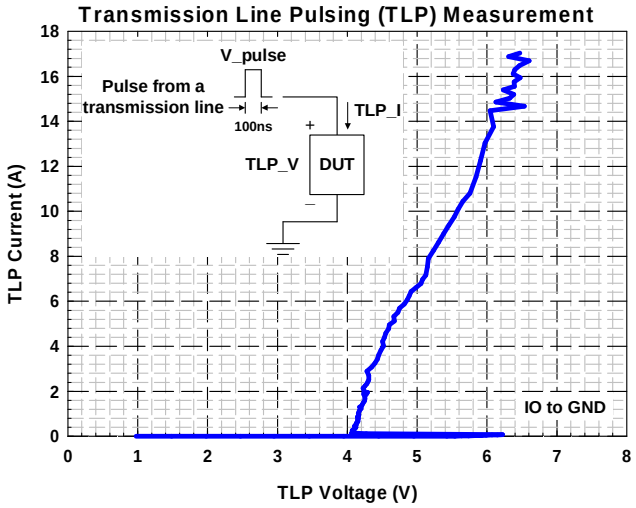
SPECIFICATIONS

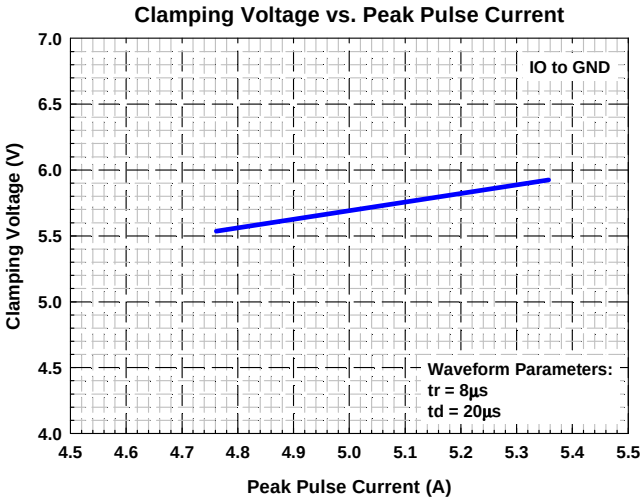
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
Operating Supply Voltage	V_{DC}	3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±20 ±20	kV kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

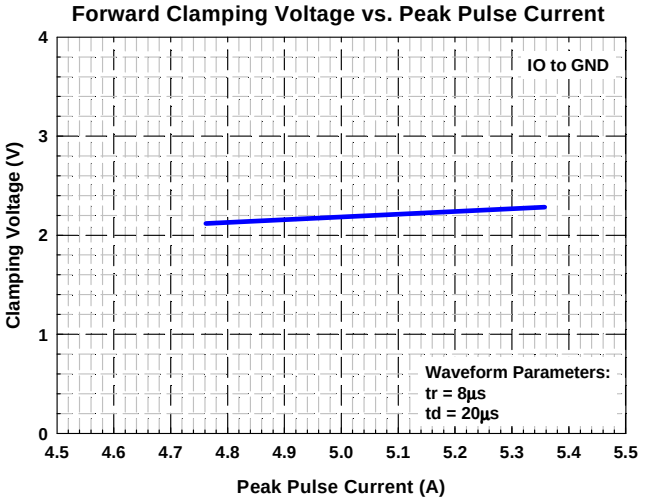
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1, -2, -3, -4, -5, -6, -7, -8 to GND pin, T=25 °C.			3.3	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 3.3V, Pin-1, -2, -3, -4, -5, -6, -7, -8 to GND pin, T=25 °C.			1	μA
Reverse DC Breakdown Voltage	V_{BV}	I_{BV} = 1mA, Pin-1, -2, -3, -4, -5, -6, -7, -8 to GND pin, T=25 °C.	4.5		6.5	V
Forward Voltage	V_F	I_F = 15mA, GND pin to Pin-1, -2, -3, -4, -5, -6, -7, -8, T=25 °C.	0.6		1.0	V
ESD Clamping Voltage	V_{ESD_CL}	IEC 61000-4-2 +6kV, Contact mode, Pin-1, -2, -3, -4, -5, -6, -7, -8 to GND pin, T=25 °C.		6.5		V
Lightning Clamping Voltage	$V_{lightning}$	I_{PP}=5A, tp=8/20μs, Pin-1, -2, -3, -4, -5, -6, -7, -8 to GND pin, T=25°C.		6.0		V
Channel Input Capacitance	C_{IN}	V_R= 0V, f = 1MHz, Pin-1, -2, -3, -4, -5, -6, -7, -8 to GND pin, T=25 °C.		36	40	pF

Typical Characteristics









Applications Information

The AZ2113-04F is designed to protect four lines against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ2113-04F is shown in Fig. 1. For ease of PCB layout, the AZ2113-04F is specifically designed for the use of flow-through layout by allowing the traces to enter one side of the device and exit the other side. Protected lines, such as data lines, control lines, or power lines, enter at the input pins of 1, 2, 3, 4 and exit from the opposite pins of 8, 7, 6, 5, respectively. The GND pin should be connected directly to a ground plane on the board.

In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ2113-04F should be kept as short as possible. In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ2113-04F.
- Place the AZ2113-04F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

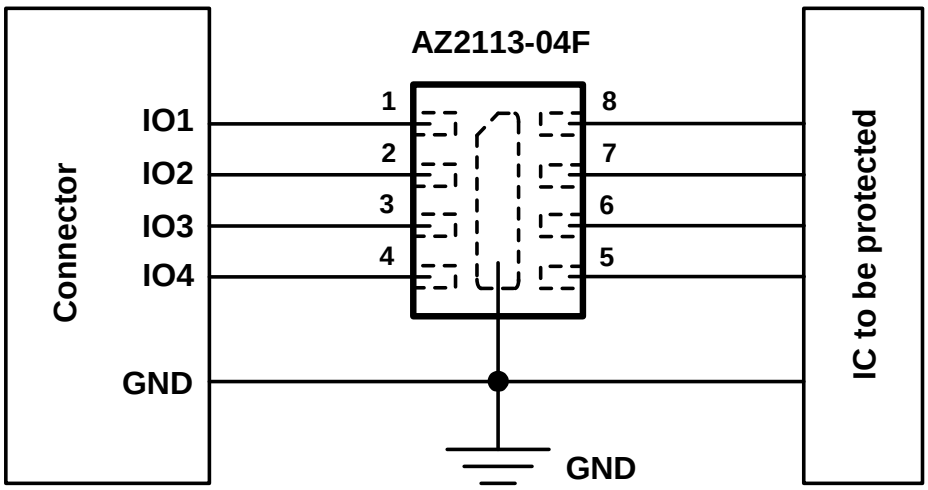


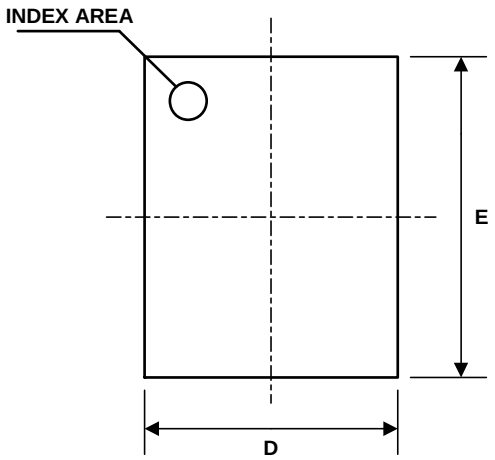
Fig. 1

Mechanical Details

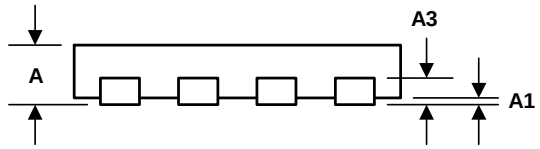
DFN2116P8X

PACKAGE DIAGRAMS

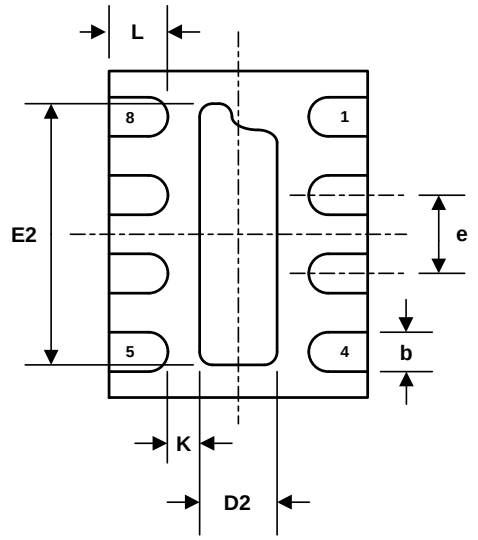
TOP VIEW



SIDE VIEW



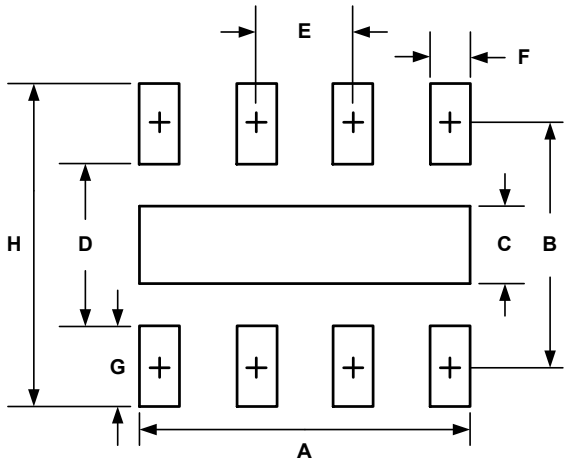
END VIEW



PACKAGE DIMENSIONS

SYMBOL	Millimeters		
	MIN.	NOMINAL	MAX.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3	-	0.127 Ref	-
b	0.20	0.25	0.30
D	1.60 BSC		
E	2.10 BSC		
e	0.50 BSC		
D2	0.35	0.40	0.45
E2	1.65	1.70	1.75
K	0.15	-	-
L	0.28	0.33	0.38

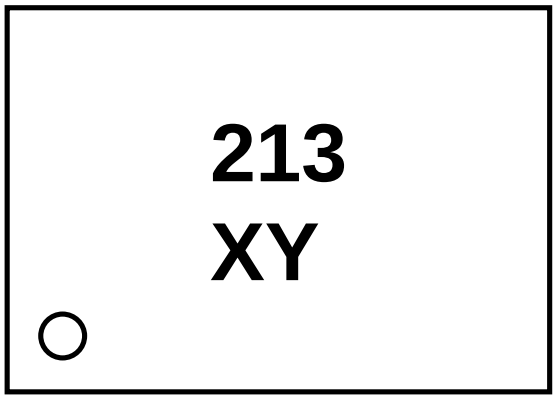
LAND LAYOUT



Dimensions	
Index	**Millimeter**
A	1.80
B	1.52
C	0.45
D	0.89
E	0.50
F	0.30
G	0.63
H	2.15

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



213=Device Code
X=Date Code
Y=Control Code

Part Number	Marking Code
AZ2113-04F (Green Part)	213 XY

Revision History

Revision	Modification Description
Revision 2013/02/08	Preliminary release.
Revision 2013/08/01	Formal release.