TPS748 1.5-A Low-Dropout Linear Regulator With Programmable Soft-Start

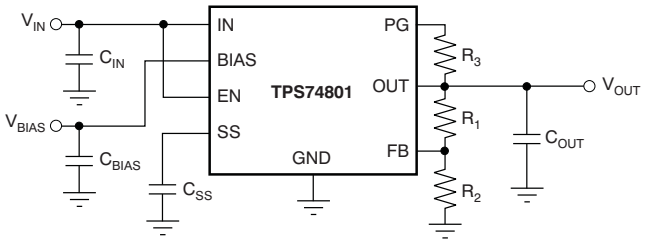
1 Features

- V_{OUT} Range: 0.8 V to 3.6 V
- Ultralow V_{IN} Range: 0.8 V to 5.5 V
- V_{BIAS} Range 2.7 V to 5.5 V
- Low Dropout: 60 mV Typical at 1.5 A, V_{BIAS} = 5 V
- Power Good (PG) Output Allows Supply Monitoring or Provides a Sequencing Signal for Other Supplies
- 2% Accuracy Over Line, Load, and Temperature
- Programmable Soft-Start Provides Linear Voltage Startup
- V_{BIAS} Permits Low V_{IN} Operation With Good Transient Response
- Stable With Any Output Capacitor ≥ 2.2 µF
- Available in a Small, 3-mm × 3-mm × 1-mm VSON-10 and 5 × 5 QFN-20 Packages

2 Applications

- FPGA Applications
- DSP Core and I/O Voltages
- Post-Regulation Applications
- Applications With Special Start-up Time or Sequencing Requirements
- Hot-Swap and Inrush Controls

Typical Application Circuit (Adjustable)



3 Description

The TPS748 low-dropout (LDO) linear regulator provides an easy-to-use robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

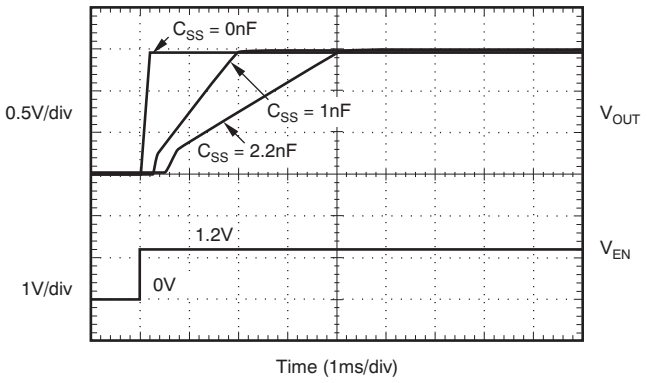
A precision reference and error amplifier deliver 2% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 2.2 µF, and is fully specified for T_J = –40°C to 125°C. The TPS748 is offered in a small, 3-mm × 3-mm, VSON-10 package, yielding a highly compact, total solution size. The device is also available in a 5 × 5 QFN-20 package for compatibility with the TPS744.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS748	VSON (10)	3.00 mm x 3.00 mm
	VQFN (20)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Turnon Response



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (January 2012) to Revision K **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed part number as printed in document from *TPS74801* to *TPS748* ... 1
- Changed *SON-10* package references in document to *VSON-10* ... 1
- Changed second paragraph of *Description* section ... 1
- Changed pin descriptions throughout *Pin Functions* table ... 4
- Changed condition statement for *Absolute Maximum Ratings* ... 5
- Changed "free-air" to "junction" temperature in condition statement for *Recommended Operating Conditions* ... 5
- Changed values for both packages in *Thermal Information* ... 6
- Changed test condition for output noise voltage from 0.001 µF to 1 nF ... 7
- Changed y-axis title in Figure 3 from abbreviation (I_{OUT}) to text (Output Current) ... 8
- Changed y-axis title in Figure 4 from abbreviation (I_{OUT}) to text (Output Current) ... 8
- Changed title for Figure 4 ... 8
- Changed y-axis and x-axis titles in Figure 5 from abbreviations to text ... 8
- Changed x-axis title in Figure 6 from abbreviation (V_{DC}) to text (Dropout Voltage) ... 8
- Changed x-axis title in Figure 7 from abbreviation (V_{DO}) to text (Dropout Voltage) ... 8
- Changed y-axis and x-axis titles in Figure 8 from abbreviations to text ... 8
- Changed y-axis and x-axis titles in Figure 13 from abbreviations to text ... 9
- Changed title for Figure 13 ... 9
- Changed x-axis title in Figure 14 from abbreviation (I_{BIAS}) to text (Bias Current) ... 9
- Changed Figure 24; added capacitor size indication for C_{SS} ... 16

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Changes from Revision I (November 2010) to Revision J **Page**

- Changed T_J range in *Absolute Maximum Ratings* table 5

Changes from Revision H (October, 2010) to Revision I **Page**

- Corrected equation for Table 2 15

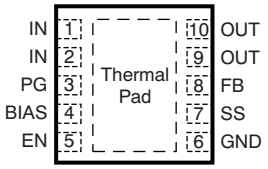
Changes from Revision G (August, 2010) to Revision H **Page**

- Corrected typo in Figure 38 25

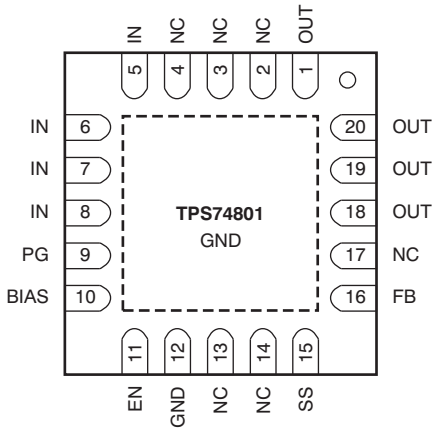
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5 Pin Configuration and Functions

DRC PACKAGE
10 Pin VSON with Thermal Pad
(TOP VIEW)



RGW PACKAGE
20-Pin VQFN
(TOP VIEW)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSON	VQFN		
IN	1, 2	5-8	I	Input to the device. A 1-µF or larger input capacitor is recommended for optimal performance.
EN	5	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
SS	7	15	—	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 µs.
BIAS	4	10	I	Bias input voltage for error amplifier, reference, and internal control circuits. A 1-µF or larger input capacitor is recommended for optimal performance. If IN is connected to BIAS, a 4.7-µF or larger capacitor must be used.
PG	3	9	O	Power Good pin. An open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply of up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
FB	8	16	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	9, 10	1, 18-20	O	Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2 µF, ceramic) is needed from this pin to ground to assure stability.
NC	N/A	2-4, 13, 14, 17	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
GND	6	12	—	Ground
Thermal Pad	PAD	PAD	—	Must be soldered to the ground plane for increased thermal performance. Internally connected to ground.

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6 Specifications

6.1 Absolute Maximum Ratings

At T_J = –40°C to 125°C, unless otherwise noted. All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}, V_{BIAS}	–0.3	6	V
Enable voltage	V_{EN}	–0.3	6	V
Power good voltage	V_{PG}	–0.3	6	V
PG sink current	I_{PG}	0	1.5	mA
Soft-start voltage	V_{SS}	–0.3	6	V
Feedback voltage	V_{FB}	–0.3	6	V
Output voltage	V_{OUT}	–0.3	V_{IN} + 0.3	V
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})	V_{OUT} + 0.3	5.5	V
V_{EN}	Enable supply voltage	0	V_{IN}	5.5	V
V_{BIAS}(1)	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})(2)	V_{OUT} + 1.6(2)	5.5	V
V_{OUT}	Output voltage	0.8		3.3	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor	2.2			µF
C_{IN}	Input capacitor(3)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS748[2]		UNIT
		RGW (VQFN)	DRC (VSON)	
		20 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[3]	35.6	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[4]	33.3	50.3	
$R_{\theta JB}$	Junction-to-board thermal resistance[5]	15	19.6	
ψ_{JT}	Junction-to-top characterization parameter[6]	0.4	0.7	
ψ_{JB}	Junction-to-board characterization parameter[7]	15.2	17.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[8]	3.8	4.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) Thermal data for the RGW and DRC packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. RGW: The exposed pad is connected to the PCB ground layer through a 4x4 thermal via array.
  ii. DRC: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
  (b) i. RGW: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  ii. DRC: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the *Estimating Junction Temperature* section of this data sheet.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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6.5 Electrical Characteristics

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	BIAS pin voltage range		2.7		5.5	V
V_{REF}	Internal reference (Adj.)	T_J = 25°C	0.796	0.8	0.804	V
$V_{OUT(\Delta VIN)}$	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A	V_{REF}		3.6	V
	Accuracy(1)	2.97 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 1.5 A	–2%	±0.5%	2%	
$V_{OUT(\Delta IOUT)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.03		%/V
V_{OUT}	Load regulation	50 mA ≤ I_{OUT} ≤ 1.5 A		0.09		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25 V(3)		60	165	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS}		1.31	1.6	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	2		5.5	A
I_{BIAS}	BIAS pin current			1	2	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V		1	50	µA
I_{FB}	Feedback pin current		–1	0.150	1	µA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		60		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
V_n	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 1 nF		25 × V_{OUT}		μV_{RMS}
t_{STR}	Minimum startup time	R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open		200		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V		440		nA
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			50		mV
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.1	1	µA
T_J	Operating junction temperature		–40		125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 6.

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6.6 Typical Characteristics I_{OUT} = 50 mA

At T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

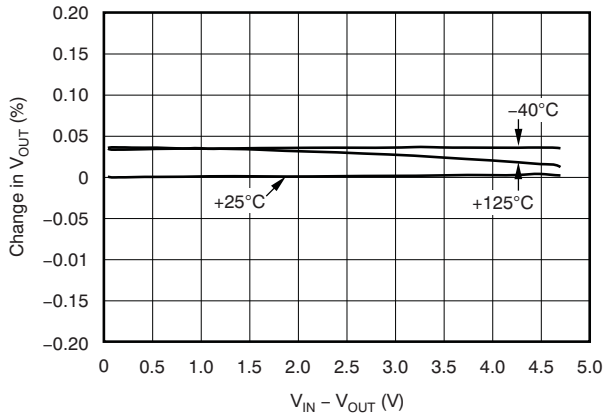


Figure 1. V_{IN} Line Regulation

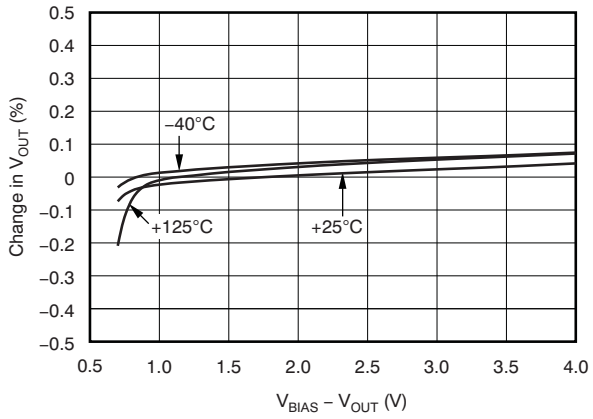


Figure 2. V_{BIAS} Line Regulation

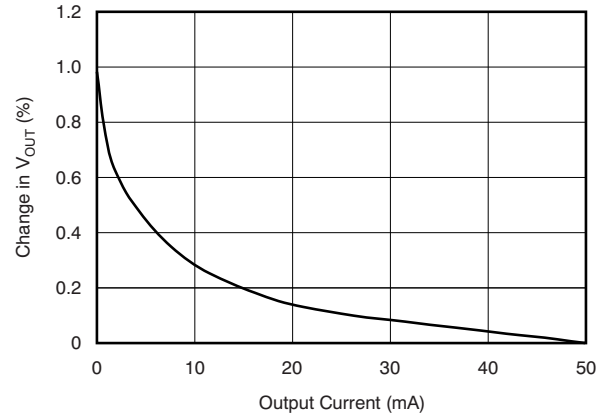


Figure 3. Load Regulation

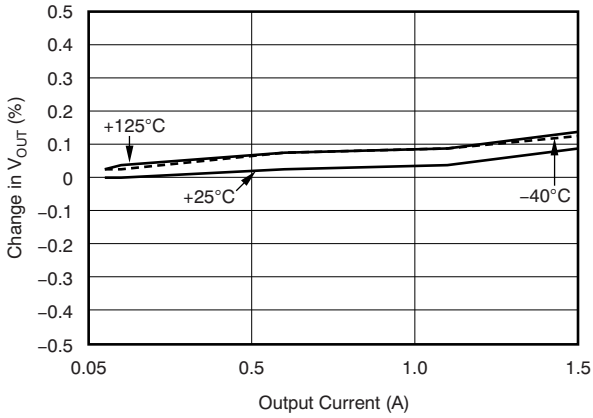


Figure 4. Load Regulation at Light Load

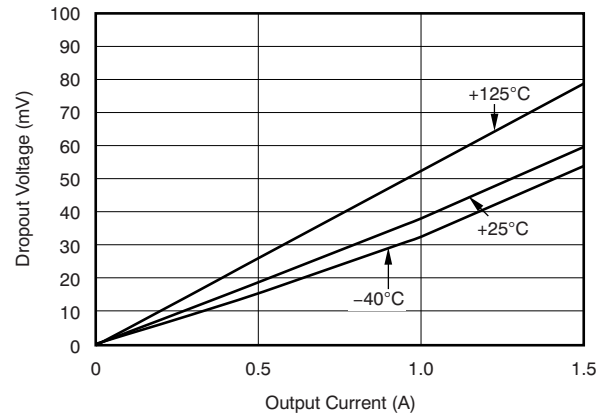


Figure 5. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

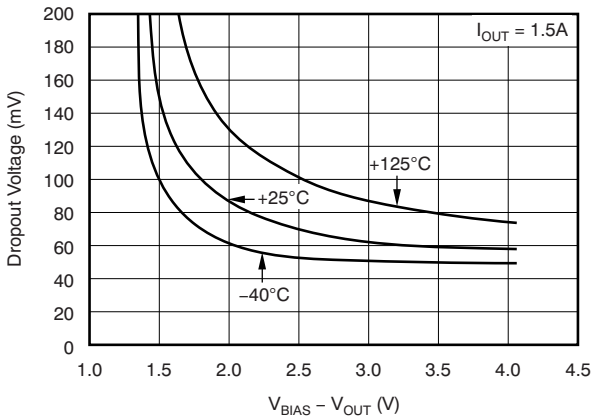


Figure 6. V_{IN} Dropout Voltage vs (V_{BIAS} – V_{OUT}) and Temperature (T_J)

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Typical Characteristics I_{OUT} = 50 mA (continued)

At T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

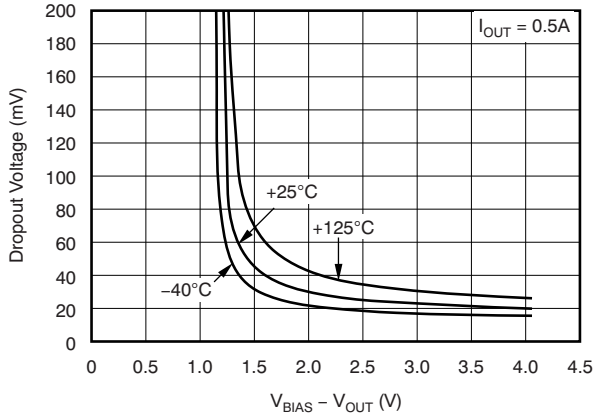


Figure 7. V_{IN} Dropout Voltage vs (V_{BIAS} – V_{OUT}) and Temperature (T_J)

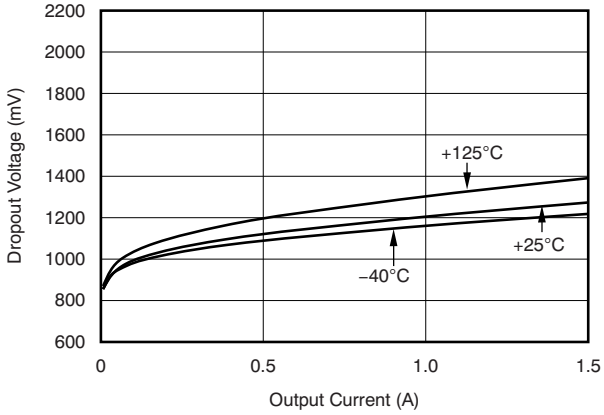


Figure 8. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

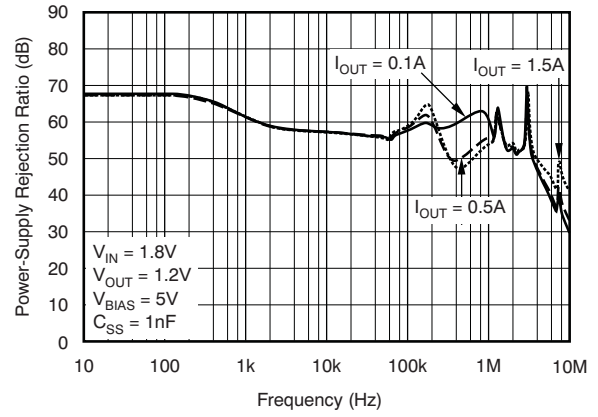


Figure 9. V_{BIAS} PSRR vs Frequency

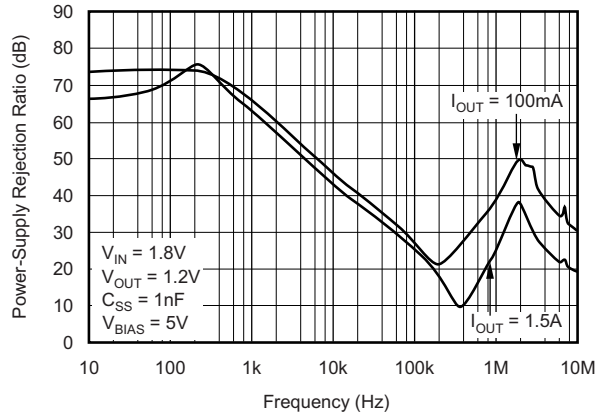


Figure 10. V_{IN} PSRR vs Frequency

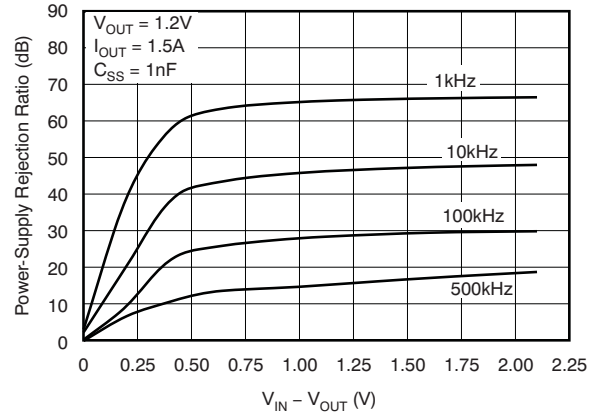


Figure 11. V_{IN} PSRR vs (V_{IN} – V_{OUT})

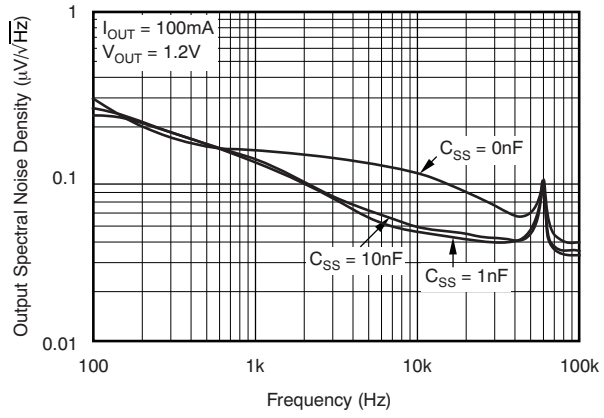


Figure 12. Noise Spectral Density

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Typical Characteristics I_{OUT} = 50 mA (continued)

At T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

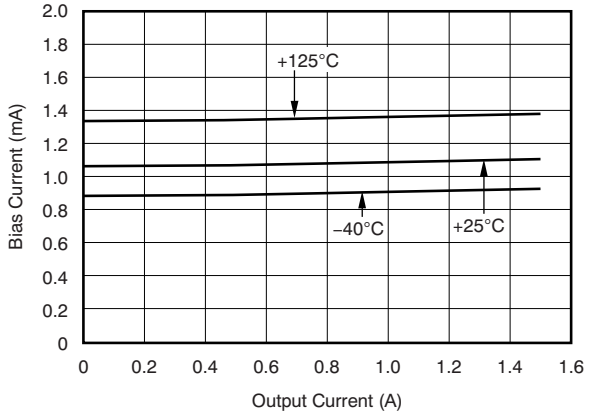


Figure 13. BIAS Pin Current vs Output Current and Temperature (T_J)

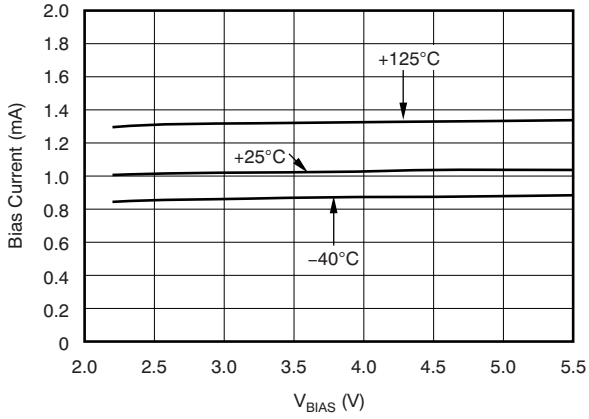


Figure 14. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)

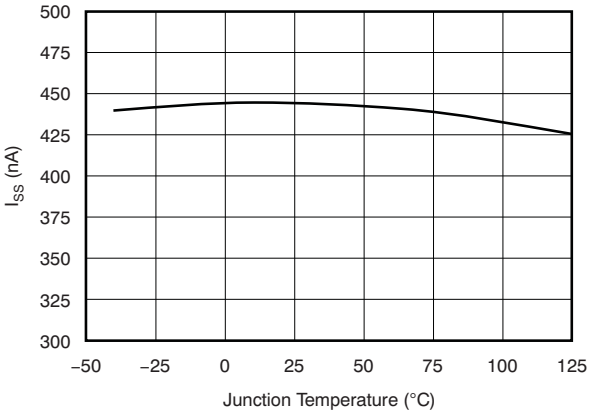


Figure 15. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)

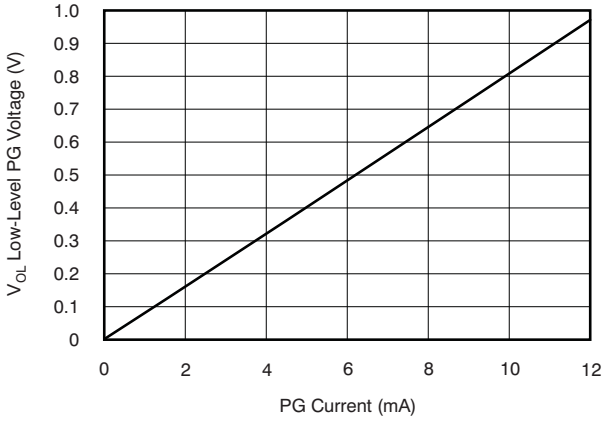


Figure 16. Low-Level PG Voltage vs Current

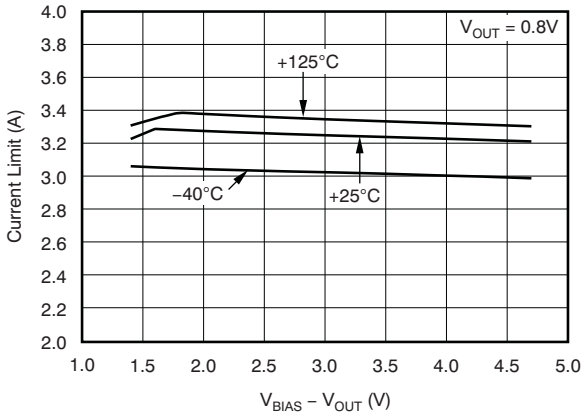


Figure 17. Current Limit vs (V_{BIAS} – V_{OUT})

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6.7 Typical Characteristics I_{OUT} = 1 A

At T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

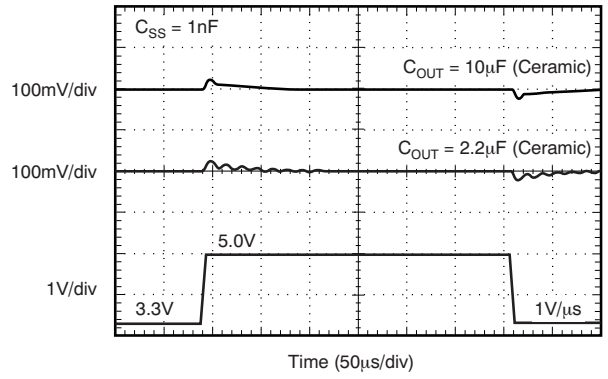


Figure 18. V_{BIAS} Line Transient

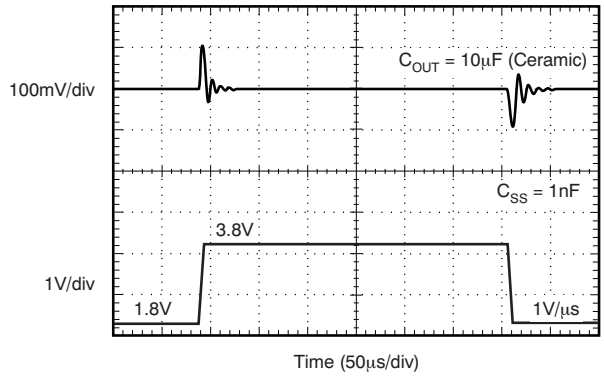


Figure 19. V_{IN} Line Transient

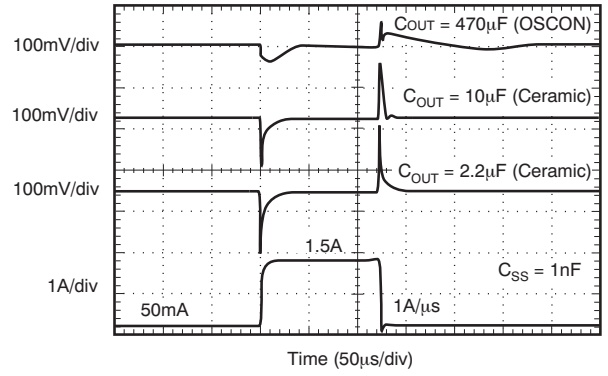


Figure 20. Output Load Transient Response

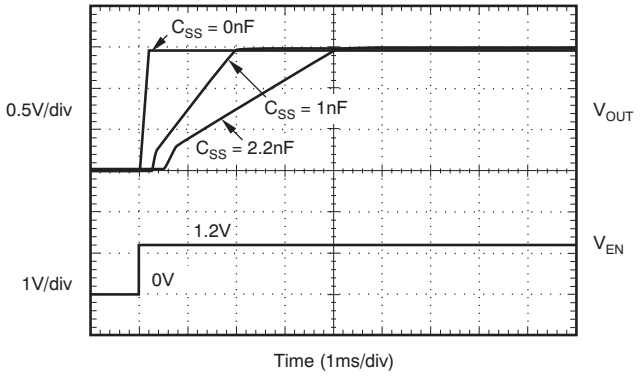


Figure 21. Turnon Response

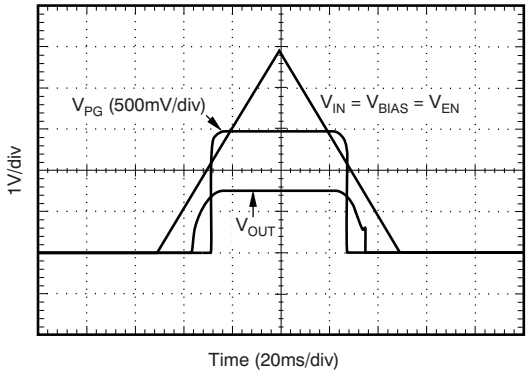


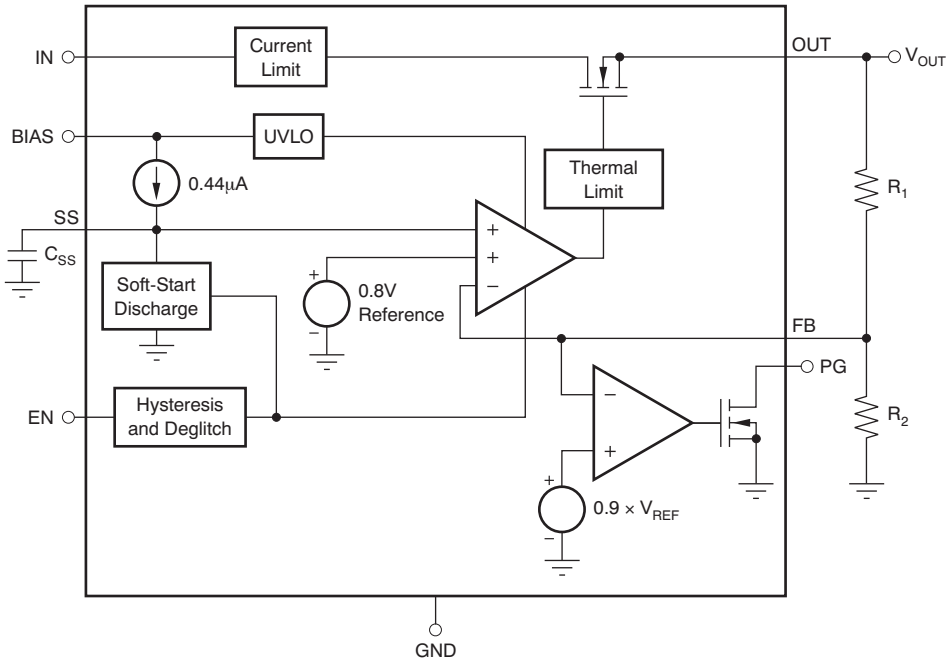
Figure 22. Power-Up/Power-Down

7 Detailed Description

7.1 Overview

The TPS748 family of low-dropout regulators (LDOs) incorporates many features to ensure a wide range of uses. Hysteresis and de-glitch on the EN input improve the ability to sequence multiple devices without worrying about false start-up. The soft-start is fully programmable and allows the user to control the startup time of the LDO output. The TPS748 family of LDOs is ideal for FPGAs, DSPs, and any other device that requires a linear supply and sequencing.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable/Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4 V turns the regulator off, while V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS748 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turnon timing is required, a fast rise-time signal must be used to enable the TPS748.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

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Feature Description (continued)

7.3.2 Power Good

The power good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pull-up resistor. This pin requires at least 1.1 V on V_{BIAS} in order to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pull-up resistor for PG should be in the range of 10 kΩ to 1 MΩ. If output voltage monitoring is not needed, the PG pin can be left floating.

7.3.3 Internal Current Limit

The TPS748 features a factory-trimmed current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 2 A and maintain regulation. The current limit responds in approximately 10 µs to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS748 is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS748 above the rated current degrades device reliability.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS748 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS748 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

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Device Functional Modes (continued)

7.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ (V_{IN})	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geq V_{OUT} + 1.6$ V	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO}$ (V_{IN})	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + 1.6$ V	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 165°C$

7.5 Programming

7.5.1 Programmable Soft-Start

The TPS748 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS748 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 1:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 2:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}}$$

where

- $V_{OUT(nom)}$ is the nominal output voltage,
- C_{OUT} is the output capacitance, and
- $I_{CL(min)}$ is the minimum current limit for the device. (2)

In applications where monotonic startup is required, the soft-start time given by Equation 1 should be set greater than Equation 2.

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Programming (continued)

The maximum recommended soft-start capacitor is 15 nF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 15 nF could be a problem in applications where it is necessary to rapidly pulse the enable pin and still require the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Refer to Table 2 for suggested soft-start capacitor values.

Table 2. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1 ms
270 pF	0.5 ms
560 pF	1 ms
2.7 nF	5 ms
5.6 nF	10 ms
10 nF	18 ms

(1) $$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A}$$ where $t_{SS}(s)$ = soft-start time in seconds.

Another option to set the start-up rate is to use a feedforward capacitor. Refer to application report *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* (SBVA042), for more information.

7.5.2 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate.

There are several different start-up responses that are possible, but not typical:

- If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until it reaches the set output voltage.
- If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}.
- If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}.
- If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor.

Figure 23 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

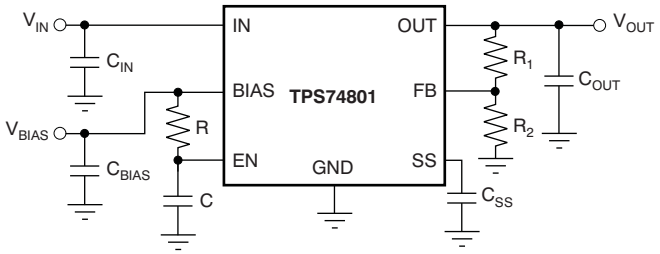


Figure 23. Soft-Start Delay Using an RC Circuit to Enable the Device

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

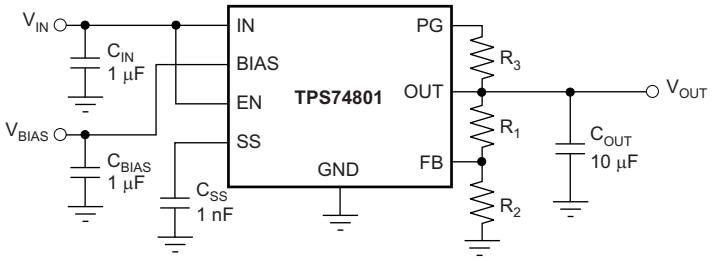
The TPS74801 belongs to a family of low-dropout regulators that feature soft-start capability. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74801 to be stable with any capacitor type of value 2.2 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74801 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits startup inrush currents that may be caused by large capacitive loads. A power good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

8.1.1 Adjusting the Output Voltage

Figure 24 illustrates the typical application circuit for the TPS748 adjustable output device.



$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Figure 24. Typical Application Circuit for the TPS748 (Adjustable)

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 24. Refer to Table 3 for sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 should be ≤ 4.99 kΩ.

Table 3. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2

(1) $V_{OUT} = 0.8 \times (1 + R_1/R_2)$.

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Table 3. Standard 1% Resistor Values for Programming the Output Voltage(1) (continued)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

NOTE

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

8.1.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1 µF and minimum recommended capacitor for V_{BIAS} is 0.1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.

8.1.3 Transient Response

The TPS748 was designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; refer to Figure 20 in the *Typical Characteristics I_{OUT} = 50 mA* section. Because the TPS748 is stable with output capacitors as low as 2.2 µF, many applications may then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

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8.1.4 Dropout Voltage

The TPS748 offers very low dropout performance, making it well-suited for high-current, low V_{IN}/low V_{OUT} applications. The low dropout of the TPS748 allows the device to be used in place of a dc/dc converter and still achieve good efficiency. Equation 3 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \quad (3)$$

This efficiency provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solutions.

There are two different specifications for dropout voltage with the TPS748. The first specification (shown in Figure 25) is referred to as *V_{IN} Dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 3.25 V(2) above V_{OUT}, which is the case for V_{BIAS} when powered by a 5.0-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} +3.25 V(2), V_{IN} dropout is less than specified.

The second specification (shown in Figure 31) is referred to as *V_{BIAS} Dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET; therefore, V_{BIAS} must be 1.6 V above V_{OUT}. Because of this usage, IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the IC package.

8.1.5 Output Noise

The TPS748 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 1-nF soft-start capacitor, the output noise is reduced by half and is typically 30 μV_{RMS} for a 1.2-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 1-nF soft-start capacitor is given in Equation 4:

$$V_N(\mu V_{RMS}) = 25\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (4)$$

The low output noise of the TPS748 makes it a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

(2) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 6.

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8.2 Typical Applications

8.2.1 FPGA I/O Supply at 1.5 V With a Bias Rail

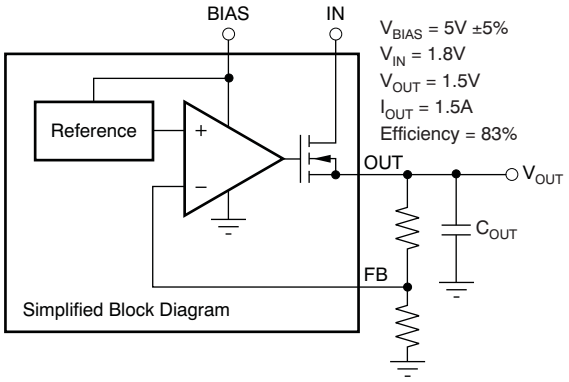


Figure 25. Typical Application of the TPS748 Using an Auxiliary Bias Rail

8.2.1.1 Design Requirements

This application powers the I/O rails of an FPGA , at $V_{OUT(nom)}$ = 1.5 V and $I_{OUT(dc)}$ = 1.5 A. The available external supply voltages are 1.8 V, 3.3 V and 5 V.

8.2.1.2 Detailed Design Procedure

First, determine what supplies to use for the input and bias rails. A 1.8-V input can be stepped down to 1.5 V at 1.5 A if an external bias is provided, because the maximum dropout voltage is 165 mV if V_{BIAS} is at least 3.25 V higher than V_{OUT}. To achieve this voltage step, the bias rail is supplied by the 5-V supply. The approximation in Equation 3 estimates the efficiency at 83.3%.

The output voltage then must be set to 1.5 V. As Table 3 shows, set R_1 = 4.12 kΩ and R_2= 4.75 kΩ to obtain the required output voltage. The minimum capacitor sizing is desired to reduce the total solution size footprint; refer to *Input, Output, and Bias Capacitor Requirements* for C_{IN} = 1 µF, C_{BIAS} = 1 µF, and C_{OUT} = 2.2 µF. Use C_{SS} = 1 nF for a typical 1.8-ms start-up time.

See Figure 25 for a simplified version of the final circuit.

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Typical Applications (continued)

8.2.1.3 Application Curves

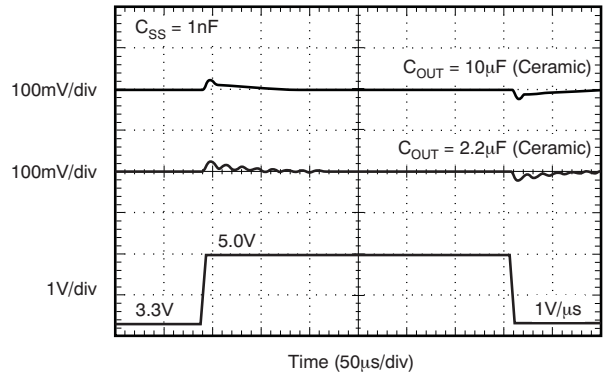


Figure 26. V_{BIAS} Line Transient

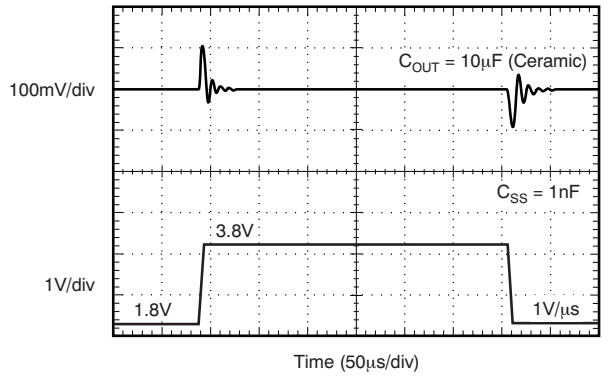


Figure 27. V_{IN} Line Transient

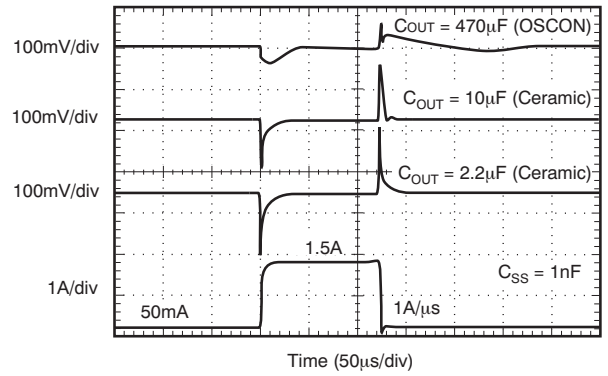


Figure 28. Output Load Transient Response

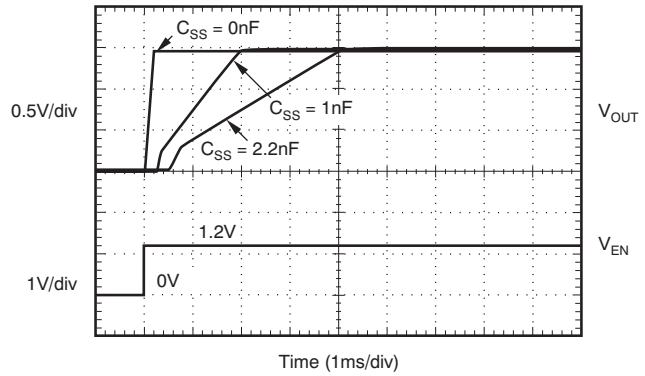


Figure 29. Turnon Response

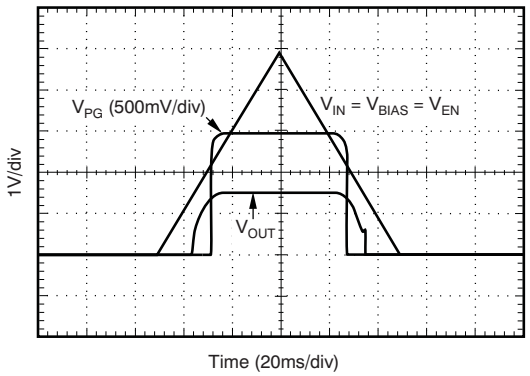


Figure 30. Power-Up/Power-Down

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Typical Applications (continued)

8.2.2 FPGA I/O Supply at 1.5 V Without a Bias Rail

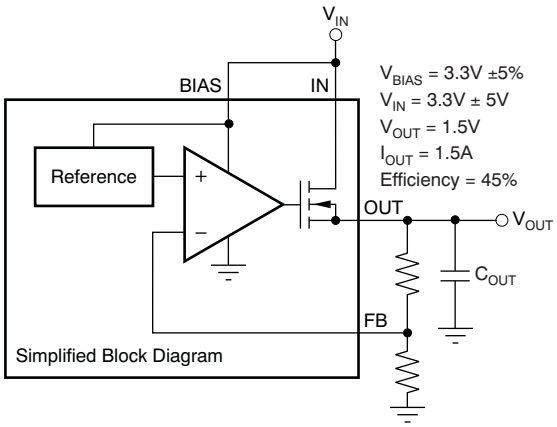


Figure 31. Typical Application of the TPS748 Without an Auxiliary Bias Rail

8.2.2.1 Design Requirements

The application powers the I/O rails of an FPGA, at $V_{OUT(nom)}$ = 1.5 V and $I_{OUT(max)}$ = 1.5 A. The only available rail is 3.3 V. The I/O pins are driven for only short durations with a 5% duty cycle, so thermal issues are not a concern.

8.2.2.2 Detailed Design Procedure

There is only one available rail; therefore, the input supply and the bias supply are connected together on the 3.3-V input supply.

The output voltage must be set to 1.5 V. As Table 3 shows, set R_1 = 4.12 kΩ and R_2= 4.75 kΩ to obtain the required output voltage. The minimum capacitor sizing is desired to reduce the total solution size footprint; refer to *Input, Output, and Bias Capacitor Requirements* for C_{IN} = C_{BIAS} = 4.7 µF, and C_{OUT} = 2.2 µF. Use C_{SS} = 1 nF for a typical 1.8-ms start-up time.

Figure 31 shows the TPS748 configured without a bias rail.

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Typical Applications (continued)

8.2.2.3 Application Curves

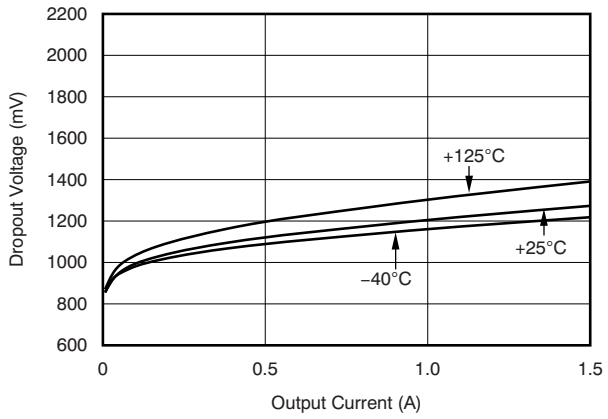


Figure 32. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

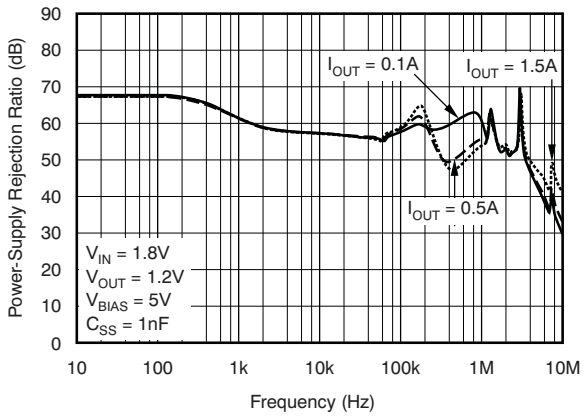


Figure 33. V_{BIAS} PSRR vs Frequency

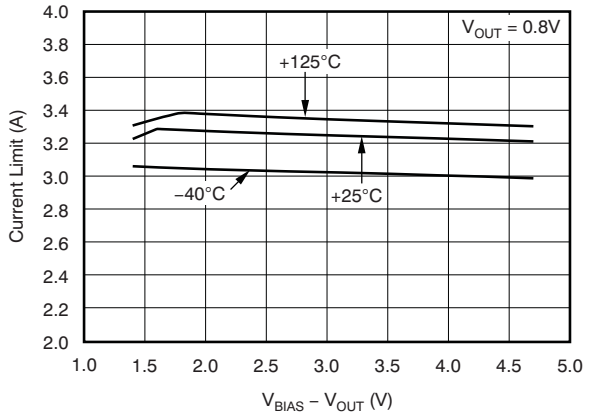


Figure 34. Current Limit vs (V_{BIAS} – V_{OUT})

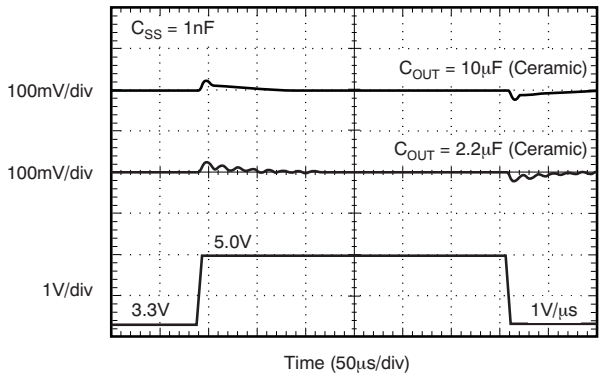


Figure 35. V_{BIAS} Line Transient

9 Power Supply Recommendations

The TPS748 is designed to operate from an input voltage up to 5.5 V, provided the bias rail is at least 1.62 V higher than the input supply and dropout requirements are met. The bias rail and the input supply should both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin of the TPS748. This supply must have at least 1 µF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1-µF or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

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10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 24 should be connected as close as possible to the load. If BIAS is connected to IN, it is recommended to connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turnon response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 5:

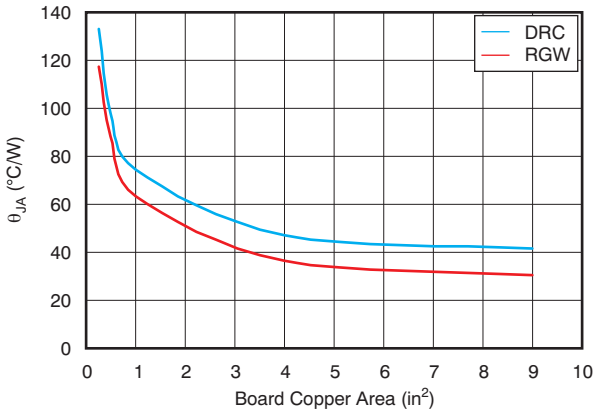
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both the VSON (DRC) and QFN (RGW) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 6:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \quad (6)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 36.



Note: θ_{JA} value at board size of 9 in^2 (that is, 3 in × 3i n) is a JEDEC standard.

Figure 36. Θ_{JA} vs Board Size

Figure 36 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in *Estimating Junction Temperature*.

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10.2 Layout Example

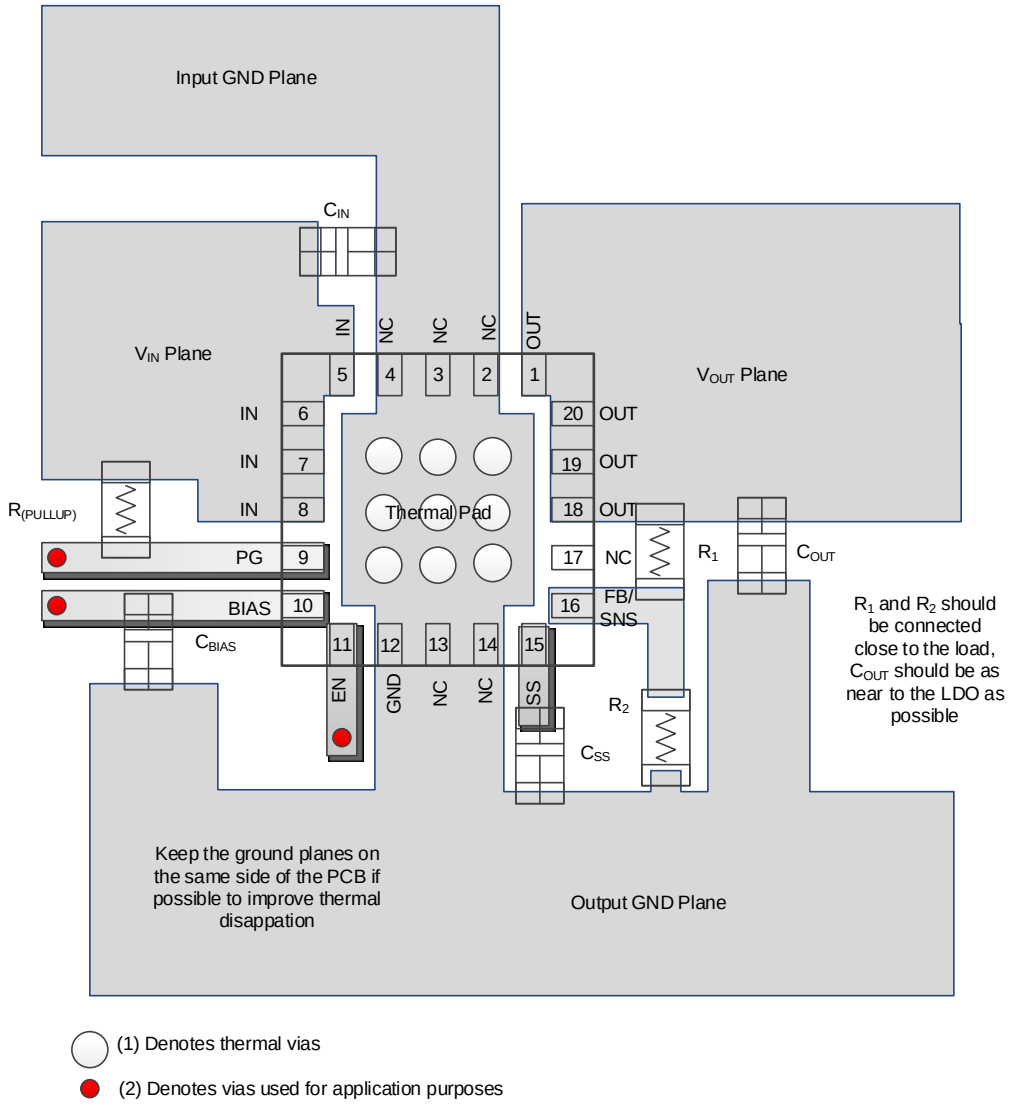


Figure 37. Layout Example (RGW Package)

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10.3 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 7). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

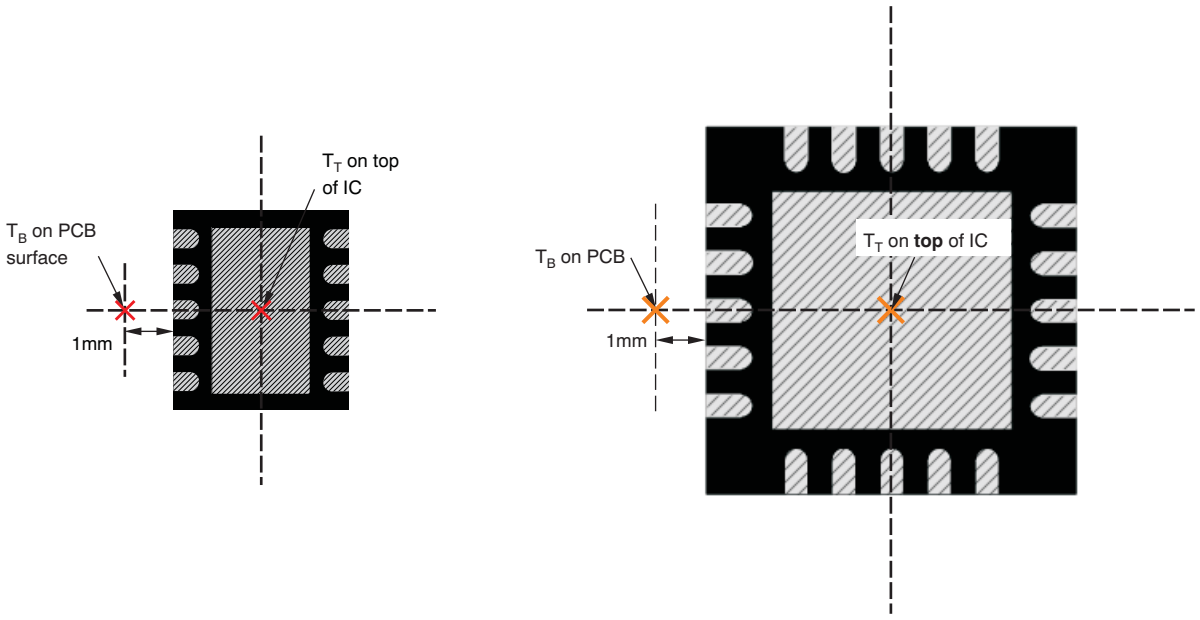
$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{7}$$

Where P_D is the power dissipation shown by Equation 5, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (see Figure 38).

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.



(a) Example DRC (SON) Package Measurement **(b) Example RGW (QFN) Package Measurement**

Figure 38. Measuring Points for T_T and T_B

By looking at Figure 39, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 7 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

Estimating Junction Temperature (continued)

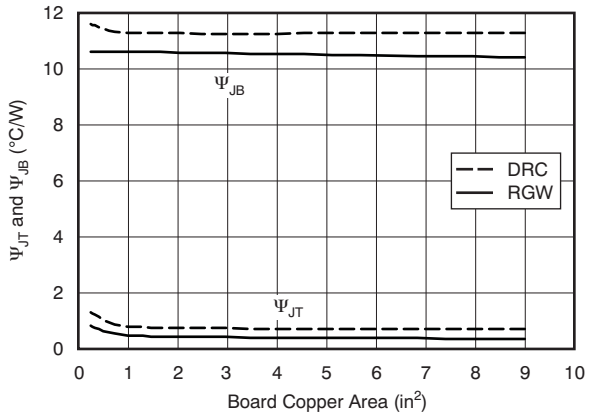


Figure 39. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS48. The TPS74801EVM-177 evaluation module (and related user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS748 is available through the product folders under *Tools & Software*.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Using New Thermal Metrics*, SBVA025.
- *IC Package Thermal Metrics*, SPRA953.
- *Ultimate Regulation of with Fixed Output Versions of the TPS742xx, TPS743xx, and TPS744xx*, SBVA024.
- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042.
- *TPS74801EVM-177 Evaluation Module User Guide*, SLVU189.

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74801DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO	Samples
TPS74801DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO	Samples
TPS74801DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO	Samples
TPS74801DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTO	Samples
TPS74801QRGWRQ1	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 74801Q	Samples
TPS74801RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801	Samples
TPS74801RGWRG4	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801	Samples
TPS74801RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801	Samples
TPS74801RGWTG4	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74801	Samples
TPS74801TDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	QVK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS74801, TPS74801-Q1 :

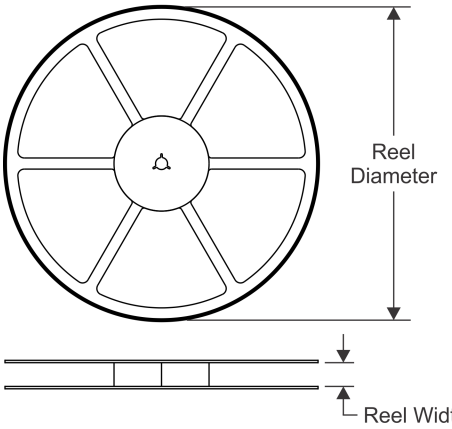
- Catalog: TPS74801
- Automotive: TPS74801-Q1

NOTE: Qualified Version Definitions:

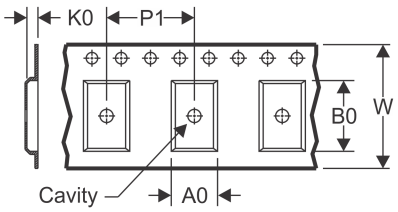
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

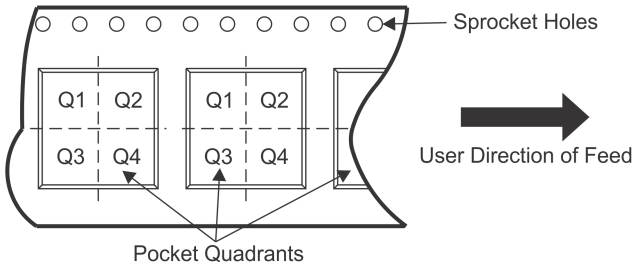


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

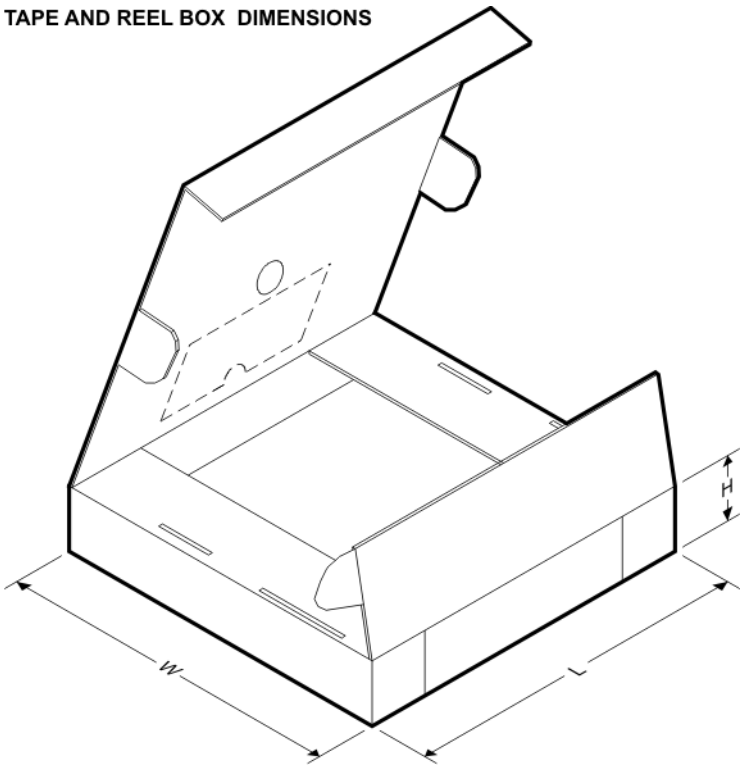
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74801DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74801QRGWRQ1	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74801RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74801RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74801TDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

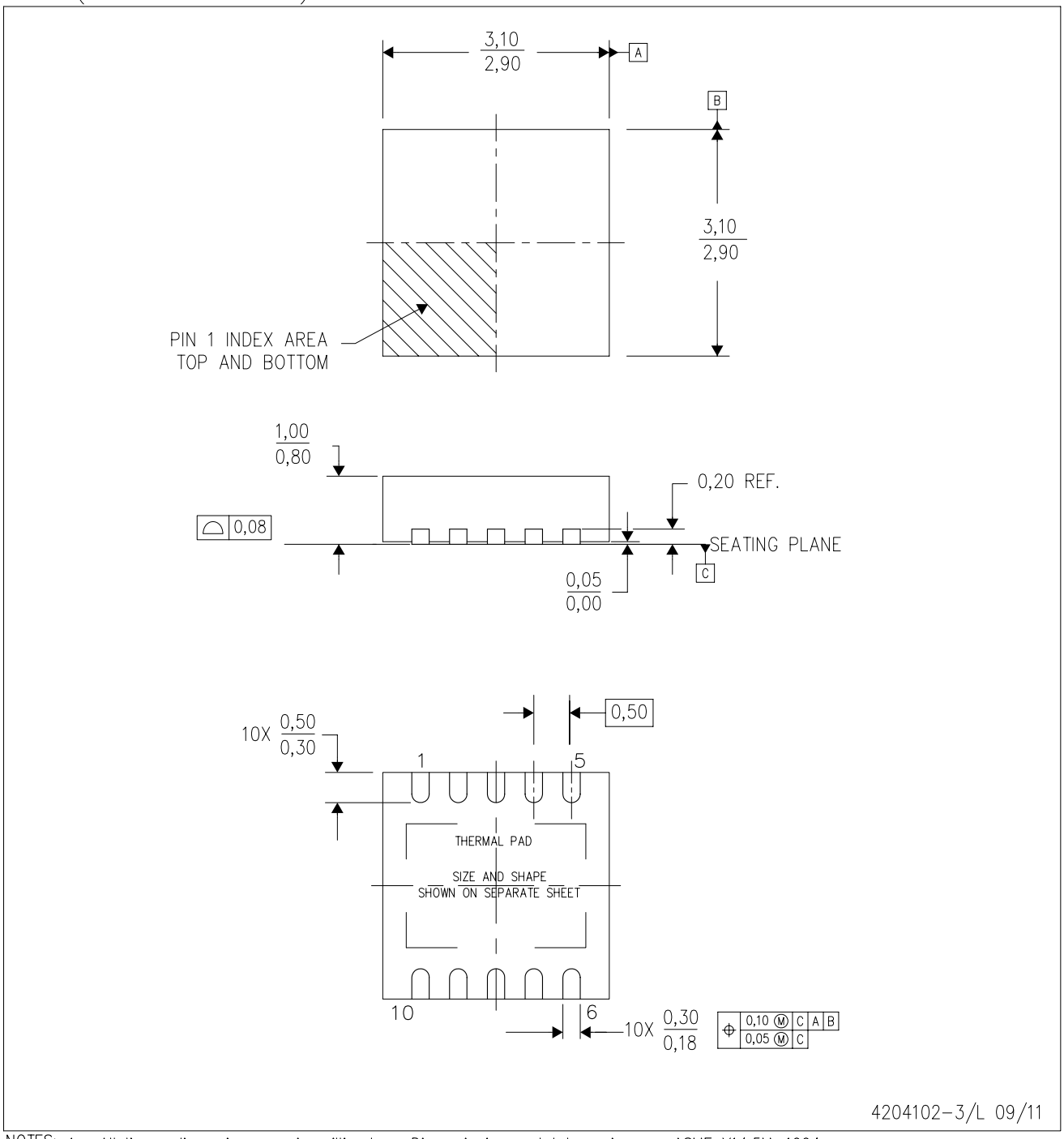
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74801DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74801DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS74801DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS74801QRGWRQ1	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801RGWT	VQFN	RGW	20	250	210.0	185.0	35.0
TPS74801TDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

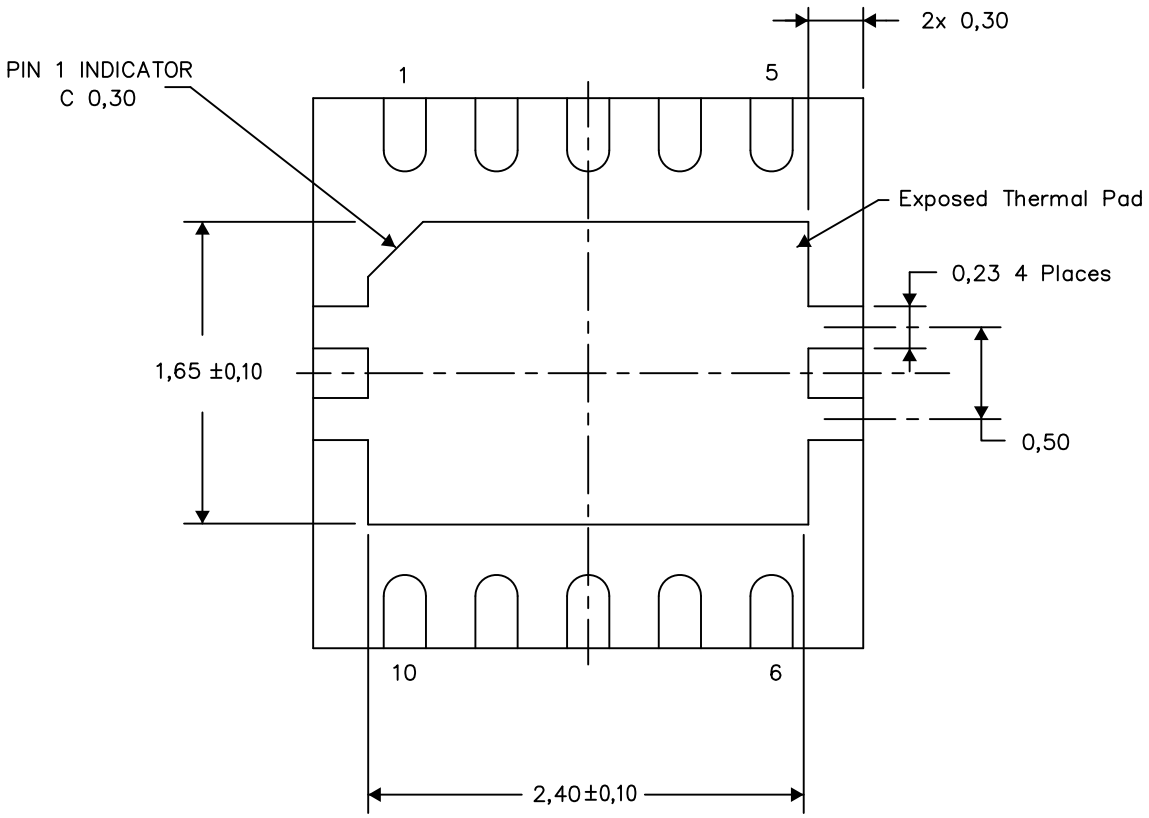
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



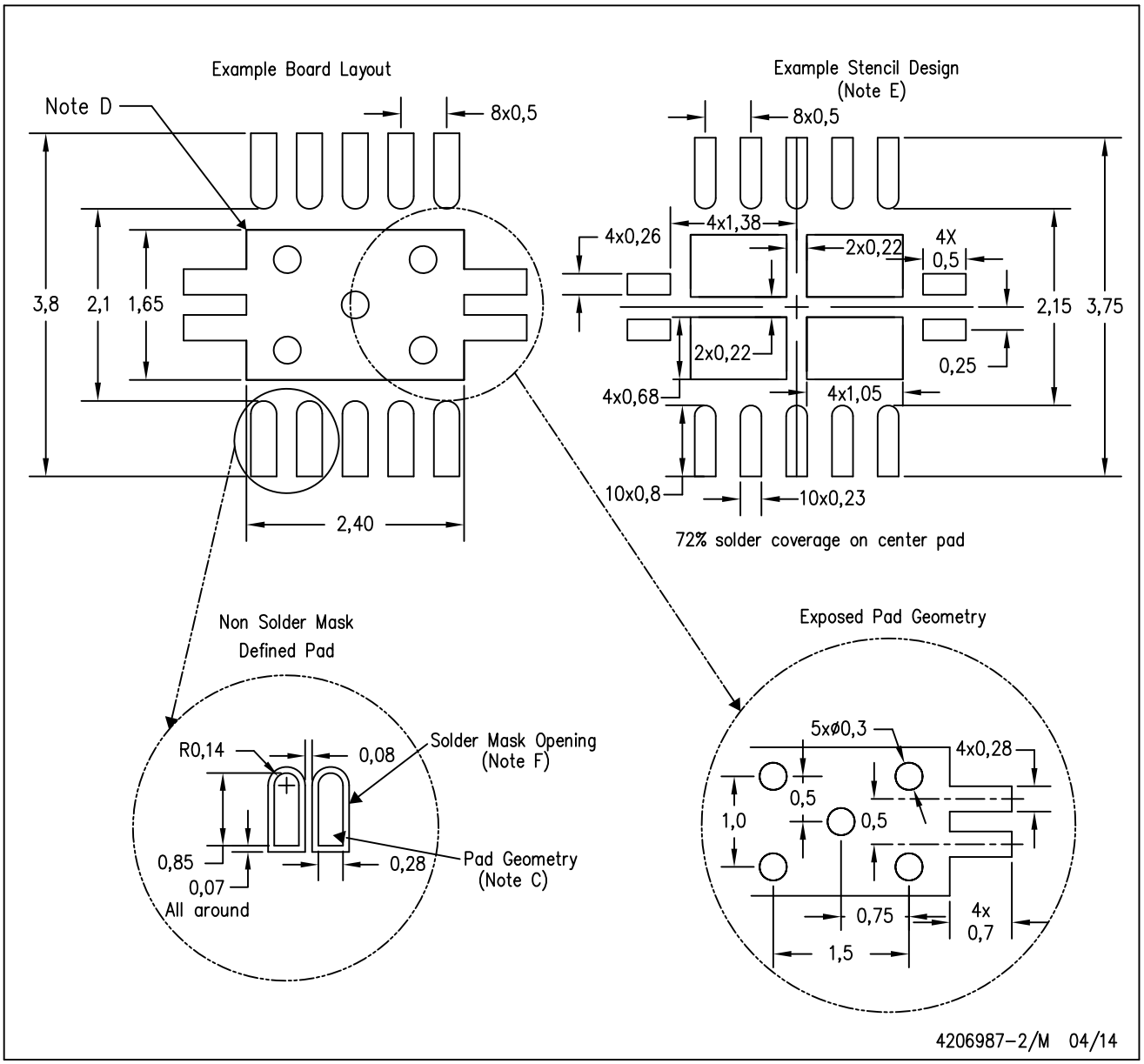
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/W 04/15

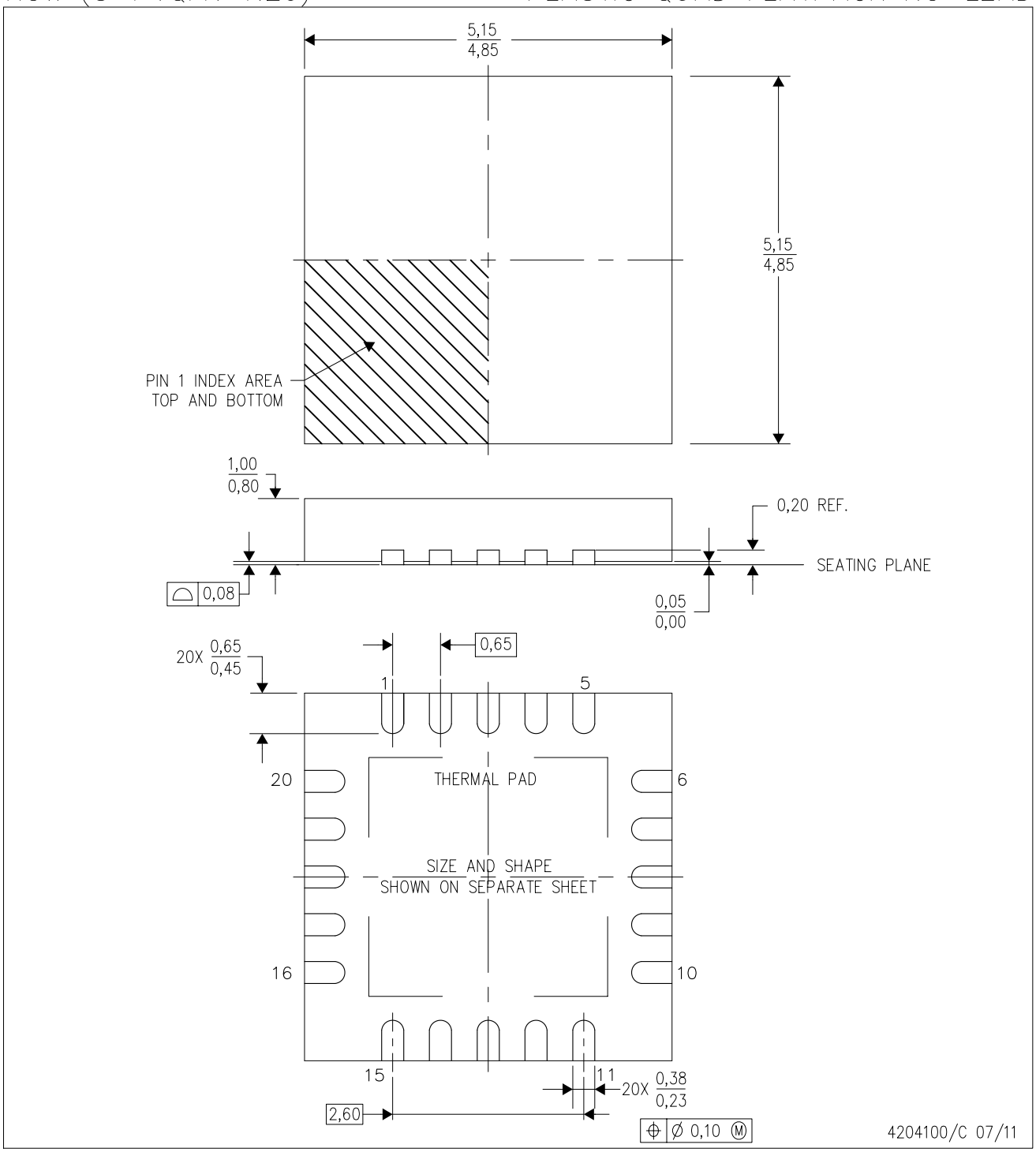
NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

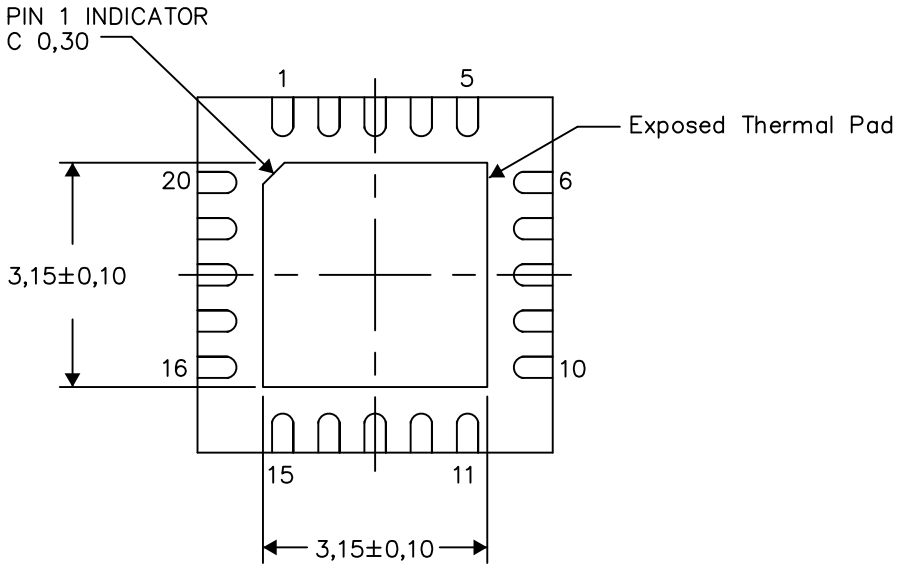
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



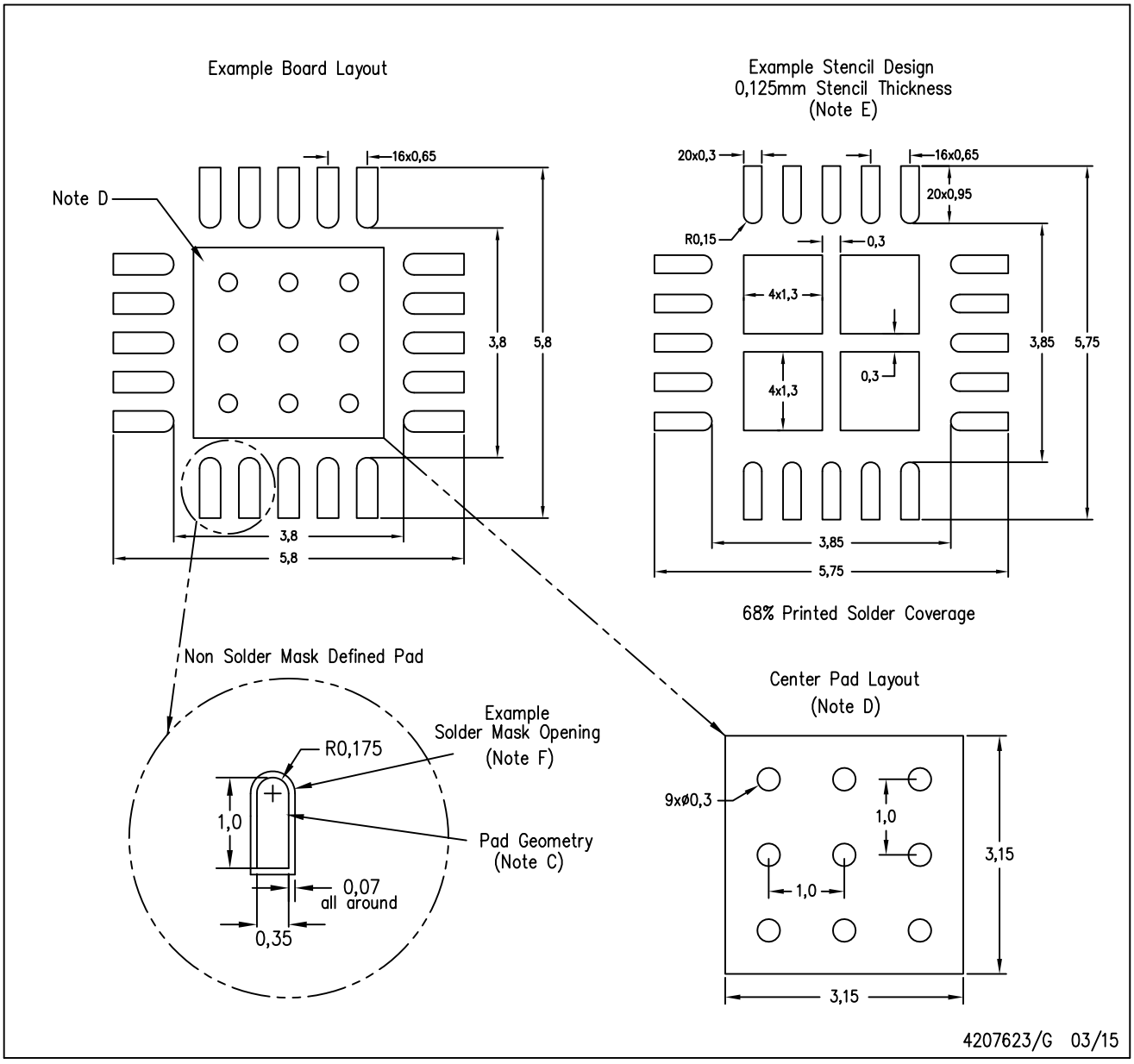
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/L 03/15

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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