19-1134; Rev 0; 10/96

EVALUATION KIT AVAILABLE

12-Bit, 30Msps, TTL-Output ADC

General Description

The MAX1172 analog-to-digital converter (ADC) is a 12-bit monolithic ADC capable of sample rates greater than 30Msps. An on-board input buffer and track/hold function ensure excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes development problems.

Logic inputs and outputs are TTL compatible. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is a very low 1.1W with power-supply voltages of +5.0V and -5.2V. The MAX1172 also provides a wide input voltage range of ±2.0V.

The MAX1172 is available in a 32-lead ceramic side-brazed package and a 44-lead surface-mount CERQUAD package.

Applications

Radar Receivers

Professional Video

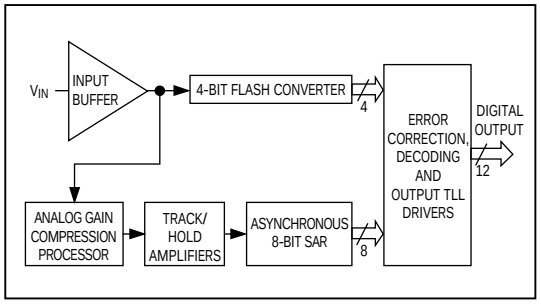
Instrumentation

Imaging

Digital Communications

Digital Spectrum Analyzers

Functional Diagram



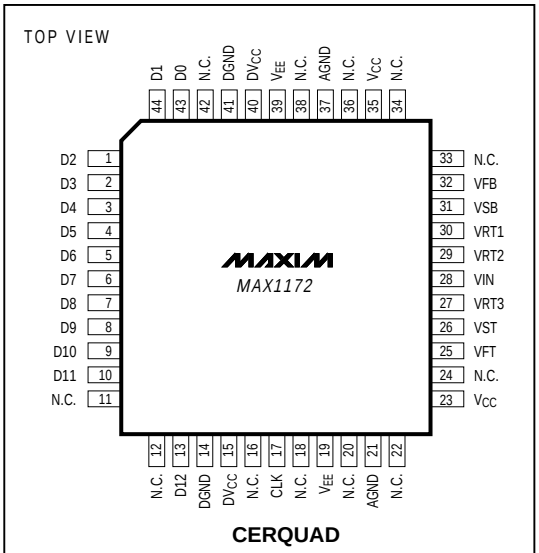
Features

- **Monolithic, 12-Bit, 30Msps Converter**
- **On-Chip Track/Hold**
- **±2.0V Analog Input Range**
- **High Input Impedance**
- **66dB SNR at 1MHz Input**
- **Low Power: 1.1W**
- **5pF Input Capacitance**
- **TTL-Compatible Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1172CDJ	0°C to +70°C	32 Ceramic SB
MAX1172CBH	0°C to +70°C	44 CERQUAD

Pin Configurations



CERQUAD

Pin Configurations continued at end of data sheet.

For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

12-Bit, 30Msps, TTL-Output ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....+6V
V_{EE} .....-6V
Analog Input .....$V_{FB} \le V_{IN} \le V_{FT}$
VFB, VFT ..... -3.0V, +3.0V
Reference Ladder Current 12mA
CLK IN .....V_{CC}
Digital Outputs.....0mA to -30mA
Operating Temperature Range.....0°C to +70°C
Junction Temperature (T_j).....+175°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 30MHz, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			12			Bits
DC ACCURACY (T_A = +25°C)						
Integral Nonlinearity	± full scale	IV		±2.0		LSB
Differential Nonlinearity	250kHz sample rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
ANALOG INPUT						
Input Voltage Range		VI		±2.0		V
Input Bias Current	T_A = +25°C	I		30	60	µA
Input Resistance	V_{IN} = 0V, T_A = +25°C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3dB small signal	V		120		MHz
Positive Full-Scale Error		V		±5.0		LSB
Negative Full-Scale Error		V		±5.0		LSB
REFERENCE INPUT						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
TIMING CHARACTERISTICS						
Maximum Conversion Rate		VI	30	40		MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A = +25°C	V		14	18	ns
Aperture Delay Time	T_A = +25°C	V		1		ns
Aperture Jitter Time	T_A = +25°C	V		5		ps-RMS

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 30MHz, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Effective Number of Bits	f_{IN} = 500kHz				10.0		Bits
	f_{IN} = 1MHz				9.8		
	f_{IN} = 3.58MHz				9.5		
Signal-to-Noise Ratio (without Harmonics)	f_{IN} = 500kHz	T_A = +25°C	I	63	66		dB
		$T_A = T_{MIN}$ to T_{MAX}	IV	58	61		
	f_{IN} = 1MHz	T_A = +25°C	I	63	65		
		$T_A = T_{MIN}$ to T_{MAX}	IV	58	60		
	f_{IN} = 3.58MHz	T_A = +25°C	I	62	64		
		$T_A = T_{MIN}$ to T_{MAX}	IV	58	60		
Harmonic Distortion	f_{IN} = 500kHz	T_A = +25°C	I	63	65		dB
		$T_A = T_{MIN}$ to T_{MAX}	IV	59	61		
	f_{IN} = 1MHz	T_A = +25°C	I	62	64		
		$T_A = T_{MIN}$ to T_{MAX}	IV	58	60		
	f_{IN} = 3.58MHz	T_A = +25°C	I	59	61		
		$T_A = T_{MIN}$ to T_{MAX}	IV	57	59		
Signal-to-Noise and Distortion	f_{IN} = 500kHz	T_A = +25°C	I	60	62		dB
		$T_A = T_{MIN}$ to T_{MAX}	IV	55	57		
	f_{IN} = 1MHz	T_A = +25°C	I	59	61		
		$T_A = T_{MIN}$ to T_{MAX}	IV	55	57		
	f_{IN} = 3.58MHz	T_A = +25°C	I	57	59		
		$T_A = T_{MIN}$ to T_{MAX}	IV	54	56		
Spurious-Free Dynamic Range	f_{IN} = 1MHz, T_A = +25°C		V		74		dBc
Differential Phase	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.2		Degrees
Differential Gain	f_{IN} = 3.58MHz and 4.35MHz, T_A = +25°C		V		0.7		%
DIGITAL INPUTS							
Logic "1" Voltage			V	2.4		4.0	V
Logic "0" Voltage			V			0.8	V
Maximum Input Current Low	T_A = +25°C		I	0	5	20	µA
Maximum Input Current High	T_A = +25°C		I	0	5	20	µA
Pulse Width Low (CLK)			IV	15			ns
Pulse Width High (CLK)			IV	15		300	ns
DIGITAL OUTPUTS							
Logic "1" Voltage	T_A = +25°C		I	2.4			V
Logic "0" Voltage	T_A = +25°C		I			0.6	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 30MHz, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
Voltages	V_{CC}	IV	4.75	5.0	5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	
Currents	I_{CC}, T_A = +25°C	I		135	150	mA
	DI_{CC}, $T_A = T_{MIN}$ to T_{MAX}	IV		40	55	
	$-I_{EE}$, T_A = +25°C	I		45	70	
Power Dissipation		VI		1.1	1.3	W
Power-Supply Rejection	5V ±0.25V, -5.2V ±0.25V	V		1.0		LSB

Note 1: Typical thermal impedances (unsoldered, in free air):
32 Ceramic SB: θ_{jA} = 50°C/W
44 CERQUAD: θ_{jA} = 78°C/W, θ_{jA} at 1m/s airflow = 58°C/W, θ_{jC} = 3.3°C/W
Use forced-air cooling or heatsinking to maintain $T_j \leq 150°C$.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

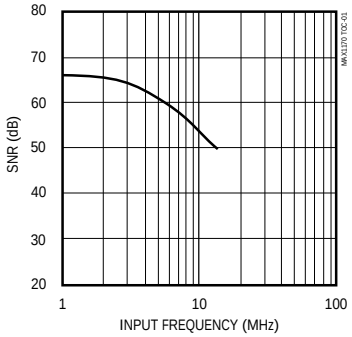
Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

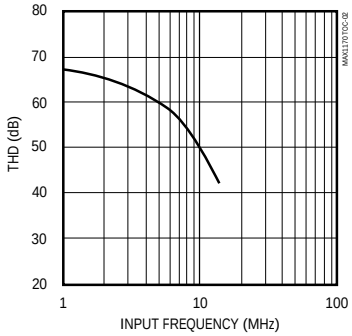
Typical Operating Characteristics

(f_S = 30Msps, f_{IN} = 1MHz, T_A = +25°C, unless otherwise noted.)

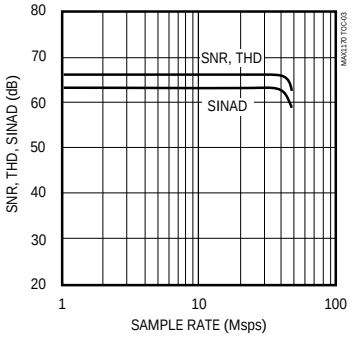
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



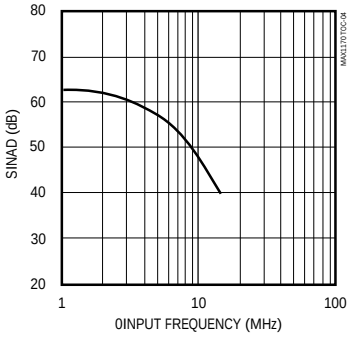
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



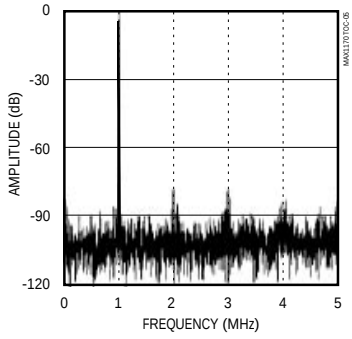
SNR, THD, SINAD vs. SAMPLE RATE



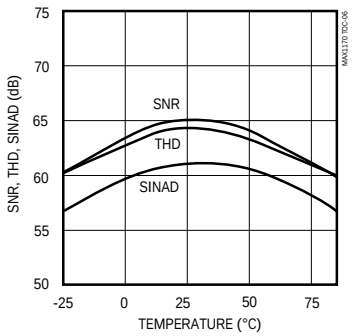
SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



SPECTRAL RESPONSE



SNR, THD, SINAD vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 15	14, 41	DGND	Digital Ground
2–13	43, 44, 1–10	D0–D11	TTL Outputs (D0 = LSB)
14	13	D12	TTL Output Overrange Bit
16, 32	15, 40	DV_{CC}	Digital +5.0V Supply (TTL Outputs)
17	17	CLK	TLL Clock Input
18, 31	19, 39	V_{EE}	-5.2V Supply
19, 30	21, 37	AGND	Analog Ground
20, 29	23, 35	V_{CC}	+5.0V Supply
21	25	VFT	Force for Top of Reference Ladder
22	26	VST	Sense for Top of Reference Ladder
23	27	VRT3	Voltage Reference Tap 3
24	28	VIN	Analog Input, ±2.0V typical
25	29	VRT2	Voltage Reference Tap 2
26	30	VRT1	Voltage Reference Tap 1
27	31	VSB	Sense for Bottom of Reference Ladder
28	32	VFB	Force for Bottom of Reference Ladder
—	11, 12, 16, 18, 20, 22, 24, 33, 34, 36, 38, 42	N.C.	No Connection

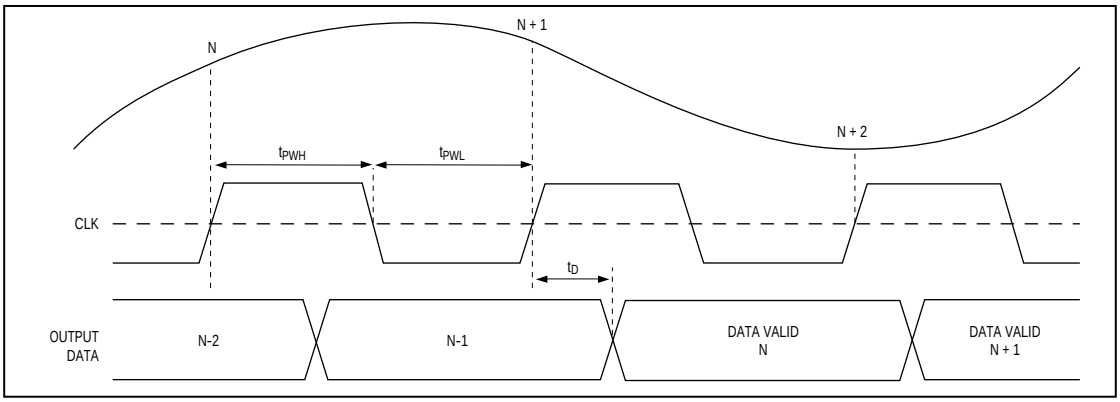


Figure 1a. Timing Diagram

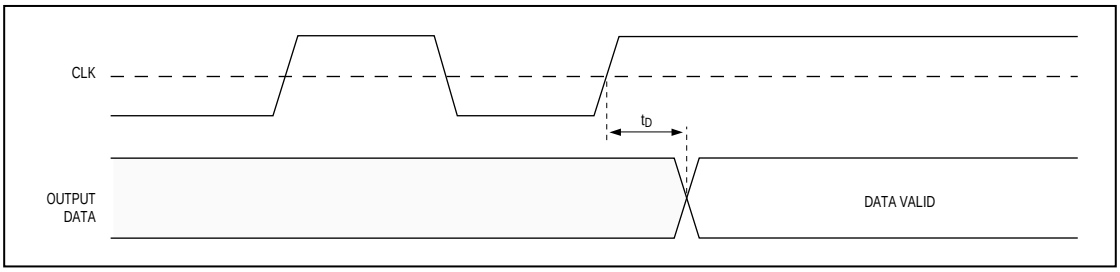


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_D	CLK to Data Valid Prop Delay		14	18	ns
t_{PWH}	CLK High Pulse Width	15		300	ns
t_{PWL}	CLK Low Pulse Width	15			ns

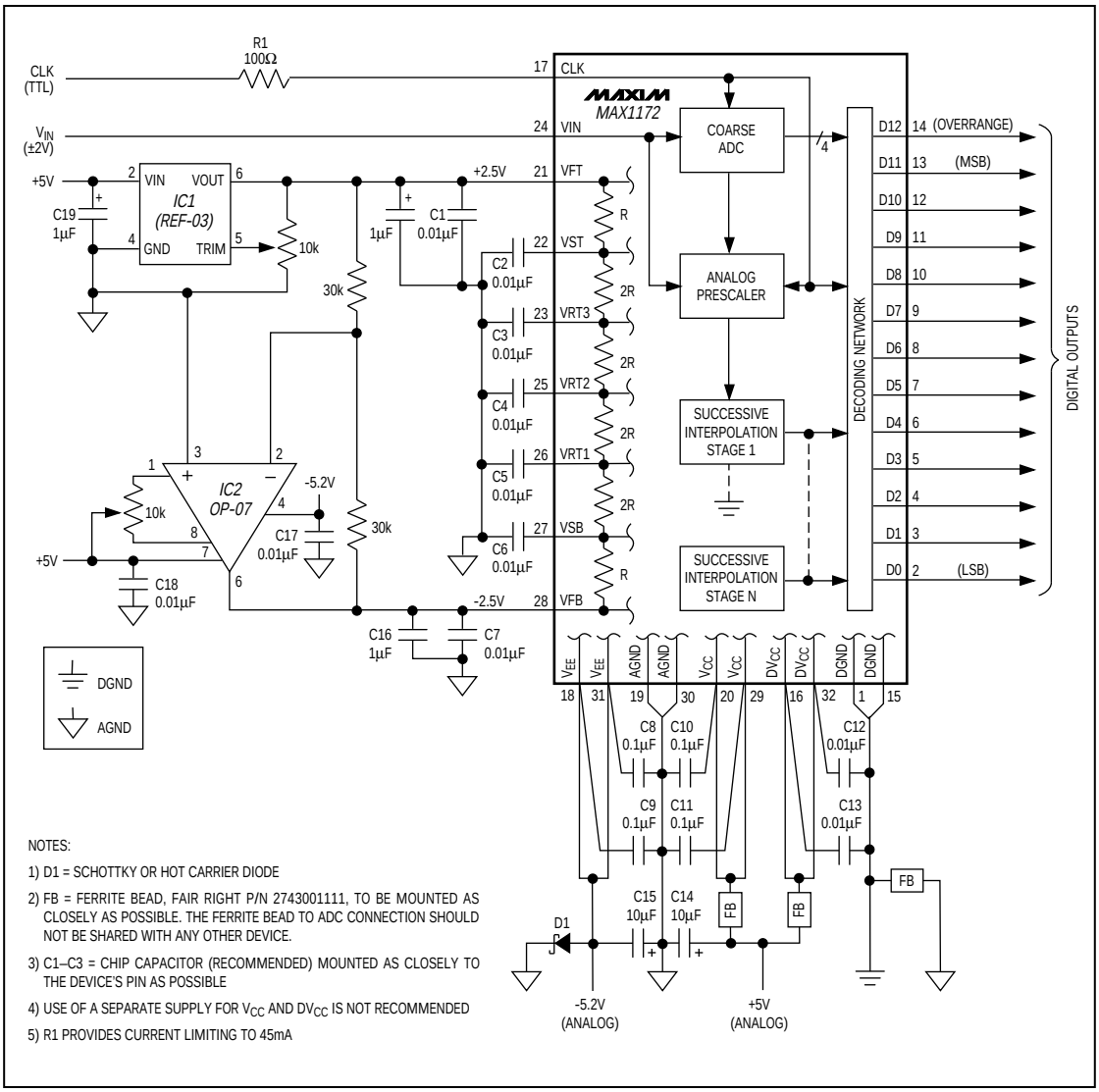
Detailed Description

The MAX1172 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1172 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria for achieving the optimal device performance.

Power Supplies and Grounding

The MAX1172 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line reduces the transient noise injected into the analog V_{CC}. These beads should be connected as close to the device as possible. The connection between the beads and the MAX1172 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1µF for V_{EE} and V_{CC}, and 0.01µF for DV_{CC} (chip capacitors are preferred).

12-Bit, 30Msps, TTL-Output ADC



NOTES:

1) D1 = SCHOTTKY OR HOT CARRIER DIODE

2) FB = FERRITE BEAD, FAIR RIGHT P/N 2743001111, TO BE MOUNTED AS CLOSELY AS POSSIBLE. THE FERRITE BEAD TO ADC CONNECTION SHOULD NOT BE SHARED WITH ANY OTHER DEVICE.

3) C1–C3 = CHIP CAPACITOR (RECOMMENDED) MOUNTED AS CLOSELY TO THE DEVICE'S PIN AS POSSIBLE

4) USE OF A SEPARATE SUPPLY FOR V_{CC} AND DV_{CC} IS NOT RECOMMENDED

5) R1 PROVIDES CURRENT LIMITING TO 45mA

Figure 2. Typical Interface Circuit

AGND and DGND are the two grounds available on the MAX1172. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power-supply sequencing latchup conditions. Use of the recommended interface circuit shown in Figure 2 will provide optimum device performance for the MAX1172.

Voltage Reference

The MAX1172 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5V typical), V_{FB} (-2.5V typical) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800Ω. The +2.5V voltage source for reference V_{FT} must be current limited to 20mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3.

In addition, there are five reference ladder taps (V_{ST}, VR_{T1}, VR_{T2}, VR_{T3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0V), VR_{T2} is the midpoint of the ladder (0.0V typical), and V_{SB} is the sense for the bottom of the reference ladder (-2.0V). VR_{T1} and VR_{T3} are quarter-point ladder taps (+1.0V and -1.0V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full-scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5V and -2.5V typical, respectively). V_{ST} and V_{SB} can be used to monitor the actual full-scale input voltage of the device. VR_{T1}, VR_{T2}, and VR_{T3} should not be driven to the expected ideal values, as is commonly done with standard flash converters. A decoupling capacitor of 0.01µF connected to AGND from each tap is recommended to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the MAX1172 is laser trimmed to optimize performance with ±2.5V references, its accuracy will degrade if operated beyond a ±2% range.

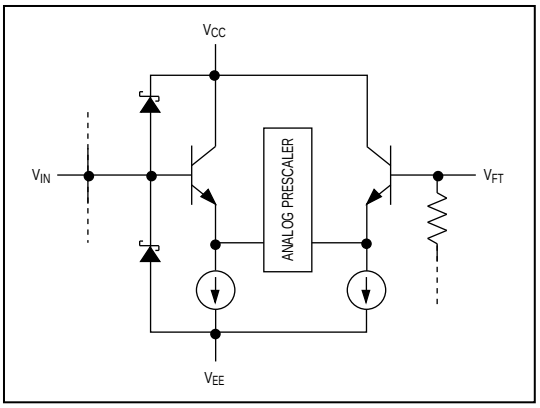


Figure 3. Analog Equivalent Input Circuit

An example of a recommended reference driver circuit is shown in Figure 2. IC1 is REF-03, the +2.5V reference with a tolerance of 0.6% or ±0.015V. The 10kΩ potentiometer supports an adjustable range of 150mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. Adjust R1 and R4 such that V_{ST} and V_{SB} are exactly +2.0V and -2.0V, respectively.

The following errors are defined:

+FS error = top of ladder offset voltage
$= \Delta(+FS - V_{ST})$

-FS error = bottom of ladder offset voltage
$= \Delta(-FS - V_{SB})$

Where the +FS (full scale) input voltage is defined as the output 1LSB above the transition of 1–10 and 1–11, and the -FS input voltage is defined as the output 1LSB below the transition of 0–00 and 0–01.

Analog Input

V_{IN} is the analog input. The full-scale input range will be 80% of the reference voltage or ±2V with V_{FB} = -2.5V and V_{FT} = +2.5V.

The drive requirements for the analog inputs are minimal compared to those of conventional flash converters, due to the MAX1172's extremely low 5pF input capacitance and high 300kΩ input impedance. For example, for an input signal of ±2Vp-p with an input frequency of 10MHz, the peak output current required for the driving circuit is only 628µA.

Clock Input

The MAX1172 is driven from a single-ended TTL input (CLK). The clock pulse width (t_{PWH}) must be kept between 15ns and 300ns to ensure proper operation of the internal track/hold amplifier (Figure 1a). When operating the MAX1172 at sampling rates above 3Msps, it is recommended that the clock input duty cycle be kept at 50% to optimize performance (Figure 4). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤ 4.5V, t_{RISE} < 6ns). In the event the clock is driven from a high current source, use a 100Ω (R1, Figure 2) resistor in series to current limit to approximately 45mA.

Digital Outputs

The format of the output data (D0-D11) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a typical propagation delay of 14ns. There is a one clock cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise times and fall times are not symmetrical. The rise time's typical propagation delay is 14ns, and the typical fall time is 6ns (Figure 5). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
> +2.0V + 1/2LSB	1	11 1111 1111
+2.0V - 1LSB	0	11 1111 111Ø
0.0V	0	ØØ ØØØØ ØØØØ
-2.0V + 1LSB	0	00 0000 000Ø
< -2.0V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

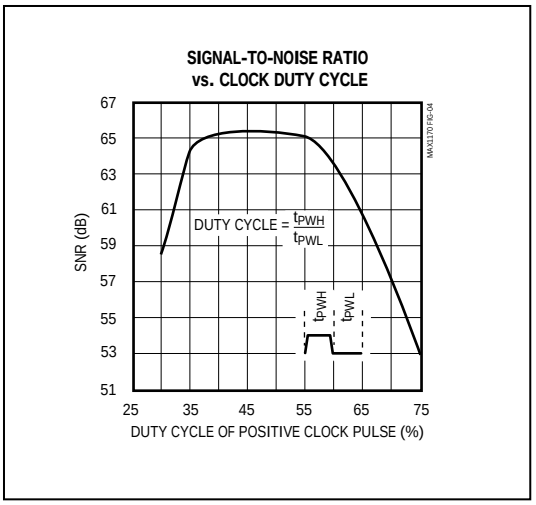


Figure 4. Signal-to-Noise Ratio vs. Clock Duty Cycle

Overrange Output

The overrange output (D12) is an indication that the analog input signal has exceeded the full-scale input voltage by 1LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the MAX1172 in higher resolution systems.

Evaluation Board

The MAX1170 evaluation kit (EV kit) is available to aid designers in demonstrating the full performance of the MAX1172 (or of the MAX1170/MAX1171). This board includes a reference circuit, clock driver circuit, output data latches, and on-board reconstruction of the digital data. A separate EV kit manual describing the operation of this board is available. Contact the factory for price and availability.

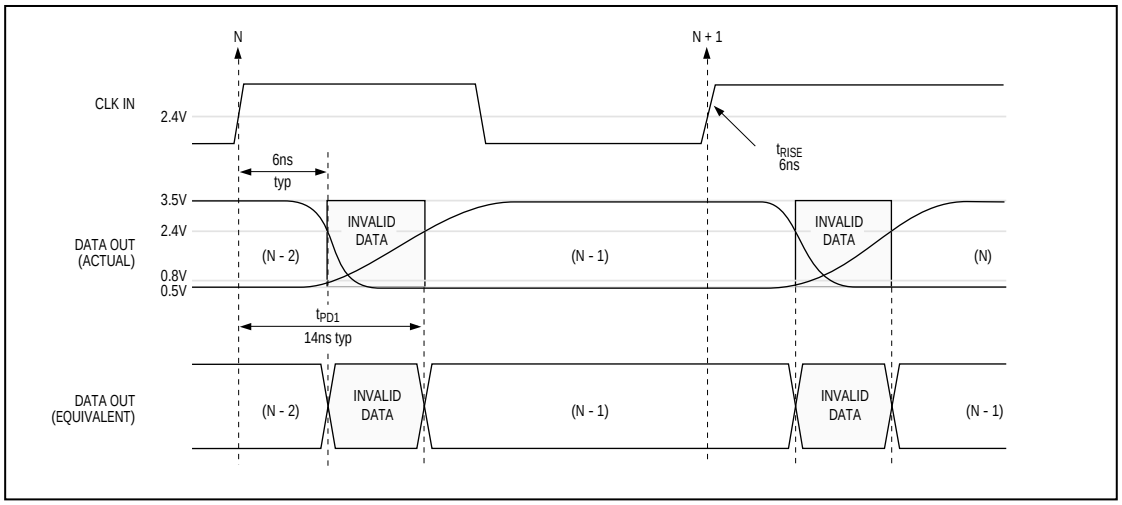
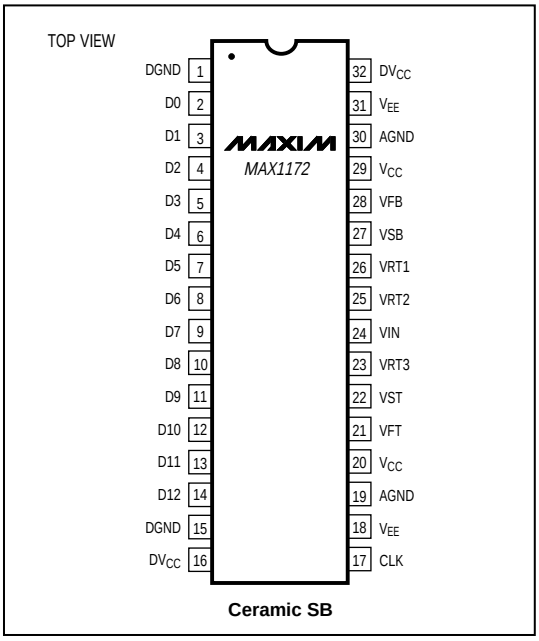


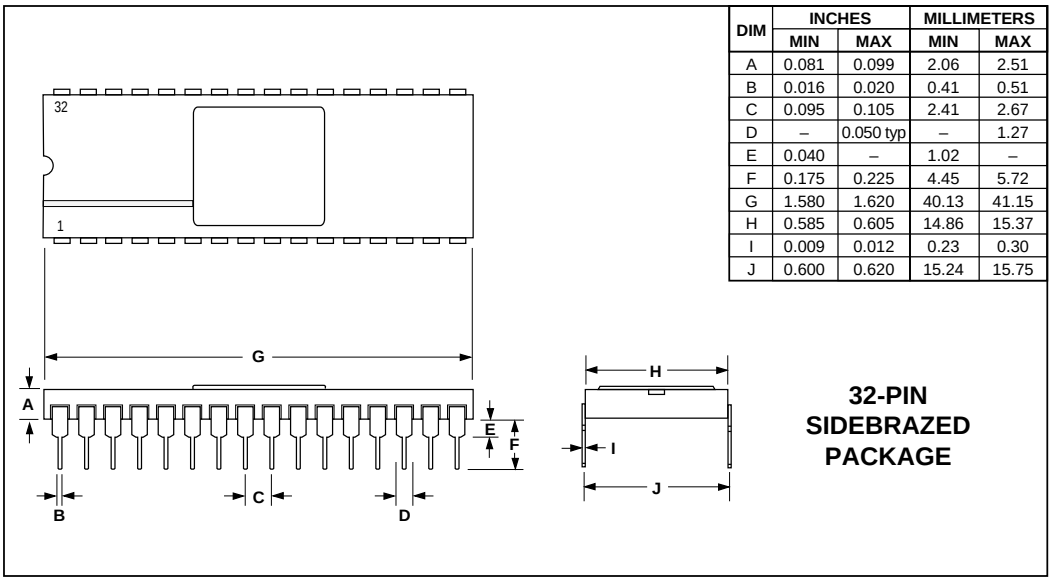
Figure 5. Digital Output Characteristics

___Pin Configurations (continued)



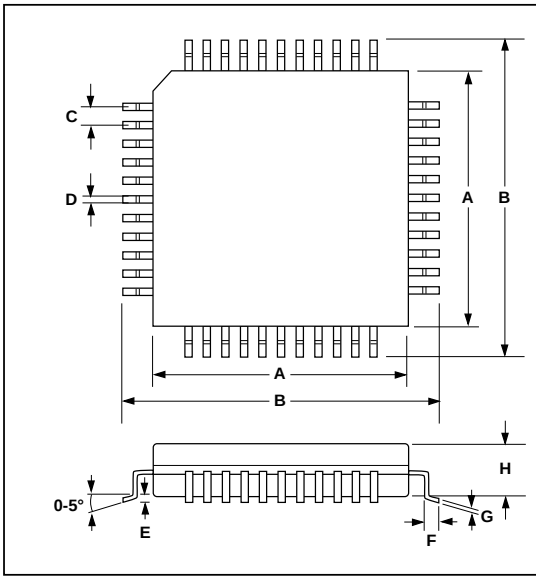
Ceramic SB

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D	–	0.050 typ	–	1.27
E	0.040	–	1.02	–
F	0.175	0.225	4.45	5.72
G	1.580	1.620	40.13	41.15
H	0.585	0.605	14.86	15.37
I	0.009	0.012	0.23	0.30
J	0.600	0.620	15.24	15.75

32-PIN SIDEBRAZED PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.546 typ	0.000	14.00 typ	–
B	0.679	0.694	17.40	17.80
C	0.038	0.040	0.98	1.02
D	0.016 typ	0.000	0.40 typ	–
E	0.008 typ	0.000	0.20 typ	–
F	0.027	0.051	0.70	1.30
G	0.006 typ	0.000	0.15 typ	–
H	0.115	0.140	2.96	3.58

44-PIN CERQUAD

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