8/7/6/5/4/3/2/1-Phase Synchronous-Rectified Buck Controller for Next Generation GPU Core Power

General Description

The uP9511 is an 8/7/6/5/4/3/2/1-phase PWM controller specifically designed to provide high-precision output voltage system for next generation GPUs. The uP9511 provides programmable output voltage and active voltage positioning functions to adjust the output voltage as a function of the load current, so it is optimally positioned for a load current transient.

The uP9511 supports NVIDIA Open Voltage Regulator 8 with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage and the output voltage is precisely regulated to the reference input.

The uP9511 adopts continuous total DCR current sensing for load line programming. The uP9511 provides hardware setting to adjust the operating phase number in different load current state. The uP9511 uses MOSFET $R_{DS(ON)}$ current sensing for channel current balance.

Other features include adjustable soft-start, channel current limit, under voltage protection, over voltage protection and power good output. The uP9511 is available in VQFN5x5-40L package.

Ordering Information

Order Number	Package	Top Marking
uP9511PQGJ	VQFN5x5 - 40L	uP9511P

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

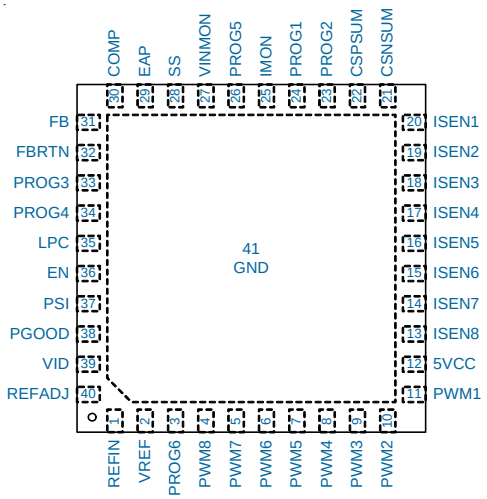
Features

- **Support NVIDIA's Open VReg Type 8 PWMVID Technology**
- **Selectable 8/7/6/5/4/3/2/1-Phase Operation by Hardware Setting**
- **Differential Remote Voltage Sensing**
- **Continuous Inductor DCR Current Sensing Voltage Adjustment**
- **Switching Frequency Adjustment**
- **Operating Phase Number Adjustment**
- **Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing**
- **Adjustable Soft-Start**
- **Channel Current Limit Protection**
- **Over/Under Voltage Protection**
- **Over Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

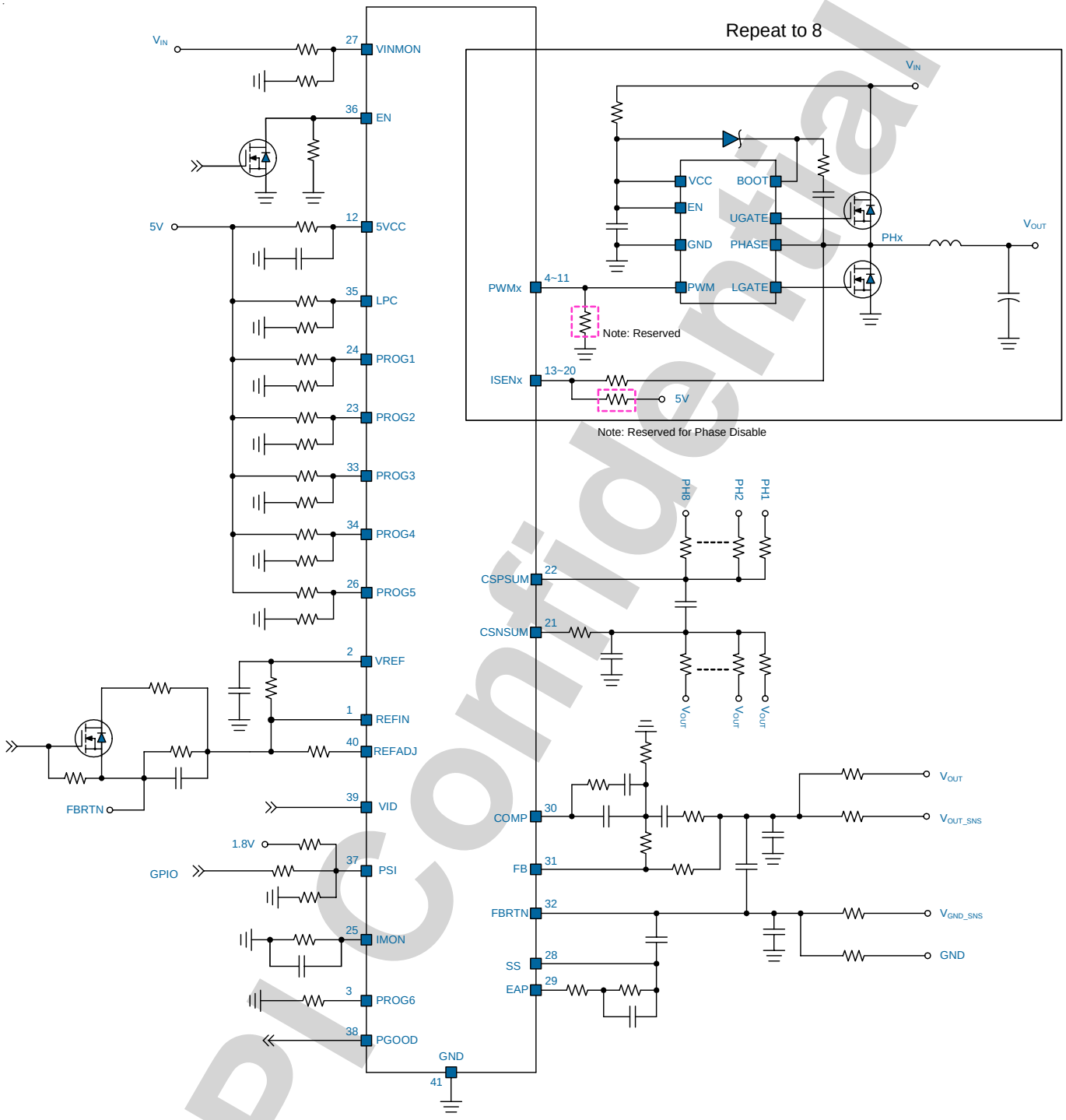
- **Middle-High End GPU Core Power Supplies**

Pin Configuration



uPI Confidential

Typical Application Circuit



uPI Confidential

Functional Pin Description

No.	Name	Pin Function
1	REFIN	**Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit.
2	VREF	**Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1 uF decoupling capacitor between this pin and GND.
3	PROG6	**Function Setting Pin 6.** Connect a resistor from this pin to GND to set the switching frequency.
4	PWM8	**Phase 8 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
5	PWM7	**Phase 7 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
6	PWM6	**Phase 6 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
7	PWM5	**Phase 5 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
8	PWM4	**Phase 4 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
9	PWM3	**Phase 3 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
10	PWM2	**Phase 2 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
11	PWM1	**Phase 1 PWM Output.** Connect this pin to the PWM input of external MOSFET driver.
12	5VCC	**Supply Input for the IC.** Connect this pin to a 5V voltage source with a 2.2Ω + 1uF filter.
13	ISEN8	**ISEN8.** Connect this pin to the PHASE8 pin with a resistor to sense phase 8 output current.
14	ISEN7	**ISEN7.** Connect this pin to the PHASE7 pin with a resistor to sense phase 7 output current.
15	ISEN6	**ISEN6.** Connect this pin to the PHASE6 pin with a resistor to sense phase 6 output current.
16	ISEN5	**ISEN5.** Connect this pin to the PHASE5 pin with a resistor to sense phase 5 output current.
17	ISEN4	**ISEN4.** Connect this pin to the PHASE4 pin with a resistor to sense phase 4 output current.
18	ISEN3	**ISEN3.** Connect this pin to the PHASE3 pin with a resistor to sense phase 3 output current.
19	ISEN2	**ISEN2.** Connect this pin to the PHASE2 pin with a resistor to sense phase 2 output current.
20	ISEN1	**ISEN1.** Connect this pin to the PHASE1 pin with a resistor to sense phase 1 output current.
21	CSNSUM	**Inverting Input of Total Current Sense Amplifier.**
22	CSPSUM	**Non-Inverting Input of Total Current Sense Amplifier.**
23	PROG2	**Function Setting Pin 2.** Connect this pin to the 5VCC with a voltage divider to set the phase reduction threshold and hysteresis.
24	PROG1	**Function Setting Pin 1.** Connect this pin to the 5VCC with a voltage divider to set the phase reduction threshold and hysteresis.
25	IMON	**Output Current Monitor.** The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMON voltage proportional to the total output current. A capacitor can be connected from IMON to GND to adjust the response time of IMON.
26	PROG5	**Function Setting Pin 5.** Connect this pin to the 5VCC with a voltage divider to set the load line enable threshold and hysteresis.
27	VINMON	**Power Stage Input Voltage Monitor.** Connect this pin to the power stage input VIN with a voltage divider. The controller senses the voltage on this pin for power stage input voltage VIN detection.

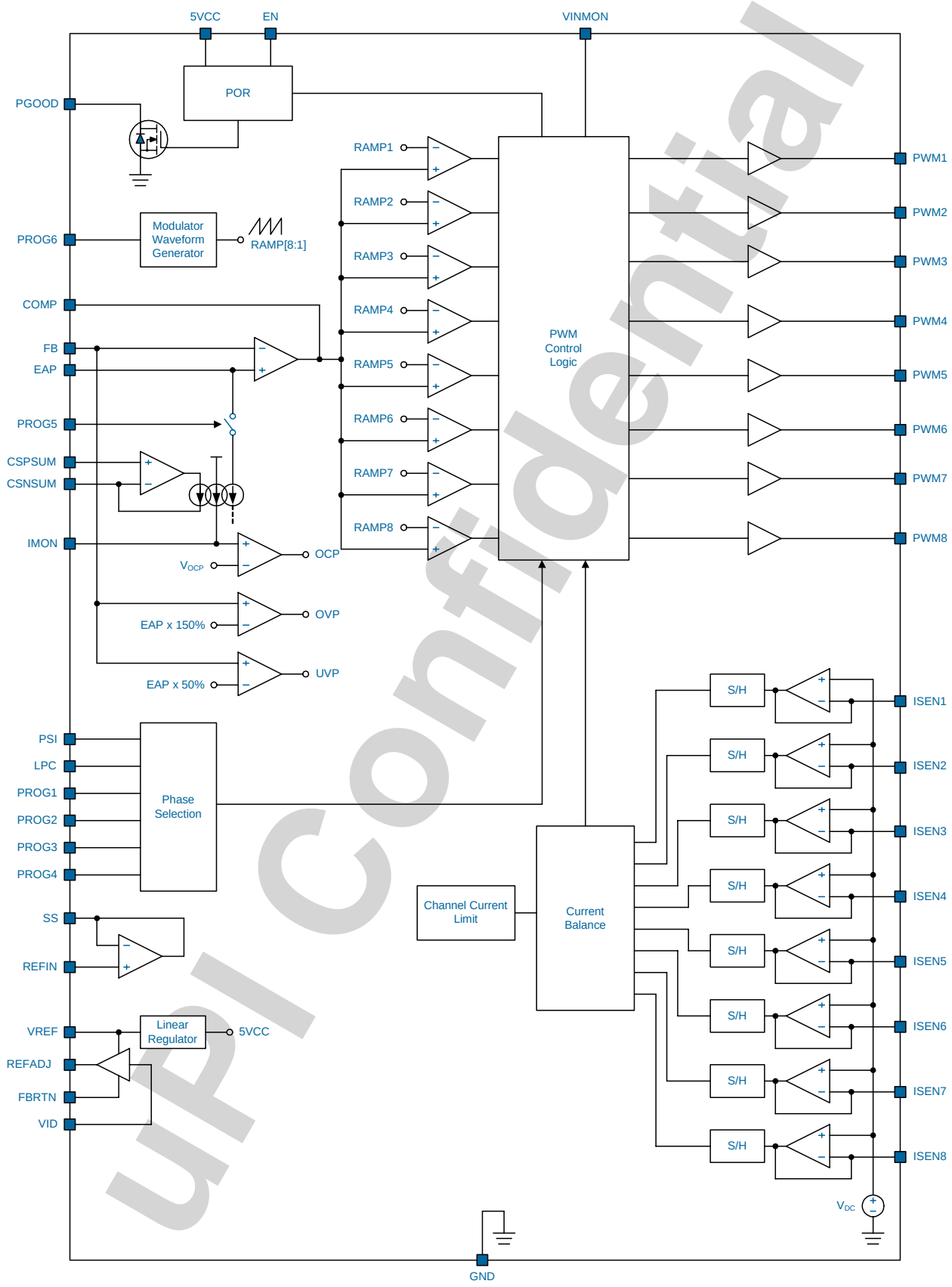
UPI Confidential

Functional Pin Description

No.	Name	Pin Function
28	SS	**Soft Start.** A capacitor connected between SS and FBRTN sets the soft start ramp-up time.
29	EAP	**Non-inverting Input of the Error Amplifier.** Connect a resistor between this pin and SS pin to set the droop (load line) function.
30	COMP	**Output of Control Loop Error Amplifier.**
31	FB	**Inverting Input of the Error Amplifier.**
32	FBRTN	**Output Voltage Feedback Return.** Inverting input to the differential voltage sense amplifier. FBRTN is the reference point in REFIN output voltage measurement.Connect this pin directly to the GPU output voltage feedback return sense point.
33	PROG3	**Function Setting Pin 3.** Connect this pin to the 5VCC with a voltage divider to set the phase reduction threshold and hysteresis.
34	PROG4	**Function Setting Pin 4.** Connect this pin to the 5VCC with a voltage divider to set the phase reduction threshold and hysteresis.
35	LPC	**Low Phase Count.** Connect a voltage divider to this pin to sets the operation phase number of Cold Boot mode and Warm Boot mode.
36	EN	**Enable.** Connect a resistor R_{EN} (ranging from 30k Ω to 10k Ω) from this pin to ground and place this resistor close to the controller. Do NOT use other resistance values other than the values specified here. Do not connect any capacitor directly to this pin. Refer to the typical application circuit, it is recommended to use a MOSFET with its drain connected to EN pin without a pull-up resistor for power sequence control. Do NOT connect EN pin directly to a voltage source for sequence control.
37	PSI	**Power Saving Input.** An input pin receiving power saving control signal from GPU.
38	PGOOD	**Power Good Indication.** Connect this pin to a voltage source with a pull-up resistor.
39	VID	**VID.** PWMVID input pin.
40	REFADJ	**Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
Exposed Pad		**Ground.** The exposed pad is the ground of logic control circuits, it must be soldered to a large PCB and connected to GND.

uPI Confidential

Functional Block Diagram



uPI Confidential

Functional Description

Power On Reset (POR)

Figure 1 shows the power ready detection circuit. The 5VCC voltage is monitored for power on reset with typically 4.3V threshold at its rising edge. When 5VCC is ready, the controller waits for EN to start up. When EN pin is driven above 0.4V, the controller begins its start up sequence. When EN pin is driven below 0.2V, the controller will be turned off, and it will clear all fault states to prepare to next soft-start once the controller is re-enabled.

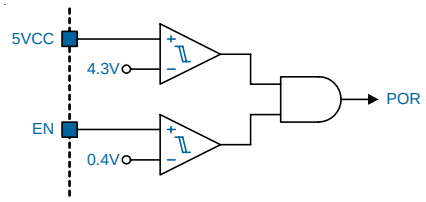


Figure 1. Circuit of Power Ready Detection

Power Input Monitor

VINMON is the power stage input voltage sense pin. Connect this pin to power stage input voltage (VIN) with a voltage divider and always keep VINMON of power stage input voltage. When VINMON less than typically 0.5V at POR, the uP9511 will forces starts up at single phase and disables the cold boot, warm boot, PSI and auto-phase function. Once this condition is triggered, it can only be reset by re-POR or EN restart.

Phase Number of Operation (Hardware Programming)

The uP9511 supports 8/7/6/5/4/3/2/1-phase operation. The maximum phase number of operation is determined by checking the status of ISENx pins when power on reset. Normally, uP9511 is 8-phase operation. Pull ISEN8 to 5VCC with a 100kΩ for 7-phase operation; Pull ISEN7 to 5VCC with a 100kΩ for 6-phase operation and so on. When operating in 7-phase, PWM8 outputs are set to high impedance; in 6-phase, PWM[8:7] outputs are set to high impedance and so on. The maximum phase number of operation is decided and latched at each POR rising edge. The unused ISENx pins and PWMx pins can be left floating.

Operation Frequency

The phase switching frequency of the uP9511 is set by an external resistor connected between PROG6 pin and GND.

Table 1 lists the operation frequency and the recommended resistor R_{PROG6} value.

Table 1. Operation Frequency and Recommended R_{PROG6}

Switching Frequency (kHz)	Recommended R_{PROG6} Resistor (kΩ)
200	51
300	33
400	24
500	20
600	16

Power Saving Mode

The uP9511 provides power saving features for platform designers to program platform specific power saving configuration. There are three operation modes: Full-Phase mode, Auto-Phase mode, and Low-Phase mode. The uP9511 switches between these three operation modes according to the input voltage level of the PSI pin. Figure 2 shows typical PSI application circuit, and table 2 shows recommended PSI setting voltage level of three operation modes. In low-phase mode, it can separate into Cold Boot Mode and Warm Boot Mode. The operation phase number of Cold Boot Mode and Warm Boot Mode is determined by LPC pin. In auto-phase mode, the operation phase number will auto increasing/reducing according to output loading. In Full-Phase mode, the maximum phase number of operation is determined by checking the status of ISENx pins when POR.

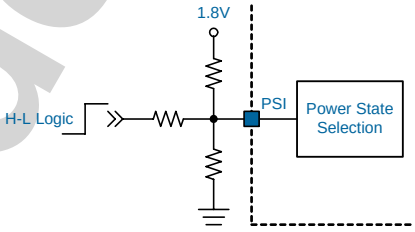


Figure 2. PSI application circuit

Table 2. Operation Mode and recommended V_{PSI}

Operation Mode	Recommended Voltage Setting at PSI
Full-Phase Mode	1.8V
Auto-Phase Mode	1V
Low-Phase Mode	GND

Auto-Phase Shedding

The uP9511 provide Auto-Phase Shedding function to reduce the switching and conduction losses at light load condition and enable high efficiency over a wide range of output current. Auto-Phase Shedding function is activated by two conditions:

1. PSI voltage stays at “Auto-Phase Mode”.
2. After PGOOD goes high, VID pin received the PWM-VID input signal from GPU.

Once the Auto-Phase Shedding function activated, the uP9511 compares the V_{IMON} with V_{PROG1}/V_{PROG2}/V_{PROG3}/V_{PROG4} to decide the operation phase number dynamically. Connect each PROGx pins to 5VCC with a voltage divider to set the threshold and hysteresis. The threshold and the hysteresis can be calculated as:

$$V_{PROGx} = \frac{R_{BOT}}{R_{TOP} + R_{BOT}} \times 5V_{CC} = \left(\frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{SUM}} \right) \times R_{IMON} + 0.6$$

UPI Confidential

Functional Description

$$V_{PROGx_Hys} = 10uA \times (R_{TOP} \parallel R_{BOT}) = \left(\frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{SUM}} \right) \times R_{IMON} + 0.6$$

Where R_{TOP} is the resistor connects from 5VCC to PROGX pin, and R_{BOT} is the resistor connects from PROGX pin to GND.

If $V_{IMON} < V_{PROG1}$, uP9511 operates in single phase; if $V_{PROG1} < V_{IMON} < V_{PROG2}$, uP9511 operates in dual phase; if $V_{PROG2} < V_{IMON} < V_{PROG3}$, uP9511 operates in four phase; if $V_{PROG3} < V_{IMON} < V_{PROG4}$, uP9511 operates in six phase; if $V_{IMON} > V_{PROG4}$, uP9511 operates in 8 phase. The uP9511 always keeps all-of-phase interleaved operation. **When setting PROG1, PROG2, PROG3 and PROG4, always keep $V_{PROG1} < V_{PROG2} < V_{PROG3} < V_{PROG4}$. Violating this rule may lead to unknown status and should be avoided.** Short the PROG1, PROG2, PROG3 and PROG4 to GND to disable the auto-phase mode.

Cold Boot and Warm Boot

The uP9511 features programmable operation phase number of Cold Boot Mode and Warm Boot Mode. When PSI=Low and uP9511P first boots up (first time of 5VCC and EN goes high), controller will enter to Cold Boot Mode. Except the first boot up, when PSI=Low state and controller power up by EN control, then uP9511 will enter to Warm Boot Mode. Connect LPC pin to 5VCC with a voltage divider (Figure 3) to set the operation phase number of Cold Boot Mode and Warm Boot Mode. Figure 4 shows all the power states of uP9511 under each combination of 5VCC/EN/PSI/VID signal. Table 3 shows the recommended resistance of the voltage divider.

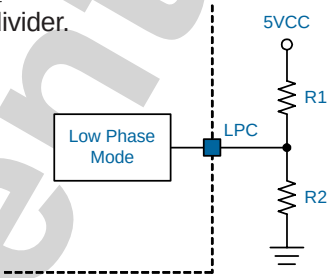


Figure 3. Circuit of LPC Setting

Table 3. Recommended resistance of Cold Boot mode and Warm Boot mode

V_{LPC} = % of 5VCC	Cold Boot Phase Count	Warm Boot Phase Count (kΩ)									
		1-phase		2-phase		3-phase		4-phase		5-phase	
		R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
40.63%	1-phase	4.92	3.37	24.61	16.84	44.3	30.32	73.84	50.53	147.67	101.06
46.88%	2-phase	4.27	3.77	21.33	18.83	38.4	33.89	63.99	56.48	127.99	112.95
53.13%	3-phase	3.76	4.27	18.82	21.34	33.88	38.4	56.47	64.01	112.93	128.01
59.38%	4-phase	3.37	4.92	16.84	24.62	30.31	44.31	50.52	73.86	101.04	147.71
65.63%	5-phase	3.05	5.82	15.24	29.1	27.43	52.37	45.71	87.29	91.42	174.57
71.88%	6-phase	2.78	7.11	13.91	35.56	25.04	64.01	41.74	106.69	83.47	213.37
78.13%	7-phase	2.56	9.14	12.8	45.72	23.04	82.3	38.4	137.17	76.8	274.35
84.38%	8-phase	2.37	12.8	11.85	64.02	21.33	115.24	35.55	192.06	71.11	384.12

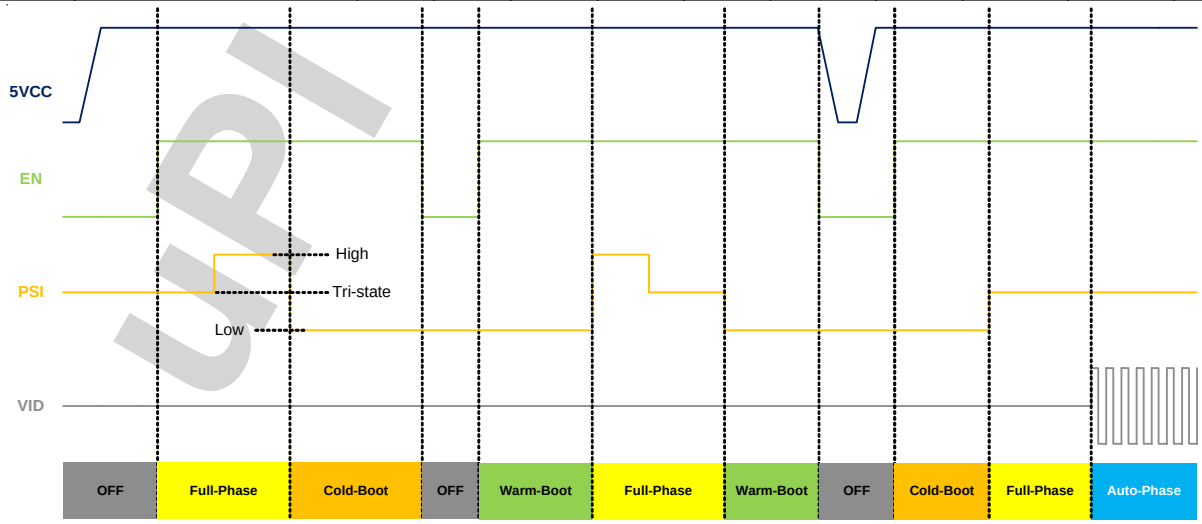


Figure 4. Power States of uP9511

UPI Confidential

Total Load Current Sense

The uP9511 uses a low input offset current sense amplifier (CSA) to sense the total load current flowing through inductors for droop function by CSPSUM and CSNSUM as shown in Figure 5.

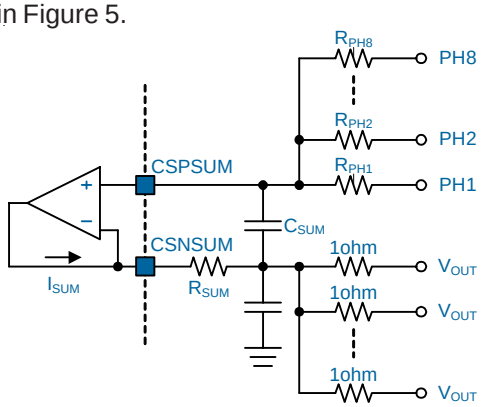


Figure 5. Total Load Current Sense

The voltage across C_{SUM} is proportional to the total load current, and the output current of CSA(I_{SUM}) is also proportional to the total load current of the voltage regulator. The sensed current I_{SUM} represents the total output current of the regulator, and it is directly used for droop function, total output over current protection and auto-phase function. I_{SUM} is calculated as follows.

$$I_{SUM} = \frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{SUM}}$$

In this inductor current sensing topology, R_{PH} and C_{SUM} must be selected according to the equation below:

$$k \times \frac{L}{R_{DC}} = \frac{R_{PH} \times C_{SUM}}{N}$$

where R_{DC} is the DCR of the output inductor L, N is the operation phase number. Theoretically, k should be equal to 1 to sense the instantaneous total load current. But in real application, k is usually between 1.2 to 1.8 for better load transient response. Note that the resistance value of R_{SUM} must be less than 2kΩ to ensure the current sensing circuit in normal operation.

Voltage Control Loop

Figure 6 illustrates the voltage control loop of the uP9511. FB and EAP are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} and the duty cycle of buck converter to force FB voltage VFB follows V_{EAP}. The sensed current signal (I_{SUM}) is mirrored to the EAP pin and creates voltage at EAP pin as:

$$V_{EAP} = V_{SS} - I_{SUM} \times R_{LL}$$

where V_{SS} is output of V_{REFIN}, I_{SUM} is a current source proportional to output current, and R_{LL} is an external resistor for adjusting load line slope. Therefore, the output voltage will be:

$$V_{OUT} = V_{SS} - \frac{I_{OUT} \times R_{DC} \times R_{LL}}{N \times R_{SUM}}$$

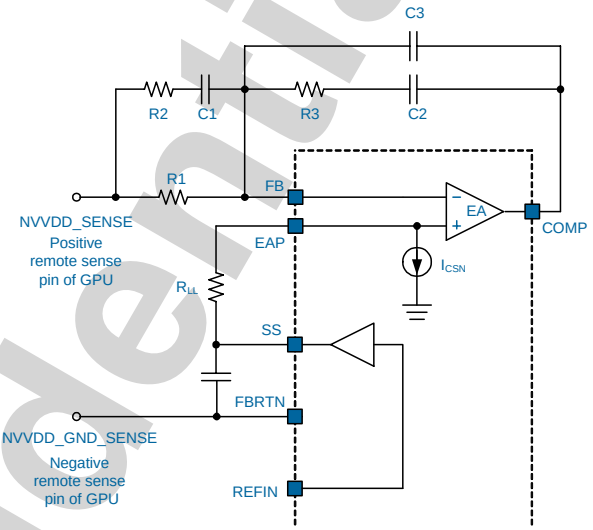


Figure 6. Voltage Control Loop

Output Voltage Differential Sense

The uP9511 uses differential sense by a high-gain low offset error amplifier for output voltage differential sense as shown in Figure 7. The GPU voltage is sensed by the FB and FBRTN pins. FB pin is connected to the positive remote sense pin NVVDD_SENSE of the GPU via the resistor R_{FB}. FBRTN pin is connected to the negative remote sense pin NVVDD_GND_SENSE of GPU directly.

Soft Start and Power Up Sequence

The uP9511 features a programmable soft start function to limits the prevent surge current from power supply input by a soft-start capacitor C_{SS} connected between SS to FBRTN pin. Controller starts the soft-start process right on V_{EN}>0.6V with typical 2ms initialization time (T_{INIT}). When soft-start cycle is initiated, an internal current source charges the C_{SS} to V_{REFIN}. The ramp up time (Tramp) during soft start period is determined by the internal current source and C_{SS}, and it can be calculated as below.

$$Tramp = \frac{V_{REFIN,BOOT} \times C_{SS}}{I_{SS}}$$

For example, suppose $V_{REFIN, BOOT}$ = 0.9V, C_{SS} = 22nF, I_{SS} = 13uA, the ramp up time is around 1.5ms.

If there is no fault detected at the end of soft-start, the controller then asserts PGOOD when the output voltage reaches its target without delay. Figure 7 shows the soft-start sequence of the uP9511.

upi confidential

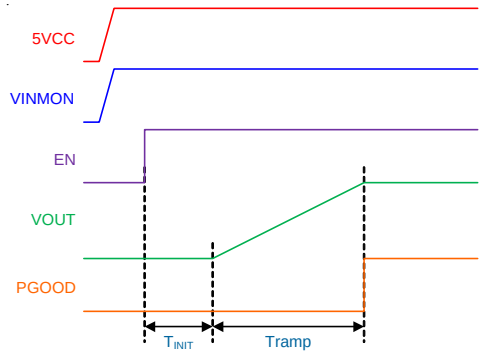


Figure 7. Power Up Sequence

PWMVID Function

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} =$$

$$V_{VREF} \times D \times \frac{R2 // (R3+R4+R5)}{R1+R2 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5} +$$

$$V_{VREF} \times \frac{R1 // (R3+R4+R5)}{R2+R1 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5}$$

where V_{REFIN} is the DC voltage of REFIN, V_{VREF} is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input. The VREF pin is an internal LDO, therefore an output decoupling capacitor is required. Recommend connecting at least a 1uF capacitor from VREF pin to local GND.

Boot Voltage and Standby Mode

The new generation PWMVID structure includes two operation modes other than normal operation: boot mode and standby mode. During boot mode, the GPU stops sending PWMVID signal and the input of the PWMVID buffer is floating. The REFADJ pin enters high impedance state after the VID pin enters tri-state region, and the REFIN voltage can then be calculated as:

$$V_{REFIN,BOOT} = V_{REF} \times \frac{R4+R5}{R2+R3+R4+R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 8 to generate the standby mode voltage:

$$V_{REFIN,STDBY} =$$

$$V_{VREF} \times \frac{(R3+R4+R5) // R_{STDBY}}{R2+(R3+R4+R5) // R_{STDBY}} + \frac{R4+R5}{R3+R4+R5}$$

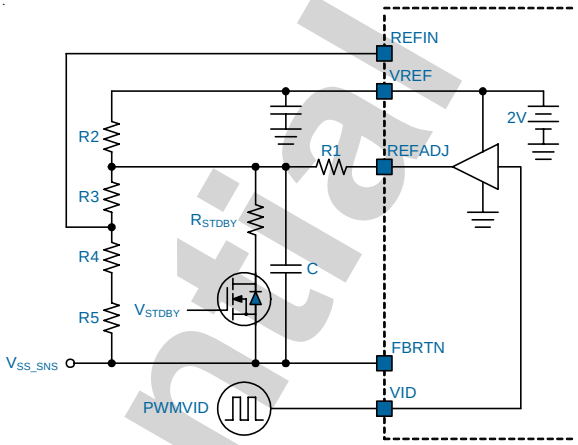


Figure 8. PWMVID structure

Load Line Enable Threshold

The uP9511 compares the V_{IMON} with V_{PROG5} to enable the Load Line function. Connect each PROG5 pins to 5VCC with a voltage divider to set the load line enable threshold and hysteresis. The load line enable threshold and the hysteresis is calculated as:

$$V_{PROG5} = \frac{R_{BOT}}{R_{TOP}+R_{BOT}} \times 5V_{CC} = \left(\frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{SUM}} \right) \times R_{IMON} + 0.6$$

$$V_{PROG5_Hys} = 10uA \times (R_{TOP} \parallel R_{BOT}) = \left(\frac{I_{OUT} \times \frac{R_{DC}}{N}}{R_{SUM}} \right) \times R_{IMON} + 0.6$$

Where R_{TOP} is the resistor connects from 5VCC to PROG5 pin, and R_{BOT} is the resistor connects from PROG5 pin to GND.

Channel Current Balance

The uP9511 senses phase currents for current balance by the means of on-resistance of power stage low-side MOSFETs when turning on as shown in Figure 9. The ISENx pins sense the corresponding phase current when the low-side MOSFETs are turned on.

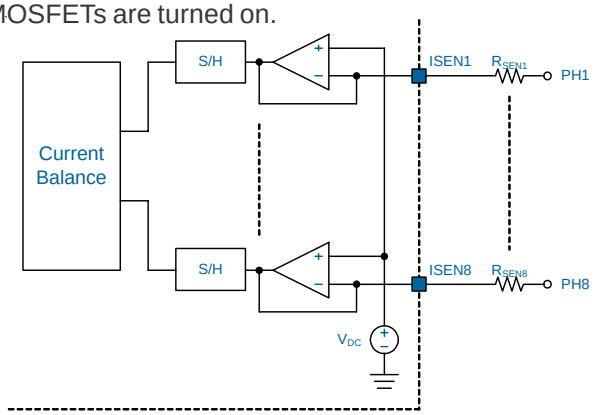


Figure 9. Current Balance Circuit

UPI Confidential

$$I_{SENX} = \frac{I_{PHX} \times R_{DS(ON)} + V_{DC}}{R_{SENX}}$$

where I_{SENX} is the sample and held phase current signal, I_{PHX} is phase current, $R_{DS(ON)}$ is the on-resistance of the low- side MOSFETs, and V_{DC} = 30mV is an internal voltage source. In this current sense mechanism, the valley of the inductor current is sampled and held. Therefore, the equivalent sensed current can be described by the following equation:

$$I_{PHX_SH} = I_{PHX_AVG} - \frac{1}{2} \times \Delta I_{PHX}$$

The sensed current I_{PHX_SH} is mirrored to the current balance circuit, comparing between each other, and generating current adjusting signals for each phase. The current balance circuit increases the duty cycle of the phase whose phase current is smaller than others and decrease the duty cycle of the phase whose phase current is larger than others.

Channel Current Limit

The uP9511 adopts channel valley current limit function to avoid catastrophic damage to power stage components. The uP9511 monitors the sensed current at ISENx pins and if the sensed $I_{SEN[N]}$ of any phase exceeds the channel current limit threshold, the channel current limit function activates. The resistor R_{EN} connected between EN and ground determines the channel current limit the threshold. According the mentioned current sense equation, the channel current limit equation can be written as:

$$I_{MAX_CH} = \frac{\frac{1500uA}{R_{EN}(k\Omega)} \times R_{ISENX} \times \frac{10}{9} - V_{DC}}{R_{DS(ON)}}$$

where 1500uA/R_{EN} denotes the internal CL_CH threshold current, R_{EN} is the EN pin to ground resistor in KΩ (e.g. R_{EN} = 30kΩ, CL_CH = 50uA), R_{ISENX} is the external sensing resistor connected at ISENx pins, V_{DC} is an internal 30mV voltage source, and $R_{DS(ON)}$ is the on-resistance of the low-side MOSFETs of the power stage in mΩ. Once the per-phase current exceeds CL_CH threshold, the per-phase output inductor current is limited to an average current. If a continuous over load event may lead the output voltage drop and eventually trigger under voltage protection and shuts down the uP9511.

Enable Sequence Control

The EN pin controls the enable and disable of this device. The resistor R_{EN} connected between EN pin to ground is also used to implement this function. It is recommended to use a MOSFET with its drain connected to EN pin without pull up resistor for power sequence control as shown in Figure 10. Do NOT connect EN pin directly to a voltage source.

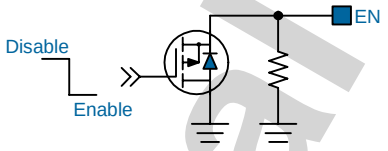


Figure 10. Enable Sequence Control

Total Output Current Protection

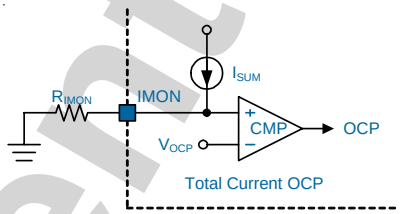


Figure 11. Total Output Current Protection

The uP9511 provides total current OCP as shown in Figure 11. The sensed current I_{SUM} is mirrored internally and fed to IMON pin. A resistor R_{IMON} is connected from IMON pin to GND. This current flows through the resistor R_{IMON}, creating voltage drop across it. As the total load current increases, the voltage on IMON pin (V_{IMON}) increases proportionally. When the IMON pin voltage is greater than V_{OCP}, the OCP will be triggered. Once OCP is triggered, it will be latched. Only re-start up can release the latch. The uP9511 will turn off both high-side and low-side MOSFETs of all channels. The total OCP level is changed per actual operating phase number. Table 4 shows the relationship between total OCP levels (V_{OCP}) and operating phase number. The total output current (I_{OUT_MAX}) of triggered OCP is calculated as :

$$I_{OUT_MAX} = \frac{V_{OCP} - 0.6V}{R_{IMON}} \times \frac{N \times R_{SUM}}{R_{Dc}}$$

The IMON pin has a 0.6V offset voltage, which means the IMON voltage increases from 0.6V as load current increases. The resistor R_{IMON} must be in the range of 10K to 60K to let the 0.6V offset mechanism work normally.

Table 4. Operation Conditions and Total Output OCP Level (V_{OCP})

Operation Condition	OCP Level (V_{OCP})
8-Phase	3.0V
7-Phase	2.7V
6-Phase	2.4V
5-Phase	2.1V
4-Phase	1.8V
3-Phase	1.6V
2-Phase	1.3V
1-Phase	1.1V

uPI Confidential

Over Voltage Protection (OVP)

The OVP is triggered if V_{FB} > 1.5x V_{EAP} sustained 5us. When OVP is activated, the uP9511 turns on all low-side MOSFETs and turns off all high-side MOSFETs. The over voltage protection is a latch-off function and can only be reset by 5VCC re-POR or EN restart.

Under Voltage Protection (UVP)

The under voltage protection is triggered if V_{FB} < 0.5 x V_{EAP} sustained 5us. When UVP is activated, the uP9511 turns off all high-side and low-side MOSFETs. The under voltage protection is a latch-off function and can only be reset by 5VCC re-POR or EN restart.

Over Temperature Protection (OTP)

The uP9511 monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP9511 is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by 5VCC re-POR or EN restart.

uPI Confidential

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, 5VCC ---------- -0.3V to +6V
Other Pins ---------- 0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN5x5 - 40L θ_{JA} ---------- 36°C/W
VQFN5x5 - 40L θ_{JC} ---------- 3°C/W
Power Dissipation, P_D @ T_A = 25°C
VQFN5x5 - 40L ---------- 2.78W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC5} ---------- 4.5V to 5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

uPI Confidential

Electrical Characteristics

(5VCC = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
5VCC POR Threshold	POR_{5VCC}	5VCC rising	4	4.3	4.5	V
5VCC POR Hysteresis	HYS_{5VCC_POR}		--	300	--	mV
Supply Current	I_{5VCC}	EN high , No switching	--	4.5	--	mA
Shutdown Current	I_{SD}	EN = 0V	--	250	--	uA
Power Stage Input Voltage Monitoring						
VINMON monitoring range			0.7	--	2.6	V
VINMON Rising Threshold	V_{VINMON}		--	0.5	--	V
VINMON Hysteresis	V_{VINMON_HYS}		--	100	--	mV
Enable Control						
Logic Low Threshold	V_{IL_EN}		--	--	0.2	V
Logic High Threshold	V_{IH_EN}		0.4	--	--	V
2V VREF Voltage						
VREF Voltage Accuracy	V_{REF}		1.98	2	2.02	V
VREF Sourcing Current	I_{REF}		10	--	--	mA
Referenece Input Voltage (REFIN)						
REFIN Disable Threshold	V_{REFIN_DSB}		--	--	0.1	V
External Reference Voltage Range	V_{REFIN}		0.2	--	2	V
PWMVID Buffer						
VID input Low Level	V_{IL_VID}		--	--	0.6	V
VID input High Level	V_{IH_VID}		1.2	--	--	V
VID Tri-state Delay	T_{TRI_VID}		--	100	--	ns
VREFADJ Source Resistance	R_{BF_SRC}	I_{SRC} = 1mA	--	20	--	Ω
VREFADJ Sink Resistance	R_{BF_SNK}	I_{SINK} = 1mA	--	20	--	Ω
Oscillator						
Operation Frequency Range	F_{SW}		200	--	600	kHz
Operation Frequency Accuraccy		R_{PROG6} = 33kΩ	270	300	330	kHz
PROG6 Output Voltage			--	1.2	--	V
Soft-Start						
Soft-Start Current	Iss	Normal(during soft-start period)	--	13	--	uA
		REFIN Transient	--	220	--	
Initialization Time	T_{INIT}	EN high to Vout Start up from 0V	--	2	--	ms

uPI Confidential

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	--	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	--	10	--	MHz
Trans-conductance	GM		--	1500	--	uA / V
COMP Source Current	I_{COMP_SRC}		--	300	--	uA
COMP Sink Current	I_{COMP_SNK}		--	300	--	uA
FBRTN						
FBRTN Current	I_{FBRTN}	EN = 1.4V, No Switching	--	--	500	uA
Current Sense Amplifier (Total Current Summing)						
Input Offset Voltage	V_{OFF_CSA}		-1	--	1	mV
Max Sourcing Current	I_{SRC_CSA}		200	--	--	uA
Current Sense Amplifier (Current Balance)						
Input Offset Voltage	V_{OFF_CSA}		-1	--	1	mV
Max Sourcing Current	I_{SRC_CSA}		200	--	--	uA
ISENx Voltage	V_{DC_CSA}		25	30	35	mV
PWM Output						
Output Low Voltage	V_{PWM_L}	I_{SNK} = 4mA	--	--	0.2	V
Output Hight Voltage	V_{PWM_H}	I_{SOURCE} = 4mA	4.7	--	--	V
High Impedance State Leakage		V_{PWM} = 0V	-1	--	0	uA
		V_{PWM} = 5V	0	--	1	uA
Power Saving Input (PSI)						
Power Saving Mode Logic	V_{PSI}	Full-Phase Mode	1.4	--	--	V
		Auto-Phase Mode	0.8	--	1.2	V
		Low-Phase Mode	--	--	0.4	V
Auto-Phase/Load Line						
Internal Sink Current	I_{SNK}		--	10	--	uA
Current Monitoring for Droop/IMON						
Current Mirror Accuracy		I_{EAP}/I_{MON}	95	100	105	%
Offset Voltage	V_{IMON_OFS}		--	0.6	--	V
Protection						
Channel Current Limit (CL_CH) Threshold	I_{OC_CH}	$I_{SENx} > I_{CL_CH}$, R_{EN} = 30kΩ	--	50	--	uA
Total Current Protection (OCP) Threshold	V_{OCP}	$V_{IMON} > V_{OCP}$, 8-phase mode	--	3	--	V
Under Voltage Protection (UVP) Threshold	V_{UVP}	V_{FB}/V_{EAP}	40	--	50	%
Under Voltage Protection (UVP) Delay	T_{UVP}		--	5	--	us

UPI Confidential

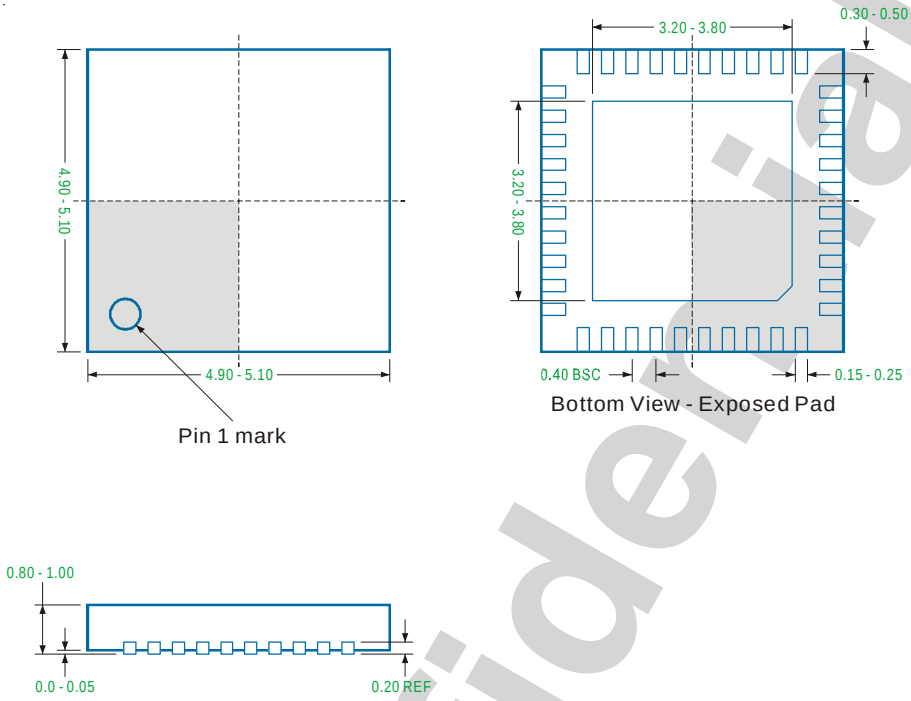
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection (cont'd)						
Over Voltage Protection (OVP) Threshold	V_{OVP}	V_{FB}/V_{EAP}	150		--	%
Over Voltage Protection (OVP) Delay	T_{OVP}		--	5	--	us
Over Temperature Protection (OTP)	T_{OTP}	Guaranteed by Design	--	150	--	°C
Power Good Indicator						
PGOOD Output Low Level	V_{PG}	I_{SINK} = 4mA	--	--	0.3	V
PGOOD Leakage Current	I_{PG_Leak}	V_{PG} = 5V	--	--	0.2	uA

uPI Confidential

Package Information

VQFN5x5 - 40L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

uPI Confidential

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the taerms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

COPYRIGHT (c) 2015, UPI SEMICONDUCTOR CORP.

uPI Confidential

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064