ABRIDGED DATA SHEET

19-6003; Rev 0; 8/11

MAX24188
Low-Cost IEEE 1588 Clock

General Description

The MAX24188 is a flexible, low-cost IEEE 1588 clock designed to be the central 1588 time base in a multiport system. In such systems (typically boundary clocks or transparent clocks) timestampers at the ports must all have a common time and frequency reference. The MAX24188 serves as that common reference. As the system exchanges 1588 packets with an external 1588 master and calculates its time offset vs. the master, the MAX24188 can be adjusted by system software to zero out the time offset and thereby achieve time and frequency synchronization with the master. As the MAX24188 is adjusted, its output frequency and time alignment signals are correspondingly adjusted. All timestampers (and other time-aware components) that receive those signals then follow the adjustment to maintain synchronization with the MAX24188. In this way all 1588 elements in the system maintain a common sense of time and frequency.

The MAX24188 can be a standalone central timing function for 1588 systems. It can also be used in conjunction with one of Maxim's clock synchronization ICs in multimode systems designed to be clocked by 1588, 1588 plus frequency (such as synchronous Ethernet), or frequency only.

Applications

Central Time-Clock for 1588-Enabled Equipment with Timestamping on Multiple Ports
Wireless Base Stations and Controllers
Switches, Routers, DSLAMs, PON Equipment
Pseudowire Circuit Emulation Equipment
Test and Measurement Systems
Medical, Industrial, and Factory Automation Equipment

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX24188ETK+	-40°C to +85°C	68 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

SPI is a trademark of Motorola, Inc.

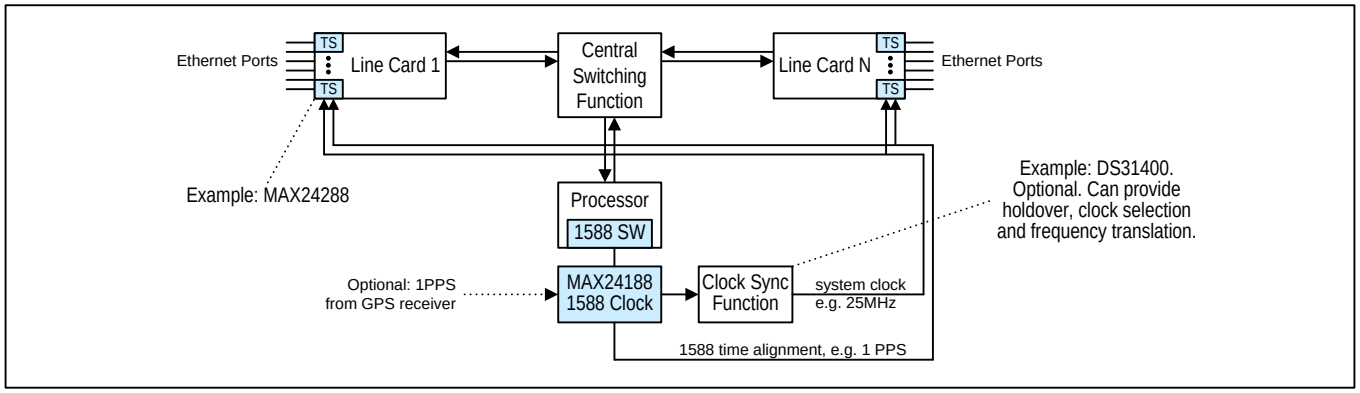
Highlighted Features

- Complete Hardware Support for IEEE 1588
- Flexible Block for Any 1588 Architecture
- Enables Ordinary, Boundary, and Transparent Clocks
- Steered by Software to Follow an External 1588 Master
- 2^{-8}ns Time Resolution and 2^{-32}ns Period Resolution
- 1ns Input Timestamp Accuracy and Output Edge Placement Accuracy
- Three Time/Frequency Controls: Direct Time Write, Time Adjustment, and High-Resolution Frequency Adjustment
- Programmable Clock and Time-Alignment I/O to Synchronize All 1588 Elements in the System
  - Can Provide an Output Clock Signal to Slave Components (125MHz/N, 1 ≤ N ≤ 255)
  - Can Provide an Output Time Alignment Signal to Slave Components (e.g., 1PPS)
  - Can Frequency-Lock to an Input Clock Signal from Elsewhere in the System
  - Can Timestamp an Input Time Alignment Signal to Time-Lock to a Master Elsewhere in the System (e.g., 1PPS)
- Input Event Timestamper Detects Incoming Time Alignment (e.g., 1PPS) or Clock Edges, Can Timestamp Rising and/or Falling Edges
- Flexible Programmable Event Generator (PEG) Can Output 1PPS (One Pulse per Period) or a Wide Variety of Clock Signals
- Built-In Support for Telecom Equipment Timing Architectures with Dual Redundant Timing Cards
- Full Support to Enable Switches and Routers to Be Transparent Clocks and/or Boundary Clocks
- Full Support for 1588 and Synchronous Ethernet
- Operates from a 10MHz, 12.8MHz, 25MHz, or 125MHz Reference Clock
- SPI™ Processor Interface
- 1.2V Operation with 3.3V I/O

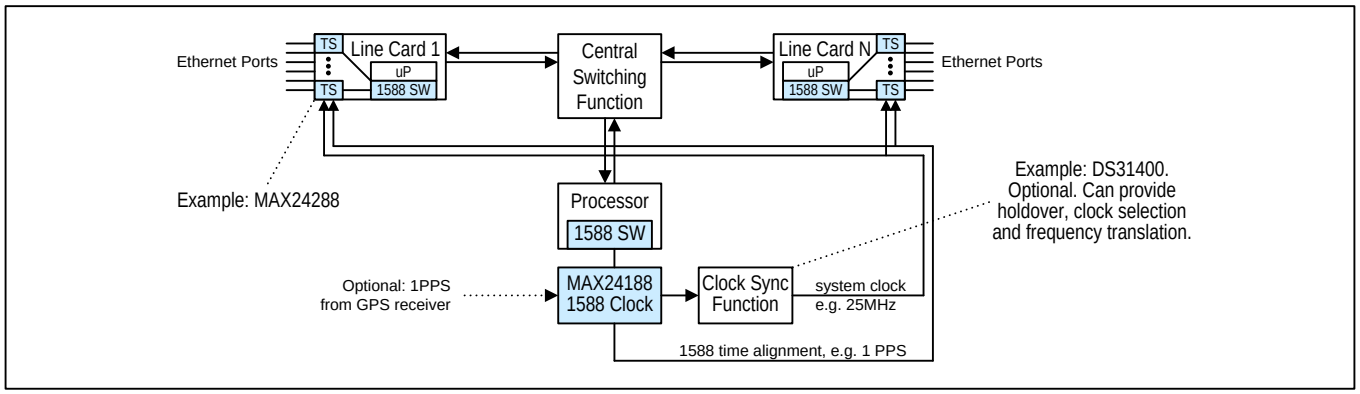
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Application Examples

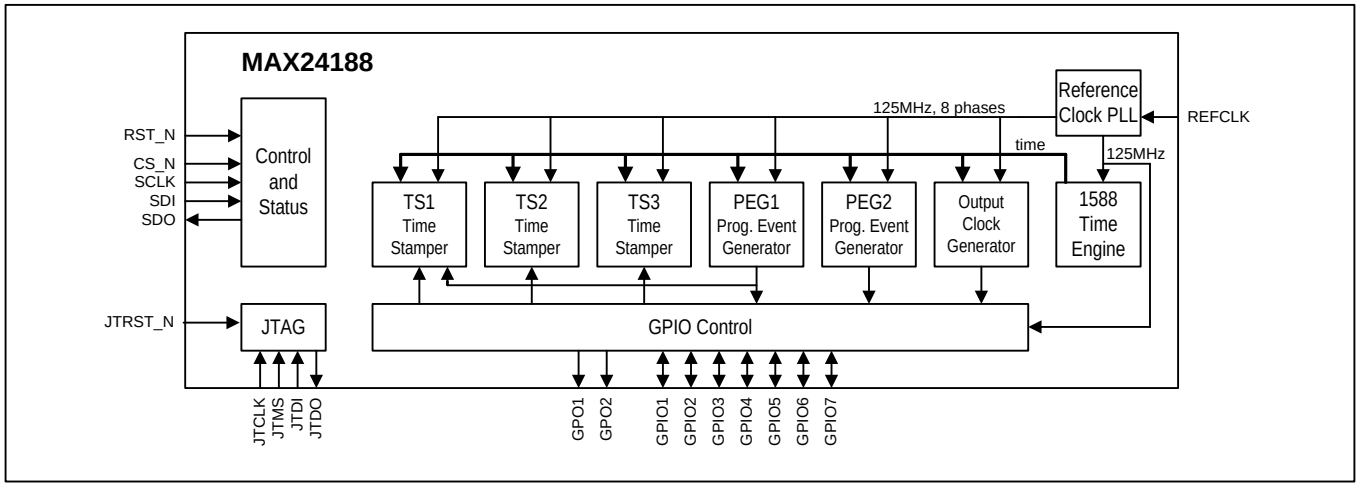
Example 1: Multiport System with Central 1588 Software



Example 2: Multiport System with Distributed 1588 Software



Block Diagram



Note to readers: This document is an abridged version of the full data sheet. To request the full data sheet, go to **www.maxim-ic.com/MAX24188** and click on **Request Full Data Sheet**.

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