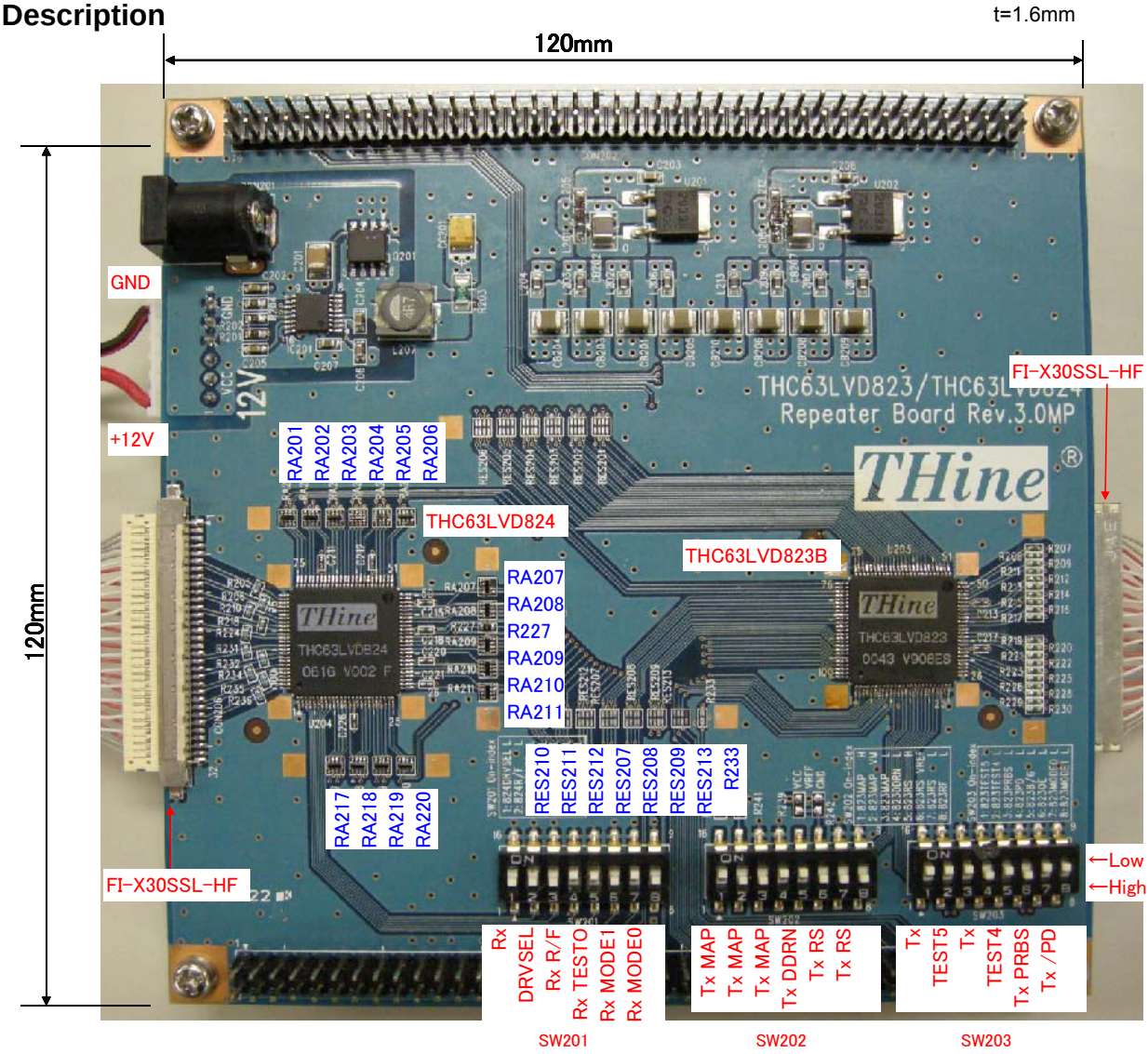
CEL California Eastern Laboratories | THine THine Electronics, Inc.
World's Leading Company in Mixed Signal Technologies

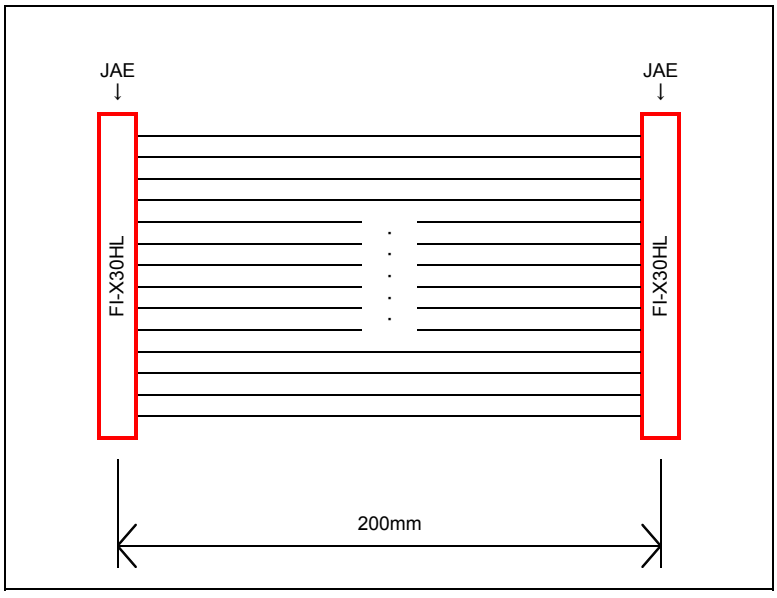
To Our Customers

Continuing it's rich tradition of partnering with high quality Japanese semiconductor suppliers, CEL is now partnering with THine from May of 2015 onwards.

Description



LVDS-Cable Type.



SW201 Setting

* Def. : Default Setting

SW Pin#	* Def.	NodeName	THC63LVD824		
			IC Pin#	PinName	Description
1	H	RX DRVSEL	9	DRVSEL	Output Driverbility Select. H : High power, L : Low power.
2	H	RX R/F	8	R/F	Output Clock Triggering Edge Select. H : Rising edge, L : Falling edge.
3	L	RX TESTO	7	GND	Ground Pins for TTL outputs and digital circuitry.
4	L	RX MODE1	6	MODE1	Pixel Data Mode.
5	L	RX MODE0	5	MODE0	
6	H	RX /PD	4	/PDWN	H : Normal operation, L : Power down (all outputs are pulled to ground)
7	L	RX TEST1	3	GND	Ground Pins for TTL outputs and digital circuitry.
8	H	N/C	-	-	Non Connected.

MODE1	MODE0	Mode
L	L	Dual Link
L	H	Single Link

SW202 Setting

* Def. : Default Setting

SW Pin#	* Def.	Node Name	THC63LVD823B		
			IC Pin#	PinName	Description
1	L	TX MAP	14	MAP	LVDS mapping table select.
2	H				
3	H				
4	L	TX DDRN	13	DDRN	DDR function is active when MODE<1:0> = HL(Single-in/Dual-out mode). Open or H : DDR(Double Edge input) function disable. L : DDR(Double Edge input) function enable.
5	L	TX RS	12	RS	LVDS swing mode, VREF select.
6	H				
7	H				
8	H	TX RF	11	R/F	Input Clock Triggering Edge Select. H : Rising edge, L : Falling edge

SW-Pin#			RS	Mapping Mode
1	2	3		
L	H(open)	H(open)	VIHM	Mapping MODE1
H(open)	L	H(open)	VIMM	Mapping MODE2
H(open)	H(open)	L	VILM	Reserved

SW-Pin#			RS	LVDS Swing	Small Swing Input Support
5	6	7			
L	H(open)	H(open)	VIHM	350mV	N/A
H(open)	L	H(open)	VIMM	350mV	RS=VREFa
H(open)	H(open)	L	VILM	200mV	N/A

a. VREF is Input Reference Voltage.

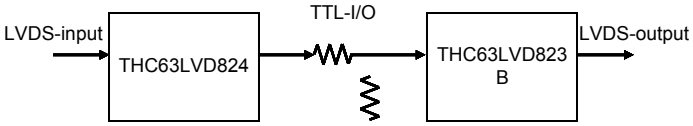
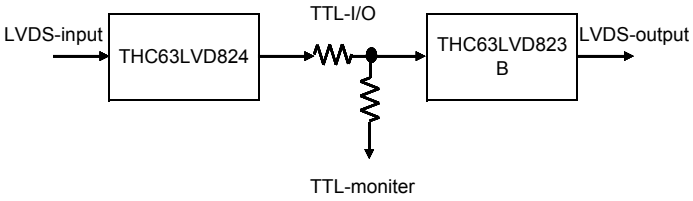
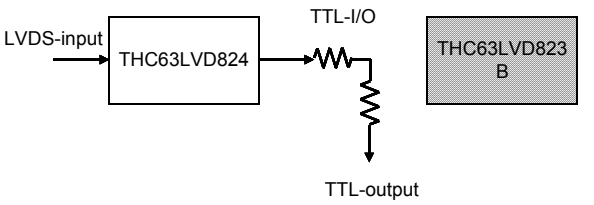
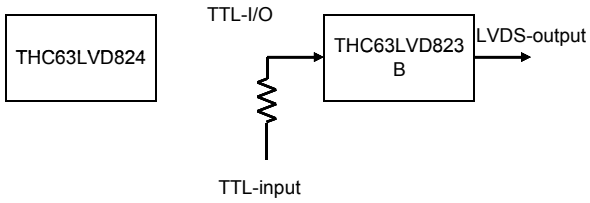
SW203 Setting

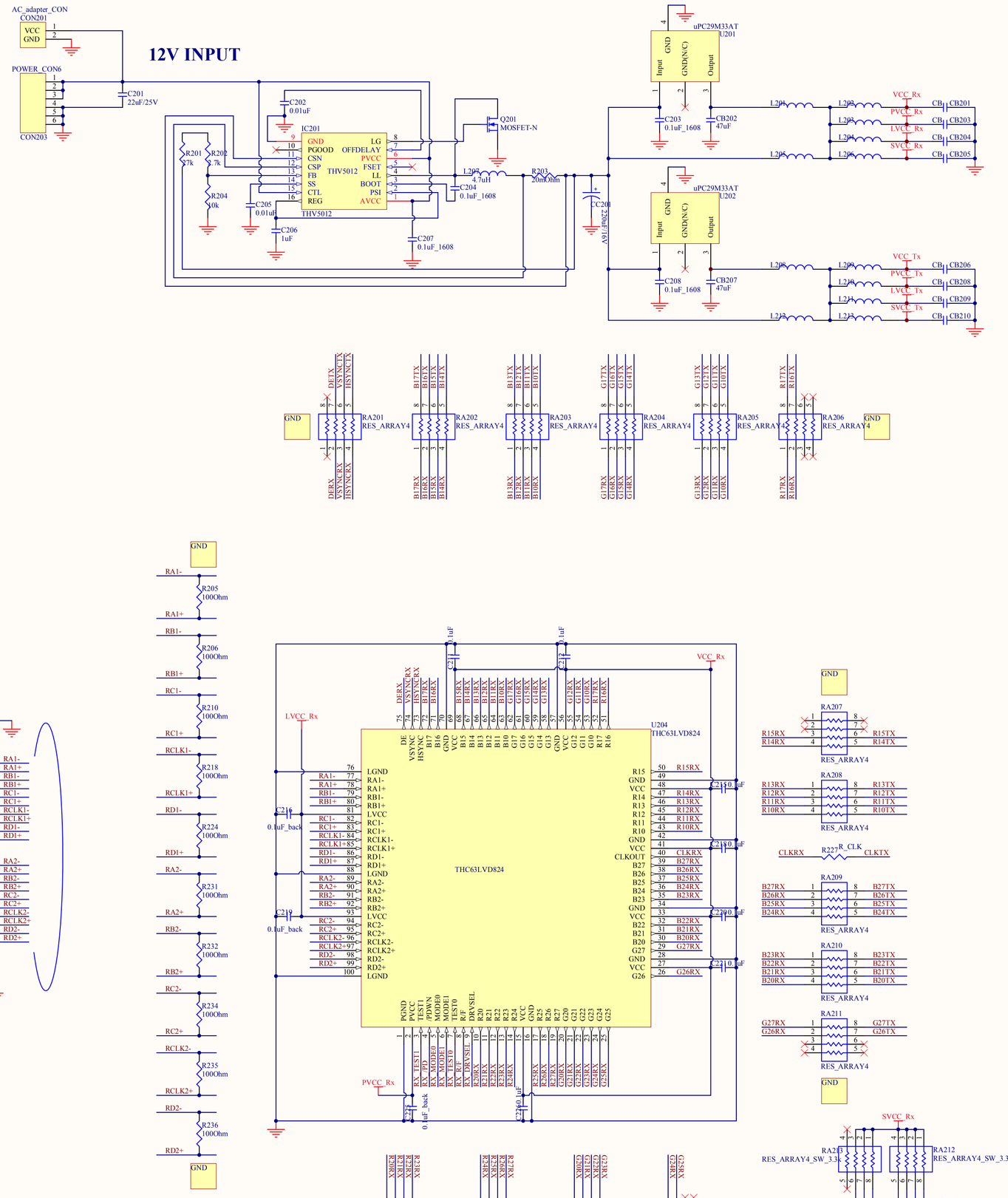
* Def. : Default Setting

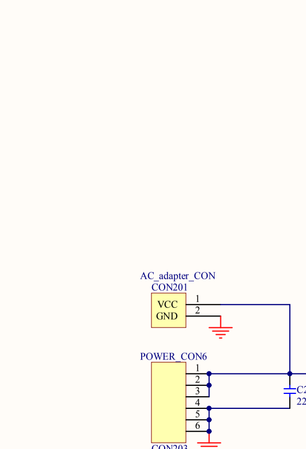
SW Pin#	* Def.	NodeName	THC63LVD823B		
			IC Pin#	PinName	Description
1	H	TX TEST5	22	N/C	Must be Open.
2	L	TX TEST4	21	Reserved	Must be tied to GND.
3	L	TX PRBS	20	PRBS	PRBS(Pseudo-Random Binary Sequence) generator is active in order to evaluate eye patterns when MODE<1:0> = LL(Dual-in/Dual-out mode). H : PRBS generator is enable. L : Normal Operation
4	H	TX /PD	19	/PDWN	H : Normal operation, L : Power down (all outputs are Hi-Z)
5	L	TX 8/6	18	GND	Ground Pins for TTL inputs and digital circuitry.
6	H	TX OE	17	OE	Output enable. H : Output enable, L : Output disable (all outputs are Hi-Z).
7	L	TX MODE0	16	MODE0	Pixel Data Mode
8	L	TX MODE1	15	MODE1	

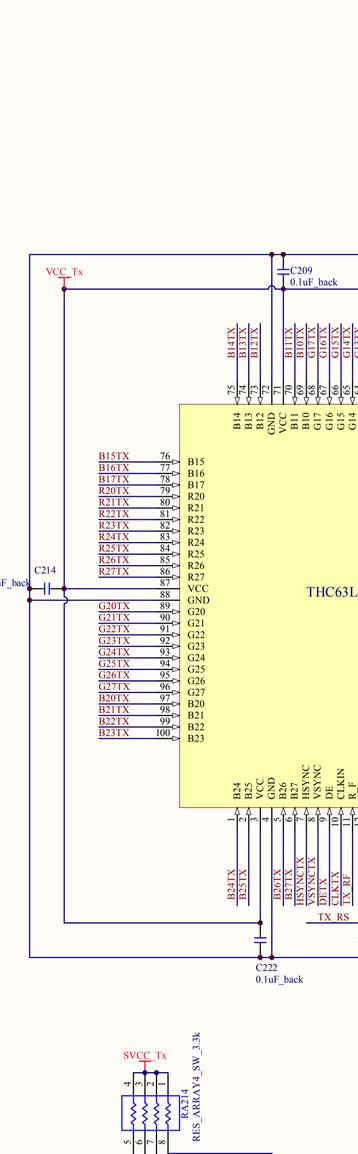
MODE1	MODE0	Mode
L	L	Dual Link(Dual-in/Dual-out)
H	L	Dual Link(Single-in/Dual-out)
L	H	Single Link(Dual-in/Single-out)
H	H	Single Link(Single-in/Single-out)

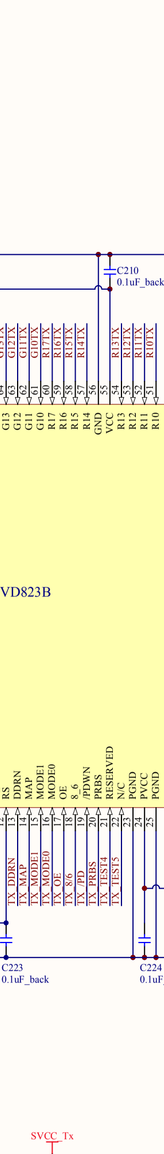
Measures Type

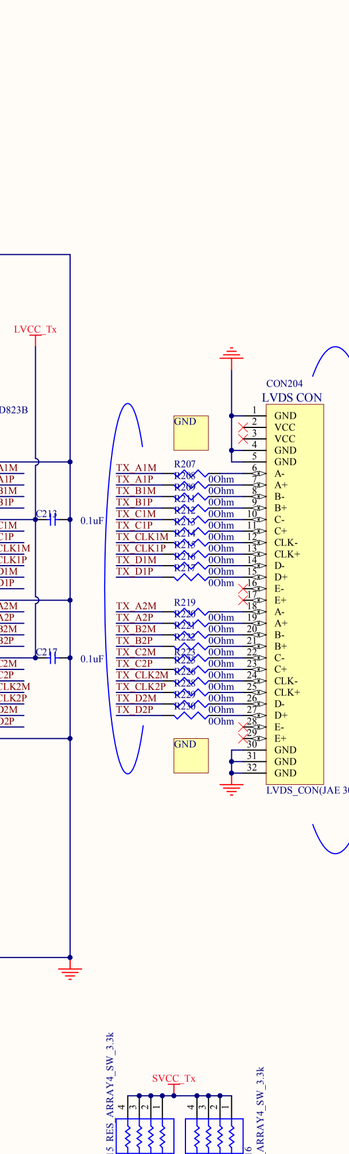
#	Type	Un-Mount	0Ω-Mount	33Ω-Mount
1		RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233		RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210
2			RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233	RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210
3		THC63LVD823B	RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233	RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210
4		RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210	RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233	





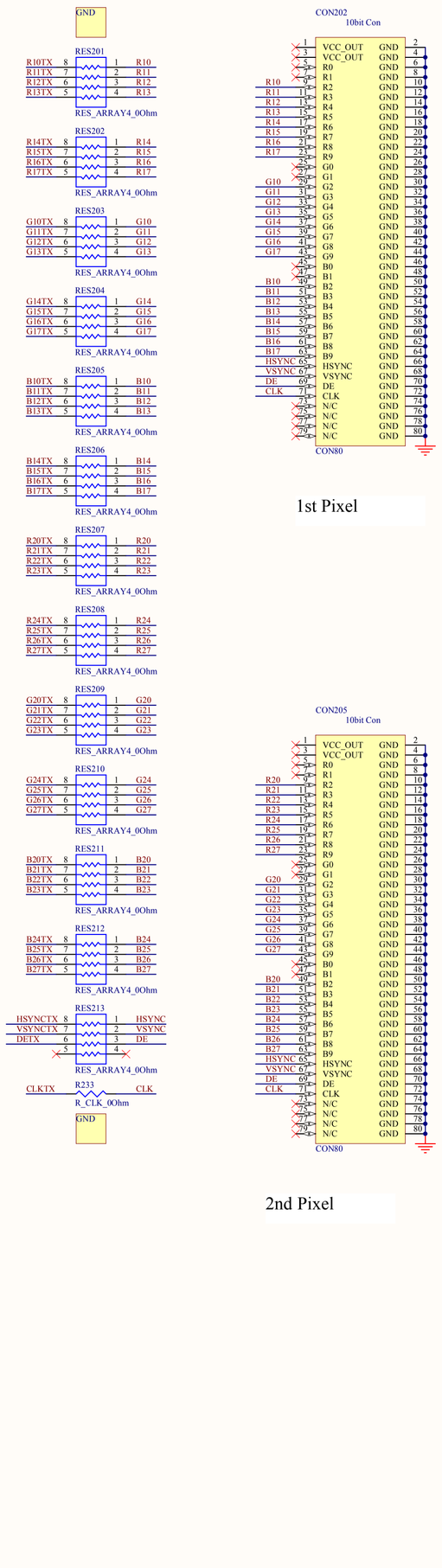






TX_TEXT5 must be open for normal operation.

From Pin header



1st Pixel

2nd Pixel

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Title	THM63LVD823/THC63LVD824 Repeater Board Rev 3.0MP
Size	A1
Number	
Revision	
Date:	2007/11/29
Sheet of	
File:	C:\ran\..\824-823B_rev3mp_E.SCHDOC
Drawn By:	Rei Fujiki

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