# N- and P-Channel 20-V (D-S) MOSFET

## CHARACTERISTICS

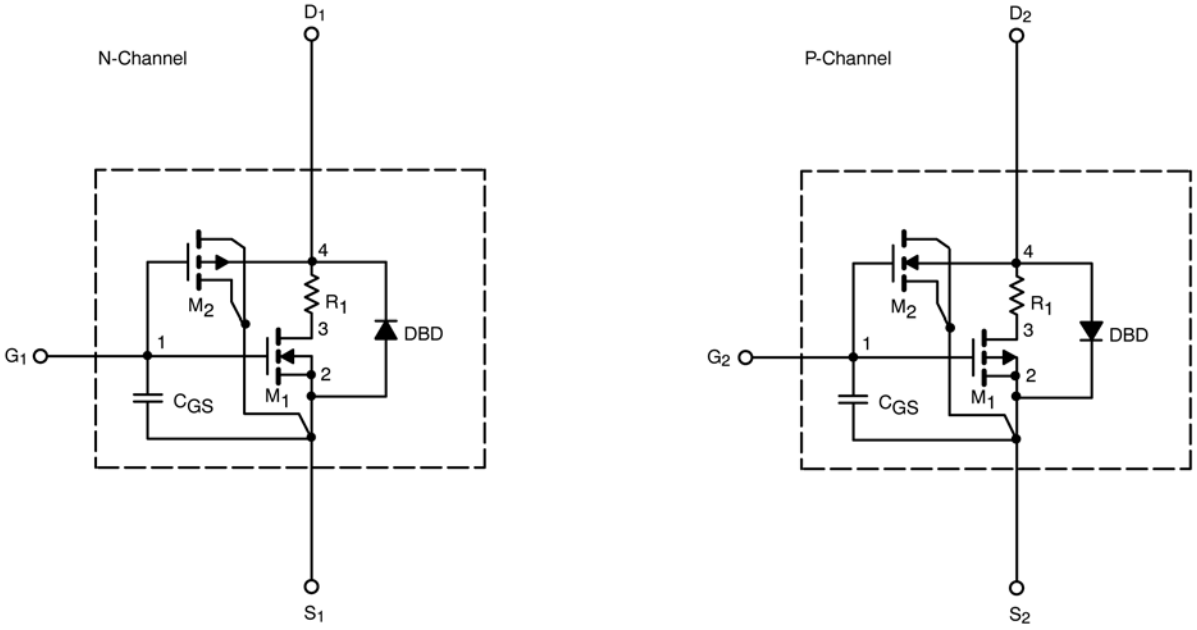
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC



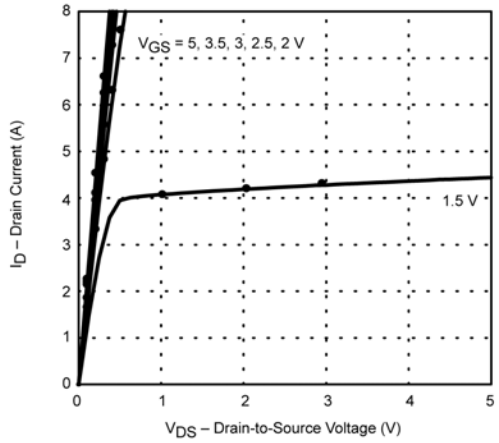

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

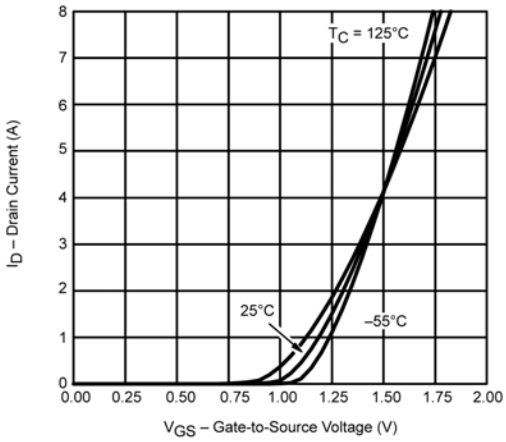
| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | N-Ch | 0.70 | | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | P-Ch | 0.78 | | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ ≥ 5 V, $V_{GS}$ = 4.5 V | N-Ch | 111 | | A |
| | | $V_{DS}$ ≤ –5 V, $V_{GS}$ = –4.5 V | P-Ch | 47 | | |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 3.4 A | N-Ch | 0.048 | 0.047 | Ω |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –2.5 A | P-Ch | 0.088 | 0.086 | |
| | | $V_{GS}$ = 2.5 V, $I_D$ = 3.2 A | N-Ch | 0.056 | 0.054 | |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –2 A | P-Ch | 0.120 | 0.116 | |
| | | $V_{GS}$ = –1.8 V, $I_D$ = –1 A | P-Ch | 0.165 | 0.170 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 5 V, $I_D$ = 3.4 A | N-Ch | 12 | 13 | S |
| | | $V_{DS}$ = –5 V, $I_D$ = –2.5 A | P-Ch | 6.4 | 6 | |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 1.05 A, $V_{GS}$ = 0 V | N-Ch | 0.80 | 0.80 | V |
| | | $I_S$ = –1.05 A, $V_{GS}$ = 0 V | P-Ch | –0.78 | –0.80 | |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | N-Channel $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 3.4 A P-Channel $V_{DS}$ = –10 V, $V_{GS}$ = –4.5 V, $I_D$ = –2.5 A | N-Ch | 4.1 | 4.1 | Nc |
| | | | P-Ch | 4 | 5 | |
| Gate-Source Charge | $Q_{gs}$ | | N-Ch | 0.65 | 0.65 | |
| | | | P-Ch | 0.68 | 0.68 | |
| Gate-Drain Charge | $Q_{gd}$ | | N-Ch | 0.90 | 0.90 | |
| | | | P-Ch | 0.90 | 0.90 | |
| Turn-On Delay Time | $t_{d(on)}$ | N-Channel $V_{DD}$ =10 V, $R_L$ = 10 Ω $I_D$ ≅ 1 A, $V_{GEN}$ = 4.5 V, $R_G$ = 6 Ω P-Channel $V_{DD}$ = –10 V, $R_L$ = 10 Ω $I_D$ ≅ –1 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | N-Ch | 29 | 30 | Ns |
| | | | P-Ch | 45 | 28 | |
| Rise Time | $t_r$ | | N-Ch | 52 | 52 | |
| | | | P-Ch | 53 | 55 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | N-Ch | 27 | 25 | |
| | | | P-Ch | 69 | 55 | |
| Fall Time | $t_f$ | | N-Ch | 27 | 20 | |
| | | | P-Ch | 11 | 32 | |

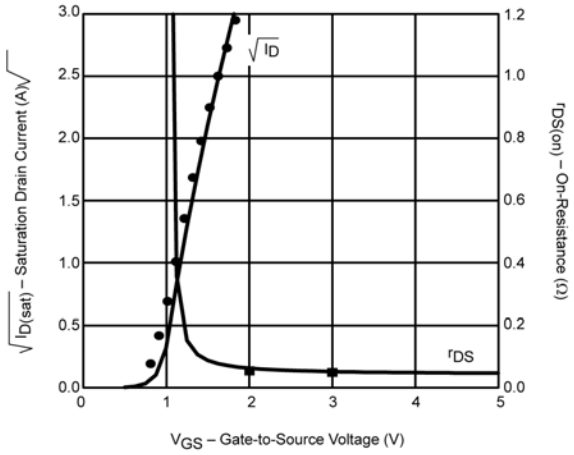
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2.
b. Guaranteed by design, not subject to production testing.

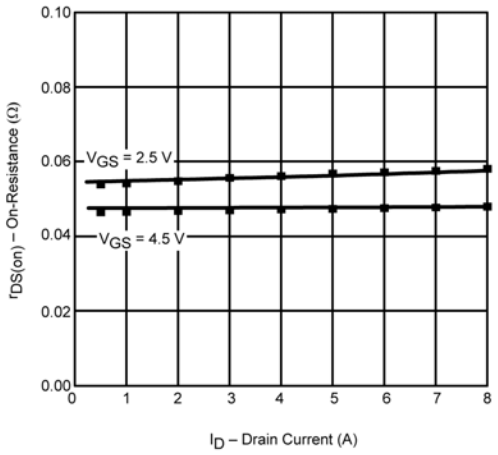
COMPARISON OF MODEL WITH MEASURED DATA ($T_J$=25°C UNLESS OTHERWISE NOTED)

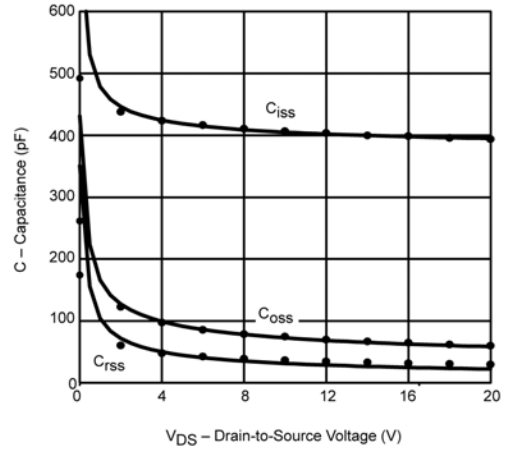
**N-Channel MOSFET**

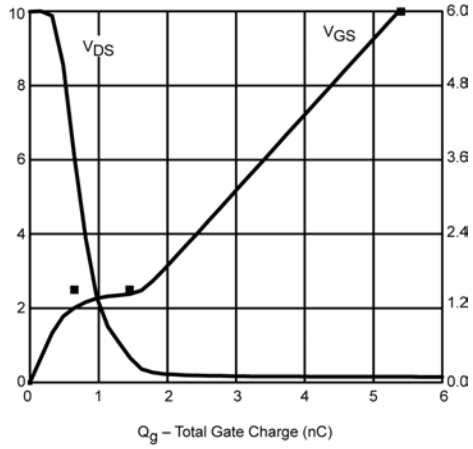


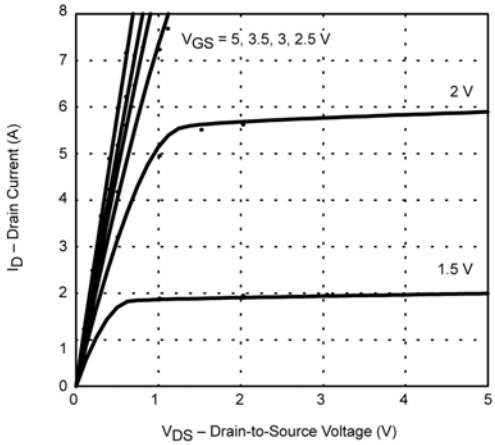



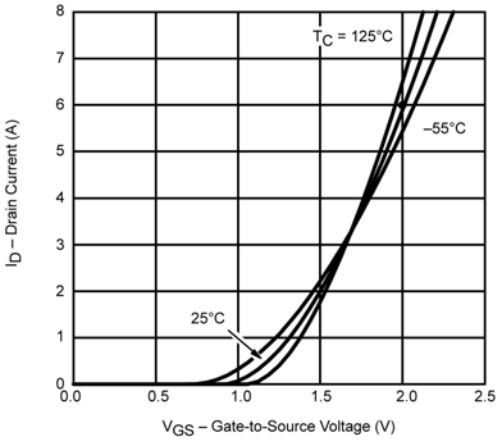



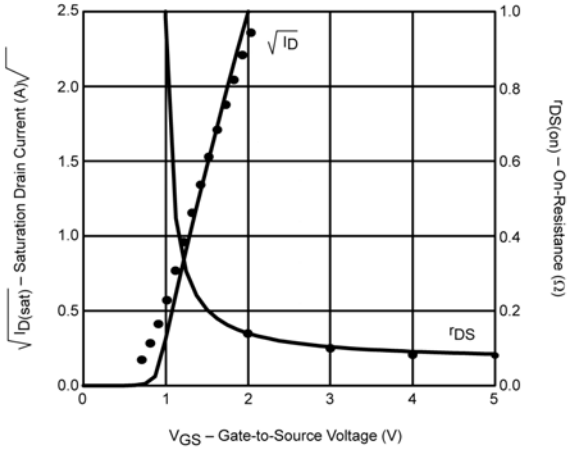



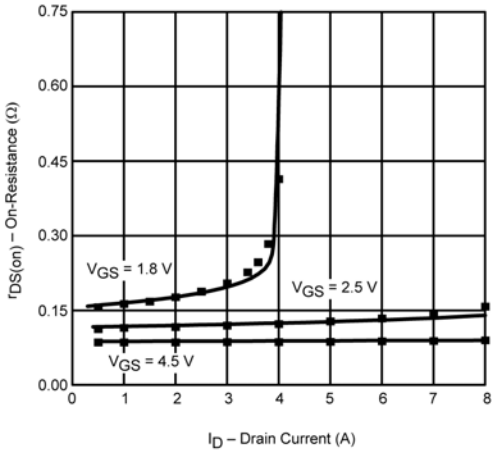

Note: Dots and squares represent measured data.

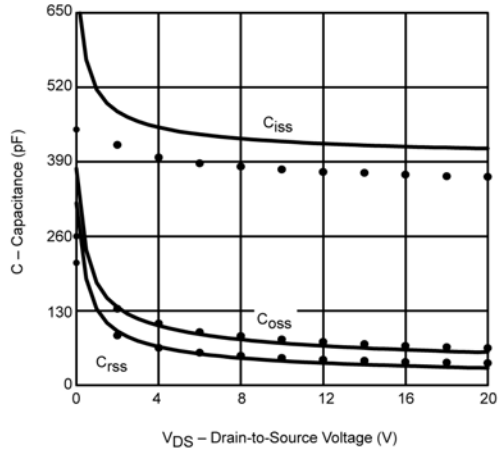
**P-Channel MOSFET**

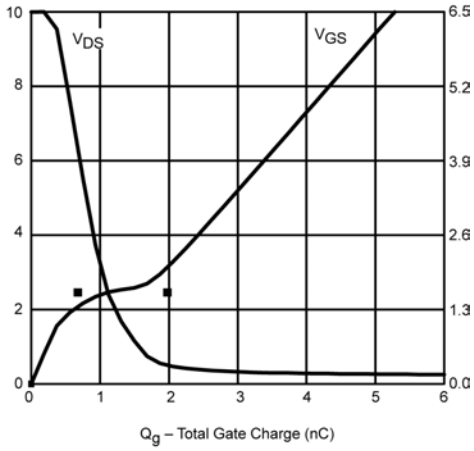



Note: Dots and squares represent measured data.