19-5918; Rev 0; 6/11

High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

General Description

The MAX15109 high-efficiency, current-mode, synchronous step-down switching regulator with integrated power switches deliver up to 8A of output current. This regulator operates from 2.7V to 5.5V and provides four output voltages using two VID control inputs.

This IC utilizes a current-mode control architecture with a high gain transconductance error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients.

This regulator offers skip-mode functionality to reduce current consumption and achieve a higher efficiency at light loads. The low $R_{DS(ON)}$ integrated switches ensure high efficiency at heavy loads while minimizing critical inductance, making the layout design a much simpler task with respect to discrete solutions. The high switching frequency (1MHz), along with the PWM current-mode architecture allows for a compact, all-ceramic capacitor design.

The IC features a capacitor-programmable slew-rate control to reduce input current at the startup and when the output changes state under VID control. Internal control circuitry ensures safe-startup into a prebiased output. Power sequencing is controlled with the enable input and power-good output.

The IC is available in a 20-bump (4 x 5 array), 2.5mm x 2mm, WLP package and is fully specified over the -40°C to +85°C temperature range.

Applications

Distributed Power Systems

DDR Memory

Notebook Power

Features

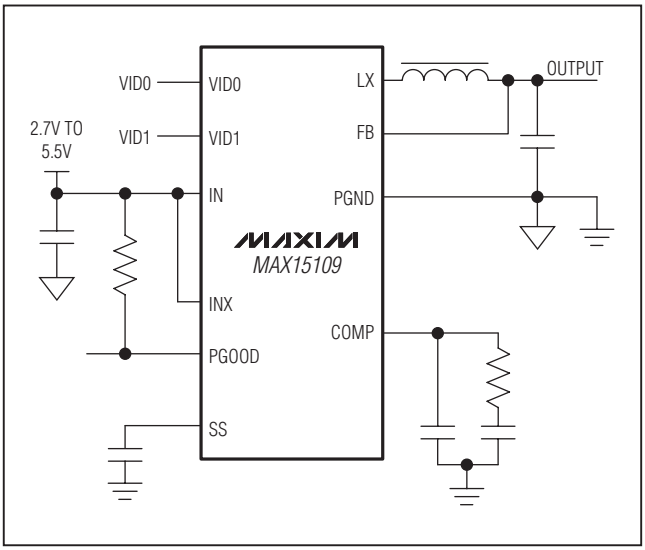
- **Continuous 8A Output Current**
- **Efficiency Over 90%**
- **±1% Accuracy Over Load, Line, and Temperature**
- **Operates from a 2.7V to 5.5V Supply**
- **VID Control Inputs for Selecting Output Voltage**
- **Programmable Slew-Rate Control**
- **Safe Startup into Prebiased Output**
- **1MHz Switching Frequency**
- **Stable with Low-ESR Ceramic Output Capacitors**
- **Enable Input and Power-Good Output for Power-Supply Sequencing**
- **Cycle-by-Cycle Overcurrent Protection Faults**
- **Fully Protected Against Overcurrent and Overtemperature**
- **Input Undervoltage Lockout**
- **20-Bump (4 x 5 Array), 2.5mm x 2mm, WLP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15109EWP+	-40°C to +85°C	20 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

ABSOLUTE MAXIMUM RATINGS

IN, PGOOD to PGND .....-0.3V to +6V
LX to PGND .....-0.3V to (V_{IN} + 0.3V)
LX to PGND .....-1V to (V_{IN} + 0.3V) for 50ns
EN, COMP, FB, SS, VID0, VID1 to PGND.....-0.3V to (V_{IN} + 0.3V)
LX Current (Note 1) ..... -12A to +12A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 21.3mW/°C above T_A = +70°C).....745.5mW
Operating Temperature Range ..... -40°C to +85°C
Operating Junction Temperature (Note 2).....+105°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) (Note 3) .....+260°C

Note 1: LX has internal clamp diodes to PGND and IN. Do not exceed the power dissipation limits of the device when forward biasing these diodes.

Note 2: Limit the junction temperature to +105°C for continuous operation at full current.

Note 3: The WLP package is constructed using a unique set of package techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, C_{SS} = 4.7nF, T_A = T_J = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		2.7		5.5	V
IN Shutdown Supply Current		V_{EN} = 0V		0.3	3	µA
IN Supply Current	I_{IN}	V_{EN} = 5V, V_{FB} = 1V, not switching		3.4	6	mA
V_{IN} Undervoltage Lockout Threshold		LX starts switching, V_{IN} rising		2.6	2.7	V
V_{IN} Undervoltage Lockout Hysteresis		LX stops switching, V_{IN} falling		200		mV
ERROR AMPLIFIER						
Transconductance	g_{MV}			1.4		mS
Voltage Gain	A_{VEA}			90		dB
Output Voltage Accuracy	V_{FB}	Over line, load, and temperature	-1		+1	%
FB Input Bias Current	I_{FB}		-100		+100	nA
COMP to Current-Sense Transconductance	G_{MOD}			25		A/V
COMP Clamp Low		V_{FB} = 0.68V		0.93		V
Compensation RAMP Valley				1		V
POWER SWITCHES						
High-Side Switch Current-Limit Threshold	I_{HSCL}			14		A
Low-Side Switch Sink Current-Limit Threshold				14		A
Low-Side Switch Source Current-Limit Threshold				14		A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, C_{SS} = 4.7nF, T_A = T_J = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
LX Leakage Current		V_{EN} = 0V					10	µA
RMS LX Output Current					8			A
OSCILLATOR								
Switching Frequency	f_{SW}				850	1000	1150	kHz
Maximum Duty Cycle	D_{MAX}					94		%
Minimum Controllable On-Time						100		ns
ENABLE								
EN Input High Threshold Voltage		V_{EN} rising			1.3			V
EN Input Low Threshold Voltage		V_{EN} falling					0.4	V
EN Input Leakage Current		V_{EN} = 5V					1	µA
VID CONTROL INPUTS								
VID_ High Threshold Voltage		$V_{VID_}$ rising			0.67			V
VID_ Low Threshold Voltage		$V_{VID_}$ falling					0.33	V
VID1 Input Leakage Current		V_{VID1} = 5V					30	µA
VID0 Input Leakage Current		V_{VID0} = 5V					1	µA
SOFT-START, PREBIAS								
Soft-Start Current	I_{SS}	V_{SS} = 0.45V, sourcing				10		µA
SS Discharge Resistance	R_{SS}	I_{SS} = 10mA, sinking				8.5		Ω
SS Prebias Mode Stop Voltage		SS rising				0.58		V
HICCUP								
Number of Consecutive Current-Limit Events to Hiccup						8		Events
Timeout						1024		Clock Cycles
POWER-GOOD OUTPUT								
PGOOD Threshold	PGT	FB rising	VID0	VID1				mV
			0	0	824	853	884	
			0	1	705	729	755	
			1	0	654	677	701	
			1	1	580	602	624	
		FB falling			559	578	600	mV
PGOOD V_{OL}		I_{PGOOD} = 5mA, V_{FB} = 0.5V				22	100	mV
PGOOD Leakage		V_{PGOOD} = 5V, V_{FB} = 0.68V					1	µA
THERMAL SHUTDOWN								
Thermal Shutdown Threshold						+160		°C
Thermal Shutdown Hysteresis		Temperature falling				25		°C

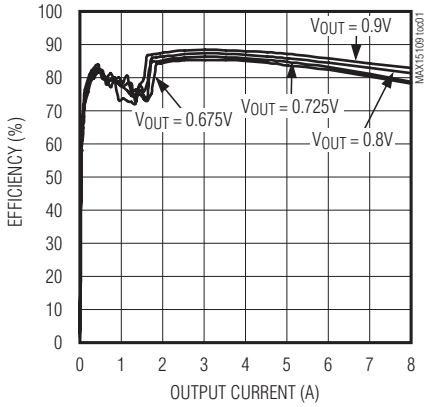
Note 4: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

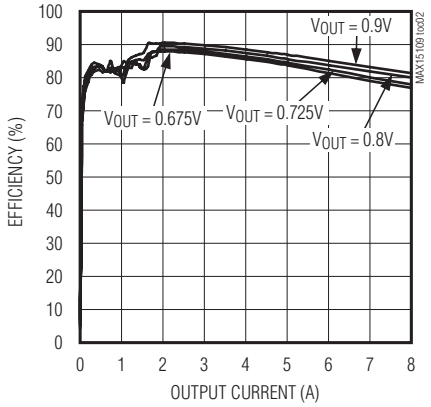
Typical Operating Characteristics

(Circuit of *Typical Application Circuit*, T_A = +25°C, unless otherwise noted.)

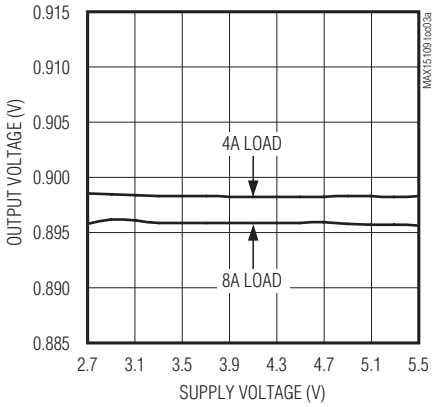
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 5V)



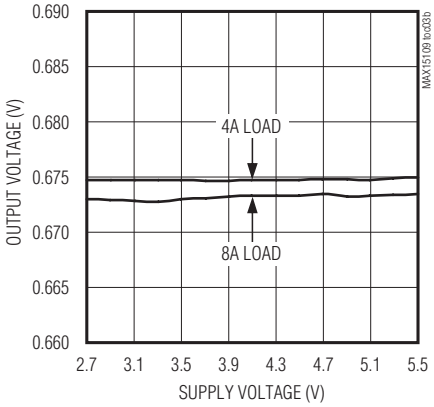
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 3.3V)



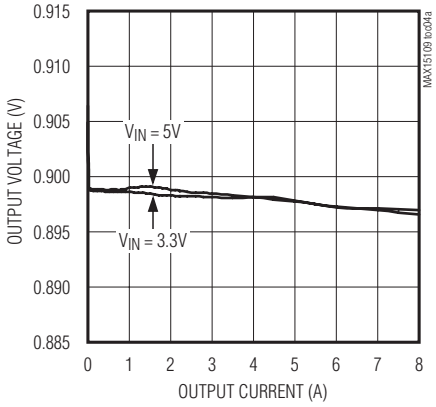
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (V_{OUT} = 0.9V)



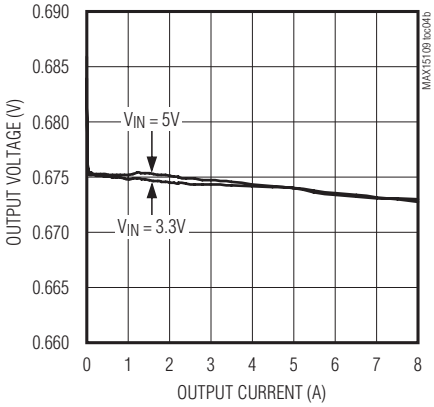
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (V_{OUT} = 0.675V)



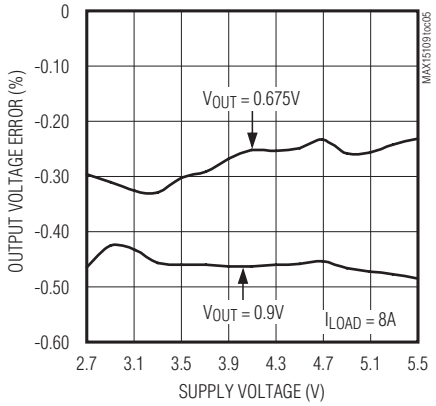
OUTPUT VOLTAGE vs. OUTPUT CURRENT (V_{OUT} = 0.9V)



OUTPUT VOLTAGE vs. OUTPUT CURRENT (V_{OUT} = 0.675V)



OUTPUT VOLTAGE ERROR vs. SUPPLY VOLTAGE

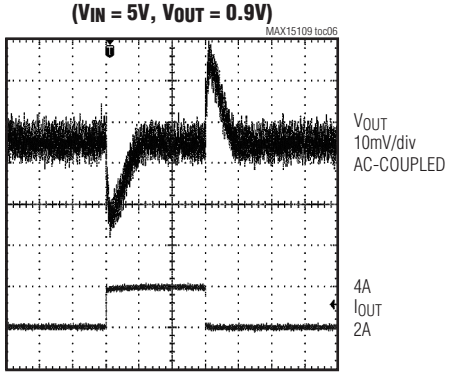


High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

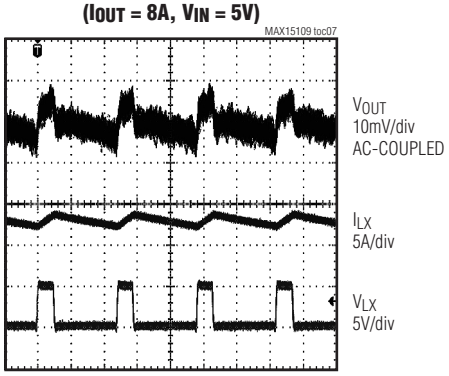
Typical Operating Characteristics (continued)

(Circuit of *Typical Application Circuit*, T_A = +25°C, unless otherwise noted.)

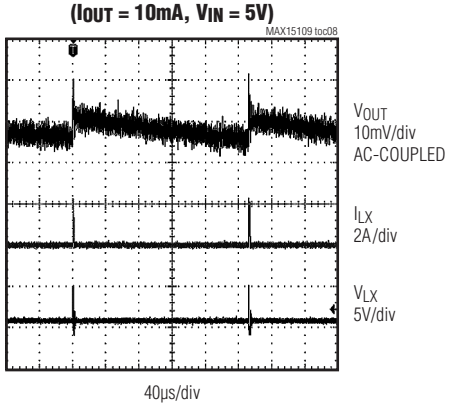
LOAD-TRANSIENT RESPONSE
(V_{IN} = 5V, V_{OUT} = 0.9V)



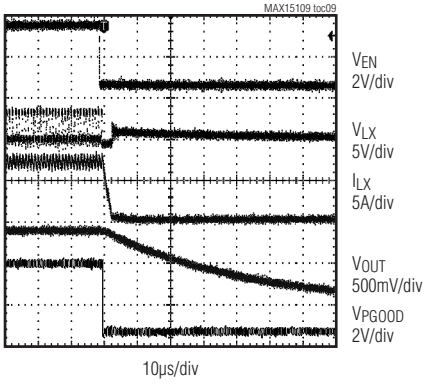
SWITCHING WAVEFORMS
(I_{OUT} = 8A, V_{IN} = 5V)



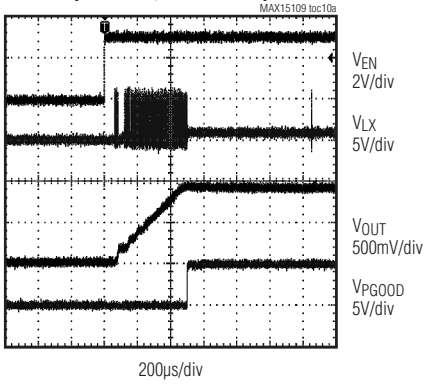
SWITCHING WAVEFORM IN SKIP MODE
(I_{OUT} = 10mA, V_{IN} = 5V)



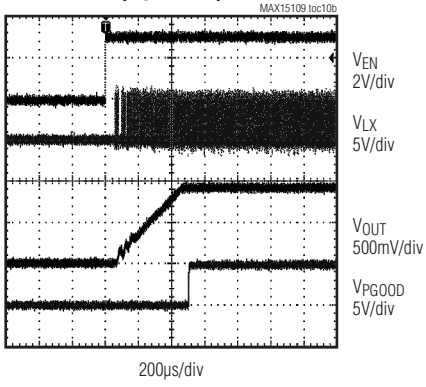
SHUTDOWN WAVEFORM
(I_{LOAD} = 8A)



SOFT-START WAVEFORMS
(NO LOAD, SKIP MODE)



SOFT-START WAVEFORMS
(I_{LOAD} = 8A)

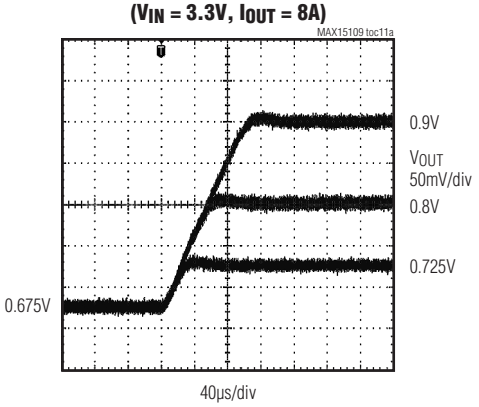


High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

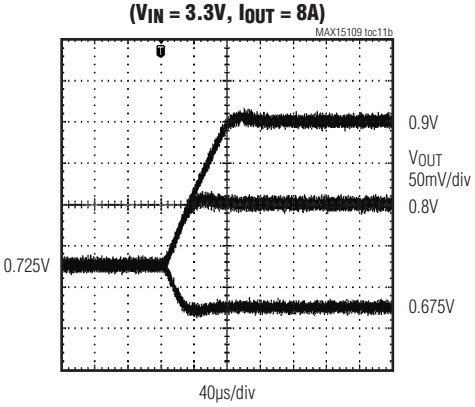
Typical Operating Characteristics

(Circuit of *Typical Application Circuit*, T_A = +25°C, unless otherwise noted.)

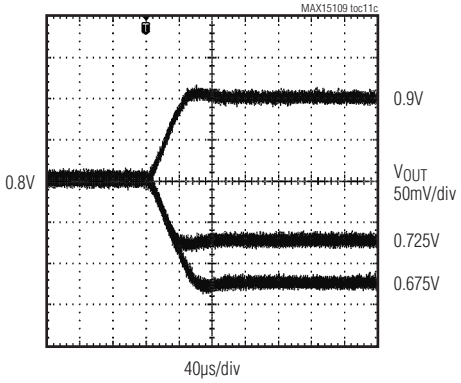
0.675V VID TRANSITIONS
(V_{IN} = 3.3V, I_{OUT} = 8A)



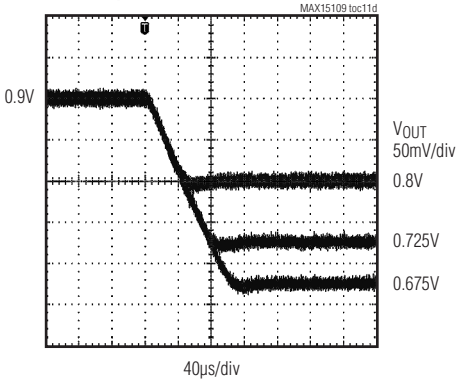
0.725V VID TRANSITIONS
(V_{IN} = 3.3V, I_{OUT} = 8A)



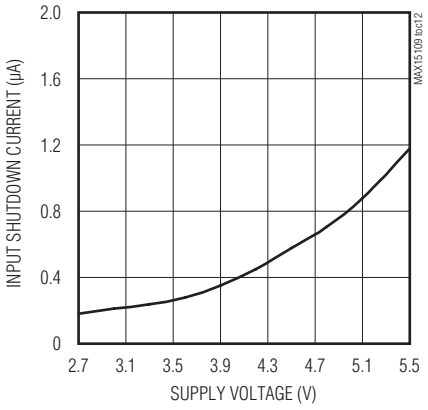
0.8V VID TRANSITIONS
(V_{IN} = 3.3V, I_{OUT} = 8A)



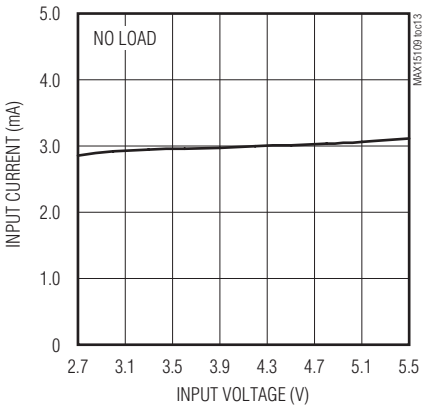
0.9V VID TRANSITIONS
(V_{IN} = 3.3V, I_{OUT} = 8A)



INPUT SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



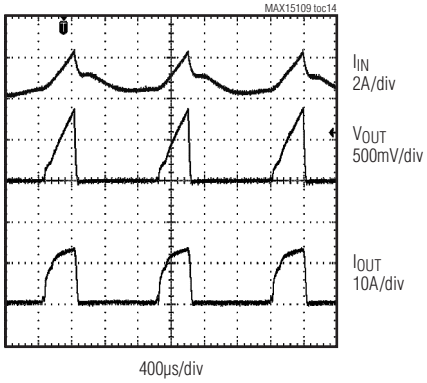
INPUT CURRENT vs. INPUT VOLTAGE



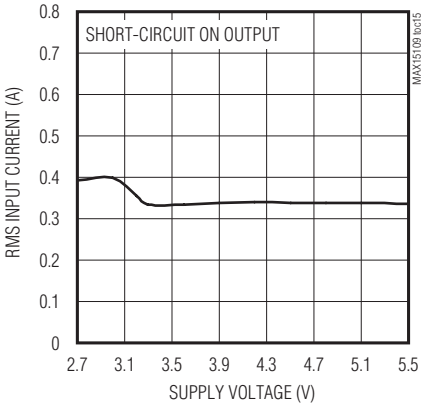
Typical Operating Characteristics (continued)

(Circuit of *Typical Application Circuit*, T_A = +25°C, unless otherwise noted.)

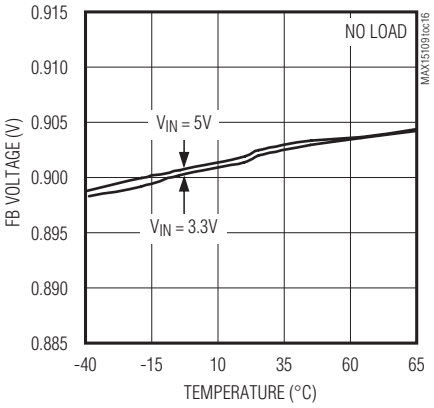
SHORT-CIRCUIT HICCUP MODE



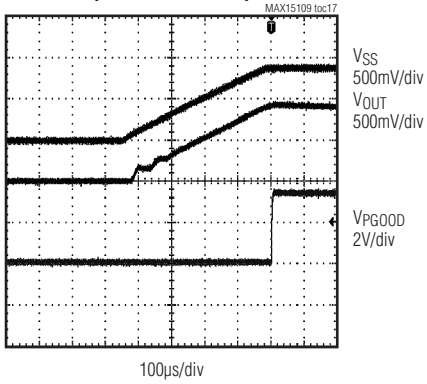
RMS INPUT CURRENT vs. SUPPLY VOLTAGE



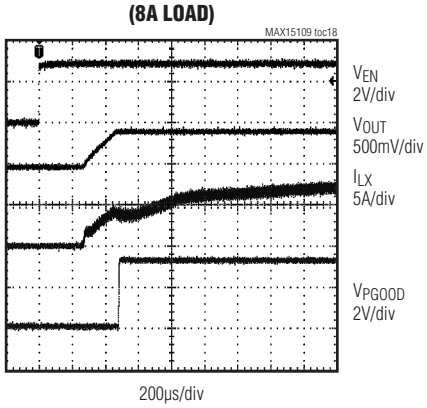
FB VOLTAGE vs. TEMPERATURE (VOUT = 0.9V)



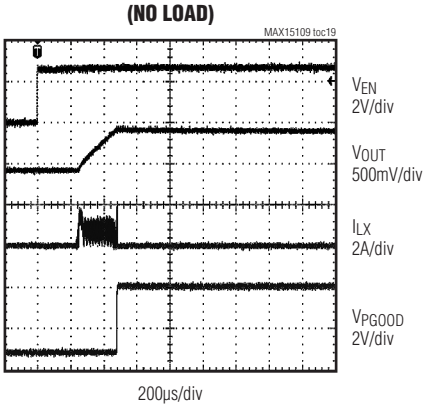
SOFT-START WAVEFORMS (EXTERNAL REFIN)



ENABLE INTO PREBIASED 0.5V OUTPUT (8A LOAD)

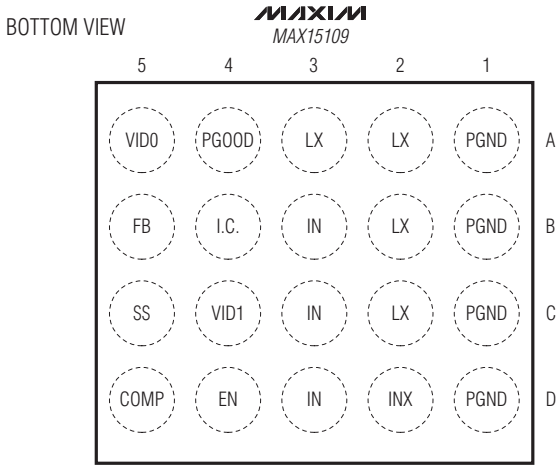


ENABLE INTO PREBIASED 0.5V OUTPUT (NO LOAD)



High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

Pin Configuration



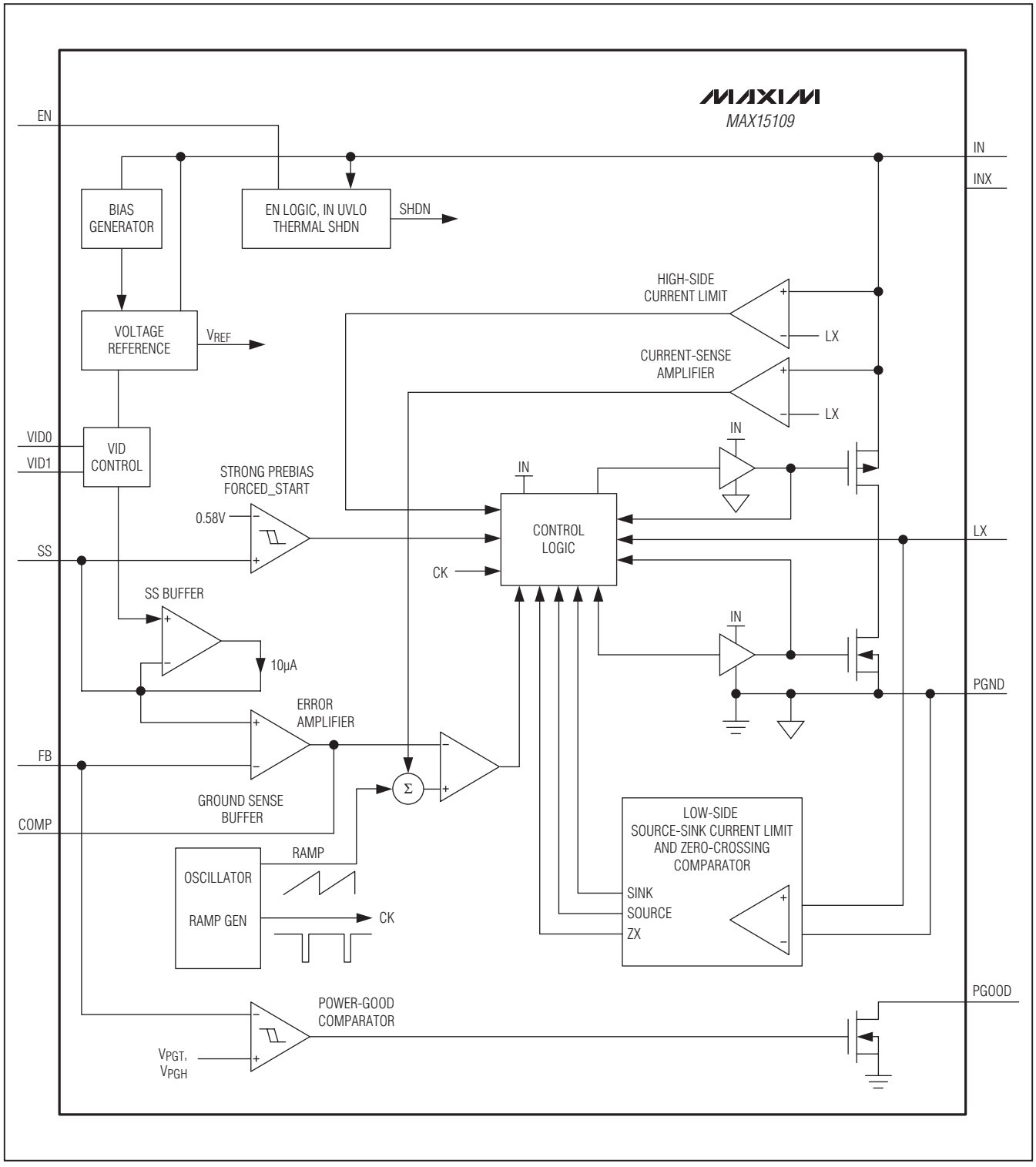
WLP

Pin Description

BUMP	NAME	FUNCTION
A1, B1, C1, D1	PGND	Power Ground. Low-side switch source terminal. Connect PGND and the return terminals of input and output capacitors to the power ground plane.
A2, A3, B2, C2	LX	Inductor Connection. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode.
A4	PGOOD	Open-Drain Power-Good Output. PGOOD goes low when V_{FB} is below the PGOOD threshold.
A5	VID0	VID0 Logic Input. Use VID0 and VID1 to select output voltage.
B3, C3, D3	IN	Input Power Supply. Input supply range is 2.7V to 5.5V. Bypass IN with a minimum 10µF ceramic capacitor to PGND. See the *Typical Application Circuit*.
B4	I.C.	Internally Connected. Leave unconnected.
B5	FB	Feedback Input. Connect FB to the sense the output voltage.
C4	VID1	VID1 Logic Input. Use VID0 and VID1 to select output voltage.
C5	SS	Soft-Start and VID Transition Timing Control. Connect a capacitor from SS to PGND to set the startup time and the output voltage transition timing. See the *Output Voltage Transition Timing* section for details.
D2	INX	Internally Unconnected. INX is not internally connected to IN. However, do externally connect INX to IN to increase the area of the power plane for optimal heat dissipation.
D4	EN	Enable Input. EN is a digital input that turns the regulator on and off. Drive EN high to turn on the regulator. Connect to IN for always-on operation.
D5	COMP	Error Amplifier Output. Connect compensation network from COMP to signal ground (SGND). See the *Compensation Design Guidelines* section.

High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

Functional Diagram



High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

Detailed Description

The MAX15109 high-efficiency, current-mode switching regulator delivers up to 8A of output current. The regulator operates from 2.7V to 5.5V and provides a VID selectable output.

The IC current-mode control architecture uses a high gain transconductance error amplifier that facilitates an easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients.

The regulator features a 1MHz fixed switching frequency, allowing for all-ceramic capacitor designs with fast transient responses. The high operating frequency minimizes the size of external components. The IC is available in a 2.5mm x 2mm (4 x 5 array), 0.5mm pitch WLP package.

The regulator offers skip-mode functionality to reduce current consumption and achieve a high efficiency at light output loads. The low $R_{DS(ON)}$ integrated switches ensure high efficiency at heavy loads while minimizing critical inductance, making the layout design a much simpler task than that of discrete solutions. The IC's simple layout and footprint assure first-pass success in new designs.

The IC has output voltages of 0.9V, 0.8V, 0.725V, and 0.625V by configuring the VID inputs. The regulator offers capacitor-programmable soft-start to reduce input inrush current. The device safely starts up into a prebiased output. The IC includes an enable input and open-drain PGOOD output for sequencing with other devices.

Controller Function—PWM Logic

The controller logic block determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator to generate the driver signals for both high-side and low-side MOSFETs. The control logic block controls the break-before-make logic and all the necessary timing.

The high-side MOSFET turns on at the beginning of the oscillator cycle and turns off when the COMP voltage crosses the internal current-mode ramp waveform. The internal ramp is the sum of the compensation ramp and the current-mode ramp. The high-side MOSFET also turns off if the maximum duty cycle exceeds 95%, or when the current limit is reached. The low-side MOSFET turns on for the remainder of the switching cycle.

Starting into a Prebiased Output

The IC can soft-start into a prebiased output without discharging the output capacitor. In safe prebiased startup, both low-side and high-side MOSFETs remain off to avoid discharging the prebiased output. PWM operation starts when the voltage on SS crosses the voltage on FB.

The IC can start into a prebiased voltage higher than the nominal set point without abruptly discharging the output. Forced PWM operation starts when the SS voltage reaches 0.58V, forcing the converter to start. When the low-side sink current-limit threshold of 14A is reached, the low-side switch turns off before the end of the clock period. The low-side sink current limit is 14A. The high-side switch turns on until one of the following conditions is satisfied:

- High-side source current hits the reduced high-side current limit (14A). The high-side switch turns off for the remaining time of clock period.
- The clock period ends.

Reduced high-side current limit is activated in order to recirculate the current into the high-side power switch rather than into the internal high-side body diode, which can cause damage to the devices. The high-side current limit is set to 14A.

Low-side sink current limit protects the low-side switch from excessive reverse current during prebiased operation.

Enable Input

The IC features independent device enable control and power-good signal that allow for flexible power sequencing. Drive the enable input (EN) high to enable the regulator, or connect EN to IN for always-on operation. Power-good (PGOOD) is an open-drain output that goes high when V_{FB} is above the PGOOD threshold, and goes low if V_{FB} is below the PGOOD threshold.

Programmable Soft-Start (SS)

The IC utilizes a soft-start feature to slowly ramp up the regulated output voltage to reduce input inrush current during startup. Connect a capacitor from SS to PGND to set the startup time. See the *Output Voltage Transition Timing* section for capacitor selection details.

Error Amplifier

A high-gain error amplifier provides accuracy for the voltage feedback loop regulation. Connect a compensation network between COMP and SGND. See the *Compensation Design Guidelines* section. The error amplifier transconductance is 1.4mS. COMP clamp low is set to 0.8V, just below the PWM ramp compensation valley, helping COMP to rapidly return to the correct set point during load and line transients.

PWM Comparator

The PWM comparator compares COMP voltage to the current-derived ramp waveform (LX current to COMP voltage transconductance value is 25A/V). To avoid instability due to subharmonic oscillations when the duty cycle is around 50% or higher, a compensation ramp is added to the current-derived ramp waveform. The compensation ramp slope (0.3V x 1MHz = 0.3V/µs) is equivalent to half of the inductor current down-slope in the worst case (load 2A, current ripple 30% and maximum duty-cycle operation of 95%). The compensation ramp valley is set to 1V.

Overcurrent Protection and Hiccup

When the converter output is connected to ground or the device is overloaded, each high-side MOSFET current-limit event (14A) turns off the high-side MOSFET and turns on the low-side MOSFET. A 3-bit counter increments on each current-limit event. The counter is reset after three consecutive events of high-side MOSFET turn-on without reaching the current limit. If the current-limit condition persists, the counter fills up reaching eight events. The control logic then discharges SS, stops both high-side and low-side MOSFETs and waits for a hiccup period (1024 clock cycles) before attempting a new soft-start sequence. The hiccup-mode also operates during soft-start.

Thermal Shutdown Protection

The IC contains an internal thermal sensor that limits the total power dissipation to protect it in the event of an extended thermal fault condition. When the die temperature exceeds +160°C, the thermal sensor shuts down the device, turning off the DC-DC converter to allow the die to cool. After the die temperature falls by 25°C, the device restarts, following the soft-start sequence.

Skip Mode Operation

The IC operates in skip mode. When in skip mode, LX output becomes high impedance when the inductor current falls below 0.7A. The inductor current does not become negative. During a clock cycle, if the inductor current falls below the 0.7A threshold (during off-time), the low side turns off. At the next clock cycle, if the output voltage is above the set point the PWM logic keeps both high-side and low-side MOSFETs off. If instead the output voltage is below the set point, the PWM logic drives the high-side on for a minimum fixed on-time (330ns). In this way, the system skips cycles, reducing the frequency of operations, and switches only as needed to service load at the cost of an increase in output-voltage ripple. See the *Skip Mode Frequency and Output Ripple* section for details. In skip mode, power dissipation is reduced and efficiency improved at light loads because the internal power MOSFETs do not switch at every clock cycle.

High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

Applications Information

Setting the Output Voltage

The output voltage is selected by using the VID0 and VID1 control inputs. Table 1 summarizes the output voltages.

Table 1. Output Voltages

VID0	VID1	VOLTAGE (V)
0	0	0.9
0	1	0.8
1	0	0.725
1	1	0.675

Inductor Selection

A large inductor value results in reduced inductor ripple current, leading to a reduced output ripple voltage. A high-value inductor is of a larger physical size with a higher series resistance (DCR) and a lower saturation current rating. Choose inductor values to produce a ripple current equal to 30% of the load current. Choose the inductor with the following formula:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f_{SW} is the internally fixed 1MHz switching frequency, and ΔI_L is the estimated inductor ripple current (typically set to 0.3 x I_{LOAD}). In addition, the peak inductor current, I_{L_PK}, must always be below the high-side current-limit value, I_{HSCL}, and the inductor saturation current rating, I_{L_SAT}.

Ensure that the following relationship is satisfied:

$$I_{L_PK} = I_{LOAD} + \frac{1}{2} \times \Delta I_L < MIN(I_{HSCL}, I_{L_SAT})$$

Input Capacitor Selection

For a step-down converter, the input capacitor C_{IN} helps to keep the DC input voltage steady, in spite of discontinuous input AC current. Use low-ESR capacitors to minimize the voltage ripple due to ESR.

Size C_{IN} using the following formula:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \times \Delta V_{IN_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}}$$

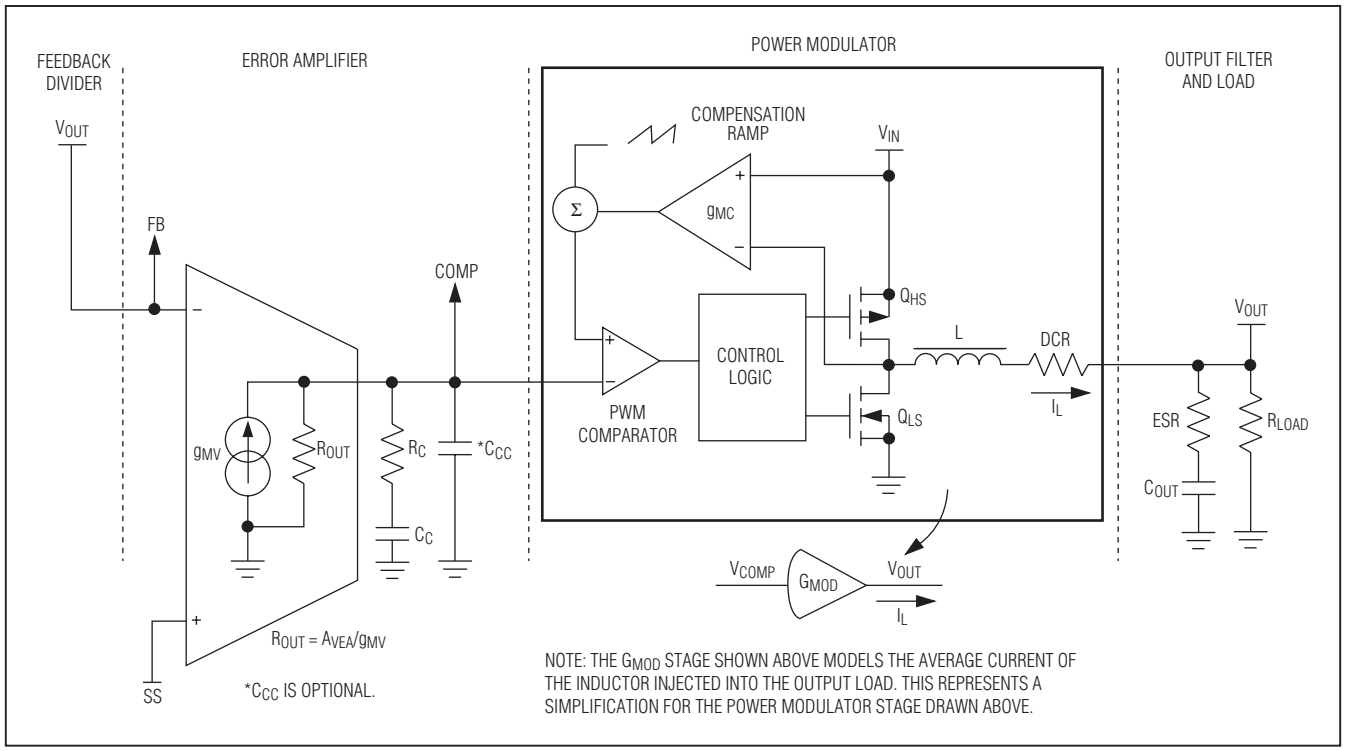


Figure 1. Peak Current-Mode Regulator Transfer Model

High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

Make sure that the selected capacitance can accommodate the input ripple current given by:

$$I_{RMS} = I_O \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

If necessary, use multiple capacitors in parallel to meet the RMS current rating requirement.

Output Capacitor Selection

Use low-ESR ceramic capacitors to minimize the voltage ripple due to ESR. Use the following formula to estimate the total output voltage peak-to-peak ripple:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR_COUT} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

Select the output capacitors to produce an output ripple voltage that is less than 2% of the set output voltage.

Output Voltage Transition Timing

The IC features programmable output voltage transition timing control. The regulator tracks the voltage on the SS pin that is set with a current-limited (10µA) VID DAC. A small capacitor at SS can therefore be used to set the transition timing for startup and VID transitions.

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V_{OUT}}$$

where I_{SS} is the soft-start current of 10µA, ΔV_{OUT} is the output-voltage transition, and Δt is the transition time. When using large C_{OUT} capacitance values, the high-side current limit can trigger during the soft-start period. To ensure the correct soft-start time, t_{SS}, choose C_{SS} large enough to satisfy:

$$C_{SS} >> C_{OUT} = \frac{V_{OUT} \times I_{SS}}{(I_{HSCL_MIN} - I_{OUT}) \times V_{FB}}$$

I_{HSCL_MIN} is the minimum high-side switch current-limit value.

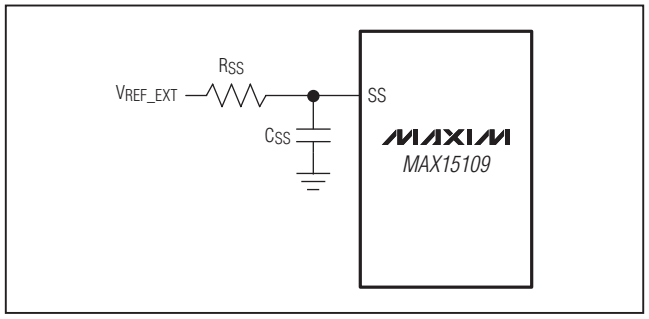


Figure 2. Setting Soft-Start Time

Skip Mode Frequency and Output Ripple

In skip mode, the switching frequency (f_{SKIP}) and output ripple voltage ($V_{OUT-RIPPLE}$) shown in Figure 3 are calculated as follows:

t_{ON} is a fixed time by design (330ns, typ); the peak inductor current reached is:

$$I_{SKIP-LIMIT} = \frac{V_{IN} - V_{OUT}}{2AV} \times t_{ON}$$

t_{OFF1} is the time needed for the inductor current to reach the zero-crossing (~0A):

$$t_{OFF1} = \frac{L \times I_{SKIP-LIMIT}}{V_{OUT}}$$

During t_{ON} and t_{OFF1}, the output capacitor stores a charge equal to:

$$\Delta Q_{OUT} = \frac{L \times (I_{SKIP-LIMIT} - I_{LOAD})^2 \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)}{2}$$

During t_{OFF2} (= n x t_{CK}, number of clock cycles skipped), the output capacitor loses this charge:

$$t_{OFF2} = \frac{\Delta Q_{OUT}}{I_{LOAD}} \rightarrow$$

$$t_{OFF2} = \frac{L \times (I_{SKIP-LIMIT} - I_{LOAD})^2 \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)}{2 \times I_{LOAD}}$$

Finally, frequency in skip mode is:

$$f_{SKIP} = \frac{1}{t_{ON} + t_{OFF1} + t_{OFF2}}$$

Output ripple in skip mode is:

$$V_{OUT-RIPPLE} = V_{COUT-RIPPLE} + V_{ESR-RIPPLE} =$$

$$\frac{(I_{SKIP-LIMIT} - I_{LOAD}) \times t_{ON}}{C_{OUT}} + R_{ESR,COUT} \times (I_{SKIP-LIMIT} - I_{LOAD})$$

$$V_{OUT-RIPPLE} =$$

$$\left[\frac{L \times I_{SKIP-LIMIT}}{C_{OUT} \times (V_{IN} - V_{OUT})} + R_{ESR,COUT}\right] \times (I_{SKIP-LIMIT} - I_{LOAD})$$

Size C_{OUT} based on the above formula to limit output ripple in skip mode.

High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

Compensation Design Guidelines

The IC uses a fixed-frequency, peak-current-mode control scheme to provide easy compensation and fast transient response. The inductor peak current is monitored on a cycle-by-cycle basis and compared to the COMP voltage (output of the voltage error amplifier). The regulator's duty cycle is modulated based on the inductor's peak current value. This cycle-by-cycle control of the inductor current emulates a controlled current source. As a result, the inductor's pole frequency is shifted beyond the gain bandwidth of the regulator. System stability is provided with the addition of a simple series capacitor-resistor from COMP to PGND. This pole-zero combination serves to tailor the desired response of the closed-loop system. The basic regulator loop consists of a power modulator (comprising the regulator's pulse-width modulator, compensation ramp, control circuitry, MOSFETs, and inductor), the capacitive output filter and load, an output feedback, and a voltage-loop error amplifier with its associated compensation circuitry. See Figure 1.

The average current through the inductor is expressed as:

$$\overline{I_L} = G_{MOD} \times \overline{V_{COMP}}$$

where $\overline{I_L}$ is the average inductor current and G_{MOD} is the power modulator's transconductance.

For a buck converter:

$$\overline{V_{OUT}} = R_{LOAD} \times \overline{I_L}$$

where R_{LOAD} is the equivalent load resistor value. Combining the above two relationships, the power modulator's transfer function in terms of $\overline{V_{OUT}}$ with respect to $\overline{V_{COMP}}$ is:

$$\frac{\overline{V_{FB}}}{\overline{V_{COMP}}} = \frac{R_{LOAD} \times \overline{I_L}}{\frac{\overline{I_L}}{G_{MOD}}} = R_{LOAD} \times G_{MOD}$$

Having defined the power modulator's transfer function gain, the total system loop gain can be written as follows (see Figure 1):

$$\alpha = \frac{R_{OUT} \times (sC_CR_C + 1)}{\left[s(C_C + C_{CC})(R_C + R_{OUT}) + 1\right] \times \left[s(C_C \parallel C_{CC})(R_C \parallel R_{OUT}) + 1\right]}$$

$$\beta = G_{MOD} \times R_{LOAD} \times \frac{(sC_{OUT}ESR + 1)}{\left[sC_{OUT}(ESR + R_{LOAD}) + 1\right]}$$

$$Gain = \frac{R_2}{R_1 + R_2} \times \frac{A_{VEA}}{R_{OUT}} \times \alpha \times \beta$$

where R_{OUT} is the quotient of the error amplifier's DC gain, A_{VEA}, divided by the error amplifier's transconductance, g_{MV}; R_{OUT} is much larger than R_C.

$$\frac{R_2}{R_1 + R_2} = \frac{V_{FB}}{V_{OUT}}$$

Also, C_C is much larger than C_{CC}, therefore:

$$C_C + C_{CC} \approx C_C$$

and

$$C_C \parallel C_{CC} \approx C_{CC}$$

Rewriting:

$$Gain = \frac{V_{FB}}{V_{OUT}} A_{VEA} \times \frac{(sC_CR_C + 1)}{\left[sC_C\left(\frac{A_{VEA}}{g_{MV}}\right) + 1\right] \times (sC_{CC}R_C + 1)} \times G_{MOD}\, R_{LOAD} \times \frac{(sC_{OUT}ESR + 1)}{\left[sC_{OUT}(ESR + R_{LOAD}) + 1\right]}$$

The dominant poles and zeros of the transfer loop gain are shown below:

$$f_{P1} = \frac{g_{MV}}{2\pi \times 10^{AVEA_dB/20} \times C_C}$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT}(ESR + R_{LOAD})}$$

$$f_{P3} = \frac{1}{2\pi \times C_{CC}R_C}$$

$$f_{Z1} = \frac{1}{2\pi \times C_CR_C}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{OUT}ESR}$$

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The order of pole-zero occurrence is:

$$f_{P1} < f_{P2} < f_{Z1} < f_{Z2} \le f_{P3}$$

Under heavy load, f_{P2}, approaches f_{Z1}. A graphical representation of the asymptotic system closed-loop response, including dominant pole and zero locations is shown in Figure 3.

If C_{OUT} is large, or exhibits a lossy equivalent series resistance (large ESR), the circuit's second zero might come into play around the crossover frequency ($f_{CO} = \omega/2\pi$). In this case, a third pole can be induced by a second (optional) small compensation capacitor (C_{CC}), connected from COMP to PGND. The loop response's fourth asymptote (in bold, Figure 4) is the one of interest in establishing the desired crossover frequency (and determining the compensation component values). A lower crossover frequency provides for stable closed-loop operation at the expense of a slower load and line transient response. Increasing the crossover frequency improves the transient response at the (potential) cost of system instability. A standard rule of thumb sets the crossover frequency ≤ 1/10th of the switching frequency. First, select the passive and active power components that meet the application's requirements. Then, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined in the *Closing the Loop: Designing the Compensation Circuitry* section.

Closing the Loop: Designing the Compensation Circuitry

Select the desired crossover frequency. Choose f_{CO} approximately 1/10th of the switching frequency f_{SW}, or $f_{CO} \approx 100kHz$.

Select R_C using the transfer-loop's fourth asymptote gain (assuming $f_{CO} > f_{P1}$, f_{P2}, and f_{Z1} and setting the overall loop gain to unity) as follows:

$$1 = \frac{V_{FB}}{V_{OUT}} \times g_{MV} \times R_C \times G_{MOD} \times R_{LOAD} \times \frac{1}{2\pi \times f_{CO} \times C_{OUT} \times (ESR + R_{LOAD})}$$

therefore:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times f_{CO} \times C_{OUT} \times (ESR + R_{LOAD})}{g_{MV} \times G_{MOD} \times R_{LOAD}}$$

For R_{LOAD} much greater than ESR, the equation can be further simplified as follows:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times f_{CO} \times C_{OUT}}{g_{MV} \times G_{MOD}}$$

where V_{FB} is equal to 0.6V.

Determine C_C by selecting the desired first system zero, f_{Z1}, based on the desired phase margin. Typically, setting f_{Z1} below 1/5th of f_{CO} provides sufficient phase margin.

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C} \le \frac{f_{CO}}{5}$$

Therefore:

$$C_C \ge \frac{5}{2\pi \times f_{CO} \times R_C}$$

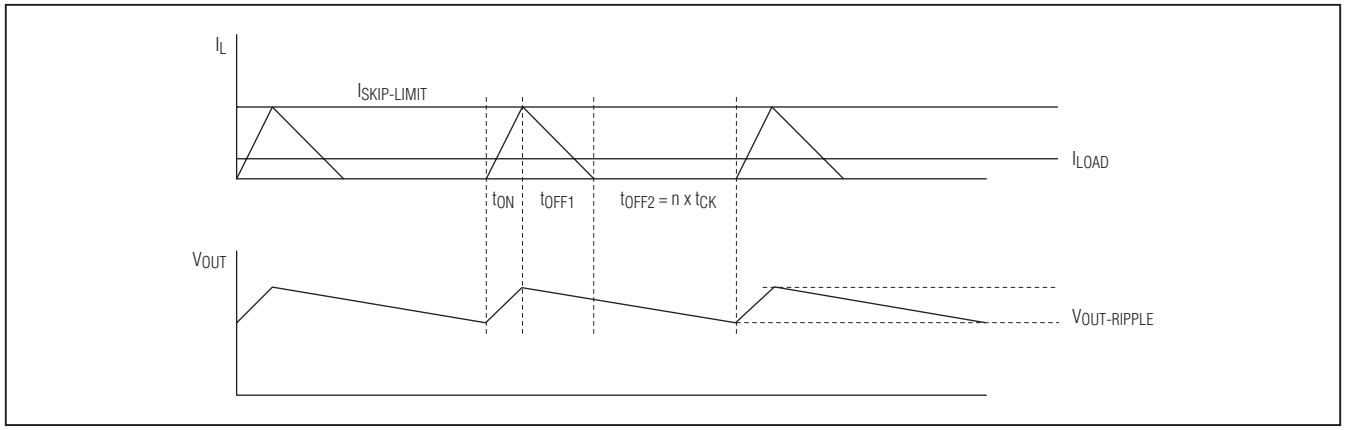


Figure 3. Skip-Mode Waveforms

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If the ESR output zero is located at less than one-half the switching frequency, use the (optional) secondary compensation capacitor, C_{CC}, to cancel it, as follows:

$$\frac{1}{2\pi \times C_{CC}R_C} = f_{P3} = f_{Z2} = \frac{1}{2\pi \times C_{OUT}ESR}$$

therefore:

$$C_{CC} = \frac{C_{OUT} \times ESR}{R_C}$$

If the ESR zero exceeds 1/2 the switching frequency, use the following equation:

$$f_{P3} = \frac{1}{2\pi \times C_{CC}R_C} = \frac{f_{SW}}{2}$$

therefore:

$$C_{CC} = \frac{2}{2\pi \times f_{SW} \times R_C}$$

Overall C_{CC} detracts from the overall system phase margin. Place this third pole well beyond the desired crossover frequency to minimize the interaction with the system loop response at crossover. Ignore C_{CC} in these calculations if C_{CC} is smaller than 10pF.

Power Dissipation

The IC is available in a 20-bump WLP package and can dissipate up to 745.5mW at T_A = +70°C. When the die temperature exceeds +160°C, the thermal-shutdown protection is activated. See the *Thermal Shutdown Protection* section.

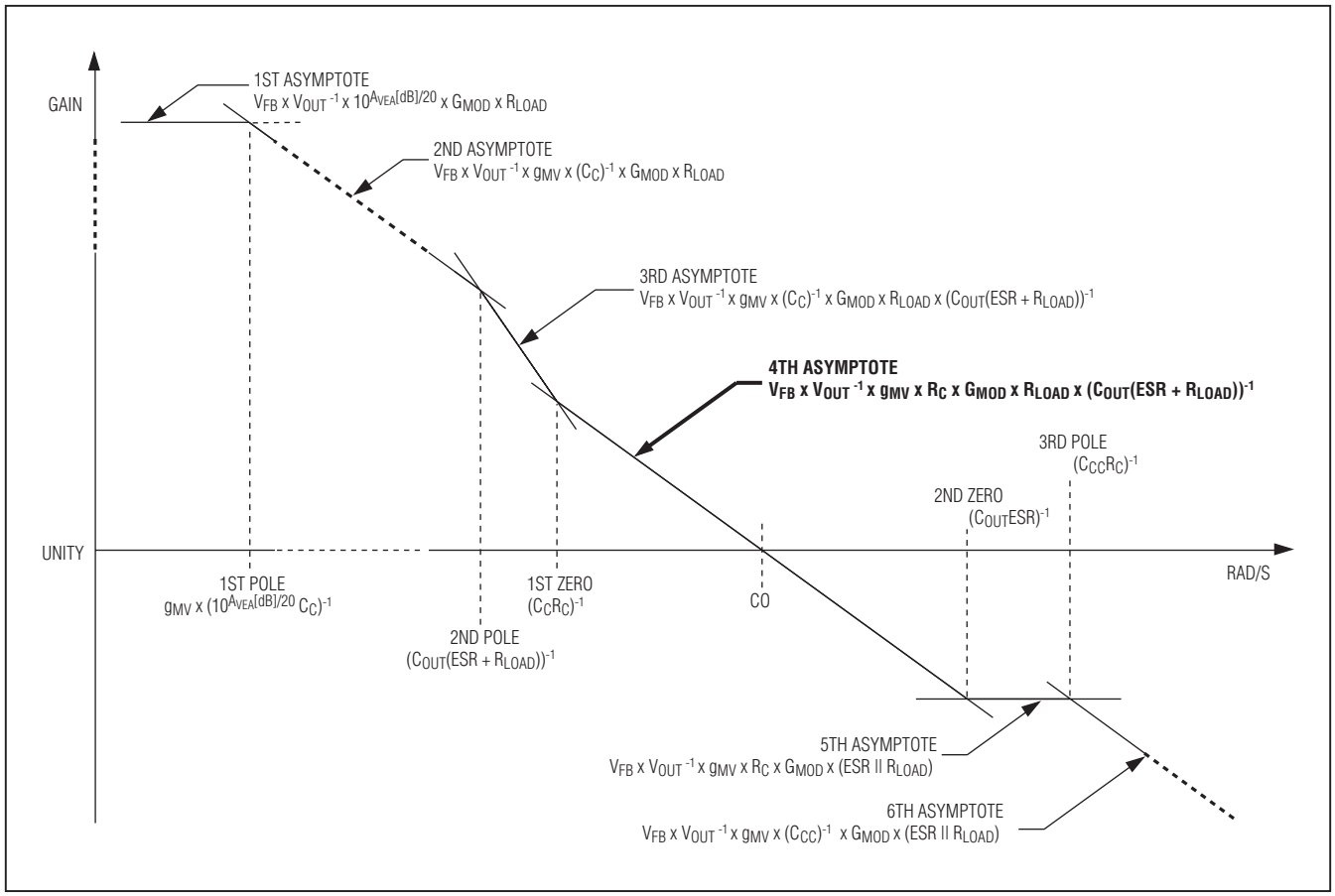


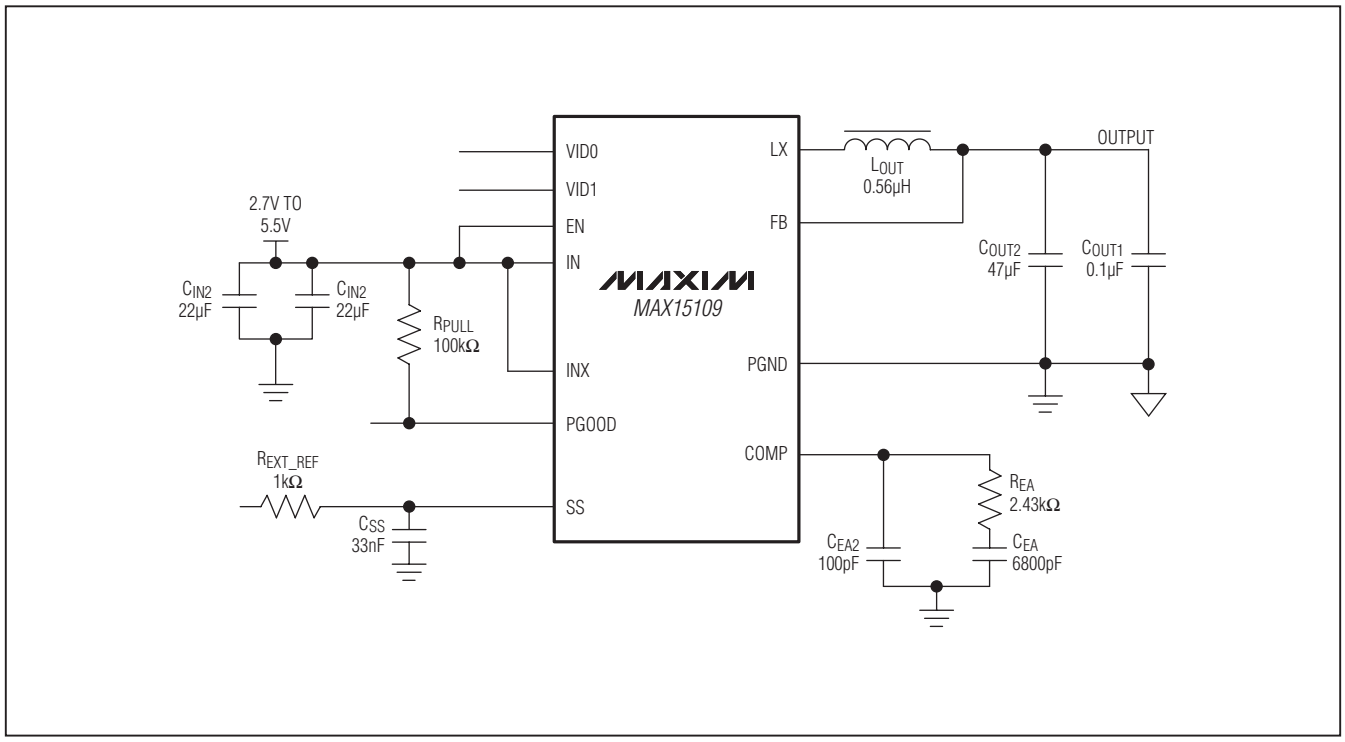
Figure 4. Asymptotic Loop Response of Peak Current-Mode Regulator

Layout Procedure

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15109 evaluation kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors to the power ground plane.
2) Place bypass capacitors as close to IN and the soft-start capacitor as close to SS as possible.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
6) Route high-speed switching nodes (such as LX) away from sensitive analog areas (such as FB, COMP, SGND, and SS).

Typical Application Circuit



High-Efficiency, 8A, Current-Mode Synchronous Step-Down Switching Regulator with VID Control

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 WLP	W202D2Z+1	21-0505	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—

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