

3V Self Recovering Watchdog

Description

The H6061 is a combined initialiser, watchdog and voltage monitor. The circuit is a low voltage low power monolithic CMOS device combining a series of voltage comparators and a programmable timer on the same chip. The device is specially suited to telecommunications applications where 3 V working is expected, for functions such as supply voltage and microprocessor monitoring. The reset outputs are self recovering after a watchdog timeout, enabling the circuit to work with standalone systems without any external push-switch or control signal to restart after a watchdog timeout. The circuit provides a reset signal of both polarities. The state of the outputs is defined down to 1.6 V. An internal debouncer ensures power-up performance for fast-rise supply lines.

Features

- ❑ Watchdog fully operational from 2.7 to 5.25 V
- ❑ Regulated DC voltage monitor, internal voltage reference
- ❑ Self recovering watchdog function: reset goes active after the 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- ❑ Standard timeout period and power-on reset time (100 ms), externally programmable from 3 ms to 3 mins if required
- ❑ Works down to 1.6 V supply voltage
- ❑ Low voltage alarm prior to reset on power-down
- ❑ Reset outputs of both polarities
- ❑ Open drain outputs
- ❑ SO8 package

Applications

- ❑ Microprocessor and microcontroller systems
- ❑ Point of sales equipment
- ❑ Telecom products
- ❑ Automotive subsystems
- ❑ Microcontroller 68HC05 applications

Typical Operating Configuration

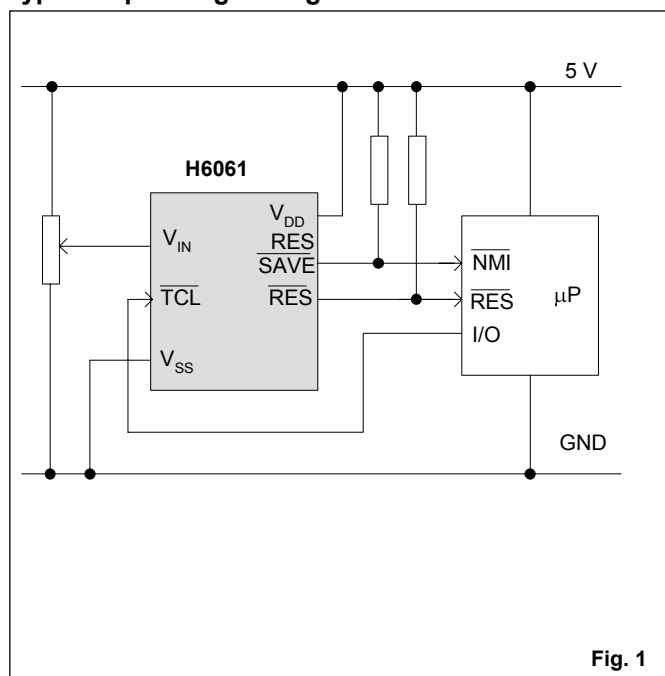


Fig. 1

Pin Assignment

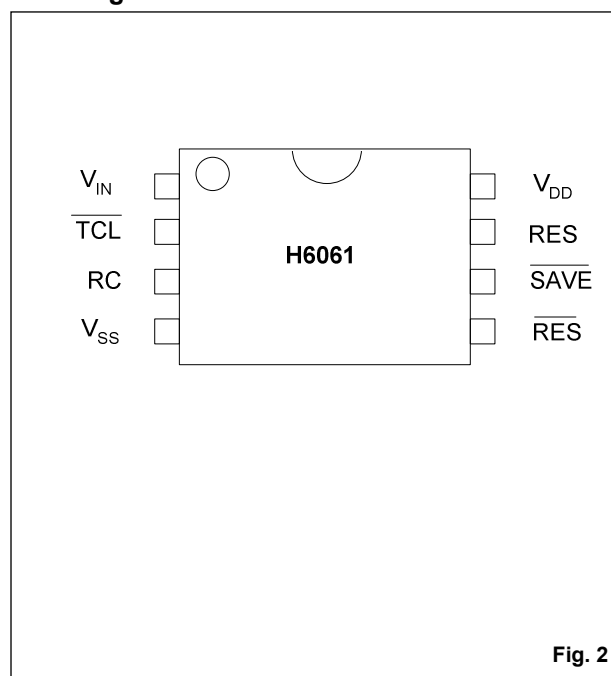


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{DD}	- 0.3 to + 5.6 V
Voltage at any pin to V_{SS}	V_{MIN}	- 0.3
Voltage at any pin to V_{DD}	V_{MAX}	+ 0.3
Voltage at V_{IN} to V_{SS}	V_{INMAX}	+ 12 V
Current at any output	I_{MAX}	± 10 mA
Storage temperature	T_{STO}	-65°C to +150°C
Electrostatic discharge max. to MIL-STD-883C method 3014	V_{Smax}	1000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating temperature Industrial	T_{AI}	-40	+85	°C
Supply voltage	V_{DD}	2.7	5.25	V
Version 11,12	V_{IN}	0	12	V
RC-oscillator programming				
External capacitance*	C1		1	μ F
External resistance	R1	10		k Ω

* Leakage < 1 μ A

Table 2

Electrical Characteristics

$V_{DD} = 5.0$ V, $T_A = -40$ to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
V_{DD} activation threshold	V_{ON}	$T_A = 25$ °C	2.3		2.7	V
V_{DD} deactivation threshold	V_{OFF}	$T_A = 25$ °C		$V_{ON}-0.3$		V
Supply current	I_{DD}	RC open, $\overline{TCL}$ at V_{DD} or V_{SS}		80	140	μ A
Input V_{IN} , $\overline{TCL}$						
Leakage current	I_P	$V_{SS} < V_{IP} < V_{DD}$ $T_A = 80$ °C		0.005	1	μ A
$\overline{TCL}$ input low level	V_{IL}				0.8	V
$\overline{TCL}$ input high level	V_{IH}		2.4			V
Leakage on pins $\overline{SAVE}$, $\overline{RES}$, RES	I_{OLK}	$V_{OUT} = V_{DD}$ $V_{OL} = 0.4$ V	4	0.050	1	μ A
O/P drive logic low	I_{OL}	$V_{DD} = 3.5$ V; $V_{OL} = 0.4$ V	2			mA
	I_{OL}	$V_{DD} = 1.6$ V; $V_{OL} = 0.4$ V	80			μ A

Table 3

V_{IN} Surveillance

Voltage thresholds at $T_A = 25$ °C

Version No.	Thresholds	at V_{DD}	Threshold Voltage Tolerance	Threshold Ratio*	Pin V_{IN} Input
	V_{SH} V_{SL} V_{RL}				
25	1.54 1.50 1.46	2.7 – 5.0 V	$\pm 10\%$	$\pm 2\%$	~ 100 M Ω

* Threshold ratio defined as V_{SH} / V_{SL} or V_{SL} / V_{RL} .

Table 4

Timing Characteristics

$V_{DD} = 5.0$ V, $T_A = -40$ °C to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays						
$\overline{TCL}$ to output pins	T_{DIDO}			250	500	ns
V_{IN} to output pins	T_{AIDO}	Excluding debounce time T_{DB}		4	10	μ s
Logic transition times on all output pins	T_{TR}	Load 10 k Ω , 100 pF		30	100	ns
Timeout period	T_{TO}	RC open, unshielded, $T_A = 25$ °C	60	100	160	ms
T_{TCL} input pulse width	T_{TCL}		150			ns
Power-on reset debounce	T_{DB}			$T_{TO}/64$		ms
Fastest pulse V_{IN} with debounce	T_{VINL}	-40 to +85 °C	10			μ s

Table 5

Voltage Reaction: V_{DD} Monitoring



Fig. 4

Fig. 5

Combined Voltage and Timer Reaction

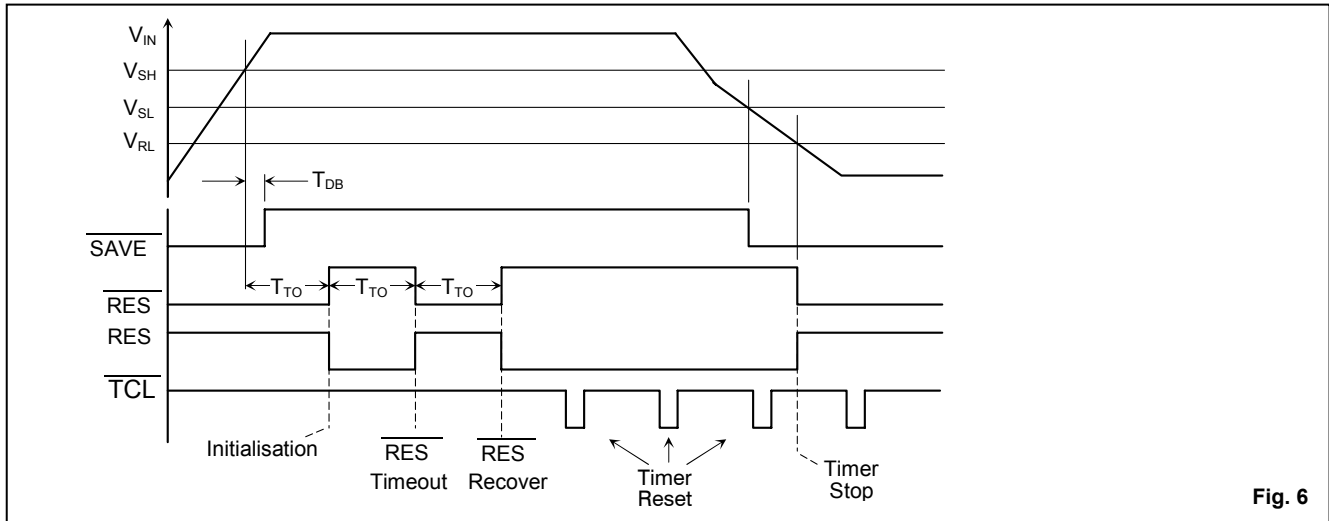


Fig. 6

Block Diagram

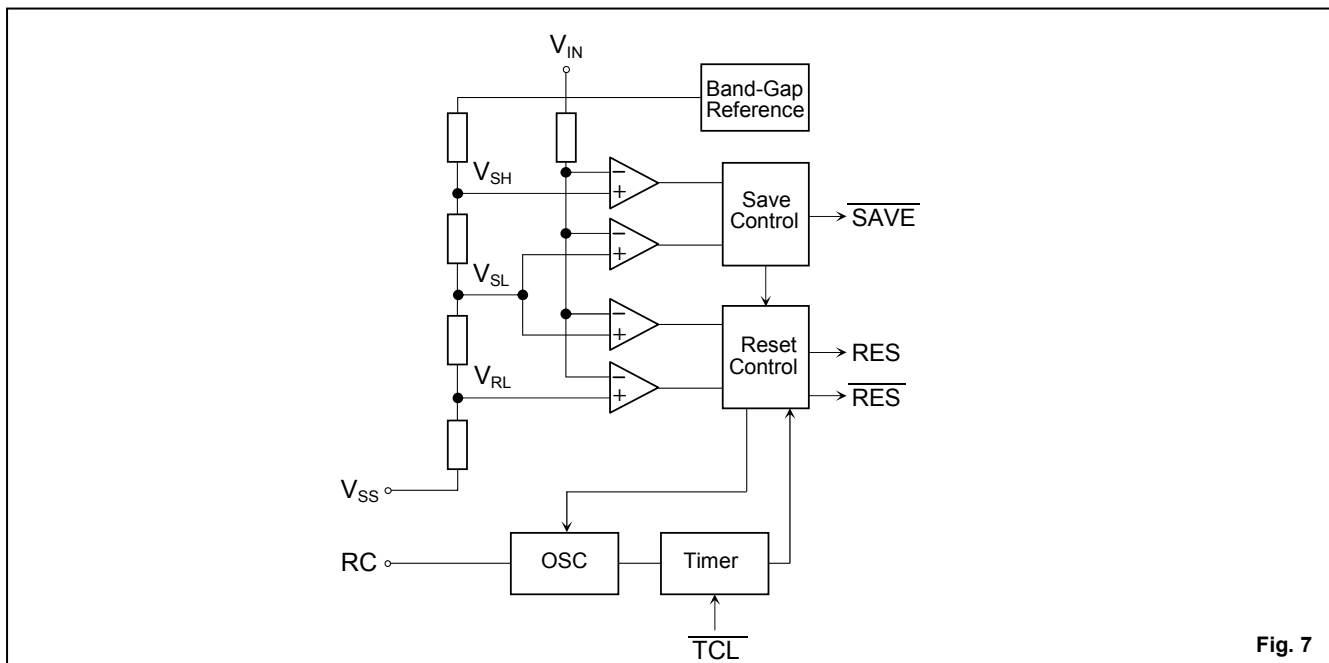


Fig. 7

Pin Description

Pin	Name	Function
1	V _{IN}	Voltage monitoring input
2	$\overline{\text{TCL}}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	V _{SS}	GND terminal
5	$\overline{\text{RES}}$	Reset output, open drain
6	$\overline{\text{SAVE}}$	Save output, open drain
7	RES	Positive reset output, open drain
8	V _{DD}	Positive supply voltage

Table 6

Functional Description

Thresholds and Outputs

The H6061 has open-drain outputs and voltage thresholds on pin V_{IN} of typically 1.5 V.

Internal Voltage Comparators

The voltage comparators detect the voltage applied to pin V_{IN} and compare it with thresholds V_{SH}, V_{SL} and V_{RL}. The H6061 is designed for monitoring regulated DC voltages and has bandgap thresholds independent of V_{DD}. The reaction of the H6061 to voltage changes on pin V_{IN} is given in Fig. 4. During powering-up, the outputs are active. After V_{IN} reaches the V_{SH} level, pin $\overline{\text{SAVE}}$ deactivates after a short debounce time T_{DB} to allow for fast ramp-ups. The initialization time T_{TO} then passes before the two reset outputs go inactive. Thereafter, when the voltage on pin V_{IN} falls below the V_{SL} level, pin $\overline{\text{SAVE}}$ goes active low as a first warning. If V_{IN} then drops below the V_{RL} level, the reset signals go active and are guaranteed down to 1.6 V. The reset outputs react also to timeouts (see "Timer clearing"). Note that when the supply voltage V_{DD} is below the level V_{OFF} (about 2.2 V), all outputs are in the active state for any allowed voltage of V_{IN}.

Voltage Programming

The H6061 was designed to give the best compromise in normal usage (see Table 3). Its voltage threshold can be programmed by an external resistor divider or a potentiometer to react at proportionally higher voltage levels (see Fig. 8 below).

Voltage Programming

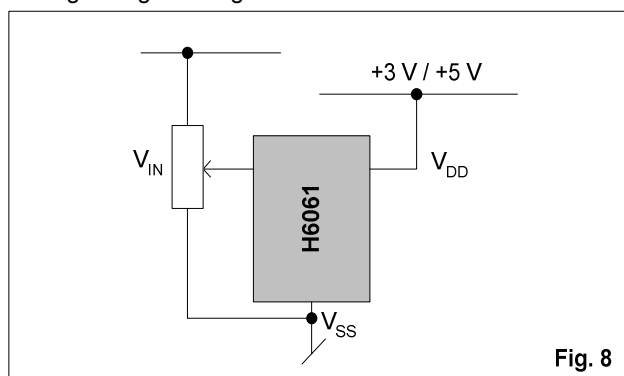


Fig. 8

Timer Programming

A single timeout period T_{TO} is used for the initialization reset duration and the watchdog timeout. With pin RC unconnected, the on-chip RC oscillator and divider chain give a timeout period T_{TO} of typically 100 ms. A resistor to V_{DD} will shorten this time, and a capacitor to V_{SS} will lengthen it (see Fig. 11). An approximation for calculating trial values given in milliseconds by the formula:

$$T_{TO} = \left[0.75 + \frac{(32 + C_1) \cdot 1.6}{4.8 + \frac{V_{DD} - 0.8}{R_1}} \right] \cdot 8.192$$

$$R_{1 \min.} = 10 \text{ k}\Omega, C_{1 \max.} = 1 \mu\text{F}$$

If R₁ is in M Ω and C₁ in pF, T_{TO} will be in ms.

Choice of component values must be determined in practice. To have a square wave of period 2T_{TO}, simply connect pin $\overline{\text{TCL}}$ to V_{DD} or V_{SS} and take the signal output from a reset pin.

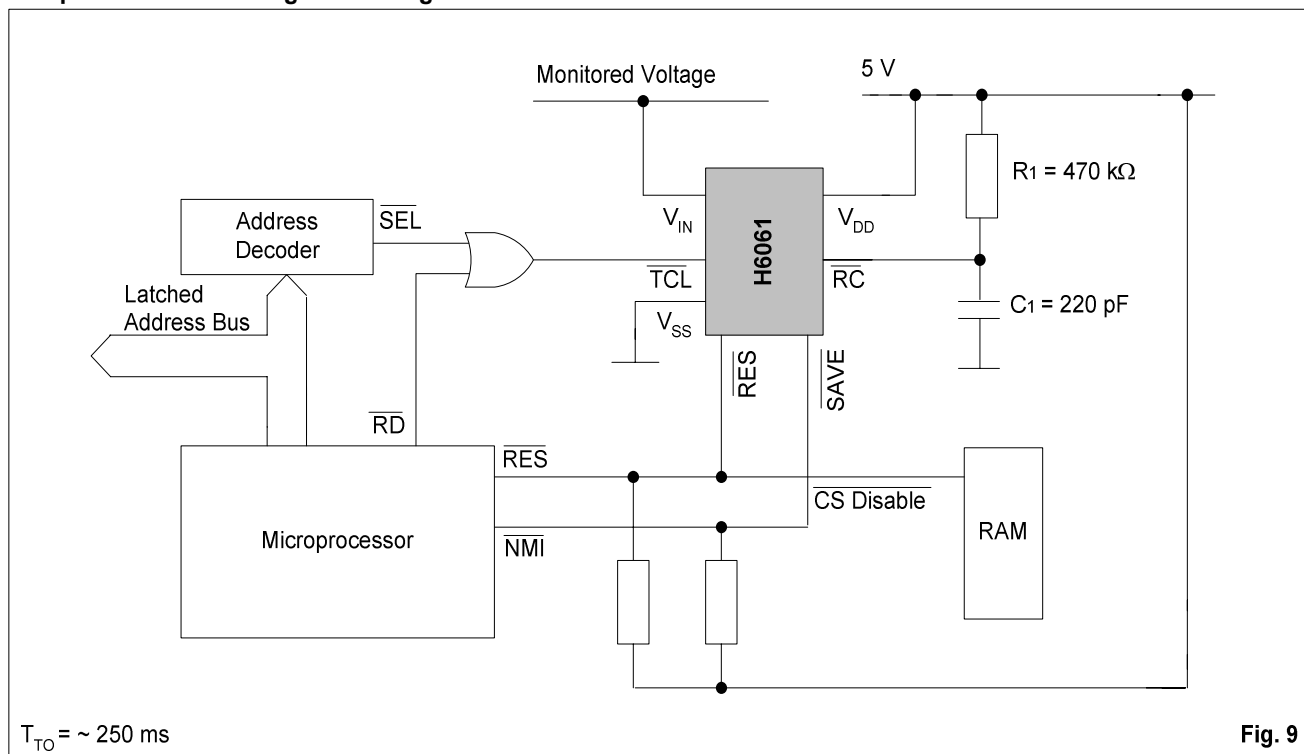
Timer Clearing

A negative edge or pulse at the $\overline{\text{TCL}}$ input longer than 150 ns will clear the timer and deactivate the reset outputs under normal running conditions (see Fig. 3). $\overline{\text{TCL}}$ will however have no effect either when V_{DD} < V_{OFF} or during the initialization period before the deactivation of the reset pins.

Combined Voltage and Timer Action

In Fig. 6 is a typical sequence of power-up, watchdog run, and power-down. During initialization the $\overline{\text{SAVE}}$ pin deactivates one debounce delay time T_{DB} after V_{IN} rises above V_{SH}, or when the power line V_{DD} rises above V_{ON}, whichever happens last. The reset pins only deactivate one timeout period T_{TO} afterwards to free the watchdog timer and end the initialization. Note that either V_{IN} falling below V_{RL} threshold or V_{DD} below V_{ON} will cause an initialization upon recovery. Following initialization, the watchdog timer will time out after time T_{TO} unless at least one $\overline{\text{TCL}}$ pulse clears it. On timeout the reset pins reactivate for a further T_{TO} period before deactivating again for another try. A $\overline{\text{TCL}}$ pulse will deactivate any timeout reset, and another $\overline{\text{TCL}}$ pulse must follow within a time T_{TO} to keep reset inactive. If no $\overline{\text{TCL}}$ pulses come at all, the reset pins go square-wave. Power-down overrides all this however. A falling voltage on V_{IN} gives a warning $\overline{\text{SAVE}} = 0$ signal at V_{IN} = V_{SL} before activating the reset pins as soon as V_{IN} drops below V_{RL}. The H6061 has fixed thresholds and low hysteresis for monitoring regulated DC lines. Additional protection is provided in case V_{DD} supply falls over about 10% below V_{ON} which thereupon activates all outputs at once.

Microprocessor Watchdog with Voltage Monitor



Combined Supply Monitor, Initializer and Watchdog

V_{IN} shield ¹⁾ or
decoupling ²⁾
optional against
interference

Nominal thresholds:

V_{SH} 2.84

V_{SL} 2.77

V_{RL} 2.70

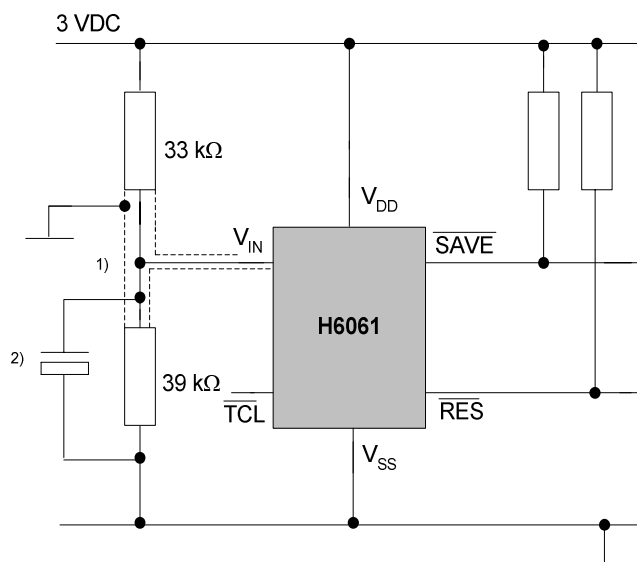


Fig.10

External Programming of RC Oscillator

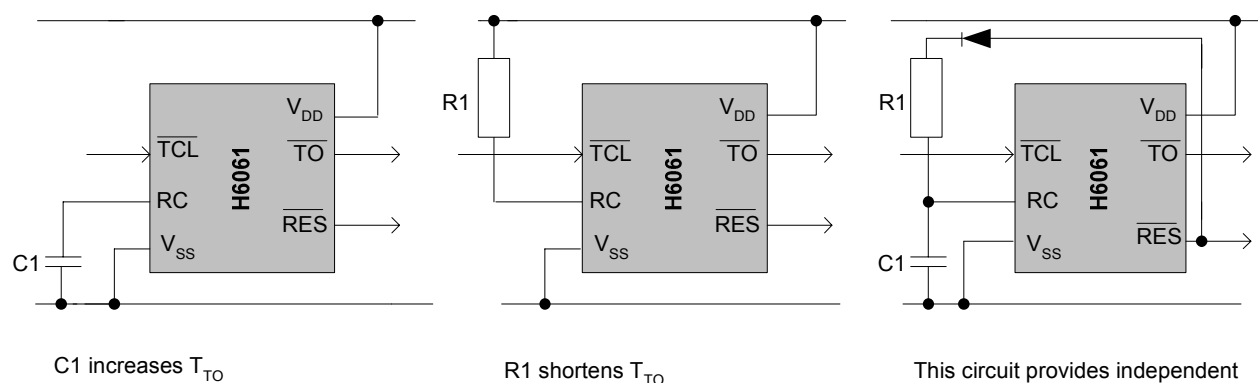


Fig. 11

Package Information

Dimensions of 8-Pin SOIC Package

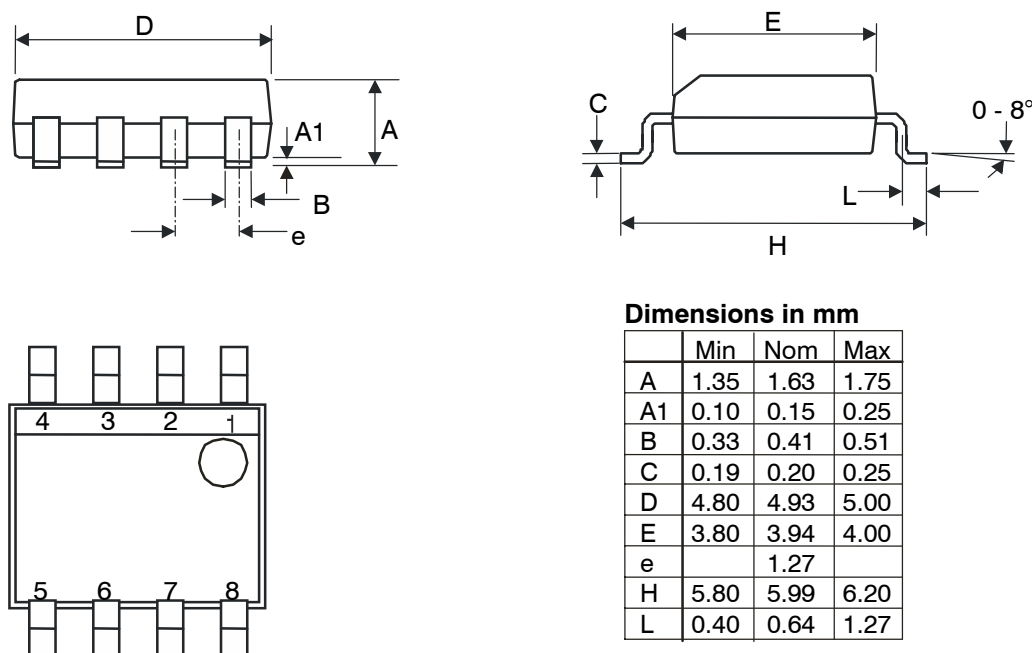


Fig. 12

Ordering Information

When ordering, please specify the complete Part Number

Part Number	Version	Package	Delivery Form	Package Marking (first line)	Temperature
H6061V25SO8A	V25	8-pin SOIC	Stick	606125	-40°C to +85°C
H6061V25SO8B		8-pin SOIC	Tape&Reel	606125	

Note: other versions are no longer available

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