ICS858020

LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-CML FANOUT BUFFER

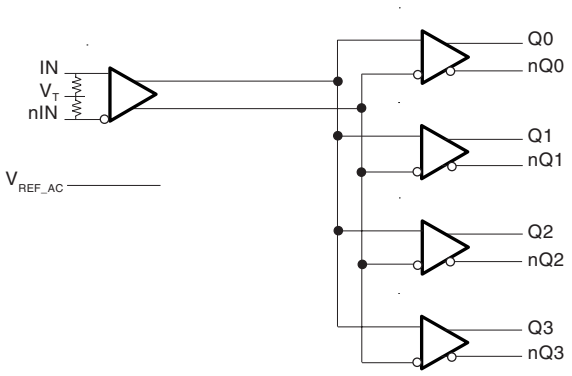
GENERAL DESCRIPTION

The ICS858020 is a high speed 1-to-4 Differential-to-CML Fanout Buffer and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. The ICS858020 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The ICS858020 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

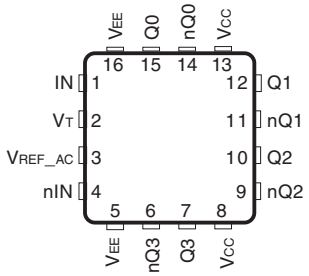
FEATURES

- Four differential CML outputs
- One LVPECL differential clock input
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 3.2GHz
- Output skew: 30ps (maximum)
- Part-to-part skew: 225ps (maximum)
- Additive phase jitter, RMS: <0.03ps (typical)
- Propagation delay: 600ps (maximum)
- Operating voltage supply range: V_{CC} = 2.375V to 3.63V, V_{EE} = 0V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS858020
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	IN	Input		Non-inverting LVPECL differential clock input. This input internally terminates with 50Ω to the V_T pin.
2	V_T	Input		Termination input.
3	V_{REF_AC}	Output		Reference voltage for AC-coupled applications. This output biases to V_{CC} - 1.38V.
4	nIN	Input		Inverting differential LVPECL clock input. This input internally terminates with 50Ω to the V_T pin.
5, 16	V_{EE}	Power		Negative supply pin.
6, 7	nQ3, Q3	Output		Differential output pair. CML interface levels.
8, 13	V_{CC}	Power		Positive supply pins.
9, 10	nQ2, Q2	Output		Differential output pair. CML interface levels.
11, 12	nQ1, Q1	Output		Differential output pair. CML interface levels.
14, 15	nQ0, Q0	Output		Differential output pair. CML interface levels.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (CML mode, V_{EE} = 0)
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	20mA
Surge Current	40mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 2A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.6V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.6	V
I_{EE}	Power Supply Current				135	mA

TABLE 2B. DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.6V; V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)	IN to V_T	40	50	60	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} - 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		2.8	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		3.4	V
V_{REF_AC}	Reference Voltage			V_{CC} - 1.5	V_{CC} - 1.4	V_{CC} - 1.3	V
V_{T_IN}	In-to-V_T Voltage					1.5	V

NOTE 1: Refer to Parameter Measurement Information, Input Voltage Swing diagram.

TABLE 2C. CML DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.6V; V_{EE} = 0V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 0.020	V_{CC} - 0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing		325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing		650	800		mV
R_{OUT}	Output Source Impedance		40	50	60	Ω

NOTE 1: Outputs terminated with 100Ω across differential output pair.

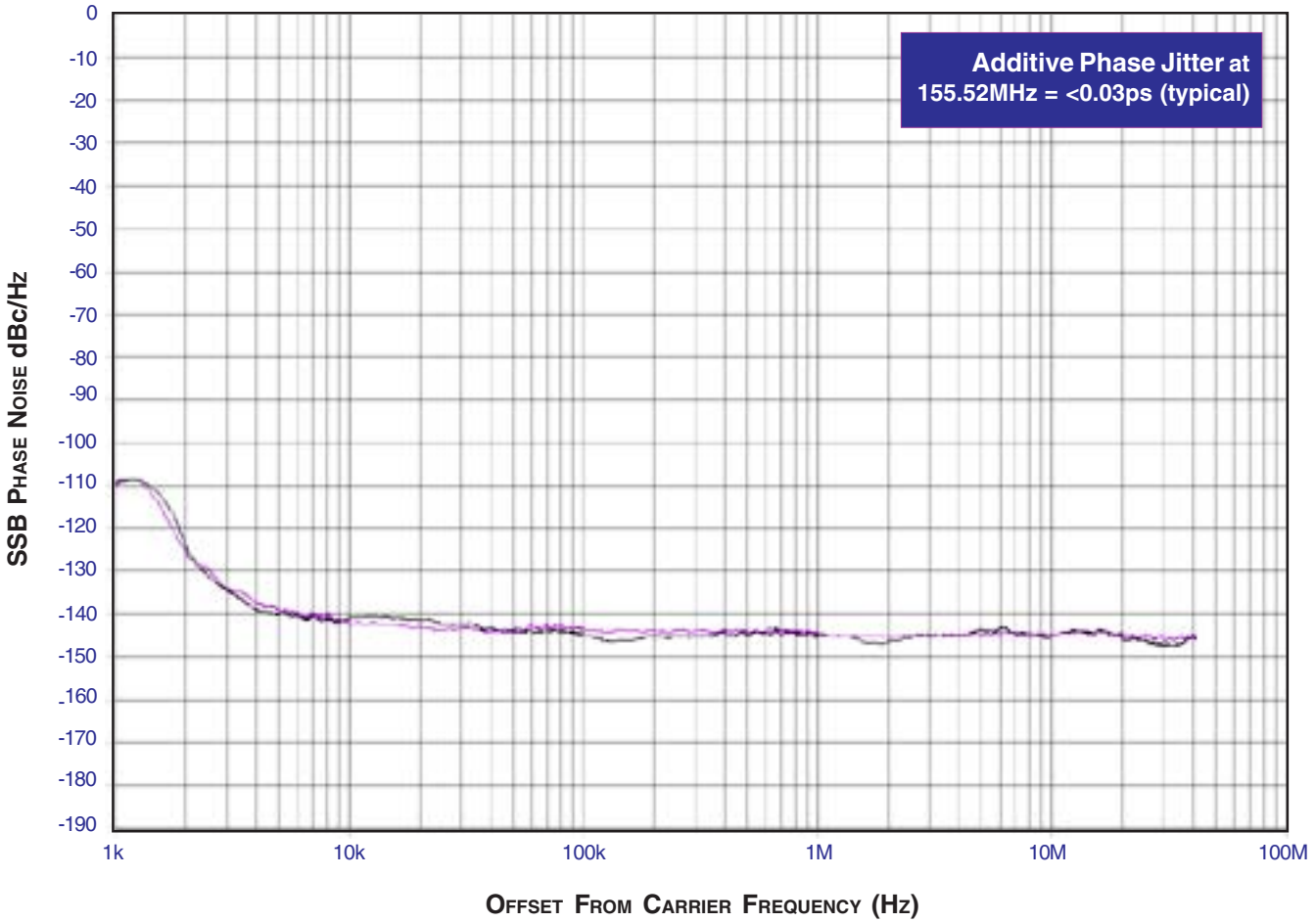
TABLE 3. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.6V TO -2.375V OR V_{CC} = 2.375 TO 3.6V; V_{EE} = 0V

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				3.2	GHz
t_{PD}	Propagation Delay; (Differential); NOTE 1		350		575	ps
*t*sk(o)	Output Skew; NOTE 2, 4			15	30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				225	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section			<0.03		ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	60		180	ps

All parameters characterized at ≤ 1.2GHz unless otherwise noted.
R_L = 100Ω after each output pair.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

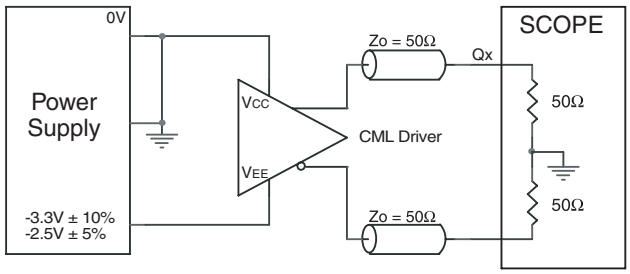
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

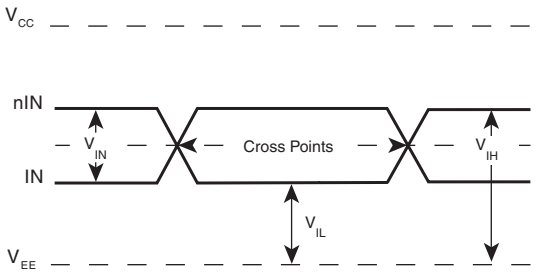


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

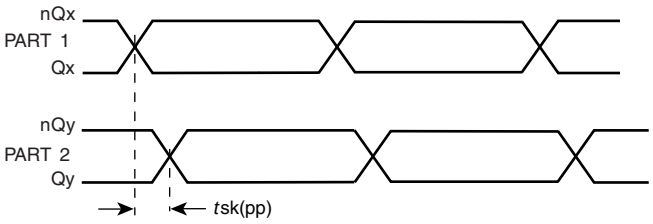
PARAMETER MEASUREMENT INFORMATION



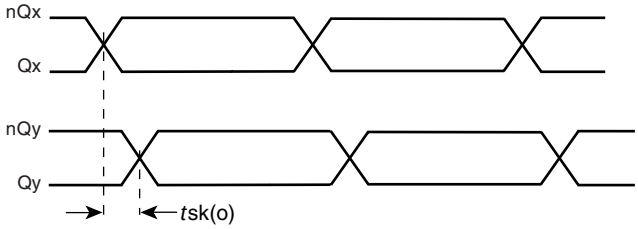
OUTPUT LOAD AC TEST CIRCUIT



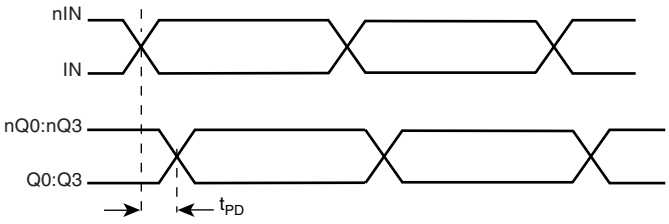
DIFFERENTIAL INPUT LEVEL



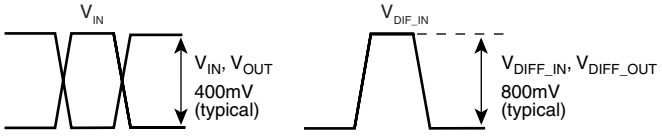
PART-TO-PART SKEW



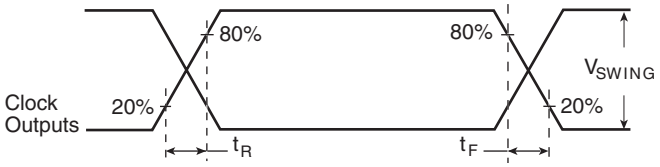
OUTPUT SKEW



PROPAGATION DELAY



SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACE (2.5V)

The IN/nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{IH} and V_{IL} input requirements. *Figures 1A to 1D* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use the termination they recommend. Please consult with the vendor of the driver component to confirm the driver termination requirements.

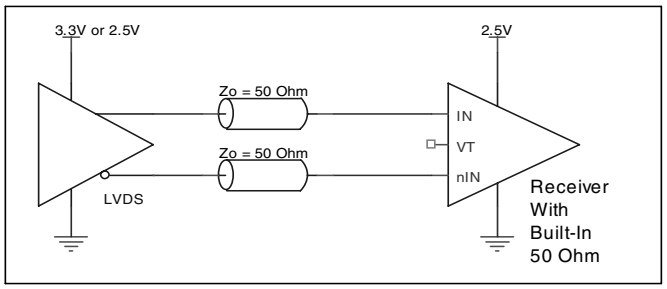


FIGURE 1A. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

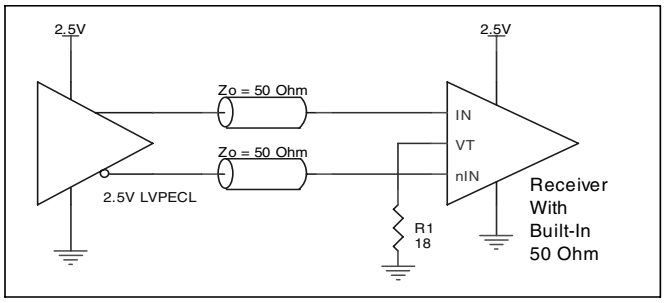


FIGURE 1B. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

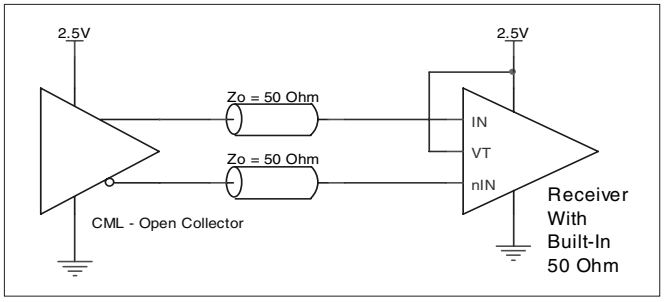


FIGURE 1C. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

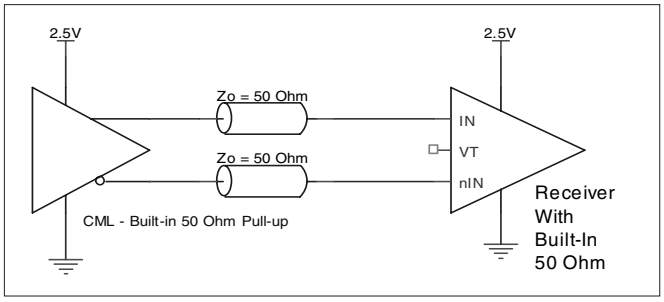


FIGURE 1D. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

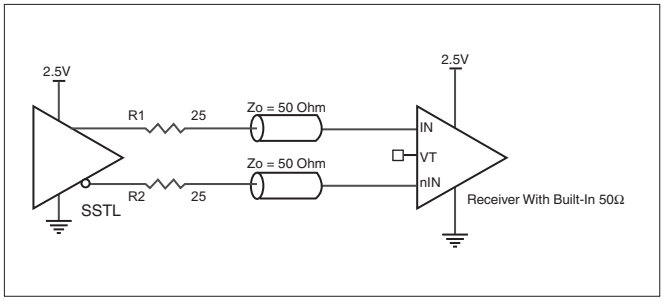


FIGURE 1E. HIPERCLOCKS IN/NIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACE (3.3V)

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{IH} and V_{IL} input requirements. *Figures 2A to 2D* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use the termination they recommend. Please consult with the vendor of the driver component to confirm the driver termination requirements.

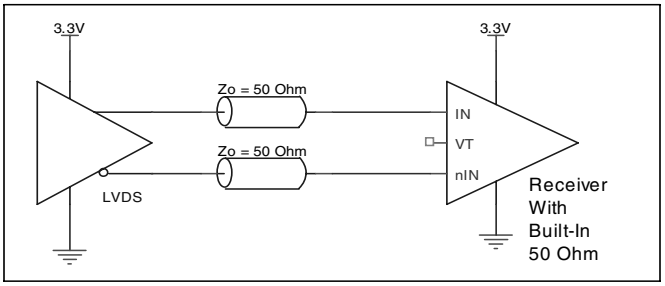


FIGURE 2A. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

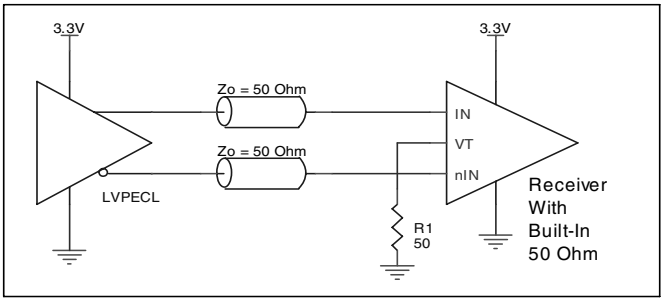


FIGURE 2B. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

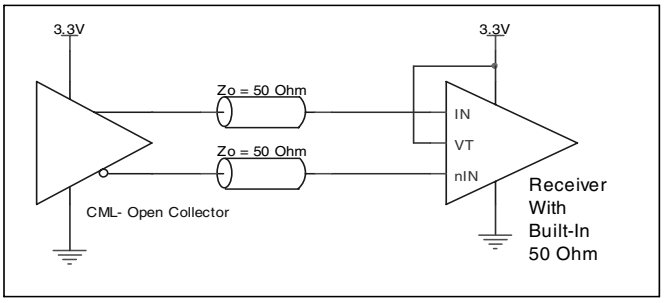


FIGURE 2C. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH OPEN COLLECTOR

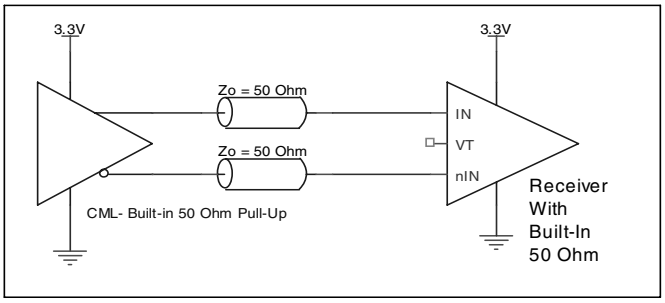


FIGURE 2D. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

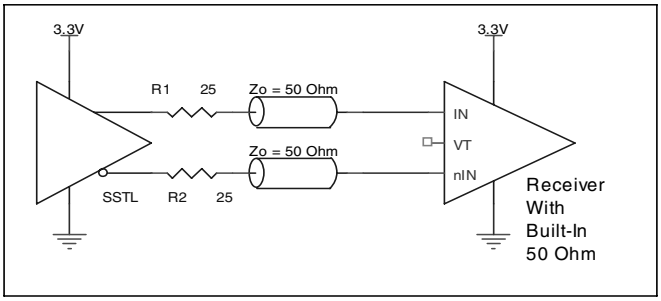


FIGURE 2E. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

SCHEMATIC EXAMPLE

Figure 3 shows a schematic example of the ICS858020. This schematic provides examples of input and output handling. The ICS858020 input has built-in 50Ω termination resistors. The input can directly accept various types of differential signal without AC couple. If AC couple termination is used, the ICS858020 also provides VREF_AC pin for proper offset level after the AC couple. This example shows the ICS858020 input driven by a 2.5V LVPECL driver with AC couple. The ICS858020 outputs are CML driver with built-in 50Ω pull up resistors. In this example, we assume the traces are long transmission line and the receiver is high input impedance without built-in matched load. An external 100Ω resistor across the receiver input is required.

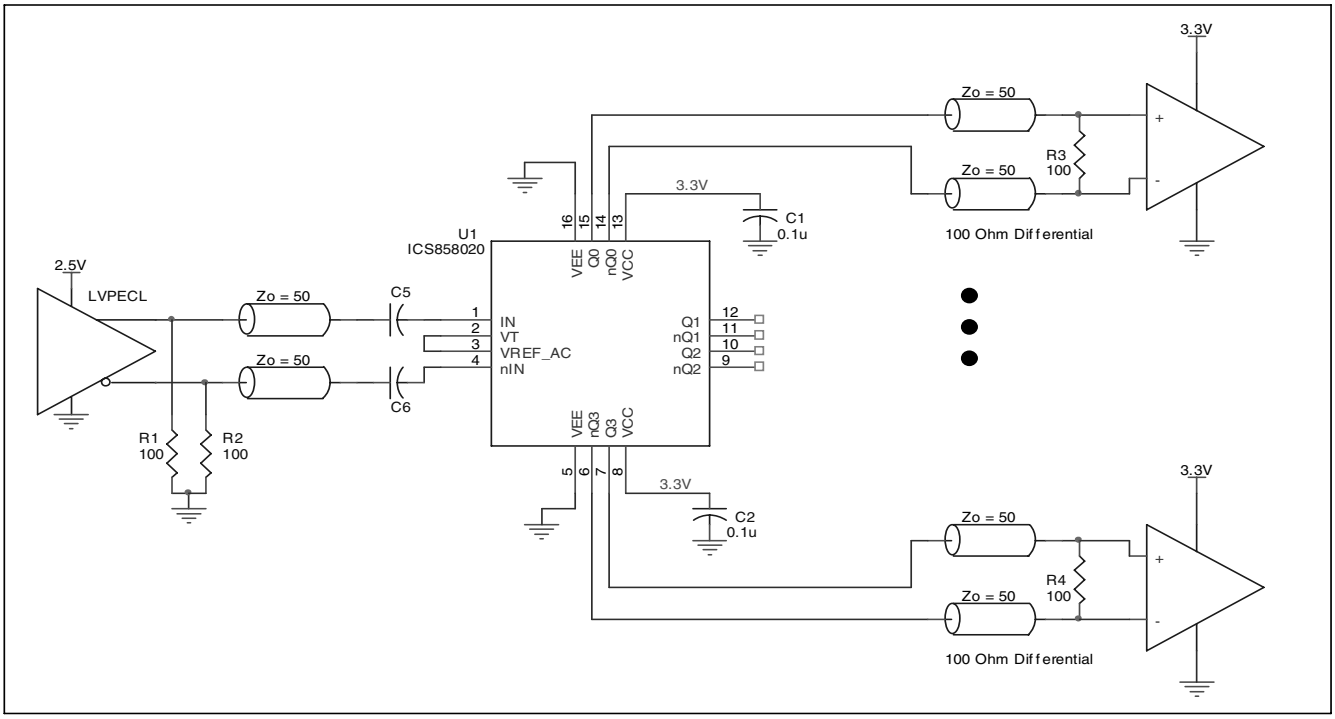


FIGURE 3. ICS858020 APPLICATION SCHEMATIC EXAMPLE

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/ electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

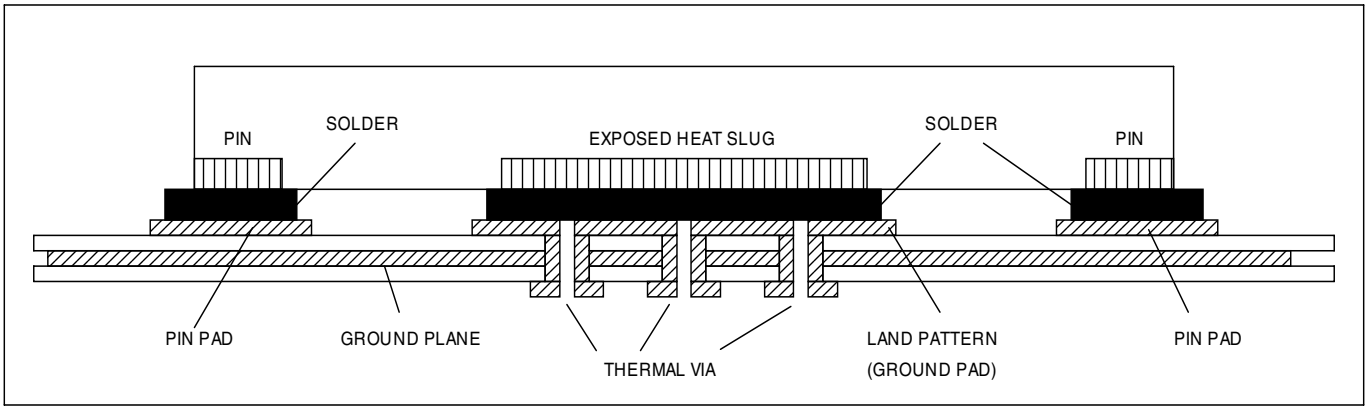


FIGURE 4. P.C. ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

RELIABILITY INFORMATION

TABLE 4. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} at 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS858020 is: 28

Pin compatible with SY58020U

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

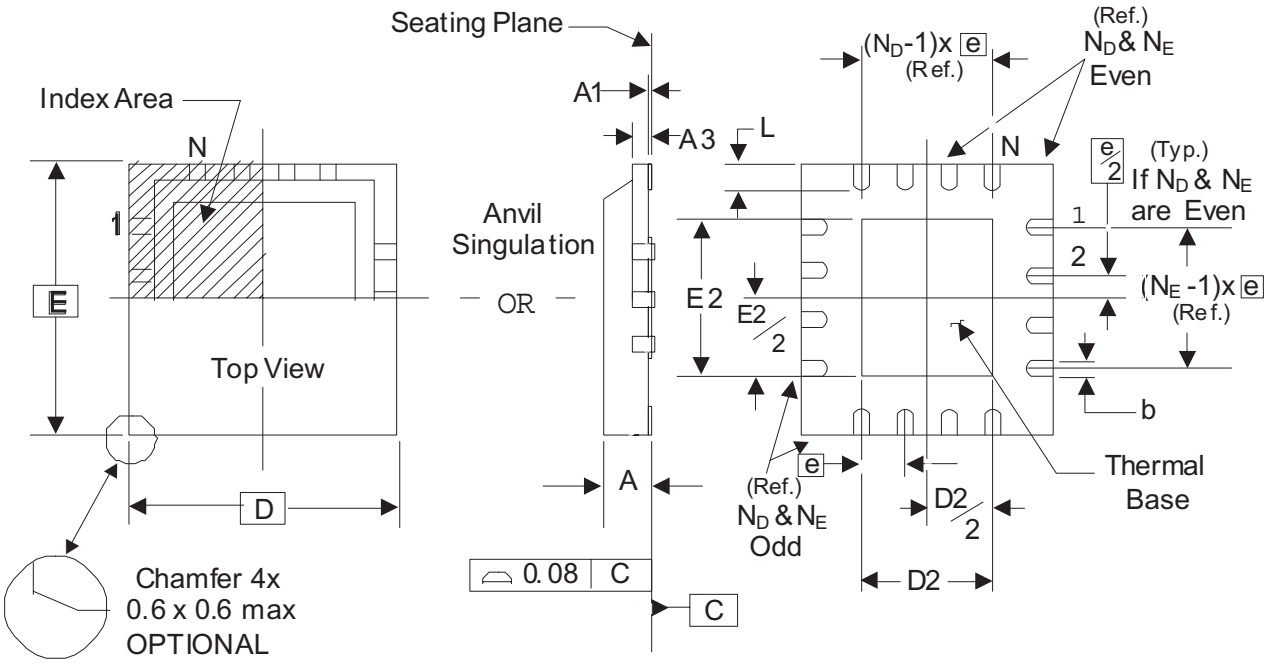


TABLE 5. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 6. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS858020AK	020A	16 Lead VFQFN	Tube	-40°C to 85°C
ICS858020AKT	020A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
ICS858020AKLF	20AL	16 Lead "Lead-Free" VFQFN	Tube	-40°C to 85°C
ICS858020AKLFT	20AL	16 Lead "Lead-Free" VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T6	12	Ordering Information Table - correct Shipping Packaging from Tray to Tube.	3/17/06
A	T6	12	Ordering Information Table - corrected marking from 820A to 020A.	4/24/06
A	 T6	10 12 13	Added *VFQFN EPAD Thermal Release Path section.* Updated VFQFN package outline. Ordering Information Table - added Lead-Free marking.	12/10/07