Low Stand-By Power, CV / CC PWM HV Switcher with Primary-Side Regulation

FEATURES

- Primary Side Regulation (PSR)
- +/- 5% Voltage Regulation
- +/- 5% Current Regulation
  - Automatic line variation compensation
  - Automatic primary inductance tolerance compensation
- <30mW Stand-by Power
- Valley Switching
- Thermal Shut down
- Over Voltage, and Low Line protection
- Frequency Jitter
- Integrated high voltage current source for low standby consumption

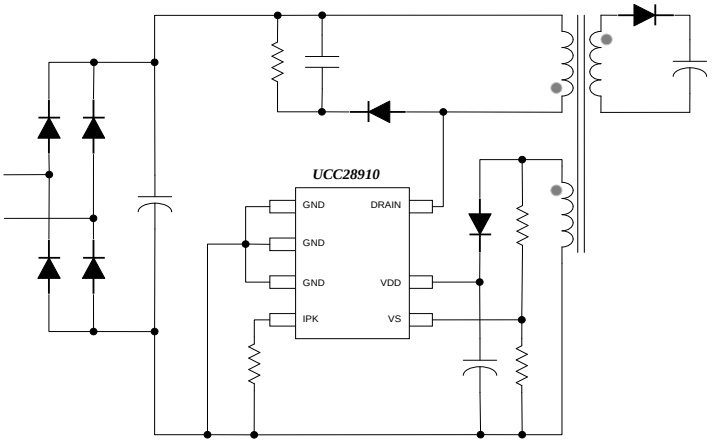
APPLICATIONS

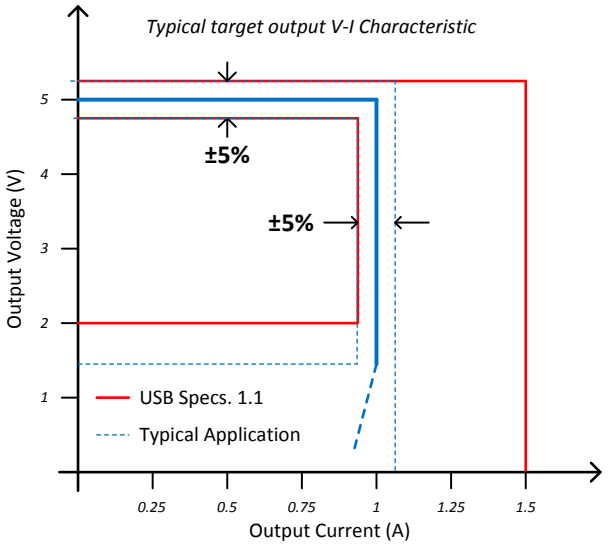
- USB compliant adapters for Cell Phones, Tablets, Cameras
- 5-7 Watt AC/DC Power Supplies

DESCRIPTION

The UCC28910 is dedicated to flyback power supplies and provides isolated output voltage and current regulation without the use of an optical coupler. The device incorporates a 700 V power FET and a controller that processes operating information from the auxiliary flyback winding and from the power FET to provide precise output voltage and current control.
The integrated high voltage current source and the controller current consumption are dynamically adjusted to allow very low stand-by power.
Control algorithms in the UCC28910 allow operating efficiencies to meet or exceed applicable standards. Discontinuous conduction mode (DCM) with valley switching is used to reduce switching losses. A combination of switching frequency and peak primary current amplitude modulation is used to keep conversion efficiency high across the full load and input voltage range.
This controller has a maximum switching frequency of 115 kHz and the protection features help to keep secondary and primary component stress levels in check across the operating range.
The controlled slope of the DRAIN voltage, during internal FET switch on and switch off, and the frequency jitter help to reduce EMI filter cost

Simplified Application Diagram and Typical V-I Regulation





ABSOLUTE MAXIMUM RATINGS (1)

PARAMETER		Min	Max	UNIT
DRAIN Voltage	V_{DRAIN}		700	V
Supply voltage, VDD	V_{DD}		Internally limited(2)	V
Maximum V_{DD} Clamp Current	I_{VDDCLP}		10	mA
Voltage range	V_{VS}	Internally limited(2)	7	V
	V_{IPK}	−0.5	5	
Peak VS Pin Current. (Current out of the pin)	I_{VS}		1.2	mA
Drain Current	I_{DRAIN}		1	A
Operating junction temperature range, T_J		−55	150	°C
Storage temperature, T_{STG}		−65	150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

(2) Do not drive with low impedance voltage source

RECOMMENDED OPERATING CONDITIONS (3)

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{VDD} operating input voltage	6		V_{DDCLP} (4)	V
I_{VS} (Current out of the pin)			1	mA
$I_{D\_PEAK(max)}$ operating DRAIN current peak			650	mA
Operating junction temperature (T_J)	-40		125	°C
Operating Ambient temperature (T_A)			100 (5)	°C

(3) Unless otherwise noted, all voltages are with respect to GND.
(4) See minimum value of V_{DDCLP} on Electrical Characteristic table.
(5) In case of thermal shut down, if T_A > 100 °C, the device doesn’t restart because of the T_{JHYS} (see protection Table)

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	RATING	UNIT
Human Body Model (HBM)	2000	V
Charged Device Model (CDM)	500	

KEY ELECTRICAL CHARACTERISTICS Test Conditions Unless Otherwise Specified:

V_{VDD}=15V, T_A= -40°C to 125°C, T_A=T_J

SUPPLY INPUT

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{RUN}	Supply current, run	V_{VDD} = 15V, V_{VS} = 3.9V, f_{SW} = $f_{SW(max)}$	2.4	2.8	3.2	mA
I_{RUNQ}	Quiescent Supply current	V_{VDD} = 15V, V_{VS} = 3.9V, f_{SW} = 0 Hz	2.0	2.4	2.8	mA
I_{WAIT}	Wait Supply Current	V_{VDD}= 15V, V_{VS} = 4.1V f_{SW} = $f_{SW(min)}$	250	280	310	μA
I_{WAITQ}	Quiescent Wait Supply Current	V_{VDD} = 15V, V_{VS} = 4.1V f_{SW} = 0 Hz	150	200	270	
I_{START}	Supply current before start	V_{VDD} from 0V to 6V, V_{DRAIN} = 0V		65		
I_{FAULT}	Supply Current after Fault	V_{VDD} = 15V, f_{SW} = *0 Hz*		175		

UNDER-VOLTAGE LOCKOUT

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD_{ON}	VDD turn-on threshold	VDD low to high	9	9.5	10	V
VDD_{OFF}	VDD turn-off threshold	VDD high to low	6	6.5	7	
VDD_{HVON}	HV Current Source start	VDD high to low	4.8	5.2	5.6	
ΔV_{UVLO}	UVLO Hysteresis	VDD_{ON} - VDD_{OFF}	2.80	3	3.2	

START UP CURRENT SOURCE

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CH1}	Start up current with VDD shorted to GND	V_{VDD} < 250mV, V_{DRAIN}=100V	-300			μA
I_{CH2}	Sourced current for start up at high VDD	V_{VDD} = 8V, V_{DRAIN}=100V			-0.6	mA
I_{CH3}	Sourced current for start up at low VDD	V_{VDD} = 2V, V_{DRAIN}=100V	-11.5			mA

VS INPUT

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{VSR}	Regulating Level	Measured in No Load Condition, T_J = 25°C	4.01	4.05	4.09	V
V_{VSNC}	Negative Clamp Level	I_{VS} = -300μA,	-190	-250	-325	mV
I_{VS}	Input Bias Current	V_{VS} = 4V	-0.25	0	0.25	μA

TIMING

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$f_{SW(max)}$	Maximum Switching Frequency	V_{VS} < 3.9V	105	115	125	kHz
$f_{SW(min)}$	Minimum Switching Frequency	V_{VS} > 4.1V	370	420	470	Hz
t_{ZTO}	Zero crossing timeout delay		1.8	2.1	2.45	μs
$t_{ON(min)}$	Minimum On time	I_{PK} = 0.85 V		300		ns

PROTECTION

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{DOCP}	DRAIN Over Current	IPK pin shorted to GND	0.8	0.86	0.9	A
V_{CSTE_OCP}	Equivalent $V_{CST(OCP)}$	V_{VS} = 3.9V, I_{D_OCP} * R_{IPK}	690	770	820	V
V_{CSTE_OCP2}	Equivalent $V_{CST(OCP2)}$	V_{VS} = 3.9V, I_{D_OCP2} * R_{IPK}		1190		V
$t_{ONMAX(max)}$	Max. FET On Time at high load	V_{VS} < 3.9V, IPK Shorted to GND	13		22	μs
$t_{ONMAX(min)}$	Max. FET On Time at low load	V_{VS} > 4.1V, IPK Shorted to GND	4.3		8	μs
V_{OVP}	Over-Voltage Threshold	At VS input	4.45	4.6	4.75	V

I_{VSLRUN}	VS Line Sense Run Current	Current out of VS pin – increasing	190	220	260	µA
$I_{VSLSTOP}$	VS Line Sense Stop Current	Current out of VS pin - decreasing	70	80	95	µA
K_{VSL}	Line sense I_{VS} ratio	I_{VSLRUN} / $I_{VSLSTOP}$	2.5	2.8	3.05	
VDD_{CLP}	VDD Voltage Clamp	I_{VDDCLP} Forced = 2mA	26	28	30	V
I_{VDDCLP_OC}	VDD Clamp Over Current	V_{VDD} > 25V	4	5	6	mA
T_{JSTOP}	Thermal Shutdown Temperature	Internal junction temperature		150		°C
T_{JHYS}	Thermal Shutdown Hysteresis	Internal junction temperature		50		°C

POWER FET

NAME	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
BV_{DSS}	Break down Voltage	T_J = 25°C		700			V
R_{DSON}	Power FET on Resistance	V_{DS} = 0.1V	T_J = 25°C		9.6	10.8	Ω
			T_J = 125°C		16	18	
$I_{LEAKAGE}$	DRAIN pin Leakage current	V_{DS} = 400V HV components off	T_J = 25°C			5	µA

CURRENTS

NAME	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{D\_PEAK(max)}$	Maximum DRAIN Peak Current	V_{VDD} =15V, IPK pin shorted to GND T_J = 25°C	590	600	610	mA
R_{IPK_SHORT}	IPK to GND resistance Max to assume IPK shorted to GND	V_{VDD} = 15V			200	Ω
$R_{IPK(min)}$	IPK to GND Min resistance	V_{VDD} = 15V	800			Ω
$V_{CSTE(max)}$	Equivalent Current sense threshold	V_{VDD} = 15V, V_{VS} = 3.9V, $I_{D\_PK(max)} * R_{IPK}$		540		V
$V_{CSTE(min)}$	Equivalent Current sense threshold	V_{VDD} = 15V, V_{VS} = 4.1V, $I_{D\_PK(min)} * R_{IPK}$		180		V
K_{AM}	AM control ratio	V_{CSEMAX} / V_{CSEMIN}		3		V / V
K_{CC}	CC regulation gain	V_{VDD} = 15V, V_{VS} > 3.9V; $T_{demag}*f_{sw}$		0.4125		
V_{CCR}	CC regulation Constant	V_{VDD} = 15V, V_{VS} < 3.9V, $V_{CSETMAX}$ *K_{CC}	215	223	232	V

DEVICE INFORMATION

Functional Blok Diagram

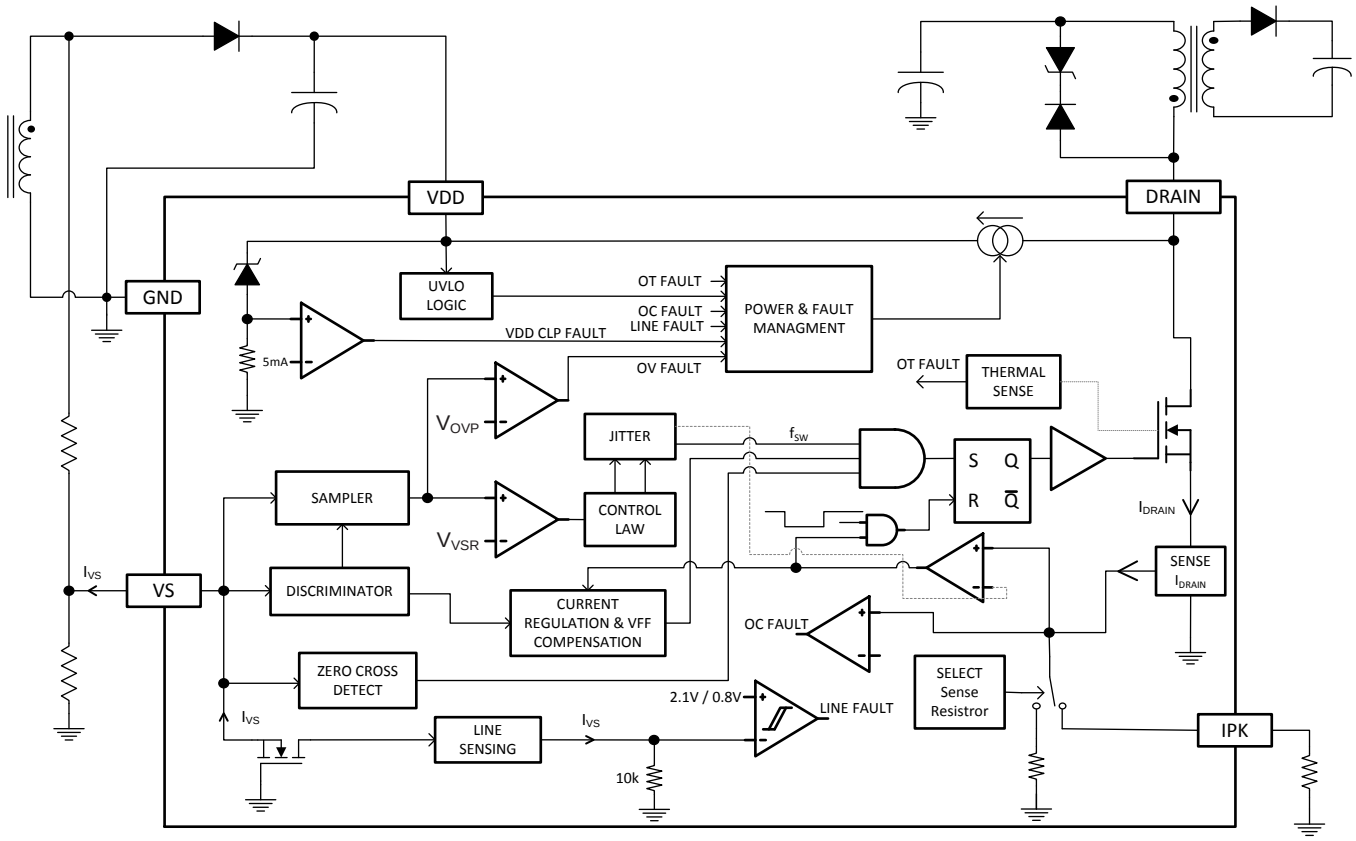


Figure 1 Device Block Diagram

SOIC7 Package

(Top view)

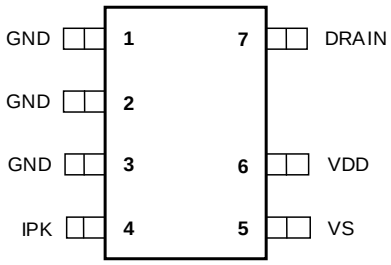


Figure 2 Device Pin Out

PACKAGES

Pin Number	Package	Mounting Type
7	SOIC - 7	Surface mounting

Terminal Function

PIN			DESCRIPTION
NAME	NO.	I/O	
DRAIN	TBD	I	**DRAIN** It is the DRAIN of the internal power FET but also the input for the high voltage current source used to start up the device.
IPK	TBD	O	**IPK** is used to set the maximum peak current flowing in the power FET that is proportional to the maximum output current
GND	TBD	P	The **GrouND** pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling as close as possible to this pin and avoid any common trace length with analog signal return paths.
VDD	TBD	P	**VDD** is the supply pin to the controller. A carefully placed bypass capacitor to GND is required on this pin.
VS	TBD	I	**Voltage Sense** this input is used to provide voltage and timing feedback to the controller. Normally this pin is connected to a voltage divider between an auxiliary winding and ground. The value of the upper resistor of this divider is used to program low line thresholds.

Thermal Resistance

Name	Parameter	Test Condition	Value	Unit
R_{thJA}	Junction to ambient thermal resistance	850mW dissipated power, 560mm^2 Copper area connected to GND pins	95	°C/W

Output power Table

Part Number	230 V_{AC}		85 – 230 V_{AC}	Unit
	Adapter (1)	Open Frame (2)	Adapter (1)	
UCC28910	10	12	7.5	W

1. Typical continuous power in enclosed adapter at 60 °C ambient, with adequate copper area connected on GND pins
2. Maximum continuous power with open frame design at 60°C ambient, with adequate copper area connected on GND pins.

APPLICATION INFORMATION

Detailed Pin Description

VDD (IC Voltage Supply)

The VDD pin is connected to a bypass capacitor to ground and typically to a rectifier diode connected to the aux winding. The VDD turn on UVLO threshold is 9.5V (VDD_{ON} Typ.) and turn off UVLO threshold is 6.5V (VDD_{OFF} Typ.). The pin is provided with an internal clamp that avoids the voltage to exceed the absolute maximum rating of the pin. The internal clamp cannot absorb very high currents, so, to avoid damaging the device, when the clamp flowing current exceeds 5 mA (I_{DDCLP_OC} Typ.) the device stops switching. The VDD pin operating range is then from 7V (VDD_{OFF} Max.) up to 25V (VDD_{CLAMP} min). The USB charging specification requires that the output current operates in constant current mode from 5V to a minimum of 2V; this is easily achieved with a nominal VDD of approximately 17V. Set N_{AS} (auxiliary to windings secondary turn ratio) to 17V / (V_{OUT}+V_F) where V_F is the voltage drop on the output diode at low current. The additional VDD headroom up to the clamp allows for VDD to rise due to the leakage energy delivered to the VDD in high load conditions.

The current consumption of the IC depends on the operating condition. Because driving the power FET requires some energy, a portion of the current consumption depends on the operating frequency. When operating in light load and the switching frequency is low enough, between two switching cycles, part of the device control logic is switched off saving energy.

The graph below shows the current consumption as a function of normalized converter output power.

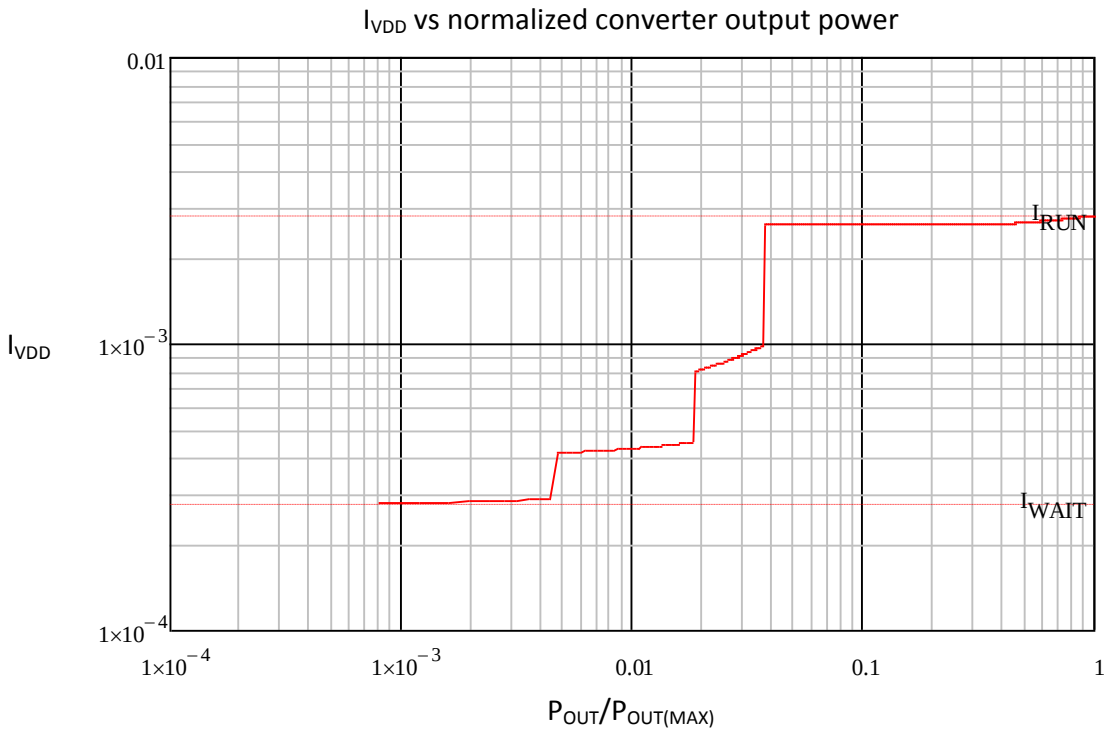


Figure 3 I_{VDD} Consumption vs Load

GND (Ground)

The device is provided with three pins, shorted together, that are used as external ground reference to the controller for analog signal reference. The three pins function to pull out the heat caused by the power dissipation of the internal power FET. Place the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and IPK signal pins.

VS (Voltage Sense)

The VS pin is connected to a resistor divider from the aux winding to ground. The VS pin provides three functions.

1) It provides output voltage information to the voltage control Loop. The output voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage.

2) It also provides timing information to achieve valley switching and the duty cycle of the secondary transformer current is determined by the waveform on the VS pin.

The data provided in 1) and 2) are sensed during the MOSFET off time.

3) A third function is sensing a sample of the bulk capacitor input voltage to provide under-voltage shutdown. This information is sensed during the MOSFET on time when the auxiliary winding voltage is negative. The voltage on VS pin is clamped to GND and through the resistance R_{S1} connected between the aux winding and VS. During the on time, the current sourced from the VS pin is sensed by the device. For the under-voltage function, the enable threshold on VS current is 210µA and the disable threshold is 75µA.

The resistor values for R_{S1} and R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{V_{RMS\_EN} \cdot \sqrt{2}}{N_{PA} \cdot I_{VSLRUN}}$$

Where

N_{PA} is the transformer primary to aux turns ratio

V_{RMS_EN} is the AC RMS voltage to enable turn on of the controller

I_{VSLRUN} is the line sense current (210µA Typ.)

$$R_{S2} = \frac{V_{VSR} \cdot R_{S1} \cdot N_{PA}}{(V_{OUT} + V_F) \cdot N_{PS} - (V_{VSR} \cdot N_{PA})}$$

Where

V_{OUT} is the converter output voltage in V

V_F is the output rectifier forward drop at low current in V

N_{PS} is the transformer primary to secondary turns ratio

R_{S1} is the VS divider high side resistance in Ohms

V_{VSR} is the regulating level of VS pin

IPK (Set the Maximum DRAIN Current Peak)

A resistance (R_{IPK}) connected between this pin and GND sets the maximum value of the power FET peak current according to the following relationship:

$$I_{D\_PK(\max)} = \frac{V_{CSTE(\max)}}{R_{IPK}}$$

If the pin is shorted to GND (R_{IPK}=0) the peak current is automatically set to 600mA ($I_{D\_PEAK(max)}$)

A test is performed at device start up to check whether the IPK pin is shorted to GND or the R_{IPK} is present. If R_{IPK} is less than R_{IPK_SHORT} (Max), the device interprets it as a short (R_{IPK}=0) and the DRAIN peak current is set to $I_{D\_PEAK(max)}$.

Otherwise, if R_{IPK} is greater than $R_{IPK(min)}$ (Min), the device sets the peak current DRAIN according to the previous equation.

A value of R_{IPK} that is in between the before said values, is not allowed since the value of the peak current may be selected using anyone of the two sense resistances: the internal sense resistance and R_{IPK}.

DRAIN

The DRAIN pin is connected with the DRAIN of the internal power FET. This pin also provides current to the high voltage current source at start up.

Functional Description

The UCC28910 is a flyback power supply switcher which provides accurate output voltage and constant current regulation with primary side feedback, eliminating the need for opto coupler feedback circuits. The device has an internal 700V power FET plus a controller which forces the converter to operate in discontinuous conduction mode with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide optimized conversion efficiency over the entire load range. The control law provides a wide dynamic operating range to achieve the < 30mW Five Star standby power requirement.
The UCC28910 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary side control.
A complete charger solution can be realized with a straightforward design process, low cost and low component count solution.

Primary Side Voltage Regulation

Figure 4 illustrates a flyback converter. The voltage regulation blocks of the device are shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary side control.

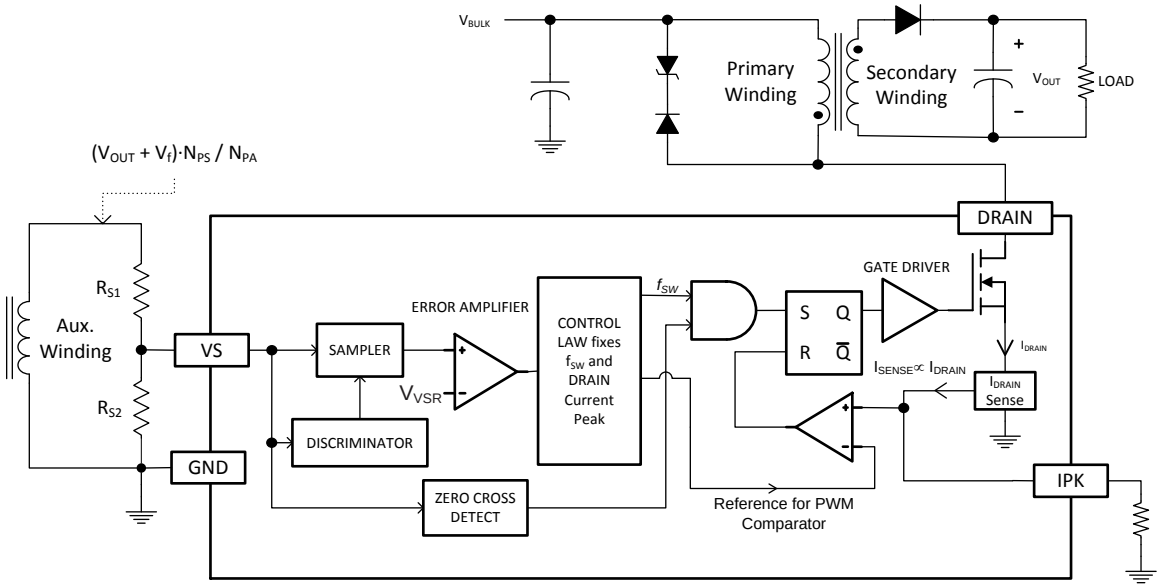


Figure 4 Voltage Loop Block Diagram

In primary side control, the output voltage is sensed by the auxiliary winding during the transfer of transformer energy to the secondary. Figure 5 shows the down slope representing a decreasing total rectifier V_F and the secondary winding resistance voltage drop as the secondary current decreases to 0A. To achieve an accurate representation of the secondary output voltage on the aux winding, the Discriminator reliably ignores the leakage inductance reset and ring, continuously samples the aux voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches 0 current. The internal reference on VS is 4V; the resistor divider is selected as outlined in the VS pin description.

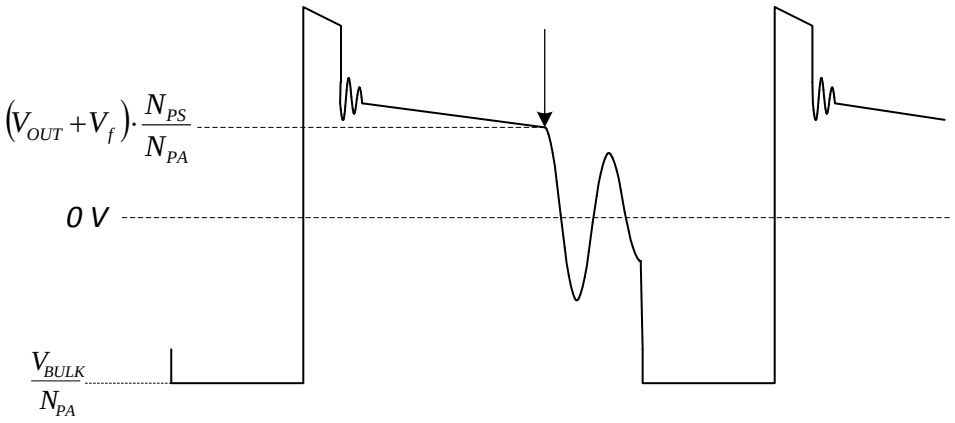


Figure 5 Auxiliary winding Voltage

The UCC28910 VS signal Discriminator block (Figure 4) ensures accurate sampling time for an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to Figure 6 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, t_{LK_RESET}. Since this can mimic the waveform of the secondary current decay, followed by a sharp down-slope, it is important to keep the leakage reset time less than 500ns for I_{DRAIN} minimum, and less than 1.5µs for I_{DRAIN} maximum. The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 100 mV_{p-p} at least 200 ns before the end of the demagnetization time, t_{DMAG}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions, when t_{DMAG} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary winding voltage by R_{S1} and R_{S2}, and is equal to 100 mV x (R_{S1} + R_{S2}) / R_{S2}.

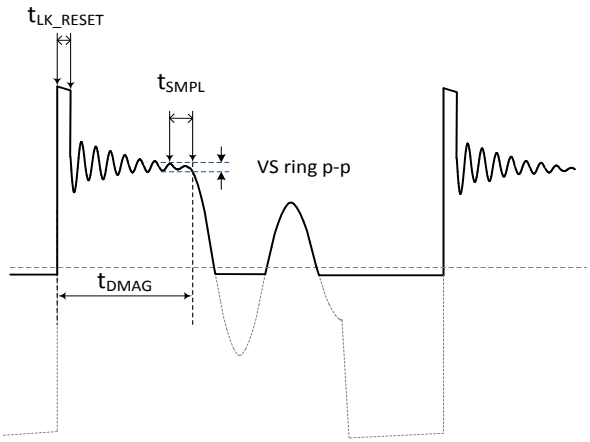


Figure 6 VS voltage

During voltage regulation, the controller operates in frequency modulation mode and amplitude modulation mode. The internal operating frequency limits of the controller are 140 kHz maximum and 420Hz minimum. The transformer primary inductance and turns ratio sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. There is no external compensation required for the UCC28910 device. Since the output capacitance and load resistance determine the pole of the plant, the following value of C_{OUT} is recommended to maintain a unity gain frequency of less than f_{SW} / 5.

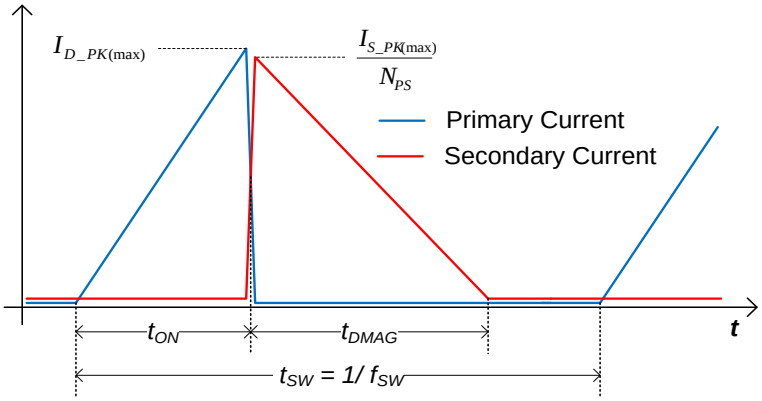
$$C_{OUT} \geq \frac{16000uF \times P_{MAX}}{f_{SW(\max)}}$$

Where
C_{OUT} is in µF
P_{MAX} is in watts
$f_{SW(max)}$ is in kHz

Example: A 5W charger operating at 100 kHz maximum should have an output capacitance ≥ 800µF.

Primary Side Current Regulation

Timing information at the VS pin and the primary current information allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current will be at $I_{D\_PK(max)} = V_{CSTE(max)} / R_{IPK}$. Referring to Figure 7 below, the primary peak current, turns ratio, secondary demagnetization time (t_{DM}), and switching period (t_{SW}) establish the secondary average output current. When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target as long as the aux winding can keep VDD above the VDD UVLO threshold (VDD_{ON}).



$$I_{OUT} = \frac{1}{2} \cdot I_{S\_PK(\max)} \cdot t_{DMAG} \cdot f_{SW} = \frac{N_{PS}}{2} \cdot I_{D\_PK(\max)} \cdot D_{MAGCC}$$

where $D_{MAGCC} = t_{DMAG} \cdot f_{SW} = K_{CC}$

Figure 7 Output current estimation

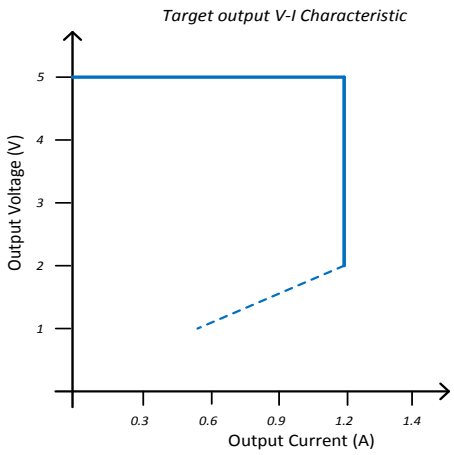


Figure 8 Target output V-I characteristic

In equations of figure 7 D_{MAGCC} is the secondary side diode conduction duty cycle during constant-current control mode operation. The D_{MAGCC} maximum value is set internally by the UCC28910 and it is equal to K_{CC}.

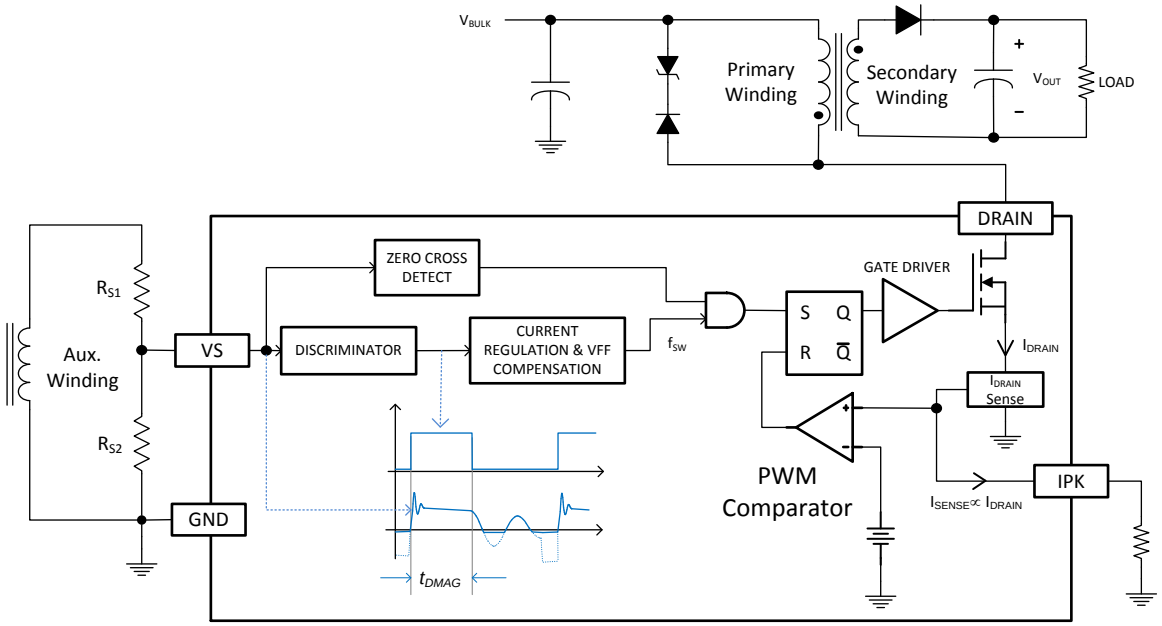
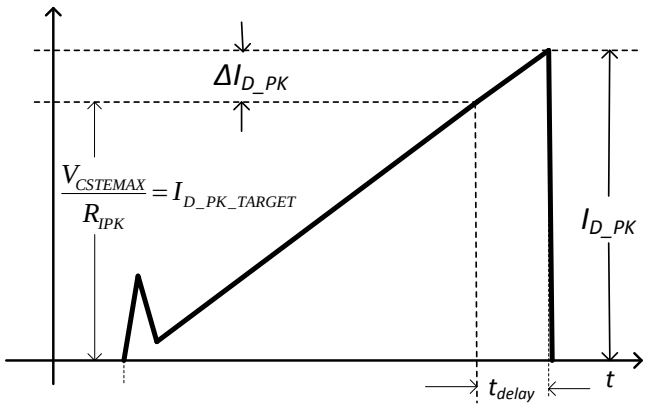


Figure 9 Output current control loop block diagram

Voltage Feed Forward Compensation

During normal operation the on time is determined by sensing the power FET current and switching off the power FET as this current reaches a threshold fixed by the feedback loop according to the load condition. The power FET is not immediately turned off and its current, that is also the primary winding current, continues to rise for some time during the propagation delay (t_{delay} in Figure 10). Keeping the reference for the PWM comparator constant, the value of the primary winding peak current depends on the slope of the primary winding current and t_{delay}.
The slope of the primary current is proportional to the Flyback stage input voltage (V_{BULK}).



$$\Delta I_{D\_PK} = \frac{V_{BULK}}{L_P} \cdot t_{delay}$$

$$I_{D\_PK} = I_{D\_PK\_TARGET} + \frac{V_{BULK}}{L_P} \cdot t_{delay}$$

Figure 10 Effect of the propagation delay on the primary current peak

The current loop estimates the output current assuming the primary winding peak current is equal to the I_{PK_TARGET} and compares this estimated current with a reference to obtain the current regulation. Considering, in reality, I_{D_PEAK} will be different from $I_{D\_PEAK\_TARGET}$ (see Figure 10) we need to compensate the effect of the propagation delay. The UCC28910 incorporates fully integrated propagation delay compensation that modifies the switching frequency keeping the output current constant during CC mode operation (constant current). This function is totally integrated in the controller and

requires no external components. This feature keeps the output current constant despite input voltage variations, for this reason it is called voltage feed forward compensation.

Control Law

During voltage regulation, the device operates in frequency modulation mode and amplitude modulation mode. The internal operating frequency limits of the device are $f_{SW(max)}$ and $f_{SW(min)}$. The transformer primary inductance and primary peak current chosen sets the maximum operating frequency of the converter. The output preload resistor and efficiency at low power determines the converter minimum operating frequency. During constant current regulation the device operates only in frequency modulation mode reducing the switching frequency as the output voltage decreases. Figure 11 shows how the primary current peak and the switching frequency changes with respect to changes in load.

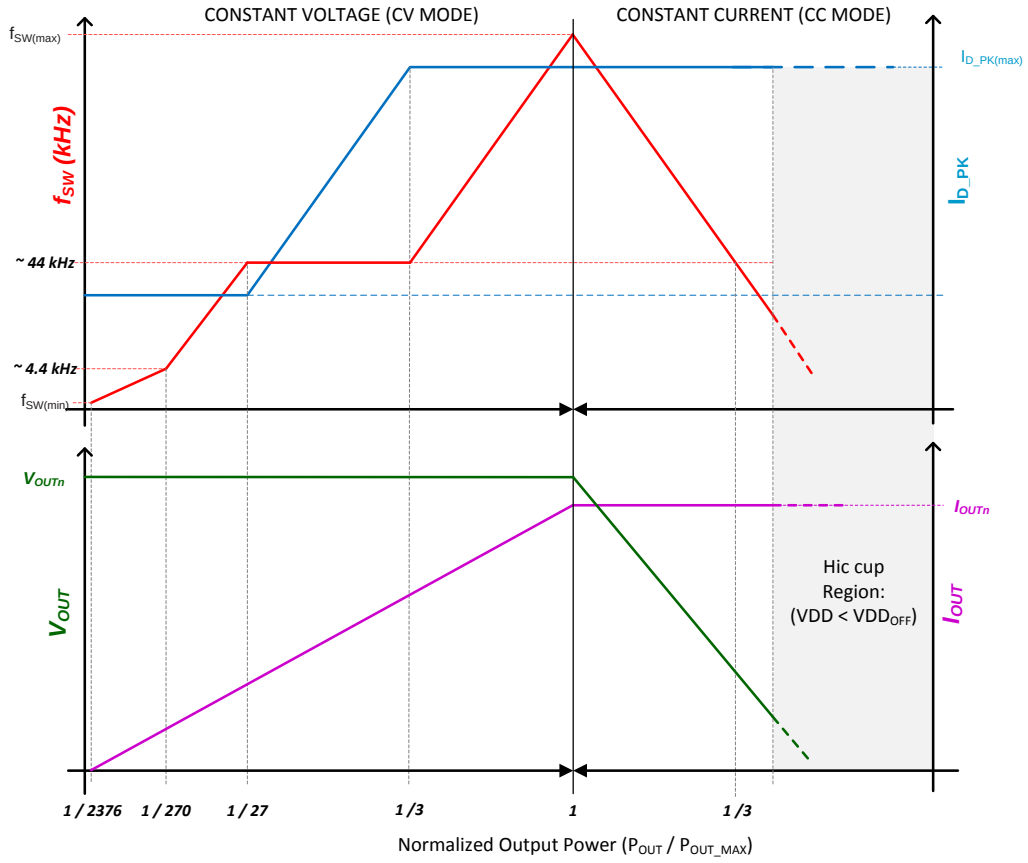


Figure 11 Control Law Profile

Valley Switching

The UCC28910 utilizes valley switching to reduce switching losses in the MOSFET and minimize the turn on FET current spike. The UCC28910 operates in valley switching in almost all load conditions until the V_{DS} ringing is diminished. By switching at the lowest V_{DS} voltage the MOSFET turn on dV / dt is minimized which is a benefit to reduce EMI.

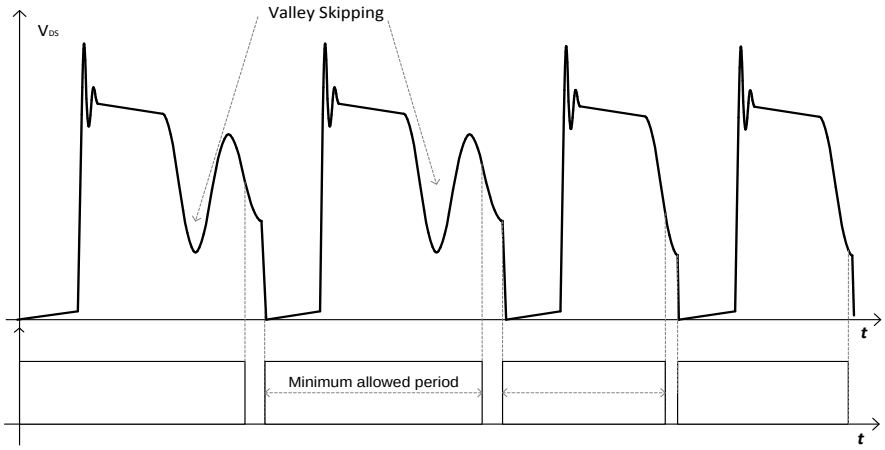


Figure 12 Valley Skipping

Referring to Figure 12, the UCC28910 will operate in a valley skipping mode in most load conditions to maintain an accurate voltage regulation point and still switch on the lowest available V_{DS} voltage.
Valley switching is maintained during constant current regulation to provide improved efficiency and EMI benefits in constant current operation.
In very light load or no load condition the V_{DS} ringing is very low and not easy to detect, moreover with very low ringing amplitude there would be no benefit in valley switching so in this condition the valley switching is disabled (see Figure 13).

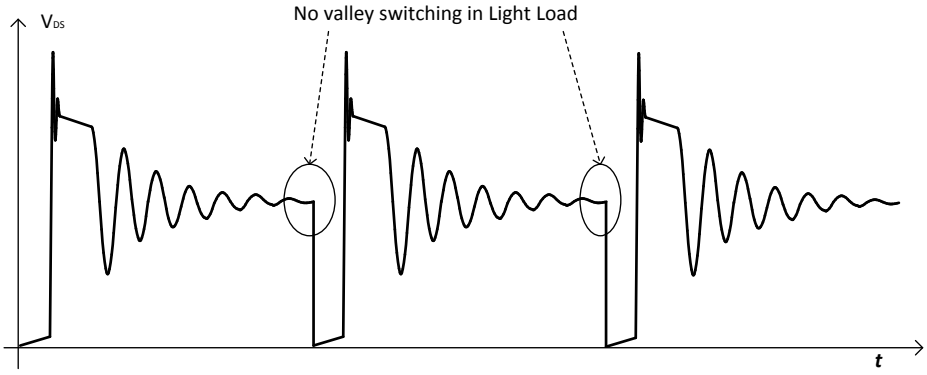


Figure 13 Valley Switching disable at light Load

Start Up Operation

UCC28910 is provided with a high voltage current source, connected between the DRAIN pin and the VDD pin; this current source is activated when a voltage is applied on DRAIN pin. The current source charges the capacitor connected between VDD and GND increasing the VDD voltage. As VDD exceeds VDD_{ON} the current source is turned off and the controller internal logic is activated and the device starts switching. If the VDD voltage falls below the VDD_{OFF} threshold or a fault condition is detected the controller stops operation and its current consumption reduced to I_{START} or I_{FAULT}. The high voltage current source is turned on again when VDD voltage goes below VDD_{HVON} (see figure 14 for reference).
The initial three cycles are limited to $I_{D\_PEAK(max)}$ /3. This allows sensing any input or output faults with minimal power delivery. After the initial three cycles at $I_{D\_PEAK(max)}$/3, the controller responds to the condition dictated by the control law.

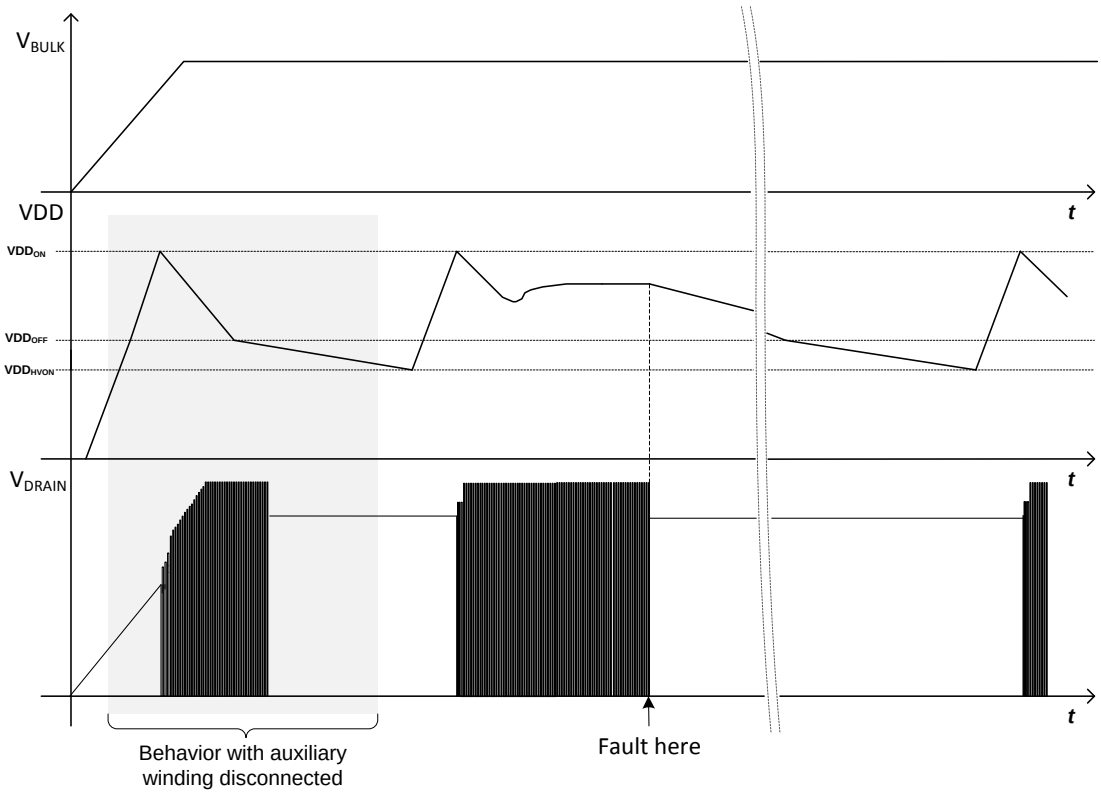


Figure 14 Start up and auto re-start operation

The converter will remain in DCM during charging of the output capacitor(s), and will operate in constant current mode until the output voltage is in regulation.
To avoid high power dissipation inside the device, such as in the event that VDD is accidentally shorted to GND, the current provided by the high voltage current source is reduced (I_{ch1}) until VDD < 1 V (Typ.).

Fault Protection

There is comprehensive fault protection incorporated into the UCC28910. Protection functions include:

- output over-voltage
- input under-voltage
- internal over-temperature
- primary over-current fault
- Max t_{ON} fault
- *VDD* Clamp over current.

Output over-voltage
The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 4.6 V, which correlates to 115% of nominal V_{OUT}, the IC stops switching and reduces its current consumption to I_{FAULT}, slowly discharging the VDD capacitor to the VDD_{HVON} threshold. At this time the standard startup sequence begins. The initial three cycles of startup at low peak DRAIN current is important to monitor V_{OUT} and deliver minimal power. The reset and restart, or hiccup, sequence applies for all fault protection. The slow VDD capacitor discharge after a fault allows the high voltage current source to have a low duty cycle to avoid over heating of the device if a fault condition is continuously present resulting in a repetitious start up sequence.

Input under-voltage

The input under-voltage is determined by current information on the VS pin during the MOSFET on time. The VS pin is clamped close to GND during the MOSFET on time; at this time the current on R_{S1} is monitored to determine a sample of the bulk capacitor voltage. The under-voltage shutdown current on VS is 75μA; the enable current threshold is 210μA. The device must sense the under-voltage condition for three consecutive switching cycles to recognize it as a fault condition. After an under-voltage fault, the same sequence described for output overvoltage occurs.

Thermal shutdown

The internal over-temperature protection threshold is 150^{o}C with a hysteresis of 50^{o}C. If an over-temperature is detected the device stops switching and its current consumption is reduced to I_{FAULT}. The VDD voltage will decrease to VDD_{HVON} where the high voltage current source is activated and the VDD voltage will rise again until VDD_{ON} where the internal logic is re-activated. If the temperature of the device is not dropped below approximately 100^{o}C (150^{o}C- 50^{o}C) no switching cycles occurs and the fault condition is maintained and the current consumption is again I_{FAULT}. For diagnostic purpose, when a thermal shut down occurs a short voltage pulse, whose amplitude is around 2 V, is transmitted on IPK pin.

Primary over-current

The UCC28910 always operates with cycle by cycle primary current control. The normal operating range for the peak DRAIN current depends on the resistance (R_{IPK}) connected between the IPK pin and the GND pin. In normal operation the peak DRAIN current should not exceeds $I_{D\_PEAK(max)}$, if the IPK pin is shorted to GND, or V_{CSTE} / R_{IPK} if the IPK pin is tied to GND with the resistance R_{IPK}. There are different reasons the DRAIN current can go out of control, for example a secondary winding short or hard saturation of the transformer. To avoid over stress of the power FET additional protections are added. If the DRAIN current exceeds I_{DOCP} (~33% higher than $I_{D\_PEAK(max)}$,), such as when IPK pin is shorted to GND, or V_{CSTE_OCP} / R_{IPK}, (V_{CSTE_OCP} ~33% higher than $V_{CSTE(max)}$), and the condition is sensed for three consecutive switching cycles, a fault shutdown and retry sequence, detailed in the output overvoltage fault description, occurs. If the DRAIN current exceeds a 2nd level of current (V_{CSTE_OCP2} / R_{IPK}) it is not necessary to detect the fault for three consecutive switching cycle the device stops switching immediately.

Maximum t_{ON}

An additional protection that limits the power FET on time was added. A timer sets a maximum t_{ON} time that is proportional to the I_{D_PEAK} value established by the control law (see Figure 7). When I_{D_PEAK} is maximum the maximum t_{ON} is $t_{ONMAX(max)}$ (18µs Typ.) if I_{D_PEAK} is minimum the maximum t_{ON} is $t_{ONMAX(min).}$ (6µs Typ.). As the maximum t_{ON} is elapsed the power FET is switched off (if it is still on). If for three consecutive switching cycles the power FET is switched off by the maximujm t_{ON} protection, the device stops switching and sets its consumption low ($I_{VDDFAULT}$) until the next restart.

VDD clamp over-current

The VDD pin is provided with an internal clamp to prevent the pin voltage from exceeding its maximum absolute rating. If the current in the clamp exceeds 5 mA (typ.), in order to avoid any damage to the device and to the system,a fault condition is assumed and the device will stop operation.

Design procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter based on UCC28910 switcher. Refer to the Figure 15 for component names and network locations. The design procedure equations use terms that are defined below.

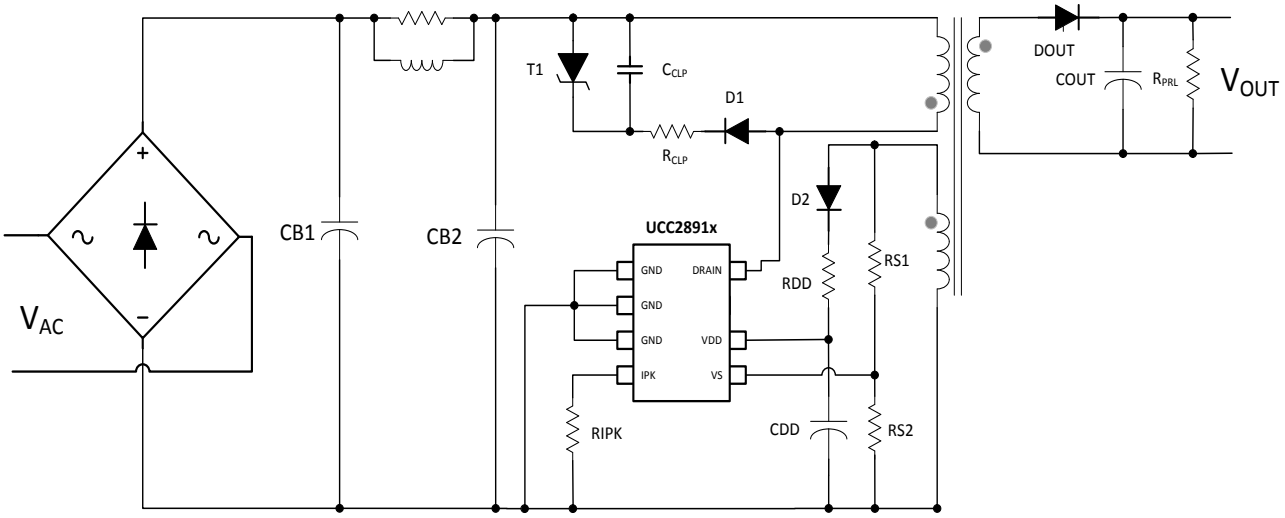


Figure 15 Standard Flyback converter based on UCC28910

Definition of terms

Capacitance Terms in Farads
- C_{BULK}: total input capacitance of C_{B1} and C_{B2}.
- C_{VDD}: capacitance on the VDD pin.
- C_{OUT}: output capacitance.

Duty Cycle Terms
- D_{MAGCC}: secondary diode conduction duty cycle in CC, (equal to K_{CC} see ELECTRICAL CHARACTERISTICS).
- D_{MAX}: MOSFET on-time maximum duty cycle.

Frequency Terms in Hertz
- f_{LINE}: minimum line frequency.
- $f_{TARGET(max)}$: target full-load maximum switching frequency of the converter.
- $f_{(min)}$: minimum switching frequency of the converter, add 15% margin over the $f_{SW(min)}$ limit of the device.
- $f_{SW(min)}$: minimum switching frequency

Current Terms in Amperes
- I_{OCC}: converter output current target when operating in constant current mode.
- $I_{D\_PK(max)}$: maximum transformer primary current which is equal to the $I_{D\_PEAK(max)}$ current if IPK pin is shorted to GND.
- I_{TRAN}: required positive load-step current.
- I_{RUN}: maximum current consumption of the device (see ELECTRICAL CHARACTERISTICS).
- I_{VSLRUN} VS pin run current (see ELECTRICAL CHARACTERISTICS).

Current and Voltage Scaling Terms
- K_{AM}: maximum-to-minimum peak primary current ratio (see ELECTRICAL CHARACTERISTICS).

Transformer Terms
- L_P: transformer primary inductance.
- N_{PA}: transformer primary-to-auxiliary turns ratio.
- N_{PS}: transformer primary-to-secondary turns ratio.

Power Terms in Watts
- P_{IN}: converter maximum input power.
- P_{INTRX}: Transformer maximum input power.

• P_{OUT}: full-load output power of the converter.
• P_{SB}: total stand-by input power.

Resistance Terms in Ω
• R_{IPK}: primary current programming resistance.
• R_{ESR}: total ESR of the output capacitor(s).
• R_{PRL}: preload resistance on the output of the converter.
• R_{S1}: high-side VS pin resistance.
• R_{S2}: low-side VS pin resistance.

Timing Terms in Seconds
• $t_{DMAG(min)}$: minimum secondary rectifier conduction time.
• $t_{ON(min)}$: minimum MOSFET on time.
• t_R: resonant frequency during the DCM (discontinuous conduction mode) time.

Voltage Terms in Volts
• V_{BULK}: highest bulk capacitor voltage for stand-by power measurement.
• $V_{BULK(min)}$: minimum voltage on C_{B1} and C_{B2} at full power.
• V_{CCR}: constant-current regulating voltage (see ELECTRICAL CHARACTERISTICS).
• $V_{O\Delta}$: output voltage drop allowed during the load-step transient.
• V_{DSPK}: peak MOSFET DRAIN-to-source voltage at high line.
• V_F: secondary rectifier forward voltage drop at near-zero current.
• V_{FA}: auxiliary rectifier forward voltage drop.
• V_{OCV}: regulated output voltage of the converter.
• V_{DD}: voltage value on VDD pin.
• V_{OCC}: target lowest converter output voltage in constant-current regulation.
• V_{REV}: peak reverse voltage on the secondary rectifier.
• V_{RIPPLE}: output peak-to-peak ripple voltage at full-load.
• V_{VSR}: CV regulating level at the VS input (see ELECTRICAL CHARACTERISTICS).
• ΔV_{UVLO}: VDD_{ON}-VDD_{OFF} (see ELECTRICAL CHARACTERISTICS).

AC Voltage Terms in V_{RMS}
• $V_{IN(max)}$: maximum AC input voltage to the converter.
• $V_{IN(min)}$: minimum AC input voltage to the converter.
• $V_{IN(run)}$: converter input start-up (run) AC voltage.

Efficiency Terms
• η: converter overall efficiency.
• η_{XFMR}: transformer primary-to-secondary power transfer efficiency.

Maximum Target Switching frequency

The maximum operative switching frequency of the converter should be selected with a trade-off between the efficiency requirement (generally decreasing the switching frequency will improved efficiency because the switching losses are reduced) and transformer size (increasing the switching frequency will result in decreased transformer size). Some limits to the maximum value of the switching frequency need to be taken into account.
First of all, the internal oscillator of the device cannot exceed 130kHz (see $f_{SW(max)}$ in the electrical characteristic section) moreover the demagnetization time cannot be too short ($t_{DMAG(min)}$ > 1µs) in order to allow for the proper working of the discriminator (see Primary Side Voltage Regulation section) and the maximum operative switching frequency is linked to the demagnetization time from the equation below.

$$f_{TARGET(\max)} < \frac{K_{AM} \cdot D_{MAGCC}}{t_{DMAG(\min)}}$$

So the target maximum operative switching frequency of the converter should satisfy to the below condition:

$$f_{TARGET\,(\max)} < MIN\left(\frac{K_{AM}\cdot D_{MAGCC}}{t_{DMAG(\min)}},\, f_{SW(\max)}\right)$$

A good value for $t_{DMAG(min)}$ could be 1.2μs with some margin respect the minimum allowed value

Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM quasi-resonant time. Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume t_R = 1 / 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period, or 1 µs assuming 500-kHz resonant frequency. D_{MAX} can be determined using the equation below.

$$D_{MAX} = 1 - \left(\frac{t_R}{2}\cdot f_{TARGET\,(\max)}\right) - D_{MAGCC}$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below.

$$N_{PS\,(\max)} = \frac{D_{MAX}\cdot V_{BULK\,(\min)}}{D_{MAGCC}\cdot\left(V_{OCV}+V_F\right)}$$

D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current control mode operation. It is set internally by the UCC28910. This is the maximum allowable demagnetizing duty cycle and it is equal to K_{CC}. The total voltage on the secondary winding needs to be determined; it is the sum of V_{OCV} and the secondary rectifier V_F. The voltage $V_{BULK(min)}$ is generally selected around 65% - 60% of $\sqrt{2}\cdot V_{IN\,(\min)}$. $V_{BULK(min)}$ is determined by the selection of the high voltage input capacitors.
For the 5-V USB charger applications N_{PS} values from 13 to 17 are typically used.

Bulk Capacitance

The minimum input capacitance voltage, the input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency are used to determine the input capacitance requirement.
Maximum input power is determined based on V_{OCV}, I_{OCC}, and the full-load efficiency target.

$$P_{IN} = \frac{V_{OCV}\cdot I_{OCC}}{\eta}$$

The following equation provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{\dfrac{2\cdot P_{IN}}{f_{LINE\,(\min)}}\cdot\left\{\dfrac{1}{RCT} - \dfrac{1}{2\cdot\pi}\cdot\arccos\left(\dfrac{V_{BULK\,(\min)}}{\sqrt{2}\cdot V_{IN\,(\min)}}\right)\right\}}{\sqrt{2}\cdot V_{IN\,(\min)}^2 - V_{BULK\,(\min)}^2}$$

In the case the input rectifier is a single diode (half wave rectifier) $RCT = 1$ and $RCT = 2$ for bridge input rectifier (full wave rectifier), as in the schematic of Figure 15.

Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no-load. For example, in USB charger applications it is often required to maintain a minimum output voltage of 4.1 V with a load-step transient from 0 to 500mA (I_{TRAN}). The equation below assumes that the switching frequency can be at the UCC28910 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN}}{V_{O\Delta} \cdot f_{SW(\min)}}$$

Another consideration of the output capacitor(s) is the ripple voltage requirement which is reviewed based on secondary peak current and ESR. A margin of 20% is added to the capacitor ESR requirement in the equation below.

$$R_{ESR} = \frac{V_{RIPPLE}}{I_{D\_PK(\max)} \cdot N_{PS}} \cdot 0.8$$

The above conditions have to be combined with the condition provided in the Primary Side Voltage Regulation section to ensure stability by meeting the conditions below:

$$C_{OUT} \geq \frac{16000uF \cdot (V_{OCV} \cdot I_{OCC})}{f_{(\max)}}$$

VDD Capacitance, C_{VDD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. At this time the auxiliary winding can sustain the supply voltage to the UCC28910. The output current available to the load to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved.

$$C_{VDD} = \frac{C_{OUT} \cdot V_{OCC} \cdot I_{RUN(\max)}}{I_{OCC} \cdot \Delta V_{UVLO}}$$

VS Resistor Divider

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous switching operation. R_{S1} is initially determined based on transformer auxiliary to primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(\min)} \cdot \sqrt{2}}{N_{PA} \cdot I_{VSLRUN(\max)}}$$

The low-side VS pin resistor is selected based on desired output voltage regulation.

$$R_{S2} = \frac{V_{VSR} \cdot R_{S1} \cdot N_{PA}}{(V_{OUT} + V_F) \cdot N_{PS} - (V_{VSR} \cdot N_{PA})}$$

R_{VDD} Resistor and Auxiliary to secondary turn ratio

The R_{VDD} resistor's main task is to decouple the VDD voltage from the voltage across the secondary winding during the transformer demagnetization. The higher this resistor value is, the lower is the effect of the VDD voltage on the sensed VS voltage and better precision is obtained in sensing V_{OUT}. Typical values of R_{VDD} range from 15Ω to 47Ω.
The value of R_{VDD} and the Auxiliary to secondary turns ratio should be selected with care in order to be sure that the VDD is always higher then the VDD_{OFF} (7V Max) threshold under all operating conditions. The R_{VDD} resistor also limits the current that can go into the VDD pin preventing I_{VDDCLP_OC} clamp over current protection from being erroneously activated.

Transformer Input Power

The power at the transformer input during full load condition is given by the output power plus the power loss in the output diode plus the power consumption of the UCC28910 control logic ($V_{VDD} \cdot I_{RUN}$) divided by the transformer efficiency that takes into account all the losses due to the transformer: copper losses, core losses, and energy loss in the leakage inductances.

$$P_{INTRX} = \frac{\left(V_{OCV} + V_F\right) \cdot I_{OCC} + V_{VDD} \cdot I_{RUN}}{\eta_{XFMR}}$$

R_{IPK} Value

The R_{IPK} value sets the value of the DRAIN current peak that equals the transformer primary winding current peak value. This value also sets the value of the output current when working in CC mode according to the following formula:

$$I_{OUT} = \left(\sqrt{\eta_{XFMR} - \frac{2 \cdot V_{VDD} \cdot I_{RUN}}{P_{INTRX}}} \right) \cdot N_{PS} \cdot \frac{1}{2} \cdot I_{D\_PK(\max)} \cdot D_{MAGCC}$$

Where:

D_{MAGCC} is the secondary diode conduction duty cycle and it is fixed by the controller (see K_{CC} in electrical characteristic tables)

N_{PS} is the Primary to secondary transformer turns ratio

The term $\left(\sqrt{\eta_{XFMR} - \frac{2 \cdot V_{VDD} \cdot I_{RUN}}{P_{INTRX}}} \right)$ takes into account that not all the energy stored in the transformer goes to the secondary side but some of this energy, through the auxiliary winding, is used to supply the IC control logic. The transfer of energy always happens with unavoidable losses. These losses are accounted for through the transformer efficiency term (η_{XFMR}).
The value of R_{IPK} can be calculated using the following formula:

$$R_{IPK} = \left(\sqrt{\eta_{XFMR} - \frac{2 \cdot V_{VDD} \cdot I_{RUN}}{P_{INTRX}}} \right) \cdot N_{PS} \cdot \frac{1}{2} \cdot \frac{V_{CCR}}{I_{OUT}}$$

Where V_{CCR} is an UCC28910 internal parameter specified in the Electrical specification tables that takes into account the relation between $I_{D\_PK(max)}$ R_{IPK} and D_{MAGCC}.

Primary inductance value

After you have fixed the maximum switching frequency and the maximum value of the primary current peak for your application, the primary inductance value can be fixed by the following equation:

$$L_{P(\min)} = \frac{2 \cdot P_{INTRX}}{\left(1 - L_P\_Tol\right) \cdot f_{TARGET(\max)} \cdot I^2_{D\_PK(\max)}}$$

L_{P}_Tol is the tolerance on the primary inductance value of the transformer. Typical values of *L_{P}_Tol are* between ±10% and ±15%)

Secondary diode selection

The maximum reverse voltage that the secondary diode had to sustain can be calculated by the equation below where a margin of 30% is considered. Usually for this kind of application a Schottky diode is used to reduce the power losses due to the lower forward voltage drop. The maximum current rating of the diode is generally selected between 2 and 5 times the maximum output current (I_{OCC}).

$$V_{REV} = \left(V_{OCV} + \frac{V_{IN(\max)} \cdot \sqrt{2}}{N_{PS}} \right) \cdot 1.3$$

Pre-Load

When absolutely no load is applied on the converter output, the output voltage will rise until the OVP (over voltage protection) of the device is tripped, because the device cannot operate at zero switching frequency. To avoid this, an R_{PRL} (Pre-Load resistance) is used. The value of this preload can be selected using the following equation:

$$R_{PRL} = \frac{V_{OCV}^2}{\frac{\eta_{XFMR}}{2} \cdot L_P \cdot (1 + L_P\_Tol) \cdot f_{(\max)} \cdot \left(\frac{I_{D\_PK(\max)}}{K_{AM}} \right)^2 - VDD_{OFF(\max)} \cdot I_{WAIT}}$$

DRAIN Voltage Clamp Circuit

The main purpose of this circuit, as in the most flyback converters, is to prevent the DRAIN voltage from rising up to the FET break down voltage, at the FET turn-off, and destroying the FET itself. An additional task, required by the primary side regulation mechanism, is to provide a clean input to UCC28910 VS pin by damping the oscillation that is typically present on the DRAIN voltage due to the transformer primary leakage inductance.

To perform damping, the D1 diode selected is not a fast recovery diode (0.3µs < t_{rr} < 1 µs) so the reverse current can flow in the RLC over damped circuit. This RLC circuit is formed by the transformer primary leakage inductance (L_{LKP}), the resistance R_{CLP}, and the capacitance C_{CLP}. To ensure proper damping the resistance R_{CLP} has to satisfy the following condition:

$$R_{CLP} > 2 \cdot \sqrt{\frac{L_{LKP}}{C_{CLP}}}$$

The capacitance C_{CLP} should not be too high so it does not require too much energy to be charged. Typical values for C_{CLP} are between 100pF and 1nF.

If the R_{CLP} is too high, the additional drop on this resistance can cause excessively high DRAIN voltage. The DRAIN clamp circuit of Figure 15 can be modified as shown in the figure below where the resistor R_{CLP} was divided in two resistances. The resistance R_{DCH} can be added to discharge the C_{CLP} capacitance if necessary.

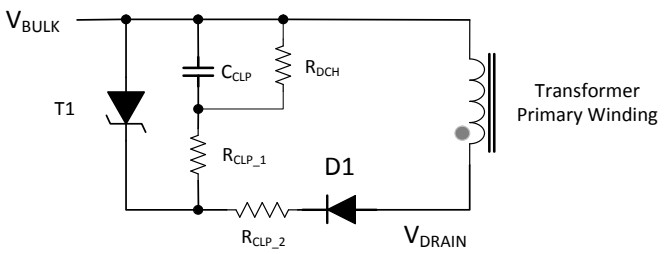
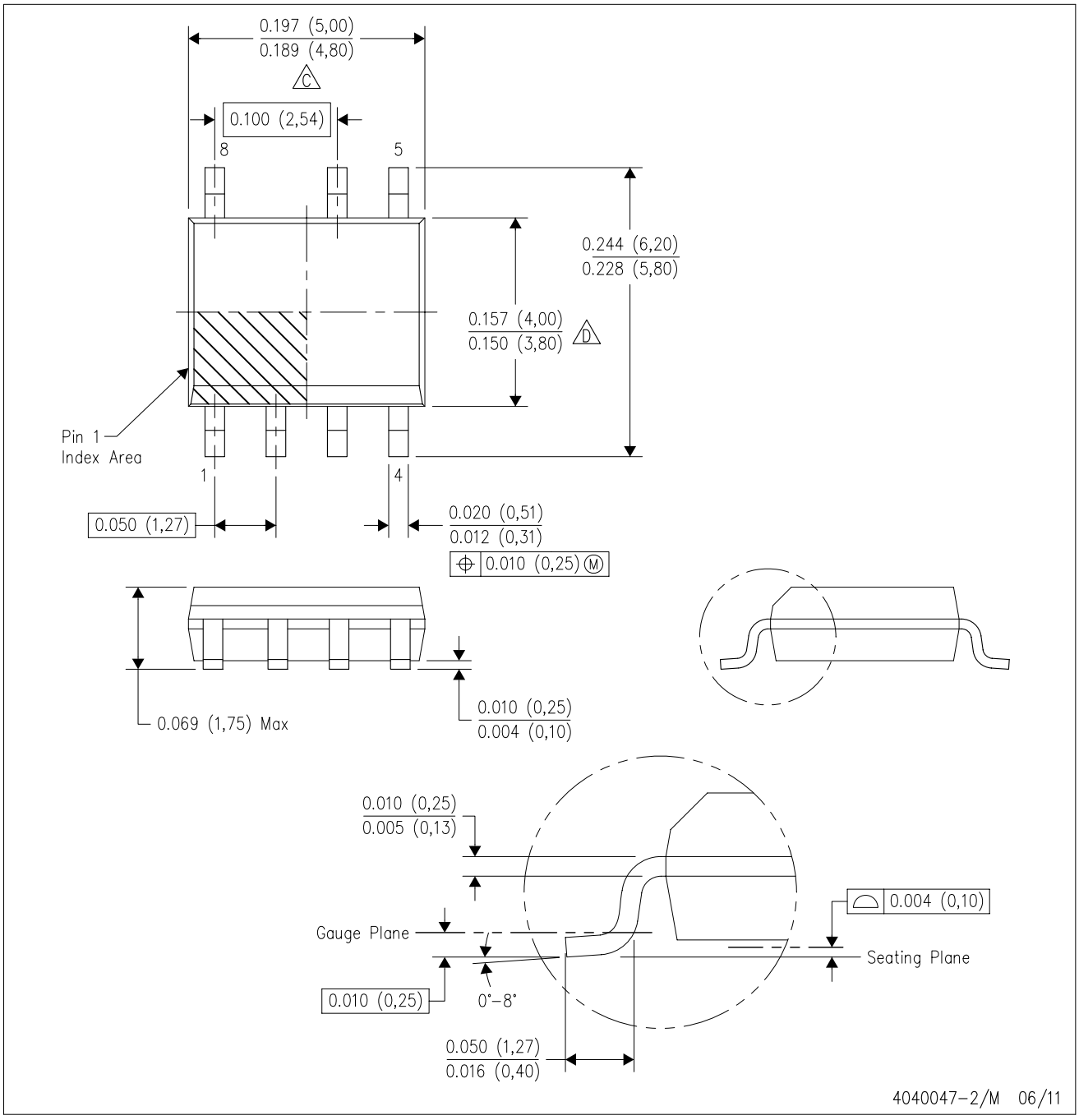


Figure 16 DRAIN Clamp circuit options

Revision History Table

Date	Added	Modified	Notes
Oct. – 12 - 2012	• IDD consumption picture • Formulas for DMAX and NPS max. • T_{ON} max Protection Description • Definition of terms table	Control Law picture	Definition of terms table to be checked.
Oct. – 26 - 2012	• Added DRAIN Pin Section	• Modified Formulas in VS Pin Section • Modified IPK Pin Section • Modified Control Law profile Picture • Modified Typical V-I Char picture	
Nov – 23 - 2012		• Specified Test condition T_J = 25 ºC for $I_{leakage}$ • Specified test condition I_D = 20µA for BV_{DSS}	
Nov – 27 - 2012	• RDD resistor and Aux to secondary turn ratio section • RIPK value section		Definition of terms table to be checked.
Dic – 03 - 2012		• Modified RIPK section	
Dic – 04 – 2012	• Primary inductance value • Secondary diode selection.		
Dic. – 11 - 2012	• Added V_{CSTE_OCP2} parameter on protection table		
Jan. – 22 - 2013		Just some grammar corrections	
Feb. – 11 - 2013	• Added Secondary Diode Section • Added Pre-Load selection section • Added DRAIN Voltage Clamp Circuit Section	Modified Definition of terms section	
Feb. – 28 - 2013	• Added picture on VDD cycling in auto restart	• Modification according to LD comments and based on observations done during Datasheet review meeting	
Mar. – 07 - 2013	• Eliminated V_{VS} line in recommended operating condition	• Moved Start up current source table close to Under Voltage Lock Out Section • Modified Limits for R_{IPK} • Added Test condition for $I_{D\_PEAK(max)}$ (TJ = 25C)	
May - 09 - 2013	• Added operative recommended maximum T_A in the recommended values table. • Added note (5) to explain why the recommended T_A is limited.	• Modified Maximum Switching Frequency. Maximum fsw is now 115kHz (typ.) • Modified Minimum Switching Frequency. Minimum fsw is now 420 Hz (typ.)	

D (R–PDSO–G7) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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