SONY

# CXA1106P/M

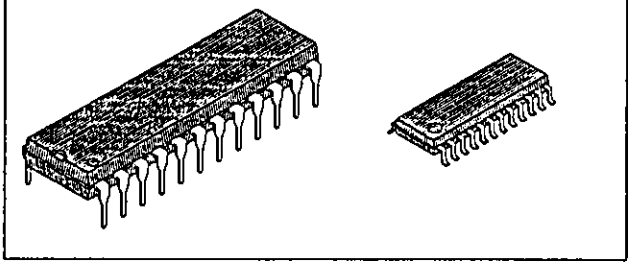
## 8-bit 35 MSPS High-Speed D/A Converter

### Description

CXA1106P/M is an 8-bit 35MSPS high-speed D/A converter IC. Summing type current for the upper 2-bits and ladder type resistance for the lower 6-bits, ensure a low power consumption of 200 mW (Single power supply).
This IC is suitable for digital TV's, graphic displays and other applications.

CXA1106P
24 pin DIP (Plastic)

CXA1106M
24 pin SOP (Plastic)



### Features

- Resolution 8-bit
- High speed operation
  35MSPS (Max. conversion speed)
- Non linear error
  less than ±1/2LSB
- Low glitch
- TTL compatible input
- +5V single power supply or ±5V dual power supply
- Low power consumption

| | |
|---|---|
| +5V single power supply | 200 mW (Typ.) |
| ±5V dual power supply | 400 mW (Typ.) |

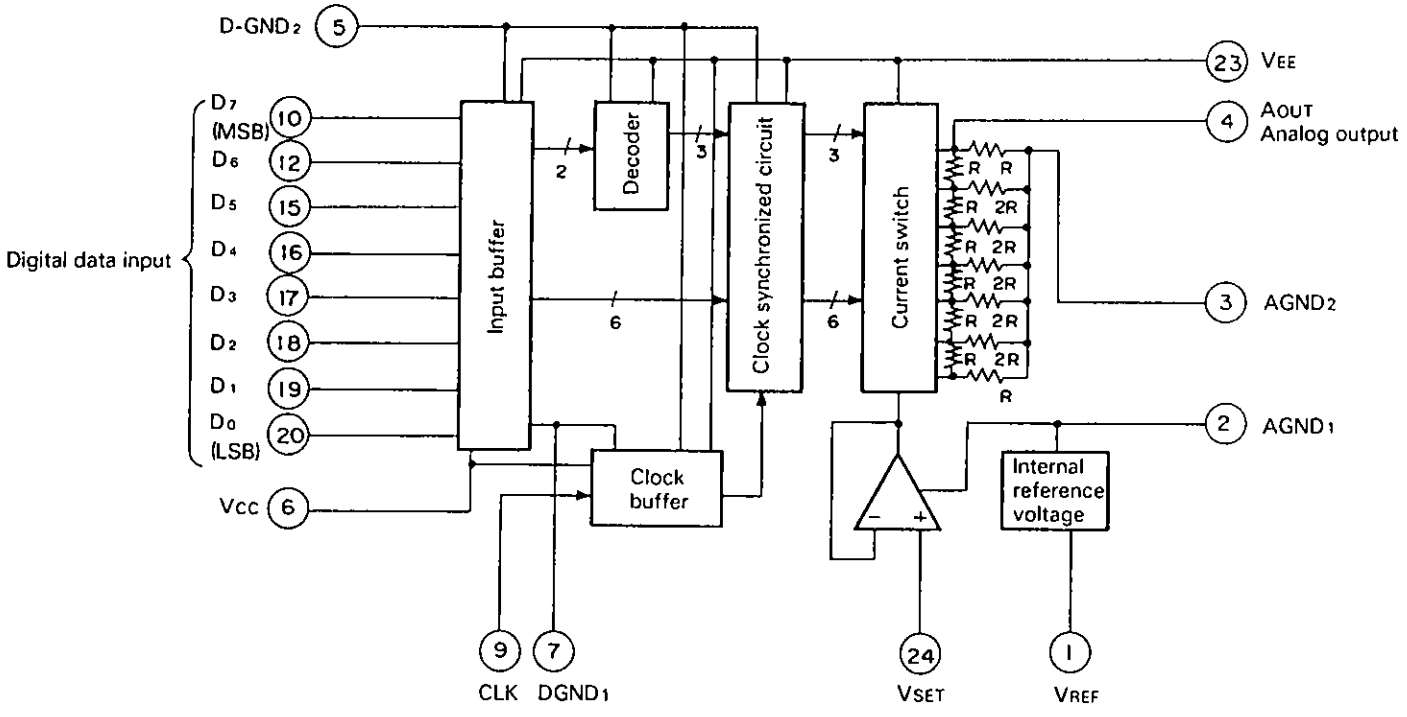
### Function

8-bit 35 MSPS D/A converter

### Structure

Bipolar silicon monolithic IC

### Block Diagram






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## Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{CC}$-DGND1 | 0 to 6 | V |
| | $V_{EE}$–AGND1,2 | −6 to 0 | V |
| | DGND2–DGND1 | 0 to 6 | V |
| • Digital input voltage | $V_I$ | DGND1−0.3 to $V_{CC}$+0.3 | V |
| | $V_{CLK}$ | DGND1−0.3 to $V_{CC}$+0.3 | V |
| • Input voltage ($V_{SET}$ pin) | $V_{SET}$ | $V_{EE}$−0.3 to $V_{EE}$+2.7 | V |
| • Output current ($V_{REF}$ pin) | $I_{REF}$ | −5 to 0 | mA |
| • Operating temperature | Topr | −20 to +75 | °C |
| • Storage temperature | Tstg | −55 to +150 | °C |
| • Allowable power dissipation | PD | 1.27 | W |

## Recommended Operating Conditions

### Single power supply

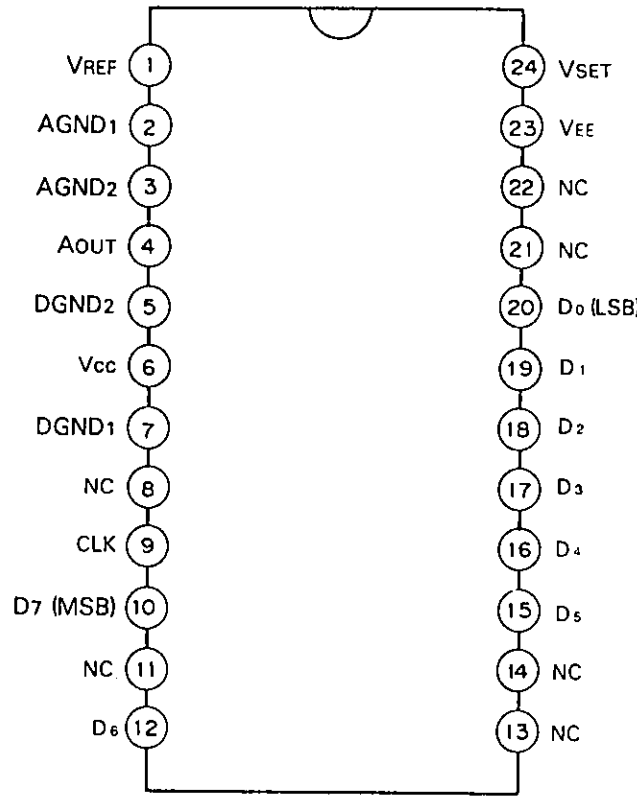
| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$, DGND2 AGND1, AGND2 | 4.75 | 5.00 | 5.25 | V |
| | | DGND2–AGND1 DGND2–AGND2 | −0.2 | 0 | 0.2 | V |
| | | AGND1–AGND2 | −0.1 | 0 | 0.1 | V |
| Digital input voltage | H level | $V_{IH}$, $V_{CLKH}$ | 2.0 | | VCC | V |
| | L level | $V_{IL}$, $V_{CLKL}$ | DGND1 | | 1.0 | V |
| $V_{SET}$ input voltage | | $V_{SET}$ | 0.70 | 0.84 | 1.0 | V |
| $V_{REF}$ pin current | | $I_{REF}$ | −3.0 | | −0.4 | mA |
| Clock pulse width* | | $T_{PW1}$ | 10 | | | ns |
| | | $T_{PW0}$ | 10 | | | ns |

***Note)** See Fig. 6. Timing chart

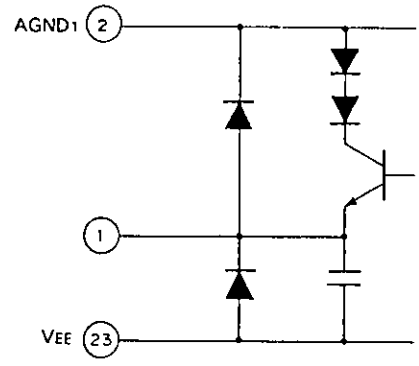
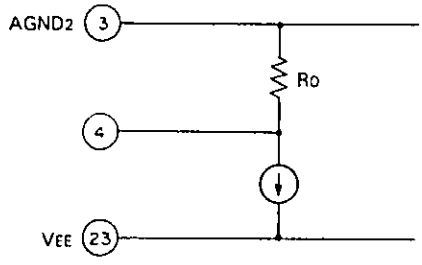
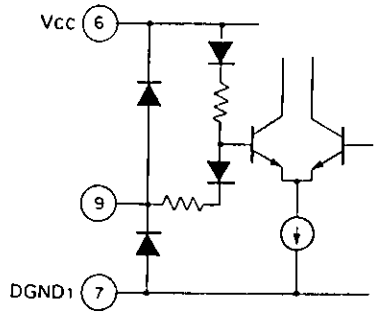
### Dual power supply

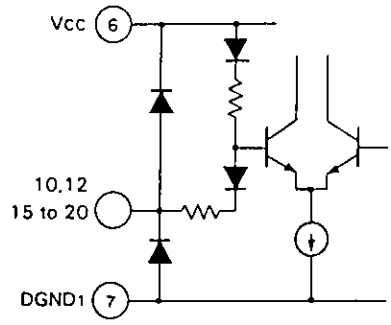
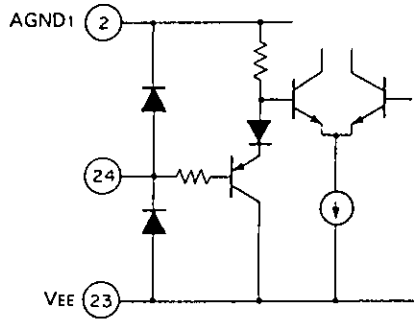
| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| | | $V_{EE}$ | −5.5 | 5.00 | −4.75 | V |
| | | DGND2–AGND1 DGND2–AGND2 | −0.2 | 0 | −0.2 | V |
| | | AGND1–AGND2 | −0.1 | 0 | 0.1 | V |
| Digital input voltage | H level | $V_{IH}$, $V_{CLKH}$ | 2.0 | | Vcc | V |
| | L level | $V_{IL}$, $V_{CLKL}$ | DGND1 | | 1.0 | V |
| $V_{SET}$ input voltage | | $V_{SET}$ | −4.30 | −4.16 | −4.00 | V |
| $V_{REF}$ pin current | | $I_{REF}$ | −3.0 | | −0.4 | mA |
| Clock pulse width | | $T_{PW1}$ | 10 | | | ns |
| | | $T_{PW0}$ | 10 | | | ns |

## Pin Configuration (Top View)



## Pin Description

| No. | Symbol | Equivalent circuit | Description |
|---|---|---|---|
| 1 | $V_{REF}$ |  | Internal reference voltage output pin 1.2 V (Typ.) An external pull down resistance is necessary. For reference see Notes on Application 1 on page 15. |
| 2 | $AGND_1$ | | Set to Analog Vcc for single power supply and to Analog GND for dual power supply. Connect to $AGND_2$ and use. |
| 3 | $AGND_2$ | | Connect to $AGND_1$ |
| 4 | $A_{OUT}$ |  | Analog output pin |
| 5 | $DGND_2$ | | Set to Digital Vcc for single power supply and to Digital GND for dual power supply. |
| 6 | $V_{CC}$ | | Digital Vcc |
| 7 | $DGND_1$ | | Digital GND |
| 8 | NC | | Non-connection |
| 9 | CLK |  | Clock input pin |

| No. | Symbol | Equivalent circuit | Description |
|---|---|---|---|
| 10, 12, 15 to 20 | $D_7$, $D_6$, $D_5$ to $D_0$ |  | Digital input pin<br>$D_1$ to MSB, $D_8$ to LSB |
| 11, 13, 14 | NC | | Non-connection |
| 21, 22 | NC | | Non connection pin. But connect to AGND or $V_{EE}$ |
| 23 | $V_{EE}$ | | Set to Analog GND for single power supply and to $V_{EE}$ for dual power supply. |
| 24 | $V_{SET}$ |  | Bias input pin<br>Normally set $V_{SET} - V_{EE}$ to 0.84V. For reference see Notes on Application 1. |

See the Application Circuit for reference.

## Electrical Characteristics (Ta = 25°C)

**Single power supply**

$V_{CC}$ = DGND2 = AGND1 = AGND2 = 5V, DGND1 = $V_{EE}$ = 0, $V_{SET}$ = 0.84V

| Item | | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | | n | | | 8 | | bit |
| Maximum conversion speed | | $f_{MAX}$ | $R_L$ > 10kΩ, $C_L$ < 20pF | 35 | | | MSPS |
| Linearity error | | $E_L$ | $R_L$ > 10 KΩ | −0.5 | | +0.5 | LSB |
| Differential linear error | | $E_D$ | | −0.5 | | +0.5 | LSB |
| Full scale output voltage | | $V_{FS}$ | $R_L$ > 10KΩ | 0.9 | 1.0 | 1.1 | V |
| Offset voltage* | | $V_{OS}$ | $R_L$ > 10KΩ | 0 | 4 | 10 | mV |
| Output resistance | | $R_O$ | | 290 | 350 | 410 | Ω |
| Power supply current | | $I_{CC}$ | $R_L$ > 10KΩ<br>$I_{REF}$ = −400μA | 32 | 40 | 48 | mA |
| Digital input current | H level | $I_{IH}$ | | 0 | | 5 | μA |
| | L level | $I_{IL}$ | | −400 | | 0 | μA |
| $V_{SET}$ input current | | $I_{SET}$ | | −3 | | 0 | μA |
| Internal reference output voltage | | $V_{REF}$ | $I_{REF}$ = −400μA | 1.17 | 1.25 | 1.33 | V |
| Accuracy output voltage range | | $V_{OC}$ | $R_L$ > 10KΩ | 0.5 | 1.0 | 1.5 | V |
| Set up time | | $t_s$ | | 10 | | | ns |
| Hold time | | $t_h$ | | 2 | | | ns |
| Propagation delay time | | $t_{PD}$ | $R_L$ > 10KΩ | | 11 | | ns |
| Glitch energy | | GE | $R_L$ > 10KΩ<br>$f_{CLK}$ = 1 MHz<br>Digital lamp output | | 30 | | pV-s |

***Note)** $V_{OS}$ = AGND2 − $V_{255}$ ($V_{255}$ is the output voltage when full input is at high level)

**Dual power supply**

$V_{CC}$ = 5V, DGND1 = DGND2 = AGND1 = AGND2 = 0, $V_{EE}$ = −5V, $V_{SET}$ − $V_{EE}$ = 0.84V

| Item | | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | | n | | | 8 | | bit |
| Maximum conversion speed | | $f_{MAX}$ | $R_L$ > 10kΩ, $C_L$ < 20pF | 35 | | | MSPS |
| Linearity error | | $E_L$ | $R_L$ > 10 KΩ | −0.5 | | +0.5 | LSB |
| Differential linear error | | $E_D$ | | −0.5 | | +0.5 | LSB |
| Full scale output voltage | | $V_{FS}$ | $R_L$ > 10KΩ | 0.9 | 1.0 | 1.1 | V |
| Offset voltage | | $V_{OS}$ | $R_L$ > 10KΩ | 0 | 4 | 10 | mV |
| Output resistance | | $R_O$ | | 290 | 350 | 410 | Ω |
| Power supply current | | $I_{CC}$ | $R_L$ > 10KΩ<br>$I_{REF}$ = −400μA | 24 | 30 | 36 | mA |
| | | $I_{EE}$ | | 40 | 50 | 60 | mA |
| Digital input current | H level | $I_{IH}$ | | 0 | | 5 | μA |
| | L level | $I_{IL}$ | | −400 | | 0 | μA |
| $V_{SET}$ input current | | $I_{SET}$ | | −3 | | 0 | μA |
| Internal reference output voltage | | $V_{REF}$ | $I_{REF}$ = −400μA | −3.83 | −3.75 | −3.67 | V |
| Accuracy output voltage range | | $V_{OC}$ | $R_L$ > 10KΩ | 0.5 | 1.0 | 1.5 | V |
| Set up time | | $t_s$ | | 10 | | | ns |
| Hold time | | $t_h$ | | 2 | | | ns |
| Propagation delay time | | $t_{PD}$ | $R_L$ > 10KΩ | | 11 | | ns |
| Glitch energy | | GE | $R_L$ > 10KΩ<br>$f_{CLK}$ = 1 MHz<br>Digital lamp output | | 30 | | pV-s |

## Input/Output Chart (when output full scale voltage at 1.00 V)

**Table 1**

| Input code | | | | | | | | Output voltage (Single supply) | Output voltage (dual supply) |
|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Vcc | −0V |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Vcc −0.5V | −0.5V |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Vcc −1.0V | −1.0V |

## Electrical Characteristics Test Circuit

### DC characteristics

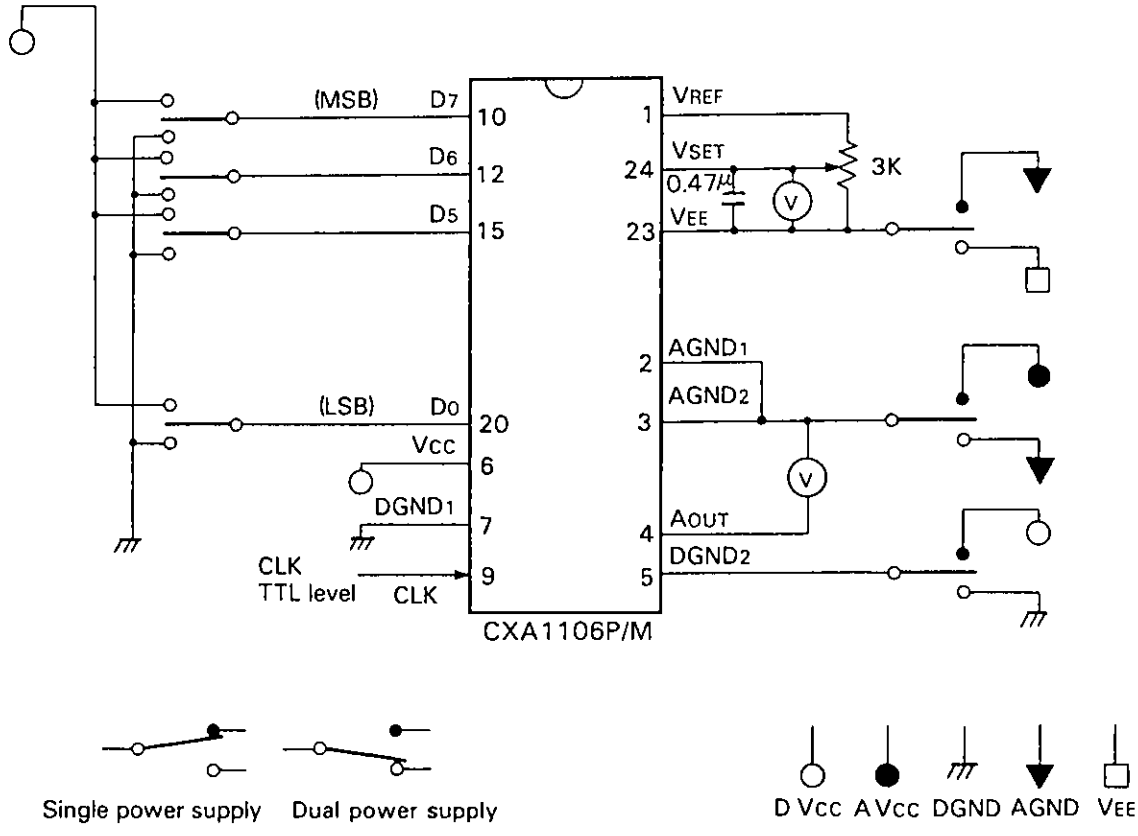
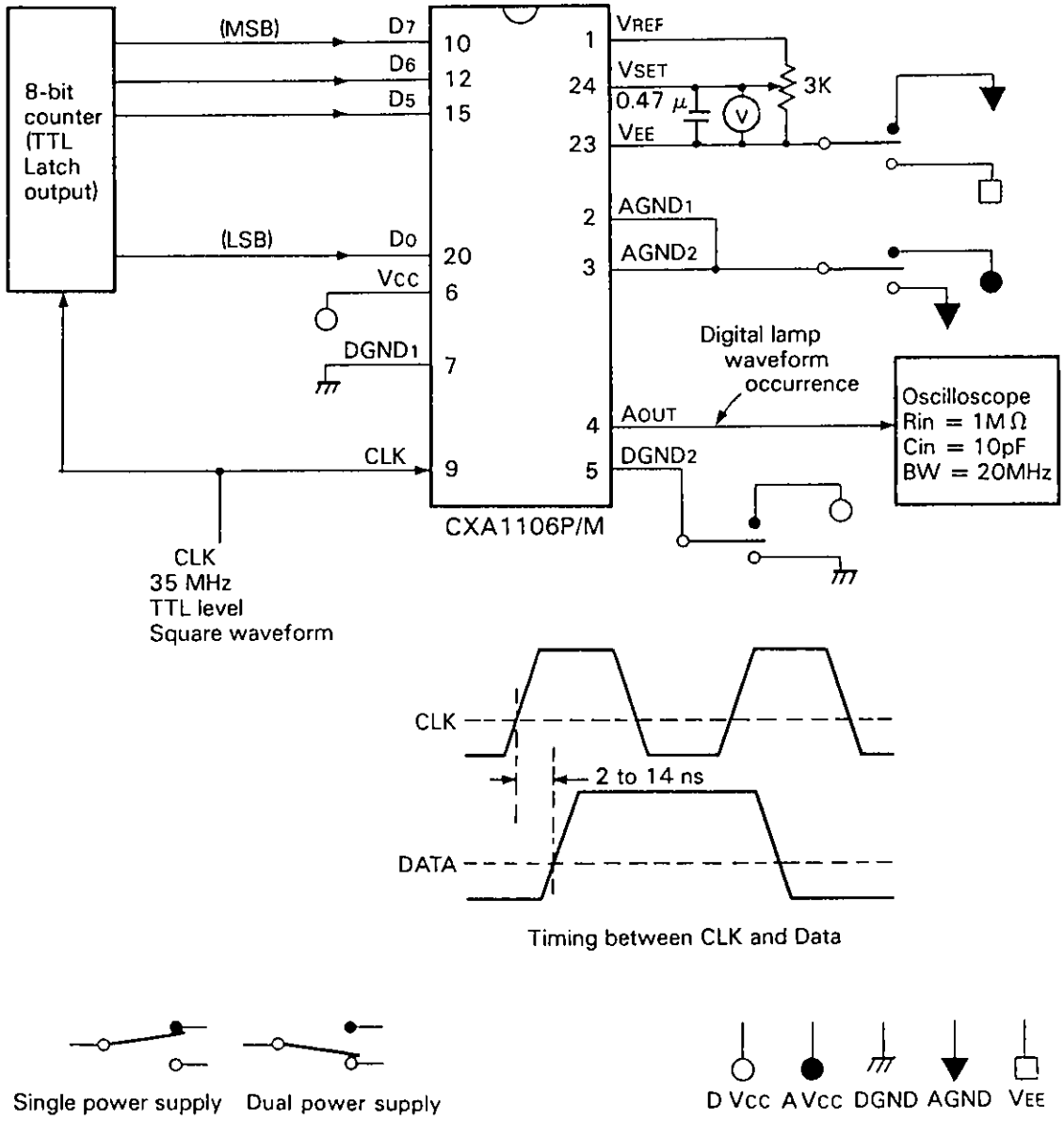



**Fig. 1**

## Test Circuit for Maximum Conversion Speed







Timing between CLK and Data



Single power supply Dual power supply




**Fig. 2**

## Test Circuit for Set-up Time, Hold Time

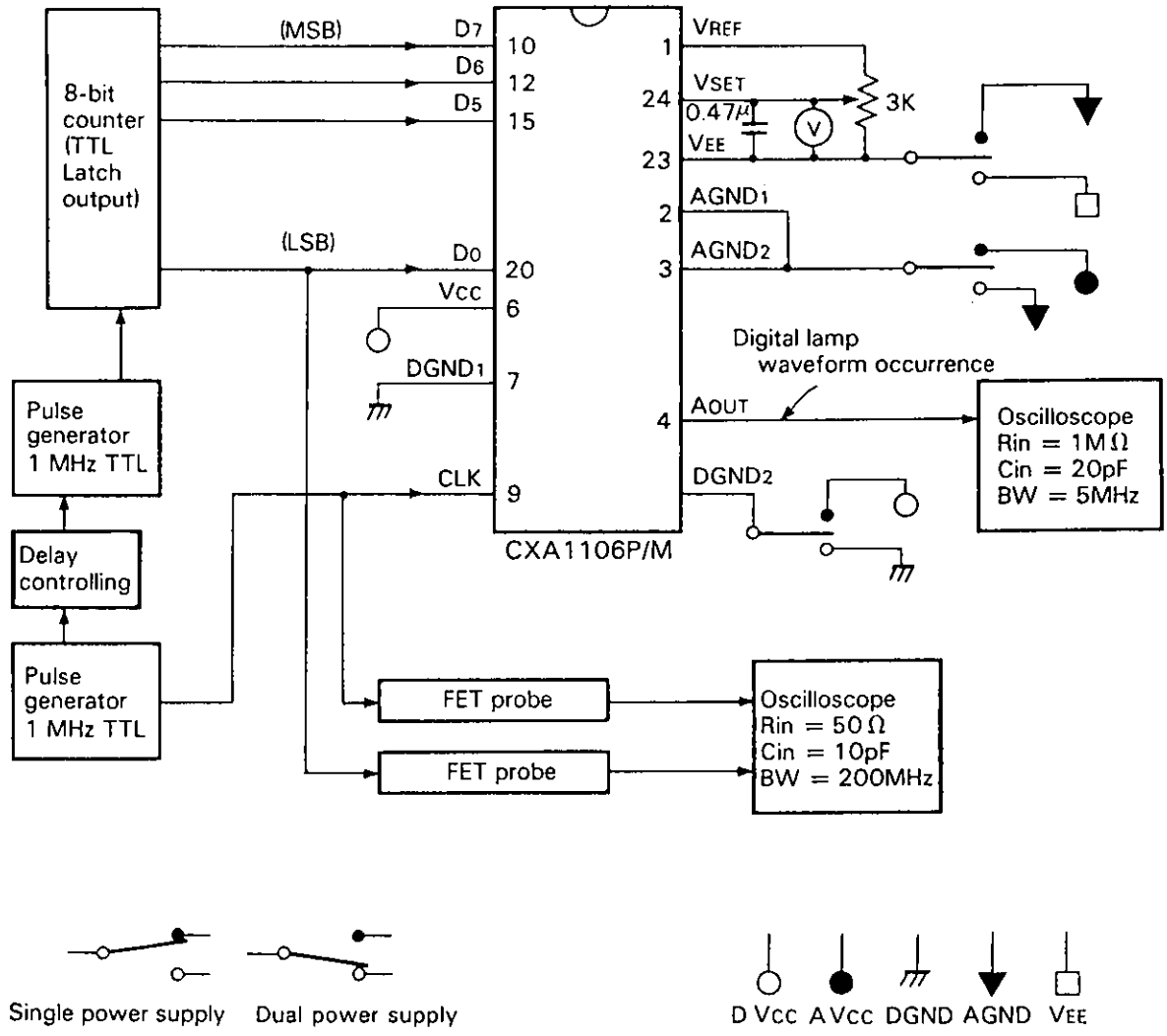
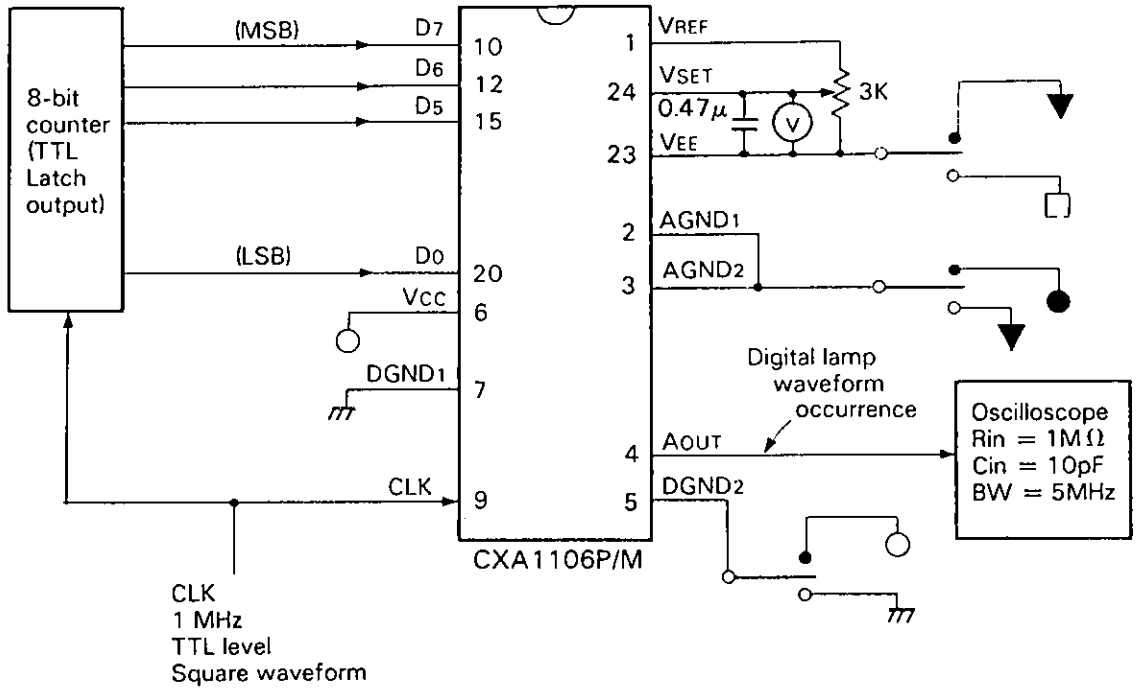
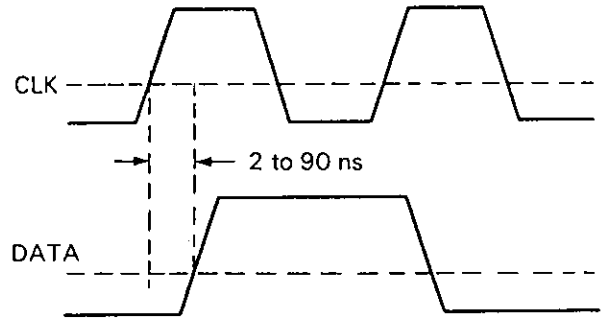


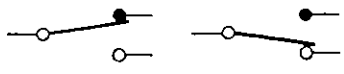

Fig. 3

## Test Circuit for Glitch Energy




Timing between CLK and Data

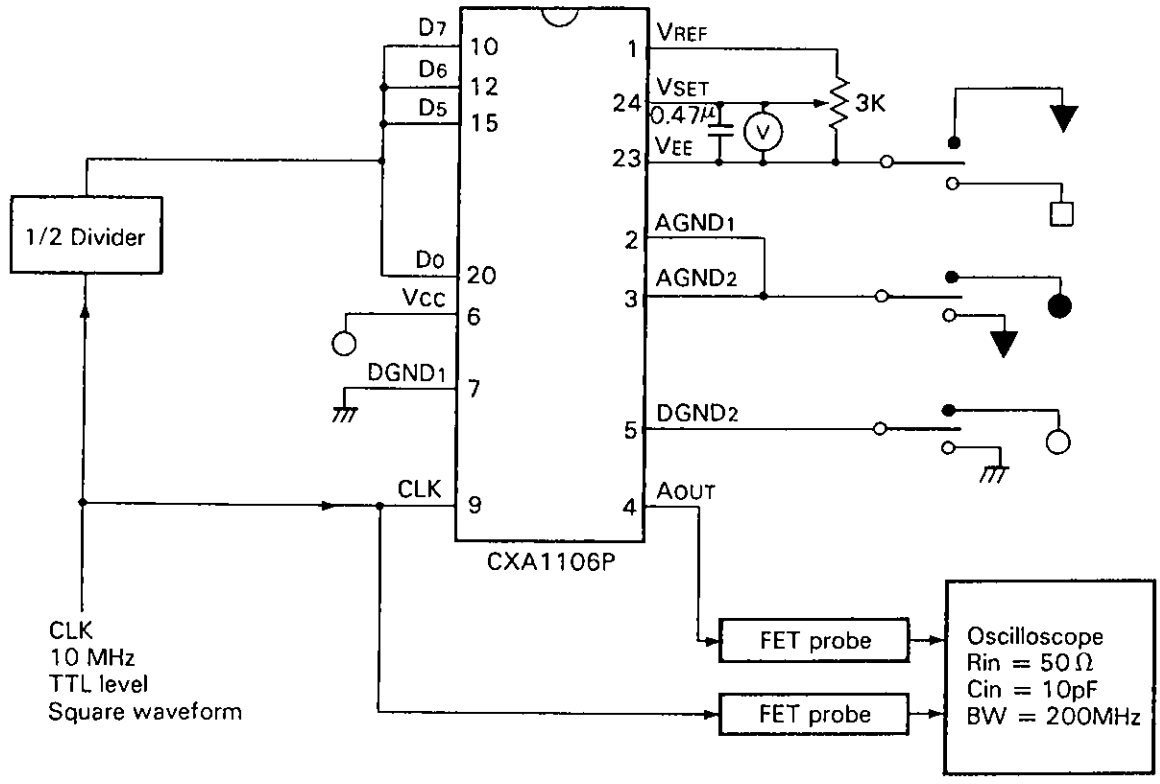


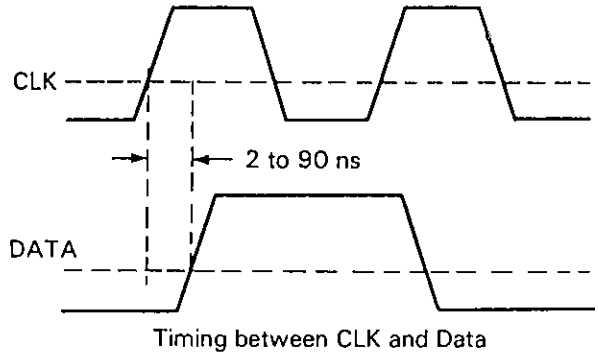
Single power supply  Dual power supply



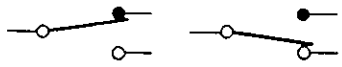

Fig. 4

## Test Circuit for Propagation Delay Time




Timing between CLK and Data



Single power supply  Dual power supply




**Fig. 5**

## Operation

### Timing chart

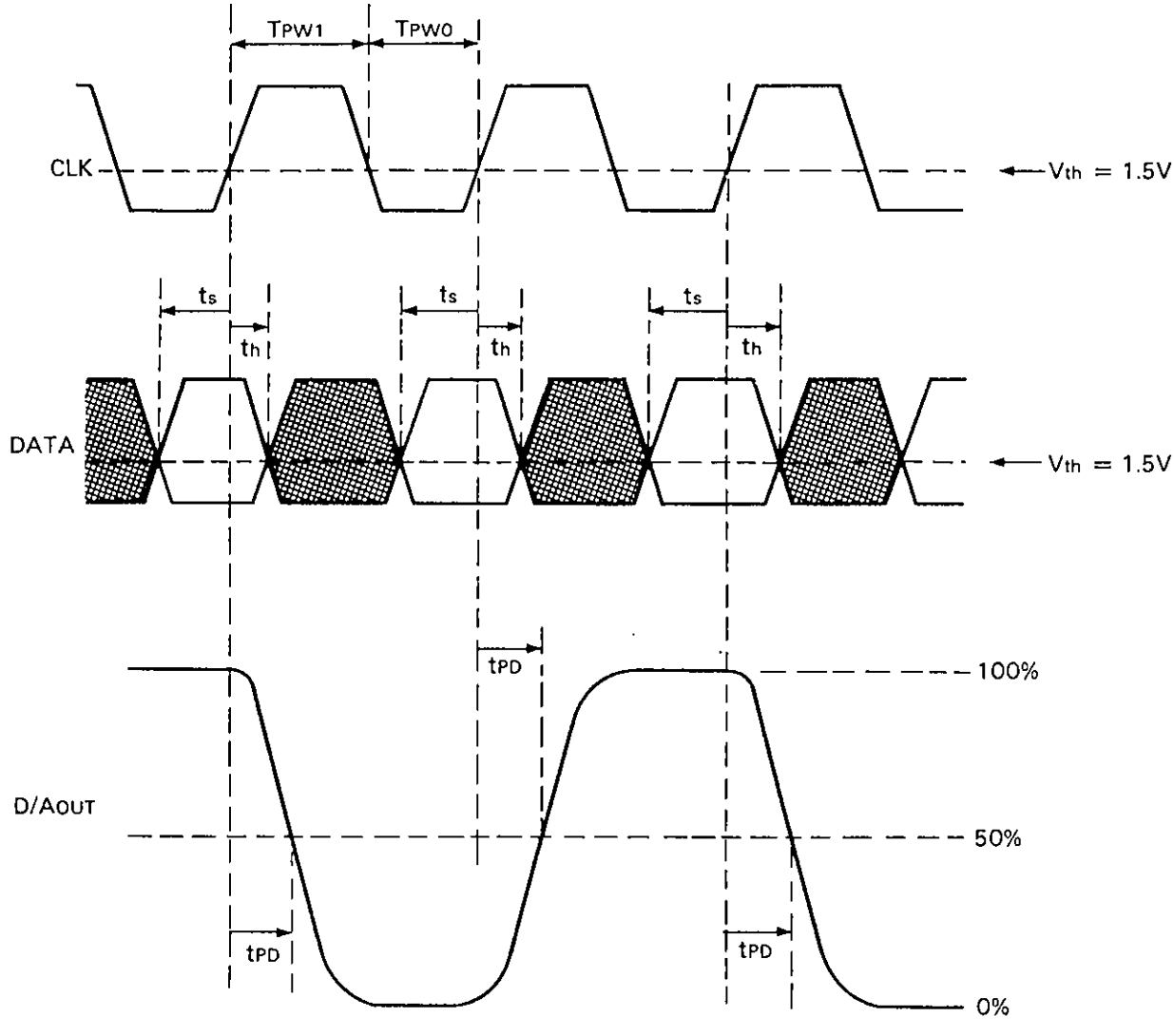
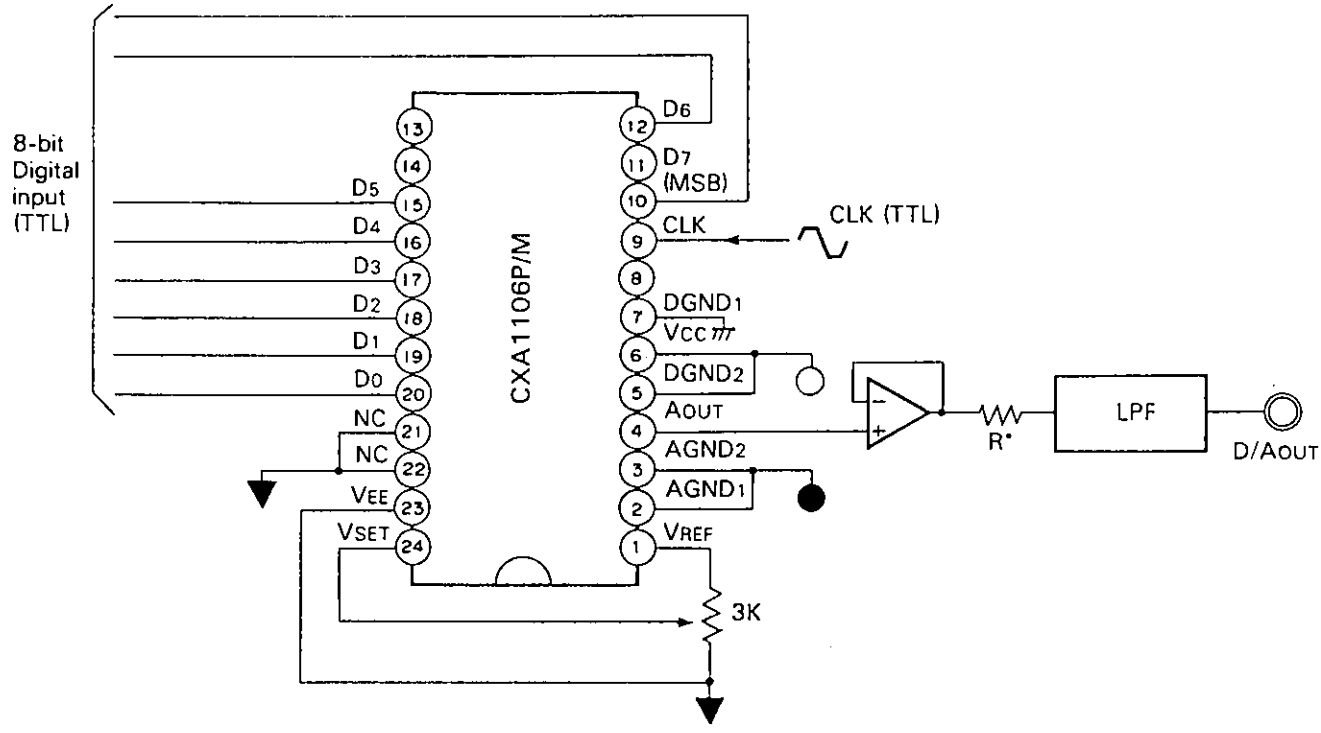


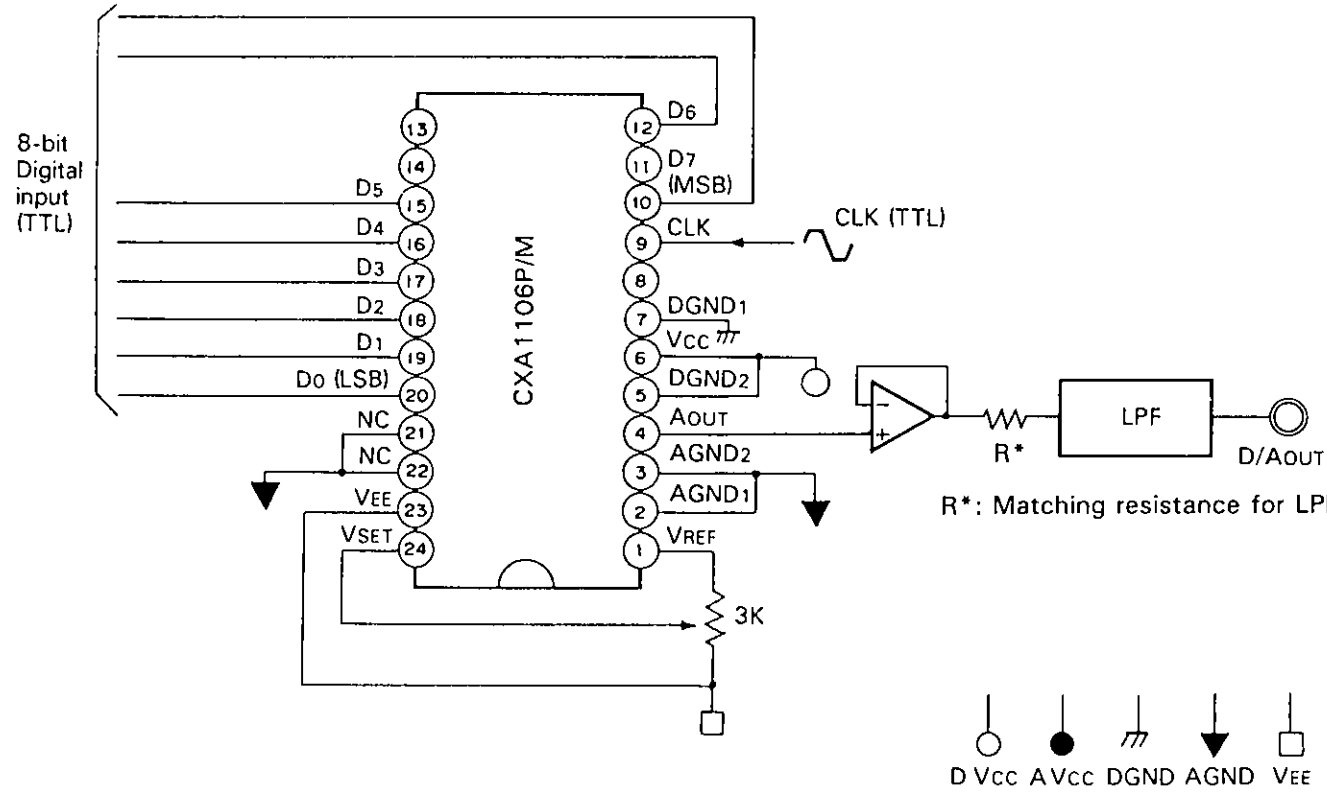

Fig. 6

## Application Circuits

Single power supply




Dual power supply



## Notes on Application

1. Setting of VSET Pin (Pin 24)

   The full-scale voltage of the D/A output is determined by VSET input voltage. As about (1.2V - VEE) DC voltage is generated at VREF pin (Pin 1) by connecting an external resistor from VREF pin to VEE pin (Pin 23), divide this voltage using resistors and apply it to VSET pin as Fig. 7.

(Example of usage)

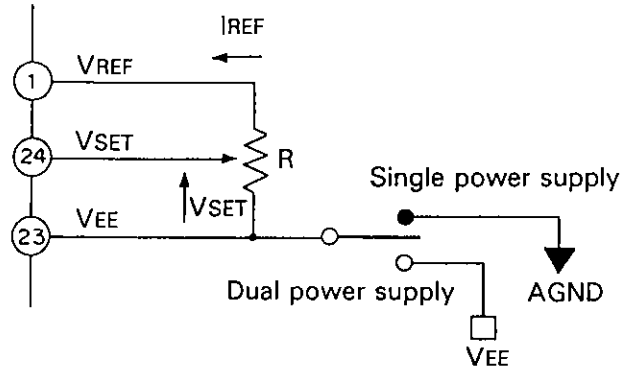



Fig. 7

The full-scale voltage of the D/A output can be determined from the following equation.

$V_{FS} = 1.2\ (V_{SET} - V_{EE})$ ($R_L > 10K\Omega$, $0.4V \leq V_{SET} \leq 1.2V$)

Select an external resistor R (Connected to VREF pin) so that IREF (current of an external resistor) is within the value indicated as the Recommended Operational Conditions ($-3$ mA $< I_{REF} < -0.4$ mA).

2. Phase relation between Data and Clock

   To make the best use of the inherent characteristics of this D/A converter the phase relation between the data and clock applied from the exterior, should be properly set.
   Set up time (ts) and Hold time (th) should be as indicated in the Electrical characteristics. For ts and th refer to Fig. 6 in the Timing Chart.
   Also, set the clock pulse width according to the Recommended Operating Conditions.

3. D/A output pin Load

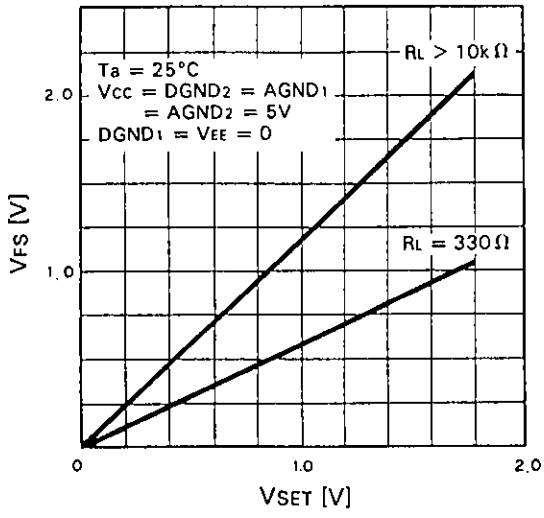
   Receive the D/A output stage at high impedance, so as to obtain

   $R_L > 10K\Omega$
   $C_L < 20pF$

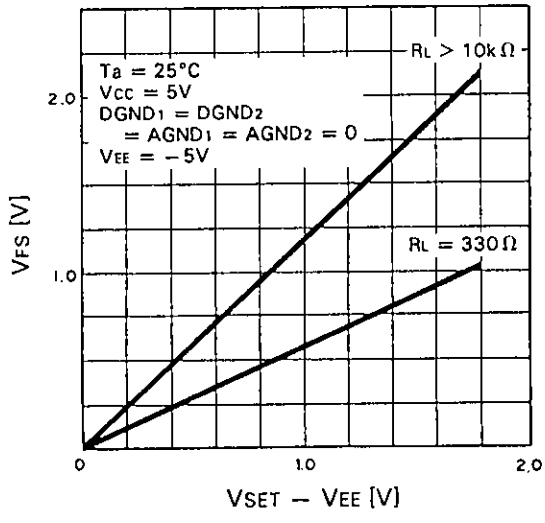
4. Noise reduction

   Refer to the following notes in order to minimize noise contamination that occurs from outside the IC and penatrates D/A output.
   - The power supply line and ground line should be made as wide as possible when fixed to the printed circuit board. Analog and Digital circuits should be separated.
   - Connected a bypass capacitor between each of DVCC (Pin 6) and DGND1 (Pin 7); AGND1,2 (Pins 2, 3) and VEE (Pin 23); VSET (Pin 24) and VEE (Pin 23), respectively.

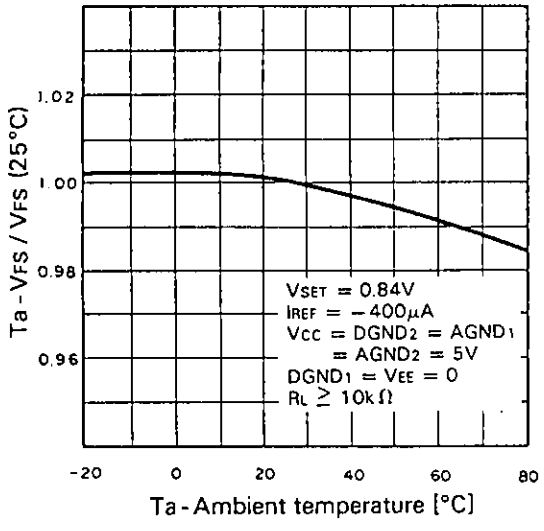
**Full-scale output voltage VFS and VSET**
(Single power supply)



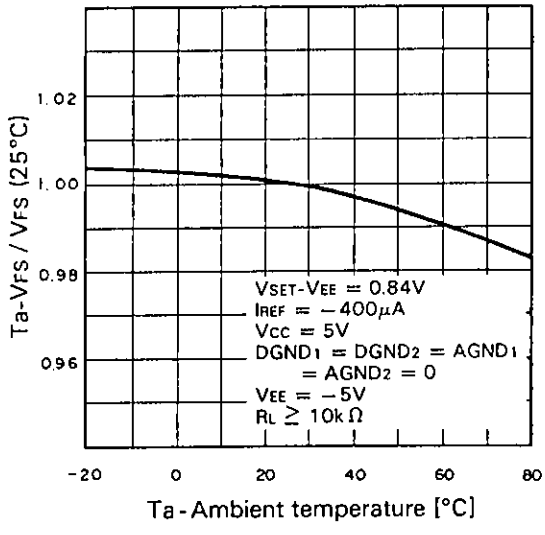

**Full-scale output voltage VFS and VSET-VEE**
(Dual power supply)



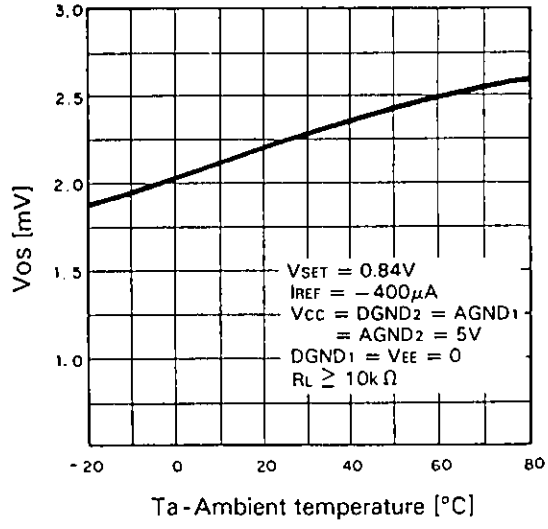

**Full-scale output voltage VFS temperature characteristics** (Single power supply)



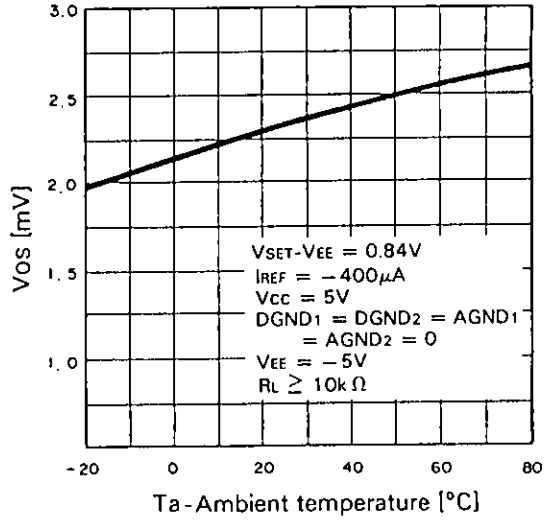

**Full-scale output voltage VFS temperature characteristics** (Dual power supply)



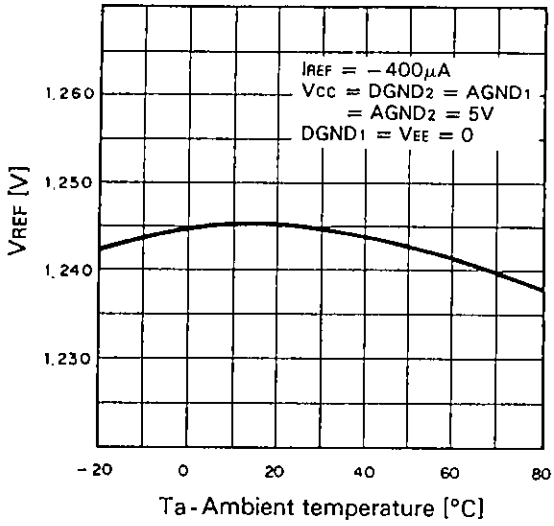

**Output offset voltage VOS temperature characteristics** (Single power supply)



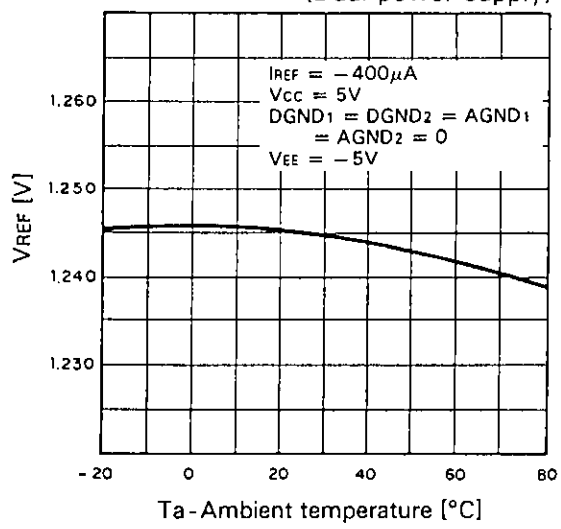

**Output offset voltage VOS temperature characteristics** (Dual power supply)



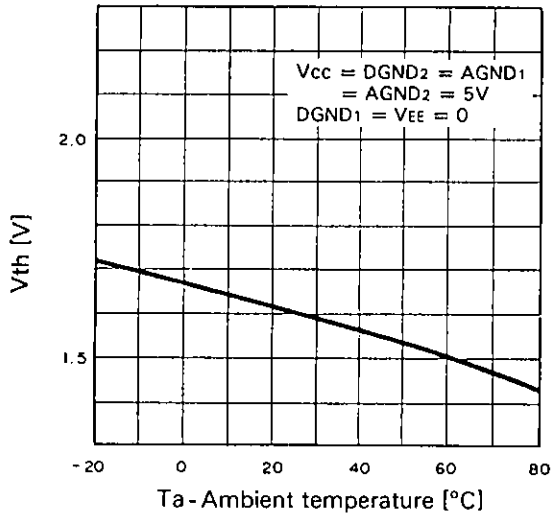
**Internal reference voltage VREF temperature characteristics** (Single power supply)



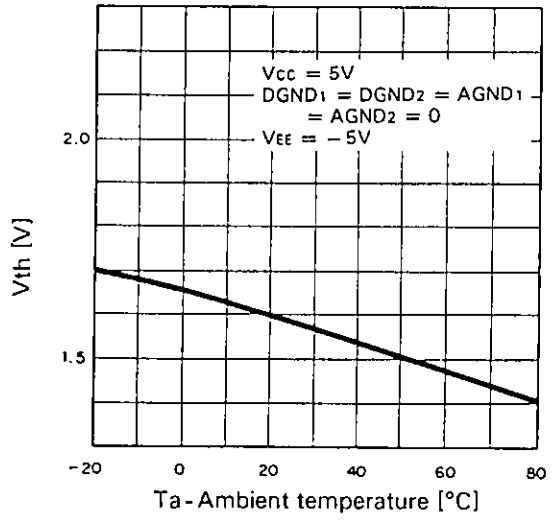

**Internal reference voltage VREF temperature characteristics** (Dual power supply)



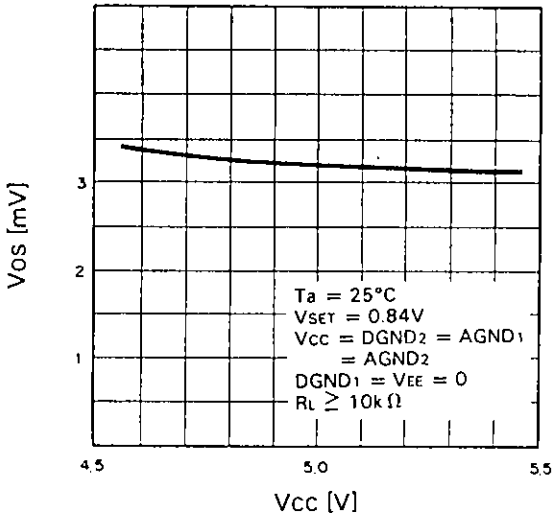

**Threshold voltage Vth of digital input temperature characteristics** (Single power supply)



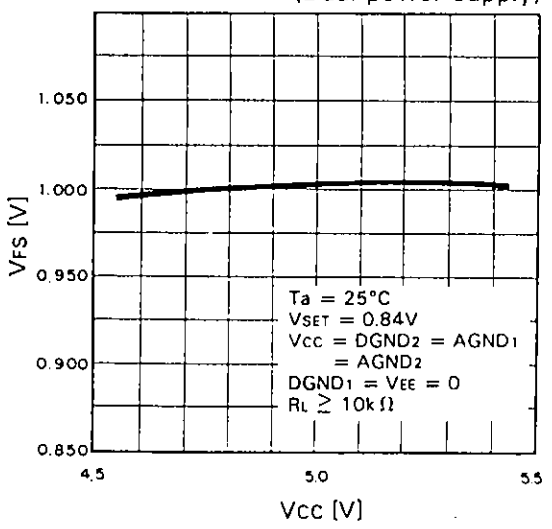

**Threshold voltage Vth of digital input temperature characteristics** (Dual power supply)




**Output offset voltage VOS to Supply voltage** (Single power supply)

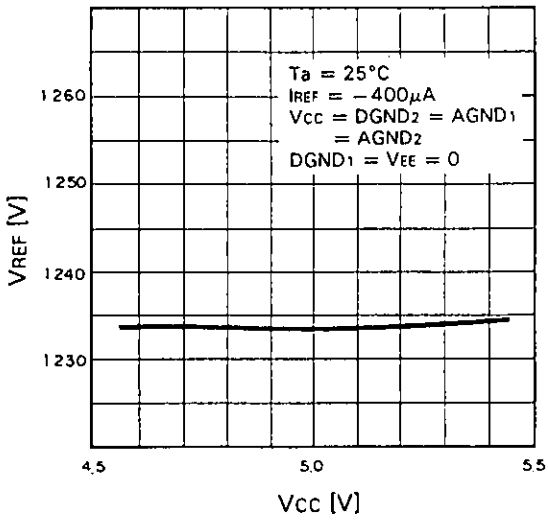



**Output full-scale voltage VFS to Supply voltage** (Dual power supply)



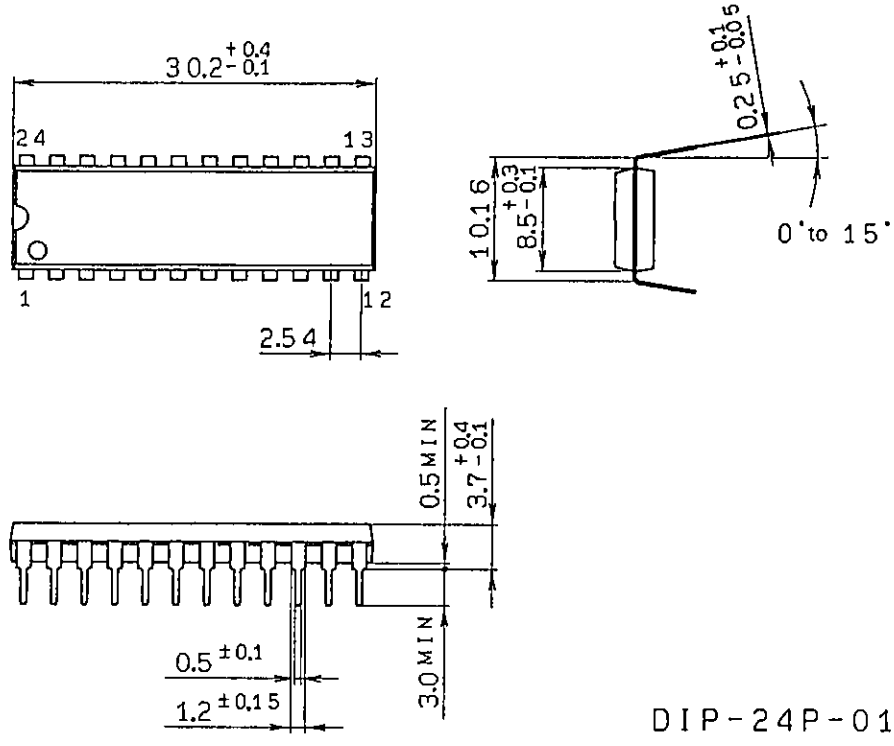
**Internal reference voltage $V_{REF}$ to supply voltage**

(Single power supply)



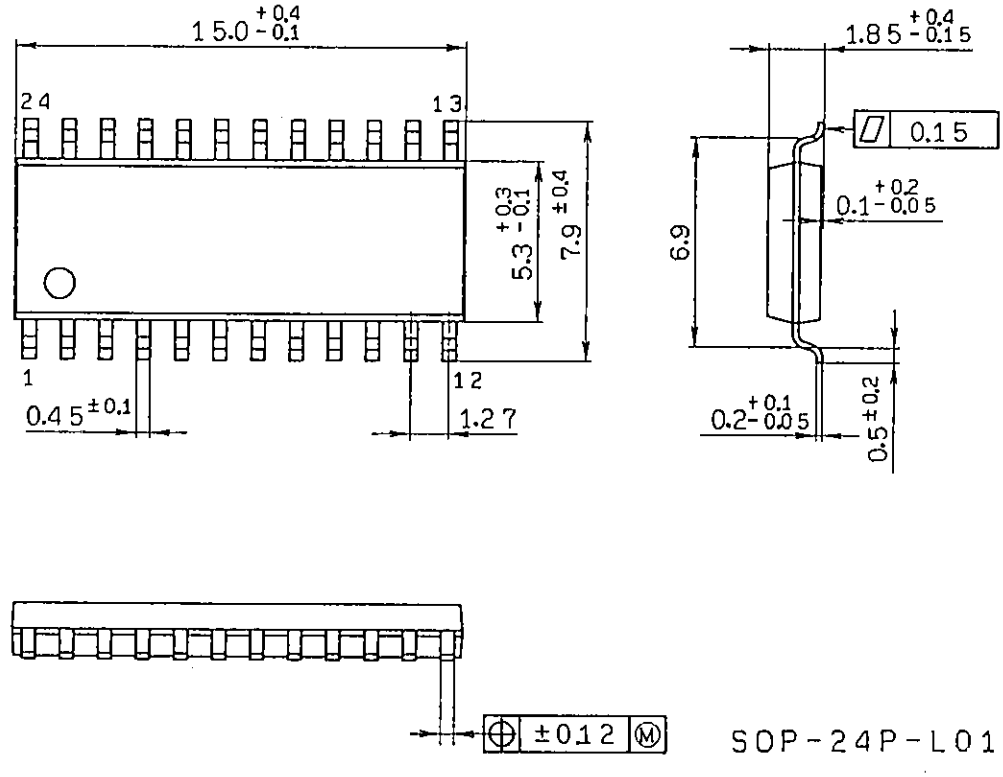
**Package Outline** Unit : mm

CXA1106P  24 pin DIP (Plastic) 400mil 2.0g




DIP-24P-01

CXA1106M  24 pin SOP (Plastic) 300mil 0.3g




SOP-24P-L01