

### OCTAL BUFFER/LINE DRIVE; 3-STATE

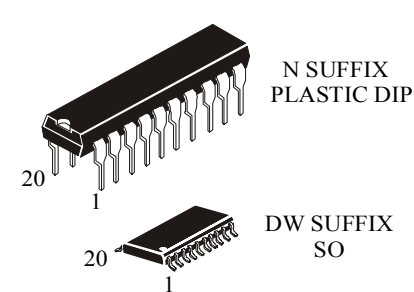
### KK74LV240

The KK74LV240 is a low-voltage Si-gate CMOS device and is pin and function compatible with KK74HC/HCT240.

The KK74LV240 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE causes the outputs to assume a high impedance OFF-state.

The KK74LV240 is identical to the KK74LV244 but has inverting outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0  $\mu$ A, 0.1  $\mu$ A at T = 25 °C
- Output Current: 8 mA at V<sub>CC</sub> = 3.0 V
- High Noise Immunity Characteristic of CMOS Devices



**N SUFFIX  
PLASTIC DIP**

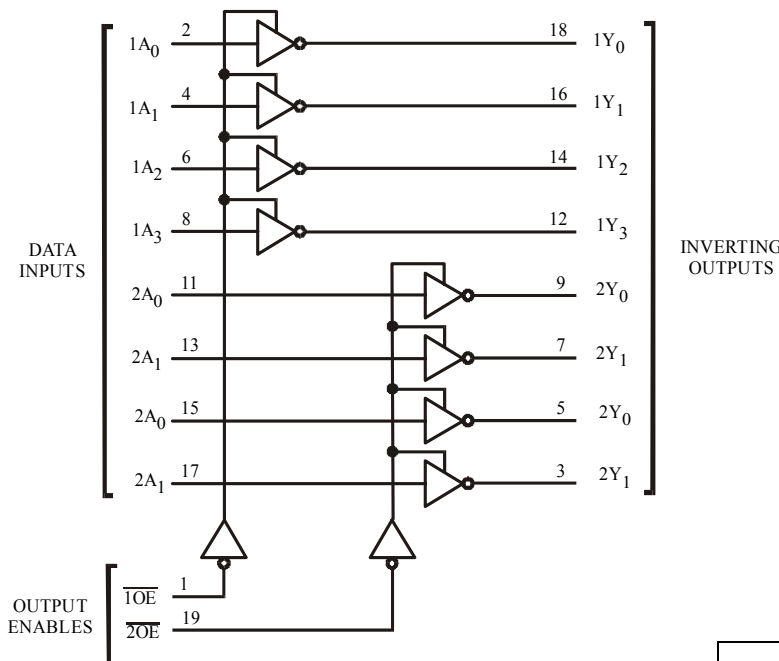
**DW SUFFIX  
SO**

**ORDERING INFORMATION**

**KK74LV240N** Plastic  
**KK74LV240DW** SOIC

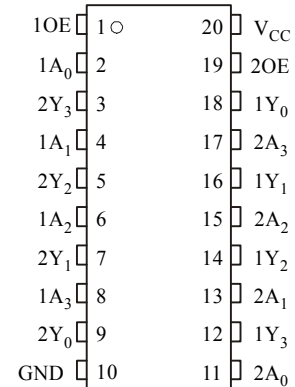
T<sub>A</sub> = -40° to 125° C for all packages

### LOGIC DIAGRAM



PIN 20 = V<sub>CC</sub>  
PIN 10 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Input		Output
$\overline{nOE}$	nAn	nYn
L	L	H
L	H	L
H	X	Z

H= high level  
 L = low level  
 X = don't care  
 Z = high impedance

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	-0.5 to +5.0	V
$I_{IK}^{*1}$	DC Input diode current	$\pm 20$	mA
$I_{OK}^{*2}$	DC Output diode current	$\pm 50$	mA
$I_O^{*3}$	DC Output source or sink current	$\pm 35$	mA
$I_{CC}$	DC $V_{CC}$ current	$\pm 70$	mA
$I_{GND}$	DC GND current	$\pm 70$	mA
$P_D$	Power dissipation per package: * <sup>4</sup>		mW
	Plastic DIP	750	
	SO	500	
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

\*<sup>1</sup>  $V_I < -0.5\text{ V}$  or  $V_I > V_{CC} + 0.5\text{ V}$ .

\*<sup>2</sup>  $V_O < -0.5\text{ V}$  or  $V_O > V_{CC} + 0.5\text{ V}$ .

\*<sup>3</sup>  $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ .

\*<sup>4</sup> Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C  
SO Package: - 8 mW/°C from 70° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	DC Supply Voltage	1.2	3.6	V	
$V_I$	Input Voltage	0	$V_{CC}$	V	
$V_O$	Output Voltage	0	$V_{CC}$	V	
$T_A$	Operating Temperature, All Package Types	-40	+125	°C	
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	$V_{CC}=1.2\text{ V}$	0	1000	ns
		$V_{CC}=2.0\text{ V}$	0	700	
		$V_{CC}=3.0\text{ V}$	0	500	
		$V_{CC}=3.6\text{ V}$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

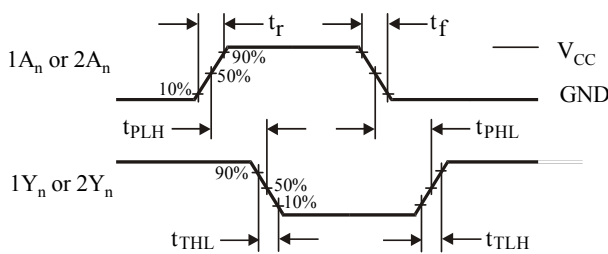
Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V <sub>IH</sub>	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V <sub>IL</sub>	LOW level input voltage		1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V <sub>OH</sub>	HIGH level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V
			2.0	1.92	-	1.9	-	1.9	-	
			3.0	2.92	-	2.9	-	2.9	-	
			3.6	3.52	-	3.5	-	3.5	-	
			V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -8 mA	3.0	2.48	-	2.34	-	2.20	-
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V
			2.0	-	0.09	-	0.1	-	0.1	
			3.0	-	0.09	-	0.1	-	0.1	
			3.6	-	0.09	-	0.1	-	0.1	
			V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 8 mA	3.0	-	0.33	-	0.4	-	0.5
I <sub>I</sub>	Input current	V <sub>I</sub> = V <sub>CC</sub> or 0 V	*	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>OZ</sub>	Three state leakage current	3-state outputs V <sub>I</sub> (01, 19) = V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> or 0 V	1.2 *	-	±0.5	-	±5	-	±10	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0 V I <sub>O</sub> = 0 μA	*	-	8.0	-	80	-	160	μA

\* V<sub>CC</sub> = 3.3 ± 0.3 V

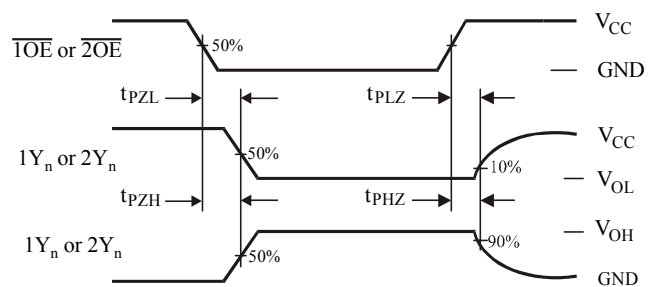
**AC ELECTRICAL CHARACTERISTICS** ( $C_L=50\text{ pF}$ ,  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation delay, 1An to 1Yn, 2An to 2Yn	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figure 1 and 3	1.2	-	100	-	125	-	150	ns
			2.0	-	24	-	30	-	36	
			*	-	15	-	19	-	23	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Propagation delay, 1OE to 1Yn, 2OE to 2Yn	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figure 2 and 4	1.2	-	140	-	175	-	210	ns
			2.0	-	30	-	35	-	41	
			*	-	20	-	24	-	28	
t <sub>PZH</sub> , t <sub>PZL</sub>	Propagation delay, 1OE to 1Yn, 2OE to 2Yn	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figure 2 and 4	1.2	-	140	-	175	-	210	ns
			2.0	-	32	-	40	-	48	
			*	-	20	-	25	-	30	
t <sub>THL</sub> , t <sub>TLH</sub>	Output Transition Time, Any Output	V <sub>I</sub> = 0 V or V <sub>CC</sub> Figure 1 and 3	1.2	-	60	-	75	-	90	ns
			2.0	-	16	-	20	-	24	
			*	-	10	-	13	-	15	
C <sub>I</sub>	Input capacitance		3.0	-	7.0	-	7.0	-	7.0	pF
C <sub>PD</sub>	Power dissipation capacitance (per one channel)	V <sub>I</sub> = 0 V or V <sub>CC</sub>		-	50	-	-	-	-	pF

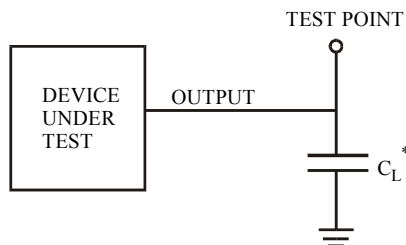
\* V<sub>CC</sub> = 3.3 ± 0.3 V



**Figure 1. Switching Waveforms**

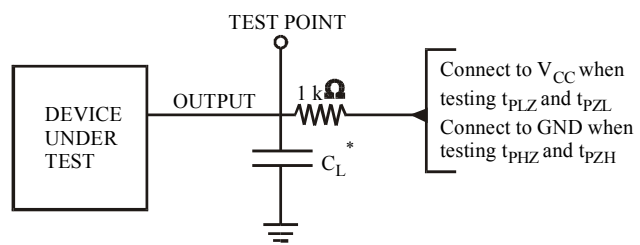


**Figure 2. Switching Waveforms**



\* Includes all probe and jig capacitance

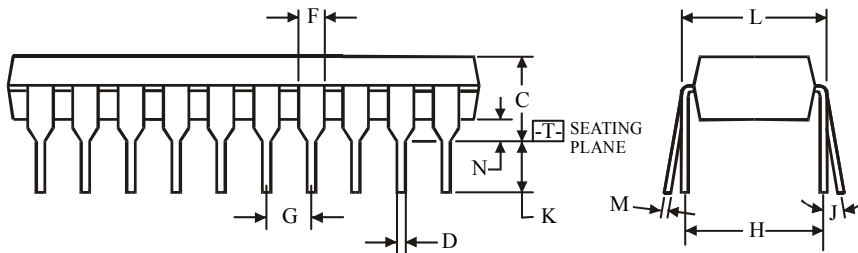
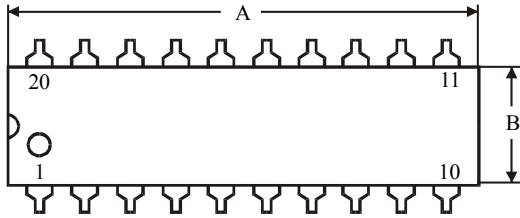
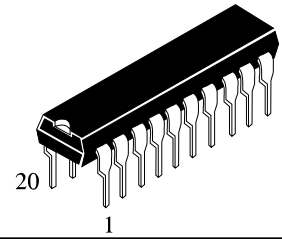
**Figure 3. Test Circuit**



\* Includes all probe and jig capacitance

**Figure 4. Test Circuit**

### N SUFFIX PLASTIC DIP (MS - 001AD)



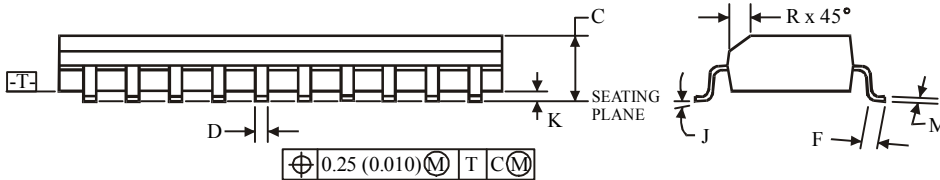
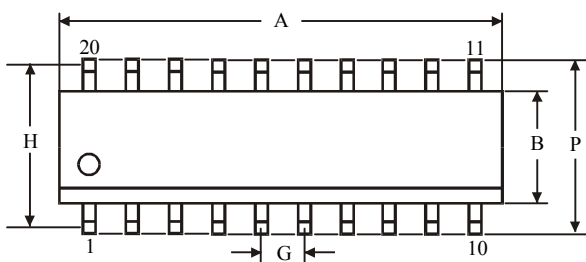
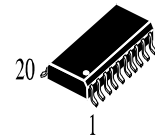
$\oplus 0.25 (0.010) \text{M} \text{T}$

#### NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	24.89	26.92
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

### D SUFFIX SOIC (MS - 013AC)



$\oplus 0.25 (0.010) \text{M} \text{T} \text{C} \text{M}$

#### NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	12.6	13
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75