SC4603
Very Low Input, MHz Operation, High Efficiency Synchronous Buck

Description

The SC4603 is a voltage mode step down (buck) regulator controller that provides accurate high efficiency power conversion from input supply range 2.25V to 5.5V. A high level of integration reduces external component count and makes it suitable for low voltage applications where cost, size and efficiency are critical.

The SC4603 drives external complementary power MOSFETs; P-channel on the high side and N-channel on the low side. The use of high side P-channel MOSFETs eliminates the need for an external charge pump and simplifies the high side gate driver. Non-overlap protection is provided for the gate drive signals to prevent shoot through of the MOSFET pair. The voltage drop across the P-channel MOSFET during its conduction is sensed for lossless short circuit current limiting.

A low power sleep mode can be achieved by forcing the SYNC/SLEEP pin below 0.8V. A synchronous mode of operation is activated as the SYNC/SLEEP pin is driven by an external clock. The quiescent supply current in sleep mode is typically lower than 10µA. A 1.7ms soft start is internally provided to prevent output voltage overshoot during start-up. A 100% maximum duty cycle allows the SC4603 to operate as a low dropout regulator in the event of a low battery condition.

The SC4603 is an ideal choice for 3.3V, 5V or other low input supply systems. It's available in 10 pin MSOP package.

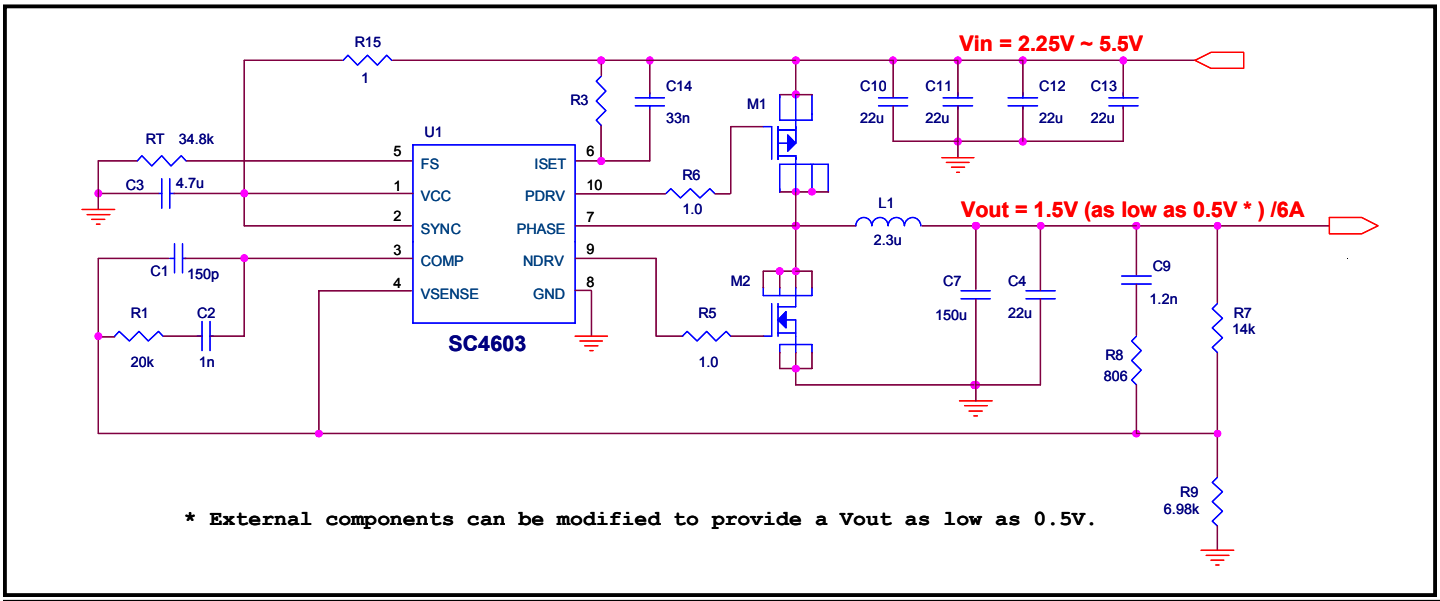
Features

- BICMOS voltage mode PWM controller
- 2.25V to 5.5V Input voltage range
- Output voltages as low as 0.5V
- Sleep mode (Icc = 10µA typ)
- Lossless adjustable overcurrent protection
- Combination pulse by pulse & hiccup mode current limit
- High efficiency synchronous switching
- 0% to 100% Duty cycle range
- Synchronization to external clock
- Asynchronous start-up
- 1MHz frequency of operation
- 10-Pin MSOP surface mount package. Lead free product. This product is fully WEEE and RoHS compliant

Applications

- Distributed power architecture
- Servers/workstations
- Local microprocessor core power supplies
- DSP and I/O power supplies
- Battery powered applications
- Telecommunication equipment
- Data processing applications

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage (V_{CC})		6	V
Output Drivers (PDRV, NDRV) Currents Continuous		±0.25	A
Inputs (VSENSE, COMP, SYNC/SLEEP, FS, ISET)		6	V
Phase		-0.3 to 5.5	V
Phase Pulse tpulse < 50ns		-2 to 6	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Junction Temperature Range	T_J	-55 to +150	°C
Thermal Impedance Junction to Case	θ_{JC}	41.9	°C/W
Thermal Impedance Junction to Ambient	θ_{JA}	113.1	°C/W
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

Unless otherwise specified, V_{CC} = 3.3V, R_T = 21Kohm, T_A = -40°C to 85°C, $T_A = T_J$.

Parameter	Test Conditions	Min	Typ	Max	Unit
Overall					
Supply Voltage		2.25		5.5	V
Supply Current, Sleep	$V_{SYNC/SLEEP}$ = 0V		10	15	µA
Supply Current, Operating			2	3	mA
V_{CC} Turn-on Threshold			2	2.25	V
V_{CC} Turn-off Hysteresis			100		mV
Error Amplifier					
Internal Reference	V_{CC} = 3.3V, T_A = 25°C	495	500	505	mV
	V_{CC} = 3.3V, T_A = -40°C to 85°C	492		508	mV
Internal Reference Change	V_{CC} = 2.25V to 3.3V, T_A = 25°C	-0.15	0.1	0.35	%/V
	V_{CC} = 3.3V to 5.5V, T_A = 25°C	-0.4	-0.2	0	%/V
VSENSE Bias Current			200		nA
Open Loop Gain (1)	V_{COMP} = 0.5V to 2.5V	80 (1)	90		dB
Unity Gain Bandwidth (1)			8		MHz
Slew Rate (1)			2.4		V/µs

Electrical Characteristics (Cont.)

Unless otherwise specified, V_{CC} = 3.3V, R_T = 21Kohm, T_A = -40°C to 85°C, $T_A = T_J$.

Parameter	Test Conditions	Min	Typ	Max	Unit
Error Amplifier (Cont.)					
VCOMP High	I_{COMP} = -5.5mA	V_{CC} - 0.6	V_{CC} - 0.4		V
VCOMP Low	I_{COMP} = 5.5mA		0.35	0.525	V
Oscillator					
Initial Accuracy	T_A = 25°C, $V_{SYNC/SLEEP}$ = HIGH	540	600	660	kHz
Voltage Stability	T_A = 25°C, V_{CC} = 2.25V to 5.5V		1		%/V
Temperature Coefficient	T_A = -40°C to 85°C		0.01		%/°C
Synchronization Frequency			1		MHz
SYNC Low Threshold				0.8	V
SYNC High Threshold		2.0			V
Ramp Peak to Valley (1)			1		V
Ramp Peak Voltage (1)			1.25		V
Ramp Valley Voltage (1)			0.25		V
Sleep, Soft Start, Current Limit					
Sleep Threshold	Measured at $V_{SYNC/SLEEP}$ LOGIC LOW			0.8	V
	Measured at $V_{SYNC/SLEEP}$ LOGIC HIGH	2.0			V
Sleep Input Bias Current (2)	$V_{SYNC/SLEEP}$ = 0V		-50		nA
Soft Start Time (1)	F_{SW} = 600kHz		1.7		ms
Current Limit Threshold (2)	Bias Current, T_J = 25°C	-43	-50	-57	µA
	Temperature Coefficient		+0.3		%/°C
Current Limit Blank Time(1)			150		ns
N-Channel and P-Channel Driver Outputs					
Pull Up Resistance (PDRV) (2)	Vcc = 3.3V, I_{OUT} = -100mA (source)		3.4		ohms
Pull Down Resistance (PDRV) (2)	Vcc = 3.3V, I_{OUT} = 100mA (sink)		3		ohms
Pull Up Resistance (NDRV) (1)	Vcc = 3.3V, I_{OUT} = -100mA (source)		3.4		ohms
Pull Down Resistance (NDRV) (2)	Vcc = 3.3V, I_{OUT} = 100mA (sink)		1.5		ohms
PDRV Output Rise Time (2)	Vgs = 3.3V, C_{OUT} = 1.0nF		8		ns
PDRV Output Fall Time (2)	Vgs = 3.3V, C_{OUT} = 1.0nF		7		ns

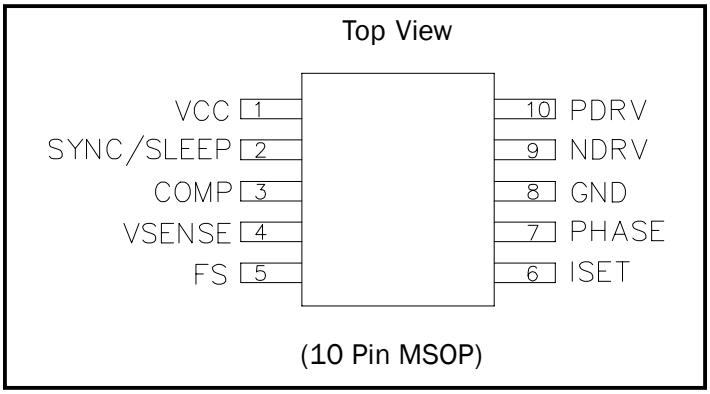
Electrical Characteristics (Cont.)

Unless otherwise specified, V_{CC} = 3.3V, R_T = 21Kohm, T_A = -40°C to 85°C, $T_A = T_J$.

Parameter	Test Conditions	Min	Typ	Max	Unit
N-channel and P-Channel Driver Outputs (Cont.)					
NDRV Output Rise Time (1)	Vgs = 3.3V, C_{COMP} = 1nF		8		ns
NDRV Output Fall Time (2)	Vgs = 3.3V, C_{COMP} = 1nF		3		ns
Deadtime Delay (PDRV high to NDRV high) (3)			adaptive		
Deadtime Delay (NDRV low to PDRV low) (1)		30	50		ns

Notes:
(1). Guaranteed by design.
(2). Guaranteed by characterization.
(3). Dead time delay from PDRV high to NDRV high is adaptive. As the phase node voltage drops below 600mV due to PDRV high, NDRV will start to turn high.

Pin Configuration



Ordering Information

Part Number[1]	Device
SC4603IMSTRT[2]	MSOP-10

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 0.1 to 4.7µF low ESL/ESR ceramic capacitor.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

FS: An external resistor connected with FS pin sets the clock frequency.

SYNC/SLEEP: The oscillator frequency of SC4603 is set by FS when SYNC/SLEEP is pulled and held above 2V. Its synchronous mode operation is activated as the SYNC/SLEEP is driven by an external clock. The oscillator and PWM are designed to provide practical operation to 1MHz when synchronized. Sleep mode is invoked if SYNC/SLEEP is pulled and held below 0.8V which can be accomplished by an external gate or transistor. The Sleepmode supply current is 10µA typical.

VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the Buck converter. It senses the output voltage through an external divider.

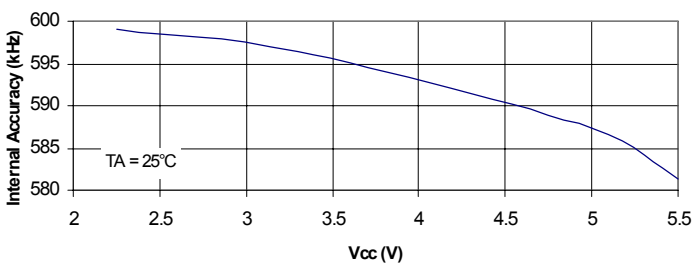
COMP: This is the output of the voltage amplifier. The voltage at this output is connected to the inverting input of the PWM comparator. A lead-lag network around the voltage amplifier compensates for the two pole LC filter characteristic inherent to voltage mode control and is required in order to optimize the dynamic performance of the voltage mode control loop.

PHASE, ISET: PHASE input is connected to the junction between the two external power MOSFET transistors. The voltage drop across the upper P-channel device is monitored by PHASE and ISET during PFET conduction and forms the current limit comparator and logic that sets the PWM latch and terminates the PFET output pulse once excessive voltage drop across the PFET is detected. The controller stops switching and goes through a soft start sequence once the converter output voltage drops below 70% its nominal voltage. This prevents excess power dissipation in the PMOSFET during a short circuit. The current limit threshold is set by the external resistor between VCC and ISET. The internal 50µA current source has a positive temperature coefficient that can compensate PMOSFET Rdson variation due to its junction temperature change.

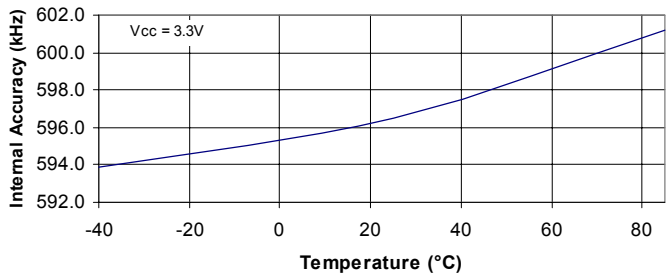
PDRV, NDRV: The PWM circuitry provides complementary drive signals to the output stages. The Cross conduction of the external MOSFETs is prevented by monitoring the voltage on the P-channel and N-channel driver pins in conjunction with a time delay optimized for FET turn-off characteristics.

Typical Characteristics

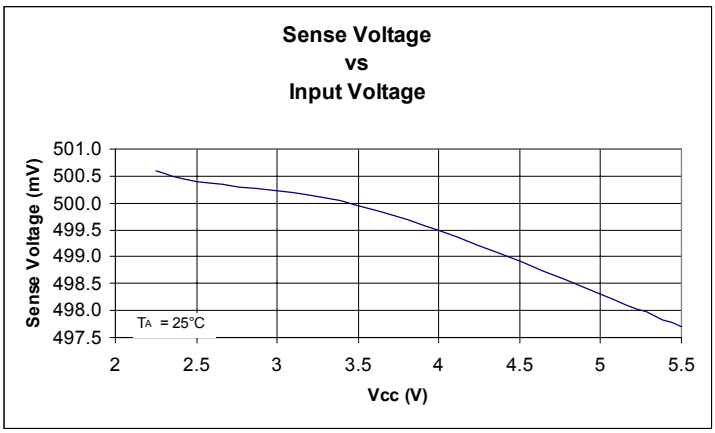
Oscillator Internal Accuracy vs Input Voltage



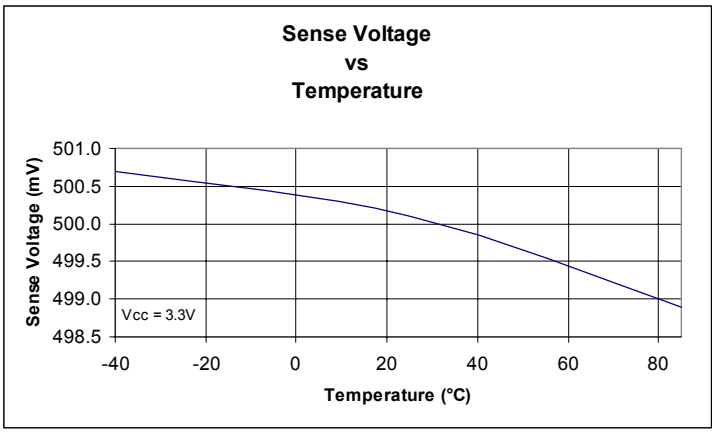
Oscillator Internal Accuracy vs Temperature



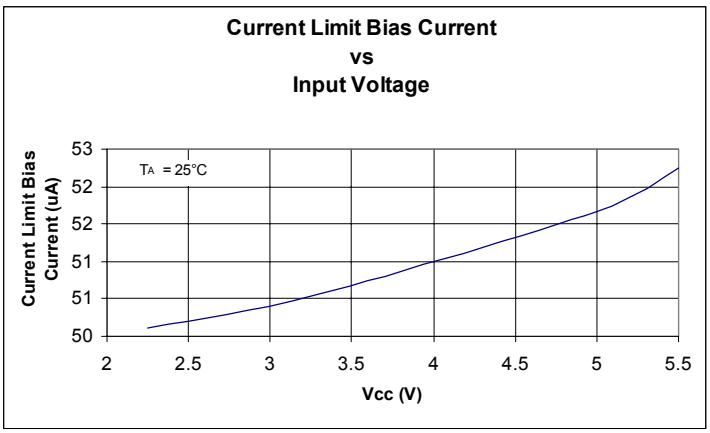
Sense Voltage vs Input Voltage



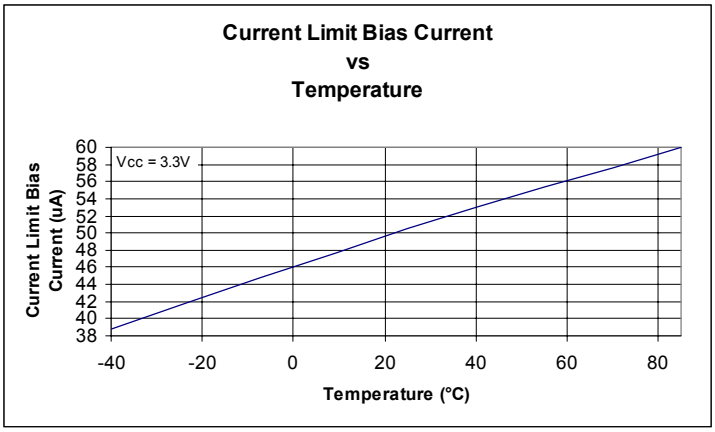
Sense Voltage vs Temperature



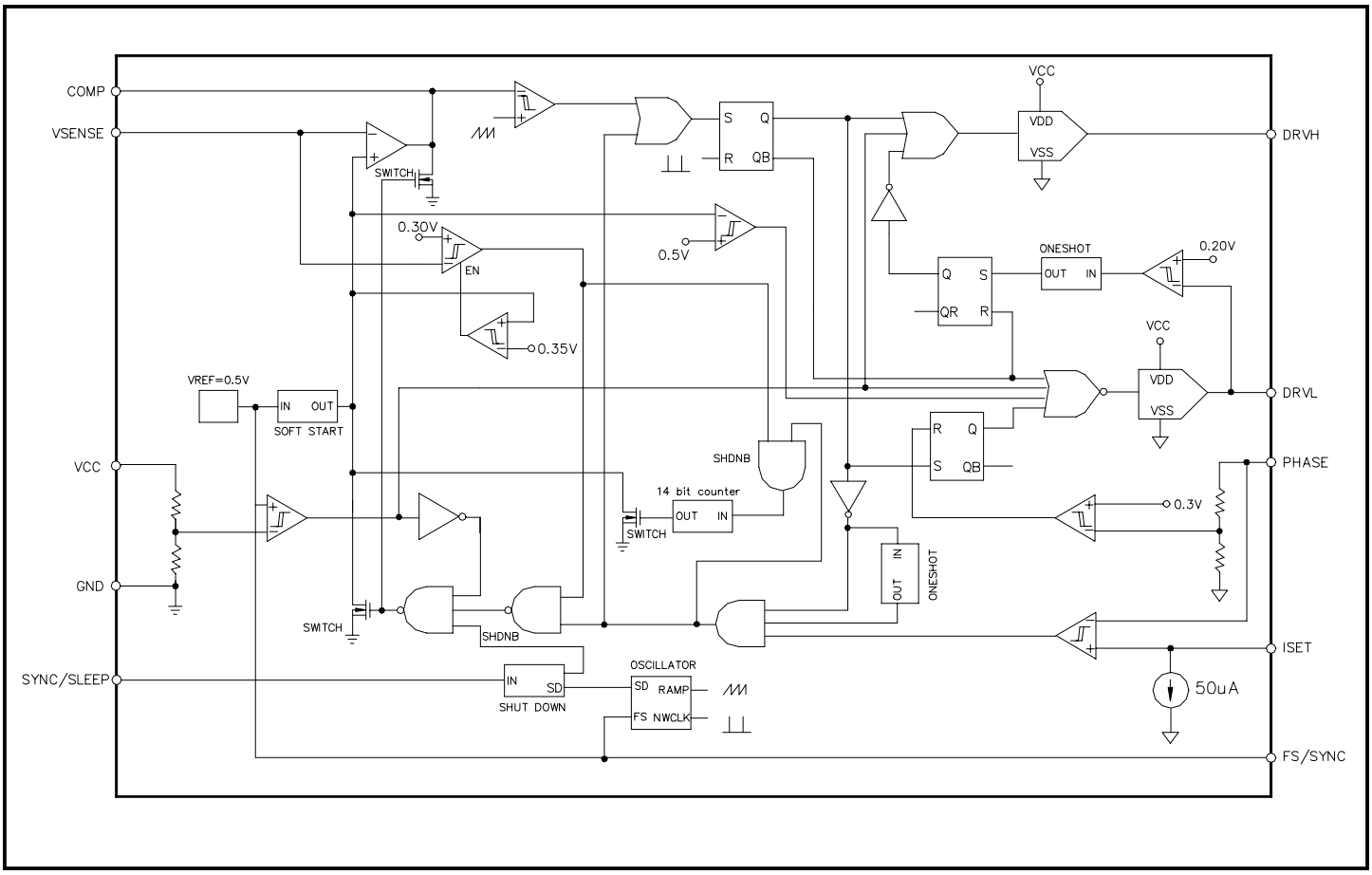
Current Limit Bias Current vs Input Voltage



Current Limit Bias Current vs Temperature



Block Diagram



Applications Information

Enable

Pulling and holding the SYNC/SLEEP pin below 0.8V initializes the SLEEP mode of the SC4603 with its typical SLEEP mode supply current of 10uA. During the SLEEP mode, the high side and low side MOSFETs are turned off and the internal soft start voltage is held low.

Oscillator

The oscillator uses an external resistor to set the oscillation frequency when the SYNC/SLEEP pin is pulled and held above 2V. The ramp waveform is a triangle at the PWM frequency with a peak voltage of 1.25V and a valley voltage of 0.25V. A 100% maximum duty cycle allows the SC4603 to operate as a low dropout regulator in the event of a low battery condition. The resistor tolerance adds to the accuracy of the oscillator frequency. The external resistor connected to the FS pin, as shown below determines the approximate operating frequency:

$$f_S = \frac{126 \bullet 10^8}{R_T}$$

An external clock connected to the SYNC/SLEEP activates its synchronous mode and the frequency of the clock can be up to 1MHz.

UVLO

When the SYNC/SLEEP pin is pulled and held above 2V, the voltage on the VCC pin determines the operation of the SC4603. As V_{CC} increases during start up, the UVLO block senses V_{CC} and keeps the high side and low side MOSFETs off and the internal soft start voltage low until V_{CC} reaches 2.25V. If no faults are present, the SC4603 will initiate a soft start when V_{CC} exceeds 2.25V. A hysteresis (100mV) in the UVLO comparator provides noise immunity during its start up.

Applications Information - (Cont.)

Soft Start

The soft start function is required for step down controllers to prevent excess inrush current through the DC bus during start up. Generally this can be done by sourcing a controlled current into a timing capacitor and then using the voltage across this capacitor to slowly ramp up the error amp reference. The closed loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady state duty cycle as the output voltage reaches its regulated value. With this, the inrush current from the input side is controlled. The duration of the soft start in the SC4603 is controlled by an internal timing circuit which is used during start up and over current to set the hiccup time. The soft start time can be calculated by:

$$T_{SOFT_START} = \frac{1020}{f_S}$$

As can be seen here, the soft start time is switching frequency dependant. For example, if f_s = 600kHz, $T_{SOFT-START}$ = 1020/600k = 1.7ms. But if f_s = 1MHz, $T_{SOFT-START}$ = 1020/1M = 1.02ms.

The SC4603 implements its soft start by ramping up the error amplifier reference voltage providing a controlled slew rate of the output voltage, then preventing overshoot and limiting inrush current during its start up.

Over Current Protection

Over current protection for the SC4603 is implemented by detecting the voltage drop of the high side P-MOSFET during conduction, also known as high side $R_{DS(ON)}$ detection. This loss-less detection eliminates the sense resistor and its loss. The overall efficiency is improved and the number of components and cost of the converter are reduced. $R_{DS(ON)}$ sensing is by default inaccurate and is mainly used to protect the power supply during a fault case. The over current trigger point will vary from unit to unit as the $R_{DS(ON)}$ of P-MOSFET varies. Even for the same unit, the over current trigger point will vary as the junction temperature of P-MOSFET varies. The SC4603 provides a built-in 50µA current source, which is combined with R_{SET} (connected between V_{CC} and I_{SET}) to determine the current limit threshold. The value of R_{SET} can be properly selected according to the desired current limit point I_{MAX} and the internal 50µA pull down current available on the I_{SET} pin based on the following expression:

$$R_{SET} = \frac{I_{MAX} \bullet R_{DS(ON)}}{50\mu A}$$

Kelvin sensing connections should be used at the drain and source of P-MOSFET.

The $R_{DS(ON)}$ sensing used in the SC4603 has an additional feature that enhances the performance of the over current protection. Because the $R_{DS(ON)}$ has a positive temperature coefficient, the 50µA current source has a positive coefficient of about 0.3%/C° providing first order correction for current sensing vs temperature. This compensation depends on the high amount of thermal transferring that typically exists between the high side P-MOSFET and the SC4603 due to the compact layout of the power supply.

When the converter detects an over current condition ($I > I_{MAX}$) as shown in Figure 1, the first action the SC4603 takes is to enter cycle by cycle protection mode (Point B to Point C), which responds to minor over current cases. Then the output voltage is monitored. If the over current and low output voltage (set at 70% of nominal output voltage) occur at the same time, the Hiccup mode operation (Point C to Point D) of the SC4603 is invoked and the internal soft start capacitor is discharged. This is like a typical soft start cycle.

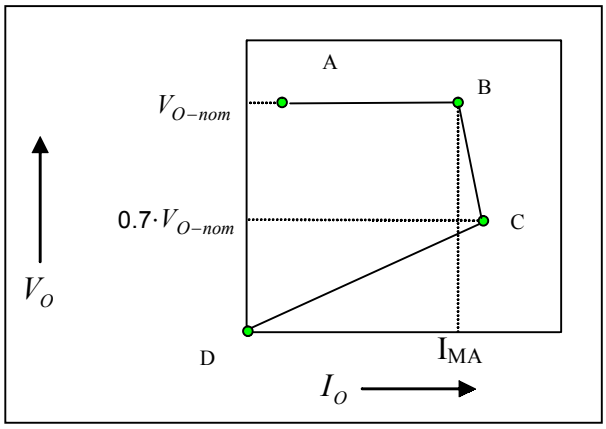


Figure 1. Over current protection characteristic of SC4603

Applications Information - (Cont.)

Power MOSFET Drivers

The SC4603 has two drivers for external complementary power MOSFETs. The driver block consists of one high side P-MOSFET driver, PDRV, and one low side N-MOSFET driver, NDRV, which are optimized for driving external power MOSFETs in a synchronous buck converter. The output drivers also have gate drive non-overlap mechanism that gives a dead time between PDRV and NDRV transitions to avoid potential shoot through problems in the external MOSFETs. By using the proper design and the appropriate MOSFETs, a 6A converter can be achieved. As shown in Figure 2, $t_{d1,}$ the delay from the P-MOSFET off to the N-MOSFET on is adaptive by detecting the voltage of the phase node. t_{d2}, the delay from the N-MOSFET off to the P-MOSFET on is fixed, is 50ns for the SC4603. This control scheme guarantees avoiding the cross conduction or shoot through between two MOSFETs and minimizes the conduction loss in the bottom diode for high efficiency applications.

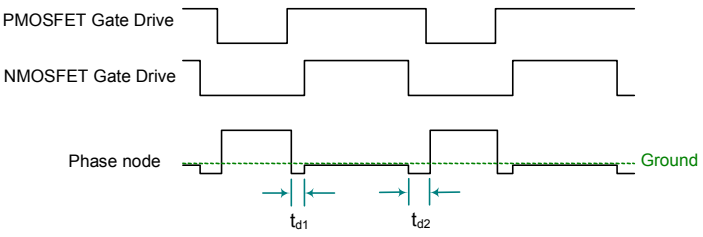


Figure 2. Timing Waveforms for Gate Drives and Phase Node

Inductor Selection

The factors for selecting the inductor include its cost, efficiency, size and EMI. For a typical SC4603 application, the inductor selection is mainly based on its value, saturation current and DC resistance. Increasing the inductor value will decrease the ripple level of the output voltage while the output transient response will be degraded. Low value inductors offer small size and fast transient responses while they cause large ripple currents, poor efficiencies and more output capacitance to smooth out the large ripple currents. The inductor should be able to handle the peak current without saturating and its copper resistance in the winding should be as low as possible to minimize its resistive power loss. A good trade-off among its size, loss and cost is to set the inductor ripple current to be within 15% to 30% of the maximum output current.

The inductor value can be determined according to its operating point and the switching frequency as follows:

$$L = \frac{V_{out} \cdot (V_{in} - V_{out})}{V_{in} \cdot f_s \cdot \Delta I \cdot I_{OMAX}}$$

Where:
f_s = switching frequency and
ΔI = ratio of the peak to peak inductor current to the maximum output load current.

The peak to peak inductor current is:

$$I_{p-p} = \Delta I \bullet I_{OMAX}$$

After the required inductor value is selected, the proper selection of the core material is based on the peak inductor current and efficiency requirements. The core must be able to handle the peak inductor current I_{PEAK} without saturation and produce low core loss during the high frequency operation.

$$I_{PEAK} = I_{OMAX} + \frac{I_{p-p}}{2}$$

The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce inductor's copper loss. The core loss can be found in the manufacturer's datasheet. The inductor's copper loss can be estimated as follows:

$$P_{COPPER} = I^2_{LRMS} \cdot R_{WINDING}$$

Where:
I_{LRMS} is the RMS current in the inductor. This current can be calculated as follows:

$$I_{LRMS} = I_{OMAX} \cdot \sqrt{1 + \frac{1}{3} \cdot \Delta I^2}$$

Output Capacitor Selection

Basically there are two major factors to consider in selecting the type and quantity of the output capacitors. The first one is the required ESR (Equivalent Series Resistance) which should be low enough to reduce the voltage deviation from its nominal one during its load changes. The second one is the required capacitance, which should be high enough to hold up the output voltage. Before the SC4603 regulates the inductor current to a new value

Applications Information - (Cont.)

during a load transient, the output capacitor delivers all the additional current needed by the load. The ESR and ESL of the output capacitor, the loop parasitic inductance between the output capacitor and the load combined with inductor ripple current are all major contributors to the output voltage ripple. Surface mount speciality polymer aluminum electrolytic chip capacitors in UE series from Panasonic provide low ESR and reduce the total capacitance required for a fast transient response. POSCAP from Sanyo is a solid electrolytic chip capacitor which has a low ESR and good performance for high frequency with a low profile and high capacitance. Above mentioned capacitors are recommended to use in SC4603 applications.

Input Capacitor Selection

The input capacitor selection is based on its ripple current level, required capacitance and voltage rating. This capacitor must be able to provide the ripple current by the switching actions. For the continuous conduction mode, the RMS value of the input capacitor can be calculated from:

$$I_{CIN(RMS)} = I_{OMAX} \cdot \sqrt{\frac{V_{out} \cdot (V_{in} - V_{out})}{V_{in}^{2}}}$$

This current gives the capacitor's power loss as follows:

$$P_{CIN} = I^{2}_{CIN(RMS)} \cdot R_{CIN(ESR)}$$

This capacitor's RMS loss can be a significant part of the total loss in the converter and reduce the overall converter efficiency. The input ripple voltage mainly depends on the input capacitor's ESR and its capacitance for a given load, input voltage and output voltage. Assuming that the input current of the converter is constant, the required input capacitance for a given voltage ripple can be calculated by:

$$C_{IN} = I_{OMAX} \cdot \frac{D \cdot (1-D)}{fs \cdot (\Delta V_I - I_{OMAX} \cdot R_{CIN(ESR)})}$$

Where:
$D = V_O/V_I$, duty ratio and
ΔV_I = the given input voltage ripple.

Because the input capacitor is exposed to the large surge current, attention is needed for the input capacitor. If tantalum capacitors are used at the input side of the converter, one needs to ensure that the RMS and surge ratings are not exceeded. For generic tantalum capacitors, it is wise to derate their voltage ratings at a ratio of 2 to protect these input capacitors.

Power MOSFET Selection

The SC4603 can drive a P-MOSFET at the high side and an N-MOSFET synchronous rectifier at the low side. The use of the high side P-MOSFET eliminates the need for an external charge pump and simplifies the high side gate driver circuit.

For the top MOSFET, its total power loss includes its conduction loss, switching loss, gate charge loss, output capacitance loss and the loss related to the reverse recovery of the bottom diode, shown as follows:

$$P_{TOP_TOTAL} = I^{2}_{TOP_RMS} \cdot R_{TOP_ON} + \frac{I_{TOP_PEAK} \cdot V_I \cdot f_s}{V_{GATE} / R_G} \cdot (Q_{GD} + Q_{GS2}) + Q_{GT} \cdot V_{GATE} \cdot f_s + (Q_{OSS} + Q_{rr}) \cdot V_I \cdot f_s$$

Where:
R_G = gate drive resistor,
Q_{GD} = the gate to drain charge of the top MOSFET,
Q_{GS2} = the gate to source charge of the top MOSFET,
Q_{GT} = the total gate charge of the top MOSFET,
Q_{OSS} = the output charge of the top MOSFET, and
Q_{rr} = the reverse recovery charge of the bottom diode.

For the top MOSFET, it experiences high current and high voltage overlap during each on/off transition. But for the bottom MOSFET, its switching voltage is the bottom diode's forward drop during its on/off transition. So the switching loss for the bottom MOSFET is negligible. Its total power loss can be determined by:

$$P_{BOT_TOTAL} = I^{2}_{BOT_RMS} \cdot R_{BOT_ON} + Q_{GB} \cdot V_{GATE} \cdot f_s + I_{D_AVG} \cdot V_F$$

Where:
Q_{GB} = the total gate charge of the bottom MOSFET and
V_F = the forward voltage drop of the bottom diode.

Applications Information - (Cont.)

For a low voltage and high output current application such as the 3.3V/1.5V@6A case, the conduction loss is often dominant and selecting low $R_{DS(ON)}$ MOSFETs will noticeably improve the efficiency of the converter even though they give higher switching losses.

The gate charge loss portion of the top/bottom MOSFET's total power loss is derived from the SC4603. This gate charge loss is based on certain operating conditions (f_s, V_{GATE}, and I_O).

The thermal estimations have to be done for both MOSFETs to make sure that their junction temperatures do not exceed their thermal ratings according to their total power losses P_{TOTAL}, ambient temperature T_A and their thermal resistances $R_{\theta JA}$ as follows:

$$T_{J(max)} < T_A + \frac{P_{TOTAL}}{R_{\theta JA}}$$

Loop Compensation Design:

For a DC/DC converter, it is usually required that the converter has a loop gain of a high cross-over frequency for fast load response, high DC and low frequency gain for low steady state error, and enough phase margin for its operating stability. Often one can not have all these properties at the same time. The purpose of the loop compensation is to arrange the poles and zeros of the compensation network to meet the requirements for a specific application.

The SC4603 has an internal error amplifier and requires the compensation network to connect among the COMP pin and VSENSE pin, GND, and the output as shown in Figure 3. The compensation network includes C1, C2, R1, R7, R8 and C9. R9 is used to program the output voltage according to:

$$V_{OUT} = 0.5 \cdot (1 + \frac{R_7}{R_9})$$

As indicated in Internal Reference Change section, the internal reference voltage (measured at VSENSE pin) changes slightly if the input voltage of the SC4603 is away from 3.3V.

For example, if $V_{CC} = 2.25V$, the reference voltage, $V_{REF}@2.25V =$

$$V_{REF}@3.3V + \frac{Vref@3.3V}{100} \bullet \text{Internal Reference Change } @2.25V \bullet |V_{CC} - 3.3V| =$$

$$500 + \frac{500}{100} \bullet 0.1 \bullet |2.25 - 3.3| = 500.5(mV)$$

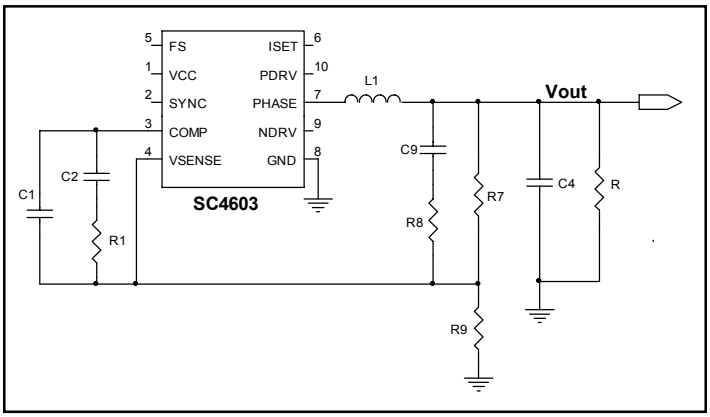


Figure 3. Compensation network provides 3 poles and 2 zeros.

For voltage mode step down applications as shown in Figure 3, the power stage transfer function is:

$$G_{VD}(s) = V_{IN} \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L_1}{R} + s^2 L_1 C_4}$$

Where:
R = load resistance and
R_C = C_4's ESR.

The compensation network will have the characteristic as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot \frac{1 + \frac{s}{\omega_{Z2}}}{\cdot 1 + \frac{s}{\omega_{P2}}}$$

Applications Information - (Cont.)

Where

$$\omega_I = \frac{1}{R_7 \cdot (C_1 + C_2)}$$

$$\omega_{Z1} = \frac{1}{R_1 \cdot C_2}$$

$$\omega_{Z2} = \frac{1}{(R_7 + R_8) \cdot C_9}$$

$$\omega_{P1} = \frac{C_1 + C_2}{R_1 \cdot C_1 \cdot C_2}$$

$$\omega_{P2} = \frac{1}{R_8 \cdot C_9}$$

After the compensation, the converter will have the following loop gain:

$$T(s) = G_{PWM} \cdot G_{COMP}(s) \cdot G_{VD}(s) =$$

$$\frac{\frac{1}{V_M} \cdot \omega_I \cdot V_{IN}}{s} \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot \frac{1 + \frac{s}{\omega_{Z2}}}{\cdot 1 + \frac{s}{\omega_{P2}}} \cdot \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L}{R} + s^2 LC}$$

Where:
G_{PWM} = PWM gain and
V_M = 1.0V, ramp peak to valley voltage of SC4603.

The design guidelines for the SC4603 applications are as following:

1. Set the loop gain crossover corner frequency ω_C for given switching corner frequency $\omega_S = 2\pi f_s$,
2. Place an integrator at the origin to increase DC and low frequency gains.
3. Select ω_{Z1} and ω_{Z2} such that they are placed near ω_0 to damp the peaking and the loop gain has a -20dB/dec rate to go across the 0dB line for obtaining a wide bandwidth.
4. Cancel the zero from C_4's ESR by a compensator pole ω_{P1} ($\omega_{P1} = \omega_{ESR} = 1/(R_C C_4)$),
5. Place a high frequency compensator pole ωp_2 ($\omega p_2 = \pi f_s$) to get the maximum attenuation of the switching ripple and high frequency noise with the adequate phase lag at ω_C.

The compensated loop gain will be as given in Figure 4:

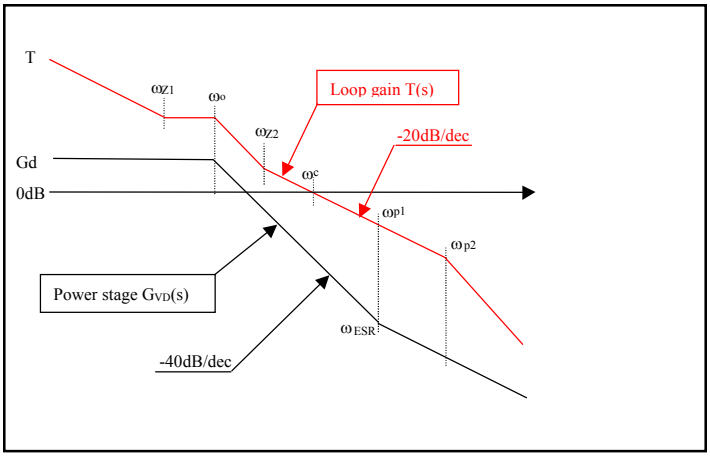


Figure 4. Asymptotic diagrams of power stage and its loop gain.

Layout Guidelines

In order to achieve optimal electrical, thermal and noise performance for high frequency converters, special attention must be paid to the PCB layouts. The goal of layout optimization is to identify the high di/dt loops and minimize them. The following guideline should be used to ensure proper functions of the converters.

1. A ground plane is recommended to minimize noises and copper losses, and maximize heat dissipation.
2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all the connections on one side of the PCB with wide copper filled areas if possible.
3. The V_{CC} bypass capacitor should be placed next to the VCC and GND pins.
4. The trace connecting the feedback resistors to the output should be short, direct and far away from the noise sources such as switching node and switching components.
5. Minimize the traces between PDRV/NDRV and the gates of the MOSFETs to reduce their impedance to drive the MOSFETs.
6. Minimize the loop including input capacitors, top/bottom MOSFETs. This loop passes high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop.
7. ISET and PHASE connections to P-MOSFET for current sensing must use Kelvin connections.

Applications Information - (Cont.)

Layout Guidelines (Cont.)

8. Maximize the trace width of the loop connecting the inductor, bottom MOSFET and the output capacitors.
9. Connect the ground of the feedback divider and the compensation components directly to the GND pin of the SC4603 by using a separate ground trace. Then connect this pin to the ground of the output capacitor as close as possible.

Design Example 1: 3.3V to 1.5V @ 5A application with SC4603 (NH020 footprint).

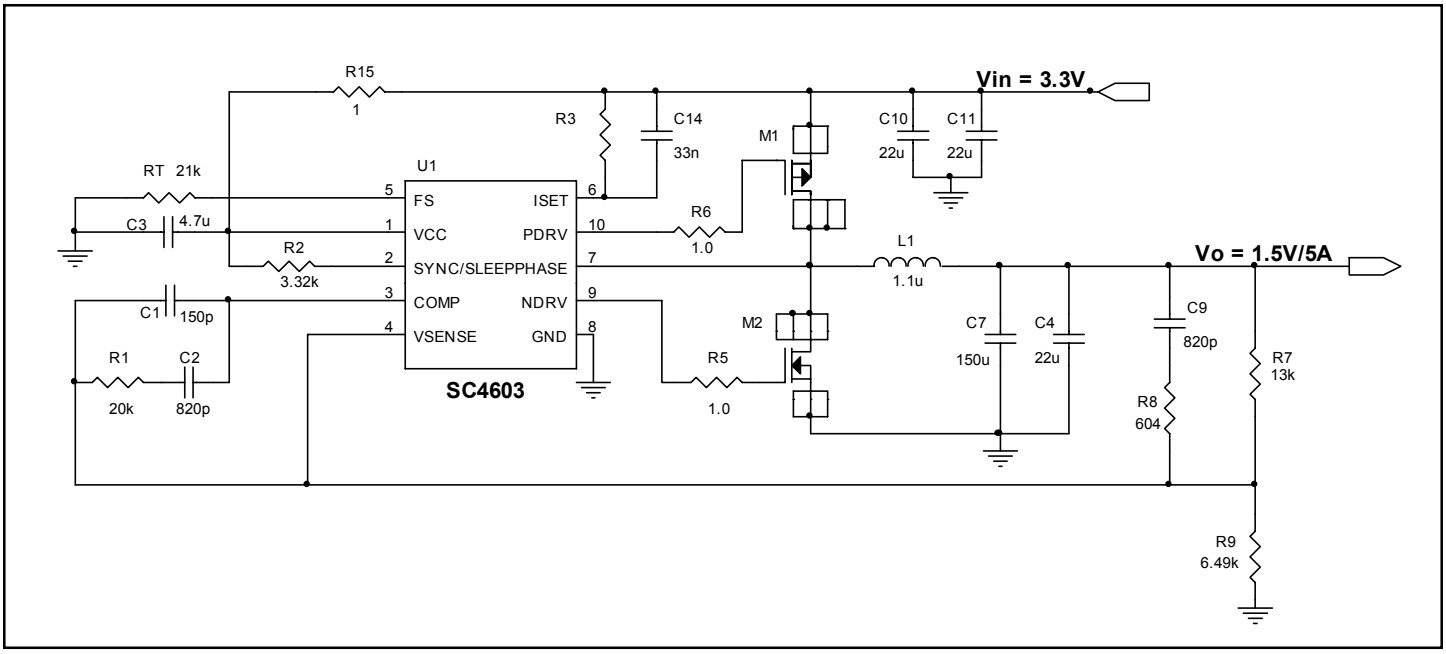


Figure 5. Schematic for 3.3V/1.5V @ 5A application

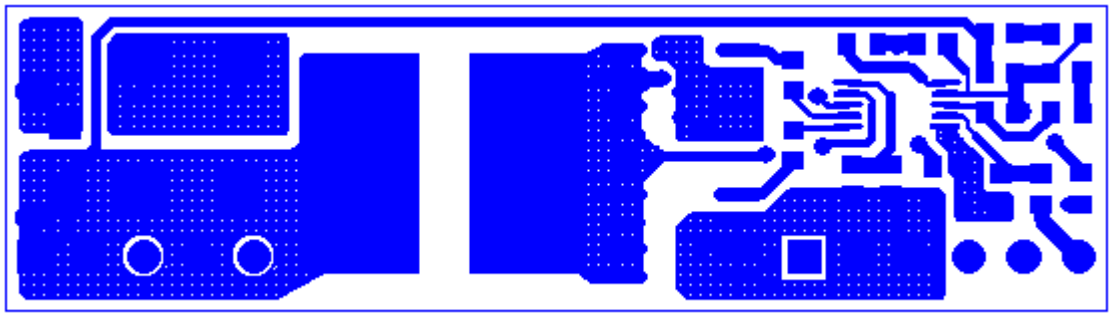
Bill of Materials - 3.3V to 1.5V @ 5A

Item	Qty	Reference	Value	Part No./Manufacturer
1	1	C1	150pF	
2	1	C2	820pF	
3	1	C3	4.7uF	
4	1	C7	150uF	Panasonic. P/N: 6.3V, SP
5	1	C9	820pF	
6	3	C10,C11,C4	22uF, 1210	TDK P/N: C3225X5R0J226M
7	1	C14	33nF	
8	1	L1	1.1uH	
9	1	M1	MOSFET P, S0-8	Fairchild P/N: FDS 6375
10	1	M2	MOSFET N, S0-8	Fairchild P/N: FDS 6680A
11	1	RT	21k	
12	1	R1	20k	
13	1	R2	3.32k	
14	1	R7	13k	
15	1	R8	604	
16	2	R5,R6	1	
17	1	R15	1	
18	1	R3	2.94k	
19	1	R9	6.49k	
20	1	U1	SC4603	Semtech P/N: SC4603IMSTRT

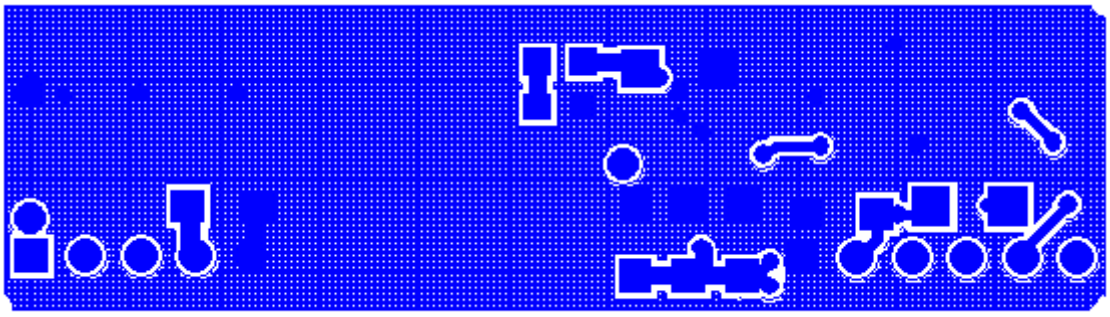
Key components:
U1: SC4603, Semtech
M1: FDS 6375, SO-8, Fairchild
M2: FDS 6680A, SO-8, Fairchild
L1: SMT power inductor, 1.1uH ETQP6F1R1H, Panasonic.
Unless specified, all resistors and capacitors are in SMD 0603 package.
Resistors are +/-1% and all capacitors are +/-20%

PCB Layout - 3.3V to 1.5V @ 6A

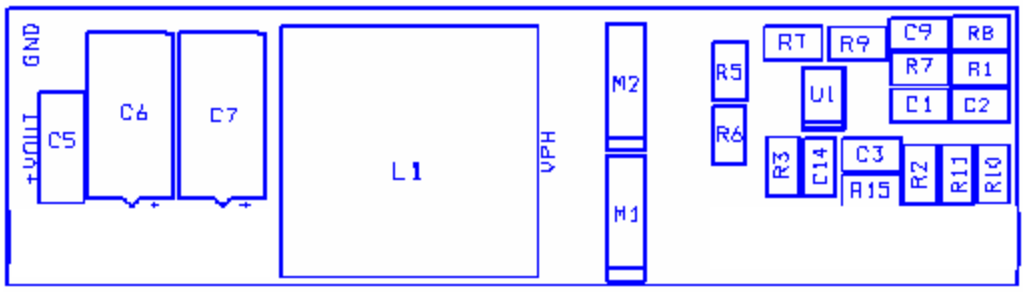
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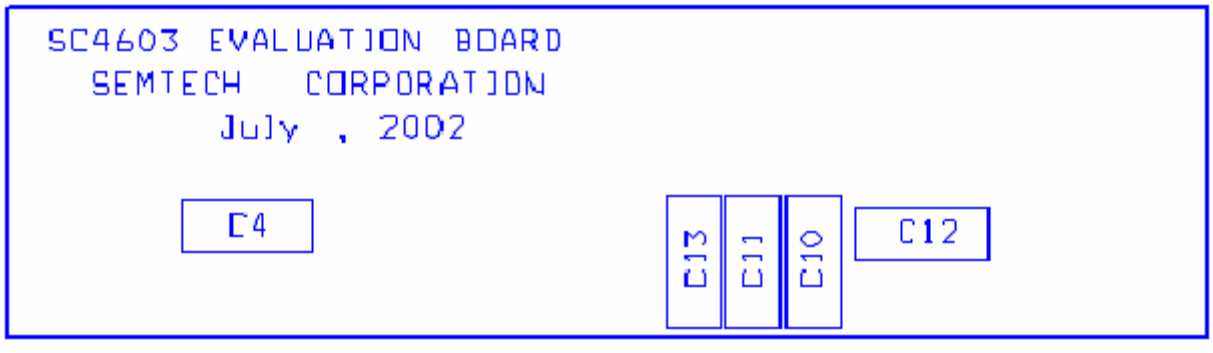
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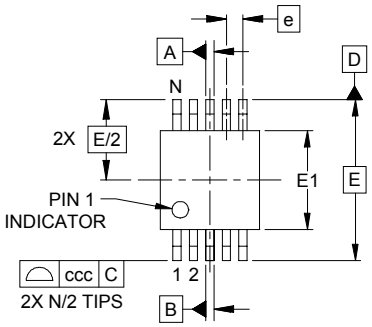
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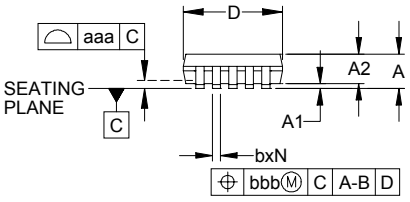
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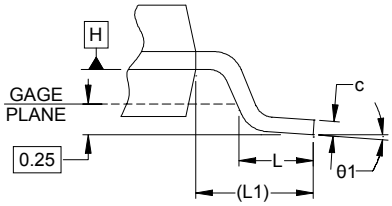


Outline Drawing - MSOP-10

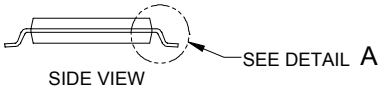


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		





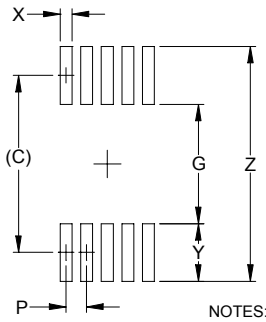
DETAIL A



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP-10



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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