

General Description

The Qorvo TGA2525 is a compact LNA Gain Block MMIC with adjustable gain control (AGC). The LNA operates from 2-18 GHz and is designed using Qorvo's proven standard 0.15 μ m Power pHEMT production process.

The TGA2525 provides a nominal 18 dBm of output power at 1 dB gain compression with a small signal gain of 17 dB. Greater than 30 dB adjustable gain can be achieved using Vg2 pin. Typical noise figure is 2 dB at 8 GHz. Special circuitry on both Vg1 and Vg2 pins provides ESD protection.

The TGA2525 is suitable for a variety of wideband systems such as point to point radios, radar warning receivers and electronic counter measures.

The TGA2525 is 100% DC and RF tested on-wafer to ensure performance compliance. The TGA2525 has a protective surface passivation layer providing environmental robustness.

Applications

- Wideband Gain Block/LNA
- X-Ku Point to Point Radio
- Electronic Warfare Applications

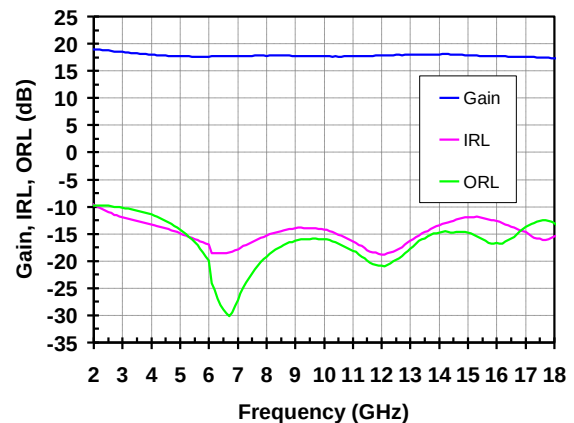
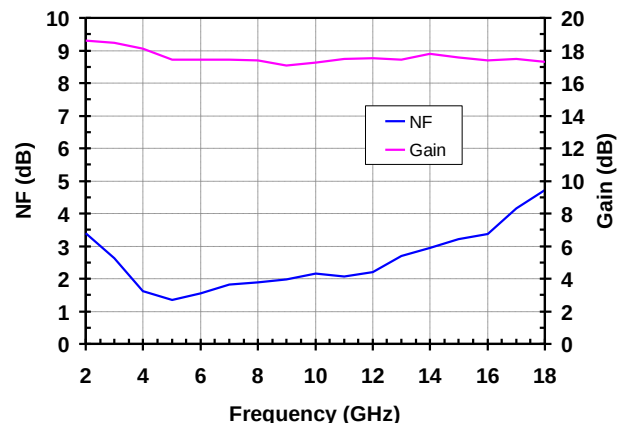
Product Features

- Frequency Range: 2-18 GHz
- Midband NF: 2 dB
- Gain: 17 dB
- >30 dB adjustable gain with Vg2
- TOI: 29 dBm Typical
- 22 dBm Nominal Psat, 18 dBm Nominal P1dB
- ESD Protection circuitry on Vg1 and Vg2
- Bias: Vd = 5 V, Id = 75 mA, Vg1 = -0.6 V, Vg2 = +1.3 V, Typical
- Technology: 3 MI 0.15 μ m Power pHEMT
- Chip Dimensions: 2.09 x 1.35 x 0.100 mm



Measured Performance

Bias conditions: Vd = 5 V, Id = 75 mA, Vg1 = -0.6 V, Vg2 = +1.3 V Typical



Ordering Information

Part	Description
TGA2525	GaAs MMIC Die, Gel Pack, Qty 100
1075728	TGA2525 Evaluation Board, Qty 1

Absolute Maximum Ratings^{1/}

Symbol	Parameter	Value	Notes
V_D - V_G	Drain to Gate Voltage	10 V	
V_D	Drain Voltage	7 V	^{2/}
V_{G1}	Gate # 1 Voltage Range	-2 to 0 V	
V_{G2}	Gate # 2 Voltage Range	-2 to +3 V	
I_D	Drain Current	144 mA	^{2/}
I_{G1}	Gate # 1 Current Range	-24 to 24 mA	^{3/}
I_{G2}	Gate # 2 Current Range	-24 to 24 mA	^{3/}
P_{IN}	Input Continuous Wave Power	22 dBm	^{2/}
$T_{channel}$	Channel Temperature	200 °C	
$T_{storage}$	Storage Temperature	-65 to 150 °C	

Note:

- ^{1/} These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.
- ^{2/} Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.
- ^{3/} ESD protection diodes on V_D , V_{G1} and V_{G2} will conduct current for voltages approaching turn-on voltages. Diode turn-on voltage levels will decrease with decreasing temperature.

Recommended Operating Conditions

Symbol	Parameter ^{1/}	Value
V _D	Drain Voltage	5 V
I _D	Drain Current	75 mA
I _{D_Drive}	Drain Current under RF Drive	130 mA
V _{G1}	Gate # 1 Voltage	-0.6 V
V _{G2}	Gate # 2 Voltage	1.3 V

Note:

^{1/} See assembly diagram for bias instructions.

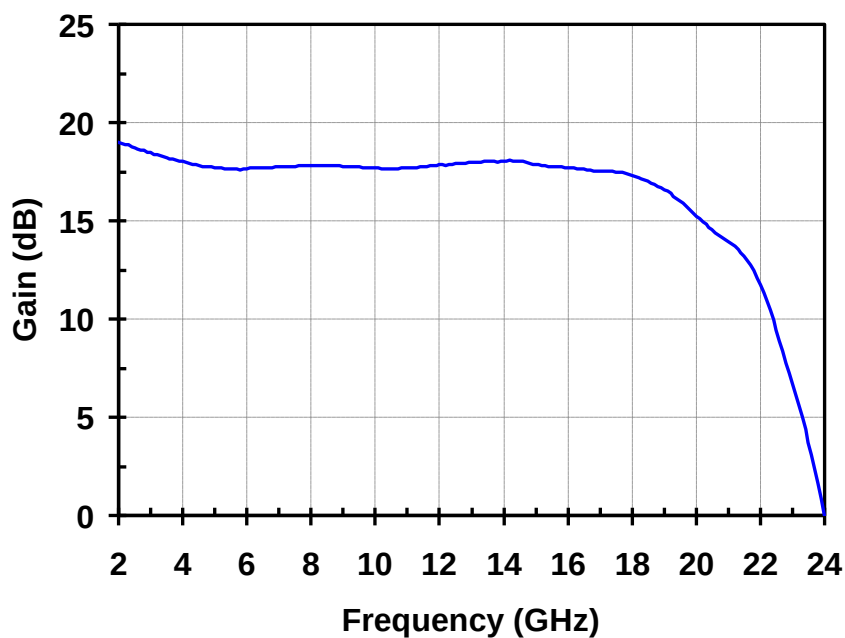
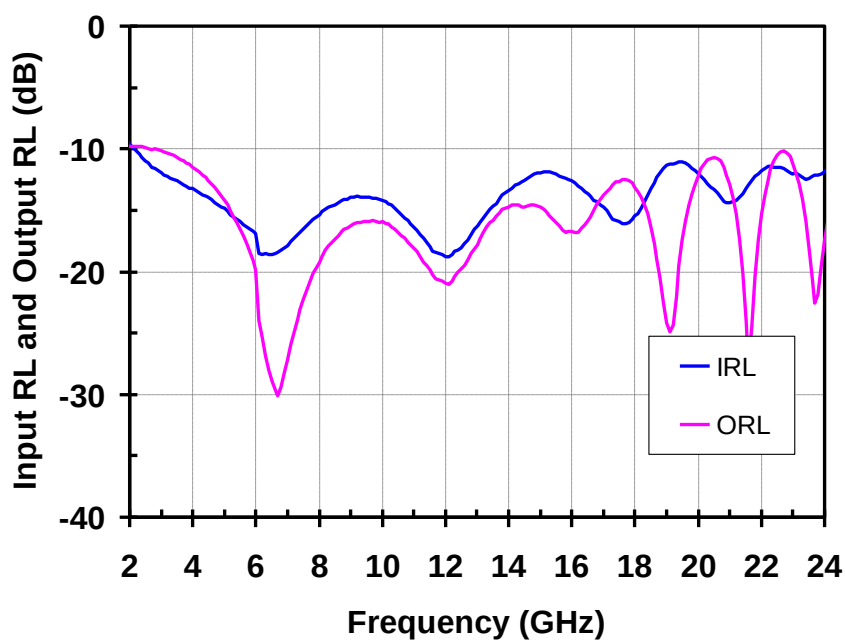
RF Characterization Table

Bias: V_D = 5 V, I_D = 75 mA, V_{G1} = -0.6 V, V_{G2} = +1.3 V, typical. Ambient temperature: 25 °C
Data de-embedded to the end of RF feeds, data include bond wire effects

Symbol	Parameter	Test Conditions	Min	Normal	Max	Units
Gain	Small Signal Gain	f = 2–18 GHz	14	17		dB
IRL	Input Return Loss	F = 2 GHz f = 3–14 GHz f = 14–18 GHz	8.5 10 10	15 15 12		dB
ORL	Output Return Loss	f = 2–4 GHz f = 5–18 GHz	9 10	11 15		dB
Psat	Saturated Output Power	f = 2–14 GHz f = 14–18 GHz		22 20		dBm
P1dB	Output Power @ 1dB Compression	f = 2 GHz f = 4, 8 GHz f = 10, 14 GHz f = 18 GHz	14 15 13 11	18 17 17 15		dBm
TOI	Output TOI	f = 2–14 GHz f = 14–18 GHz	- -	29 25		dBm
NF	Noise Figure	f = 2–14 GHz f = 14–18 GHz	- -	2 4	4 6	dB
S21 / T	S21 Temperature Dependence	f = 2–18 GHz	-	-0.008	-	dB / °C

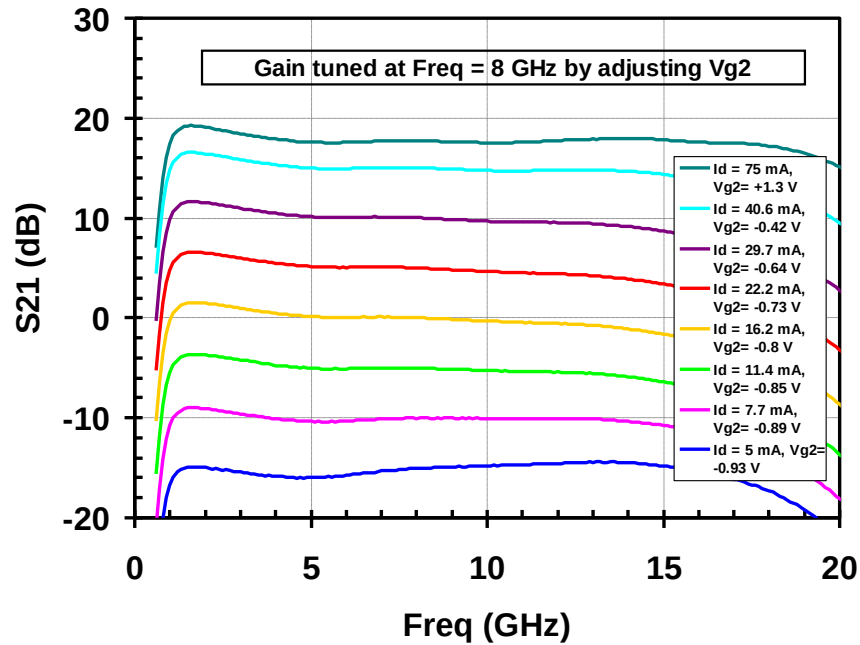
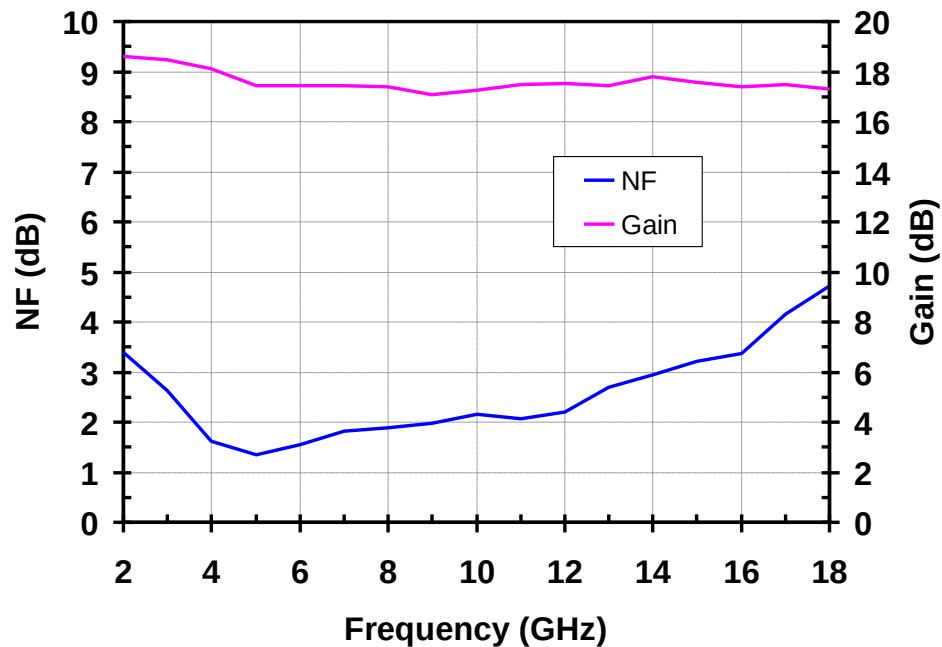
Measured Data

Bias conditions: $V_D = 5\text{ V}$, $I_D = 75\text{ mA}$, $V_{G1} = -0.6\text{ V}$, $V_{G2} = +1.3\text{ V}$ Typical, $25\text{ }^{\circ}\text{C}$



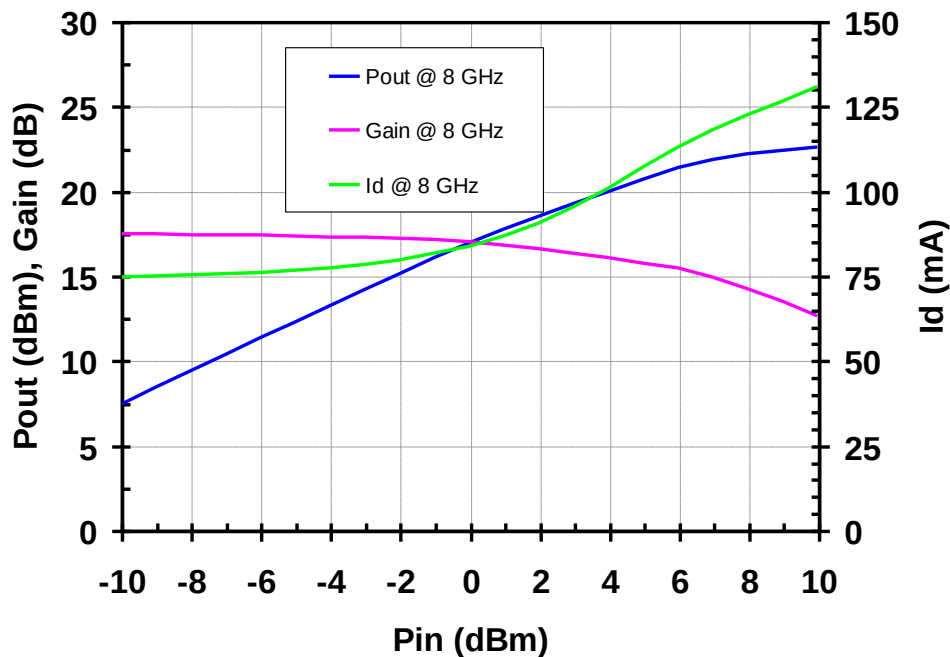
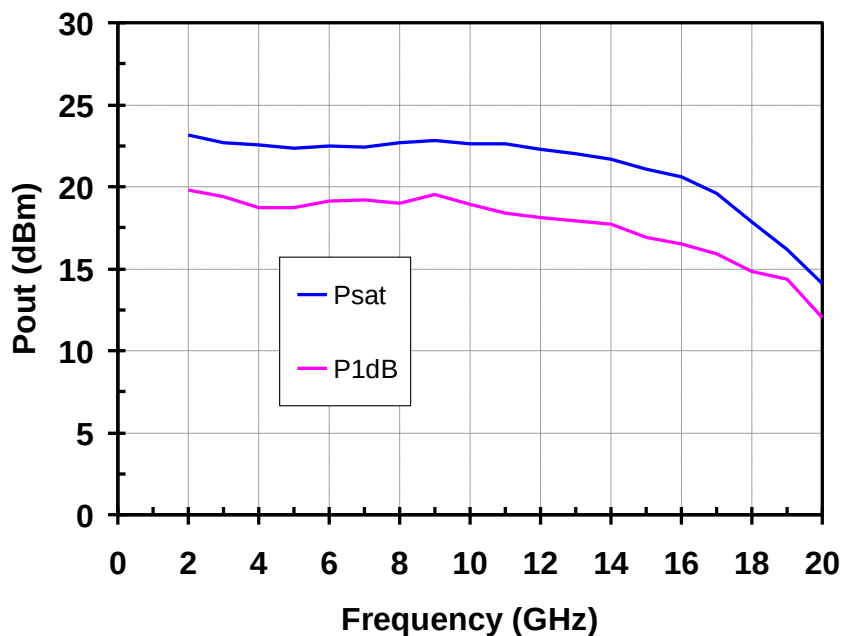
Measured Data

Bias conditions: $V_D = 5$ V, $I_D = 75$ mA, $V_{G1} = -0.6$ V, $V_{G2} = +1.3$ V Typical, 25 °C



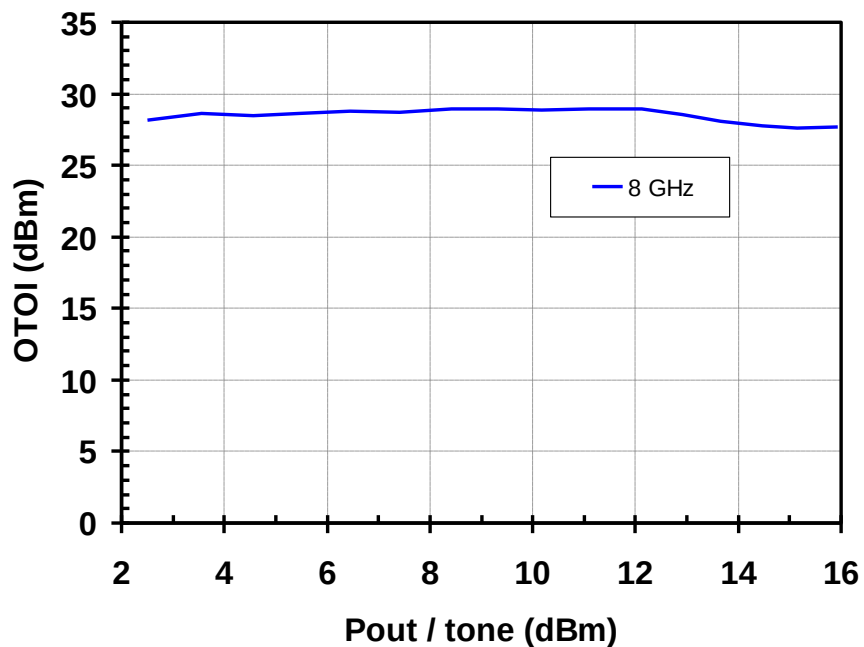
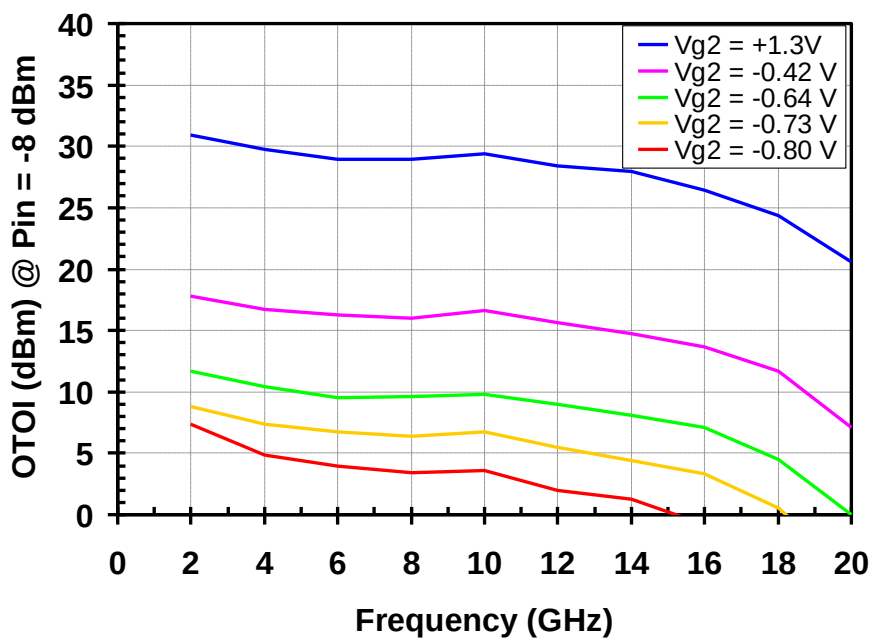
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Measured Data

Bias conditions: $V_D = 5\text{ V}$, $I_D = 75\text{ mA}$, $V_{G1} = -0.6\text{ V}$, $V_{G2} = +1.3\text{ V}$ Typical, $25\text{ }^{\circ}\text{C}$

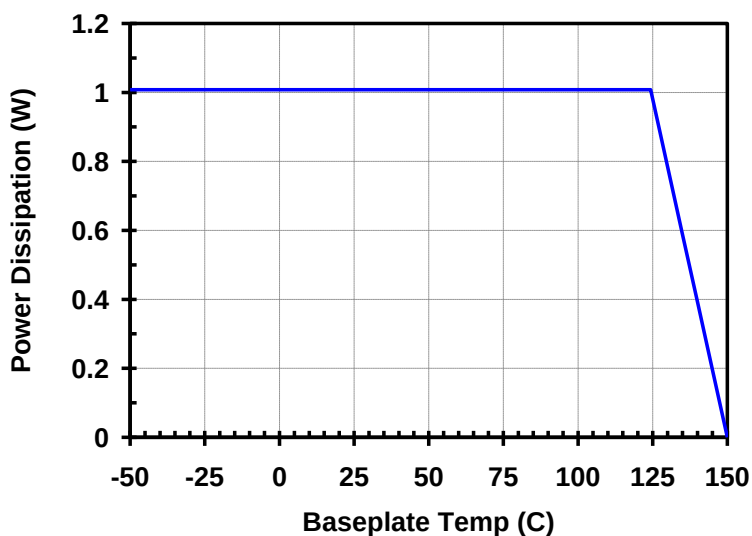


Power Dissipation and Thermal Properties

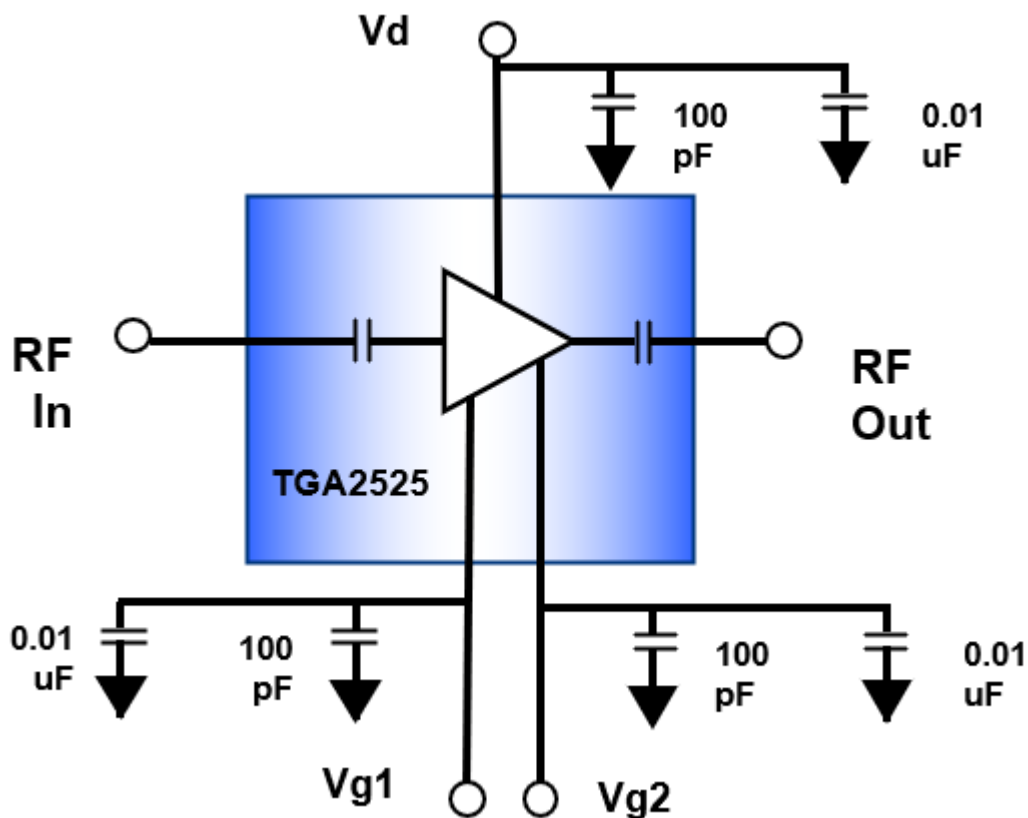
Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbase = 70 °C	Pd = 1.01 W Tchannel = 96 °C Tm = 9.7 E+8 Hrs	1/ 2/
Thermal Resistance, θ_{jc}	Vd = 5 V Id = 75 mA Pd = 0.375 W	θ_{jc} = 41.4 (°C/W) Tchannel = 86 °C Tm = 4.3 E+9 Hrs	
Thermal Resistance, θ_{jc} Under RF Drive	Vd = 5 V Id = 120 mA Pout = 22 dBm Pd = 0.45 W	θ_{jc} = 41.4 (°C/W) Tchannel = 89 °C Tm = 2.7 E+9 Hrs	
Mounting Temperature	30 Seconds	320 °C	
Storage Temperature		-65 to 150 °C	

- 1/ For a median life of 1E+6 hours, Power Dissipation is limited to
 $Pd(max) = (150\text{ °C} - Tbase\text{ °C})/\theta_{jc}$.
- 2/ Channel operating temperature will directly affect the device median time to failure (MTTF).
For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

Power De-rating Curve



Electrical Schematic



Bias Procedures

Bias-up Procedure

V_{G1} set to -1.5 V

V_D set to +5 V

V_{G2} set to +1.3 V

Adjust V_{G1} more positive until I_d is 75 mA.
This will be ~ V_{G1} = -0.6 V

Apply RF signal

Bias-down Procedure

Turn off RF signal

Reduce V_{G1} to -1.5 V. Ensure I_d ~ 0 mA

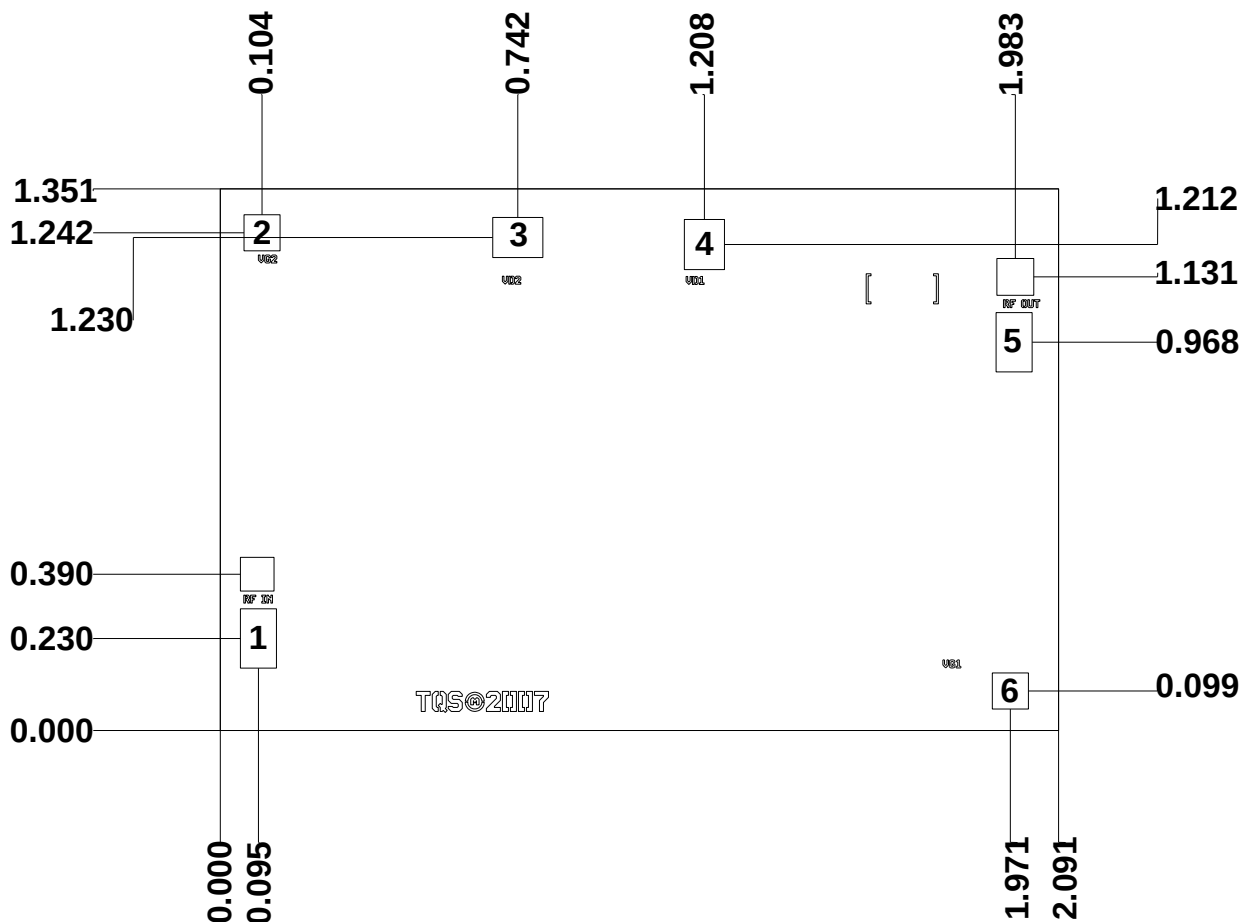
Turn V_{G2} to 0 V

Turn V_D to 0 V

Turn V_{G1} to 0 V

Turn off all power supplies

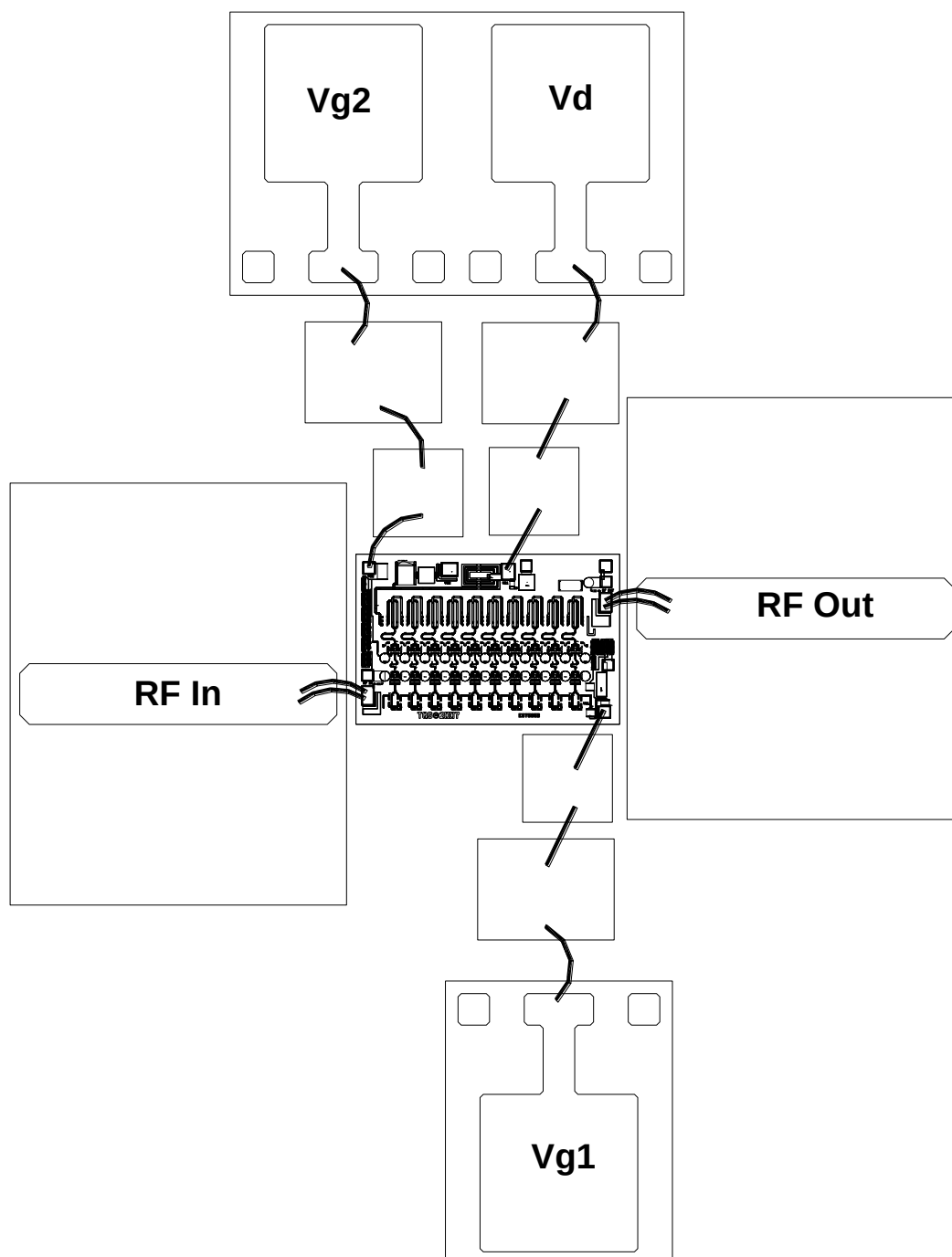
Mechanical Drawing and Bond Pad Description



Unit: millimeters. Die thickness: 0.10, Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad. Ground is backside of die

Pad No.	Label	Pad Size (mm)	Description
1	RF Input	0.090 x 0.148	RF Input Port, matched to 50 ohms, DC blocked
2	VG2	0.090 x 0.090	Gate Voltage Control
3	VD2	0.125 x 0.100	Drain voltage termination, no connection required
4	VD1	0.100 x 0.125	Drain Voltage
5	RF output	0.090 x 0.148	RF Output Port, matched to 50 ohms, DC blocked
6	VG1	0.090 x 0.090	Gate Voltage Control

Recommended Assembly Diagram



Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	TBD	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	N / A	



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free
- PFOS Free

Contact Information

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