Data Sheet May 2000 File Number 4778.1

Power Distribution Controllers

The HIP1015 and HIP1016 are hot swap power controllers. The HIP1015 is targeted for a +12V bus whereas the HIP1016 is targeted for +5V applications. Each has an undervoltage (UV) monitoring and reporting with a threshold level ~17% lower than the nominal +12V and +5V.

The HIP1015 has an integrated charge pump allowing control of up to a +12V bus using an external N-channel MOSFET. The HIP1016 can also be used to control much higher positive or negative voltages in a low side controller configuration. Both the HIP1015 and HIP1016 feature programmable Overcurrent (OC) detection, current limiting regulation with time delay to latch off and soft start.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HIP1015CB	0 to 85	8 Lead SOIC	M8.15
HIP1015CB-T	0 to 85	8 Lead SOIC Tape and Reel	M8.15
HIP1016CB	0 to 85	8 Lead SOIC	M8.15
HIP1016CB-T	0 to 85	8 Lead SOIC Tape and Reel	M8.15

Features

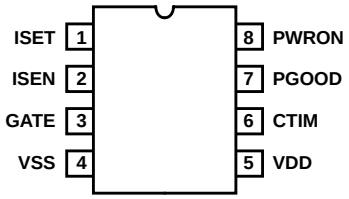
- HOT SWAP Single Power Distribution Control (HIP1015 for 12V, HIP1016 for 5V and Low Side Switch)
- Undervoltage Monitoring and Notification
- Overcurrent Fault Isolation
- Programmable Current Regulation Level
- Programmable Current Limit Time to Latch-Off
- Rail to Rail Common Mode Input Voltage Range (HIP1015)
- Internal Charge Pump Allows the use of N-channel MOSFET (HIP1015)
- Undervoltage and Overcurrent Latch Indicators
- Adjustable Turn-On Ramp
- Protection During Turn On
- Two Levels of Overcurrent Detection Provide Fast Response to Varying Fault Conditions
- Less Than 1µs Response Time to Dead Short

Applications

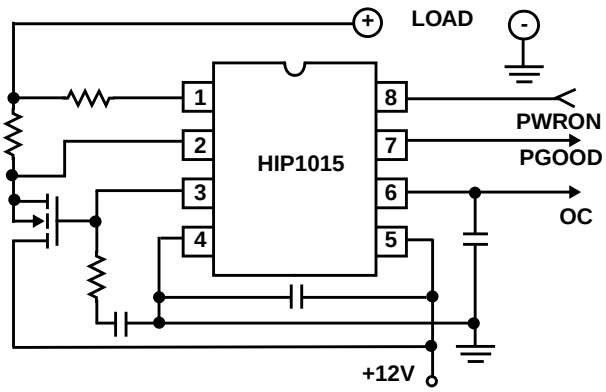
- Power Distribution Control
- Hot Plug Components and Circuitry
- High Side Low Voltage (< +15V) Switching
- Low Side High Voltage (> +15V, Negative V) Switch

Pinout

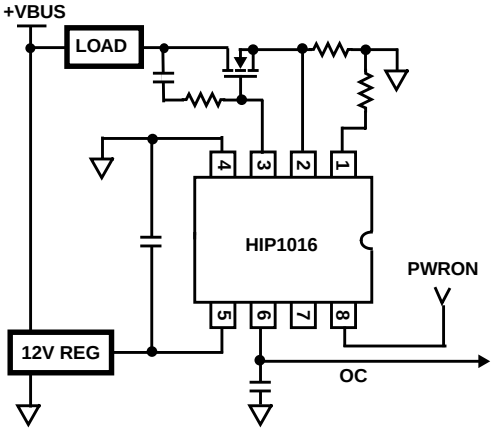
HIP1015, HIP1016 (SOIC)
TOP VIEW



Application One - High Side Controller

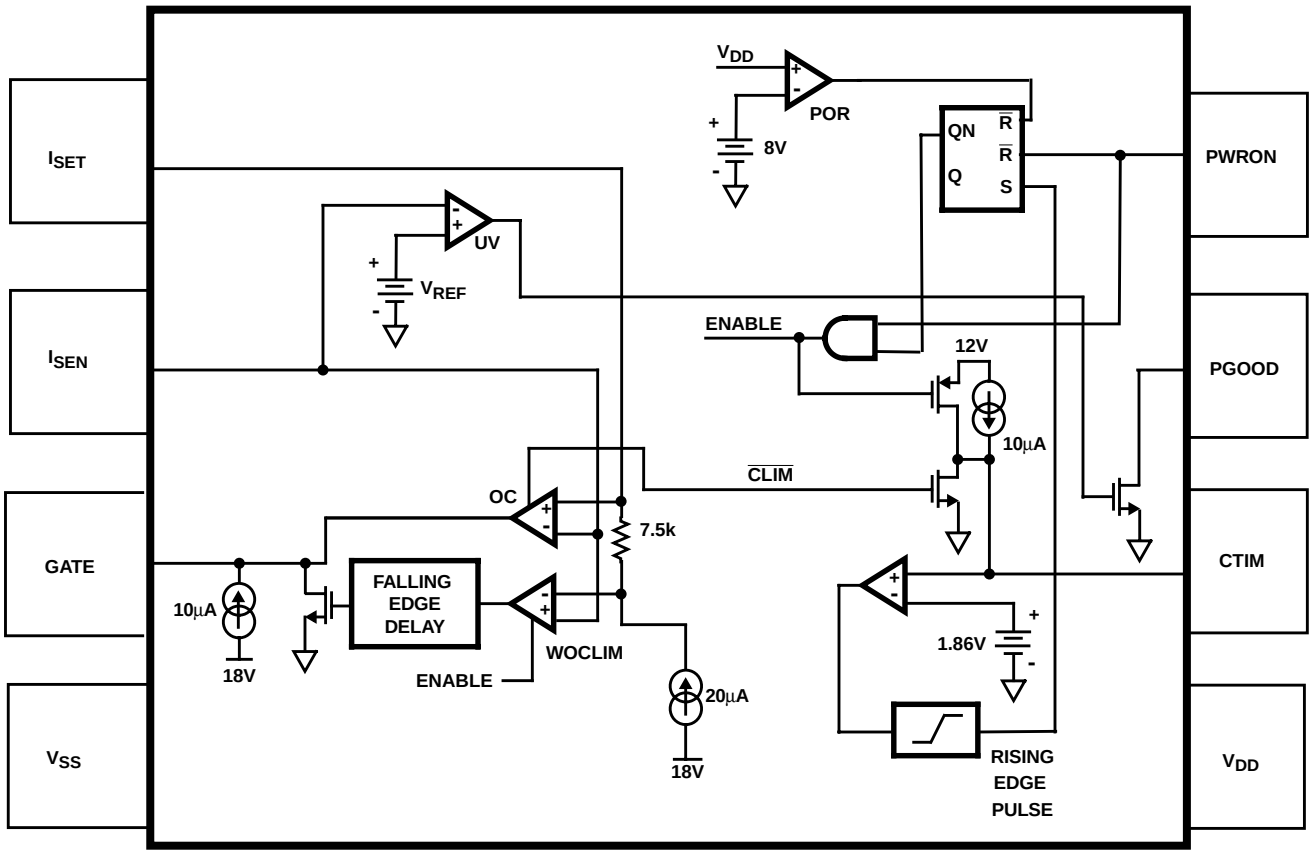


Application Two - Low Side Controller



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Simplified Block Diagram



Pin Descriptions

PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	ISET	Current Set	Connect to the low side of the current sense resistor through the current limiting set resistor. This pin functions as the current limit programming pin.
2	ISEN	Current Sense	Connect to the more positive end of sense resistor to measure the voltage drop across this resistor
3	GATE	External FET Gate Drive Pin	Connect to the gate of the external N-Channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to V_{DD} +5V (HIP1015) and to V_{DD} (HIP1016) by a 10µA current source.
4	VSS	Chip Return	
5	V_{DD}	Chip Supply	12V chip supply. This can be either connected directly to the +12V rail supplying the switched load voltage or to a dedicated V_{SS} +12V supply.
6	CTIM	Current Limit Timing Capacitor	Connect a capacitor from this pin to ground. This capacitor determines the time delay between an overcurrent event and chip output shutdown (current limit time-out). The duration of current limit time-out (in seconds) = 93kΩ x C_{TIM} (Farads).
7	PGOOD	Power Good Indicator	Indicates that the voltage on ISEN pin is within specification. PGOOD is driven by an open drain N-Channel MOSFET and is pulled low when the output is not within specification.
8	PWRON	Power ON	PWRON is used to control and reset the chip. The chip is enabled when PWRON pin is driven high or is open. After a current limit time out, the chip is reset by a low level signal applied to this pin. This input has 20µA pull up capability

Absolute Maximum Ratings $T_A = 25^oC$

V_{DD} . . . . . -0.3V to +16V
GATE . . . . . -0.3V to V_{DD}+8V
ISEN, PGOOD, PWRON, CTIM, ISET. . . . . -0.3V to V_{DD} + 0.3V
ESD Classification 5kV

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +12v+/-15%
Temperature Range (T_A) . . . . . 0^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	98

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. (See Tech Brief, #TB379.1 for details.)
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications V_{DD} = 12V, $T_A = T_J = 0^oC$ to 85^oC, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ISET Current Source	I_{ISET}		18.5	20	21.5	µA
Current Limit Amp Offset Voltage		V_{ISET} - V_{ISEN}	-6	0	6	mV
Current Limit Time-Out Threshold Voltage	C_{TIM}_Vth	CTIM Voltage	1.3	1.8	2.3	V
GATE Response Time To Severe Overcurrent	pd_woc_amp	V_{GATE} to 10.8V	-	100	-	ns
GATE Response Time to Overcurrent	pd_oc_amp	V_{GATE} to 10.8V		600		ns
GATE Turn-On Current	I_{GATE}	V_{GATE} to = 6V	8.4	10	11.6	µA
GATE Pull down Current	OC_GATE_I_4V	Overcurrent	45	75		mA
GATE Pull down Current	WOC_GATE_I_4V	Severe Overcurrent	0.5	0.8	1.5	A
HIP1015 Undervoltage Threshold	$12V_{UV_VTH}$		9.2	9.6	10	V
HIP1015 Undervoltage Disabled	$12V_{UV_VTH_dis}$		V_{DD}+1.9V	V_{DD}+2.5V		V
HIP1015 GATE High Voltage	12VG	GATE Voltage	V_{DD}+4.5V	V_{DD}+5V	-	V
HIP1016 Undervoltage Threshold	$5V_{UV_VTH}$		4.0	4.35	4.5	V
HIP1016 Undervoltage Disabled	$5V_{UV_VTH_dis}$		V_{DD}-3V	V_{DD}-2.5V		V
HIP1016 GATE High Voltage	5VG	GATE Voltage	V_{DD}-1.5V	V_{DD}	-	V
V_{DD} Supply Current	I_{VDD}		-	3	5	mA
V_{DD} POR Rising Threshold	$V_{DD_POR_L2H}$	VDD Low to High	7.8	8.4	9	V
V_{DD} POR Falling Threshold	$V_{DD_POR_H2L}$	VDD High to Low	7.5	8.1	8.7	V
V_{DD} POR Threshold Hysteresis	$V_{DD_POR_HYS}$	$V_{DD_POR_L2H}$ - $V_{DD_POR_H2L}$	0.1	0.3	0.6	V
PWRON Pull-up Voltage	PWRN_V	PWRON Pin Open	2.7	3.2	-	V
PWRON Rising Threshold	PWR_Vth		1.4	1.7	2.0	V
PWRON Hysteresis	PWR_hys		130	170	250	mV
PWRON Pull-Up Current	PWRN_I		9	17	25	µA
C_{TIM} Charging Current	C_{TIM}_ichg0	V_{CTIM} = 0V	16	20	23	µA
C_{TIM} Fault pull-up Current			16	20	23	mA
HIP1015 ISEN Current	ISEN_5V_I		41	72	88	µA
HIP1016 ISEN Current	ISEN_5V_I		100	145	170	µA

HIP1015, HIP1016 Description and Operation

The HIP1015 and HIP1016 are single power supply distribution controllers for generic hot swap applications. The HIP1015 is targeted for +12V switching applications whereas the HIP1016 is targeted for +5V applications as each has an undervoltage (UV) threshold level ~17% lower than the nominal +12V and +5V, respectively.

The HIP1015 and HIP1016 features include a highly accurate programmable Overcurrent (OC) detecting comparator, programmable current limiting regulation with programmable time delay to latch off and programmable soft start turn-on ramp all set with a minimum of external passive components. The HIP1015 and HIP1016 also include severe overcurrent protection that immediately shuts down the MOSFET switch should the load current cause the OC voltage threshold to exceed the programmed OC level by 150mV. Additionally the HIP1015 and HIP1016 have an UV indicator and an OC latch indicator.

Upon initial power up, the HIP1015 or HIP1016 can either isolate the voltage supply from the load by holding the external N-Channel MOSFET switch off or apply the supply rail voltage directly to the load for true hot swap capability. In either case the HIP1015 and HIP1016 turns on in a soft start mode protecting the supply rail from sudden in-rush current. The PWRON pin must be pulled low for the device to isolate the power supply from the load by holding the external N-channel MOSFET off, otherwise with the PWRON pin held high or floating the HIP1015 and HIP1016 will be in true hot swap mode.

At turn-on, the gate capacitor of the external N-Channel MOSFET is charged with a 10µA current source resulting in a programmable ramp (soft start turn-on). The internal HIP1015 charge pump supplies the gate drive for the 12V supply switch driving that gate to V_{DD} +5V. The HIP1016 gate drive is limited to the chip bias voltage.

Load current passes through the external current sense resistor. When the voltage across the sense resistor exceeds the user programmed Overcurrent voltage threshold value, (See Table 1 for R_{ISET} programming resistor value and resulting nominal overcurrent threshold voltage, V_{OC}) the controller enters current regulation. At this time, the time-out capacitor, on C_{TIM} pin starts charging with a 20mA current source and the controller enters the current limit time to latch-off period. The length of the current limit time to latch-off period is set by the single external capacitor (See Table 2 for CTIM capacitor value and resulting nominal current limited time out to latch-off period.) placed from the CTIM pin (pin 6) to ground. The programmed current level is held until either the OC event passes or the time out period expires. If the former is the case then the N-Channel MOSFET is fully enhanced and the C_{TIM} capacitor is discharged. Once CTIM charges to 1.87V, signaling that the time out period has expired an internal latch is set whereby the FET gate is quickly pulled to 0V turning off the N-Channel MOSFET switch, isolating the faulty load.

TABLE 1.

R_{ISET} RESISTOR	NOMINAL OC VTH
10kΩ	200mV
4.99kΩ	100mV
2.5kΩ	50mV
750Ω	15mV

NOTE: Nominal Vth = R_{ISET} x 20µA.

TABLE 2.

C_{TIM} CAPACITOR	NOMINAL CURRENT LIMITED PERIOD
0.022µF	2ms
0.047µF	4.4ms
0.1µF	9.3ms

NOTE: Nominal time-out period in seconds = C_{TIM} x 93kΩ.

The HIP1015 and HIP1016 respond to a severe overcurrent load (defined as a voltage across the sense resistor >150mV over the OC Vth set point) by immediately, driving the N-Channel MOSFET gate to 0V in less than 1µs. The gate voltage is then slowly ramped up turning on the N-Channel MOSFET to the programmed current limit level, this is the start of the time out period.

Upon an UV condition the PGOOD signal will pull low when tied high through a resistor to the logic supply. This pin is an UV fault indicator. For an OC latch off indication, monitor CTIM, pin 6. This pin will rise rapidly from 1.9V to 12V once the time out period expires.

The HIP1015 and HIP1016 are reset after an OC latch-off condition by a low level on the PWRON pin and is turned on by the PWRON pin being driven high.

Application Considerations

During the **Time-Out Delay Period** with the HIP1015 and HIP1016 in current limit mode, the V_{GS} of the external N-Channel MOSFETs is reduced driving the N-Channel MOSFET switch into a high $r_{DS(ON)}$ state. Thus avoid extended time out periods as the external N-Channel MOSFETs may be damaged or destroyed due to excessive internal power dissipation. Refer to the MOSFET manufacturers data sheet for SOA information.

With the high levels of inrush current e.g., highly capacitive loads and motor start up currents, **choosing the current limiting level** is crucial to provide both protection and still allow for this inrush current without latching off. Consider this in addition to the time out delay when choosing MOSFETs for your design.

Physical layout of R_{SENSE} resistor is critical to avoid the possibility of false overcurrent occurrences. Ideally trace routing between the R_{SENSE} resistors and the HIP1015 and HIP1016 is direct and as short as possible with zero current in the sense lines. (See Figure 1.)

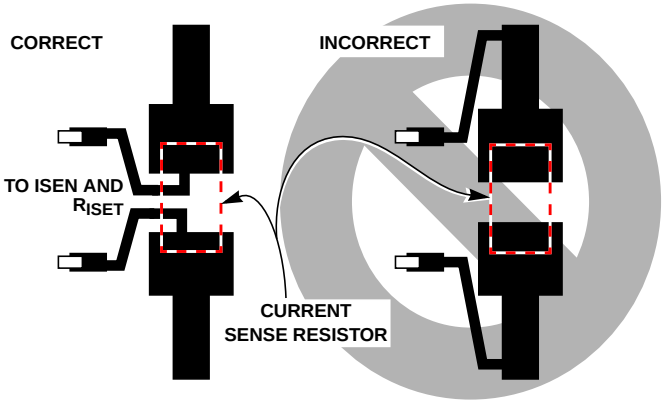


FIGURE 1. SENSE RESISTOR PCB LAYOUT

Using the HIP1016 as a -48V Low Side Hot Swap Power Controller

To supply the required V_{DD}, it is necessary to maintain the chip supply 12V above the -48V bus. This may be accomplished with a +12V Regulator between the voltage rail and pin 5 (VDD). By using a Regulator, the designer may ignore the bus voltage variations. However, a low-cost alternative is to use a Zener diode (See Figure 2 for typical 5A load control) this option is detailed below.

Note that in this configuration the PGOOD feature (pin 7) is not operational.

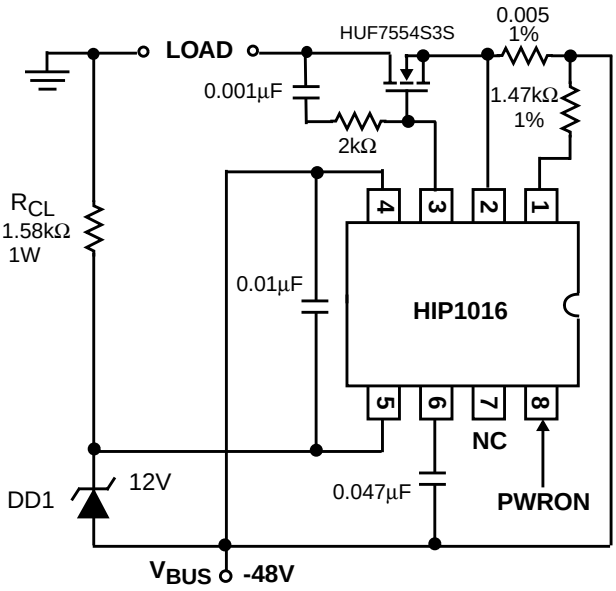


FIGURE 2.

Biasing the HIP1016

Table 3 gives typical component values for biasing the HIP1016 in a 48V application. The formulas and calculations deriving these values are also shown below.

TABLE 3. TYPICAL VALUES FOR A -48V HOT SWAP APPLICATION

SYMBOL	PARAMETER
R_{CL}	1.58kΩ, 1W
DD1	12V Zener Diode, 50mA Reverse Current

When using the HIP1016 to control -48V, a Zener diode may be used to provide the +12V bias to the chip. If a Zener is used then a current limit resistor should also be used. Several items must be taken into account when choosing values for the current limit resistor (R_{CL}) and Zener Diode (DD1):

- The variation of the V_{BUS} (in this case, -48V)
- The chip supply current needs for all functional conditions
- The power rating of R_{CL}.
- The current rating of DD1

Formulas

1. Sizing R_{CL}:
   $R_{CL} = (V_{BUS,MIN} - 12)/I_{CHIP}$
2. Power Rating of R_{CL}:
   $P_{RCL} = I_C(V_{BUS,MAX} - 12)$
3. DD1 Current Rating:
   $I_{DD1} = (V_{BUS,MAX} - 12)/R_{CL}$

Example:

A typical -48V supply may vary from -36 to -72V. Therefore,
$V_{BUS,MAX} = -72V$
$V_{BUS,MIN} = -36V$

$I_{CHIP} = 15mA$ (max)

Sizing R_{CL}:
$R_{CL} = (V_{BUS,MIN} - 12)/I_C$
$R_{CL} = (36 - 12)/0.015$
R_{CL} = 1.6kΩ [Typical Value = 1.58kΩ]

Power Rating of R_{CL}:
$P_{RCL} = I_C(V_{BUS,MAX} - 12)$
$P_{RCL} = (0.015)(72 - 12)$
P_{RCL} = 0.9W [Typical Value = 1W]

DD1 Current Rating:
$I_{DD1} = (V_{BUS,MAX} - 12)/R_{CL}$
$I_{DD1} = (72 - 12)/1.58k\Omega$
I_{DD1} = 38mA [Typical Value = 12V rating, 50mA reverse current]

Typical Performance Curves

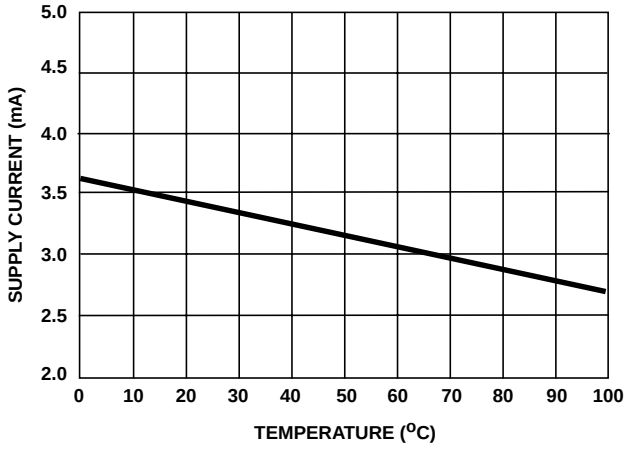


FIGURE 3. VDD BIAS CURRENT

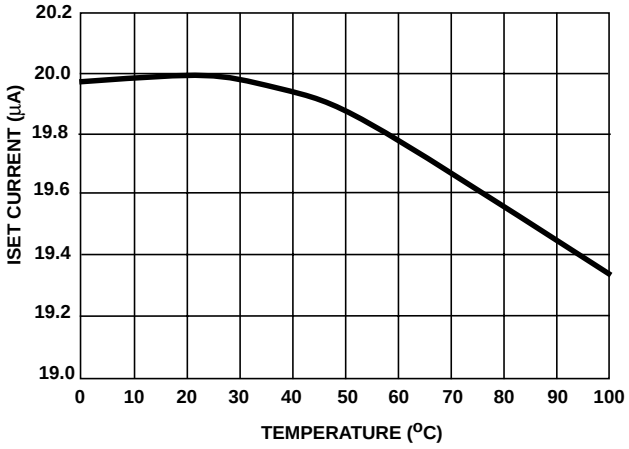


FIGURE 4. ISET SOURCE CURRENT

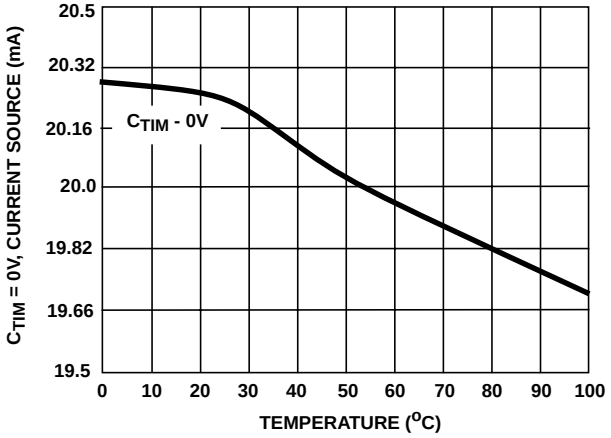


FIGURE 5. C_{TIM} CURRENT SOURCE

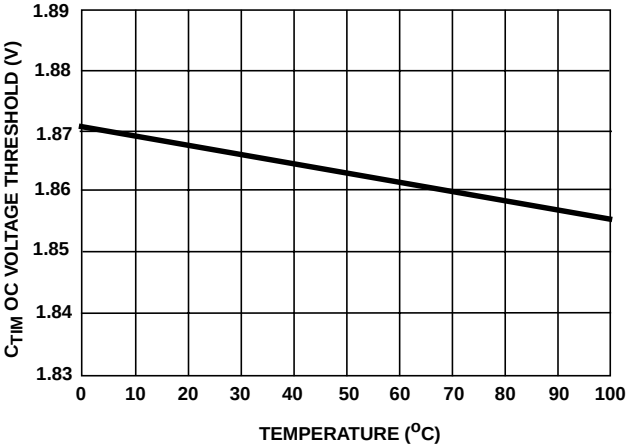


FIGURE 6. C_{TIM} OC VOLTAGE THRESHOLD

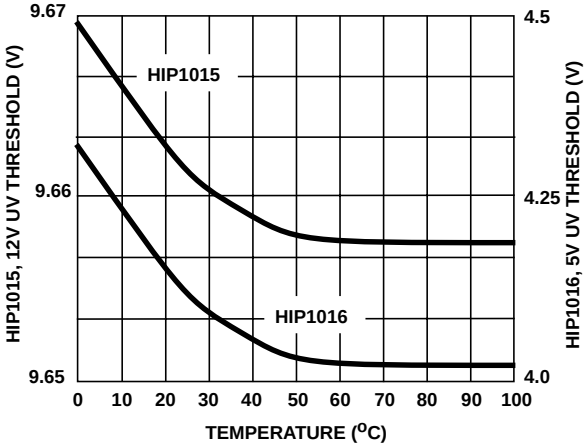


FIGURE 7. UV THRESHOLD

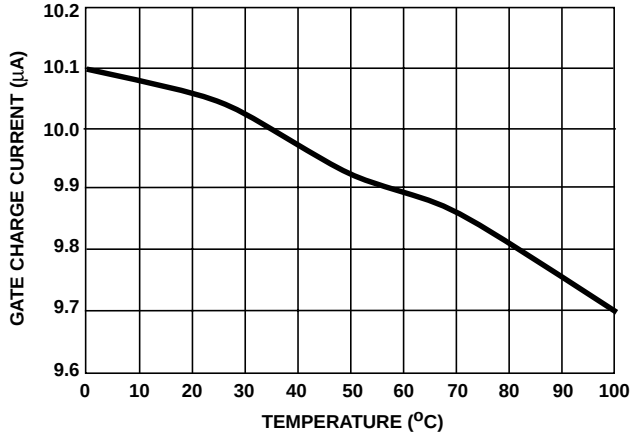


FIGURE 8. GATE CHARGE CURRENT

Typical Performance Curves (Continued)

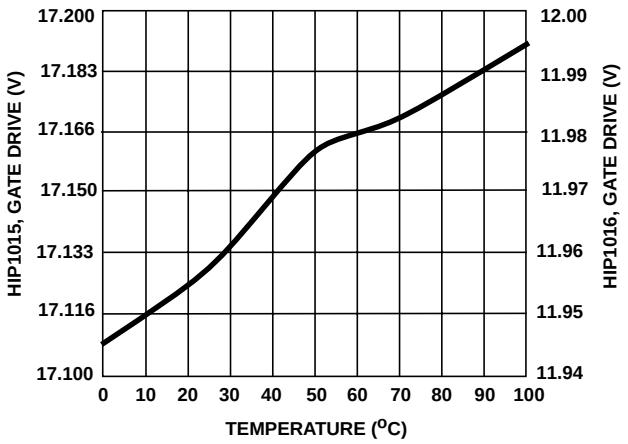


FIGURE 9. GATE DRIVE VOLTAGE, VDD = 12V

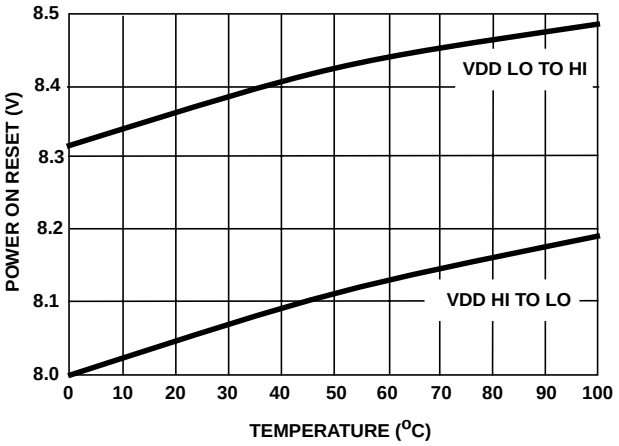


FIGURE 10. POWER ON RESET VOLTAGE THRESHOLD

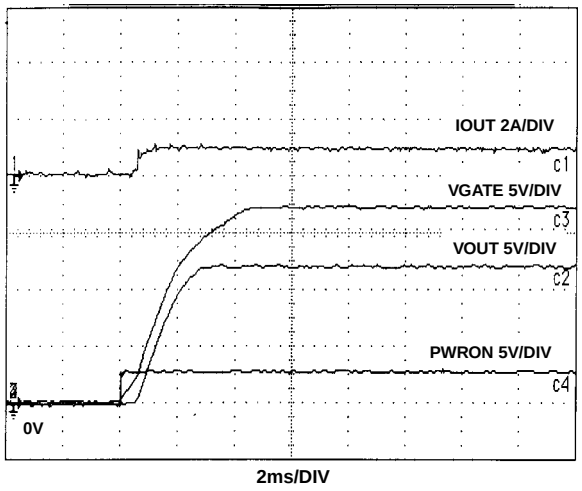


FIGURE 11. HIP1015 HIGH SIDE +12V TURN-ON

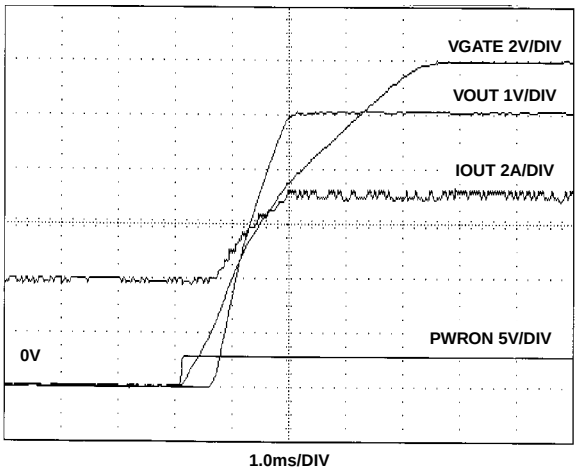


FIGURE 12. HIP1016 HIGH SIDE +5V TURN-ON

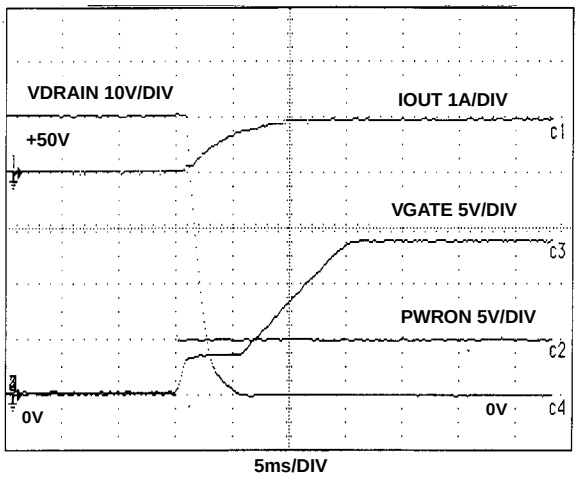


FIGURE 13. +50V LOW SIDE SWITCHING CGATE = 100pF

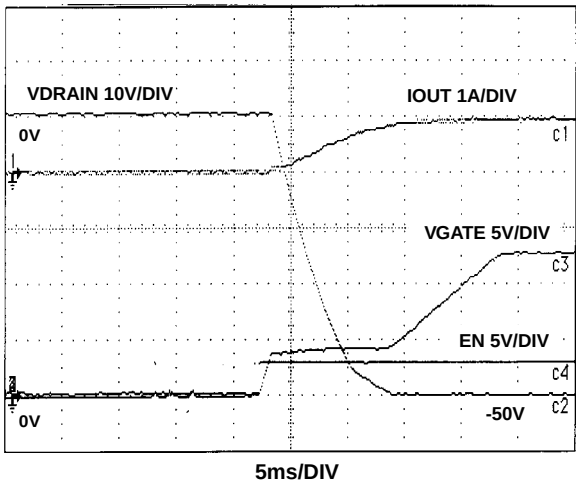


FIGURE 14. -50V LOW SIDE SWITCHING CGATE = 1000pF

Typical Performance Curves (Continued)

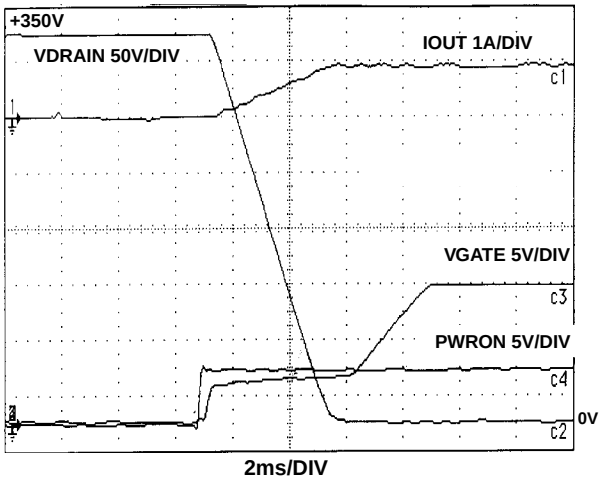


FIGURE 15. +350V LOW SIDE SWITCHING CGATE = 100pF

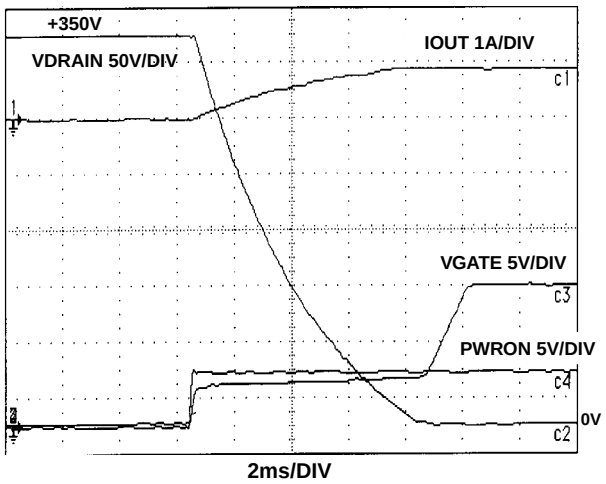


FIGURE 16. +350V LOW SIDE SWITCHING CGATE = 1000pF

HIP1015EVAL1 Board

The HIP1015EVAL1 is configured as a +12V high side switch controller with the OC latch-off level set at ~1.5A. (See Figure 16. for HIP1015EVAL1 schematic and Table 4. for BOM.) Bias and load connection points are provided along with test points for each IC pin. Also included with the HIP1015EVAL1 board is one loose packed HIP1016 for 5V bus switching evaluation.

With the chip to be biased from the +12V bus being switched, through B2, GND B5, the load connected between B3 and B4 and with jumper J1 installed the HIP1015 can be evaluated. PWRON pin pulls high enabling HIP1015 if not driven low.

With the 750Ω Overcurrent Voltage Threshold set resistor (R2) the OC Vth is set to 15mV and with the 10mΩ sense resistor the HIP1015EVAL1 has a nominal OC trip level of 1.5A. The 0.047µF delay time to latch-off capacitors results in a nominal 4.4ms before latch-off of outputs after an OC event.

HIP1016EVAL1 Board

The HIP1016EVAL1 is default configured as a negative voltage low side switch controller with a ~2.4A OC latch-off level. (See Figure 17 for HIP1016EVAL1 schematic and Table 4 for BOM and component description.) This basic configuration is capable of controlling both larger positive or negative potential voltages with minimal changes.

Bias and load connection points are provided in addition to test points, TP1-8 for each IC pin. The terminals, J1 and J4 are for the bus voltage and return, respectively, with the more negative potential being connected to J4. With the load between terminals J2 and J3 the board is now configured for evaluation. The device is enabled through LOGIN, TP9 with a TTL signal. HIP1016EVAL1 includes a level shifting circuit with an opto-coupling device for the PWRON input so that standard TTL logic can be translated to the -V reference for chip control.

When controlling a positive voltage, PWRON can be accessed at TP8.

The HIP1016EVAL1 is provided with a high voltage linear regulator for convenience to provide chip bias from +/-24V to +/-350V. This can be removed and replaced with the zener & resistor bias scheme as discussed earlier. High voltage regulators are no longer available from Intersil but can be purchased from other IC manufacturers.

Reconfiguring the HIP1016EVAL1 board for increased OC latch-off can be done by changing the R_{SENSE} and R_{ISET} resistor values as the provided FET is 75A rated. If evaluation at > 60V, an alternate FET must be chosen with an adequate BV_{DSS}. Table 3 below provides a sample of Intersil Power MOSFET offerings for various bus voltages.

TABLE 4. MOSFETs FOR EVALUATED V_{BUS} VOLTAGE

+/-V_{BUS}	MOSFET
24V	HUF76145
36V	HUF75345
48V	HUF75545, HUF75542
72V	HUF75645
140V	IRF646, IRFR214
350V	IRFP450

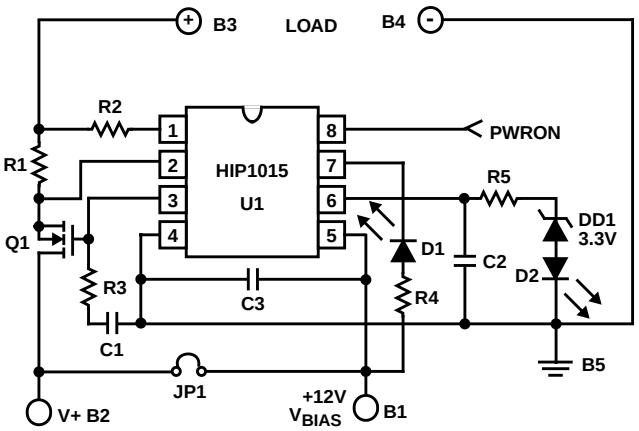


FIGURE 17. HIP1015EVAL1
HIGH SIDE SWITCH APPLICATION

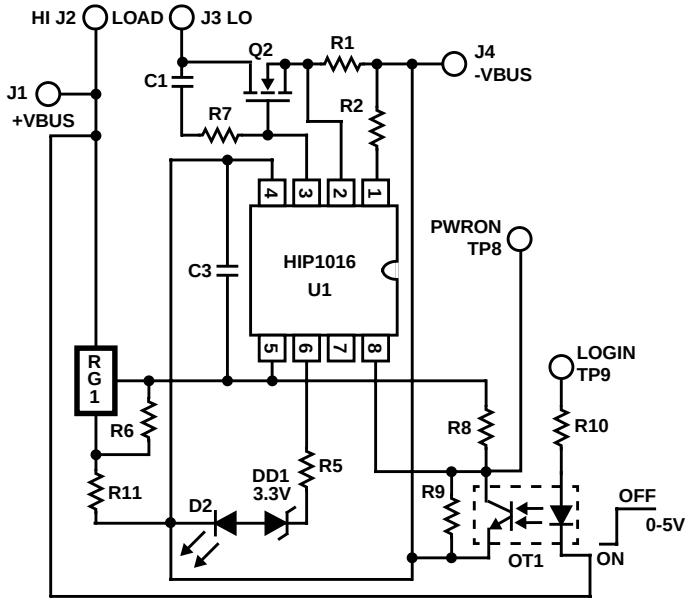


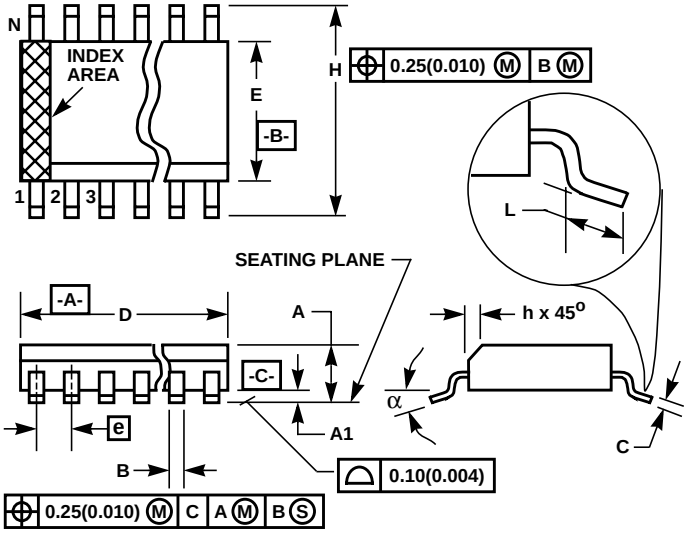
FIGURE 18. HIP1016EVAL1
NEGATIVE VOLTAGE LOW SIDE CONTROLLER

TABLE 5. BILL OF MATERIALS, HIP1015EVAL1, HIP1016EVAL1

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
Q1	HUF76132SK8	INTERSIL CORP, HUF76132SK8, 11.5mΩ, 30V, 11.5A Logic Level N-Channel UltraFET® Power MOSFET
Q2	HUF7554S3S	INTERSIL CORP, HUF7554S3S, 10mΩ, 80V, 75A N-Channel UltraFET® Power MOSFET
R1	Load Current Sense Resistor	Dale, WSL-2512 10mΩ 1W Metal Strip Resistor
HIGH SIDE R2	Overcurrent Voltage Threshold Set Resistor	750Ω 805 Chip Resistor (Vth = 15mV)
LOWSIDE R2	Overcurrent Voltage Threshold Set Resistor	1.21kΩ 805 Chip Resistor (Vth = 24mV)
C2	Time Delay Set Capacitor	0.047µF 805 Chip Capacitor (4.5ms)
C1	Gate Timing Capacitor	0.001µF 805 Chip Capacitor (<2ms)
C3	IC Decoupling Capacitor	0.1µF 805 Chip Capacitor
R3	Gate Stability Resistor	20Ω 805 Chip Resistor
R7	Gate to Drain Resistor	2kΩ 805 Chip Resistor
JP1	Bias Voltage Selection Jumper	Install if switched rail voltage is = +12V+/-15%. Remove and provide separate +12V bias voltage to U1 pin 5 if switched rail voltage is lower than 12V.
R4, R5	LED Series Resistors	2.32kΩ 805 Chip Resistor
D1, D2	Fault Indicating LEDs	Low Current Red SMD LED
DD1	Fault Voltage Dropping Diode	3.3V Zener Diode, SOT-23 SMD 350mW
OT1	PWRON Level Shifting Opto-Coupler	PS2801-1 NEC
R8	Level Shifting Bias Resistor	2.32kΩ 805 Chip Resistor
R9	Level Shifting Bias Resistor	1.18kΩ 805 Chip Resistor
R10	Level Shifting Bias Resistor	200Ω 805 Chip Resistor
RG1	HIP5600IS	High Voltage Linear Regulator
R6	Linear Regulator RF1	1.78kΩ 805 Chip Resistor
R11	Linear Regulator RF2	15kΩ 805 Chip Resistor
TP1-TP8	Test Points for Device Pin Numbers 1-8	

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Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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