IS28F002BV/BLV

262,144 x 8 SmartVoltage BOOT BLOCK FLASH MEMORY

ADVANCE INFORMATION NOVEMBER 1997

- **SmartVoltage Technology**
  — 5V or 12V Program/Erase
  — 2.7V, 3.3V or 5V Read Operation
- **High-Performance Read**
  (Maximum Access Times)
  — 5V: 60/80/120 ns
  — 3V: 110/130/150 ns
  — 2.7V: 120 ns
- **Low Power Consumption**
  — Max 60 mA Read Current at 5V
  — Max 30 mA Read Current at 3V/2.7V
- **Optimized Array Block Architecture**
  — One 16-KB Protected Top or Bottom Boot Block
  — Two 8-KB Parameter Blocks
  — One 96-KB Main Block
  — One 128-KB Main Block
- **Hardware-Protection for Boot Block**
- **Software EEPROM Emulation with Parameter Blocks**
- **Industrial Temperature Operation**
  — –40°C to +85°C
- **Automated Byte Write and Block Erase**
  — Industry-Standard Command User Interface
  — Status Registers
  — Erase Suspend Capability
- **SRAM-Compatible Write Interface**
- **Automatic Power Savings Feature**
  — 1 mA Typical Icc Active Current in Static Operation
- **Reset/Deep Power-Down Input**
  — 0.2 µA Icc Typical
  — Provides Reset for Boot Operations
- **Hardware Data Protection Feature**
  — Erase/Write Lockout during Power Transitions
- **Industry-Standard Surface Mount Packaging**
  — 40-Lead TSOP
- **Footprint Upgradeable to 4-Mbit and to 8-Mbit Boot Block Flash Memories**

DESCRIPTION

This datasheet contains specifications for the products in the SmartVoltage 2-Mbit boot block flash memory. These are the BV/BLV suffix products which offer 2.7-3.6V, 3.0-3.6V, and 5V V_{CC} operation.

New Features in the SmartVoltage Products

The SmartVoltage boot block flash memory offers identical operation with the BX/BL 12V program products, except for the differences listed below. All other functions are equivalent to current products, including signatures, write commands, and pinouts.

- $\overline{WP}$ pin has replaced a DU (Don't Use) pin. Connect the $\overline{WP}$ pin to control signal or to V_{CC} or GND (in this case, a logic-level signal can be placed on DU pin).
- 5V program/erase operation has been added. If switching V_{PP} for write protection, switch to GND (not 5V) for complete write protection. To take advantage of 5V write-capability, allow for connecting 5V to V_{PP} and disconnecting 12V from V_{PP} line.
- Enhanced circuits optimize low V_{CC} performance, allowing operation down to V_{CC} = 2.7V/3.3V.

If you are using BX/BL 12V V_{PP} boot block products today, you should account for the differences listed above and also allow for connecting 5V to V_{PP} and disconnecting 12V from V_{PP} line, if 5V writes are desired.

Main Features

ISSI's SmartVoltage technology is the most flexible voltage solution in the flash industry, providing two discrete voltage supply pins: V_{CC} for read operation, and V_{PP} for program and erase operation. Discrete supply pins allow system designers to use the optimal voltage levels for their design. The IS28F002BV/BLV provides program/erase capability at 5V or 12V. The IS28F002BV/BLV allows reads with V_{CC} at 2.7V-3.6V, 3.3V ± 0.3V or 5V. Since many designs read from the flash memory a large percentage of the time, read operation using the 2.7V range can provide great power savings. If read performance is an issue, 5V V_{CC} provides faster read access times.

For program and erase operations, 5V V_{PP} operation eliminates the need for in system voltage converters, while 12V V_{PP} operation provides faster program and erase for situations where 12V is available, such as manufacturing or designs where 12V is in-system. For design simplicity, V_{CC} and V_{PP} can be hooked up to the same 5V ± 10% source.

The IS28F002BV/BLV boot block flash memory is a high-performance, 2-Mbit (2,097,152 bit) flash memory organized as 256K by 8 bits.

Separately erasable blocks, including a hardware-lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each) and main blocks (one block of 98,304 bytes and one block of 131,072 bytes), define the boot block flash family architecture. Each block can be independently erased and programmed.

The boot block is located at either the top (denoted by T suffix) or the bottom (B suffix) of the address map in order to accommodate different microprocessor protocols for boot code location. The hardware-lockable boot block provides complete code security for the kernel code required for system initialization. Locking and unlocking of the boot block is controlled by $\overline{WP}$ and/or $\overline{RP}$.

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the boot block flash memory. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verifications, thereby unburdening the microprocessor or microcontroller of these tasks. The Status Register (SR) indicates the status of the WSM and whether it successfully completed the desired program or erase operation.

Program and Erase Automation allows program and erase operations to be executed using an industry-standard two-write command sequence to the CUI. Data writes are performed in byte increments.

Each byte in the flash memory can be programmed independently of other memory locations, unlike erases, which erase all locations within a block simultaneously.

The 2-Mbit SmartVoltage boot block flash memory is also designed with an Automatic Power Savings (APS) feature which minimizes system battery current drain, allowing for very low power designs. To provide even greater power savings, the boot block family includes a deep power-down mode which minimizes power consumption by turning most of the flash memory's circuitry off. This mode is controlled by the $\overline{RP}$ pin and its usage is discussed along with other power consumption issues.

Additionally, the $\overline{RP}$ pin provides protection against unwanted command writes due to invalid system bus conditions that may occur during system reset and power-up/down sequences. For example, when the flash memory powers-up, it automatically defaults to the read array mode, but during a warm system reset, where power continues uninterrupted to the system components, the flash memory could remain in a non-read mode. Consequently, the system Reset signal should be tied to $\overline{RP}$ to reset the memory to normal read mode upon activation of the Reset signal.

SMARTVOLTAGE FLEXIBILITY

		V_{CC}			V_{PP}	
Product Name	**Bus Width**	**2.7V-3.6V**	**3.3V ± 0.3V**	**5V ± 10%**	**5V ± 10%**	**12V ± 5%**
IS28F002BV/BLV	x8	X	X	X	X	X

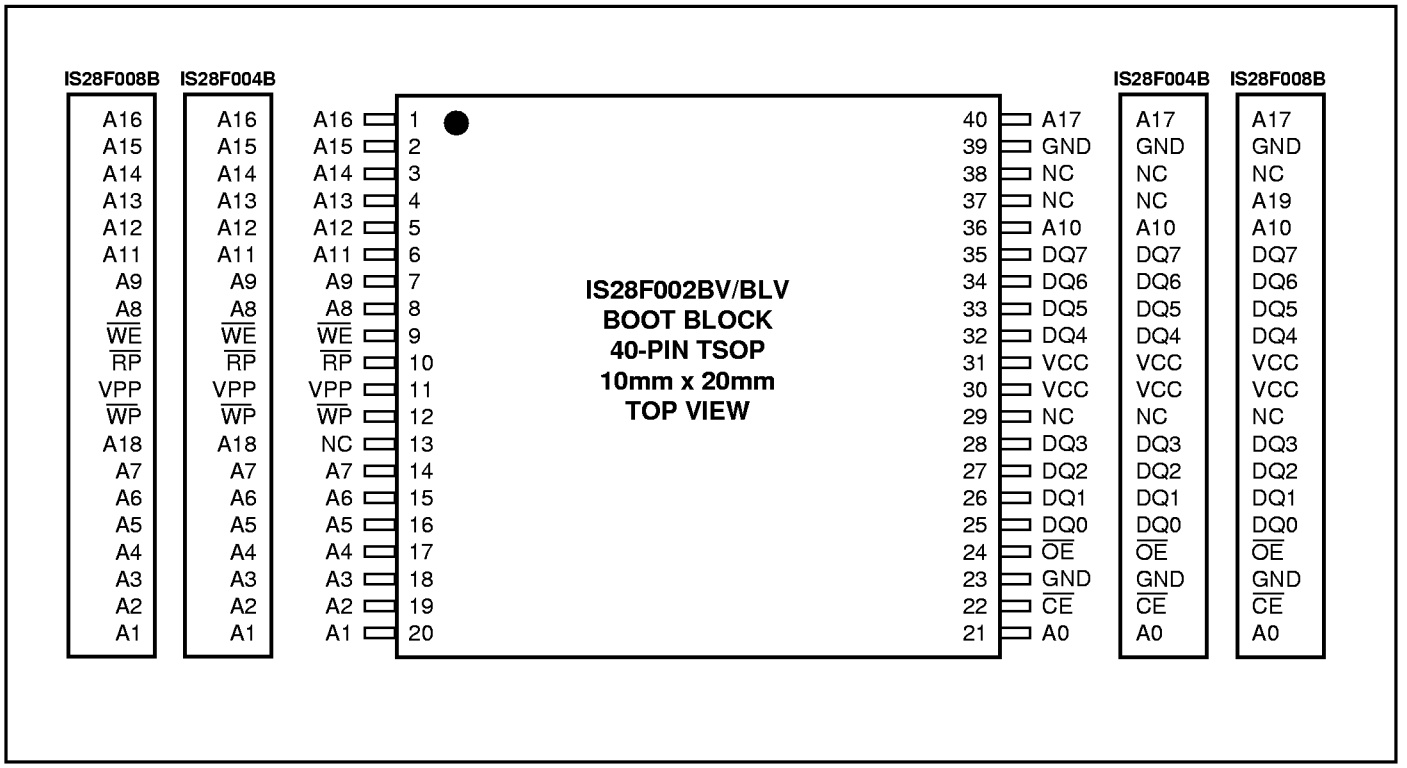
PIN DESCRIPTIONS

Symbol	Type	Name and Function
A0-A17	INPUT	**ADDRESS INPUT:** for memory addresses. Addresses are internally latched during a write cycle.
A9	INPUT	**ADDRESS INPUT:** When A9 is at V_{HH} the signature mode is accessed. During this mode, A0 decodes between the manufacturer and device IDs.
DQ0-DQ7	INPUT OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second $\overline{CE}$ and $\overline{WE}$ cycle during a Program command. Inputs commands to the Command User Interface when $\overline{CE}$ and $\overline{WE}$ are active. Data is internally latched during the write cycle. Outputs array, Intelligent Identifier and Status Register data. The data pins float to tri-state when the chip is deselected or the outputs are disabled.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low. $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels. If $\overline{CE}$ and $\overline{RP}$ are high, but not at a CMOS high level, the standby current will increase due to current flow through the $\overline{CE}$ and $\overline{RP}$ input stages.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and array blocks. $\overline{WE}$ is active low. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{RP}$	INPUT	**RESET/DEEP POWER-DOWN:** Uses three voltage levels (V_{IL}, V_{IH}, and V_{HH}) to control two different functions: reset/deep power-down mode and boot block unlocking. **When $\overline{RP}$ Is at logic low, the device is in reset/deep power-down mode,** which puts the outputs at High-Z, resets the Write State Machine, and draws minimum current. **When $\overline{RP}$ Is at logic high, the device is in standard operation.** When $\overline{RP}$ transitions from logic-low to logic-high, the device defaults to the read array mode. **When $\overline{RP}$ is at V_{HH}, the boot block is unlocked** and can be programmed or erased. This overrides any control from the $\overline{WP}$ input.

PIN DESCRIPTIONS *(continued)*

Symbol	Type	Name and Function
$\overline{WP}$	INPUT	**WRITE PROTECT:** Provides a method for unlocking the boot block in a system without a 12V supply. **When $\overline{WP}$ is at logic low, the boot block is locked,** preventing program and erase operations to the boot block. If a program or erase operation is attempted on the boot block when $\overline{WP}$ is low, the corresponding status bit (bit 4 for program, bit 5 for erase) will be set in the Status Register to indicate the operation failed. **When $\overline{WP}$ is at logic high, the boot block Is unlocked** and can be programmed or erased. **NOTE:** This feature is overridden and the boot block unlocked when $\overline{RP}$ is at V_{HH}.
V_{CC}		**DEVICE POWER SUPPLY:** 5.0V ± 10%, 3.3V ± 0.3V, 2.7V-3.6V
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** For erasing memory array blocks or programming data in each block, a voltage either of 5V ± 10% or 12V ± 5% must be applied to this pin. When $V_{PP} < V_{PPLK}$ all blocks are locked and protected against Program and Erase commands.
GND		**GROUND:** For all internal circuitry.
NC		**NO CONNECT:** Pin may be driven or left floating.

PIN CONFUGURATIONS: 40-Pin TSOP



PRODUCT DESCRIPTION

Memory Blocking Organization

This product features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others. The block sizes have been chosen to optimize their functionality for common applications of nonvolatile storage. The combination of block sizes in the boot block architecture allow the integration of several memories into a single chip. For the address locations of the blocks, see the memory map.

BOOT BLOCK - 1 x 16-KB

The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller based system. The 16-Kbyte (16,384 bytes) boot block is located at either the top (denoted by T suffix) or the bottom (B suffix) of the address map to accommodate different microprocessor protocols for boot code location. This boot block features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the V_{PP}, $\overline{RP}$ and $\overline{WP}$ pins.

PARAMETER BLOCKS - 2 x 8-KB

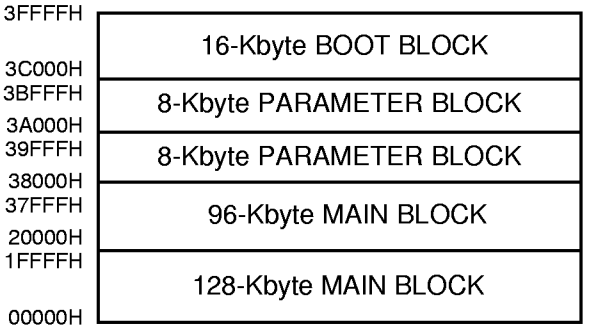
The boot block architecture includes parameter blocks to facilitate storage of frequently updated small parameters that would normally require an EEPROM. By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. Each boot block component contains two parameter blocks of 8 Kbytes (8,192 bytes) each. The parameter blocks are not write-protectable.

MAIN BLOCKS - 1 x 96-KB + 1 x 128-KB

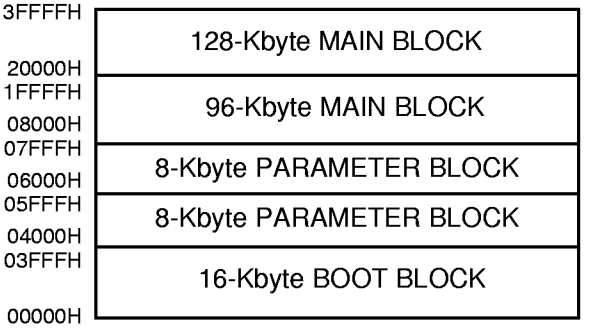
After the allocation of address space to the boot and parameter blocks, the remainder is divided into main blocks for data or code storage. Each 2-Mbit device contains one 96-Kbyte (98,304 byte) block and one 128-Kbyte (131,072 byte) block. See the memory maps for each device for more information.

Byte-Wide x8 Memory Maps

IS28F002BV/BLVT



IS28F002BV/BLVB



PRINCIPLES OF OPERATION

Flash memory combines EPROM functionality with in-circuit electrical write and erase. The boot block flash family utilizes a Command User Interface (CUI) and automated algorithms to simply write and erase operations. The CUI allows for 100% TTL-level control inputs, fixed power supplies during erasure and programming, and maximum EPROM compatibility.

When $V_{PP} < V_{PPLK}$, the device will only successfully execute the following commands: Read Array, Read Status Register, Clear Status Register and intelligent identifier mode. The device provides standard EPROM read, standby and output disable operations. Manufacturer identification and device identification data can be accessed through the CUI or through the standard EPROM A9 high voltage access (V_{ID}) for PROM programming equipment.

The same EPROM read, standby and output disable functions are available when 5V or 12V is applied to the V_{PP} pin. In addition, 5V or 12V on V_{PP} allows write and erase of the device. All functions associated with altering memory contents: Program and Erase, Intelligent Identifier Read, and Read Status are accessed via the CUI.

The internal Write State Machine (WSM) completely automates program and erase, beginning operation signaled by the CUI and reporting status through the Status Register. The CUI handles the $\overline{WE}$ interface to the data and address latches, as well as system status requests during WSM operation.

Bus Operations

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized in Bus Operations.

Read Operations

READ ARRAY

When $\overline{RP}$ transitions from V_{IL} (reset) to V_{IH}, the device will be in the read array mode and will respond to the read control inputs ($\overline{CE}$, address inputs, and $\overline{OE}$) without any commands being written to the CUI.

When the device is in the read array mode, five control signals must be controlled to obtain data at the outputs.

- $\overline{WE}$ must be logic high (V_{IH})
- $\overline{CE}$ must be logic low (V_{IL})
- $\overline{OE}$ must be logic low (V_{IL})
- $\overline{RP}$ must be logic high (V_{IH})

In addition, the address of the desired location must be applied to the address pins.

If the device is not in read array mode, as would be the case after a program or erase operation, the Read Mode command (FFH) must be written to the CUI before reads can take place.

During system design, consideration should be taken to ensure address and control inputs meet required input slew rates of <10 ns.

Mode	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	A0	A–1	V_{PP}	DQ0-7
Read (1,2,3)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	X	X	D_{OUT}
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	High Z
Standby	V_{IH}	V_{IH}	X	X	X	X	X	X	High Z
Deep Power-Down(9)		V_{IL}	X	X	X	X	X	X	X High Z
Intelligent(4) Identifier (Mfr)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	D5H
Intelligent Identifier (Device)(4,5) Table	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{IH}	X	X	See Intelligent Identifier
Write(6,7,8)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	X	X	D_{IN}

Notes:
1. Refer to DC Characteristics.
2. X can be V_{IL}, V_{IH} for control pins and addresses, V_{PPLK} or V_{PPH} for V_{PP}.
3. See DC Characteristics for V_{PPLK}, V_{PPH1}, V_{PPH2}, V_{HH}, V_{IO} voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence, A1-A17 = X.
5. See Intelligent Identifier Table for device IDs.
6. Refer to Command Bus Definitions for valid D_{IN} during a write operation.
7. Command writes for block erase or byte write are only executed when $V_{PP} = V_{PPH1}$ or V_{PPH2}.
8. To write or erase the boot block, hold $\overline{RP}$ at V_{HH} or $\overline{WP}$ at V_{IH}.
9. $\overline{RP}$ must be at GND ± 0.2V to meet the maximum deep power-down current specified.

INTELLIGENT IDENTIFIERS

To read the manufacturer and device codes, the device must be in intelligent identifier read mode, which can be reached using two methods: by writing the intelligent identifier command (90H) or by taking the A9 pin to V_{ID}. Once in intelligent identifier read mode, A0 = 0 outputs the manufacturer's identification code and A0 = 1 outputs the device code. To return to read array mode, write a Read Array command (FFH).

Write Operations

COMMAND USER INTERFACE (CUI)

The Command User Interface (CUI) is the interface between the microprocessor and the internal chip controller. Commands are written to the CUI using standard microprocessor write timings. The available commands are Read Array, Read Intelligent Identifier, Read Status Register, Clear Status Register, Erase and Program. The three read modes are read array, intelligent identifier read, and status register read. For Program or Erase commands, the CUI informs the Write State Machine (WSM) that a write or erase has been requested. During the execution of a Program command, the WSM will control the programming sequences and the CUI will only respond to status reads. During an erase cycle, the CUI will respond to status reads and erase suspend. After the WSM has completed its task, it will set the WSM Status bit to a "1" (ready), which indicates that the CUI can respond to its full command set. Note that after the WSM has retuned control to the CUI, the CUI will stay in the current command state until it receives another command.

COMMAND FUNCTION DESCRIPTION

Device operations are selected by writing specific commands into the CUI. "Command Codes and Descriptions" and "Command Bus Definitions" define the available commands.

INTELLIGENT IDENTIFIER TABLE

Product	Mfr. ID	Device ID	
		T	B
		(Top Boot)	(Bottom Boot)
IS28F002BV/BLV	D5H	7CH	7DH

COMMAND CODES AND DESCRIPTIONS

Code	Device Mode	Description
00	Invalid/Reserved	Unassigned commands that should not be used. Right reserved to redefine these codes for future functions.
FF	Read Array/ Program or Erase Abort	Places the device in read array mode, so that array data will be output on the data pins. This command can also be used to cancel erase and program sequences after their setup commands have been issued. To cancel after issuing an Erase Set-Up command, issue this command, which will reset to read array mode. To cancel a program operation after issuing a Program Setup command, issue two Read Array commands in sequence to reset to read array mode. If a program or erase operation has already been initiated to the WSM this command can not cancel that operation in progress.
40	Program Setup	Sets the CUI into a state such that the next write will load the Address and Data registers. After this command is executed, the outputs default to the Status Register. A two Read Array command sequence (FFH) is required to reset to Read Array after the Program Setup command. The second write after the Program Setup command will latch addresses and data, initiating the program algorithm. The device outputs Status Register data when $\overline{OE}$ is enabled. To read array data, issue a Read Array command.
10	Alternate Prog Setup	(See 40H/Program Setup)
20	Erase Setup	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will set both the Program Status and Erase Status bits of the Status Register to a "1," place the device into the read Status Register state, and wait for another command.

(continued)

COMMAND CODES AND DESCRIPTIONS

Code	Device Mode	Description
D0	Erase Resume/ Erase Confirm	If the previous command was an Erase Setup command, then the CUI will latch address and data, and begin erasing the block indicated on the address pins. During erase, the device will respond only to the Read Status Register and Erase Suspend commands and will output Status Register data when $\overline{OE}$ is toggled low. Status Register data is updated by toggling either $\overline{OE}$ or $\overline{CE}$ low.
B0	Erase Suspend	Valid only while an erase operation is in progress and will be ignored in any other circumstance. Issuing this command will begin to suspend erase operation. The Status Register will indicate when the device reaches erase suspend mode. In this mode, the CUI will respond only to the Read Array, Read Status Register, and Erase Resume commands and the WSM will also set the WSM Status bit to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input control pins except $\overline{RP}$, which will immediately shut down the WSM and the remainder of the chip, if it is made active. During a suspend operation, the data and address latches will remain closed, but the address pads are able to drive the address into the read path.
70	Read Status Register	Puts the device into the read Status Register mode, so that reading the device outputs Status Register data, regardless of the address presented to the device. The device automatically enters this mode after program or erase has completed. This is one of the two commands that is executable while the WSM is operating.
50	Clear Status Register	The WSM can only set the Program Status and Erase Status bits in the Status Register to "1;" it cannot clear them to "0." The Status Register operates in this fashion for two reasons. The first is to give the host CPU the flexibility to read the status bits at any time. Second, when programming a string of bytes, a single Status Register query after programming the string may be more efficient, since it will return the accumulated error status of the entire string.
90	Intelligent Identifier	Puts the device into the intelligent identifier read mode, so that reading the device will output the manufacturer and device codes. (A0 = 0 for manufacturer, A0 = 1 for device, all other address inputs are ignored).

COMMAND BUS DEFINITIONS

	First Bus Cycle			Second Bus Cycle		
Command	**Operation**	**Address**	**Data**	**Operation**	**Address**	**Data**
Read Array	Write	X	FFH			
Intelligent Identifier(1)	Write	X	90H	Read	IA	ID
Read Status Register(2,4)	Write	X	70H	Read	X	SRD
Clear Status Register(3)	Write	X	50H			
Byte Write	Write	WA	40H	Write	WA	WD
Alternate Byte Write(6,7)	Write	WA	10H	Write	WA	WD
Block Erase/Confirm(6,7)	Write	BA	20H	Write	BA	D0H
Erase Suspend/Resume(5)	Write	X	B0H	Write	X	D0H

Notes:
1. Bus operations are defined in "Bus Operations".
2. IA = Identifier Address: A0 = 0 for manufacturer code, A0 = 1 for device code.
3. SRD = Data read from Status Register.
4. ID = Intelligent Identifier Data. Following the Intelligent Identifier command, two read operations access manufacturer and device codes.
5. BA = Address within the block being erased.
6. WA = Address to be written. WD = Data to be written at location WD.
7. Either 40H or 10H command is valid.

ADDRESS
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
SRD = Status Register Data
ID = Identifier Data
WD = Write Data

STATUS REGISTER BIT DEFINITION

	Bits	Status Register	Notes
WSMS	7	SR.7 = WRITE STATE MACHINE 1 = Ready 0 = Busy	Check Write State Machine bit first to determine Byte program or Block Erase completion, before checking Program or Erase Status bits.
ESS	6	SR.6 = ERASE-SUSPEND 1 = Erase Suspended 0 = Erase In Progress/ Completed	When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to ESS bit remains set to "1" until an Erase Resume command is issued.
ES	5	SR.5 = ERASE STATUS (ES) 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to "1," WSM has applied the maximum number of erase pulses to the block and is still unable to verify successful block erasure.
DWS	4	SR.4 = PROGRAM STATUS (DWS) 1 = Error in Byte Program 0 = Successful Byte Program	When this bit is set to "1," WSM has attempted but failed to program a byte.
VPPS	3	SR.3 = V_{PP} STATUS (V_{PPS}) 1 = V_{PP} Low Detect, Oper. Abort 0 = V_{PP} OK	The V_{PP} Status bit does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Byte Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PP} Status bit is not guaranteed to report accurate feedback between V_{PPLK} and V_{PPH}.
R	2, 1, 0	SR.2-SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	These bits are reserved for future use and should be masked out when polling the Status Register.

STATUS REGISTER

The device Status Register indicates when a program or erase operation is complete, and the success or failure of that operation. To read the Status Register write the Read Status (70H) command to the CUI. This causes all subsequent read operations to output data from the Status Register until another command is written to the CUI. To return to reading from the array, issue a Read Array (FFH) command.

The Status Register bits are output on DQ0-DQ7.

Important: *The contents of the Status Register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last in the read cycle.* This prevents possible bus errors which might occur if Status Register contents change while being read. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the Status Register will not indicate completion of a program or erase operation.

When the WSM is active, the SR.7 register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation.

Clearing the Status Register

The WSM sets status bits 3 through 7 to "1," and clears bits 6 and 7 to "0," but cannot clear status bits 3 through 5 to "0." Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register (50H) command, because these bits indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence) before reading the Status Register to determine if an error occurred during that series. Clear the Status Register before beginning another command or sequence. Note, again, that a Read Array command must be issued before data can be read from the memory or intelligent identifier.

PROGRAM MODE

Programming is executed using a two-write sequence. The Program Setup command is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of intemally timed events to:

1. Program the desired bits of the addressed memory byte.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within a byte being changed to a "0."

If the user attempts to program "1"s, there will be no change of the memory cell content and no error occurs.

The Status Register indicates programming status: while the program sequence is executing, bit 7 of the Status Register is a "0." The Status Register can be polled by toggling either $\overline{CE}$ or $\overline{OE}$. While programming, the only valid command is Read Status Register.

When programming is complete, the Program Status bits should be checked. If the programming operation was unsuccessful, bit 4 of the Status Register is set to a "1" to indicate a Program Failure. If bit 3 is set to a "1," then V_{PP} was not within acceptable limits, and the WSM did not execute the programming sequence.

The Status Register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, reads from the Memory Array or Intelligent Identifier cannot be accomplished until the CUI is given the appropriate command.

ERASE MODE

To erase a block, write the Erase Setup and Erase Confirm commands to the CUI, along with the addresses identifying the block to be erased. These addresses are latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1." Only one block can be erased at a time.

The WSM will execute a sequence of internally timed events to:

1. Program all bits within the block to "0."
2. Verify that all bits within the block are sufficiently programmed to "0."
3. Erase all bits within the block to "1."
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the Status Register is a "0."

When the Status Register indicates that erasure is complete, check the Erase Status bit to verify that the erase operation was successful. If the Erase operation was unsuccessful, bit 5 of the Status Register will be set to a "1," indicating an Erase Failure. If V_{PP} was not within acceptable limits after the Erase Confirm command is issued, the WSM will not execute an erase sequence; instead, bit 5 of the Status Register is set to a "1" to indicate an Erase Failure, and bit 3 is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits.

Clear the Status Register before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, reads from the Memory Array, Status Register, or Intelligent Identifier cannot be accomplished until the CUI is given the Read Array command.

Suspending and Resuming Erase

Since an erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from another block of the memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The Status Register will indicate if or when the erase operation has been suspended.

At this point, a Read Array command can be written to the CUI in order to read data from blocks other than that which is being suspended. The only other valid command at this time is the Erase Resume command or Read Status Register command.

During erase suspend mode, the chip can go into a pseudo-standby mode by taking $\overline{CE}$ to V_{IH}, which reduces active current.

To resume the erase operation, enable the chip by taking $\overline{CE}$ to V_{IL}, then issuing the Erase Resume command, which continues the erase sequence to completion. As with the end of a standard erase operation, the Status Register must be read, cleared, and the next instruction issued in order to continue.

Boot Block Locking

The boot block family architecture features a hardware-lockable boot block so that the kernel code for the system can be kept secure while the parameter and main blocks are programmed and erased independently as necessary. Only the boot block can be locked independently from the other blocks.

$V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

For complete write protection of all blocks in the flash device, the V_{PP} programming Voltage can be held low. When V_{PP} is below V_{PPLK}, any program or erase operation will result in a error in the Status Register.

$\overline{WP} = V_{IL}$ FOR BOOT BLOCK LOCKING

When $\overline{WP} = V_{IL}$, the boot block is locked and any program or erase operation to the boot block will result in an error in the Status Register. All other blocks remain unlocked in this condition and can be programmed or erased normally. Note that this feature is overridden and the boot block unlocked when $\overline{RP} = V_{HH}$.

$\overline{RP} = V_{HH}$ OR $\overline{WP}$ V_{IH} FOR BOOT BLOCK UNLOCKING

Two methods can be used to unlock the boot block:

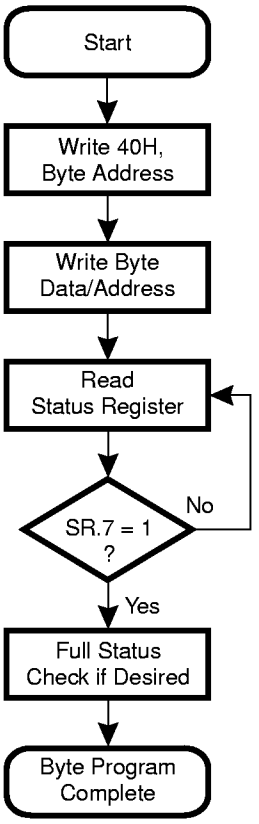
1. $\overline{WP} = V_{IH}$
2. $\overline{RP} = V_{HH}$

If both or either of these two conditions are met, the boot block will be unlocked and can be programmed or erased.

WRITE PROTECTION TRUTH TABLE FOR SMARTVOLTAGE BOOT BLOCK FAMILY

V_{PP}	$\overline{RP}$	$\overline{WP}$	Write Protection Provided
V_{IL}	X	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	X	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	V_{IL}	Boot Lock Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

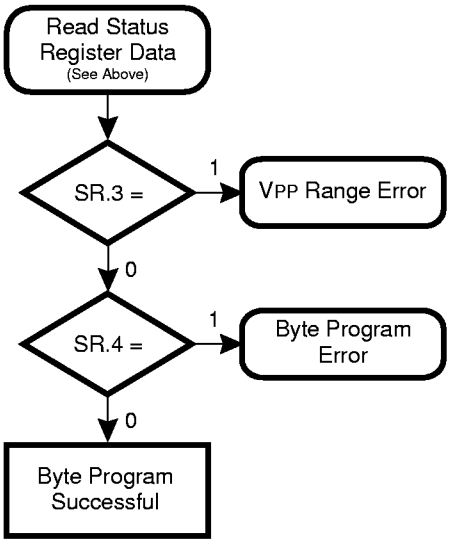
AUTOMATED BYTE PROGRAMMING FLOWCHART



Bus Operation	Command	Comments
Write	Setup Program	Data = 40H Addr = Byte to Program
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Dats Toggle $\overline{CE}$ or $\overline{OE}$ to update SRD.
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent Byte Writes. SR Full Status Check can be done after each Byte Write, or after a sequence of Byte Writes. Write FFH after the last write operation to reset device to read array mode.

Full Status Check Procedure



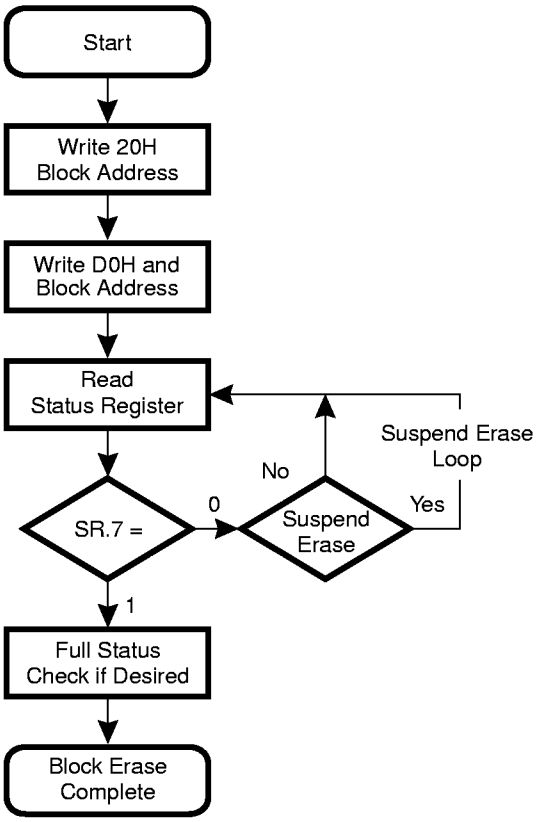
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = Byte Program Error

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.4 is only cleared by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

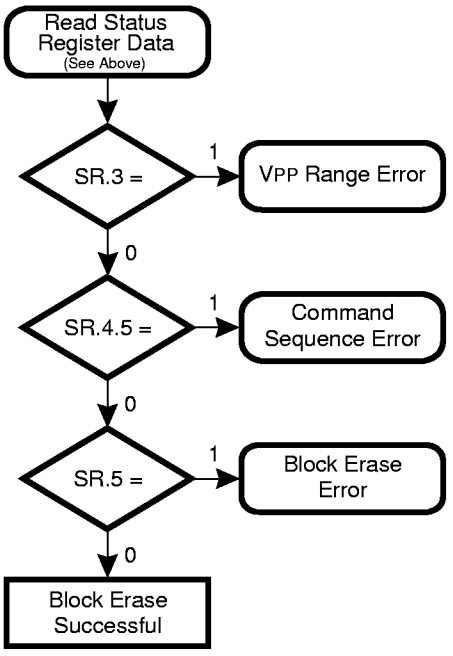
AUTOMATED BLOCK ERASE FLOWCHART



Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data Toggle $\overline{CE}$ or $\overline{OE}$ to Update Status Register
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.
Full Status Check can be done after each block erase, or after a sequence of block erasures.
Write FFH after the last operation to reset device to read array mode.

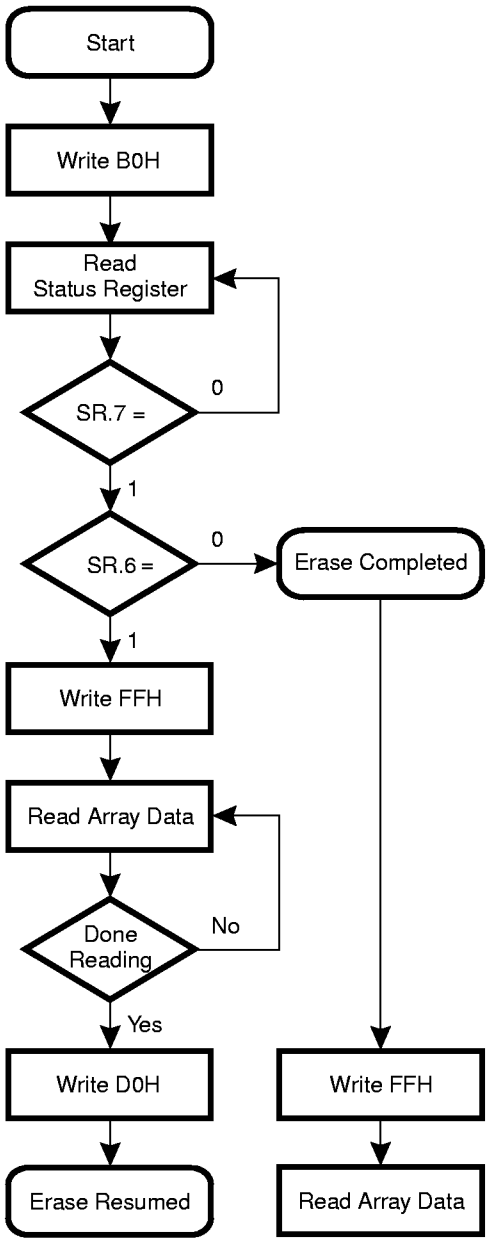
Full Status Check Procedure



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both = 1 Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.
SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

ERASE SUSPEND/RESUME FLOWCHART



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Toggle $\overline{CE}$ or $\overline{OE}$ to update SRD. Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being erased.
Write	Erase Resume	Data = D0H Addr = X

Power Consumption

ACTIVE POWER

With $\overline{CE}$ at a logic-low level and $\overline{RP}$ at a logic-high level, the device is placed in the active mode. Refer to the DC Characteristics table for I_{CC} current values.

AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings (APS) provides low-power operation during active mode. Power Reduction Control (PRC) circuitry allows the device to put itself into a low current state when not being accessed. After data is read from the memory array, PRC logic controls the device's power Consumption by entering the APS mode where typical I_{CC} current is less than 1 mA. The device stays in this static state with outputs valid until a new location is read.

STANDBY POWER

With $\overline{CE}$ at a logic-high level (V_{IH}), and the CUI in read mode, the memory is placed in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the status of the $\overline{OE}$ signal. When $\overline{CE}$ is at logic-high level during erase or program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

DEEP POWER-DOWN MODE

The SmartVoltage boot block family supports a low typical I_{CC} in deep power-down mode, which turns off all circuits to save power. This mode is activated by the $\overline{RP}$ pin when it is at a logic-low (GND ± 0.2V).

During read modes, the $\overline{RP}$ pin going low deselects the memory and places the output drivers in a high-impedance state. Recovery from the deep power-down state, requires a minimum access time of t_{PHQV} (see AC Characteristics table).

During erase or program modes, $\overline{RP}$ low will abort either erase or program operations, but the memory contents are no longer valid as the data has been corrupted by the $\overline{RP}$ function. As in the read mode above, all internal circuitry is turned off to achieve the power savings.

$\overline{RP}$ transitions to V_{IL}, or turning power off to the device will clear the Status Register.

Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. The CUI is reset to the read mode after power-up, but the system must drop $\overline{CE}$ low or present a new address to ensure valid data at the outputs.

A system designer must guard against spurious writes when Vcc voltages are above V_{LKO} and V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until $\overline{RP}$ is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset ($\overline{RP}$ connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

$\overline{RP}$ CONNECTED TO SYSTEM RESET

The use of $\overline{RP}$ during system reset is important with automated write/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization would not occur because the flash memory may be providing status information instead of array data. The Flash memories allow proper CPU initialization following a system reset by connecting the $\overline{RP}$ pin to the same $\overline{RESET}$ signal that resets the System CPU.

V_{CC}, V_{PP} AND $\overline{RP}$ TRANSITIONS

The CUI latches commands as issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its default state upon power-up, after exit from deep power-down mode, or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read array mode.

After any byte write or block erase operation is complete and even after V_{PP} transitions down to V_{PPLK}, the CUI must be reset to read array mode via the Read Array command if accesses to the flash memory are desired.

Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling methods. System designers should consider three supply current issues:

1. Standby current levels (Iccs)
2. Active current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of $\overline{CE}$.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

V_{PP} TRACE ON PRINTED CIRCUIT BOARDS

Designing for in-system writes to the flash memory requires special consideration of the V_{PP} power supply trace by the printed circuit board designer. The V_{PP} pin supplies the flash memory cells current for programming and erasing. One should use similar trace widths and layout considerations given to the Vcc power supply trace. Adequate V_{PP} supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
T_A	Commercial Operating Temperature		
	During Read	0 to +70	°C
	During Block Erase and Byte Write	0 to +70	°C
	Temperature Bias	–10 to +80	°C
T_A	Industrial Operating Temperature		
	During Read	–40 to +85	°C
	During Block Erase and Byte Write	–40 to +85	°C
	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +125	°C
V_{TERM}	Voltage on Any Pin (except V_{CC}, V_{PP}, A9 and $\overline{RP}$) with Respect to GND	–2.0 to +7.0(2)	V
V_{TERM}	Voltage on Pin $\overline{RP}$ or Pin A9 with Respect to GND	–2.0 to +13.5(2,3)	V
V_{PP}	Program Voltage with Respect to GND during Block Erase and Byte Write	–2.0 to +14.0(2,3)	V
V_{CC}	Supply Voltage with Respect to GND	–2.0 to + 7.0(2)	V
	Output Short Circuit Current	100(4)	mA

Notes:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is –0.5V on input/output pins. During transitions, this level may undershoot to –2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
3. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns. Maximum DC voltage on $\overline{RP}$ or A9 may overshoot to 13.5V for periods <20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

***WARNING:** Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may effect device reliability.*

COMMERCIAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	0	+70	°C
Vcc	Vcc Supply Voltage (3.3V ± 0.3V)	3.0	3.6	V
	Vcc Supply Voltage (5V ± 10%)[1]	4.50	5.50	V

Notes:
1. 10% Vcc specifications apply to the 60, 80, and 120 ns product versions in their standard test configuration.

Applying V_{CC} Voltages

When applying V_{CC} voltage to the device, a delay may be required before initiating device operation, depending on the V_{CC} ramp rate. If Vcc ramps slower than 1V/100 µs (0.01 V/µs) then no delay is required. If Vcc ramps faster than 1V/100 µs (0.01 V/µs), then a delay of 2 µs is required before initiating device opeation. $\overline{RP}$ = GND is recommended during power-up to protect against spurious write signals when V_{CC} is between V_{LKO} and V_{CCMIN}.

Vcc Ramp Rate	Required Timing
≤ 1V/100 µs	No delay required.
> 1V/100 µs	A delay time of 2 µs is required before any device operation is initiated, including read operations, command writes, program operations, and erase operations. This delay is measured beginning from the time V_{CC} reaches V_{CCMIN} (2.7V for 2.7V-3.6V operation, 3.0V for 3.3V ± 0.3V operation; and 4.5V for 5V operation).

Notes:
1. These requirements must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3V and 5V operation, the system should first transition V_{CC} from the existing voltage range to GND, and then to the new voltage. Any time the V_{CC} supply drops below V_{CCMIN}, the chip may be reset, aborting any operations pending or in progress.
3. These guidelines must be followed for any V_{CC} transition from GND.

DC CHARACTERISTICS, COMMERCIAL

Symbol	Description	Test Conditions	3.3V ± 0.3V Typ.	3.3V ± 0.3V Max.	5V ± 10% Typ.	5V ± 10% Max.	Unit
I_{IL}	Input Load Current(1)	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or GND	—	±1.0	—	±1.0	µA
I_{LO}	Output Leakage Current(1)	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or GND	—	±10	—	±10	µA
I_{CCS}	V_{CC} Standby Current(1,3)	**CMOS Levels**: V_{CC} = V_{CC} Max $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{CC} ± 0.2V	60	110	50	130	µA
		TTL Levels: V_{CC} = V_{CC} Max $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}	0.4	1.5	0.8	2	mA
I_{CCD}	V_{CC} Deep Power-Down Current(1)	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND $\overline{RP}$ = GND ± 0.2V	0.2	8	0.2	8	µA
I_{CCR}	V_{CC} Read Current(1,5,6)	**CMOS Inputs:** V_{CC} = V_{CC} Max $\overline{CE}$ = GND, $\overline{OE}$ = V_{CC}, f = 10 MHz (5V), 5 MHz (3.3V) I_{OUT} = 0 mA, Inputs = GND ± 0.2V or V_{CC} ± 0.2V	15	30	50	60	mA
		TTL Inputs: V_{CC} = V_{CC} Max $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} f = 10 MHz (5V), 5 MHz (3.3V) I_{OUT} = 0 mA, Inputs = V_{IL} or V_{IH}	15	30	55	65	mA
I_{CCW}	V_{CC} Write Current(1,4)	V_{PP} = V_{PPH1} (at 5V) Write in Progress	13	30	30	50	mA
		V_{PP} = V_{PPH2} (at 12V) Write in Progress	10	25	30	45	mA
I_{CCE}	V_{CC} Erase Current(1,4)	V_{PP} = V_{PPH1} (at 5V) Block Erase in Progress	13	30	18	35	mA
		V_{PP} = V_{PPH2} (at 12V) Block Erase in Progress	10	25	18	30	mA
I_{CCES}	V_{CC} Erase Suspend (1,2) Current	$\overline{CE}$ = V_{IH} Block Erase Suspend	3	8	5	10	mA
I_{PPS}	V_{PP} Standby Current(1)	V_{PP} < V_{PPH2}	±0.5	±15	±0.5	±10	µA
I_{PPD}	V_{PP} Deep Power-Down Current(1)	$\overline{RP}$ = GND ± 0.2V	0.2	5	0.2	5	µA
I_{PPR}	V_{PP} Read Current(1)	V_{PP} ≤ V_{PPH2}	50	200	30	200	µA
I_{PPW}	V_{PP} Current(1,4)	V_{PP} = V_{PPH1} (at 5V) Write in Progress	13	30	13	25	mA
		V_{PP} = V_{PPH2} (at 12V) Write in Progress	8	25	8	20	mA
I_{PPE}	V_{PP} Erase Current(1,4)	V_{PP} = V_{PPH1} (at 5V) Block Erase in Progress	13	30	10	20	mA
		V_{PP} = V_{PPH2} (at 12V) Block Erase in Progress	8	25	5	15	mA
I_{PPES}	V_{PP} Erase Suspend Current(1)	V_{PP} = V_{PPH} Block Erase Suspend in Progress	50	200	30	200	µA

(continued)

DC CHARACTERISTICS, COMMERCIAL (Continued)

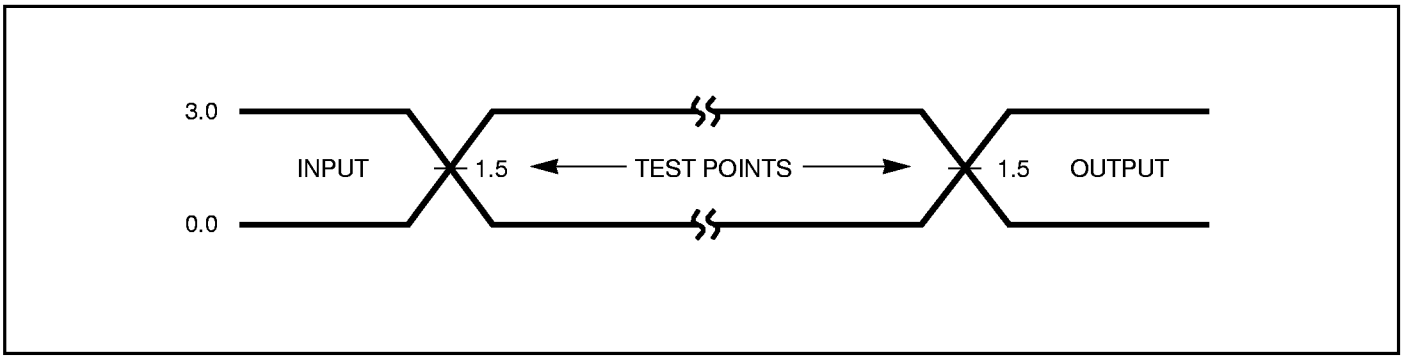
Symbol	Description	Test Conditions	3.3V ± 0.3V Min	3.3V ± 0.3V Max	5V ± 10% Min	5V ± 10% Max	Unit
$I_{\overline{RP}}$	$\overline{RP}$ Boot Block Unlock Current[1,4]	$\overline{RP} = V_{HH}$	—	500	—	500	µA
I_{ID}	A9 Intelligent Identifier Current[1,4]	A9 = V_{ID}	—	500	—	500	µA
V_{ID}	A9 Intelligent Identifier Voltage		11.4	12.6	11.4	12.6	V
V_{IL}	Input Low Voltage		–0.5	0.8	–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5V	2.0	V_{CC} + 0.5V	V
V_{OL}	Output Low Voltage	V_{CC} = V_{CC} Min. I_{OL} = 5.8 mA (5V), 2 mA (3.3V)	—	0.45	—	0.45	V
V_{OH1}	Output High Voltage (TTL)	V_{CC} = V_{CC} Min. I_{OH} = –2.5 mA	2.4	—	2.4	—	V
V_{OH2}	Output High Voltage (CMOS)	V_{CC} = V_{CC} Min. I_{OH} = –2.5 mA	0.85 x V_{CC}	—	0.85 x V_{CC}	—	V
		V_{CC} = V_{CC} Min. I_{OH} = –100 µA	V_{CC} – 0.4V	—	V_{CC} – 0.4V	—	V
V_{PPLK}	V_{PP} Lock-Out Voltage[3]	Total Write Protect	0	1.5	0	1.5	V
V_{PPH1}	V_{PP} (Prog/Erase Operations)	V_{PP} at 5V	4.5	5.5	4.5	5.5	V
V_{PPH2}	V_{PP} (Prog/Erase Operations)	V_{PP} at 12V	11.4	12.6	11.4	12.6	V
V_{LKO}	V_{CC} Erase/Write Lock Voltage[8]		2	—	2	—	V
V_{HH}	$\overline{RP}$ Unlock Voltage		11.4	12.6	11.4	12.6	V

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance[4]	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance[4,7]	V_{OUT} = 0V	10	12	pF

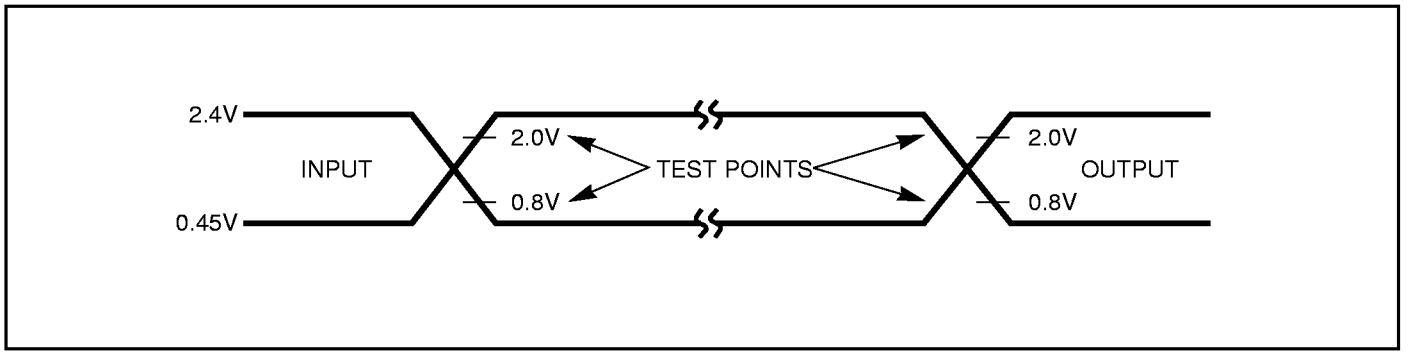
Notes:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, T_A = +25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the device is read while in erase suspend, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases and byte writes are inhibited when V_{PP} = V_{PPLK}, and not guaranteed in the range between V_{PPH1} and V_{PPLK}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
7. For the IS28F002B address pin A10 follows the C_{OUT} capacitance numbers.
8. For all BV/BLV parts, V_{LKO} = 2.0V for both 3.3V and 5V operations.

3.3V INPUTS AND MEASUREMENT POINTS



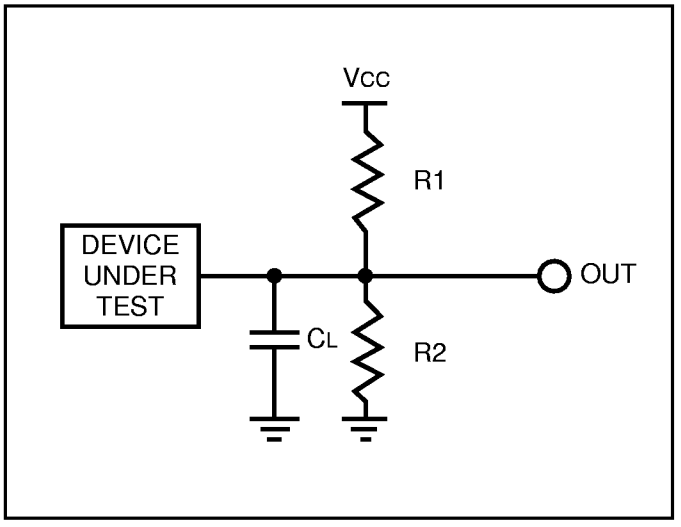
Note:
AC test inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

5V INPUTS AND MEASUREMENT POINTS



Note:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

TEST CONFIGURATION



TEST CONFIGURATION COMPONENT VALUES

Test Configuration	C_L (pF)	R1 (Ω)	R2 (Ω)
3.3V Standard Test	50	989	773
5V Standard Test	100	585	394
5V High-Speed Test	50	585	394

Note: C_L includes jig capacitance

AC CHARACTERISTICS, READ ONLY OPERATIONS, COMMERCIAL[2,3]

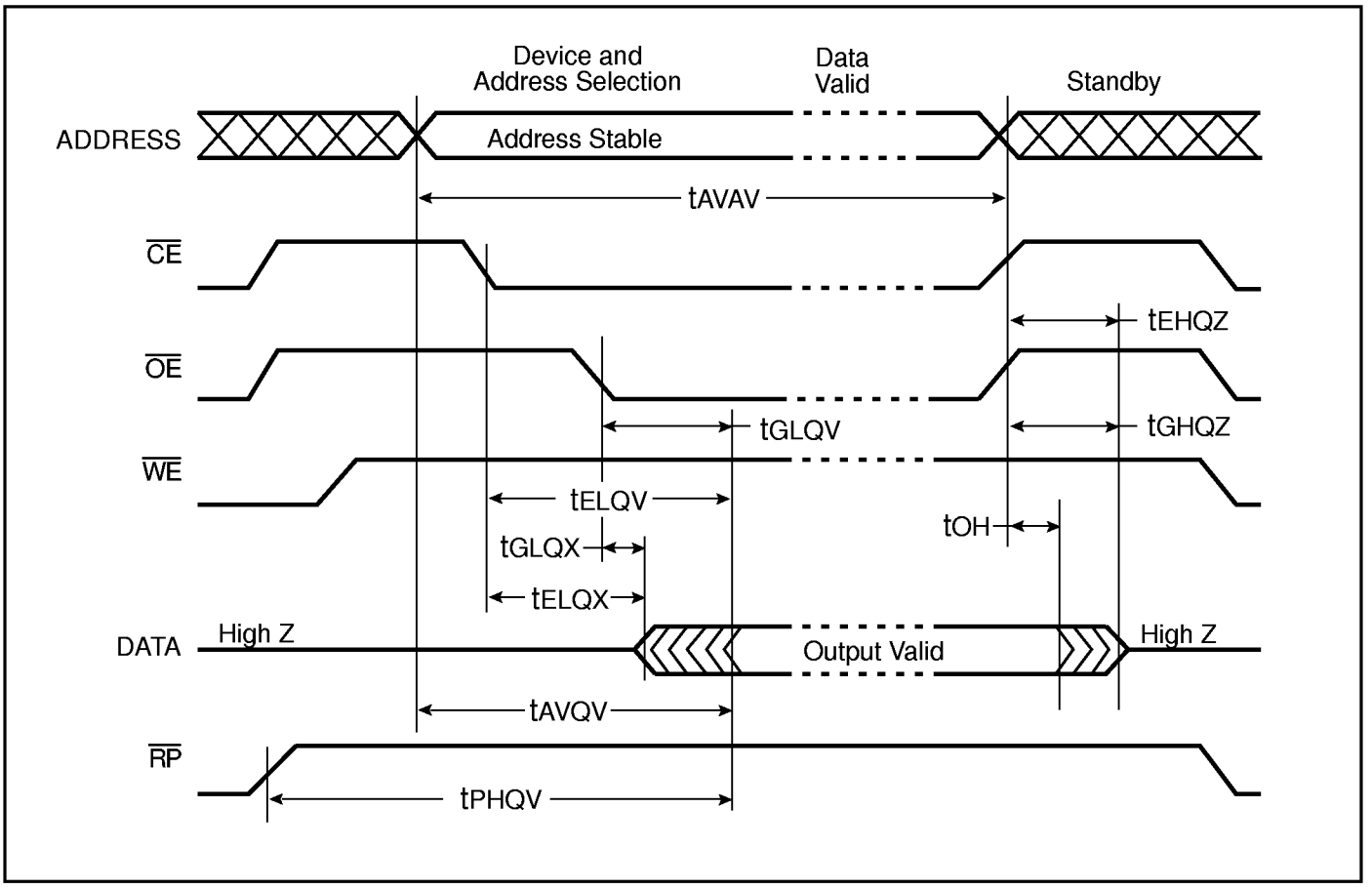
		Product	-60						
		Vcc	3.3V ± 0.3V[4]		5V ± 10%[5]		5V ± 10%[6]		
		Load	50 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Read Cycle Time		110	—	60	—	70	—	ns
t_{AVQV}	Address to Output Delay		—	110	—	60	—	70	ns
t_{ELQV}	$\overline{CE}$ to Output Delay[2]		—	110	—	60	—	70	ns
t_{PHQV}	$\overline{RP}$ to Output Delay		—	0.8	—	0.45	—	0.45	µs
t_{GLQV}	$\overline{OE}$ to Output Delay[2]		—	50	—	25	—	30	ns
t_{ELQX}	$\overline{CE}$ to Output in Low Z[3]		0	—	0	—	0	—	ns
t_{EHQZ}	$\overline{CE}$ to Output in High Z[3]		—	25	—	20	—	20	ns
t_{GLQX}	$\overline{OE}$ to Output in Low Z[3]		0	—	0	—	0	—	ns
t_{GHQZ}	$\overline{OE}$ to Output in High Z[3]		—	25	—	20	—	20	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change, Whichever Occurs First[3]		0	—	0	—	0	—	ns

AC CHARACTERISTICS, READ ONLY OPERATIONS, COMMERCIAL[2,3]

		Product	-80				-120				
		Vcc	3.3V ± 0.3V[4]		5V ± 10%[6]		3.3V ± 0.3V[4]		5V ± 10%[6]		
		Load	50 pF		100 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Read Cycle Time		150	—	80	—	180	—	120	—	ns
t_{AVQV}	Address to Output Delay		—	150	—	80	—	180	—	120	ns
t_{ELQV}	$\overline{CE}$ to Output Delay[2]		—	150	—	80	—	180	—	120	ns
t_{PHQV}	$\overline{RP}$ to Output Delay		—	0.8	—	0.45	—	0.8	—	0.45	µs
t_{GLQV}	$\overline{OE}$ to Output Delay[3]		—	90	—	40	—	90	—	40	ns
t_{ELQX}	$\overline{CE}$ to Output in Low Z[3]		0	—	0	—	0	—	0	—	ns
t_{EHQZ}	$\overline{CE}$ to Output in High Z[3]		—	80	—	30	—	80	—	30	ns
t_{GLQX}	$\overline{OE}$ to Output in Low Z[3]		0	—	0	—	0	—	0	—	ns
t_{GHQZ}	$\overline{OE}$ to Output in High Z[3]		—	60	—	30	—	60	—	30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change, Whichever Occurs First[3]		0	—	0	—	0	—	0	—	ns

Notes:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. See Test Configurations, 3.3V Standard Test component values.
5. See Test Configurations, 5V High-Speed Test component values
6. See Test Configurations, 5V Standard Test component values.

AC WAVEFORMS FOR READ OPERATIONS



AC CHARACTERISTICS: $\overline{WE}$ CONTROLLED WRITE OPERATIONS[1], COMMERCIAL

		Product	-60					
		V_{CC}	3.3V ± 0.3V[9]		5V ± 10%[10]		5V ± 10%[10]	
		Load	50 pF		50 pF		100 pF	
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		110	—	60	—	70	—	ns
t_{PHWL}	$\overline{RP}$ Setup to $\overline{WE}$ Going Low		0.8	—	0.45	—	0.45	—	µs
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		0	—	0	—	0	—	ns
t_{PHHWH}	Boot Block Lock Setup to $\overline{WE}$ Going High[6,8]		200	—	100	—	100	—	ns
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High[5,8]		200	—	100	—	100	—	ns
t_{AVWH}	Address Setup to $\overline{WE}$ Going High[3]		90	—	50	—	50	—	ns
t_{DVWH}	Data Setup to $\overline{WE}$ Going High[4]		90	—	50	—	50	—	ns
t_{WLWH}	$\overline{WE}$ Pulse Width		90	—	50	—	50	—	ns
t_{WHDX}	Data Hold Time from $\overline{WE}$ High[4]		0	—	0	—	0	—	ns
t_{WHAX}	Address Hold Time from $\overline{WE}$ High[3]		0	—	0	—	0	—	ns
t_{WHEH}	$\overline{CE}$ Hold Time from $\overline{WE}$ High		0	—	0	—	0	—	ns
t_{WHWL}	$\overline{WE}$ Pulse Width High		20	—	10	—	20	—	ns
t_{WHQV}	Duration of Program[2,5]		6	—	6	—	6	—	µs
t_{WHQV}	Duration of Erase (Boot)[2,5,6]		0.3	—	0.3	—	0.3	—	s
t_{WHQV}	Duration of Erase (Parameter)[2,5]		0.3	—	0.3	—	0.3	—	s
t_{WHQV}	Duration of Erase (Main)[2,5]		0.6	—	0.6	—	0.6	—	s
t_{QWL}	V_{PP} Hold from Valid SRD[5,8]		0	—	0	—	0	—	ns
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD[6,8]		0	—	0	—	0	—	ns
t_{PHBR}	Boot-Block Lock Delay[7,8]		—	200	—	100	—	100	ns

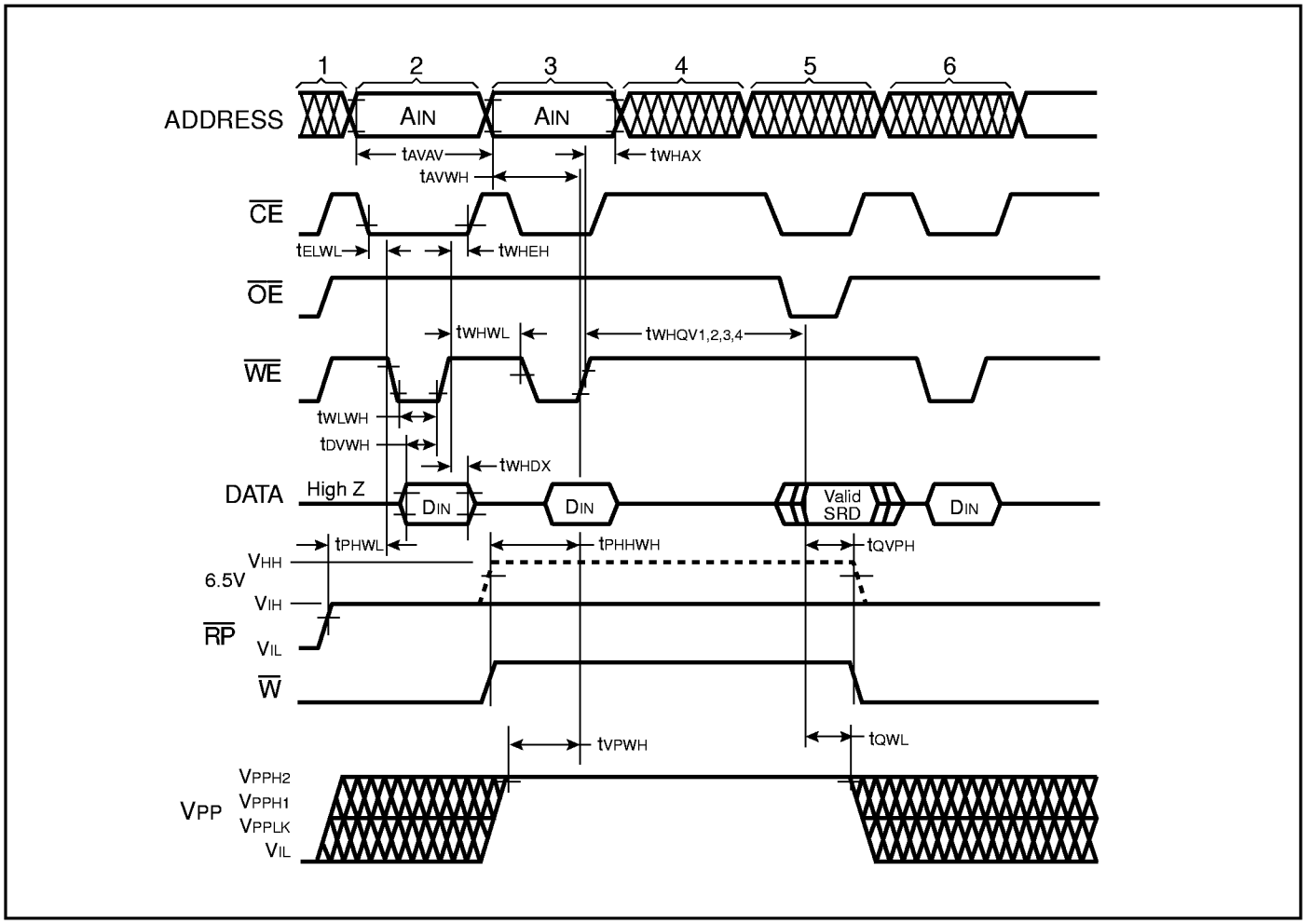
Notes:
1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC characteristics during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled intemally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, $\overline{RP}$ should be held at V_{HH} or $\overline{WP}$ should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful locking of the boot block.
8. Sampled, but not 100% tested.
9. See Test Configurations, 3.3V Standard Test component values.
10. See Test Configurations, 5V High-Speed Test component values.
11. See Test Configurations, 5V Standard Test component values.

AC CHARACTERISTICS: $\overline{WE}$ CONTROLLED WRITE OPERATIONS[1], COMMERCIAL (Cont.)

		Product	-80				-120				
		V_{CC}	3.3V ± 0.3V[4]		5V ± 10%[6]		3.3V ± 0.3V[4]		5V ± 10%[6]		
		Load	50 pF		100 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Read Cycle Time		150	—	80	—	180	—	120	—	ns
t_{PHWL}	$\overline{RP}$ Setup to $\overline{WE}$ Going Low		0.8	—	0.45	—	0.8	—	0.45	—	µs
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		0	—	0	—	0	—	0	—	ns
t_{PHHWH}	Boot Block Lock Setup to $\overline{WE}$ Going High[6,8]		200	—	100	—	200	—	100	—	ns
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High[5,8]		200	—	100	—	200	—	100	—	ns
t_{AVWH}	Address Setup to $\overline{WE}$ Going High[3]		120	—	50	—	150	—	50	—	ns
t_{DVWH}	Data Setup to $\overline{WE}$ Going High[4]		120	—	50	—	150	—	50	—	ns
t_{WLWH}	$\overline{WE}$ Pulse Width		120	—	50	—	150	—	50	—	ns
t_{WHDX}	Data Hold Time from $\overline{WE}$ High[4]		0	—	0	—	0	—	0	—	ns
t_{WHAX}	Address Hold Time from $\overline{WE}$ High[3]		0	—	0	—	0	—	0	—	ns
t_{WHEH}	$\overline{CE}$ Hold Time from $\overline{WE}$ High		0	—	0	—	0	—	0	—	ns
t_{WHWL}	$\overline{WE}$ Pulse Width High		30	—	30	—	30	—	30	—	ns
t_{WHQV1}	Program Time[2,5]		6	—	6	—	6	—	6	—	µs
t_{WHQV2}	Erase Duration (Boot)[2,5,6]		0.3	—	0.3	—	0.3	—	0.3	—	s
t_{WHQV3}	Erase Duration Parameter[2,5]		0.3	—	0.3	—	0.3	—	0.3	—	s
t_{WHQV4}	Erase Duration (Main)[2,5]		0.6	—	0.6	—	0.6	—	0.6	—	s
t_{QWL}	V_{PP} Hold from Valid SRD[5,8]		0	—	0	—	0	—	0	—	ns
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD[6,8]		0	—	0	—	0	—	0	—	ns
t_{PHBR}	Boot-Block Lock Delay[7,8]		—	200	—	100	—	200		100	ns

Notes:
1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC characteristics during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled intemally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, $\overline{RP}$ should be held at V_{HH} or $\overline{WP}$ should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful locking of the boot block.
8. Sampled, but not 100% tested.
9. See Test Configurations, 3.3V Standard Test component values.
10. See Test Configurations, 5V High-Speed Test component values.
11. See Test Configurations, 5V Standard Test component values.

AC WAVEFORMS FOR WRITE AND ERASE OPERATIONS ($\overline{WE}$ CONTROLLED WRITES)



AC CHARACTERISTICS: $\overline{CE}$ CONTROLLED WRITE OPERATIONS[1,12], COMMERCIAL

		Product	-60						
		Vcc	3.3V ± 0.3V[4]		5V ± 10%[5]		5V ± 10%[6]		
		Load	50 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		110	—	60	—	70	—	ns
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low		0.8	—	0.45	—	0.45	—	µs
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0	—	0	—	0	—	ns
t_{PHHEH}	Boot Block Lock Setup to $\overline{CE}$ Going High[6,8]		200	—	100	—	100	—	ns
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going High[5,8]		200	—	100	—	100	—	ns
t_{AVEH}	Address Setup to $\overline{CE}$ Going High[3]		90	—	50	—	50	—	ns
t_{DVEH}	Data Setup to $\overline{CE}$ Going High[4]		90	—	50	—	50	—	ns
t_{ELEH}	$\overline{CE}$ Pulse Width		90	—	50	—	50	—	ns
t_{EHDX}	Data Hold Time from $\overline{CE}$ High[4]		0	—	0	—	0	—	ns
t_{EHAX}	Address Hold Time from $\overline{CE}$ High[3]		0	—	0	—	0	—	ns
t_{EHWH}	$\overline{WE}$ Hold Time from $\overline{CE}$ High		0	—	0	—	0	—	ns
t_{EHEL}	$\overline{CE}$ Pulse Width High		20	—	10	—	20	—	ns
t_{EHQV1}	Duration of Programming Operation[2,5]		6	—	6	—	6	—	µs
t_{EHQV2}	Erase Duration (Boot)[2,5,6]		0.3	—	0.3	—	0.3	—	s
t_{EHQV3}	Erase Duration Parameter[2,5]		0.3	—	0.3	—	0.3	—	s
t_{EHQV4}	Erase Duration(Main)[2,5]		0.6	—	0.6	—	0.6	—	s
t_{QWL}	V_{PP} Hold from Valid SRD[5,8]		0	—	0	—	0	—	ns
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD[6,8]		0	—	0	—	0	—	ns
t_{PHBR}	Boot-Block Lock Delay[7,8]		—	200	—	100	—	100	ns

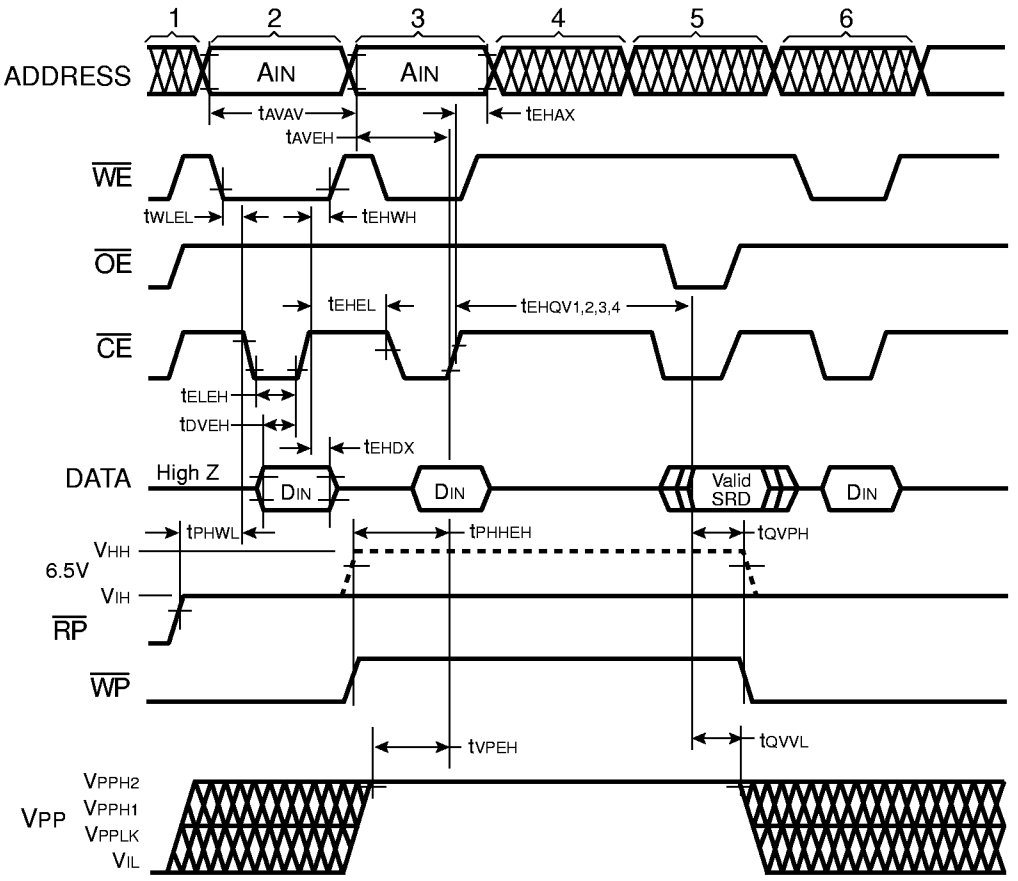
(continued)

AC CHARACTERISTICS: $\overline{CE}$ CONTROLLED WRITE OPERATIONS[1,12], COMMERCIAL (Cont.)

		Product	-80				-120				
		Vcc	3.3V ± 0.3V[4]		5V ± 10%[6]		3.3V ± 0.3V[4]		5V ± 10%[6]		
		Load	50 pF		100 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		150	—	80	—	180	—	120	—	ns
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low		0.8	—	0.45	—	0.8	—	0.45	—	µs
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0	—	0	—	0	—	0	—	ns
t_{PHHEH}	Boot Block Lock Setup to $\overline{CE}$ Going High[6,8]		200	—	100	—	200	—	100	—	ns
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going[5,8]		200	—	100	—	200	—	100	—	ns
t_{AVEH}	Address Setup to $\overline{CE}$ Going High [3]		120	—	50	—	150	—	50	—	ns
t_{DVEH}	Data Setup to $\overline{CE}$ Going High[4]		120	—	50	—	150	—	50	—	ns
t_{ELEH}	$\overline{CE}$ Pulse Width		120	—	50	—	150	—	50	—	ns
t_{EHDX}	Data Hold Time from $\overline{CE}$ High[4]		0	—	0	—	0	—	0	—	ns
t_{EHAX}	Address Hold Time from $\overline{CE}$ High[3]		0	—	0	—	0	—	0	—	ns
t_{EHWH}	$\overline{WE}$ Hold Time from $\overline{CE}$ High		0	—	0	—	0	—	0	—	ns
t_{EHEL}	$\overline{CE}$ Pulse Width High		30	—	30	—	30	—	30	—	ns
t_{EHQV1}	Duration of Programming Operation [2,5]		6	—	6	—	6	—	6	—	µs
t_{EHQV2}	Erase Duration (Boot)[2,5,6]		0.3	—	0.3	—	0.3	—	0.3	—	s
t_{EHQV3}	Erase Duration Parameter[2,5]		0.3	—	0.3	—	0.3	—	0.3	—	s
t_{EHQV4}	Erase Duration (Main)[2,5]		0.6	—	0.6	—	0.6	—	0.6	—	s
t_{QWL}	V_{PP} Hold from Valid SRD[5,8]		0	—	0	—	0	—	0	—	ns
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD[6,8]		0	—	0	—	0	—	0	—	ns
t_{PHBR}	Boot-Block Lock Delay[7,8]		—	200	—	100	—	200	—	100	ns

Notes:
See $\overline{WE}$ Controlled Write Operations for notes 1 through 11.
12. Chip Enable controlled writes: write operations are driven by the valid combination of $\overline{CE}$ and $\overline{WE}$ in systems where $\overline{CE}$ defines the write pulse-width (within a longer $\overline{WE}$ timing waveform), all setup, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.

ALTERNATE AC WAVEFORMS FOR WRITE AND ERASE OPERATIONS ($\overline{CE}$ CONTROLLED WRITES)



ERASE AND PROGRAM TIMINGS, COMMERCIAL (T_A = 0°C to +70°C)

	V_{PP}	5V ± 10%				12V ± 5%				
	V_{CC}	3.3V ± 0.3V		5V ± 10%		3.3V ± 0.3V		5V ± 10%		
Parameter		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Boot/Parameter Block Erase Time		0.84	7	0.8	7	0.44	7	0.34	7	s
Main Block Erase Time		2.4	14	1.9	14	1.3	14	1.1	14	s
Main Block Write Time (Byte Mode)		1.7	—	1.8	—	1.6	—	1.2	—	s
Write Time		10	—	10	—	8	—	8	—	µs

Notes:
1. All numbers are sampled, not 100% tested.
2. Maximum erase times are specified under worst case conditions. The maximum erase times are tested at the same value independent of V_{CC} and V_{PP}. See Note 3 for typical conditions.
3. Typical conditions are 25°C with V_{CC} and V_{PP} at the center of the specified voltage range. Production programming using V_{CC} = 5.0V, V_{PP} = 12.0V typically results in a 60% reduction in programming time.

INDUSTRIAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	–40	+85	°C
Vcc	Vcc Supply Voltage(2.7V)[1]	2.7	3.6	V
	Vcc Supply Voltage (3.3V ± 0.3V)[1]	3.0	3.6	V
	Vcc Supply Voltage (5V ± 10%)[2]	4.5	5.5	V

Notes:
1. AC specifications are valid at both voltage ranges. See DC Characteristics for voltage range-specific specifications.
2. 10% V_{CC} specifications apply to 80 and 120 ns versions in their standard test configuration.

Applying Vcc Voltages

When applying V_{CC} voltage to the device, a delay may be required before initiating device operation, depending on the Vcc ramp rate. If Vcc ramps slower than 1V/100 µs (0.01 V/µs) then no delay is required. If V_{CC} ramps faster than 1V/100 µs (0.01V/µs), then a delay of 2 µs required before initiating device opeation. $\overline{RP}$ = GND is recommended during power-up to protect against spurious write signals when V_{CC} is between V_{LKO} and V_{CCMIN}.

Vcc Ramp Rate	Required Timing
≤ 1V/100 µs	No delay required.
> 1V/100 µs	A delay time of 2 µs is required before any device operation is initiated, including read operations, command writes, program operations, and erase operations. This delay is measured beginning from the time V_{CC} reaches V_{CCMIN} (2.7V for 2.7V-3.6V operation, 3.0V for 3.3V ± 0.3V operation; and 4.5V for 5V operation).

Notes:
1. These requirements must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3V and 5V operation, the system should first transition V_{CC} from the existing voltage range to GND, and then to the new voltage. Any time the V_{CC} supply drops below V_{CCMIN}, the chip may be reset, aborting any operations pending or in progress.
3. These guidelines must be followed for any V_{CC} transition from GND.

DC CHARACTERISTICS, INDUSTRIAL TEMPERATURE

			Vcc	2.7V-3.6V 3.3V ± 0.3V		5V ± 10%		
Symbol	**Description**	**Test Conditions**		**Typ**	**Max**	**Typ**	**Max**	**Unit**
I_{IL}	Input Load Current[1]	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or GND		—	±1.0	—	±1.0	µA
I_{LO}	Output Leakage Current[1]	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or GND		—	±10	—	±10	µA
I_{CCS}	V_{CC} Standby Current[1,3]	**CMOS Levels**: V_{CC} = V_{CC} Max $\overline{CE}$ = $\overline{RP}$ = V_{CC} ± 0.2V		60	110	70	150	µA
		TTL Levels: V_{CC} = V_{CC} Max $\overline{CE}$ = $\overline{RP}$ = V_{IH}		0.4	1.5	0.8	2.5	mA
I_{CCD}	V_{CC} Deep Power-Down Current[1]	V_{CC} = V_{CC} Max V_{IN} = V_{CC} or GND $\overline{RP}$ = GND ± 0.2V		0.2	8	0.2	8	µA
I_{CCR}	V_{CC} Read Current[1,5,6]	**CMOS Inputs:** V_{CC} = V_{CC} Max $\overline{CE}$ = GND, $\overline{OE}$ = V_{CC}, f = 10 MHz (5V), 5 MHz (3.3V), I_{OUT} = 0 mA, Inputs = GND ± 0.2V or V_{CC} ± 0.2V		15	30	50	65	mA
		TTL Inputs: V_{CC} = V_{CC} Max $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 10 MHz (5V), 5 MHz (3.3V), I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH}		15	30	55	70	mA
I_{CCW}	V_{CC} Write Current[1,4]	V_{PP} = V_{PPH1} (at 5V) Write in Progress		13	30	30	50	mA
		V_{PP} = V_{PPH2} (at 12V) Write in Progress		10	25	30	45	mA
I_{CCE}	V_{CC} Erase Current[1,4]	V_{PP} = V_{PPH1} (at 5V) Erase in Progress		13	30	22	45	mA
		V_{PP} = V_{PPH2} (at 12V) Erase in Progress		10	25	18	40	mA
I_{CCES}	V_{CC} Erase Suspend Current[1,2]	$\overline{CE}$ = V_{IH}, V_{PP} = V_{PPH1} (at 5V) Block Erase Suspend		3	8.0	5	12.0	mA
I_{PPS}	V_{PP} Standby Current[1]	V_{PP} < V_{PPH2}		±5	±15	±5	±15	µA
I_{PPD}	V_{PP} Deep Power-Down Current[1]	$\overline{RP}$ = GND ± 0.2V		0.2	10	0.2	10	µA
I_{PPR}	V_{PP} Read Current[1]	V_{PP} ≤ V_{PPH2}		50	200	50	200	µA
I_{PPW}	V_{PP} Write Current[1,4]	V_{PP} = V_{PPH1} (at 5V) Write in Progress		13	30	13	30	mA
		V_{PP} = V_{PPH2} (at 12V) Write in Progress		8	25	8	25	mA
I_{PPE}	V_{PP} Erase Current[1,4]	V_{PP} = V_{PPH1} (at 5V) Block Erase in Progress		13	30	15	25	mA
		V_{PP} = V_{PPH2} (at 12V) Block Erase in Progress		8	25	10	20	mA
I_{PPES}	V_{PP} Erase Suspend Current[1]	V_{PP} = V_{PPH} Block Erase Suspend in Progress		50	200	50	200	µA

DC CHARACTERISTICS, INDUSTRIAL TEMPERATURE (Continued)

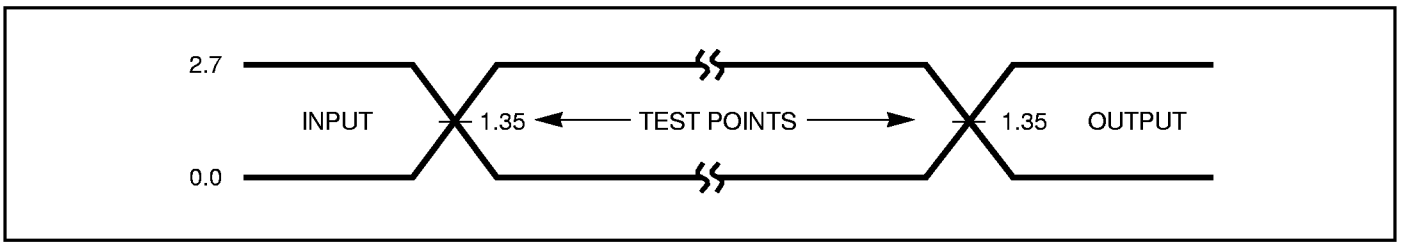
			Vcc	2.7V-3.6V 3.3V ± 0.3V		5V ± 10%		
Symbol	**Description**	**Test Conditions**		**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
$I_{\overline{RP}}$	$\overline{RP}$ Boot Block Unlock Current[1,4]	$\overline{RP} = V_{HH}$ $V_{PP} = 12V$		—	500	—	500	µA
I_{ID}	A9 Intelligent Identifier Current[1,4]	A9 = V_{ID}		—	500	—	500	µA
V_{ID}	A9 Intelligent Identifier Voltage			11.4	12.6	11.4	12.6	V
V_{IL}	Input Low Voltage			–0.5	0.8	–0.5	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 0.5 V	2	V_{CC} + 0.5V	V
V_{OL}	Output Low Voltage	$V_{CC} = V_{CC}$ Min. V_{PP} = 12V, I_{OL} = 5.8 mA (5V) 2 mA (3.3V), 2 mA (2.7V)		—	0.45	—	0.45	V
V_{OH1}	Output High Voltage (TTL)	$V_{CC} = V_{CC}$ Min. I_{OH} = –2.5 mA		2.4	—	2.4	—	V
V_{OH2}	Output High Voltage (CMOS)	$V_{CC} = V_{CC}$ Min. I_{OH} = –2.5 mA		0.85 x Vcc	—	0.85 x Vcc	—	V
		$V_{CC} = V_{CC}$ Min. I_{OH} = –100 µA		V_{CC} – 0.4V	—	V_{CC} – 0.4V	—	V
V_{PPLK}	V_{PP} Lock-Out Voltage[3]	Complete Write Protection		0	1.5	0	1.5	V
V_{PPH1}	V_{PP} (During Progam/Erase Operations)	V_{PP} at 5V		4.5	5.5	4.5	5.5	V
V_{PPH2}	V_{PP} (During Progam/Erase Operations)	V_{PP} at 12V		11.4	12.6	11.4	12.6	V
V_{LKO}	V_{CC} Erase/Write Lock Voltage[8]			2	—	2	—	V
V_{HH}	$\overline{RP}$ Unlock Voltage			11.4	12.6	11.4	12.6	V

CAPACITANCE (T_A = 25°C, f = 1 MHz)[4]

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	12	pF

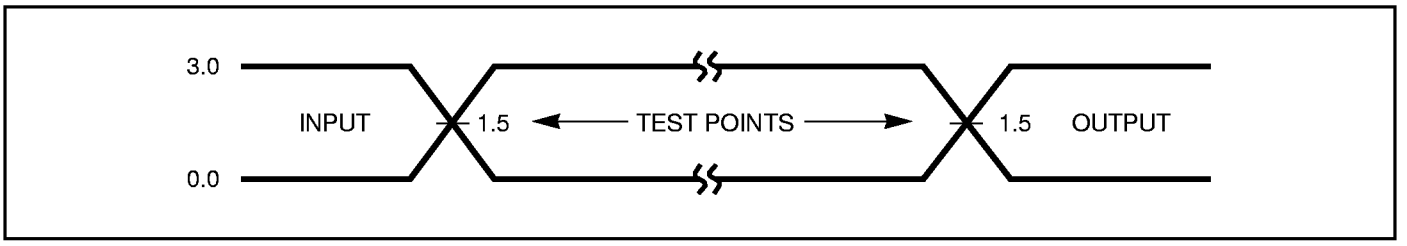
Notes:
1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, T_A = +25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCES} is specified with the device deselected. If the device is read while in erase suspend, current draw is the sum of I_{CCES} and I_{CCR}.
3. Block erases and byte writes are inhibited when $V_{PP} = V_{PPLK}$, and not guaranteed in the range between V_{PPH1} and V_{PPLK}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to less than 1 mA typical, in static operation.
6. CMOS Inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL Inputs are either V_{IL} or V_{IH}.
7. For the IS28F002B address pin A10 follows the C_{OUT} capacitance numbers.
8. For all BV/BLV parts, V_{LKO} = 2.0V for 2.7V, 3.3V, and 5V operations.

2.7V INPUT RANGE AND MEASUREMENT POINTS



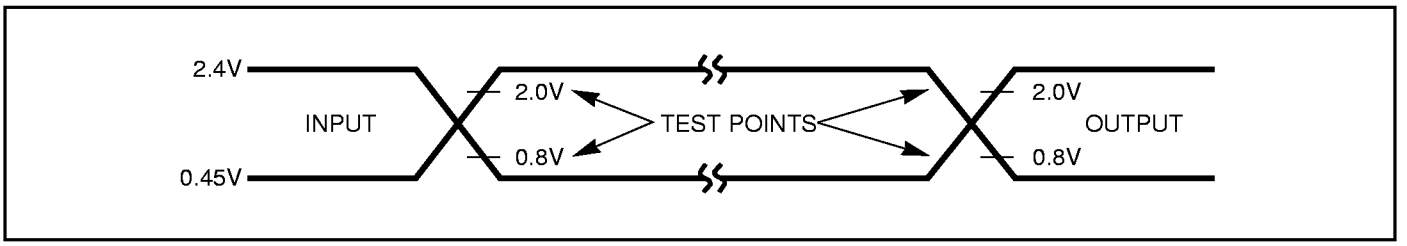
Note:
AC test inputs are driven at 2.7 for a logic "1"and 0.0V for a logic "0" Input timing begins and output timing ends at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

3.3V INPUT RANGE AND MEASUREMENT POINTS



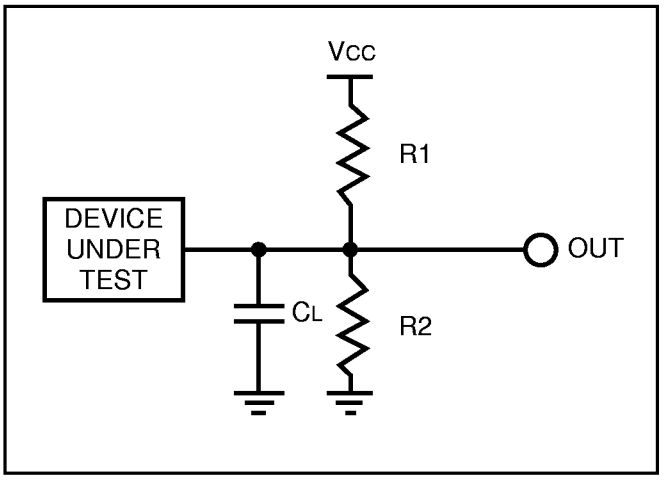
Note:
AC test inputs are driven at 3.0V for a logic land 0.0V for a logic “0.” Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

5V INPUT RANGE AND MEASUREMENT POINTS



Note:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

TEST CONFIGURATION



Note: See table for component values.

TEST CONFIGURATION COMPONENT VALUES

Test Configuration	C_L (pF)	R1 (Ω)	R2 (Ω)
2.7V Standard Test	50	888	845
3.3V Standard Test	50	989	773
5V Standard Test	100	585	394

Note: C_L includes jig capacitance.

AC CHARACTERISTICS
READ ONLY OPERATIONS[1], INDUSTRIAL TEMPERATURE

		Product	-80				-120				
		Vcc	3.3V ± 0.3V[5]		5V ± 10%[6]		2.7V-3.6V[5]		5V ± 10%[6]		
		Load	50 pF		100 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Read Cycle Time		110	—	80	—	120	—	80	—	ns
t_{AVQV}	Address to Output Delay		—	110	—	80	—	120	—	80	ns
t_{ELQV}	$\overline{CE}$ to Output Delay[2]		—	110	—	80	—	120	—	80	ns
t_{PHQV}	$\overline{RP}$ to Output Delay		—	0.8	—	0.45	—	0.8	—	0.45	µs
t_{GLQV}	$\overline{OE}$ to Output Delay[2]		—	65	—	40	—	65	—	40	ns
t_{ELQX}	$\overline{CE}$ to Output in Low Z[3]		0	—	0	—	0	—	0	—	ns
t_{EHQZ}	$\overline{CE}$ to Output in High Z[3]		—	55	—	30	—	55	—	30	ns
t_{GLQX}	$\overline{OE}$ to Output in Low Z[3]		0	—	0	—	0	—	0	—	ns
t_{GHQZ}	$\overline{OE}$ to Output in High Z[3]		—	45	—	30	—	55	—	30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change, Whichever Occurs First[3]		0	—	0	—	0	—	0	—	ns

Notes:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to t_{CE}–t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, but not 100% tested.
4. See Test Configurations, 2.7V-3.6V and 3.3V ± 0.3V Standard Test component values.
5. See Test Configurations, 5V Standard Test component values.

AC CHARACTERISTICS
WE CONTROLLED WRITE OPERATIONS(1), INDUSTRIAL TEMPERATURE

		Product	-80				-120				
		Vcc	3.3V ± 0.3V(9)		5V ± 10%(10)		2.7V-3.6V(9)		5V ± 10%(10)		
		Load	50 pF		100 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Unit
tAVAV	Write Cycle Time		110	—	80	—	120	—	120	—	ns
tPHWL	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low		0.8	—	0.45	—	0.8	—	0.45	—	µs
tELWL	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		0	—	0	—	0	—	0	—	ns
tPHHWH	Boot Block Lock Setup to $\overline{WE}$ Going High(6,8)		200	—	100	—	200	—	100	—	ns
tVPWH	VPP Setup to $\overline{WE}$ Going High(5,8)		200	—	100	—	200	—	100	—	ns
tAVWH	Address Setup to to $\overline{WE}$ Going Low(3)		90	—	60	—	90	—	60	—	ns
tDVWH	Data Setup to to $\overline{WE}$ Going Low(4)		90	—	60	—	90	—	60	—	ns
tWLWH	$\overline{WE}$ Pulse Width		90	—	60	—	90	—	60	—	ns
tWHDX	Data Hold Time to $\overline{WE}$ Going Low(4)		0	—	0	—	0	—	0	—	ns
tWHAX	Address Hold Time from $\overline{WE}$ High(3)		0	—	0	—	0	—	0	—	ns
tWHEH	$\overline{CE}$ Hold Time from $\overline{WE}$ High		0	—	0	—	0	—	0	—	ns
tWHWL	$\overline{WE}$ Pulse Width High		30	—	30	—	30	—	30	—	ns
tWHQV1	Program Time(2,5,8)		6	—	6	—	6	—	6	—	µs
tWHQV2	Erase Duration (Boot)(2,5,6,8)		0.3	—	0.3	—	0.3	—	0.3	—	s
tWHQV3	Erase Duration (Parameter)(2,5,8)		0.3	—	0.3	—	0.3	—	0.3	—	s
tWHQV4	Erase Duration (Main)(2,5,8)		0.6	—	0.6	—	0.6	—	0.6	—	s
tQWL	VPP Hold from Valid SRD(5,8)		0	—	0	—	0	—	0	—	ns
tQVPH	$\overline{RP}$ VHH Hold from Valid SRD (6,8)		0	—	0	—	0	—	0	—	ns
tPHBR	Boot-Block Lock Delay(7,8)		—	200	—	100	—	200	—	100	ns

Notes:
1. Read timing characteristics during write and erase operations are the same as during read-only operations. Refer to AC characteristics during read mode.
2. The on-chip WSM completely automates program/erase operations; program/erase algorithms are now controlled intemally which includes verify and margining operations.
3. Refer to command definition table for valid A_{IN}.
4. Refer to command definition table for valid D_{IN}.
5. Program/erase durations are measured to valid SRD data (successful operation, SR.7 = 1).
6. For boot block program/erase, $\overline{RP}$ should be held at V_{HH} or $\overline{WP}$ should be held at V_{IH} until operation completes successfully.
7. Time t_{PHBR} is required for successful locking of the boot block.
8. Sampled, but not 100% tested.
9. See Test Configurations, 2.7V-3.6V and 3.3V ± 0.3V Standard Test component values.
10. See Test Configurations, 5V Standard Test component values.

ERASE AND PROGRAM TIMINGS (INDUSTRIAL T_A = –40°C to +85°C)

	V_{PP}	5V ± 10%				12V ± 5%				
	V_{CC}	2.7V-3.6V 3.3 ± 0.3V		5V ± 10%		2.7V-3.6V 3.3 ± 0.3V		5V ± 10%		
Parameter		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Boot/Parameter Block Erase Time		0.84	7	0.8	7	0.44	7	0.34	7	s
Main Block Erase Time		2.4	14	1.9	14	1.3	14	1.1	14	s
Main Block Write Time (Byte Mode)		1.7	—	1.4	—	1.6	—	1.2	—	s
Write Time		10	—	10	—	8	—	8	—	µs

Notes:
1. All numbers are sampled, not 100% tested.
2. Maximum erase times are specified under worst case conditions. The maximum erase times are tested at the same value, independent of V_{CC} and V_{PP}. See Note 3 for typical conditions.
3. Typical conditions are 25°C with V_{CC} and V_{PP} at the center of the specifed voltage range. Production programming using V_{CC} = 5.0V, V_{PP} = 12.0V typically results in a 60% reduction in programming time.

AC CHARACTERISTICS
$\overline{CE}$ CONTROLLED WRITE OPERATIONS[1,11], INDUSTRIAL TEMPERATURE

		Product	-80				-120				
		V_{CC}	3.3V ± 0.3V[9]		5V ± 10%[10]		2.7V-3.6V[9]		5V ± 10%[10]		
		Load	50 pF		100 pF		50 pF		100 pF		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{AVAV}	Write Cycle Time		110	—	80	—	120	—	120	—	ns
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low		0.8	—	0.45	—	0.8	—	0.45	—	µs
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0	—	0	—	0	—	0	—	ns
t_{PHHEH}	Boot Block Lock Setup to $\overline{CE}$ Going High[6,8]		200	—	100	—	200	—	100	—	ns
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going High[5,8]		200	—	100	—	200	—	100	—	ns
t_{AVEH}	Address Setup to $\overline{CE}$ Going High		90	—	60	—	90	—	60	—	ns
t_{DVEH}	Data Setup to $\overline{CE}$ Going High[3]		90	—	60	—	90	—	60	—	ns
t_{ELEH}	$\overline{CE}$ Pulse Width[4]		90	—	60	—	90	—	60	—	ns
t_{EHDX}	Data Hold Time from $\overline{CE}$ High		0	—	0	—	0	—	0	—	ns
t_{EHAX}	Address Hold Time from $\overline{CE}$ High[4]		0	—	0	—	0	—	0	—	ns
t_{EHWH}	$\overline{WE}$ Hold Time from $\overline{CE}$ High[3]		0	—	0	—	0	—	0	—	ns
t_{EHEL}	$\overline{CE}$ Pulse Width High		30	—	30	—	30	—	30	—	ns
t_{EHQV1}	Program Time[2,5]		6	—	6	—	6	—	6	—	µs
t_{EHQV2}	Erase Duration (Boot)[2,5,6]		0.3	—	0.3	—	0.3	—	0.3	—	s
t_{EHQV3}	Erase Duration (Parameter)[2,5]		0.3	—	0.3	—	0.3	—	0.6	—	s
t_{EHQV4}	Erase Duration (Main)[2,5]		0.6	—	0.6	—	0.6	—	0.6	—	s
t_{QWL}	Hold from Valid SRD[5,8]		0	—	0	—	0	—	0	—	ns
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD[6,8]		0	—	0	—	0	—	0	—	ns
t_{PHBR}	Boot-Block Lock Delay[7,8]		—	200	—	100	—	200	—	100	ns

Notes:
See $\overline{WE}$ Controlled Write Operations for notes 1 through 10.
11. Chip Enable controlled writes: write operations are driven by the valid combination of $\overline{CE}$ and $\overline{WE}$ in systems where $\overline{CE}$ defines the write pulse-width (within a longer $\overline{WE}$ timing waveform), all setup, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

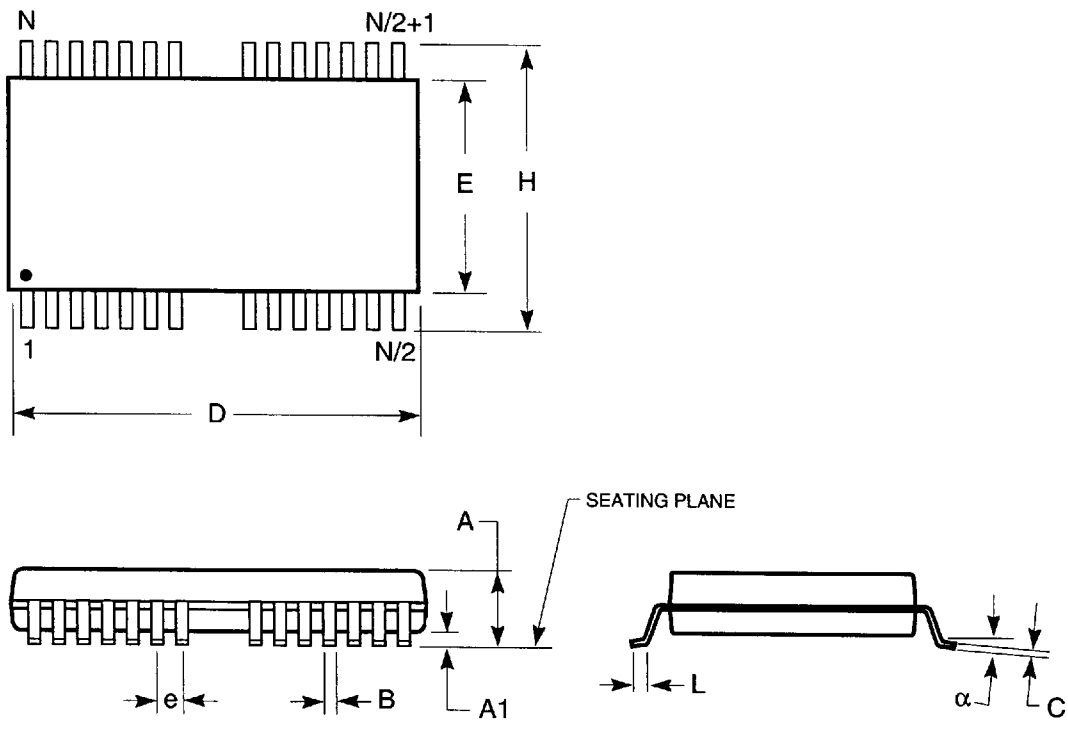
Speed (ns)	Order Part No.	Package
60	IS28F002BVB-60T	40-pin TSOP, Bottom Boot Block, V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V
60	IS28F002BVT-60T	40-pin TSOP, Top Boot Block, V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V
80	IS28F002BVB-80T	40-pin TSOP, Bottom Boot Block, V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V
80	IS28F002BVT-80T	40-pin TSOP, Top Boot Block, V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V
120	IS28F002BVB-120T	40-pin TSOP, Bottom Boot Block, V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V
120	IS28F002BVT-120T	40-pin TSOP, Top Boot Block, V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
80	IS28F002BVB-80TI	40-pin TSOP, Bottom Boot Block V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V
80	IS28F002BVT-80TI	40-pin TSOP, Top Boot Block V_{CC} = 3.3V or 5V, V_{PP} = 5V or 12V
120	IS28F002BLVB-120TI	40-pin TSOP, Bottom Boot Block V_{CC} = 2.7V or 5V, V_{PP} = 5V or 12V
120	IS28F002BLVT-120TI	40-pin TSOP, Top Boot Block V_{CC} = 2.7V or 5V, V_{PP} = 5V or 12V

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Fax: (408) 588-0802
Toll Free: 1-800-379-4774
http://www.issiusa.com

Plastic TSOP
Package Code: T (Type II)



Plastic TSOP (T - Type II)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
N	40/44			
A	1.00	1.20	0.039	0.047
A1	0.05	0.20	0.002	0.008
B	0.30	0.40	0.012	0.016
C	0.12	0.21	0.0047	0.0083
D	18.313	18.517	0.721	0.729
E	10.058	10.262	0.396	0.404
e	0.800 BSC		0.0315 BSC	
H	11.735	11.938	0.462	0.470
L	0.432	0.584	0.017	0.023
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.